

# Attenuation of Conducted EMI for Three-Level Inverters Through PWM

Jianan Chen, Dong Jiang, and Qiao Li

**Abstract**—This paper presents two typical modulations to reduce conducted electromagnetic interference (EMI) for three-level voltage-source inverters. The first modulation called variable switching frequency pulse-width modulation (VSFPWM) based on real-time current ripple prediction is used to reduce differential-mode (DM) EMI noise. This technique can make conducted EMI between kHz and MHz achieve great attenuation. The other method named zero common-mode (CM) PWM is used to decrease CM voltage and current. A comprehensive analysis and comparison between normal SVPWM and zero-CM PWM state that zero-CM PWM pays the prices of higher Total Harmonic Distortion (THD), serious neutral voltage unbalance, more switching loss and lower modulation index to achieve theoretical elimination of CM voltage. Then, combination of VSFPWM and zero-CM modulation is designed to avoid the disadvantages such as large switching loss produced by zero-CM PWM, and the new method has obvious predominance of reducing conducted EMI noise. Relevant experimental results validate the advantages of these modulations.

**Index Terms**—Conducted EMI, three-level inverters, variable switching frequency PWM, zero-CM PWM.

## I. INTRODUCTION

THREE-PHASE voltage-source-inverter (VSI) with pulse-width modulation (PWM) is one of the most widely used topologies for high power applications. With requirements for higher power and voltage rating as well as lower harmonics, multilevel VSI has its advantages over regular two-level VSI [1], [2]. Three-level neutral point clamped (NPC) inverter is a typical multilevel inverter and has been applied to high power applications in industrial fields, such as photovoltaic inverter power system, medium-voltage drive system, uninterrupted power system (UPS) and high voltage direct current transmission (HVDC) [3], [4].

PWM is the key technology for VSI regardless of application scenarios [5]–[7]. However, PWM can also bring three major by-products for the inverter. Firstly, the switching losses of power electronics devices will dramatically accumulate, accompanied by high switching frequency; secondly, the switching actions will generate current ripple for the inverter; finally yet importantly, PWM will generate electromagnetic interference (EMI) noise source, including differential-mode (DM) EMI

and common-mode (CM) EMI. High-frequency harmonics in line-to-line, the typical representative for DM EMI, is capable of polluting power grid to make other electric equipment in an unsafe operating state and malfunction for microprocessors or automatic protective devices. Whereas, common-mode noise means the EMI noise conducted in the same direction together in the transmission line, which is usually representing as high frequency CM voltage. For motor drive applications, discharge current caused by CM voltage with high  $dv/dt$  will impair bearing and destroy the reliability of electrical machine. Therefore, the wide applications of PWM have put forward urgent requirements for EMI reduction [8]–[9].

With the requirement of EMI noise reduction, much research have been carried out in recent decades. The major approach of EMI mitigation in power electronics system is through two ways: the first is to block the EMI propagation path; the second is to mitigate the noise source. The first way is mainly through the design of EMI filter, which requires extra components to attenuate EMI before conducting into the objective [10]–[12]. Without applying extra filter, EMI can also be attenuated directly in the noise source: the switching pattern of power electronics inverters. For the noise source shaping, the high frequency EMI is mainly caused by the device switching pattern and is usually shaped through power electronics device and gate drivers [13], [14]. However, for the EMI spectrum between kHz and MHz range, the noise source is mainly determined by the pulse series. For this range, the shaping of EMI noise is mainly through converter topology and modulation schemes. For three-level inverter, the modulation freedom is more complicated than regular two-level inverter and is worthy with deep analysis, which is the major topic in this paper.

Many efforts have been made to develop novel PWM methods to reduce EMI noises. One typical approach is utilizing the freedom of switching frequency, which is variable switching frequency PWM (VSFPWM) [15]–[18]. Based on the current ripple prediction model for two-level VSI, switching frequency is controlled to meet the current ripple peak value requirement. Compared with regular constant switching frequency PWM (CSFPWM), VSFPWM can reduce switching losses and EMI noise peak and keep the same current ripple peak value. For three-level VSI, [19] has studied the current ripple through space vector analysis. Nevertheless, it is much complicated and VSFPWM has not been implemented for three-level inverters.

CM noise source is CM voltage, so the way to reducing CM noise is to re-shape output voltage pulses. However, PWM in widely used two-level inverter is only with capability to reduce the CM voltage amplitude but not eliminate CM voltage theo-

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The authors are with Huazhong University of Science and Technology, Wuhan, China (e-mail: chen\_jianan@hust.edu.cn; jiangd@hust.edu.cn; liqiao@hust.edu.cn).

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retically since the phase voltage is either positive or negative in two-level inverter and ‘three’ is an odd number. Three-level inverter is able to reduce or even eliminate CM voltage theoretically since the phase voltage is with positive, negative or zero. [20]-[21] have studied the advanced modulation for CM voltage elimination, but the method is at the price of lower utilization of DC voltage and bigger switching losses. [22]-[23] have done research on the way to reduce CM voltage, whose effect on CM mitigation is not so good as zero-CM whereas the modulation index can still reach to 1.15 and even have lower switching losses in respect to normal SVPWM. Reference [24] has in-depth compared the EMI performance between two above-mentioned methods and normal space vector pulse-width modulation (SVPWM), which provides some useful information to roundly understand CM conducted EMI. Nevertheless, little subject matter literature introduce ideas to improve these methods.

Modeling and analysis of VSFPWM for two-level inverters with modulation have been done well. However, the study for three-level inverter is not sufficient since the modulation freedom is more and complicated to utilize. Based on the previous work of EMI reduction through modulation, this paper will introduce a general current ripple prediction method for three-level VSI with carrier-based PWM approach, and implement it into VSFPWM for three-level inverters in part II. The zero-CM modulation has been proposed for many year, whereas little literatures thoroughly research the equivalent relationship between space vector modulation and carrier based modulation of zero-CM PWM, which are presented in part III together with comprehensive comparison between normal SVPWM and zero-CM PWM. In addition, the combination of VSFPWM and zero-CM designed together to help improve the performance of zero-CM methods are introduced in part IV. Conclusions are summarized in part V.

## II. DIFFERENTIAL-MODE CONDUCTED EMI REDUCTION

For the modulation based optimization of DM EMI noise, the major approach is making the switching frequency vary, which can re-distribute the EMI noise from concentrating near the harmonics of constant switching frequency to a wide range in frequency domain. Then the EMI noise peak can be reduced. Previous study of so called ‘random PWM’ that changes the switching frequency randomly is highly depending on the statistic effect, and cannot control the current ripple and power losses [25], [26]. Based on the model predictive VSFPWM in two-level VSI [17], [18], this part will introduce the current ripple prediction model and model predictive VSFPWM for three-level inverter to reduce conducted EMI.

### A. Current Ripple Prediction Model

Fig. 1 shows the topology of three-level NPC inverter. The three terminals ( $A$ ,  $B$ , and  $C$ ) are switching with voltage of  $V_{dc}/2$ ,  $0$ , and  $-V_{dc}/2$  referring to the DC neutral point  $O_1$ . The load is representing general AC load, including inductors and balanced three-phase voltage sources. The AC voltage source can represent motor back-EMF for motor drive application

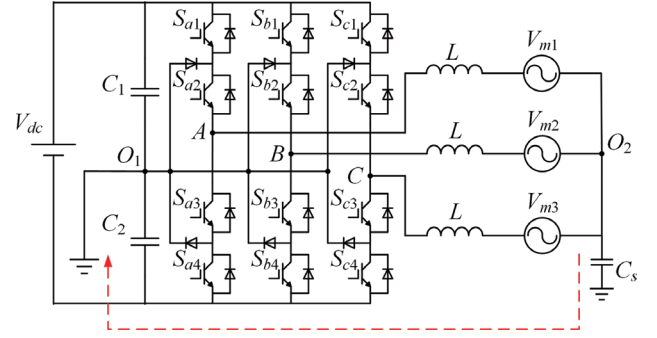


Fig. 1. Topology of three-level NPC inverter.



Fig. 2. Experimental platform.

or grid voltage for grid application. The voltage produced by inverter is rectangular pulse series whereas the terminal voltage of load is sinusoidal waveform, so their voltage difference imposed on inductance will result in affluent high frequency current ripple. According to three-level schematic diagram in Fig. 1, experimental platform is set up as shown in Fig. 2. The  $10\ \Omega$  resistor in parallel with  $35\ \mu\text{F}$  capacitor is capable of representing three-phase balanced voltage [15]. Inductors with  $0.5\ \text{mH}$  connect inverter and three-phase voltage source to sustain the voltage difference.

Fig. 3 shows the phase currents and their  $50\ \text{Hz}$  fundamental component achieved by FFT analysis, which are the experimental results of the modulation with constant switching frequency called normal SVPWM. The experimental condition are with  $270\ \text{V}$  DC bus voltage,  $20\ \text{kHz}$  switching frequency, and modulation index of  $0.85$ . These experiment parameters and condition mentioned above summarized in TABLE I will be applied to all experiments in this paper.

Obvious ripple can be found in the phase current, which is caused by switching events and is synchronous with PWM signals. Fig. 4 shows the three-phase output voltage together with phase-A current ripple during one switching cycle. The current ripple is following the switching actions of the three-phase rectangular pulse voltage. In addition, the variation of current ripple between each two adjacent switching actions is linear,

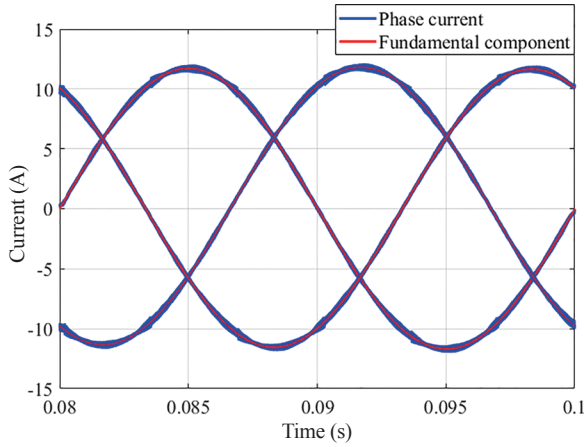


Fig. 3. Phase current and fundamental value of SVPWM (experimental result).

TABLE I  
EXPERIMENTAL PARAMETERS AND CONDITION

Symbol	Parameters	Value
$V_{dc}$	DC voltage	270 V
$C_1/C_2$	DC side capacitance	470 $\mu$ F
$m$	modulation index	0.85-1.00
$f_s$	constant switching frequency	20 kHz
$f_0$	fundamental frequency	50 Hz
$L$	filtering inductance	0.5 mH
$R$	load resistance	10 $\Omega$
$C$	load capacitance	35 $\mu$ F
$C_s$	parasitic capacitance for CM loop	10 nF
$P$	power	2.0 kW-2.8 kW

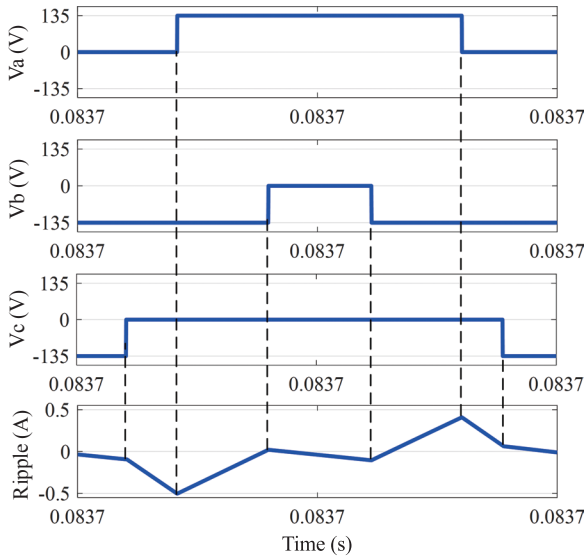


Fig. 4. Output voltage and current ripple during one switching cycle (simulation results).

which is the basic precondition for current ripple prediction. Nevertheless, three-level inverter's output voltage is switching between  $V_{dc}/2$  and 0, or 0 and  $-V_{dc}/2$ , not between  $V_{dc}/2$  and  $-V_{dc}/2$ , which is different from the current ripple generation in

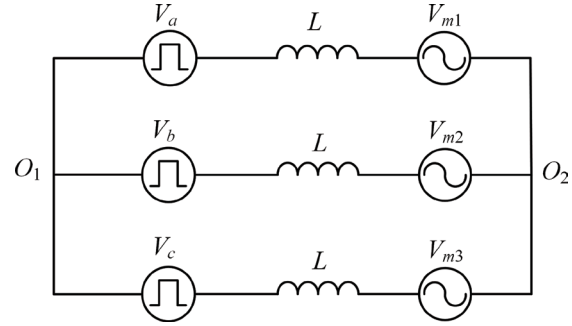


Fig. 5. Equivalent circuit for ripple prediction.

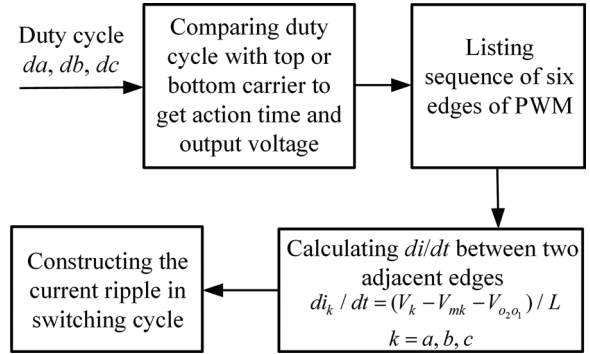


Fig. 6. Current ripple prediction diagram.

two-level VSI in [15]–[18]. Then, the switching voltage model should be re-constructed to predict current ripple.

SVPWM, a rather complicated modulation for multilevel converters, is still considered as the most useful technique for power electronics converters. Owing to equivalent theory [27], carrier-based PWM could replace SVPWM to simplify the modulation and obtain the same performance for multilevel converters. Therefore, this paper implement the modulation SVPWM with carrier-based PWM equivalently, rather than the complicated process of the vector synthesis with 27 space vectors for three-level inverters.

For the carrier-based PWM analysis of three-level inverters, there are two carriers in the modulator to compare with the reference value. Top carrier is used to generate output voltage of  $V_{dc}/2$  and 0, the bottom carrier is for 0 and  $-V_{dc}/2$ . Then, the output voltage and action time in each switching cycle can be determined. With the output voltage model, the current ripple can be derived through the equivalent circuit in Fig. 5 [17], which is the equivalent model of Fig. 1. In each switching cycle, the pulse voltage sources ( $V_a$ ,  $V_b$ ,  $V_c$ ) are determined by comparison between the duty cycles and carrier, the balanced three-phase load average voltage ( $V_{m1}$ ,  $V_{m2}$ ,  $V_{m3}$ ) are supposed to be constant value in a switching cycle) are directly determined by duty cycles. With the output voltage and action time, the current ripple can be predicted [28].

The current ripple prediction diagram is shown in Fig. 6. The duty cycles from the controller are the input. In each switching cycle, by comparing the duty cycles with the top and bottom carrier in the three-level inverter modulator, the action time for three phases will be determined as well as the terminal voltage.



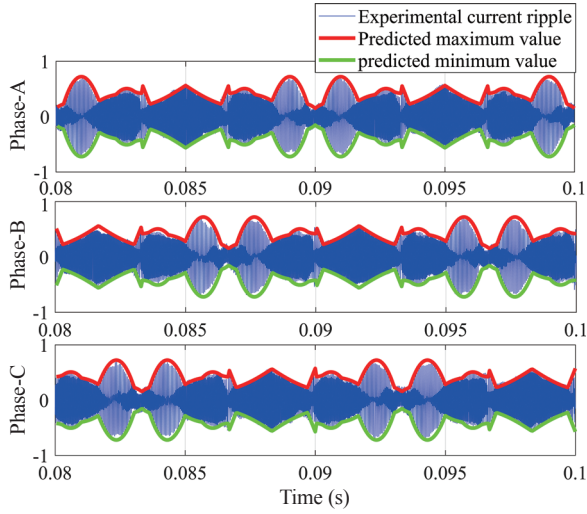


Fig. 7. Current ripple comparison between experiment and prediction (Normal SVPWM).

Then, by listing the six edges (three rising edges and three falling edges) in the switching cycle, the action time and output voltage between each two adjacent edges can be determined. With the equivalent model in Fig. 5, the  $di/dt$  between each two adjacent edges can also be calculated. With the  $di/dt$  and action time  $\Delta t$  between each two adjacent edges, the current ripple in the full switching cycle can be predicted.

Fig. 7 shows the comparison of current ripple between experiment and prediction for all three phases. The predicted current of maximum and minimum value in each switching cycle are matching well with the experimental current ripple. The experimental results indicate that the prediction model is effective and possesses real-time prediction capability.

### B. Variable Switching Frequency PWM

The variable switching frequency PWM (VSFPWM) for three-level inverter is similar with the structure of VSFPWM for two-level VSC in [18]. The VSFPWM diagram is shown in Fig. 8. Duty cycle references ( $da$ ,  $db$ ,  $dc$ ) are generated from controller. They are sent to the ripple prediction module, the predicted current ripple is calculated and sent to the switching period generation block. The generated triangle carriers with variable frequency (top and bottom) are used to compare with duty cycles and generate the gate drive signals for the power devices in the three-level VSI. At the same time, the variable switching frequency sampler is generated to the controller for control.

The core for the VSFPWM algorithm is the switching period calculation module. With the real-time prediction of current ripple in each switching cycle, the maximum ripple current in three phases with nominal switching cycle  $T_{sN}$  is calculated. The updated switching cycle  $T_s$  is calculated in (1). The updated switching period will control the maximum current ripple to be equal to the ripple requirement in each switching cycle.

$$T_s = T_{sN} \times \frac{I_{ripple\_require}}{I_{ripple\_max}} \quad (1)$$

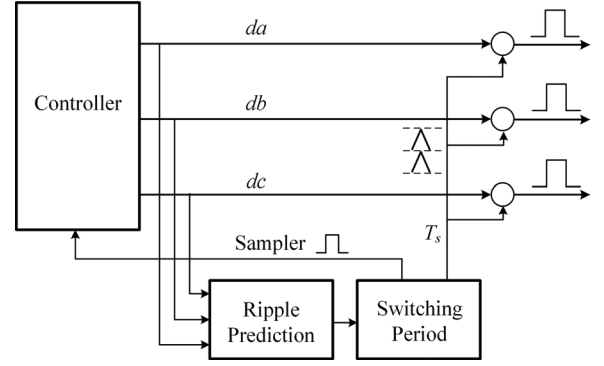


Fig. 8. Structure of VSFPWM generation.

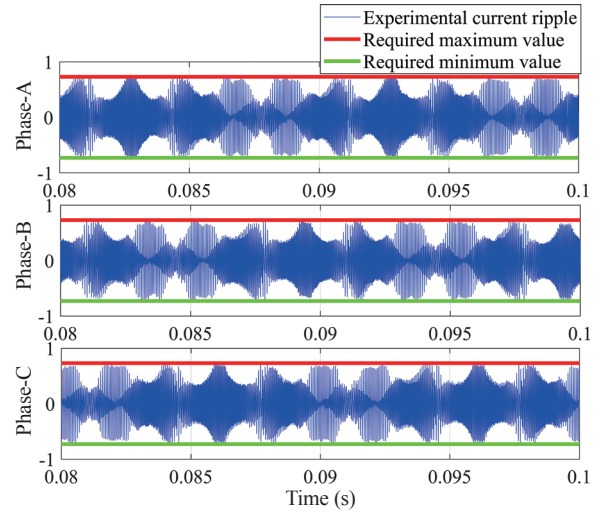


Fig. 9. Three-phase current ripple of VSFPWM (experimental result).

Compared with the model predictive VSFPWM in two-level inverter discussed in [15]–[18], the basic principle of VSFPWM in three-level inverter is similar: actively adjusting the switching frequency in each cycle to control the maximum current ripple clamped to the required value. The major difference for three-level inverter is double carrier, which makes prediction model more complicated than two-level. Because the variation range of current ripple in three-level inverter is big, there is a big range for switching frequency variation.

### C. Experimental Results for Three-Level VSFPWM

In order to verify the variable switching frequency methods proposed in previous parts, the experiments have been implemented in a three-phase PWM three-level NPC inverter connected to the  $L$ - $R$ - $C$  load shown in Fig. 2. Three-phase currents are measured by high precision current probes and recorded as data. With FFT analysis of the current data, fundamental current and plenty of harmonics components can be re-constructed. By subtracting the fundamental component from three-phase full current, current ripple of VSFPWM is obtained in Fig. 9. Compared with ripple in Fig. 7 for normal SVPWM, the VSFPWM has better effective utilization rate of space limited by the identical required current peak value ( $\pm 0.73$  A) apparently.

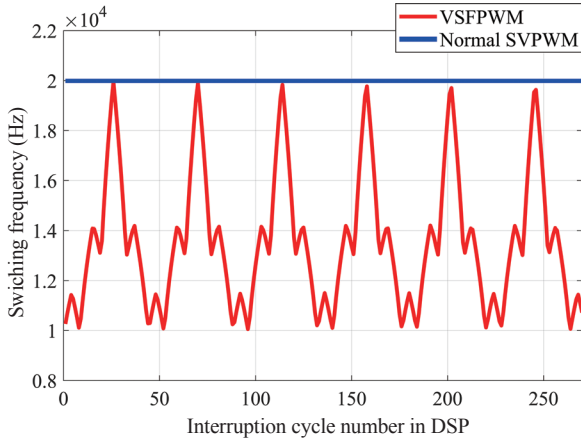


Fig. 10. Switching frequency variation of VSFPWM (experimental result).

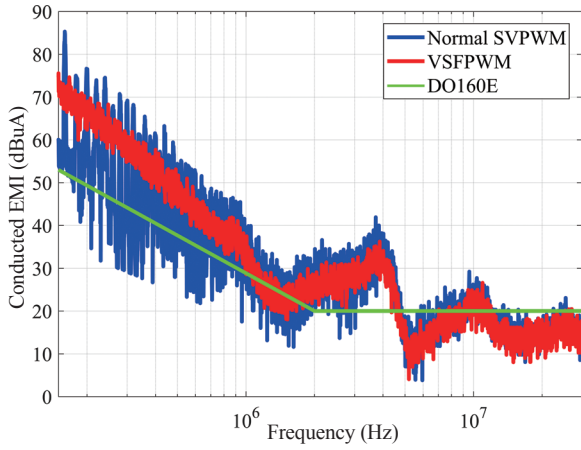


Fig. 11. Comparison of conducted EMI: VSFPWM and normal SVPWM (experimental result).

According to (1), the maximum current ripple of three-phase in carrier period and the required limitation of ripple determine the variation range of frequency. In Fig. 7, it is clear that the maximum ripple is not always clamped to required value (0.73A) when normal SVPWM is applied. Nevertheless, the VSFPWM methods can make the maximum ripple equal to required value in every switching cycle as shown in Fig. 9. Fig. 10 shows the switching frequency of VSFPWM, which is acquired from the register of DSP. Its switching frequency varies in a wide range from 10 kHz to 20 kHz other than being fixed at a constant switching frequency (20 kHz), leading to a large reduction in switching loss. The reason for reducing switching loss is that the average switching frequency related to switching loss and efficiency has reduced significantly with respect to the normal SVPWM (20 kHz).

DM conducted EMI of two cases are compared in Fig. 11 with frequency range from 150 kHz to 30 MHz measured by EMI test receiver, which adheres to the narrowband standard DO-160E. EMI noise energy spread into a broad range, which makes the peak value obviously smaller than normal SVPWM. The EMI peak value could nearly reduce 10 dB around the carrier harmonics. The limit of EMC standard is also plot in Fig. 11

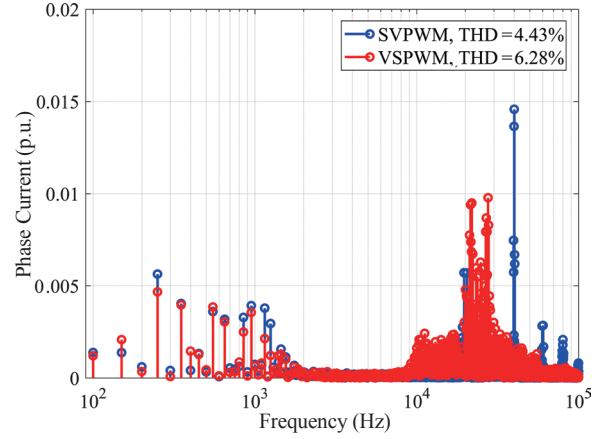


Fig. 12. Comparison of phase current spectrum: VSFPWM and normal SVPWM (experimental result).

where the green line is. Although the advanced modulation can make conducted EMI achieve great attenuation, the EMI filter is also need to satisfy the EMI requirement. However, reduction of EMI noise can increase cut-off frequency and decrease migration requirement for EMI filter, which could reduce the volume and weight of the passive components, finally increase the power density of whole system.

The variable frequency methods will have impact on the low frequency harmonics and the THD of the output currents. The THD increases from 4.43% to 6.28% after applying variable switching frequency method into normal SVPWM. The reason for the increase of THD is obvious that the switching frequency is keeping smaller than 20 kHz and resulting the current ripple bigger. Fig. 12 shows the current spectrum comparison between VSFPWM and normal SVPWM. Compared with normal SVPWM, VSFPWM not only spreads the spectrum around carrier harmonics, but also has little impact on low frequency harmonics.

### III. COMMON-MODE VOLTAGE REDUCTION

#### A. Review of Zero Common-Mode Modulation

The common-mode voltage elimination technology, is the predominance of multilevel converters, has been proposed for many years [20]. Common-mode voltage of three-phase converter can be calculated as (2).

$$V_{CM} = \frac{V_{AO1} + V_{BO1} + V_{CO1}}{3} \quad (2)$$

There are 27 switching sequences for three-level inverters shown in Fig. 13. According to (2), different space vectors produces different common-mode voltage between AC neutral point and DC side. However, among the 27 space vectors, only the six medium vectors and one zero vector (ooo) is able to realize zero CM voltage output to decrease CM current that is the typical representative of CM conducted EMI. Fig. 1 shows CM loop and CM current  $i_{cm}$  in red dotted line, the CM current flows through stray capacitors and ground. The basic method

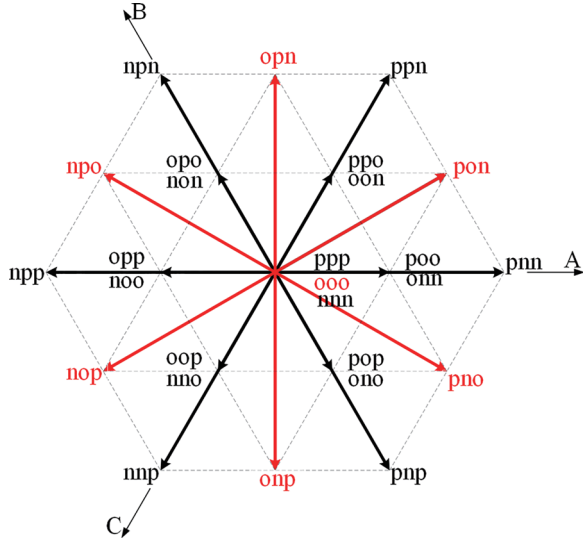


Fig. 13. Space vector map for three-level topology.

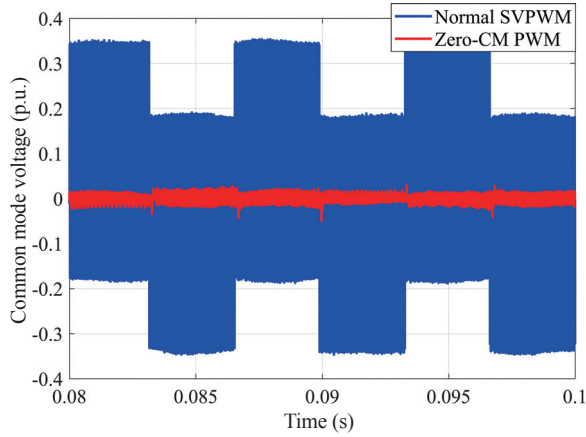


Fig. 14. CM voltage comparison between zero-CM PWM and normal SVPWM (experimental result).

for three-level to eliminate CM voltage is utilizing the seven vectors (the red vector in Fig. 13) to combine the rotary vector. It is obvious that this vector space with six effective vectors is similar to two-level, so its procedure of synthesizing reference vector can imitate the SVPWM of two-level converters.

Fig. 14 shows the experimental results of zero-CM modulation in comparison with normal SVPWM for three-level inverters concerning CM voltage. It can be observed that the zero-CM modulation could decrease common-mode voltage greatly compared with conventional SVPWM. The CM voltage nearly reduces to zero with common-mode elimination algorithm; consequently, weakening the source of CM conducted EMI.

The DC bus neutral point is connected to AC neutral point by capacitance with 10nF, which is designed to simulate stray capacitor of CM loop and conduct CM current. Fig. 15 is the CM current waveform comparison of the two modulations. CM current peak value of SVPWM nearly reach 800 mA, but the zero-CM PWM only with 150 mA. It is worth mentioning

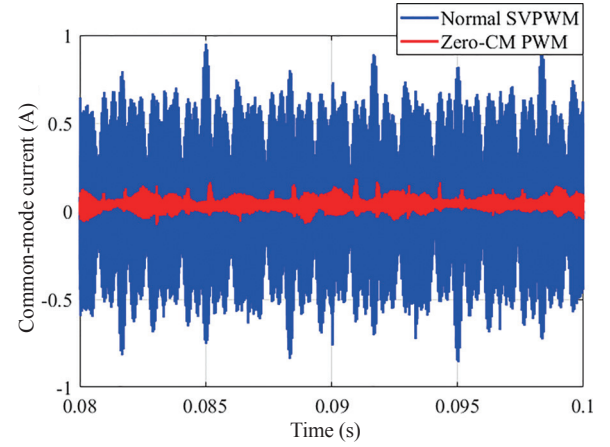


Fig. 15. CM current comparison between zero-CM PWM and normal SVPWM (experimental result).

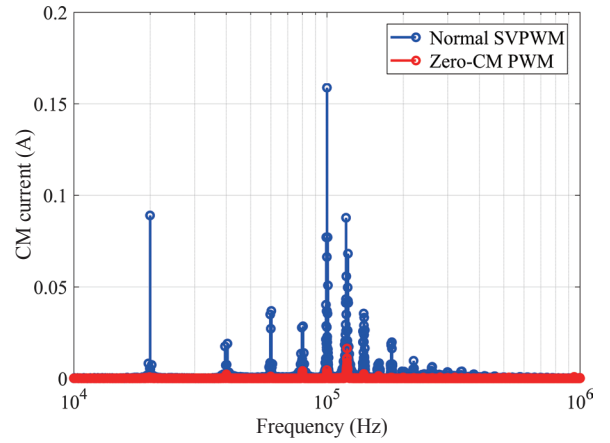


Fig. 16. Comparison of common-mode current spectrum: zero-CM PWM and normal SVPWM (experimental result).

that non-ideal factors such as dead time and switching transient greatly affect the performance of CM elimination [21].

Fig. 16 is the CM current spectrum of two methods between 10 kHz and 1 MHz. As expected, the main harmonic component have decreased largely. For example, the biggest harmonic with 100 kHz can fall from 0.16 A to 0.005 A. Fig. 17 exhibits experimental frequency spectrum of CM current EMI. It is apparent that CM current EMI peak value can attenuate 15 dB during wide range of frequency spectrum (150 kHz-1 MHz), some points such as 180 kHz even more than 20dB. The experimental results indicate that zero-CM modulation succeeds in restraining CM voltage and current.

### B. Analysis of Zero Common-Mode Modulation

Three-level inverter may effectively suppress CM noise whereas several problems still exist in zero-CM modulation. Firstly, THD increases under the circumstance of zero-CM modulation. Fig. 18 and Fig. 19 show the phase current waveforms and spectrums comparison respectively: blue waveform is the phase current and corresponding spectrum of conventional SVPWM with THD of 4.43%; the red one is zero-CM PWM

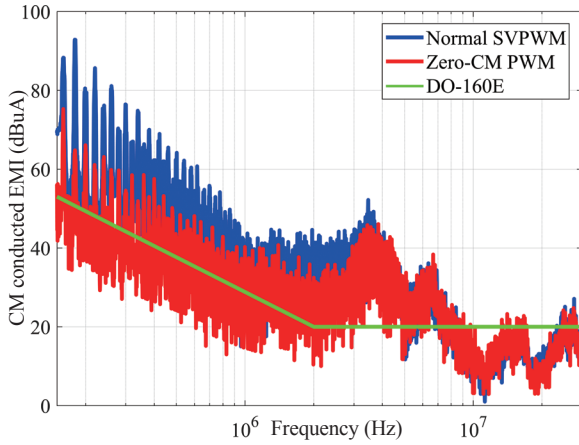


Fig. 17. CM Conducted EMI comparison between zero-CM PWM and SVPWM (experimental result).

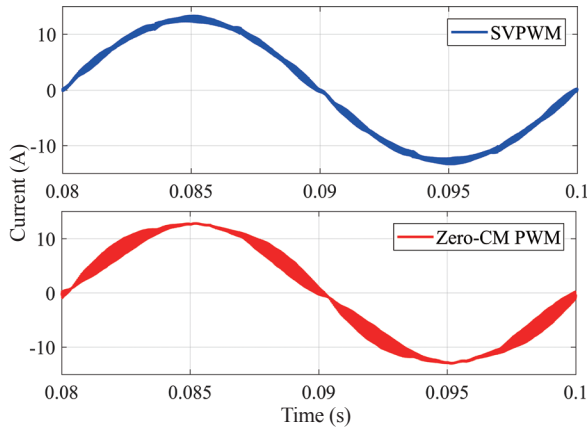


Fig. 18. Phase current comparison between normal SVPWM and zero-CM PWM.

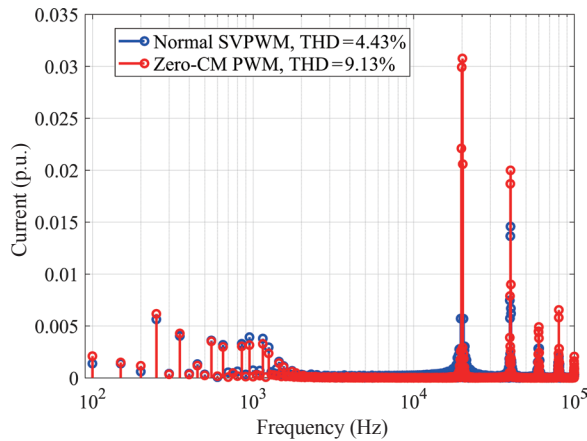


Fig. 19. Comparison of phase current spectrum: zero-CM PWM and normal SVPWM (experimental result).

with THD of 9.13%. Zero-CM modulation largely increases current ripple, whereas the current quality is acceptable with the experimental condition. Fig. 20(a) reveals the reference vector combination of normal SVPWM, and Fig. 20(b) depicts the process of vectors synthesis for zero-CM modulation, which

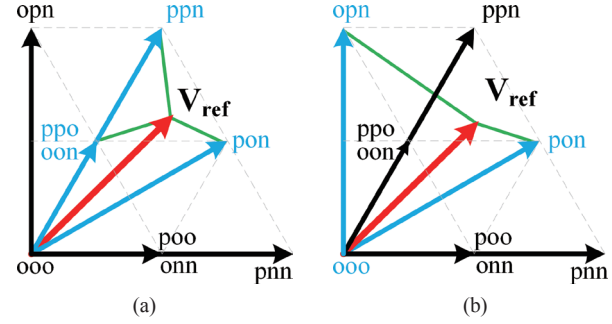


Fig. 20. Output voltage vectors combination comparison. (a) Normal SVPWM. (b) Zero-CM PWM.

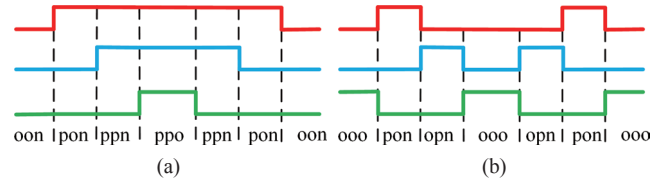


Fig. 21. Switching sequence combination comparison. (a) Normal SVPWM. (b) Zero-CM PWM.

chooses farther vector (opn) rather than the nearest one (oon or ppo) to synthesis the reference voltage vector. The reason for choosing farther vector in Fig. 20(b) is to eliminate CM voltage, but it will increase the voltage difference from the reference voltage and generate bigger current ripple. Then, the novel modulation loses the advantage of three-level such as lower harmonics for abandoning using the affluent vectors.

Secondly, switching loss is twice of the conventional SVPWM. For instance, Fig. 21 shows the switching sequence of reference vector in Fig. 20. There are four switching events during one switching period, which is twice of traditional SVPWM. Therefore, the switching loss of zero-CM PWM has doubled.

What's more, utilization of DC voltage is reduced to 0.866 while normal SVPWM is 1. The reason is that the combination does not select large vector and the length of reference vector bigger than 0.866 of DC voltage fails to combine.

Another important issue for three-level NPC inverter is neutral point voltage balancing. Large voltage vectors and zero vectors will not influence neutral point voltage since no phase is connected to neutral point [29]. Medium voltage vectors are not good choices for neutral point voltage balancing. Full load current is connected to the neutral point for the duration of the medium vector duty cycle and will cause low frequency neutral point voltage. Small voltage vectors appear in pairs for each identical vector. The two small vectors in each pair will provide exact opposite load current to the neutral point and can be used as a freedom to control the neutral point voltage balancing. For zero-CM PWM, only medium voltage vectors (and zero vector) are used and no small voltage vector can be used to help the balancing the neutral point voltage like normal SVPWM. Then, the neutral point voltage balancing for zero-CM will be more difficult than normal SVPWM. As shown in Fig. 22, the neutral point voltage of zero-CM PWM is much larger than normal SVPWM with DC side capacitor equaling to 470  $\mu$ F.



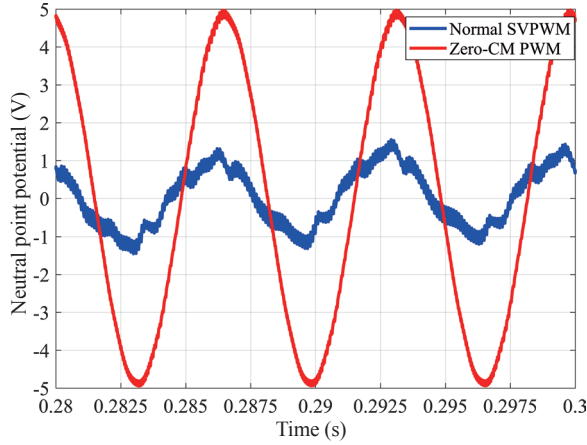


Fig. 22. Neutral point voltage comparison between normal SVPWM and zero-CM PWM.

In a word, zero-CM PWM pays the prices of higher THD, serious neutral voltage unbalancing and lower modulation index to achieve theoretical elimination of CM voltage.

### C. Implement of Zero Common-Mode Modulation

All discussion above is based on space vector modulation (SVM), whose algorithm is tedious and difficult to implement. However, regular SVM is popular and widely applied by virtue of lower harmonics and higher modulation index. Another well-known modulation is called carrier-based PWM, whose typical representative is sinusoidal pulse width modulation (SPWM), possesses the advantage of easily being implemented. Normal SVPWM can be equivalently realized by injecting zero sequence voltage into balanced three-phase voltage reference of SPWM [27].

It is easy to prove the inherent relationship between the two zero-CM modulations and the result is similar to normal ones. Fig. 23 shows the principle of zero-CM SPWM in sector I, which involves the line-to-line reference transferred into gate drive signals for phase [21].

As shown in Fig. 23, take the gate drive signal of phase-A for example. Firstly, calculating three-phase balanced reference signal  $V_1$ ,  $V_2$ , and  $V_3$ . Secondly, comparing the reference signals and triangular carrier to get signals  $g_1$ ,  $g_2$  and  $g_3$  that must be either 0 or 1, whose progress is similar to the carrier-based PWM method for two level converters. Lastly, the signal  $(g_1 - g_2)/2$  is as the reference of the gate drive for phase-A. The value 1, 0, and -1 of  $(g_1 - g_2)/2$  represent the output voltage are  $V_{dc}/2$ , 0, and  $-V_{dc}/2$  respectively. Therefore, the fundamental component of phase voltage is equal to  $(V_1 - V_2)/2$ , which means the real modulation index  $m$  is equal to  $0.866 * m'$ . The variable  $m'$  in  $V_1$ ,  $V_2$  and  $V_3$  is not representing the modulation index, so  $m'$  is used to be distinguished from modulation index  $m$ .

The switching sequence in Fig. 23 for carrier-based modulation is the same as Fig. 20(a) for space vector modulation. Distinctly, the duration of effective vectors is equal for volt-second balance. Therefore, the only difference is the duration of zero vector arrangement between center and two side. The injected

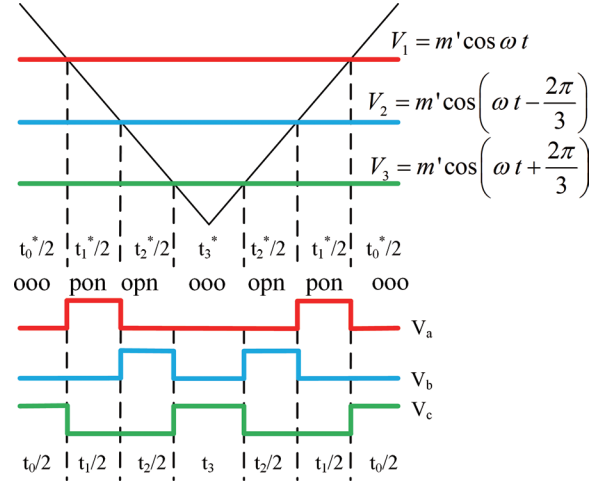


Fig. 23. Zero-CM SVPWM through carrier comparison.

zero sequence can play the role of distributing transient time of zero vector to realize the equivalence. That is to say, the zero-CM SPWM can be equivalent to zero-CM SVPWM by injecting zero sequence voltage  $v_z$  into references  $V_1$ ,  $V_2$  and  $V_3$ . The zero sequence voltage is concluded as  $v_z = -(v_{\max} + v_{\min})/2$ ,  $v_{\max}$  ( $v_{\min}$ ) represents the instantaneous maximum (minimum) value of  $V_1$ ,  $V_2$  and  $V_3$ . The other five sectors are the same.

Owing to the equivalent theory, simple zero-CM SPWM is able to replace complicated zero-CM SVPWM without losing the predominance of SVPWM. In DSP controller, we observed that the calculation time for zero-CM SVPWM is  $7.31 \mu s$  whereas only  $4.30 \mu s$  for zero-CM SPWM.

## IV. CONDUCTED EMI REDUCTION

### A. Variable Switching Frequency Theory for Zero-CM PWM

The zero-CM PWM assuredly reduces CM voltage and current whereas other aspects of performance degrade. Considering the merits of variable switching frequency, the advanced PWM introduced in part II and III can be incorporated together to improve the performance of zero-CM modulation. That is to say, the switching frequency of zero-CM PWM can change according to current ripple prediction model and the limit value for current ripple. The method of prediction model is based on Thevenin's equivalent circuit [16] rather than single-phase model [17] for brevity and convenience. There are only seven vectors in zero CM modulation while two pulses in one switching cycle, which makes the prediction model for single-phase more complicated. Fig. 24 shows four typical transient circuits and their Thevenin's equivalent circuit for phase-A. The current slope for this four different cases could be calculated by (3)-(6) ( $V_{sum}$  represents the sum of three-phase voltage) in the light of equivalent circuit and circuit theory.

The current rate for other space voltage vectors and phases is similar to the aforementioned four cases due to the symmetry of three-phase circuit and vectors. Therefore, the current slope for all situations is summarized in TABLE II ( $i_k$  represents the



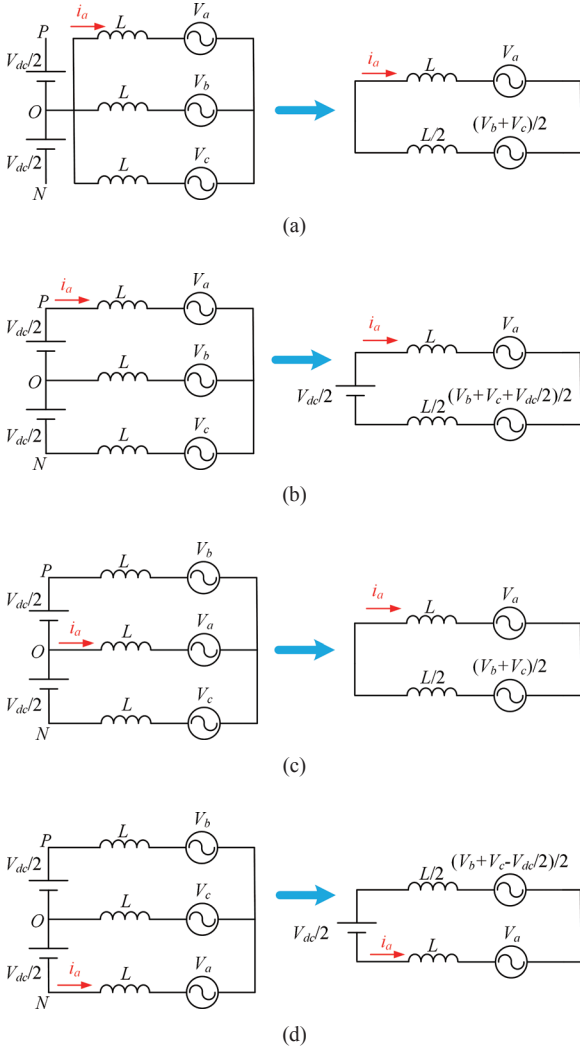


Fig. 24. Four typical transient circuits and their Thevenin's equivalent circuit. (a) vector ooo. (b) vector pon. (c) vector opn. (d) vector npo.

current for phase  $k$ ,  $V_k$  is the same). It is apparent that the current slope is only related to the location of DC bus connected into the phase and phase voltage regardless of other two phases, which makes the model rather simple. Therefore, there are only three kinds of cases for each phase to predict its current ripple based on space vectors, which is rather simple.

$$\frac{di_a}{dt}(ooo) = \frac{1}{3L}(V_{sum} - 3V_a) \quad (3)$$

$$\frac{di_a}{dt}(pon) = \frac{1}{3L}\left(\frac{3}{2}V_{dc} + V_{sum} - 3V_a\right) \quad (4)$$

$$\frac{di_a}{dt}(opn) = \frac{1}{3L}(V_{sum} - 3V_a) \quad (5)$$

$$\frac{di_a}{dt}(nop) = \frac{1}{3L}\left(-\frac{3}{2}V_{dc} + V_{sum} - 3V_a\right) \quad (6)$$

Fig. 25 shows the comparison of high frequency current ripple of experiment and predicted results for model, which powerfully proves the accuracy of prediction model. The

TABLE II  
CURRENT RIPPLE SLOPE FOR ALL SITUATIONS

Condition	Current Ripple Slope
Phase $k$ clamped to positive DC bus	$\frac{di_k}{dt} = \frac{1}{3L}\left(\frac{3}{2}V_{dc} + V_{sum} - 3V_k\right)$
Phase $k$ clamped to negative DC bus	$\frac{di_k}{dt} = \frac{1}{3L}(V_{sum} - 3V_k)$
Phase $k$ clamped to neutral point	$\frac{di_k}{dt} = \frac{1}{3L}\left(-\frac{3}{2}V_{dc} + V_{sum} - 3V_k\right)$

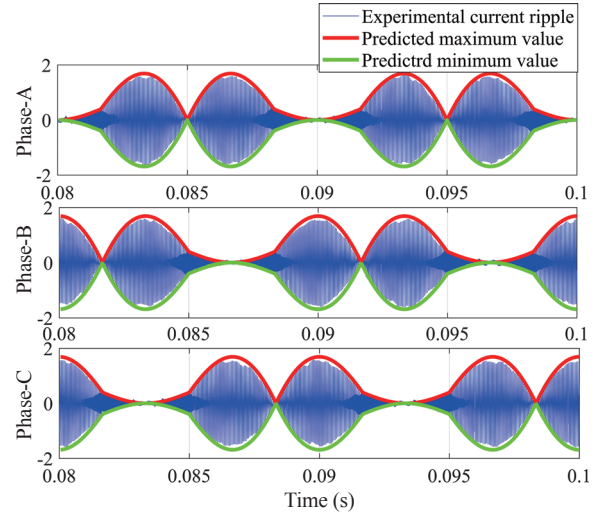


Fig. 25. Current ripple comparison between experiment and prediction (zero-CM SVPWM).

procedure of variable switching frequency is identical to the block diagram in Fig. 8, so the detail progress is not explained any more here. The proposed modulation combines zero-CM and VSFPWM is called zero-CM VSFPWM.

### B. Experimental Result of Zero-CM VSFPWM

As mentioned above, zero-CM PWM possesses a big issue with higher switching loss, which may restrain its wide applications. In addition, its space vectors map degenerate to be like two-level makes DM conducted EMI problem serious. Fortunately, by utilizing the freedom of switching frequency, zero-CM VSFPWM can bring many benefits.

Firstly, it is capable of reducing switching loss and raising efficiency of system greatly. Fig. 26 shows the switching frequency for zero-CM VSFPWM, whose carrier frequency varies from 5 kHz to 20 kHz. The criterion to determine the range of switching frequencies is the maximum current ripple of three-phase in switching cycle, which will be made clamped to the required current ripple by changing switching frequency. In this paper, the required current ripple we selected is the maximum current ripple in line cycle. Then, the current ripple at any time is smaller than the required value for constant switching frequency PWM. Therefore, the switching frequency will be

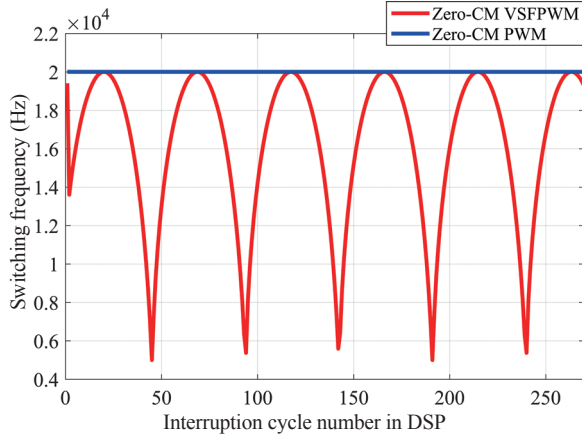


Fig. 26. Switching frequency variation of zero-CM VSFPWM in DSP.

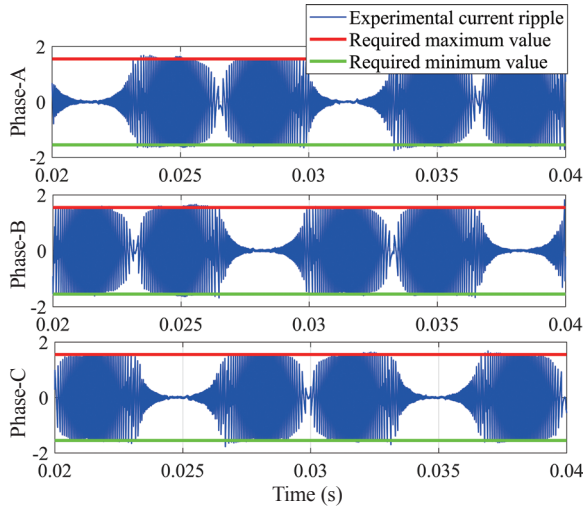


Fig. 27. Three-phase current ripple of zero-CM VSFPWM (experimental result).

smaller than the one for zero-CM PWM (20 kHz). Because the minimum three-phase current ripple (not the minimum current ripple for only one phase) is the one fourth of maximum current ripple in line cycle, the switching frequency range will be from 5 kHz to 20 kHz. This rather large range variation of switching frequency validates the huge advantage of VSFPWM and reduces the switching losses of zero-CM PWM. The current ripple of zero-CM VSFPWM is shown in Fig. 27. Compared with ripple in Fig. 25 for zero-CM PWM, zero-CM VSFPWM methods have better effective utilization rate of space limited by the identical required current peak value ( $\pm 1.65$  A) apparently.

Secondly, the CM conducted EMI can be further reduced. Fig. 28 shows CM conducted EMI for four modulations mentioned in this paper. It is apparent that the envelope curve of zero-CM VSFPWM is the lowest and reduces more than 20 dB in comparison with normal SVPWM.

Finally, the conducted EMI of zero-CM VSFPWM has huge superiority compared with other modulations. For conducted EMI test requirement, the current in line is conducted to EMI receivers for test, which do not distinguish DM and CM com-

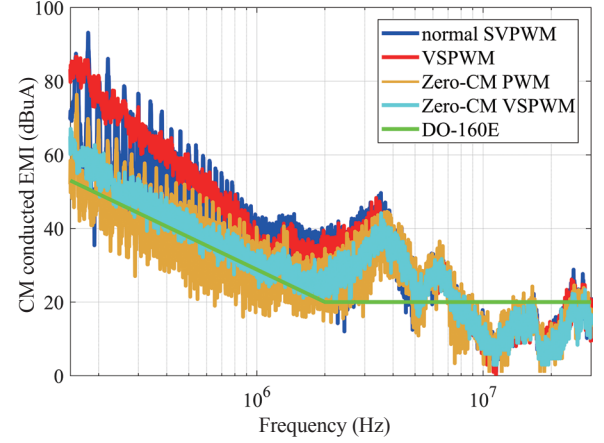


Fig. 28. Comparison of CM conducted EMI (experimental result).

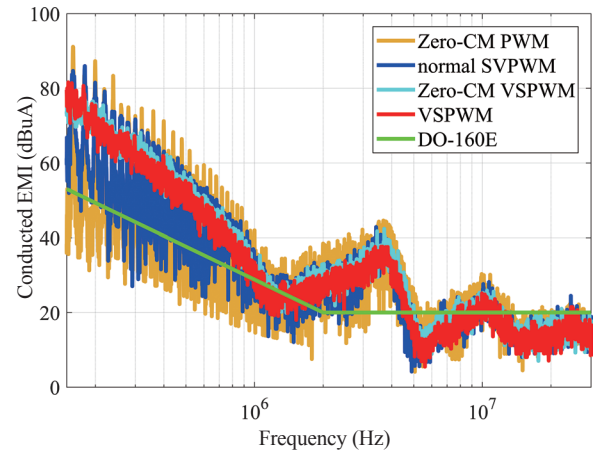


Fig. 29. Comparison of conducted EMI (experimental result).

ponents. Fig. 29 shows the conducted EMI in transmission line considering CM loop. On the one hand, zero-CM VSFPWM EMI is smaller than zero-CM and SVPWM, and almost as big as VSPWM. On the other hand, zero-CM VSFPWM spread spectrum, which would further reduce the damage caused by CM noise.

As mentioned above, the variable switching frequency methods have impact on low frequency harmonics and THD. Fig. 30 shows the FFT results of phase currents for both zero-CM PWM and zero-CM SVPWM. Apart from 2<sup>nd</sup> fundamental harmonics, variable switching frequency methods hardly have influence on other low frequency harmonics. Also, the THD only increases by 1.71%. In summary, zero-CM VSFPWM could improve the performance of zero-CM PWM, at the same time reduces CM problem furtherly.

### C. Comprehensive Comparison of Four PWM Methods

Based on previous discussion of four mentioned PWM methods, TABLE III summaries their comprehensive comparison of SVPWM, VSFPWM, zero-CM PWM, and zero-CM VSFPWM. Firstly, variable switching frequency methods can decrease conducted EMI and switching loss compared with

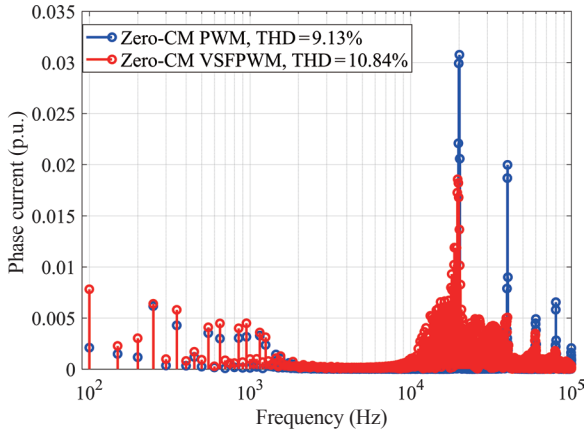


Fig. 30. Comparison of phase current spectrum: zero-CM PWM and zero-CM VSFPWM (experimental result).

TABLE III  
COMPARISON OF FOUR PWM METHODS

Performance	SVPWM	VSFPWM	Zero-CM SVPWM	Zero-CM VSFPWM
THD (a specific condition)	4.43%	6.28%	9.13%	10.84%
Average Switching Frequency	20 kHz	13.64 kHz	20 kHz	16.09 kHz
Efficiency (a specific condition)	98.15%	98.26%	97.61%	97.94%
Switching Loss	small	smallest	biggest	big
CM Current	big	big	small	small
Conducted EMI	bigger	small	biggest	small

invariable switching frequency methods. Then, zero-CM PWM methods pay the prices of higher THD, serious neutral voltage unbalancing and lower modulation index to achieve theoretical elimination of CM voltage. Lastly, zero-CM VSFPWM methods can improve the worse performance of zero-CM PWM, which contain bigger switching loss and higher conducted EMI.

In the TABLE III, we observed that the algorithm with variable switching frequency reduce switching loss greatly and increase the efficiency by 0.11% and 0.33% for VSFPWM and zero-CM VSFPWM respectively. In addition, zero-CM PWM makes the efficiency decreases by 0.54% for the double switching action compared with normal SVPWM during a switching cycle. Fortunately, the zero-CM VSFPWM can compensate the disadvantage with low efficiency for zero-CM PWM. In order to understand the efficiency of the four methods thoroughly, a switching loss curve with different operating points with calculation method is provided. The three-level converter module used in the platform is FS3L50R07W2H3F\_B11 produced by Infineon. The operating point is DC voltage 600 V and phase current 50 A, whose parameters are selected to calculate switching loss of the module to increase the computational accuracy. The following Fig. 31 is the switching curve with different power factor. It is noticeable that the switching loss decreases with the increasing of power factor.

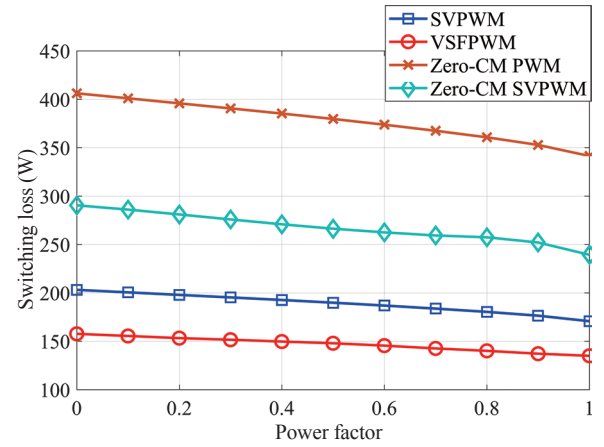


Fig. 31. Comparison of switching loss with different power factor (calculation result).

## V. CONCLUSION

This paper gives a comprehensive study on EMI reduction methods for three-level voltage source inverter through PWM. It contains the study of both DM and CM EMI reduction.

For DM conducted EMI noise reduction, this paper introduced VSFPWM method based on the current ripple prediction model for three-level voltage source inverter. For three-level inverter, with carrier-based PWM analysis, current ripple prediction model has been proposed. Then, VSFPWM method has been developed for three-level inverter to control the current ripple peak value. Experimental result demonstrates the attenuation of EMI noise peak value for three-level inverter, with current ripple peak value to be the same with normal SVPWM.

Three-level inverters possess the freedom to restrain CM by selecting appropriate vectors to reduce common-mode voltage. However, the attenuation of CM conducted EMI pays the price of lower utilization of DC voltage, higher THD and more switching losses. The equivalence of two significant PWM contributes to simplify algorithm is introduced at the same time to optimize the algorithm for zero-CM modulation.

The variable switching frequency method successfully expands to zero common-mode modulation, whose mechanism is briefly illustrated with experimental results. This advanced method greatly reduces switching loss, decreases conducted EMI and has further improvement on CM problem.

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**Jianan Chen** was born in Nantong, China, in 1992. He received the B.S. degree in Building electricity and intelligence from Nanjing University of Technology, Nanjing, China, in 2015. He received the M.S. degree in Electrical Engineering in Huazhong University of Science and Technology, Wuhan, China, in 2018. Now he is currently working towards Ph.D. degree in Electrical Engineering in Huazhong University of Science and Technology, Wuhan, China.

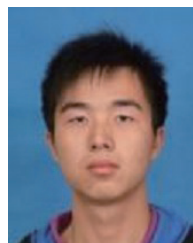
His current research interests include pulse-width modulation technique of multilevel converters and electromagnetic interference of power electronics.



**Dong Jiang** received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2007, respectively. He started working toward the Ph.D. degree in high density motor controller from the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, in 2007 and was transferred with his advisor in 2010 to the University of Tennessee, Knoxville, TN, USA, where he received the Ph.D. degree in Dec. 2011.

He was with the United Technologies Research Center, Connecticut as a Senior Research Scientist/Engineer from Jan. 2012 to July 2015. He has been with the Huazhong University of Science and Technology, Wuhan, China, as a Professor since July 2015. His major research interests include power electronics and motor drives, with more than 50 published IEEE journal and conference papers in this area.

Dr. Jiang is an Associate Editor for the IEEE Transactions on Industry Applications. He received two best paper awards in IEEE conferences.



**Qiao Li** received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2015. He is currently working toward the Ph.D. degree in electrical engineering at Huazhong University of Science and Technology, Wuhan, China.

His research interests include pulse width modulation strategy, converter control and power hardware-in-the-loop.