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SPECIAL ISSUE ON ROBUST AND RELIABLE POWER ELECTRONICS

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Editorial for the Special Issue on Robust and Reliable Power Electronics

AS power electronic systems are gradually gaining more and more important status in a wide range of applications, their reliability has become an important issue for the manufacturers. In recent years, the automotive and aerospace industries have brought more stringent reliability constraints on power electronic systems, because of safety requirements but also because such systems becomes much more electrified. The industrial and energy sectors are also following the same trend, and a lot of efforts are being devoted to improving power electronic systems in order to account for reliability with cost-effective combined with sustainable solutions. A paradigm shift in reliability research and engineering in power electronics is going on in terms of the design methodologies, reliability testing concepts, and robustness validation approaches [1], [2] and Fig. 1 illustrates the important aspects of modern reliability engineering in power electronics, which need to be mastered for future products.

Research on active switching devices, passive components, and interconnections is of high interest in order to have a better understanding on the component-level reliability physics and this is naturally extended to system-level reliability based on component level reliability physics. Furthermore, with the consideration of reliability as performance, the existing or new power converter topologies and control schemes need to be studied in multi-physics domains to optimize their design. Further on fault-tolerant design and prognostic health management are also interesting research areas to provide additional opportunities to ensure the reliable field operation of power electronic systems, especially in reliability-critical applications. However, the more easy interconnection – eg. IoT will make such things commodity in almost all kind of products. At the same time emerging technologies like GaN and SiC devices call constantly for new life time models, new test methods to understand the devices fully as well as doing better integration in order to keep the pace and launch strong products to a power electronics market, which is booming for the moment as a part of making the society more sustainable.

The purpose of this Special Issue is to review the state-of-the-artin the Robust and Reliable Power Electronics fields and to disseminate the recent advancements in Reliability Engineering and how to approach it from device to systems. It is my believe this field is one of the very emerging topics in the next decade and it needs a very multidisciplinary efforts to achieve the goal.

This Special Issue on Robust and Reliable Power Electronics has collected 3 papers from basic reliability engineering to more system engineering in terms of control and operation.

The first paper entitled "Enhancing PV Inverter Reliability with Battery System Control Strategy" is written by Dr. Ariya Sangwongwanich and colleagues from Aalborg University (Denmark) and colleagues from RWTH Aachen (Germany) where different operation, and control strategies for a photovoltaic (PV) system also having a battery energy storage system are discussed. It is a system engineering paper and the analysis shows that with a proper control of the battery-PV system much higher reliability can be achieved for the grid connected converter.

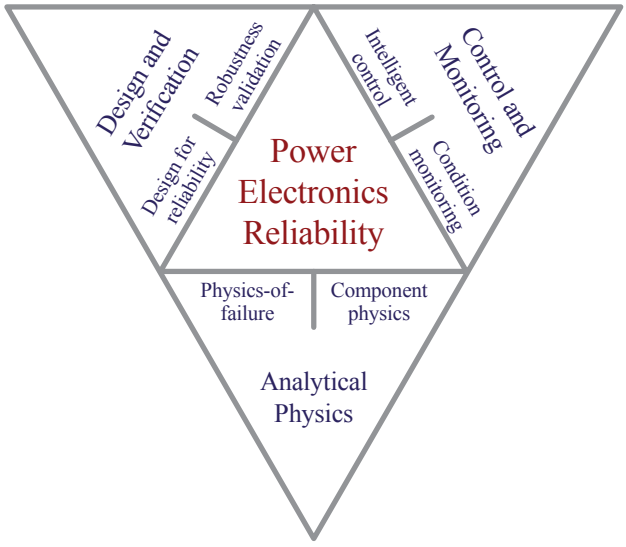

Fig. 1. Main areas in modern reliability engineering in power electronics – from components to control and monitoring of products in the field.

The second paper is authored by Dr. Alessandro Soldati and his colleagues from University of Parma (Italy) and it has the title of "Electric-vehicle Power Converters Model-based Design for Reliability". This paper is proposing a design for reliability approach in EV's where they are especially studying different driving cycles impact on the thermal aging of the power electronic devices. They are also discussing how active thermal control in the drive train can increase the expected life time on the power electronics. Further – the variation of the components are treated in order to take a statistical approach for the analysis.

The third paper on "Analysis of Electromagnetic Transient Characteristics of Doubly-fed Induction Generator Under Grid Voltage Swell" is contributed by Mr. Yonghong Deng and his colleagues from China University of Petroleum (China) and it is dealing with the control issues of a DFIG-based wind turbine system when transients are occurring in the grid – if they are not properly handled failure will occur in the wind turbine system and thereby having poor reliability. Both simulations and experimental results are provided to support the theory presented.

I would like to express thanks to the guest associate editors for their efforts spend of this special issue making 3 good papers as well as I wish to thank the time spend from the expert reviewers, who have provided comments and input to the assessment and scoring of the submitted manuscripts.

Further Reading

[1] H. Wang, M. Liserre, F. Blaabjerg, P. P. Rimmen, J. B. Jacobsen, T. Kvisgaard, J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, no. 1, pp. 97-114, 2014

[2] K. Ma, H. Wang and F. Blaabjerg, "New approaches to reliability assessment: Using physics-of-failure for prediction and design in power electronics systems," *IEEE Power Electronics Magazine,* vol. 3, no. 4, pp. 28-41, Dec. 2016.

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Frede Blaabjerg was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the Ph.D. degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 500 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of 9 books in power electronics and its applications.

He has received 28 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the *IEEE Transactions on Power Eelectronics* from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2018 he is President Elect of IEEE Power Electronics Society.

He is nominated in 2014, 2015, 2016 and 2017 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.

Enhancing PV Inverter Reliability With Battery System Control Strategy

Ariya Sangwongwanich, Georg Angenendt, Sebastian Zurmühlen, Yongheng Yang, Dezso Sera, Dirk Uwe Sauer, and Frede Blaabjerg

***Abstract*—The increasing integration of Photovoltaic (PV) and Battery Energy Storage Systems (PV-BESS) adds more power control flexibility of the PV systems. This offers an opportunity to improve the PV inverter reliability, where the loading of the PV inverter can be modified through the operation of the battery system (e.g., charge/discharge). In that case, the control strategy of battery systems will affect the PV inverter loading and thereby also the reliability. This paper investigates the potential solution to enhance the PV inverter reliability through the control of battery system, where three self-consumption control strategies are considered. The impact of the battery system control strategies on the PV inverter reliability is analyzed with the mission profile of a 6-kW PV-BESS installed in Germany. The evaluation results indicate that limiting the maximum charging power of the battery system has high potential to enhance the PV inverter reliability, where the damage of power devices in the inverter can be reduced by approximately 50%.**

***Index Terms*—Battery, control strategy, lifetime, mission profile, PV inverters, reliability, self-consumption.**

I. Introduction

To further increase the penetration level of Photovoltaic (PV) systems, a significant reduction in the cost of PV energy is still demanded. It is recommended in [1] that the cost of PV energy should be reduced by a factor of around three in the near future (e.g., from 0.18 USD/kWh in 2016 to 0.05 USD/kWh by 2030 for residential PV systems in the US) to increase the competitiveness of PV systems. This is a challenging target, which requires improving PV systems in several aspects. Among those, the PV inverter reliability is one of the areas that should be enhanced [1]. From the field experience, the PV inverter is one of the most fragile parts in PV systems and it is responsible for a majority of unexpected failure events [2]. As a consequence, such an event results in higher maintenance cost as well as PV energy yield losses, and eventually, increasing the cost of PV energy. Therefore, enhancing the reliability of PV inverters has high potential to bring down the cost of PV energy.

The reliability of PV inverters (and power electronics in general) is strongly affected by the system operating condition (also referred to as the mission profile) [3]. In that regard, the control strategy of PV systems inevitably affects the PV inverter reliability, as it changes the operating conditions. Nevertheless, the relationship increases the awareness of control for reliability. In the literature, many attempts have been made in recent years to enhance the PV inverter reliability. For instance, in [4], a control strategy to limit the maximum feed-in power of the PV inverter has been discussed, and its contribution to the inverter reliability improvement has been analyzed in [5]. Another control strategy to reduce the thermal loading fluctuation of PV inverters was proposed in [6], where the maximum power point tracking algorithm is modified during the fast change in the solar irradiance condition. In both control strategies, there is a trade-off between the improvement in the PV inverter reliability and the PV energy yield loss, since the PV power extraction is intentionally reduced (power curtailment) to alleviate the thermal loading of PV inverters. In some cases, the effectiveness of those control strategies is thus limited, considering the overall cost of energy [5].

Recently, the integration of PV and Battery Energy Storage Systems (PV-BESS) has become more economical-viable due to the declining cost of battery systems and the supportive policies [7]. For instance, in recent years, more than 40% of residential PV systems in Germany have been installed with battery systems, where self-consumption schemes are widely adopted [8], [9]. With the integration of battery systems, more control flexibilities of the PV system is enabled. In that case, the loading of PV inverters can be reduced by storing a certain amount of PV energy in the battery, instead of being curtailed, as it is illustrated in Fig. 1. This thus offers a possibility to enhance the PV inverter reliability without a loss of the total energy production. Hereby, the control strategies for battery systems are important to maintain the energy yield or the power flow, which affects the PV inverter loading and thus its reliability. Considering the PV self-consumption scheme, there are several battery system control strategies [10]-[13], whose impacts have also been investigated and compared for several aspects (e.g., battery lifetime, grid-relieving effect) in the literature [14]-[17]. However, the influence on the PV inverter reliability has not been explored yet.

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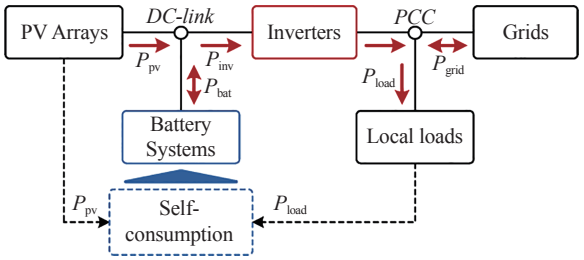

Fig. 1. Power flow of PV system with integrated battery system (P_{pv}: PV array output power, P_{bat}: battery power, P_{inv}: PV inverter input power, P_{load}: load consumption, and P_{grid}: power exchanged with the grid).

In this paper, the impact of battery system control strategies on the PV inverter reliability is analyzed. The analysis is carried out on a 6-kW PV-BESS with a PV self-consumption scheme. The control strategies for battery systems are described in Section III, and the impact on the PV inverter loading is discussed in Section IV. Then, a reliability assessment of the PV inverter is carried out in Section V, where the mission profile of the PV-BESS installed in Germany is considered. Finally, concluding remarks are given in Section VI.

II. System Description of PV-BESS

In this paper, a single-phase PV-BESS is considered, as shown in Fig. 2, where the battery system is connected to the DC-link of the PV system, being a DC-coupled configuration. The system parameters are given in TABLE I.

A. PV Arrays and Converter

PV arrays are the main power source of the system. Since the PV array characteristic is strongly dependent on the environmental conditions (e.g., the solar irradiance and temperature), a Maximum Power Point Tracking (MPPT) operation is normally employed to maximize the PV energy yield. This is achieved through the control of the PV converter (e.g., the DC-DC converter), which regulates the PV array voltage at the Maximum Power Point (MPP), and the extracted PV power is then delivered to the DC-link [18].

B. Battery and Converter

For the DC-coupled configuration, the battery system is connected to the DC-link in parallel with the PV converter. Here, the battery system adds more power control flexibility, where the self-consumption control scheme can be implemented. The charging and discharging of the battery (i.e., bidirectional power flow) is achieved by controlling the battery converter (e.g., the bidirectional DC-DC converter). In this paper, the battery system parameters are designed according to the recommendation in [19], where the ratio between the battery capacity and the PV array rated power (kWh/kWp) is selected as 1:1.

C. PV Inverter

The PV inverter is the interface between the DC-link and the point of common coupling. The total power at the DC-link, depending on the PV array output power and the battery power, should be delivered to the grid and/or load through the PV inverter. The DC-link voltage of the inverter is regulated to be constant through the control of the output AC current. Moreover, the injected current should be synchronized with the grid voltage, e.g., by means of phase-locked loops [20]. In this paper, a single-phase full-bridge PV inverter is used, as it is shown in Fig. 2. The power devices, whose reliability is considered, are Insulated-Gate Bipolar Transistor (IGBT) devices from [21]. Regarding the cooling system design, the heat sink is selected to limit the junction temperature of the power devices at 90 ºC when the inverter operates at the rated power (i.e., 6 kW) and the ambient temperature is 50 ºC.

TABLE I
Parameters of the Single-Phase PV-BESS (Fig. 2)

PV array rated power	6 kW
Battery capacity	6 kWh
Battery converter rated power	3 kW
PV inverter rated power	6 kW
DC-link capacitor	C_{dc} = 1100 μF
LC-filter	L_{inv} = 4.8 mH, C_f = 4.3 μF
Switching frequency	Full-Bridge inverter: f_{inv} = 10 kHz
DC-link voltage	v^*_{dc} = 450 V
Grid voltage (RMS)	V_g = 230 V
Grid nominal frequency	$\omega_0 = 2\pi \times 50$ rad/s

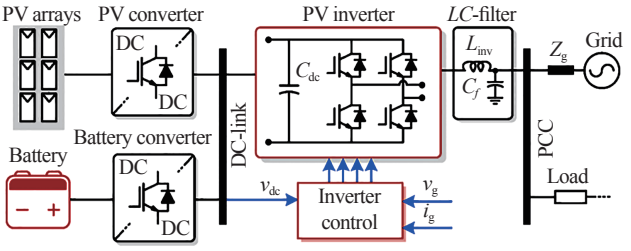

Fig. 2. System description of PV system with battery energy storage system (PV-BESS), where the battery system is connected to the DC-link.

III. Control Strategy of PV Self-Consumption

The basic concept of the PV self-consumption is to locally consume the generated PV electricity within the household, instead of drawing the electricity from the grid to supply the loads. The Self-Consumption Rate (SCR) is normally defined as the ratio between the self-consumed energy Eself and the generated PV energy E_{pv}: SCR = E_{self}/ E_{pv} [13]. Clearly, the higher the SCR is, the better the utilization of PV energy for local consumption will be. With battery systems, the surplus PV power during the day can be stored in the battery, and it will be used to supply the loads during nights. As a result, the SCR of the PV systems can be increased. Several battery system control strategies to realize the self-consumption operation are available in the literature. The operational principle of different control strategies will be discussed in the following, where the one-day PV power

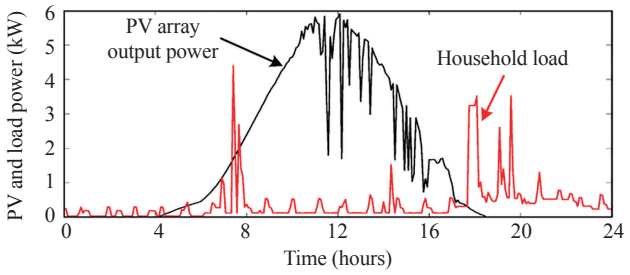

Fig. 3. Example of the PV power production and load profiles during a day.

and load profiles in Fig. 3 are considered.

A. Maximizing Self-Consumption

The most commonly-used battery system control strategy within the self-consumption scheme is the maximizing self-consumption method [13]. In this control strategy, the battery is charged as soon as the PV power production is higher than the load demand, as it is demonstrated by simulations in Fig. 4. By doing so, it can be ensured that the SCR of the PV-BESS is maximized, which is the advantage of this control strategy. However, this control strategy usually leads to a situation where the battery is fully charged before noon (especially during summer) [15], as it can be seen in Fig. 4(b) from the State of Charge (SOC) of the battery. This is undesirable from the grid integration perspective, since the battery system cannot contribute to the PV peak power reduction (e.g., the battery is fully charged before midday). Additionally, the early fully charged batteries will lead to a high average SOC during operation. This will accelerate the calendar aging of some types of batteries (i.e., lithium-ion batteries), which limits the battery lifetime [22].

B. Delaying Charging Period

To tackle the above issues, a control strategy that delays the charging period of the battery system has been discussed in [12]. In this control strategy, the battery will not be charged immediately when the surplus PV power becomes positive. In contrast, the battery will be charged after a certain time period in a way to shift the charging period from the early morning to midday. An operational example of the delaying charging period control strategy is shown in Fig. 5, where the battery is allowed to be charged after 9:00. In this case, the battery is fully charged around 12:00.

Compared with the maximizing self-consumption control strategy in Fig. 4, the time duration where the battery SOC is kept at 100% is reduced with this control strategy. Thus, the average SOC of the battery is effectively reduced. As a consequence, the lifetime of the battery can be improved and at the same time a certain amount of PV peak power injected into the grid is reduced. However, this control strategy may reduce the SCR in the case of a low solar irradiance conditions (e.g., during winter period), where the battery may not be fully charged by the end of the day (e.g., less load during night can be supplied by the PV energy). In that case, the PV

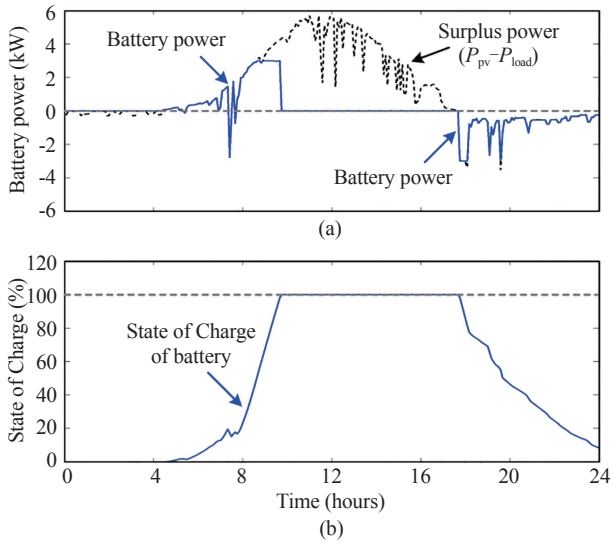

Fig. 4. Operation principle of the PV-BESS with the maximizing self-consumption control strategy: (a) battery power and (b) State of Charge of the battery.

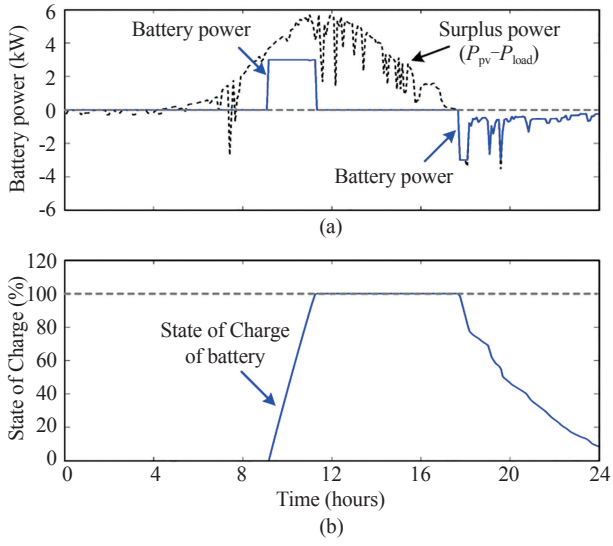

Fig. 5. Operation principle of the PV-BESS with the delaying charging period control strategy: (a) battery power and (b) State of Charge of the battery.

energy is not fully utilized for local consumption.

C. Limiting Charging Power

Limiting the charging power of the battery is another possible solution to avoid the battery to be fully charged early in the day. In this control strategy, the maximum battery charging power is limited to a certain value [11]. When the surplus PV power is higher than the charging power limit, the battery will be charged with a constant power corresponding to the maximum power limit, while the rest of the surplus PV power will be delivered to the grid. The operation of this control strategy is demonstrated in Fig. 6, where the maximum charging power of the battery is kept at 30% of the battery converter power rating (i.e., the maximum

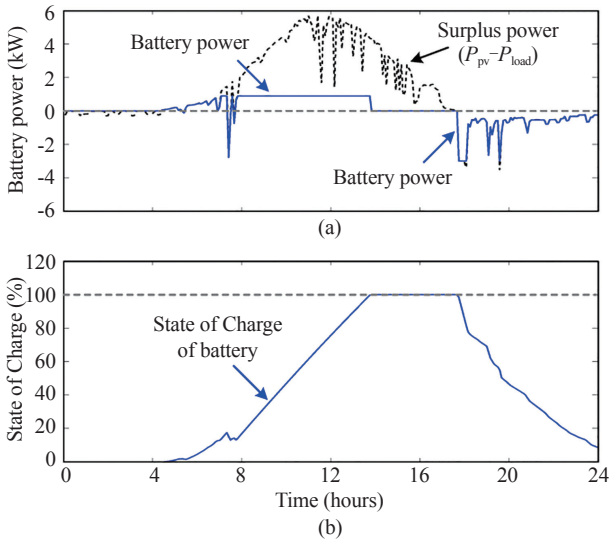

Fig. 6. Operation principle of the PV-BESS with the limiting charging power control strategy: (a) battery power and (b) State of Charge of the battery.

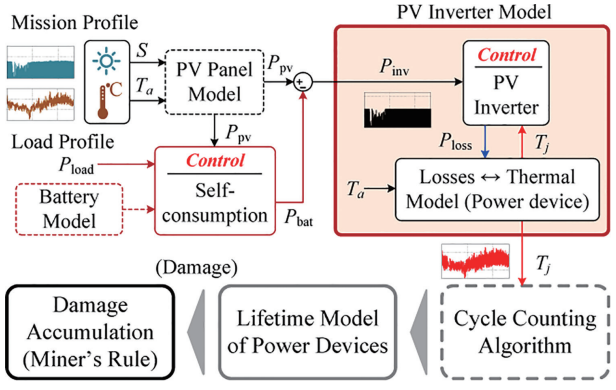

Fig. 7. Loading determination and reliability evaluation process of PV inverters with battery systems under with self-consumption.

charging power is 900 W). As a result, the battery charging time is prolonged, where the battery is fully charged around 14:00.

The limiting charging power control strategy can effectively reduce the average SOC of the battery, as it can be seen from the battery SOC in Fig. 6(b). However, its contribution to the grid-relieving is limited, since a part of the surplus power is injected to the grid due to the limited battery charging power. Moreover, it also shares the same drawback with the delaying charging period method, where the SCR may be reduced during a low irradiance day.

IV. Impact of Battery System Control Strategy on PV Inverter Loading

In this section, the impact of battery system control strategies on the PV inverter loading is analyzed. There are several quantities to map the PV inverter loading: 1) the input power of PV inverters, 2) the thermal stress of the power devices, and 3) the damage of the power devices, which can be

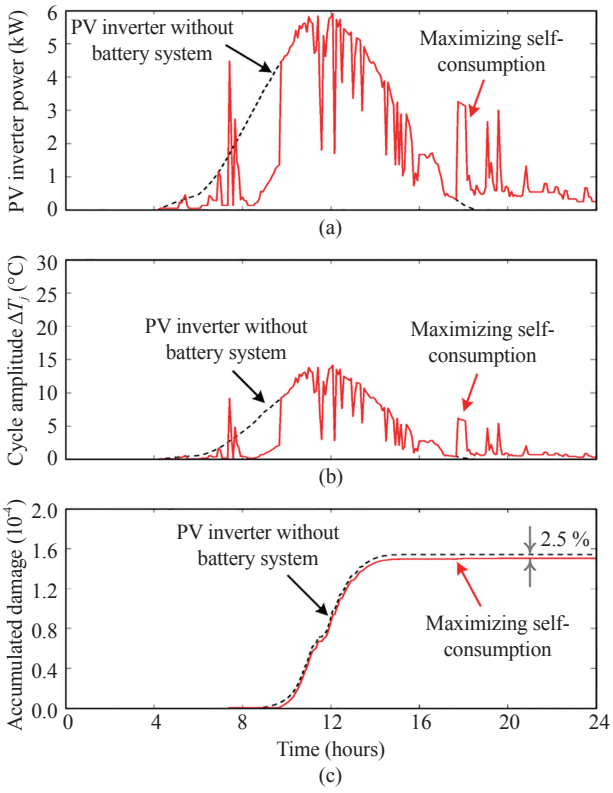

Fig. 8. Loading of the PV inverter with the maximizing self-consumption control strategy: (a) PV inverter power P_{pv}, (b) the thermal cycle amplitude of the power device ΔT_j, and (c) the damage accumulation of the power device.

obtained following the procedure in Fig. 7. This procedure will be explained in details.

A. Input Power of PV Inverters

The input power of the PV inverter P_{inv} can be used to represent the system-level loading of the PV inverter. For the PV-BESS, the input power of the PV inverter P_{inv} can be obtained by subtracting the PV array output power P_{pv} with the battery power P_{bat}. Therefore, the battery system control strategy (discussed in Section III) will determine the battery power, as it is shown in Fig. 7.

Here, the impact of battery system control strategies on the input power of the PV inverters is demonstrated by using the one-day PV power and load profiles in Fig. 3. The input power of the PV inverter with the maximizing self-consumption control strategy is demonstrated in Fig. 8(a), where the battery power profile in Fig. 4(a) is used. It can be seen that the maximizing self-consumption control strategy can reduce the input power of the PV inverter during the early morning, which corresponds to the charging time period of the battery. However, the PV inverter will experience similar peak loading periods during noon as the case of PV inverters without battery system, since the batteries have been fully charged before noon and thus the PV peak-power cannot be stored.

On the other hand, the loading of PV inverters during the PV peak power generation period can be reduced with

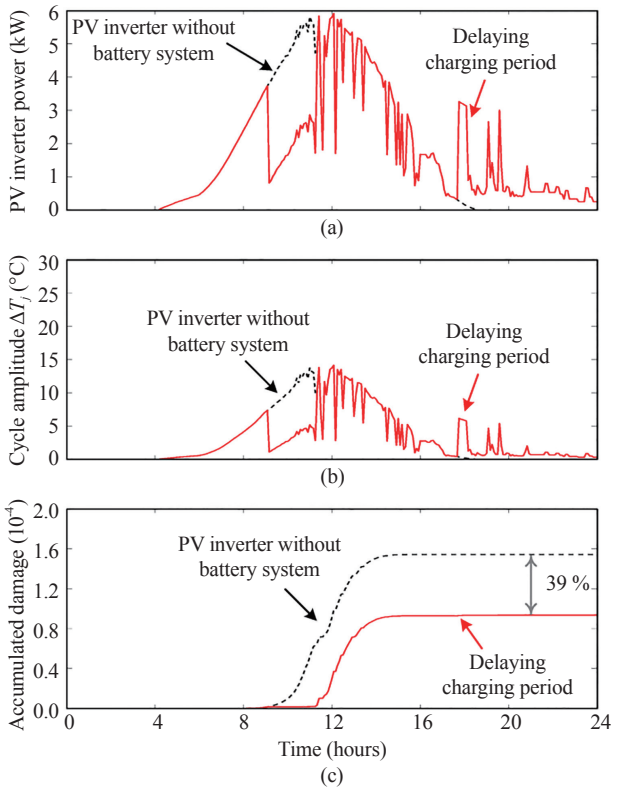

Fig. 9. Loading of the PV inverter with the delaying charging period control strategy: (a) PV inverter power P_{pv}, (b) the thermal cycle amplitude of the power device ΔT_j, and (c) the damage accumulation of the power device.

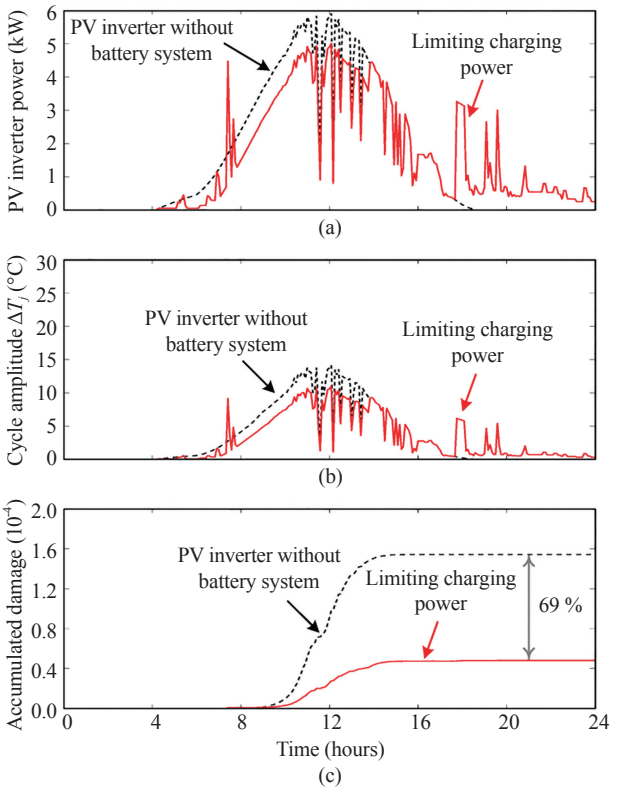

Fig. 10. Loading of PV the inverter with limiting charging power control strategy: (a) PV inverter power P_{pv}, (b) the thermal cycle amplitude of the power device ΔT_j, and (c) the damage accumulation of the power device.

the delaying charging period control strategy, as it can be seen in Fig. 9(a). In this case, the PV inverter loading starts decreasing after 9:00, which is the time when the battery system starts the operation (i.e., Fig. 5(a)). Therefore, a certain amount of PV power during noon is stored in the battery, and thus the peak load of the PV inverter can be reduced to some extent.

Similarly, the limiting charging power control strategy contributes also to the peak load reduction of the PV inverters. The input power of the PV inverters under this control strategy is demonstrated in Fig. 10(a). It can be seen in Fig. 10(a) that the loading of the PV inverter is reduced with the power difference corresponding to the maximum charging power. In this case, the load reduction starts from early morning until afternoon, corresponding to the battery charging time period.

Notably, the input power of the PV inverter during night is similar for all battery control strategies, since they share the same discharging control strategy (e.g., discharging as soon as the surplus power becomes negative). In that case, the loading of PV inverters will be increased during nights, as the battery is discharged to supply the load through the PV inverter.

B. Thermal Stress of Power Devices

The thermal stress of power devices is another quantity that can be used to indirectly assess the reliability. Thus, the impact of battery system control strategies on the PV inverter reliability can be analyzed considering the thermal stress of the power devices [23]. From the input power of the PV inverter, the thermal stress of the power devices can be obtained using the loss and thermal models of the power device, as it is shown in Fig. 7. Notably, the translation from the input power to the power loss and thermal stress is normally realized through a look-up table in order to handle long-term simulations (e.g., one-year mission profile). More details about the mission profile translation has been provided in [24]. For IGBT power devices, the cycle amplitude ΔT_j of the junction temperature is the main stress factor that induces wear-out failures after a number of cycles (e.g., resulting in bond-wire lift-off) [3].

The thermal stress of the power device under different battery system control strategies is determined by translating the input power of the PV inverter in Fig. 8(a), Fig. 9(a), and Fig. 10(a) into the junction temperature of the power device (e.g., the cycle amplitude) following Fig. 7. In general, the thermal stress of the power device has a similar tendency as the input power profile of the PV inverter. More specifically, the cycle amplitude of the power device decreases significantly in the early morning with the maximizing self-consumption control strategy, as it is shown in Fig. 8(b). In the case of the delaying charging period control strategy, the thermal stress of the power device starts decreasing after the battery system is activated (i.e., after 9:00), as it is shown in Fig. 9(b). For the limiting charging power control strategy, the thermal stress in the power device reduces from the early

morning until the afternoon, covering the PV peak power generation period, as it is shown in Fig. 10(b).

C. Damage Evaluation of Power Devices

For power devices, one main wear-out failure mechanism is related to the thermal cycling, which can cause the bond-wire lift-off after a number of thermal cycles [25]. Therefore, a cycle counting algorithm such as the rainflow analysis needs to be applied to the thermal stress profile in order to obtain the thermal cycling information. Normally, it is assumed that the contribution of each thermal cycle to the failure, also referred to as damage, is accumulated linearly and independently during operation (i.e., using the Miner's rule) [3]. For instance, the accumulated damage in the power device during operation is calculated as

$$AD = \sum_i \frac{n_i}{N_{fi}} \tag{1}$$

where AD is the accumulated damage of the power device. n_i is the number of cycles for a certain thermal stress condition (e.g., the cycle amplitude ΔT_j, the mean value T_{jm}, and the cycle period t_{on}), which is obtained from the cycle counting algorithm. N_{fi} is the number of cycles to failure at a certain stress condition, which can be calculated from the lifetime model of the power device as

$$N_f = A \cdot \left(\Delta T_j\right)^{\alpha} \cdot \left(ar\right)^{\beta_1 \Delta T_j + \beta_0} \cdot \left[\frac{C + \left(t_{on}\right)^{\gamma}}{C+1}\right] \cdot \exp\left(\frac{E_a}{k_b \cdot T_{jm}}\right) \cdot f_d \tag{2}$$

where the lifetime model parameters are given in TABLE II [25]. It is worth mentioning that this lifetime model is obtained through the accelerated testing where the power devices are subjected to the stress level higher than normal operation in order to obtain the test results in a reasonable time. This lifetime prediction (damage calculation) is based on the extrapolation of this model when the operating condition falls outside the testing conditions [3].

The accumulated damage AD can be used as a quantitative reliability metric to compare the contribution of the operating condition (e.g., battery system control strategies) to the reliability of power devices. It indicates a proportion of the component lifetime that has been consumed during the operation. The operation with high accumulated damage indicates low reliability, resulting in a high failure rate, where the end of life of the power devices is reached when the damage is accumulated to unity (i.e., AD = 1 after a few years of operation) [3].

The accumulated damage during one-day operation is obtained by considering the thermal stress in the power devices, and it is compared with the case of the PV inverter without battery system. It can be seen in Fig. 8(c) that the maximizing self-consumption control strategy has a limited contribution to the damage reduction of the power devices. On the other hand, the control strategy with a delaying charging period can reduce the damage of the power devices significantly, where the accumulated damage during one-day is reduced by 39% (compared to the case of the PV inverter without battery system), as it is shown in Fig. 9(c). Nevertheless, the battery system control strategy with a limited charging power is the most effective solution in terms of damage reduction, as it can be seen in Fig. 10(c). In that case, the accumulated damage during one-day is reduced by 69% (compared to the case of the PV inverter without battery system). This is mainly due to the reduced peak load of the PV inverter during noon, where the maximum cycle amplitude of the power device junction temperature is decreased and thereby the damage of power devices is reduced significantly.

TABLE II
PARAMETERS OF THE LIFETIME MODEL OF AN IGBT MODULE USED IN THE PV INVERTER [25]

Parameter	Value	Experimental Condition
A	3.4368×10^{14}	
α	-4.923	$64\ \text{K} \le \Delta T_j \le 113\ \text{K}$
β_1	-9.012×10^{-3}	
β_0	1.942	$0.19 \le ar \le 0.42$
C	1.434	
γ	-1.208	$0.07\text{s} \le t_{on} \le 63\text{s}$
f_d	0.6204	
E_a	0.06606 eV	$32.5\ ^\circ\text{C} \le T_j \le 122\ ^\circ\text{C}$
k_B	8.6173324×10^{-5} eV/K	

V. RELIABILITY ASSESSMENT OF PV INVERTERS WITH SELF-CONSUMPTION CONTROL STRATEGY

The previous analysis during one-day operation suggests that the battery system control strategy can strongly affect the reliability of PV inverters. Nevertheless, the impact of the control strategy is also dependent on the mission profile of the PV system (e.g., solar irradiance and ambient temperature), which varies during the operation [23]. In this section, the reliability assessment of the PV inverter is carried out with a one-year mission profile of the PV-BESS in Germany. By doing so, the seasonal variations in the mission profile (e.g., during summer and winter) can be included in the analysis, and the long-term impact of the battery system control strategies on the PV inverter reliability is then examined.

A. Mission Profile of PV-BESS

For PV systems, the mission profile usually consists of the solar irradiance and the ambient temperature, as the PV array output power is mainly determined by the two parameters [24]. One-year solar irradiance and ambient temperature profiles recorded in Lindenberg, Germany are shown in Fig. 11 and used as a case study, where the annual PV energy yield is approximately 6600 kWh/year. Due to a strong seasonal variation (e.g., between summer and winter) in the mission profile, it can be expected that the amount of surplus power during the day in the summer will be much higher than that in winter. In that case, the issues associated with the early

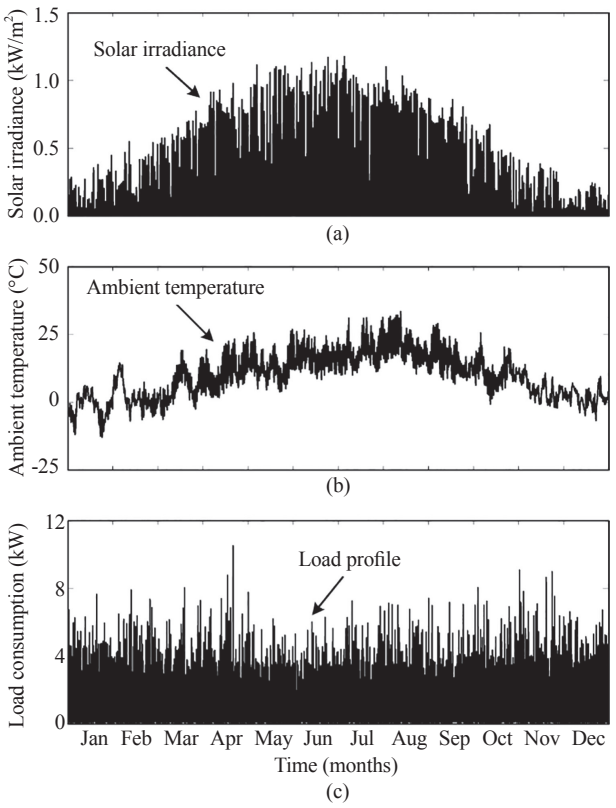

Fig. 11. One-year mission profile of the PV-BESS in Lindenberg, Germany with a sampling rate of 1 minute per sample: (a) solar irradiance, (b) ambient temperature, and (c) household load profile.

fully charged battery will be more pronounced in summer.

In addition to the solar irradiance and ambient temperature profiles, the household load profile also plays an important role in determining the battery system operation under the self-consumption scheme. Here, a one-year load profile of typical residential household shown in Fig. 11(c) is employed. This load profile is stochastically modified based on the measurement data to represent the dynamic behavior and variation in the household load [26]. The annual energy consumption is approximately 4800 kWh/year, which represents an average 4-person household load. From the load and PV array output power profiles, the battery power can then be obtained according to the battery system control strategy.

B. Description of the Case Study

In the analysis, three case studies with different battery system control strategies are applied to the mission profile in Fig. 11. As discussed previously, the delaying charging period and limiting charging power control strategies may reduce the SCR during the day with low irradiance conditions. To minimize this drawback, the above two control strategies are not applied during the winter period (i.e., November-February), since the surplus energy during the day is already lower than the battery capacity. Instead, the control strategy similar to the maximizing self-consumption is applied to all cases during the winter period, as it is suggested in [14].

TABLE III
ACCUMULATED DAMAGE IN THE POWER DEVICE UNDER DIFFERENT BATTERY SYSTEM CONTROL STRATEGIES

Control Strategy	Accumulated Damage (per year)
Without battery system	16.2×10^{-3}
Maximizing self-consumption	15.2×10^{-3}
Delaying charging period	9.75×10^{-3}
Limiting charging power	8.05×10^{-3}

Additionally, the start charging time and the maximum charging power are the parameters that strongly affect the battery system operation for the delaying charging period and the limiting charging power control strategies, respectively. In general, using a low charging power or large delaying charging period (e.g., start charging the battery after 10:00) will further benefit the PV inverter reliability, but decrease the SCR (e.g., during low solar irradiance days). In this case study, the battery with the delaying charging period control strategy is charged after 9:00, while the maximum charging power of the limiting charging power control strategy is selected as 30% of the rated power. These parameters are selected in a way to maintain an equal SCR for both control strategies (i.e., 2% lower SCR than that of the maximizing self-consumption control strategy). By doing so, the SCR of all control strategies are comparable (resulting in a similar energy yield), and the benefit in terms of reliability improvement of different control strategies can be benchmarked.

C. Reliability Evaluation

The reliability evaluation is carried out during one-year operation, where the battery system control strategies and the mission profile are considered. The *AD* over one-year is used as a reliability metric to quantify the impact of battery system control strategies on the reliability of the PV inverter. The improvement in the PV inverter reliability can be analyzed by comparing the *AD* of the PV inverter with battery system control strategies and the case without battery system.

The *AD* of the power device in the PV inverter with different battery system control strategies is summarized in TABLE III. It can be seen that employing the maximizing self-consumption control strategy results in a comparable *AD* as the case without battery system. Thus, its effectiveness in terms of PV inverter reliability enhancement is limited. On the other hand, the delaying charging period and limiting charging power control strategies can effectively improve the PV inverter reliability, where the *AD* during operation is reduced significantly. It can be seen from the comparison in the *AD* shown in Fig. 12 that the delaying charging period control strategy can reduce the *AD* of the power device by approximately 40% compared to the case without batteries. Nevertheless, the limiting charging power control strategy is the most effective solution among the three control strategies in terms of the PV inverter reliability improvement, where more than 50% reduction in the *AD* can be achieved.

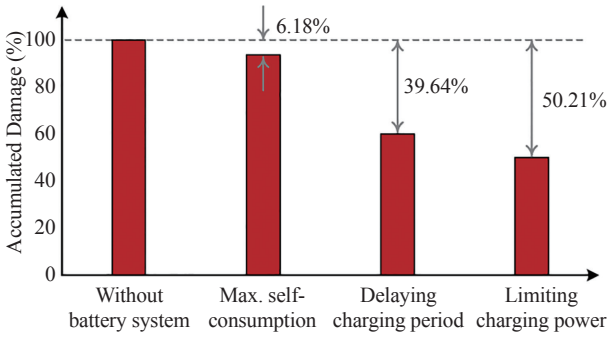

Fig. 12. Comparison of the accumulated damage of power device for different battery system control strategy over one year.

Accordingly, it can be seen that the delaying charging period and the limiting charging power control strategies are promising solutions to enhance the PV inverter reliability with a minimum reduction in the SCR (i.e., 2% lower than the maximizing self-consumption case).

VI. Conclusion

In this paper, solutions to enhance the PV inverter reliability through the control of battery system were explored. Three different control strategies for self-consumption operation were discussed, and their impact on the PV inverter loading was investigated. The loading analysis indicates that the delaying charging period and limiting charging power control strategies can reduce the peak load of the PV inverter to some extent and thereby it has high potential for the reliability improvement. The reliability assessment has shown that the limiting charging power control strategy can effectively reduce the damage of power devices by 50% compared to the case of the PV inverter without a battery system. Therefore, it has the potential to enhance the reliability of the PV inverters, and thus maximize the benefit of the integration of battery systems in PV applications.

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Electric-Vehicle Power Converters Model-Based Design-for-Reliability

Alessandro Soldati, Giorgio Pietrini, Matteo Dalboni, and Carlo Concari

***Abstract*—Fully electric vehicles are rapidly gaining user and market interest worldwide, due to their zero direct emissions, appealing driving experience and fashionable perception. Unfortunately, cost, range and reliability have not reached the desired targets yet. Since consumers are prone to spend money to have a more reliable system, Design-for-Reliability will be a useful tool for the Design of tomorrow's EVs, justifying part of the increased cost for these products. In this work, a vertical model-based approach to design-for-Reliability of power converters for EVs is presented, paying special attention to thermally-induced aging. The design starts from various driving cycles, properly assembled to describe the vehicle mission, then load profiles for the converters are found and the resulting thermal stress is quantified. The converter lifetime can be estimated, taking into account also parameter dispersion, and requirements for the active thermal control of the parts modeled achieved, thus giving practical information to the system designers.**

***Index Terms*—Design-for-Reliability, driving cycles, electric vehicles, model-based design, power converters.**

I. Introduction

ELECTRIC Vehicles (EVs) and, especially, Fully Electric Vehicles (FEVs) are gaining more attention and market share every day. Things changed a lot with respect to the recent past: Internal Combustion Engines (ICEs) are getting difficult to design to fulfill pressing limitations from the particulates and carbon dioxide points of view. In the meantime, different car makers put many EV models on the market, dispelling the myth that mobility by electric energy is unfashionable [1]-[3].

Despite this positive trend for EVs, some issues still require close attention: the charging infrastructure needs to be widened, battery performance should be improved, the cost reduced and reliability increased [4], [5]. The last two points are somehow related: design and production costs are high because sales volume is still small, but also because creating affordable EVs requires a lot of research and manufacturing effort. Moreover, the electric part of a vehicle is still perceived as unreliable by many users, even by those that drive modern yet ICE-based vehicles.

In the continuous effort to reduce both cost and time-to-market, as well as to increase safety, the automotive industry introduced massively model-based design into its project workflow [6]-[8]. Certainly, this methodology can be applied to meet all the performance metrics of a vehicle as well as to improve the design of the implementation platforms which are in charge to host the control algorithms [6]. Another advantage deriving from the model-based design consists in the possibility to lead also system-level analysis, hence increasing the integration of different physical domains which unavoidably cohabit in complex systems [7]. Moreover, such approach can be leveraged to obtain a quantitative assessment of the health and reliability of complex and distributed systems [8]. It is thus obvious that model-based design is widely accepted by car manufacturers, and that new technologies should be developed according to this paradigm. Therefore, this work, which settles in the automotive scenario, can be regarded as an effort to provide a novel design strategy of power converters from a vehicle-system-level point of view.

When reliability of modern power converters is concerned, the approach described by Design-for-Reliability (DfR), rather than reliability testing, is the preferred choice, as it has already been proposed for photovoltaics (PV) and energy systems based on renewables [9]-[11]. Indeed, for these applications life-time prediction is very important because the cost of renewable energy and hence its greater convenience over fossil energy depends directly on the number of faults and unexpected maintenance interventions which are required for the proper operation of PV and wind plants. Thus, in this work DfR is borrowed from the renewable energy field, where it represents a consolidated methodology, and it is exploited as a means to make automotive power converters more reliable and, consequently, to make EVs more desirable for consumers.

Furthermore, it is worth observing that DfR implies a paradigm switch towards the so called Physics of Failure (PoF) since this approach implies the detection of the root-causes of failure as stated in [9]-[11].

In the DfR method the designer effort is concerned with reliability from the early stages of the project. Methodologies that account for time dependent parameters and varying operating conditions are introduced, besides the more traditional, statistics-based approach.

This work proposes a possible workflow to design reliable power converters to be used in EVs, accounting also for design parameters of the vehicle that do not strictly belong to the inverter. To this aim, simulations of one year of realistic vehicle use are performed in order to determine the junction temperature profile of the power devices given the year-long

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mission profile. From the obtained temperature profile, rainflow counting and reliability models are used to finally determine the expected lifetime of the power converters. The simulation includes a set of several mechanical, electrical, and thermal parameters. The number and type of parameters used, as well as several assumptions, have been chosen in order to strike an optimal compromise between accuracy and simulation time. The parameter values have been determined from various sources, including scientific literature (for vehicle mechanical parameters) and device data sheets (for power electronic devices).

This work aims to satisfy both the manufacturer side, providing a completely model-based flow, and the user side, taking advantage of DfR to effectively guarantee lifetime and reliability performances. Similar works in this field exist; with respect to [12], more details are experienced in this work, paying special attention to models and focusing less on data collection. Comparing this work to [4], here a major effort in the powertrain modeling is undertaken, including also e-motor parameters and control.

Several of the previous works on this matter rely on motor models with a very low detail and assume a linear electrical behavior in every operating point. In order to have an accurate evaluation of the motor current request for a specific operating point, different control techniques must be considered. The approach proposed in this paper, takes into account the two main working regions of the Interior Permanent Magnet (IPM) motors: the Constant Torque Speed Range (CTSR), subject to the maximum current limit only, and the Constant Power Speed Range (CPSR), where also the maximum voltage limits have to be met.

The fitting parameters used in the reliability model (i.e. Coffin-Manson) are unavoidably affected by uncertainty, that is usually dealt with by means of Montecarlo analysis [9], [10], [11], [13], [14]. The authors of this paper present a Montecarlo analysis of the final results to analyze the effects of reliability model parameter dispersion.

All the above consider thermally induced material fatigue as the main failure mechanism; the battery, that is indeed a key part for vehicle system reliability, is neglected for now, since the focus is on power converter design. Future work should address this weakness.

II. System Requirements

A. Functional Requirements

The realization of EVs, despite being quite complex, is rooted in very simple functional requirements: the vehicle should be able to carry its passengers wherever they want, in a comfortable and inexpensive way, while assuring safety into disparate traffic and environmental conditions. The main difficulty is the determination of a clear and quantitative definition of those aspects. Comfort, environment and traffic explicit models are outside the scope of this work, but "carrying passengers to their destination" can be accounted for by means of driving cycles (DCs). DCs come from the effort to substitute complex and random processes with repeatable and deterministic quantities, without losing the statistical properties of the former [15], [16]. From the lifetime point of view, a single driving cycle is supposed to have little impact on the overall system lifespan, since durations are usually limited to half an hour; moreover, they are often not so meaningful for the real behavior of a vehicle [4]. If "standard" driving cycles are used, it is worth assuming a specific distribution of different driving cycles on a longer period. This allows to gather more variability than that available in a single, specific driving cycle, and to account for day-to-day aging of the vehicle system.

TABLE I
Physics Parameters Used into Model Equations

Symbol	Description	Unit
Δt	Simulation time step	s
ρ	Air density	kg/m^3
g	Gravity acceleration	m/s^2

B. Reliability Requirements

Reliability requirements for EVs are the same of traditional ICE cars: to achieve a wide adoption of the new form of mobility, users should have the possibility to buy a new EV while, at least, maintaining the same expected lifetime. This supports in amortizing the purchase expense, that is still higher for EVs with respect to ICE vehicles. However, it is worth pointing out that the operating costs of owning an electric vehicle can be lower than those connected to other types of vehicle [3].

Roughly, for a typical consumer, the ownership of a vehicle ranges from 10 to 15 years [2], [3]: during this period, the vehicle is expected to be healthy, safe and reliable. As a matter of fact, in the United States vehicle and powertrain manufacturers must grant a 10 years warranty, which is an apparent indication of the minimum life expectation of a generic light-duty vehicle. Consequently, also EVs are required to meet at least a comparable lifespan.

III. System Modeling

The vehicle is a complex system; hence its modeling can be a difficult task. Various degrees of detail can be retained or abandoned, depending on the desired target. In the following, the vehicle is described by four models. The first is concerned with the mission profile and the dynamic constraints, the second describes the electrical machines and their power electronic converter, then a thermal model is used to infer the temperature of the relevant parts. Lastly, proper reliability models are introduced to complete the tool collection needed for DfR in EVs. The symbols used in the following models and their descriptions and units of measure are collected in TABLE I to TABLE V.

A. Dynamic-Energetic Model

The dynamic request coming from a driving cycle can be transformed into a power request by using the dynamic-energetic

TABLE II
VEHICLE PARAMETERS USED INTO MODEL EQUATIONS

Symbol	Description	Unit
m	Vehicle mass	kg
J_w	Wheel inertia	kg m^2
J_m	EM rotor inertia	kg m^2
r	Wheel radius	m
S	Cross-sectional area of the vehicle	m^2
C_x	Drag coefficient	–
f_o	Friction coefficient, static	–
k	Friction coefficient, motion	s^2/m^2
τ	Reduction ratio motor-wheel	–
n_m	Number of e-motors	–

model presented here. It accounts for the inertia of both wheels and electric motors, the vehicle mass, aerodynamic and rolling friction. It supposes that the vehicle has n_m electric motors, each coupled to the wheels by a fixed-ratio (τ) gearbox and, possibly, a differential gear. The differential is neglected from the energetic point of view, since it is assumed ideal. This is consistent with the driving cycles not providing information about the trajectory followed by the vehicle.

Under these assumptions, the overall friction force acting on the vehicle is ascribed to rolling and aerodynamics, represented by the first and second terms of (1), respectively. There, it can be seen that a square-law dependence on the vehicle speed v exists.

$$F_\mu = (f_0 + kv^2)mg + \frac{1}{2}\rho C_x S v^2 \tag{1}$$

The power needed to change the vehicle speed in a certain amount of time depends on the frictional force that needs to be won (F_μ), the vehicle parameters and the magnitude of the speed change, as described by (2), which is obtained from the kinetic energy conservation.

$$P_{req} = \left[\left(m + \frac{4J_w}{r^2} + \frac{n_m \tau^2 J_m}{r^2}\right)\frac{\mathrm{d}v}{\mathrm{d}t} + F_\mu\right]v \tag{2}$$

The power request will be satisfied by the traction system, possibly distributed on several (n_m) motors; under the hypothesis of a straight-going vehicle, the torque (T) and speed (ω) are almost equally distributed among them. Their effective value depends also on the fixed ratio τ of the gearbox, as stated by (3).

$$\begin{aligned} T_{req} &= \frac{\mathrm{P}_{req}\, r}{n_m \tau v} \\ \omega_{req} &= \frac{vp\tau}{r} \end{aligned} \tag{3}$$

Equations (1)-(3), when fed with a speed vs. time profile, i.e. a *driving cycle*, can thus yield the torque and electrical speed request for a single e-motor inside the powertrain, keeping into account many vehicle parameters.

B. Electric Model

The electric model is devoted to project the power request on motors and power converters. The model is considered an ideal transducer (without losses), while the non-ideal behavior of the converter (motor drive) is accounted for, to obtain the thermal stress that it undergoes during the operation of the vehicle. The electric model is thus split into two parts: the inverse motor model and the inverter loss model, presented below.

1) Inverse Motor Model

In this work, the e-motor is supposed to belong to the category of IPM synchronous machines, since this is the most common choice for EVs; the generated torque can approximately be expressed as in (4), where λ_m, L_d and L_q are considered constant over the entire working range (hypothesis of linearized motor).

$$T = \frac{3}{2}p\left[\lambda_m + (L_d - L_q)i_d\right]i_q = (A + Bi_d)i_q \tag{4}$$

The second term is a simpler expression that will be used in the following to find the explicit control currents for each working point; the parameters are $A = 3p\lambda_m/2$ and $B = 3p\,(L_d - L_q)/2$. For the control currents to be determined, the relevant limits of the motor needs to be known: in this model, they are analytically determined from the motor and drive parameters themselves. The limiting values come from the maximum converter current modulus (I_{max}), the maximum phase voltage V_{max} (that descends from the DC link voltage V_{dc}, $V_{max} = V_{dc}/\sqrt{3}$) and the maximum running speed $\omega_{max} = \frac{2\pi p}{60}\omega_{rpm,max}$. The explicit limits of voltages and currents in rotating frame coordinates, with amplitude-conserving Clarke-Park transform, are expressed in (5).

$$\begin{aligned} \left|i_{dq}\right| &= \left|i_d + ji_q\right| = i_d^2 + i_q^2 < I_{max}^2 \\ \left|v_{dq}\right| &= \left|v_d + jv_q\right| = v_d^2 + v_q^2 < V_{max}^2 \end{aligned} \tag{5}$$

Firstly, starting from I_{max}, the dq-currents for the maximum torque can be determined as in (6):

$$\begin{aligned} i_{d,Tmax} &= \frac{-A + \sqrt{A^2 + 8B^2 I_{max}^2}}{4B} \\ i_{q,Tmax} &= \sqrt{I_{max}^2 - i_{d,Tmax}^2} \end{aligned} \tag{6}$$

so that the maximum torque can be easily computed as $T_{max} = (A + B_{id,Tmax})i_{q,Tmax}$. Once the maximum torque is known, the base speed can be determined as in (7). This quantity is not critical for the control, but it is a useful value for debugging the model.

$$\omega_{base} = \frac{v_{max}}{\sqrt{(\lambda_m + L_d i_{d,Tmax})^2 + (L_q i_{q,Tmax})^2}} \tag{7}$$

TABLE III
MOTOR PARAMETERS USED INTO MODEL EQUATIONS

Symbol	Description	Unit
p	Number of pole pairs	–
L_d	D-axis inductance	H
L_q	Q-axis inductance	H
λ_m	PM linked flux	V s
I_{max}	Maximum current	A
V_{dc}	DC link voltage	V
$\omega_{rpm,max}$	Maximum mechanical speed	rpm

When the torque request is below the T_{max} limit, a good control algorithm is represented by the MTPA (Maximum Torque Per Ampere) trajectory in the i_{dq} plane. This locus is obtained by equating (4) to the requested torque T_{req} , while imposing the minimum current modulus (current circle tangent to iso-torque curve). The i_q current can be obtained using (8):

$$i_q = \frac{T}{A + Bi_d} \tag{8}$$

This results in a fourth-order polynomial (9); out of the general four solutions, the one of interest is the only real and negative one.

$$B^3 i_d^4 + 3AB^2 i_d^3 + 3A^2 B i_d^2 + A^3 i_d - BT_{req}^2 = 0 \tag{9}$$

This approach allows to find the control point necessary to achieve any torque below the maximum one, with speed below the base value (CTSR operating region). It is possible to determine the operating voltage of the motor, recalling (10):

$$v_{dq} = v_d + jv_q = -\omega L_q i_q + j\omega(L_d i_d + \lambda_m) \tag{10}$$

If the threshold of (5) is exceeded, the MTPA trajectory cannot be used any longer, and the control point should be determined by the flux-weakening technique intersecting the current circle with the voltage ellipsis in the *dq* plane (CPSR operating region). This gives the polynomial (11), again with order four:

$$\begin{aligned} &B^2 L_d^2 i_d^4 + (2ABL_d^2 + 2\lambda_m L_d B^2) i_d^3 + \\ &(B^2\lambda_m^2 + 4AB\lambda_m L_d + A^2 L_d^2 - B^2 V_{max}^2/\omega^2) i_d^2 + \\ &(2AB\lambda_m^2 + 2A^2\lambda_m L_d - 2ABV_{max}^2/\omega^2) i_d + \\ &(A^2\lambda_m^2 + L_q^2 T_{req}^2 - V_{max}^2 A^2/\omega^2) = 0 \end{aligned} \tag{11}$$

In this case the desired solution is the maximum among the negative (and real) ones. If all those constraints lead to unacceptable solutions, it means that the requested operating point is unachievable by the motor. Detailed description and units of measure of the parameters of this model are reported in TABLE III.

2) Inverter Loss Model

The inverse motor model described in Section III-B-1) transforms the mechanical requests coming from the vehicle into electric requests that need to be fulfilled by the motor converter.

TABLE IV
INVERTER PARAMETERS USED INTO MODEL EQUATIONS

Symbol	Description	Unit
V_{dc}	DC-link voltage	V
f_{sw}	Switching frequency	Hz
V_c	Switch voltage drop ($I > 0$)	V
R_c	Switch on-state resistance ($I > 0$)	Ω
V_d	Switch voltage drop ($I < 0$)	V
R_d	Switch on-state resistance ($I < 0$)	Ω
E_{on}	Turn-on energy	J
I_{Eon}	Current of E_{on} measure	A
E_{off}	Turn-off energy	J
I_{Eoff}	Current of E_{off} measure	A

Those, in turn, determine the inverter losses, that are the main cause of thermal cycling of the converter itself, thus leading to material fatigue.

Inverter losses in a traditional three-phase bridge architecture for battery-supplied vehicles can be ascribed mainly to the power switches, since no large magnetic components are involved. Device losses are determined by the inverter generated waveform, the phase-shift between voltage and current (load angle) and the voltage and current moduli, as obtained from the inverse motor model. The conduction loss is described analytically by (12):

$$\begin{aligned} P_{on} = &\frac{I_0^2}{8}(R_c + R_d) + \frac{I_0}{2\pi}(V_c - V_d) + \\ &\frac{2I_0^2 V_0}{3\pi V_{dc}}(R_c - R_d)\cos\varphi + \frac{I_0 v_0}{4V_{dc}}(V_c + V_d)\cos\varphi \end{aligned} \tag{12}$$

To achieve this very concise formulation, some hypotheses were needed. Firstly, the output waveform is supposed to be a PWM-generated sinusoid, where the third-harmonic injection is neglected for simplicity. Then, each device is modeled, in the on-state, by a linear relationship (with offset) between current and voltage; four independent values are needed to properly describe the switch under positive and negative currents, since conduction losses are usually different. These values, represented by V_c, R_c, V_d and R_d in TABLE IV can describe effectively both MOSFETs and IGBTs behavior. Since V_d is the switch voltage when it carries negative current, it has a negative value, while the resistance R_c is positive. For MOSFETs, typically, $V_c = V_d = 0$ because they do not exhibit any threshold behavior, but $R_c = R_d > 0$, because their behavior with respect to current is almost symmetrical. From this it descends that the conduction loss of a MOSFET-based converter is flat and independent of the load angle, if the current conduction is symmetric in the device itself.

Equation (12) was obtained averaging, on an output sinusoid period, the mean power loss on each PWM cycle, while accounting for the current direction, that is determined by the load (motor) angle φ.

A similar averaging approach was used to determine the switching losses over a sinusoidal period. In this case a loose dependence exists on the voltage, since each commutation happens with the entire DC link voltage V_{dc}, here assumed constant.

However, during the sinusoid generation, the current changes, and as many switching events as the ratio between the switching and the fundamental frequency (f_{sw}/f_0) happen. This suggests that averaging translates into a finite sum of energy packets; this computation was done by approximating the finite sum with a definite integral, which holds approximately for f_{sw}/f_0>10. The final result is described in (13), where the datasheet values E_{on} and E_{off} are scaled by their characteristic current.

$$P_{sw} = \frac{2 f_{sw} I_0}{\pi}\left(\frac{E_{on}}{I_{Eon}} + \frac{E_{off}}{I_{Eoff}}\right) \tag{13}$$

It is shown that, at least under the given approximations, the switching loss depends only on the motor current and the switching frequency, but neither on the fundamental frequency nor on the load angle: this dependence is canceled by averaging over the output waveform. The parameters used in the model are described in TABLE IV.

C. Thermal Model

The thermal model represents the cooling system and its effects on the temperature of the parts of interest. This sub-system has a serious impact on the overall system reliability, at least for the thermally-induced faults. Four relevant points were chosen, out of which only three are non-trivial, so a three-time-constants network was initially devised. The "ambient" node (A) is kept at a constant temperature, while the other nodes are connected to each other through a simple Cauer thermal network. The non-trivial nodes are: junction (J), which is also where the power loss source is located, case (C), i.e. the device case, and the heatsink (S), that is the main source of cooling in the system.

Given the three time constants, a third-order ODE (Ordinary Differential Equation) is expected; an analytical solution is possible even in this case, but possibly complex. Moreover, the model is intended to be used to simulate an entire year of operation of a vehicle, which is quite a long period. Nonetheless, almost all driving cycles available have time base greater or equal than one second. With typical devices, the time-dependent effects of the junction and case capacitances are almost unnoticeable at this bandwidth. The system can thus be simplified, retaining all the thermal resistances and the heatsink capacitance C_s only.

The result is a simple first-order ODE, that can be straightforwardly solved for the heatsink temperature as in (14), where P_{loss} is the device power loss and $T_{s,0}$ the temperature at the beginning of the sampling period (which coincides with the narrowest driving cycle time base):

$$Ts = (R_{sa}P_{loss} + T_a)\left[1 - \exp\left(-\frac{\Delta t}{R_{sa}C_s}\right)\right] + T_{s,0}\exp\left(-\frac{\Delta t}{R_{sa}C_s}\right) \tag{14}$$

Neglecting both C_j and C_c, the case and junction temperatures are determined using only the resistance among those layers, resulting in $T_c = T_s + R_{cs}P_{loss}$ and $T_j = T_c + R_{jc}P_{loss}$. The parameters are detailed in TABLE V.

TABLE V
THERMAL PARAMETERS USED INTO MODEL EQUATIONS

Symbol	Description	Unit
R_{jc}	Junction-case thermal resistance	K/W
R_{cs}	Case-sink thermal resistance	K/W
R_{sa}	Sink-ambient thermal resistance	K/W
C_j	Junction thermal capacitance	J/K
C_c	Case thermal capacitance	J/K
C_s	Heatsink thermal capacitance	J/K
T_a	Ambient temperature	°C

D. Reliability Model

The reliability model is usually constituted by a collection of models, depending on the failure mechanisms and failing parts that are considered. These are collected from literature and computed in parallel, in order to see which is the first mechanism that determines the system failure. This technique is coherent with the PoF approach that is nowadays preferred to the older "testing for reliability" [14].

Before applying the reliability models, out of which we selected only that describing the thermal fatigue mechanism, the thermal loading of the device inside the converter should be analyzed. This can be accomplished by sound counting algorithms, among which the rainflow counting is the most renowned.

1) Rainflow Counting

Counting algorithms are used to infer the relevant number of fatigue cycles from a general mission profile. The rainflow counting used here is based on the standard [17], as implemented in the MATLAB environment. This implementation follows the three-point algorithm, but can work on a stream of data, without any specific need for sample reordering.

2) Lifetime Models for the Power Devices

When it comes to thermal fatigue in power electronics, the Norris-Landzberg model, as a modification of the basic Coffin-Manson equation to include frequency, is the flagship relationship. Despite more advanced models being available [18], the highest hurdle is represented by finding the proper parameters, that allow a precise representation of the device statistical behavior.

For this work, the expected number of cycles to failure N_f of a specific cycling, with average junction temperature $T_{j,\,avg}$ and range ΔT_j, is obtained by (15), which is the simple Coffin-Manson model:

$$N_f = C \cdot \Delta T_j^a \cdot \exp\left(\frac{E_a}{k_B T_{j,avg}}\right) \tag{15}$$

where k_B is the Boltzmann constant and C, a and E_a are the reliability parameters, which were obtained from [4]. To take into account the distribution of the various cycles, as resulting

TABLE VI
PARAMETERS USED IN THE SIMULATION PRESENTED AS EXAMPLE OF THE DESIGN WORKFLOW

$\Delta t = 1$ s	$k = 1\times10^{-4}$ s^2/m^2	$V_c = 0$ V	$R_{sa} = 0.30$ K/W
$\rho = 1.293$ kg/m^3	$\tau = 7.5$	$R_c = 4$ m	$C_j = 0$ J/K
$g = 9.81$ m/s^2	$n_m = 1$	$V_d = 0$ V	$C_c = 0$ J/K
$m = 1500$ kg	$p = 4$	$R_d = 4$ m	$C_s = 2000$ J/K
$J_w = 250 \times 10^{-3}$ kg m^2	$L_d = 300$ H	$E_{on} = 5.6$ mJ	$T_a = 20$ °C
$J_m = 15 \times 10^{-3}$ kg m^2	$L_q = 800$ H	$I_{Eon} = 300$ A	$C = 302500$ K$^{-\alpha}$
$r = 180 \times 10^{-3}$ m	$\lambda_m = 85 \times 10^{-3}$ V s	$E_{off} = 3.7$ mJ	$a = -5.039$
$S = 2$ m^2	$I_{max} = 400$ A	$I_{Eoff} = 300$ A	$E_a = 9.89 \times 10^{-20}$ J
$C_x = 0.3$	$V_{dc} = 650$ V	$R_{jc} = 0.10$ K/W	
$f_0 = 10 \times 10^{-3}$ Hz	$f_{sw} = 40$ Hz	$R_{cs} = 0.17$ K/W	

from the rainflow counting, the linear damage accumulation as described by Palmgren-Miner's rule was used [19]-[21].

IV. SIMULATION

To obtain relevant information from the models described above, some secondary tasks need to be accomplished. They involve driving cycle preparation, transient simulation post-processing and, finally, result interpretation. These steps are detailed in the following, while the values for the parameters used are collected in TABLE VI.

A. Preparation

Driving cycle preparation is essential to obtain practically relevant results. Known cycles (ARTEMIS, EU and USA ones, …) were collected and assembled in a long driving cycle (the *master cycle*), which can be regarded as a tangible element of novelty with respect to previous works. The construction procedure, in the effort to reproduce a plausible vehicle usage, accounts for relatively long stationary phases, with some driving moments interleaved. Fundamentally, the aforementioned extended driving cycle mirrors the endeavor to generate a significant virtual mission profile which is conceived to overcome the limitations of the single standard driving profiles. Indeed, as pointed out in [4], some driving cycles may lack of realism due to underestimate of maximum accelerations and, consequently they may mislead in damage assessment on power converters. Moreover, it is important to point out that rest phases in driving profiles have a paramount role for the sake of DfR of power electronics systems because they foster wide thermal cycles: these depict generally the major stressor for the electronic components [22].

The master cycle is based on three random variables: the drive/no-drive flag (P_d), the driving frame index (I_d) and the stop duration (L_s). P_d is a Bernoulli random variable, that determines, at each draw, if the vehicle will move or not in the following driving cycle. The driving probability was set to 10%, to describe roughly a 2 hour/day use of the vehicle (approximately $35\cdot10^3$ km/year), in accordance with statistics asserting that, on average, a vehicle is idling more than 90% of the time [22]. If the vehicle moves, the I_d random variable, with discrete uniform distribution, chooses one out of the available conventional driving cycles. If the vehicle rests, the L_s variable, with uniform distribution between 0 and 1, determines the rest duration in hours. At the moment, no special means to avoid driving by night is enforced, nor any feedback on the effective distance traveled.

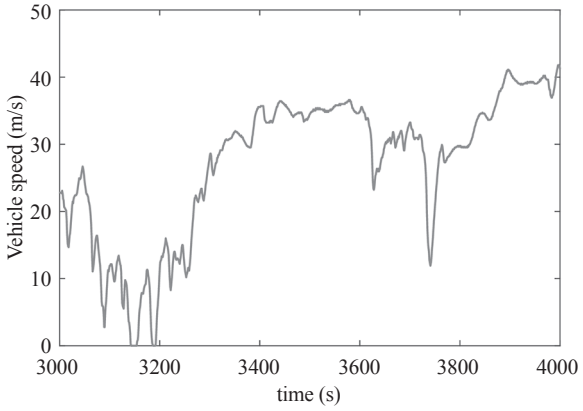

Fig. 1. Snapshot of a part of the driving cycle.

B. Post-Processing

The transient simulation, running the models of section III, determines the junction temperature profile related to the master driving cycle, together with other information, such as the heatsink temperature, the dynamic request to the motor and the electrical quantities.

After that, the junction temperature profile is analyzed by rainflow counting and the consumed lifespan for a specific set of reliability parameters was determined. Since these parameters are usually affected by a large uncertainty, a Montecarlo analysis was carried out. Hence, each parameter was changed based on a Gaussian distribution with unitary mean and variable standard deviation, and the new lifespan determined, always using the same temperature profile obtained from the simulation. This results in a specific lifetime histogram, that can be fitted to various distributions to find detailed lifetime metrics.

C. Results

The transient simulation is capable of giving many quantities of interest. Some of them are reported in Fig. 1-Fig. 5. The driving cycle (a short snapshot) is represented in Fig. 1, with the resulting mechanical power request, to be satisfied by the e-motors

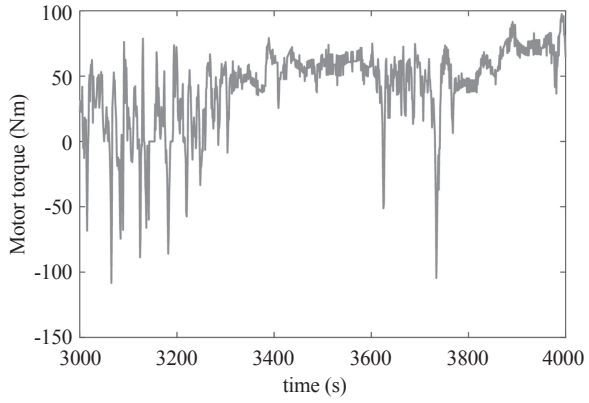

Fig. 2. Dynamic torque request corresponding to the driving cycle of Fig. 1.

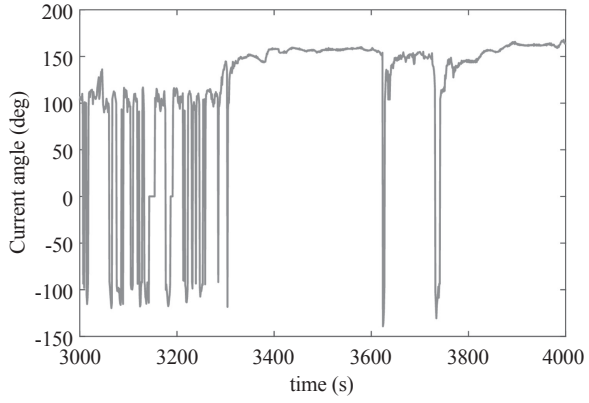

Fig. 3. Motor current angle in *dq* axes.

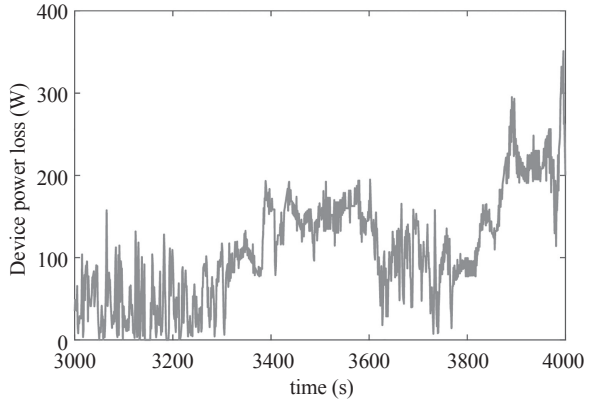

Fig. 4. Power loss on one inverter device, corresponding to the load profile of Fig. 3.

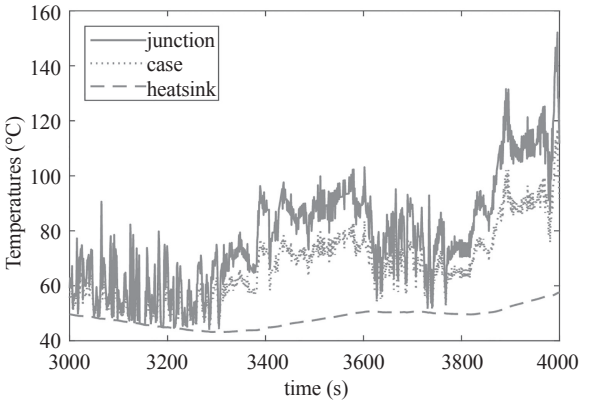

Fig. 5. Device temperatures due to the loss profile of Fig. 4.

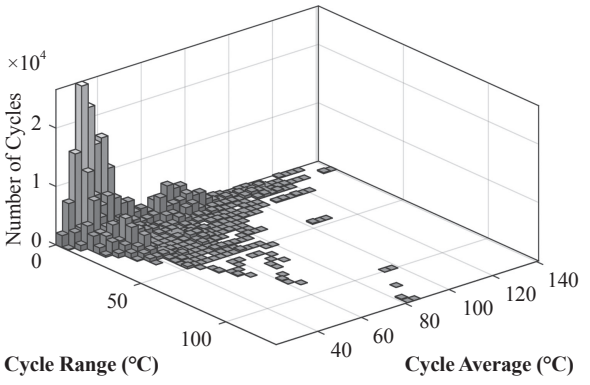

Fig. 6. Rainflow diagram of the junction temperature cycles under a one-year-long driving cycle.

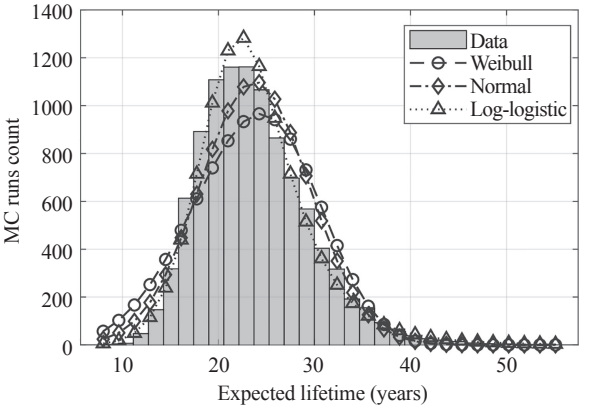

Fig. 7. Lifetime histogram from Monte Carlo simulations, with various fitting distributions.

in the powertrain, in Fig. 2. The i_{dq} current angle, used to control the motor in a rotating reference frame, is depicted in Fig. 3; the power loss of a device in the inverter is in Fig. 4. Lastly, the device temperatures (junction, case and heatsink) are outlined in Fig. 5 stroked, dotted and dashed, respectively.

The results of the rainflow counting are reported in Fig. 6. It can be seen that a specific distribution of counts, coming from the master driving cycle, is obtained. Each count is used to apply Miner's rule and the fraction of consumed lifetime.

The aforementioned post-processing results in a distribution described by the histogram of Fig. 7, where also Normal, Weibull and Log-logistic fitting distributions are represented. Fitting the Montecarlo data (10^4 runs) to specific distributions allows to determine quantitatively the lifetime metrics, with statistical meaning. In TABLE VII the B_{10} lifetime, i.e. the time after which 10% of the initial population has failed, is reported, as well as mean (μ) and standard deviation (σ). B_{10} can be sometimes more effective that a rough average value in describing the expected lifetime from a practical point of view. The distribution of Fig. 7 shows a prominent and fairly narrow peak; con-

TABLE VII
STATISTICAL CHARACTERIZATION OF THE CONVERTER LIFETIME, AS RESULTING FROM A ONE-YEAR-LONG MASTER DRIVING CYCLE AND MONTE CARLO ANALYSIS ALL QUANTITIES ARE EXPRESSED IN YEARS

Fitting	B_{10}	μ	σ
Weibull	15.2	23.6	6.3
Normal	16.5	23.8	5.7
Log-logistic	17.2	23.8	6.0

sequently, uncertainty on the lifetime model parameters does not affect significantly the lifetime estimate.

V. CONCLUSION

This paper describes a possible workflow to perform model-based Design-for-Reliability for power converters in EVs. Since it encompasses many vehicle parameters, it is able to correlate many design choices (also extraneous to the inverter itself) to the resulting lifetime change, in a statistical sense.

In the example reported here, a sufficient lifetime, also in the B_{10} sense, was achieved, suggesting the correctness of the design choices.

Further work will deal with the sensitivity analysis of the lifetime to each parameter, while including also the battery properties and other aging mechanisms, to describe not only the effects on converter life, but also for the entire vehicle reliability.

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Analysis of Electromagnetic Transient Characteristics of Doubly-Fed Induction Generator Under Grid Voltage Swell

Yonghong Deng, Zhigang Xing, and Quanzhu Zhang

***Abstract*—The electromagnetic transient characteristics (ETC) of doubly-fed induction generator (DFIG) under grid voltage dip have been extensively studied theoretically, and various control strategies have been proposed. However, the ETC of DFIG under grid voltage swell are less studied. In order to study the influence on the ETC of DFIG under grid voltage swell and the corresponding control strategy, this paper compares and analyzes the steady-state and transient components of the stator flux linkage, rotor induced voltage and rotor current of DFIG under grid voltage swell and dip. It is deduced that DFIG is less prone to rotor over-current under grid voltage swell so the crowbar protection circuit is not needed, and the grid voltage amplitude changes little, the rotor side inverter is less prone to overmodulation. An experimental setup and simulation model is implemented with high-voltage ride-through of 1.5 MW doubly-fed wind Turbine. Simulation in addition to experimental results verifies the correctness and effectiveness of the theoretical analysis.**

***Index Terms*—Doubly-fed induction generator (DFIG), electromagnetic transient characteristics (ETC), grid voltage failure, wind power generation.**

I. Introduction

In recent years, wind power generation has developed rapidly, and the amount of electricity delivered to the grid from wind power generation is also increasing. The high proportion of wind power grid-connected operation has brought great challenges to the safety and stability of power systems, and the impact of wind power accidents cannot be ignored [1]. The major wind power developed countries and regions in the world have adopted the grid-connected rules to regulate the grid-connected behavior of wind power, especially the fault-pass capability of wind power, including low voltage ride through (LVRT) and high voltage ride through (HVRT). Doubly-fed induction generator (DFIG) is the most widely used type of wind turbine generator because of its advantages of small capacity, low cost, and variable speed constant frequency operation. However, due to its stator windings directly connected to the grid, the excitation converter capacity is limited, causing it to be sensitive to grid disturbances, and in the event of a power grid failure, problems such as over-current, over-voltage, torque shock and pulsating output, and active and reactive power fluctuations are likely to occur, which seriously endanger the unit's operation safety and affect the output power quality.

For the low-voltage ride-through problem of the grid-connected operation of doubly-fed wind turbines, there has been a lot of theoretical research and engineering practice. These LVRT schemes can be summarized as hardware-based and control-based algorithms. Based on the hardware scheme, the topological structure of the doubly-fed wind power converter is implemented through additional hardware devices to improve the LVRT capability of the wind turbine [2], [3]. Based on the control algorithm, the control strategy is optimized based on the operating characteristics of the DFIG unit. Documents [4] and [5] comprehensively discuss several commonly used and improved control strategies for solving the problem of low-voltage ride-through of doubly-fed wind turbines. Aiming at the characteristics of DFIG, a large number of literatures have done in-depth research on the transient characteristics of DFIG during low-breakage faults, and given a variety of solutions. The literature [6]-[8] studied the electromagnetic transient characteristics of DFIG and the short-circuit current under LVRT control when the voltage of the power grid falls, and provided the theoretical basis for the relevant LVRT strategy. According to the transient characteristics of DFIG when voltage drops, the literature [9] is based on the idea of "demagnetization", by timely and accurately injecting the transient compensation amount on the rotor side, the controllability in the LVRT process of the unit is effectively improved, and the LVRT performance of the double-fed unit is improved. Literature [10] and literature [11] proceeded from the direction of speeding up the decay of the stator flux transients and proposed the virtual inductance demagnetization control and virtual resistance control respectively. Corresponding to the voltage drop, the voltage swell occurs when the grid voltage recovers or the grid reactive power excess time. If the unit does not consider the over-voltage protection design at this time and does not have the HVRT control capability, it must be disconnected from the power grid to generate a large-scale off-grid phenomenon of the wind turbine. At present, there are few researches on transient characteristics and related countermeasures of DFIG when the voltage of power grid is suddenly increased. Literature [12], [13] proposed an improved control

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strategy based on variable damping and virtual impedance to improve the high-voltage ride-through performance of the unit, but the article proposes a control strategy only from the theoretical analysis point of view. It does not do a detailed analysis of the changes in the electromagnetic quantities of the DFIG when the grid voltage swells, and does not consider the effect of the actual surge amplitude of the grid voltage. Considering the voltage drop and swell of the power grid, the transient processes of the stator flux linkage, rotor induced electromotive force and rotor current of the DFIG are similar. Based on the theoretical calculation, experiment and simulation verification, this paper analyzes the change process and influencing factors of DFIG electromagnetic flux when the power grid falls and swells separately, and compares the similarities and differences between the two faults. It provides theoretical support for the study of the HVRT control strategy of the double-fed unit and defines the key to the HVRT control of the DFIG unit.

II. The Mathematical Model of DFIG

In the stator stationary frame, the vector form of the doubly-fed motor voltage equation and the flux linkage equation are

$$\begin{cases} \boldsymbol{u}_s = R_s \boldsymbol{i}_s + \dfrac{d}{dt}\boldsymbol{\psi}_s \\ \boldsymbol{u}_r = R_r \boldsymbol{i}_r + \dfrac{d}{dt}\boldsymbol{\psi}_r - \mathrm{j}\omega_r \boldsymbol{\psi}_r \end{cases} \tag{1}$$

$$\begin{cases} \boldsymbol{\psi}_s = L_s \boldsymbol{i}_s + L_m \boldsymbol{i}_r \\ \boldsymbol{\psi}_r = L_r \boldsymbol{i}_r + L_m \boldsymbol{i}_s \end{cases} \tag{2}$$

(1) is the voltage equation, and (2) is the flux linkage equation. Where $\boldsymbol{u}_s$ and $\boldsymbol{u}_r$ are stator and rotor voltages, R_s and R_r are stator and rotor resistances, $\boldsymbol{i}_s$ and $\boldsymbol{i}_r$ are stator and rotor currents, respectively; $\boldsymbol{\psi}_s$ and $\boldsymbol{\psi}_r$ are fixed and rotor flux chains, ω_r is the rotor angular velocity, and L_s , L_r and L_m are stator inductance, rotor inductance and mutual inductance, respectively.

According to the voltage equation of (1), the equivalent circuit of DFIG shown in Fig. 1 can be obtained. L_{ls} and L_{lr} in Fig. 1 are stator leakage inductance and rotor leakage inductance, respectively.

III. Stator Flux Transient Analysis of Grid Voltage Swell and Drop Fault

Assume that the system is operating stably before t_0, the stator voltage at this time can be expressed as

$$\boldsymbol{u}_s = U e^{j\omega_1 t} (t < t_0) \tag{3}$$

where U is the stator voltage amplitude and ω_1 is the stator synchronous angular velocity.

If the grid voltage occurs symmetrical fault at t_0, set the grid voltage amplitude change degree p, and when $p < 0$ system voltage drop fault occurs, the drop depth is | p |; when $p > 0$, a voltage surge fault occurs and the magnitude of the

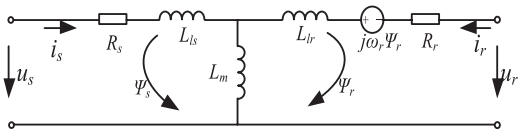


Fig. 1. Equivalent circuit of DFIG.

swell is | p | . In this process, the stator voltage can be expressed as

$$\boldsymbol{u}_s = (1+p) U e^{j\omega_1 t} (t \geq t_0) \tag{4}$$

The corresponding stator steady state flux chain expression is

$$\boldsymbol{\psi}_s = \begin{cases} \dfrac{U}{j\omega_1} e^{j\omega_1 t} & t < t_0 \\ \dfrac{(1+p)U}{j\omega_1} e^{j\omega_1 t} & t \geq t_0 \end{cases} \tag{5}$$

In the course of grid voltage faults, the stator flux linkage gradually transitions from one steady state to another because the flux cannot mutate. In order to facilitate the analysis of the transient process of the stator flux linkage when the grid voltage amplitude changes, it is assumed that the rotor is open, i.e. the rotor current is zero. Then substituting the stator flux equation in (2) into the stator voltage equation in (1) gives the stator flux differential equation

$$\frac{d}{dt}\boldsymbol{\psi}_s = \boldsymbol{u}_s - \frac{R_s}{L_s}\boldsymbol{\psi}_s \tag{6}$$

Solving this differential equation yields

$$\boldsymbol{\psi}_s = \frac{(1+p)U}{j\omega_1} e^{j\omega_1 t} + \boldsymbol{\psi}_{n0} e^{-t/\tau_s} \tag{7}$$

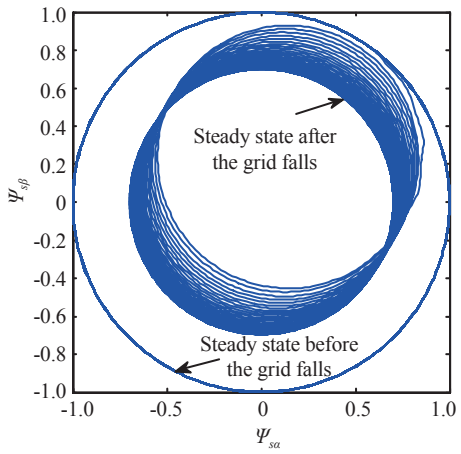
where, $\boldsymbol{\Psi}_{n0}$ is a constant related to the fault condition, $\tau_s = \frac{R_s}{L_s}$.

It is analyzed that the solution of the flux differential equation is composed of homogeneous solution and nonhomogeneous solution. Where, the non-homogeneous solution is the steady-state component of the flux linkage $\boldsymbol{\Psi}_{sn}$, its amplitude is related to the stator voltage, and its frequency is the synchronous angular frequency; the homogeneous solution is the transient decay component of the flux linkage $\boldsymbol{\Psi}_{sn}$, which reflects the continuity of the flux linkage change and is an exponentially decaying DC value.

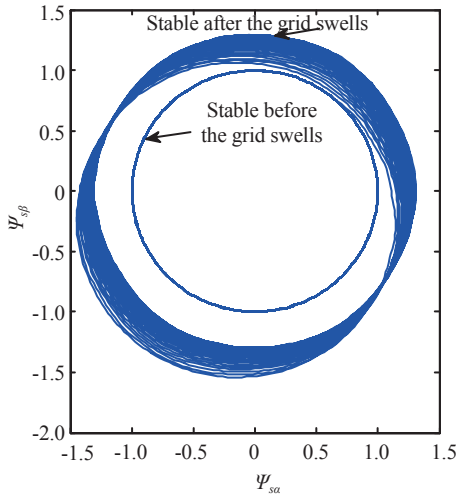
Since the instantaneous value of the flux linkage is the same before and after the grid voltage fault, there are

$$\boldsymbol{\psi}_{sf}(t_0^-) = \boldsymbol{\psi}_{sf}(t_0^+) + \boldsymbol{\psi}_{sn}(t_0^+) \tag{8}$$

Assuming that the grid voltage fault occurs at time $t_0 = 0$, the corresponding expressions in (5) and (6) are substituted into (8). After the fault occurs, the complete expression of



(a) grid voltage dip



(b) grid voltage swell

Fig. 2. Stator flux waveforms in αβ frames during grid voltage fault.

the stator flux linkage is

$$\boldsymbol{\psi}_s = \boldsymbol{\psi}_{sf} + \boldsymbol{\psi}_{sn} = \frac{(1+p)U}{j\omega_1} e^{j\omega_1 t} - \frac{pU}{j\omega_1} e^{-\frac{t}{\tau_s}} \tag{9}$$

From (9), the change process of the stator flux linkage in the αβ coordinate system is shown in Fig. 2 after the grid voltage has dropped and swelled. The steady state of the stator flux is a circle with a constant amplitude, a fixed center and a rotation at the synchronous angular frequency. When a three-phase grid voltage drop or swell failure occurs, the amplitude of the flux linkage cannot be abrupt, and under the action of the DC transient component, it gradually shifts to a new steady state in a way that the center is shifted, and steady-state pre-fault constitute concentric circles.

IV. Rotor Induced Voltage of Grid Voltage Swell and Drop Fault

After the grid voltage fails, the two components of the stator flux will each generate an induced electromotive force in the rotor, and thus a transient process will also occur in the rotor induced electromotive force. And because the output voltage controllable range of voltage source type inverter is limited, so need to consider the rotor end voltage when the voltage fault of the power grid.

According to the DFIG mathematical model, from (2) can get

$$\boldsymbol{\psi}_r = L_m \boldsymbol{\psi}_s / L_s - \sigma L_r \boldsymbol{i}_r \tag{10}$$

where: $\sigma = 1 - L_m^2/(L_s L_r)$.

Substituting (10) into (1), the expression of the rotor voltage can be obtained as

$$\boldsymbol{u}_r = L_m(d/dt - j\omega_r)\,\boldsymbol{\psi}_s/L_s + [R_r + \sigma L_r(d/dt - j\omega_r)]\boldsymbol{i}_r \tag{11}$$

The first term in (11) is the induced electromotive force generated by the stator flux on the rotor loop, denoted by $\boldsymbol{u}_{r0}$, which is the open circuit voltage of the rotor; and the second term is the impedance drop of the rotor loop.

The induced electromotive force generated on the rotor loop by the steady-state and transient components of the stator flux is denoted by $\boldsymbol{e}_{rf}$ and $\boldsymbol{e}_{rn}$, respectively, and its relationship with the open-circuit voltage of the rotor can be expressed as

$$\boldsymbol{u}_{r0} = \boldsymbol{e}_{rf} + \boldsymbol{e}_{rn} \tag{12}$$

Calculated by (9) and (11) are available

$$\begin{cases} \boldsymbol{e}_{rf} = L_m/L_s(1+p)Use^{j\omega_1 t} \\ \boldsymbol{e}_{rn} = (L_m/L_s)(pU/j\omega_1)\, e^{-t/\tau_s}(1/\tau_s + j\omega_r) \\ \quad\;\; = -(L_m/L_s)(1/\tau_s + j\omega_r)\boldsymbol{\psi}_{sn} \end{cases} \tag{13}$$

where, $s = (\omega_1 - \omega_r)/\omega_1$ is the slip ratio.

Ignoring the smaller $1/\tau_s$ terms, there are

$$\boldsymbol{e}_{rn} \approx -j\omega_r(L_m/L_s)\boldsymbol{\psi}_{sn} \tag{14}$$

Therefore, the open circuit voltage of the rotor is

$$\boldsymbol{u}_{r0} = L_m/L_s(1+p)Use^{j\omega_1 t} - j\omega_r(L_m/L_s)\boldsymbol{\psi}_{sn} \tag{15}$$

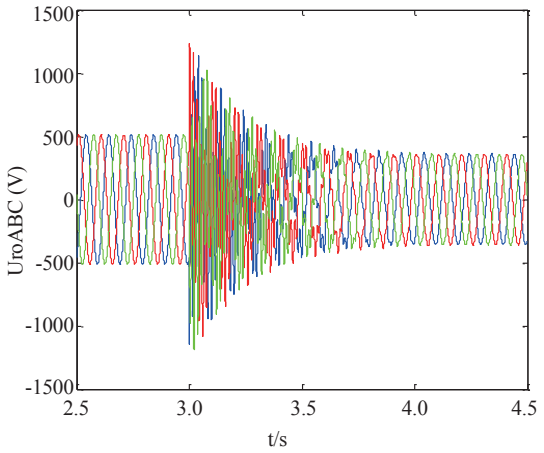
The conversion of (15) to the rotor coordinate system can be expressed as

$$\boldsymbol{u}_{ro}^r = L_m/L_s U\left[(1+p)se^{j\omega_s t} + (1-s)pe^{-j\omega_r t}e^{-t/\tau_s}\right] \tag{16}$$

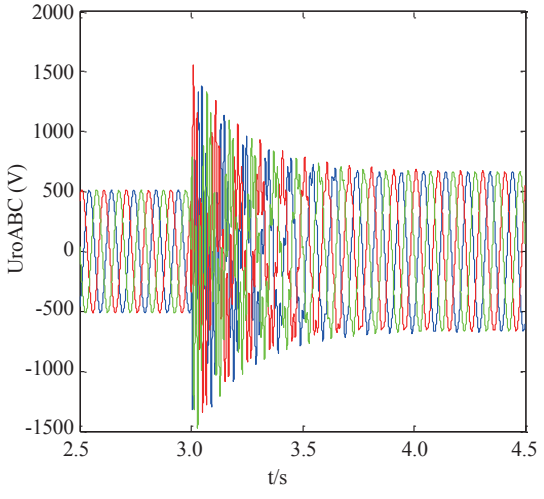
From (16), it can be seen that after the grid fault, the steady-state amplitude of the open-circuit voltage of the rotor is $1+p$ times that before the grid fault.

The transient amplitudes of the open-circuit voltage of the rotor are the same when the voltage drop fault and the swell fault of the power grid occur, and the phases are 180 degrees apart.

Simulation of the same doubly-fed generator in the open rotor case, the running slip is -0.2, when the stator voltage drop



(a) grid voltage dip



(b) grid voltage swell

Fig. 3. Rotor three-phase open circuit voltage in grid fault.

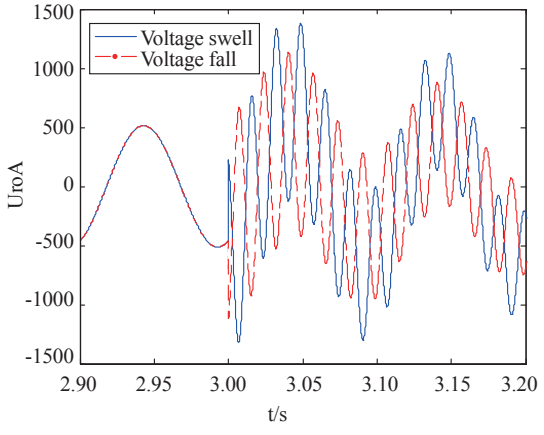


Fig. 4. A phase voltage of rotor in power grid failure.

or swell 30%, the rotor of the motor induced transient changes in the electromotive force. As shown in Fig. 3, the three-phase open circuit voltage of the rotor when the stator voltage drops and swells. It can be seen that the steady-state amplitude of the open-circuit voltage of the rotor is $1+p$ times before the fault, and the steady-state frequency is 10 Hz. In Fig. 4, taking the a-phase of the opencircuit voltage of the rotor as an example, the transient change of the open-circuit voltage of the rotor when the stator voltage is dropped or swelled separately at 3 s is compared. As can be seen from the figure, the transient amplitudes of the open-circuit voltages of the rotors are equal in both cases and the phases are 180 degrees out of phase. In the case where the slip is -0.2, the frequency of transient components in the rotor coordinate system is 60 Hz.

V. Rotor Current of Grid Voltage Swell and Drop Fault

When the double-fed unit is operating normally, the influence of rotor current should be considered. The expression of the rotor voltage in (11) in the stator coordinate system is transformed into a synchronous rotating coordinate system, finally get

$$\sigma L_r \frac{d\boldsymbol{i}_{r,dq}}{dt} + (R_r + j\omega_s \sigma L_r)\boldsymbol{i}_{r,dq} = \boldsymbol{u}_{r,dq} - \boldsymbol{u}_{r0,dq} \quad (17)$$

where, the subscript dq in $\boldsymbol{i}_{r,dq}$, $\boldsymbol{u}_{r,dq}$, $\boldsymbol{u}_{r0,dq}$ represents the value of this vector in dq synchronous rotating coordinate system, $\boldsymbol{u}_{r0,dq} = L_m / L_s U\,[(1+p)s + (1-s)\,pe^{-j\omega_1 t}e^{-t/\tau_S}]$. $\boldsymbol{u}_{r,dq}$ is the AC output voltage of the rotor side converter, which reflects the influence of the control performance of the rotor side converter on the rotor current. From (17), it can be seen that when the grid fault occurs, the rotor current change is determined by both the stator flux linkage and the rotor-side converter, and the interaction relationship is related to the generator electromagnetic parameters and the rotation speed. The rotor-side converter changes the AC-side output voltage according to the active and reactive control strategy to track the set rotor current, and the rotor current can be approximated as a reference value. After the grid fails, it is assumed that the capacity of the converter is sufficiently large and the rotor crowbar protection does not act. The size of the rotor voltage is affected by the rotor-side converter control system. The rotor-side converter control of DFIG often adopts vector control mode of stator flux orientation, and the decoupled control of active and reactive power is achieved by means of feedforward compensation of coupling terms. Fig. 5 shows the control block diagram of the rotor-side converter. i^*_{rd} and i^*_{rq} are the reference values of the d, q-axis current components of the rotor, respectively, and are determined by the reference values of the active and reactive power. u^*_{rd} and u^*_{rq} are the rotor voltage reference values needed to track the rotor current.

From Fig. 5, the control equation is

$$\begin{cases} u^*_{rd} = k_p \Delta i_{rd} + k_i \int \Delta i_{rd} dt - \omega_s \sigma L_r i_{rq} \\ u^*_{rq} = k_p \Delta i_{rq} + k_i \int \Delta i_{rq} dt + \omega_s \sigma L_r i_{rd} \end{cases} \quad (18)$$

where, $\Delta i_{rd} = i^*_{rd} - i_{rd}$, $\Delta i_{rq} = i^*_{rq} - i_{rq}$, k_p and k_i are the ratios and

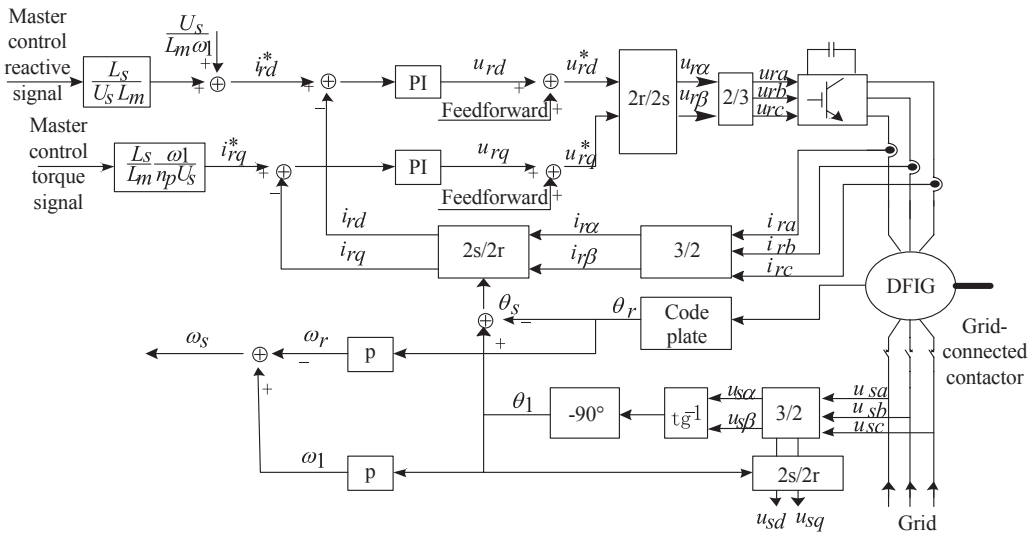


Fig. 5. Stator flux oriented VC control diagram of DFIG.

integral coefficients of the current loop controller, respectively.

Assuming that the closed-loop bandwidth of the current control loop is large enough, the voltage on the AC side of the converter can track the reference value without any error, and the switching transients are ignored, then the rotor voltage space vector in the synchronous rotating coordinate system when the power grid fails can be written as

$$\boldsymbol{u}_{r,dq} = k_p + k_i \int \left(\boldsymbol{i}^*_{r,dq} - \boldsymbol{i}_{r,dq}\right) + j\omega_s \sigma L_r \boldsymbol{i}_{r,dq} \quad (19)$$

Combining (17) and (19), considering the influence of stator flux and converter control system on rotor current, the rotor current dynamic equation after grid short circuit can be obtained

$$\frac{d^2 \boldsymbol{i}_{r,\mathrm{dq}}}{dt^2} + \mu \frac{d\boldsymbol{i}_{r,dq}}{dt} + \nu \boldsymbol{i}_{r,dq} = \nu \boldsymbol{i}^*_{r,dq} - \lambda \boldsymbol{e}_{rn,dq} \quad (20)$$

where, $\mu = (R_r + k_p)/\sigma L_r$; $\nu = k_i/\sigma L_r$; $\lambda = (j\omega_1 + 1/\tau_s)/\sigma L_r$; $\boldsymbol{e}_{rn,dq} = L_m/L_s U(1-s) p e^{-j\omega_1 t} e^{-t/\tau_s}$.

According to the principle of solving the second-order constant-coefficient differential equation and solving the differential equation in (12), the rotor current under the combined action of the rotor induced electromotive force and the rotor-side converter control can be obtained:

$$\boldsymbol{i}_{r,\mathrm{dq}} = \boldsymbol{i}_{rf,\mathrm{dq}} + \boldsymbol{i}_{rn1,\mathrm{dq}} + \boldsymbol{i}_{rn2,\mathrm{dq}} \quad (21)$$

$\boldsymbol{i}_{rn1,\mathrm{dq}}$ is the special solution of the differential equation at the input $\nu \boldsymbol{i}^*_{r,dq}$, that is the forced component of the rotor current and is the response of the rotor current to the control quantity of the rotor-side converter. According to the previous assumption that the closed-loop bandwidth of the current control loop is large enough, there are

$$\boldsymbol{i}_{rn1,\mathrm{dq}} = \boldsymbol{i}^*_{r,dq} \quad (22)$$

$\boldsymbol{i}_{rn2,\mathrm{dq}}$ is the special solution of the differential equation at the input $-\lambda \boldsymbol{e}_{rn,dq}$ and is the response of the rotor current to the transient dc back-EMF component $\boldsymbol{e}_{rn,dq}$

$$\boldsymbol{i}_{rn2,\mathrm{dq}} = -\frac{\lambda \boldsymbol{e}_{rn,dq}}{\tau_s'^2 - \mu\tau_s' + \lambda} = -\frac{\lambda L_m U(1-s) p e^{-\tau_s' t}}{L_s(\tau_s'^2 - \mu\tau_s' + \lambda)} \quad (23)$$

where, $\tau'_s = j\omega_1 + 1/\tau_s$.

$\boldsymbol{i}_{rf,\mathrm{dq}}$ is the general solution of the second-order differential equation, which is the natural component of the rotor current and is related to the current $\boldsymbol{i}_{r0,\mathrm{dq}}$ when the rotor is operating normally

$$\boldsymbol{i}_{rf,\mathrm{dq}} = \frac{r_1 e^{r_2 t} - r_2 e^{r_1 t}}{r_1 - r_2} \boldsymbol{i}_{r0,dq} \quad (24)$$

where, r_1 and r_2 are the characteristic roots of differential equations.

$$r_{1,2} = \frac{-\mu \pm \sqrt{\mu^2 - 4\nu}}{2} \quad (25)$$

From the above derivation we can see that under the controllable conditions of the rotor-side converter, the rotor current contains the periodic component and the transient dc component. Among them: The steady-state component $\boldsymbol{i}_{rn1,\mathrm{dq}}$ is the periodic component of the rotor current, the value of which is determined by the output control strategy of the rotor-side converter; the transient component $\boldsymbol{i}_{rf,\mathrm{dq}}$ is the natural component of the rotor current and is only related to the parameters of the generator and the converter; the transient dc component $\boldsymbol{i}_{rn2,\mathrm{dq}}$ is generated by the rotor's transient dc back-EMF, and its magnitude is related to the voltage drop and speed of the machine terminal, which reflects the influence of the voltage amplitude change on the rotor current when the grid voltage fails. Of the three components of the rotor current, only $\boldsymbol{i}_{rn2,\mathrm{dq}}$ is related to the magnitude p of the grid voltage change. It can be seen from the expression of $\boldsymbol{i}_{rn2,\mathrm{dq}}$ that if other control conditions are not changed, when the grid voltage drops or swells by the same

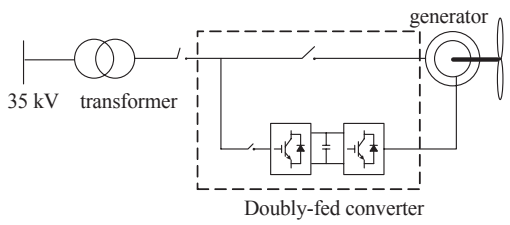
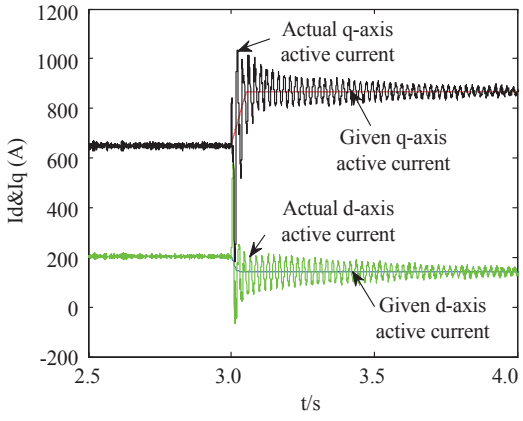
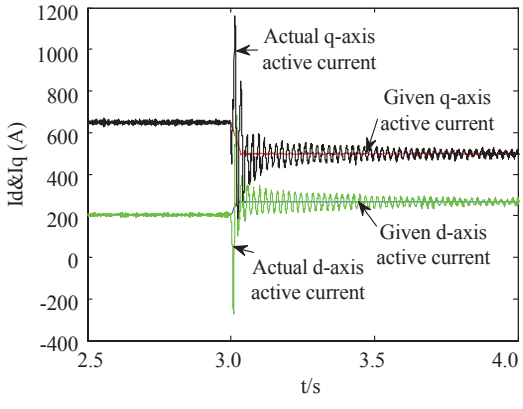


Fig. 6. Experiment and simulation structure diagram of DFIG.



(a) grid voltage dip



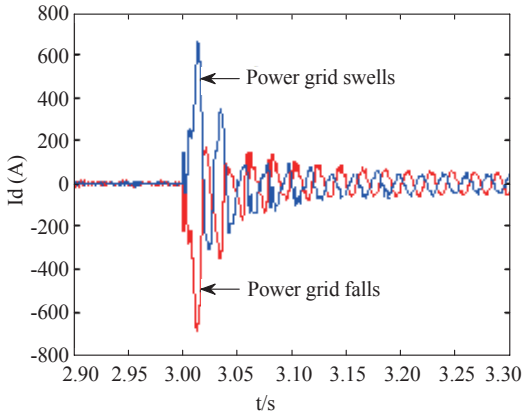
(b) grid voltage swell

Fig. 7. Rotor current in dq frame with 30% change in grid voltage amplitude.

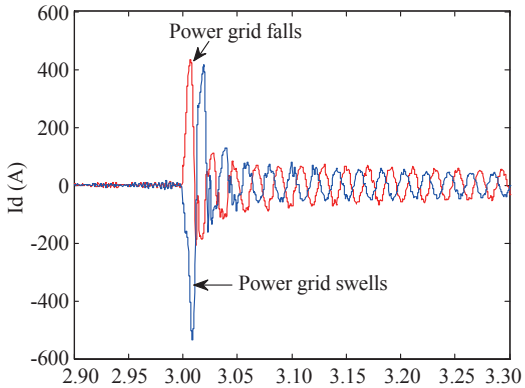
magnitude, the amplitude of the rotor current changes caused by the transient dc component of the stator flux is the same, but the phase difference is 180 degrees. In addition, (23) shows that, considering the influence of the rotor-side converter, the magnitude of the transient DC component of the rotor current is also closely related to the control parameters of the rotor-side converter.

The 1.5 MW double-fed converter experiment and simulation system is shown in Fig. 6. The parameters of the generator used are: stator rated voltage is 690 V; rotor open circuit voltage is 1900 V; stator resistance is 0.015 4 Ω; rotor resistance is 0.003 3 Ω; the stator leakage inductance is 0.034 Ω; the rotor leakage inductance is 0.029 7 Ω; the magnetizing inductance is 1.2 Ω; the rotor speed is 1800 rpm; the proportional constant of the rotor side current transformer PI current controller is 5, and the integral constant is 0.05.

As shown in Fig. 7, when the grid voltage drops by 30%



(a) Iq



(b) Id

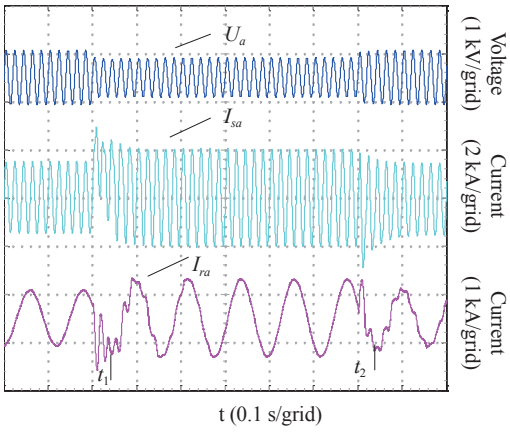
Fig. 8. Rotor current in dq frame of power grid swell and drop.

and swells by 30%, respectively, the rotor dq axis current is given and actual value based on the synchronous rotation coordinate system of the stator flux linkage orientation. When the power grid fails, the rotor dq-axis current superimposes a transient current component whose main frequency is 60 Hz and whose amplitude gradually decays.

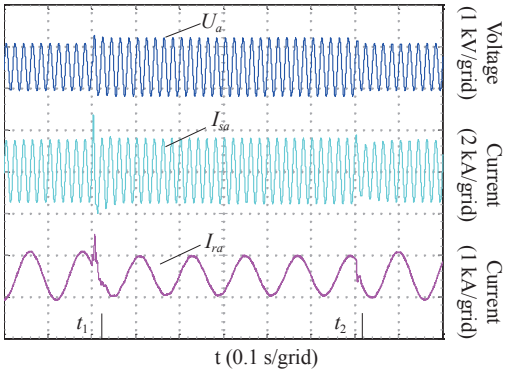
Fig. 8 shows the comparison of the transient current component of the dq axis of the rotor after the same amplitude (30%) of drop and swell failure occurred at the same time, confirming the theoretical analysis results, that is, the grid voltage fault affects the transient decay component of the rotor current $\boldsymbol{i}_{rn2,dq}$.The rotor transient current amplitude caused by the two faults is equal and the phase difference is 180 degrees. However, since the rotor current is also superimposed with the natural component $\boldsymbol{i}_{rf,dq}$, which is the amount related to the current $\boldsymbol{i}_{r0,dq}$ when the rotor is in normal operation, thus, the amplitude of the rotor transient current under the two grid faults is not exactly equal, and the phase is not exactly 180 degrees out of phase.

VI. Experiment Verification

Fig.9 shows high and low voltage ride through fault results of 1.5 MW doubly-fed converter. Fig.9(a) shows the experimental waveforms for DFIG current and voltage when



(a) Experimental waveforms for DFIG current and voltage when the grid voltage drop to 70%.



(b) Experimental waveforms for DFIG current and voltage when the grid voltage swelling to 130%.

Fig. 9. High and low voltage ride through fault results of 1.5 MW doubly-fed converter.

the grid voltage drop to 70%, and (b) shows the experimental waveforms for DFIG current and voltage when the grid voltage swelling to 130%. Where U_a is A phase grid voltage, I_{sa} is A phase stator current, I_{ra} is A phase rotor current, t_1 is the grid fault start time, t_2 is the grid voltage recovery moment. Fig.9 show that the experimental results are consistent with the theoretical analysis when the grid voltage is reduced by 30% or increased by 30%.

VII. Conclusion

By comparing the generator's electromagnetic transients during grid voltage dips and swell faults, it can be concluded that:

1) After two kinds of faults, the steady-state amplitude of the stator flux linkage、rotor open circuit voltage and rotor current is related to the magnitude of the voltage after the fault. Among them, the steady-state amplitude after the stator flux linkage and the open circuit voltage fault is (1+p) times before the fault.
2) The amplitudes of the transient attenuation components of the stator flux linkage, rotor open circuit voltage, and rotor current under the two faults are equal, and the attenuation speeds are the same and the phases are 180 degrees out of phase.
3) The most severe situation of the grid voltage drop is that the voltage drops to 0, that is, p = −100%. And the most severe situation of the grid voltage swell is p = 30%, so the grid voltage swell without causing a particularly strong electromagnetic transient state process. From the conclusion in 2), it can be seen that when high-voltage ride through is performed on a unit that already has low-voltage ride through capability, only the influence of the phase of the transient component needs to be considered in the low voltage ride-through electromagnetic transient suppression strategy.
4) Since the steady-state amplitude of the open-circuit voltage of the rotor is approximately s (slip rate) times the magnitude of the stator voltage, the s of a doubly-fed machine is generally between −0.25 and 0.25, and the amplitude of the sudden rise p is up to 30%. From (16), $\boldsymbol{u}^r_{ro,\max} = 0.55\, L_m / L_s\, U$ is known, so the rotor side converter is less prone to overmodulation.

This paper only compares the changes of the electromagnetic quantity of the generator when the grid voltage drops and swells, and does not consider the control of the grid-side converter. Since the grid-side converter is directly connected to the grid, when the grid voltage suddenly rises to 1.3 times the high voltage, it is necessary to consider withstand voltage capability of the components of the grid-side converter, especially the power unit. Moreover, it can be known from the vector control theory that the high voltage on the AC side causes overmodulation of the converter, resulting in uncontrollable current. In view of the possible over-modulation of the grid-side converter, the method of dynamically adjusting the DC bus voltage reference and controlling the network side to absorb reactive power to reduce the voltage of the AC side terminal can be improved.

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High Bandwidth Non-Resonant High Voltage Generator for X-Ray Systems

Michael Leibl, Johann W. Kolar, and Josef Deuringer

***Abstract*—High-voltage supplies for medical X-ray systems require up to 150 kV DC at up to 100 kW to supply the tube. The challenge for the power supply however is not only to deal with the high voltage and high power demand, but also to provide short voltage rise- and fall times in the range of 100µs. A coupled interleaved circuit variant of a single active bridge concept, the coupled interleaved single active bridge converter, is demonstrated in this work providing very fast output voltage control due to its non-resonant structure. The conduction modes of the circuit are analysed in detail and compared to the uncoupled interleaved single active bridge approach, demonstrating the advantages of low inverter RMS current, zero voltage switching (or at least zero current switching) over the full operating range with constant switching frequency. Analytic expressions for the output current-duty cycle relationship are provided. Experiments on a 60 kW (low voltage equivalent) prototype show that rise times as low as five switching cycles are possible, allowing to reach the target of 100µs rise time using a switching frequency of only 50 kHz.**

***Index Terms*—DC-DC power conversion, high bandwidth, high voltage generator, X-ray generator.**

I. Introduction

X-RAY tubes used for diagnostic purposes require accelerating voltages of up to 150 kV but are at the same time relatively inefficient. Only ≈1% of the energy used for accelerating the electrons is actually emitted in form of Bremsstrahlung (X-rays) [1]. Therefore, the power demand of medical X-ray tubes ranges from a few kW for dental imaging to more than 100 kW for computed tomography (CT) applications. The major part of the power is dissipated as heat at the anode which is typically a composite of tungsten and copper or molybdenum in order to withstand high temperatures [2]. Due to the surrounding vacuum, cooling capability of the tube is limited and thus also the average power that needs to be provided by the high voltage supply is typically less than 1 kW. Consequently the high voltage transformer is usually not dimensioned for full power continuous operation. Instead high power density transformer designs are common, resulting in a relatively high leakage inductance due to the high number of turns and the required winding isolation distance. Despite the high output voltage, high power transfer and high transformer leakage inductance fast output voltage dynamics are desired. Short output voltage rise- and fall times also allow short pulses to be generated which is beneficial to reduce the patient dose in pulsed fluoroscopy [3]. Another application that benefits from shorter pulses is dual energy CT. Most of nowadays' dual energy systems are equipped with two X-ray tubes emitting radiation at two different energies, typically by applying 80 kV to one and 140 kV to the other tube. A different approach is to use a single tube (single source) which is switched between two voltage levels, requiring rise- and fall times of less than 100 µs [4]. Besides eliminating one tube single source dual energy CT also reduces the patient dose [5]. Although recent achievements in SiC semiconductor technology offer diode break-down voltages up to 35 kV [6], [7], the secondary side of the high-voltage DC-DC converter is typically involving multiple diode rectifier stages connected in series in order to reduce the winding capacitance. Therefore, topologies employing transistors on the secondary side are not feasible due to the excessive gate driver and isolation circuit overhead. The only way to achieve low output voltage fall time is to reduce the output capacitance. For a given voltage ripple specification this can be achieved by increasing the switching frequency or by using interleaving [8]. Therefore, in order to reach a high switching frequency a low switching loss zero voltage switching (ZVS) or zero current switching (ZCS) topology is required for the high-voltage generator. Additionally, the circuit needs to work with high transformer leakage inductance, should provide the possibility of interleaving and should exhibit favorable dynamics for output voltage control.

In this work a coupled interleaved variant of the single active bridge converter (CISABC) is proposed that meets these demands. In Section II the topology is derived first from the uncoupled interleaved single active bridge converter (ISABC) and the steady state operation is analysed in detail. Experimental results obtained on a full-scale hardware prototype are provided in Section III verifying the analysis. Analytic expressions for the duty cycle-output current relationship are provided in the Appendix.

II. Steady-State Analysis

The complete circuit of the high voltage generator proposed in this work is shown in Fig. 1 together with an active three-phase rectifier providing a stabilized DC-link voltage to the inverter and sinusoidal input currents to the mains [9]. At the primary side each of the two inverters, which are operating with 90° phase shift, feeds a series connection of two primary windings, wound on two different transformer cores. Each inverter consists of two series connected half-bridges which, with an additional DC-blocking

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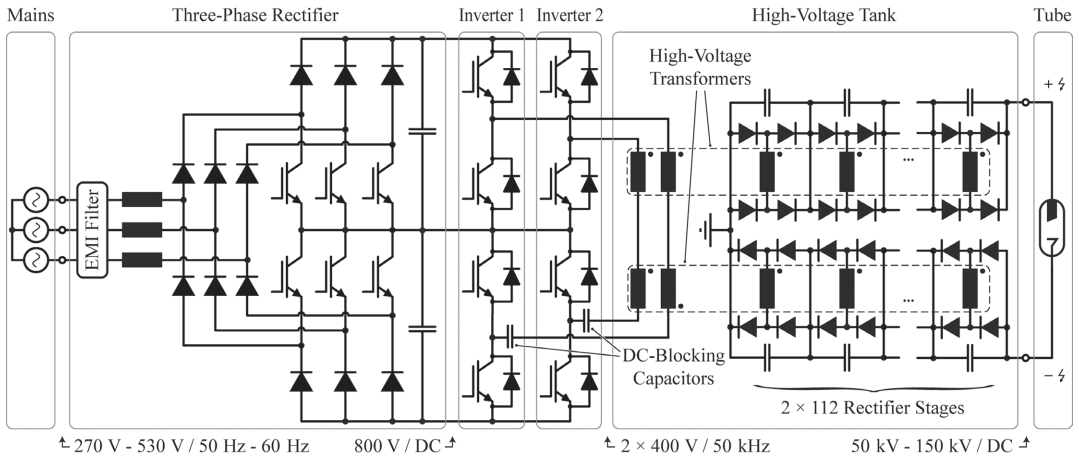


Fig. 1. Circuit of the proposed high voltage generator, consisting of a wide input voltage range active three-phase mains rectifier, providing a stabilized DC voltage for two interleaved inverters, feeding two transformers, each equipped with 112 series connected secondary winding rectifier units, supplying up to 150 kV and up to 60 kW to the X-ray tube.

capacitor, are working as a full-bridge. The separation and series connection of the half-bridges is advantageous for the given application, since it allows the use of low switching loss, low cost 650 V IGBTs for the inverters.

At the secondary side each of the two transformers uses 112 secondary windings, each connected to an individual rectifier stage. Similarly to diode split transformers used in CRT monitors this approach reduces the AC winding capacitance to a negligible value [10]. The winding capacitance is therefore not considered in the analysis and an equivalent secondary winding is used for the following circuit analysis. The proposed high voltage generator uses a coupled interleaved version of the single active bridge converter (SABC). Before analysing the steady-state operation of the CISABC in detail the ISABC, i.e. the converter without the additional coupling of the CISABC is analysed.

A. Interleaved Single Active Bridge Converter (ISABC)

The circuit of the ISABC is shown in Fig. 2, consisting of two full-bridge inverters at the primary and two full-bridge diode rectifiers at the secondary side. The two half-bridges of each inverter are distributed on the two parts of the primary DC-link, using DC-blocking capacitors. Therefore, the two inverters can be considered as parallel connected. The two rectifiers are connected to two series connected DC-links at the secondary side. Therefore, an input parallel output series connection results. Each of two independent transformers links one inverter with one rectifier. The inverters are operated with 90° phase-shift. The first harmonics of the two secondary side DC-link voltage ripples, which occur at twice the switching frequency f_s, are phase shifted by 180° and, therefore, cancel out due to the series connection. Accordingly, the total output voltage U_o only contains ripple components with $4f_s$ and higher. Therefore, a relatively small DC-link capacitance can be used. The steady state behavior of the SABC as described in [11], [12] is briefly reviewed in the following for the case of the ISABC since it serves as reference for the comparison with the CISABC which

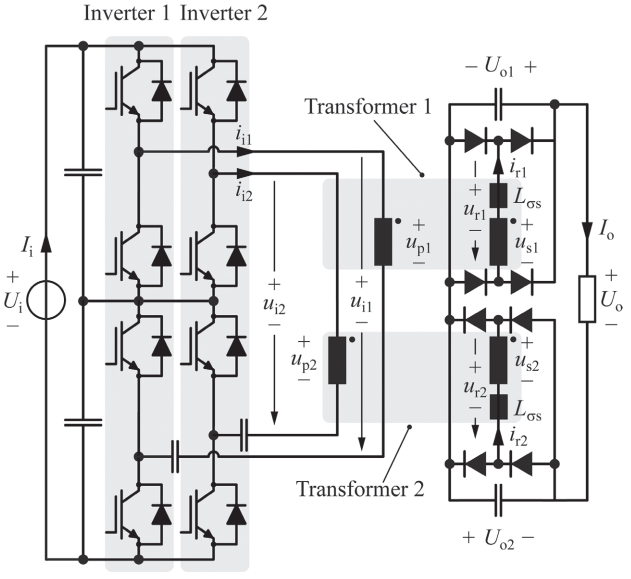


Fig. 2. ISABC circuit in input parallel output series (IPOS) configuration with the two half bridges of each full-bridge inverter distributed on two split DC-links and two full-bridge diode rectifiers connected to two series connected DC-links on the secondary side, linked via two transformers with leakage inductances $L_{\sigma s}$ (reflected to the secondary side).

is introduced in Section II-B.

1) Operating Principle

The only passive elements relevant for the operation of the ISABC are the two leakage inductances of the transformers, represented as lumped elements $L_{\sigma s}$ on the secondary sides. Otherwise the transformers are considered ideal, i.e. the magnetizing inductances are neglected, since they are not essential for the operation. The inverter switching frequency is assumed to be constant, although it could also be employed as control parameter [13]. However, a constant switching frequency is desired since the projected system is operating at a, for IGBTs relatively high, switching frequency of 50 kHz. The output voltage control is therefore solely achieved by varying the inverter duty

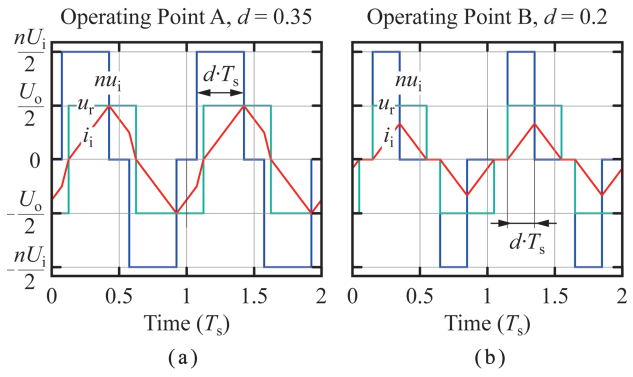


Fig. 3. Steady-state waveforms of one of the two SABCs of the ISABC in CCM (a) and DCM (b) for $\frac{U_o}{nU_i} = 0.5$.

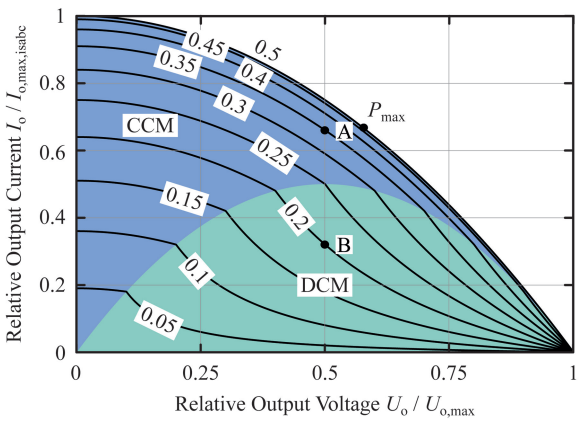


Fig. 4. ISABC output current-output voltage characteristic for different values of duty cycle including the operating points A and B for the waveforms shown in Fig. 3.

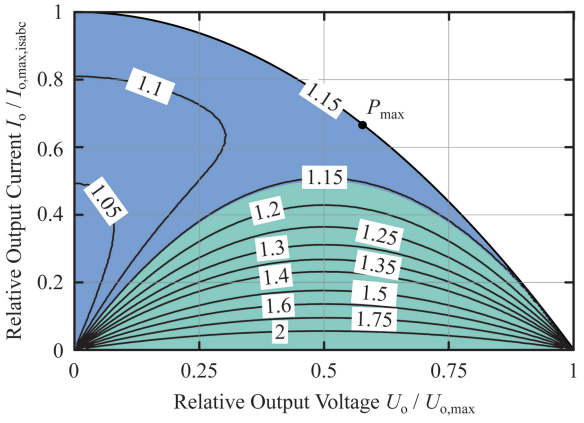


Fig. 5. ISABC RMS inverter current to DC output current ratio.

cycle $d \in [0, 0.5]$.

2) Output Current Characteristic

It is assumed that both SABCs of the ISABC operate with the same duty cycle. At high duty cycle values each of the two SABCs operates in continuous conduction mode (CCM) with typical waveforms as shown in Fig. 3(a). In CCM the steady state output current of the ISABC is derived as

$$I_{\mathrm{o,ccm}} = \frac{nU_\mathrm{i}}{16 f_\mathrm{s} L_{\sigma\mathrm{s}}}\left(4d(1-d) - \left(\frac{U_\mathrm{o}}{nU_\mathrm{i}}\right)^2\right) \tag{1}$$

If the duty cycle is less than

$$d = \frac{U_o}{2nU_\mathrm{i}}, \tag{2}$$

discontinuous conduction mode (DCM), as shown in Fig. 3(b), is entered. The steady-state output current in DCM is derived as

$$I_{\mathrm{o,dcm}} = \frac{nU_\mathrm{i}}{2 f_\mathrm{s} L_{\sigma\mathrm{s}}}\left(\frac{nU_\mathrm{i}}{U_\mathrm{o}} - 1\right) d^2. \tag{3}$$

The steady state output current-output voltage characteristic of the ISABC is shown in Fig. 4 for different duty cycles. The regions of CCM and DCM are highlighted showing that a wide operating range is covered by DCM operation. The maximum output current is supplied at the maximum duty cycle $d = 0.5$ and zero output voltage (short circuit), it amounts to

$$I_{\mathrm{o,max,isabc}} = \frac{nU_\mathrm{i}}{16 f_\mathrm{s} L_{\sigma\mathrm{s}}}. \tag{4}$$

The maximum output voltage $U_{\mathrm{o,max}} = nU_\mathrm{i}$ is reached at zero output current (open circuit).

3) Inverter RMS Current

For the calculation of the inverter conduction loss and the transformer winding loss, the inverter root mean square (RMS) current is essential. Fig. 5 shows the RMS inverter current to DC output current ratio of the ISABC. In the CCM region, the ratio is less than $\frac{2}{\sqrt{3}} \approx 1.15$, whereas in DCM the inverter RMS current to DC output current ratio increases dramatically causing high conduction loss. Together with the fact that the maximum output power is reached at relatively low output voltage, therefore at relatively high output-and inverter current, this is the major drawback of the ISABC. This disadvantage can be overcome using a series resonant converter (SRC) [15]. However, the SRC, due to its integrating plant [16], requires more sophisticated control such as cascaded control which is relatively slow, or optimum trajectory control (OTC) which is relatively complex [17]. Compared to that the direct duty cycle-output current relationship (1), (3) of the ISABC allows direct (single control loop) output voltage control. Another solution to reduce the RMS current of the ISABC is to use an inductive output filter [18]. However, due to the high output voltage the filter inductor needs to be split up into one inductor per rectifier stage which is not feasible due to the high number of rectifier stages.

4) Inverter Switched Current

The ISABC offers ZVS on both inverter half-bridges in CCM. In DCM ZVS is only achieved on the leading half-bridge, i.e. the half bridge which is the one causing the first of the two rising and falling edges (Fig. 3(b)). The lagging half-bridge achieves still ZCS in DCM at constant switching

frequency. In comparison the switching frequency of a SRC would need to be varied by a factor of two to obtain ZVS or at least ZCS over the full operating range [19].

B. Coupled Interleaved Single Active Bridge Converter (CISABC)

The CISABC provides a solution to maintain the advantages of the ISABC over the SRC, i.e. ZVS with constant switching frequency and direct output voltage control, while reducing the inverter RMS current. The basic idea is illustrated in Fig. 6. By limiting the inverter duty cycle of a ISABC to 25% the numbers of turns on both sides of the transformers can be cut in half, thus reducing the stray inductances and increasing the output current at 25% duty cycle by a factor of four (Fig. 6(a) - without increasing the peak flux density in the core. Compared to the maximum output current with 50% duty cycle more output current can be transferred if the duty cycle is limited to 25% for all output voltages.

The CISABC achieves these 25% duty cycle voltages at the transformer primary windings using two primary windings on each transformer and connecting them to the inverters as shown in Fig. 7. Because, inverter voltage 1 is the difference and inverter voltage 2 the sum of the two transformer primary voltages, the transformer primary voltages have to exhibit a 25% duty cycle shape as shown in Fig. 6(b) (neglecting the primary leakage inductances for the meantime). The advantage of this circuit is that the secondary side amp-turns are now shared by the two primary windings. Since, the secondary currents, as well as the voltages, are 90° phase shifted this does not cut the inverter currents in half but still reduces them by a factor of $\sqrt{2}$. The following analysis proves this point and considers also the primary leakage inductances which have been neglected up to now.

1) Operating Principle

All three windings of one transformer are wound around the same magnetic path with N_p turns on each primary winding and $N_s = nN_p$ on each secondary winding. The windings of the high voltage transformer are coaxially arranged with one primary winding closest to the core, directly enclosed by the next primary winding and finally with 12.5 mm isolation distance surrounded by the secondary winding. Therefore, the transformer model includes two slightly different primary leakage inductances $L_{\sigma pa}$ and $L_{\sigma pb}$ and the dominating secondary leakage inductance $L_{\sigma s}$.

Due to the symmetry (two inverters, transformers and rectifiers) of the circuit, voltage and current pairs are summarized using vector notation. E.g. the inverter and the rectifier current vectors with the notation of Fig. 7 are expressed as

$$\vec{i}_i = \begin{bmatrix} i_{i1} \\ i_{i2} \end{bmatrix}, \vec{i}_r = \begin{bmatrix} i_{r1} \\ i_{r2} \end{bmatrix}. \tag{5}$$

The secondary current of transformer 1 is the sum of the two primary currents divided by the turns ratio and the secondary current of transformer 2 is the difference of the second primary current and the first primary current divided by the turns ratio. Therefore, the rectifier current vector is expressed as

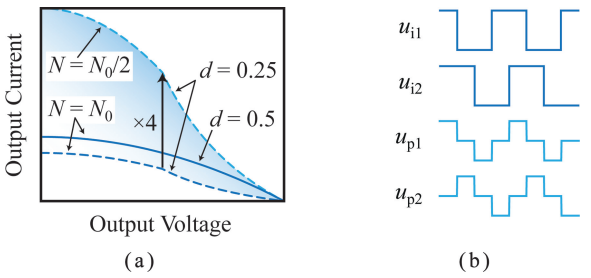


Fig. 6. (a) Reducing the duty cycle of the ISABC from 50% to 25% allows to reduce the number of turns by a factor of two, increasing the maximum output current. (b) Inverter voltages $\boldsymbol{u_{i1}}$, $\boldsymbol{u_{i2}}$ and winding voltages $\boldsymbol{u_{p1}}$, $\boldsymbol{u_{p2}}$ of the CISABC.

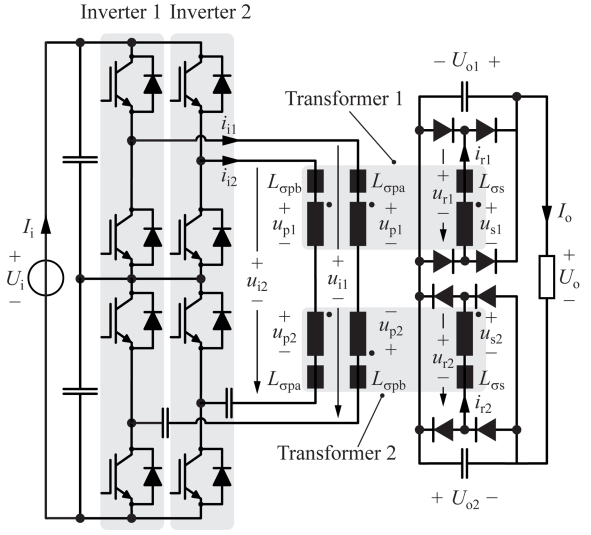


Fig. 7. Basic CISABC circuit in IPOS configuration with the two half bridges of each inverter distributed on two split DC-links.

$$\vec{i}_r = \frac{1}{n}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}\vec{i}_i, \tag{6}$$

and by inverting the matrix the inverter current vector

$$\vec{i}_i = \frac{n}{2}\begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}\vec{i}_r \tag{7}$$

follows. Considering the voltages at the leakage inductance elements, the inverter voltage vector equals

$$\vec{u}_i = \left(L_{\sigma pa} + L_{\sigma pb}\right)\frac{d\vec{i}_i}{dt} + \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}\vec{u}_p, \tag{8}$$

and at the secondary side, the rectifier voltage vector is expressed as

$$\vec{u}_r = \vec{u}_s - L_{\sigma s}\frac{d\vec{i}_r}{dt}. \tag{9}$$

With $\vec{u}_s = n\vec{u}_p$, combining (7), (8) and (9) the time derivative of the secondary side currents is obtained as

$$\frac{d\vec{i}_r}{dt} = \frac{1}{L_{\sigma s,tot}}\left(\vec{u}_{r0} - \vec{u}_r\right) \tag{10}$$

with the total leakage inductance referred to the secondary side

$$L_{\sigma s,\mathrm{tot}} = \frac{n^2}{2}\left(L_{\sigma \mathrm{pa}} + L_{\sigma \mathrm{pb}}\right) + L_{\sigma s}, \tag{11}$$

and the no-load rectifier voltage vector

$$\vec{u}_{\mathrm{r0}} = \frac{n}{2}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}\vec{u}_i. \tag{12}$$

In case of no-load ($\frac{\mathrm{d}\vec{i}_\mathrm{r}}{\mathrm{dt}} = 0$) the rectifier voltage vector equals the no-load rectifier voltage vector. From (10) it is evident that the rectifier currents result from the difference between the no-load rectifier voltages and the rectifier voltages. Of the three, possibly different leakage inductances $L_{\sigma pa}$, $L_{\sigma pd}$ and $L_{\sigma s}$ only their sum is effectively influencing the current. Therefore, different leakage inductances of the two primary windings because of asymmetric construction due to the coaxial primary winding arrangement still lead to equal current sharing between the inverters. However, the two transformers have to be identical and each inverter needs to connect in series to two different types (a, b) of primary windings, i.e. an outer and an inner one of the coaxial arrangement. The CISABC can, therefore, be modelled by replacing transformers and inverters by two controlled voltage sources with the values of the no-load rectifier voltages (12). Together with the total leakage inductance referred to the secondary side (11) this voltage sources can be imagined to be connected to the output rectifier as shown in Fig. 8. This simplified model allows to study the full steady-state and dynamic behaviour of the CISABC. The no-load rectifier voltage waveforms are shown in Fig. 9 for different values of inverter duty cycle. With maximum duty cycle ($d = 0.5$) the no-load rectifier voltage actually looks like a 25% duty cycle signal. If the inverter duty cycle is reduced to $d = 0.375$ a five-level stepped no-load voltage occurs. The voltage time product of this waveform however is still the same as with maximum inverter duty cycle. In case of $d = 0.25$ the highest level vanishes and a full block rectangular waveform at the half level remains, still having the same voltage time product as with maximum inverter duty cycle. If the duty cycle is further reduced, the zero level is entered four times per switching period, and a gap is inserted in the full block voltage, the voltage time product is now reduced. It is pointed out that the CISABC actually provides five voltage levels to the transformer, potentially allowing a low RMS current in the transformer at low output voltage levels. Simulated waveforms of the CISABC for 50%, i.e. maximum, duty cycle on both inverters with $U_o = 0.75\, nU_i$ are shown in Fig. 10. According to (12), with turns ratio $n = 1$ as in this simulation, the first no-load rectifier voltage u_{r01} equals half of the sum of the two inverter voltages (25% duty cycle no-load rectifier voltage waveform). With $n = 1$, the peak value of this waveform equals the peak value of the inverter voltages, the RMS value, however, is smaller by a factor $\sqrt{2}$. During the time when the no-load rectifier voltage of one transformer equals n times the inverter peak voltage, the rectifier current is building up. As soon as the no-load voltage returns to zero, the rectifier current drops too eventually reaching zero. On the secondary side this particular case is similar to the DCM of the ISABC. On the primary side,

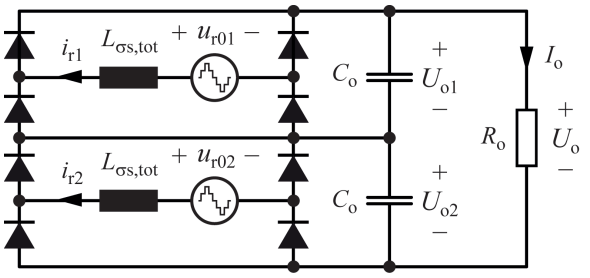


Fig. 8. Equivalent CISABC circuit employing two voltage sources representing the rectifier no-load voltages acting on the total leakage inductances referred to the secondary side.

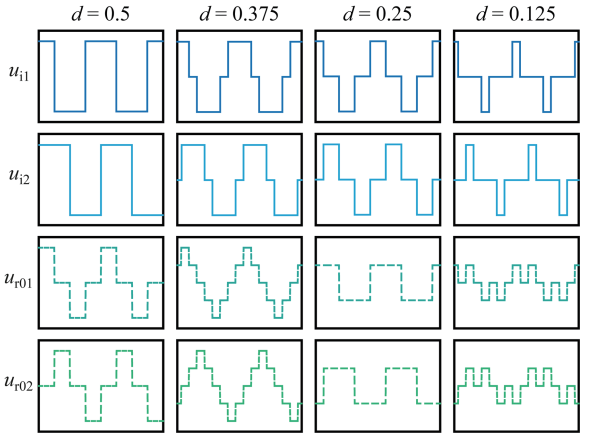


Fig. 9. Inverter voltages $\boldsymbol{u}_{\mathrm{i1}}$ and $\boldsymbol{u}_{\mathrm{i2}}$ and resulting no-load rectifier voltages $\boldsymbol{u}_{\mathrm{r01}}$ and $\boldsymbol{u}_{\mathrm{r02}}$ (dashed) for different values of inverter duty cycle $\boldsymbol{d}$.

according to (7), with $n = 1$ the first inverter current equals half the difference between the first and the second rectifier current and the second inverter current equals half the sum of the two rectifier currents. Since the rectifier currents show half-cycle symmetry all even harmonics are zero. Because the two rectifier currents are also identically shaped but 90° phase shifted all remaining (odd) harmonics are 90° phase shifted as well. Therefore, the rectifier currents are orthogonal which means that each harmonic amplitude of the sum (or difference) of the two rectifier currents equals the square root of the sum of the two corresponding rectifier harmonics squared. The RMS value of the first inverter current is, therefore, calculated as

$$\mathrm{rms}(i_\mathrm{i}) = \frac{n}{2}\mathrm{rms}(i_{\mathrm{r1}} - i_{\mathrm{r2}}) = \frac{n}{2}\sqrt{\mathrm{rms}(i_{\mathrm{r1}})^2 + \mathrm{rms}(i_{\mathrm{r2}})^2} \tag{13}$$

and since $rms(i_{r1}) = rms(i_{r2})$, the RMS value of the inverter currents is

$$rms(i_\mathrm{i}) = \frac{n}{\sqrt{2}} rms(i_\mathrm{r}). \tag{14}$$

Therefore, with the proposed transformer configuration and turns ratio $n = 1$, the RMS value of the inverter currents is by a factor $\sqrt{2}$ lower than the RMS value of the rectifier currents, while the peak value of the rectifier no-load voltage equals the peak value of the inverter voltage. Compared to the ISABC this property allows a significant reduction of the inverter conduc-

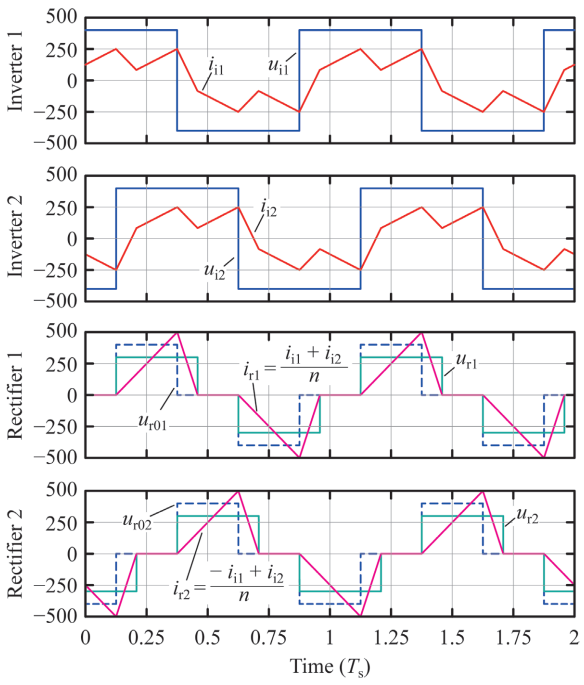


Fig. 10. Simulated primary- and secondary-side voltage and current waveforms of the CISABC according to Fig. 7 with turns ratio $n = 1$ (no-load rectifier voltage shown dashed), total leakage inductance referred to the secondary side $L_{\sigma s,tot} = 1$ µH, switching frequency $f_s = 50$ kHz, input voltage $U_i = 800$ V, output voltage $U_o = 600$ V and duty cycle $d = 0.5$.

tion loss. Furthermore, for the case shown in Fig. 10, the peak value of one rectifier current occurs when the other is zero, resulting in only half the current peak value being switched by the inverter.

2) Conduction Modes

Due to the five-level characteristic of the rectifier no-load voltage (Fig. 9) three different DCMs and also three CCMs have to be distinguished when aiming to describe the output current-duty cycle relationship. As shown in Fig. 11 it depends on the duty cycle and the relative output voltage which conduction mode occurs. Power transfer for output voltages higher than half the maximum output voltage is only possible in DCM and only if $d > 0.25$. For the working points A, B and C in Fig. 11, representing the three DCMs, the waveforms of no-load voltage, rectifier current and rectifier voltage of one rectifier are shown in Fig. 12. The working points D, E and F in Fig. 11 serve as example for the three CCMs with the according waveforms shown in Fig. 13. The analytic expressions for the output current as function of the duty cycle and the boundaries between the different conduction modes can be derived from Fig. 12 and Fig. 13 as shown in the Appendix.

3) Output Current Characteristic

The output current as function of the output voltage of the CISABC is plotted for different values of duty cycle in Fig. 14 together with the conduction mode boundaries. CCM1 only appears at very high output currents and low output voltages and is therefore not relevant for many applications because of thermal limitations. Therefore, because of the identical relation-

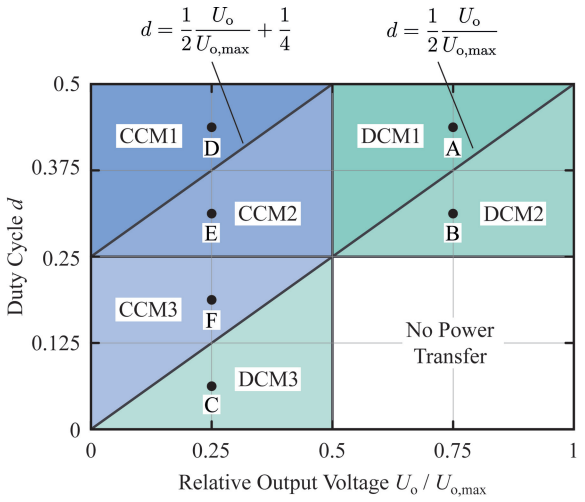


Fig. 11. CISABC conduction modes as function of duty cycle and output voltage relative to maximum output voltage.

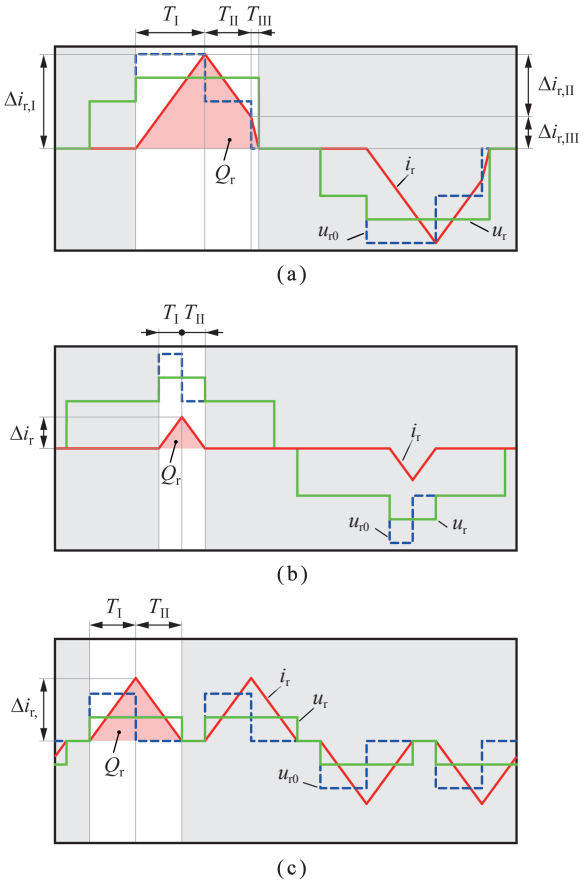


Fig. 12. Rectifier current, rectifier voltage and rectifier no-load voltage waveforms of the CISABC for DCM1 in working point A of Fig. 14(a), for DCM2 in working point B of Fig. 14(b) and for DCM3 in working point C of Fig. 14(c).

ship between duty cycle and output current of CCM2 (46) and CCM3 (54), it is practically sufficient to distinguish between four operating regions for hardware implementation.

The output current characteristic of the CISABC looks similar as the one of the ISABC. The output current decreases

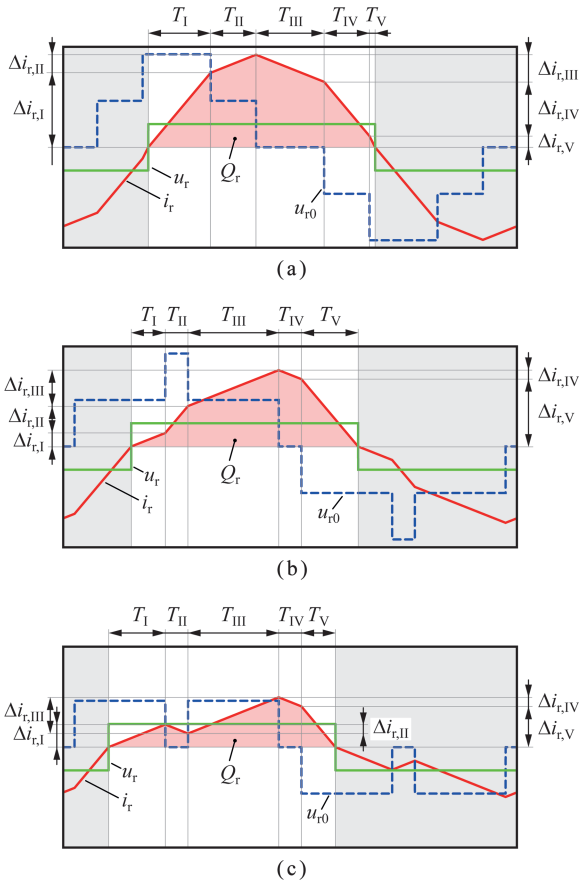


Fig. 13. Rectifier current, rectifier voltage and rectifier no-load voltage waveforms of the CISABC for CCM1 in working point D of Fig. 14(a), CCM2 in working point E of Fig. 14(b), CCM3 in working point F of Fig. 14(c).

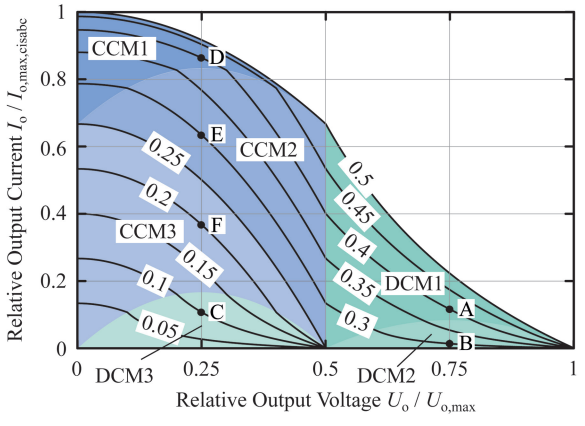


Fig. 14. CISABC output current as function of output voltage for different values of duty cycle with exemplary operating points used for analysing the different conduction modes in Section II-B2.

with increasing output voltage for a given duty cycle and with increasing duty cycle the output current is monotonously increasing. The shape of the characteristic at 50% duty cycle resembles the one of the ISABC at 25% duty cycle (cf. Fig. 4).

From (46) the maximum output current (at $U_o = 0$) of the CISABC can be expressed as

$$I_{o,max,cisabc} = \frac{3nU_i}{64 f_s L_{\sigma s,tot}}. \quad (15)$$

At first sight, this value seems to be smaller than the maximum output current of the ISABC (4). However, for the given application the transformers are designed for maximum power density, and are therefore operating at the maximum flux density allowed by the core material. Because of the 25% duty cycle shape of the rectifier no-load voltage, the maximum voltage time product at the primary winding of the CISABC is only half the one of the ISABC. Therefore, the number of turns necessary to reach the same flux density with the CISABC is only half that of the ISABC, resulting in a four times lower leakage inductance. Therefore, the maximum output current of the CISABC at zero output voltage is three times higher than the one of the ISABC.

4) Inverter RMS- and Peak-Current

Apart from the higher possible power transfer, the fact that the primary side RMS current value is only $\frac{n}{\sqrt{2}}$ times the secondary side RMS value (14) suggests that the primary side RMS currents of the CISABC are lower than the ones of the ISABC. The RMS inverter current to DC output current ratio of the CISABC is shown in Fig. 15. As can be seen the RMS inverter current to DC output current (IC2OC) ratio is less than one on a wide operating range. The plot also shows the output current limit of the CISABC compared to the output current limit of the ISABC, demonstrating that the achievable output current with the CISABC is higher than with the ISABC for all values of output voltage. A direct comparison of the inverter RMS and peak-currents of CISABC and ISABC is provided in Fig. 16. In Fig. 16(a) the inverter current RMS value of the CISABC is related to the one of the ISABC, showing that the inverter RMS current with the CISABC is smaller over the whole operating range covered by the ISABC. At high output voltages the inverter current RMS values are comparable but a significant reduction is achieved in particular at medium output voltage levels. Apart from the higher circuit complexity, the CISABC therefore provides lower RMS current stress on the inverter side. The inverter peak current of the CISABC related to the one of the ISABC is shown in Fig. 16(b). For output voltages less than 30% of the maximum value the inverter peak current is slightly lower with the ISABC, for higher output voltages the inverter peak current is lower with the CISABC. Fig. 16 also shows that the CISABC significantly extends the output current range compared to the ISABC.

5) Inverter Switched Current

Similar to the ISABC the CISABC inherently provides ZVS or at least ZCS in the full operating range. The condition for ZVS is that all rising edges of each inverter voltage u_i occur while the corresponding inverter current i_i is negative and that all falling edges of each inverter voltage u_i occur while the corresponding inverter current i_i is positive (voltage and current directions as in Fig. 2). The switched inverter current related to the DC output current reflected to the primary side is shown in Fig. 17. During the first (leading) falling edge of the inverter voltage (Fig. 17(a)) the switched current is positive in the full

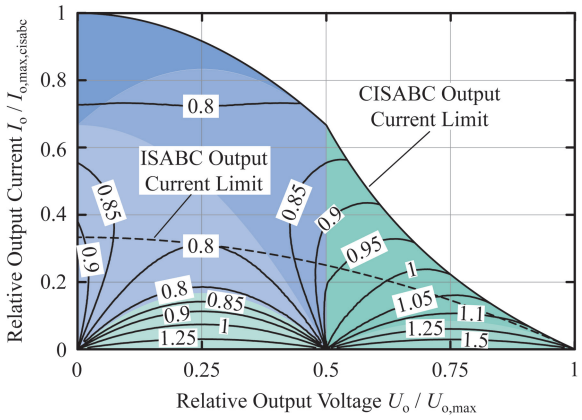
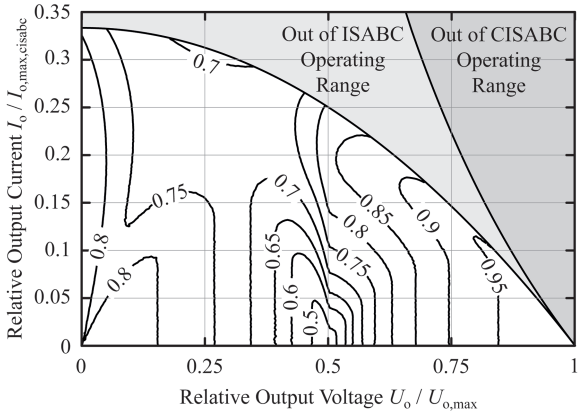
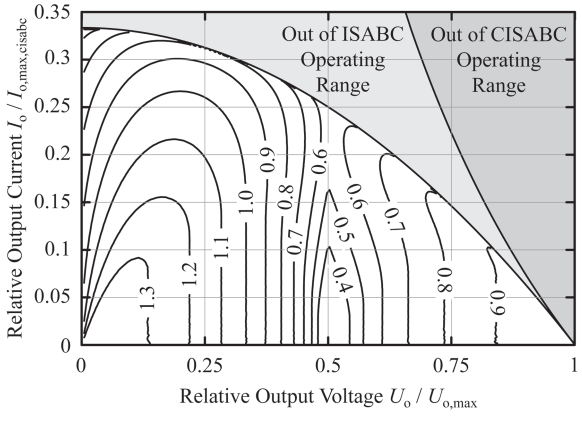


Fig. 15. RMS inverter current to DC output current ratio of the CISABC and output current limit compared to the output current limit of the ISABC.



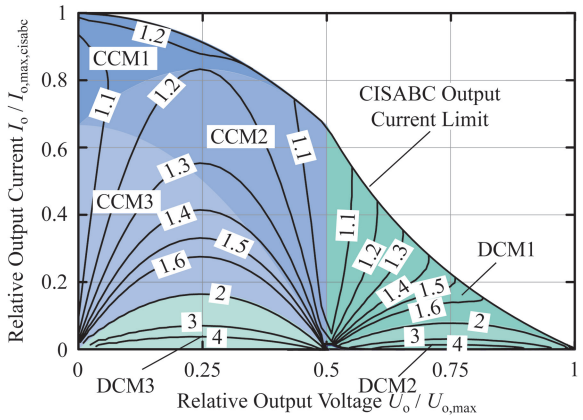
(a)



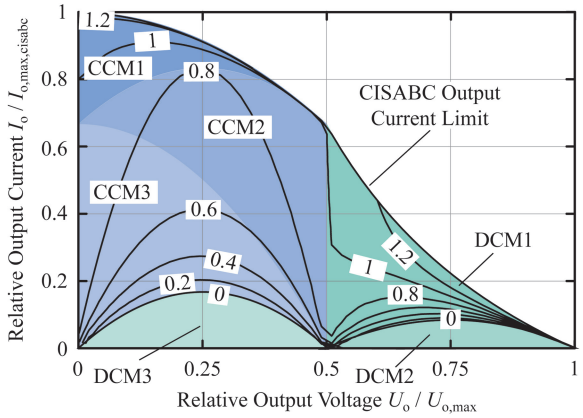
(b)

Fig. 16. Inverter current RMS value (a) and peak value (b) of the CISABC related to the respective values of the ISABC for the part of the operating range covered by both topologies.

operating range. Therefore, the leading half bridge achieves ZVS in the full operating range. During the second (lagging) falling inverter voltage edge (Fig. 17(b)) the switched current is only positive in all continuous conductions modes and in DCM1. In DCM2 and DCM3 the lagging half bridge switches zero current. With nowadays 600 V class insulated gate field



(a)



(b)

Fig. 17. CISABC switched current relative to the output current reflected to the primary side during first falling edge of the inverter voltage (a) and during second falling edge of the inverter voltage (b).

effect transistor (IGBT)s the turn-off losses are actually lower than the turn-on losses, i.e. a soft ZVS commutation is preferred over a hard one. However, the switching loss minimum is still achieved with ZCS which occurs at low output currents at the lagging half bridge.

6) Dimensioning the Leakage Inductance

Based on the maximum required output voltage $U_{o,nom}$ and the inverter input voltage the turns ratio n and the total leakage inductance $L_{\sigma s,tot}$ need to be selected. The choice of the turns ratio leaves some room for optimization, depending on the output voltage / output current requirements of the application. With a low turns ratio (e.g. $n = \frac{U_{o,nom}}{0.9U_i}$) the secondary current is reflected to the primary side with a low gain but at light load the current is discontinuous and thus the RMS current is high. With a high turns ratio (e.g. $n = \frac{U_{o,nom}}{0.6U_i}$) the current shape is continuous even at light load, but the secondary current is reflected with a high gain to the primary side. Usually a good choice is $n = \frac{U_{o,nom}}{0.75U_i}$ which is a compromise between light- and full load efficiency. After the turns ratio is set, the total stray inductance $L_{\sigma s,tot}$ is determined according to (20) with $d = 0.5$ such that the

required output current with some additional margin can be transferred.

III. Experimental Results

In order to demonstrate the functionality of the proposed CISABC circuit and control scheme without requiring high-voltage equipment the prototype uses transformers with a lower ($n = 9 : 6$) turns ratio. The transformer core is the same as will be used for the high voltage version including also the number of turns of the primary windings and the isolation distance between primary and secondary. A picture of the test set-up is shown in Fig. 18. Since only short (< 1 ms) pulses are required to demonstrate the functionality, the two inverters are supplied by a 23.5 mF, 400 V electrolytic capacitor bank. All inverter half-bridges are connected in parallel to this capacitor bank. The inverters are operated with 50 kHz using 650 V IGBTs [20]. The transformers use N87 ferrite cores, two six-turns 0.5 mm foil primary windings and one nine-turn 820 × 200 µm secondary winding that resembles the geometry of the 112 14-turn secondary windings that will be used on the high voltage version. The low winding capacitance of the equivalent transformer is justified, since the total winding capacitance of the high voltage transformer will be comparable, due to the partitioning of the winding into 112 parts each connected to a separate rectifier stage. The AC winding voltage is therefore only 670 V at 150 kV output voltage. The secondary windings of the equivalent transformers used in the low voltage test set-up are connected to two rectifier stages using 650 V Si diodes [21] which connect via two 7.6 µF DC-links to a load resistor, not shown in the picture.

A. Steady-State Operation

Measured waveforms of the inverter and rectifier side voltages and currents representing working point A of the nominal operating range (Fig. 20) are shown in Fig. 19. Note that the rectifier currents are obtained only mathematically using (6) from the measurements taken on the primary side. With the equivalent transformer used, the set voltage for this operating point of 853 V at 71 A represents an output voltage of 150 kV at 400 mA with the real system. This point of maximum voltage and maximum power (60 kW) is located in the region of DCM1, therefore the current on the rectifier side is discontinuous while the current on the inverter side is continuous. The measurement also shows the typical ringing of the rectifier capacitance with the transformer leakage inductance during the current zero state causing small oscillations also in the inverter currents. However, as expected ZVS is obtained at both inverters. The waveforms representing operating point B, i.e. 567 V output voltage and 106 A output current, are provided in Fig. 21. This operating point marks the lowest voltage, equivalent to 100 kV, at which the maximum power of 60 kW has to be transferred. The rectifier current waveform is still continuous and resembles the shape of CCM2. The inverter duty cycle in this measurement is $d = 0.35$ and with $U_{\mathrm{o,max}} = nU_{\mathrm{i}} = 1200\mathrm{V}$ the ratio $\frac{U_{\mathrm{o}}}{U_{\mathrm{o,max}}} = 0.47$, therefore this agrees with the conduction mode

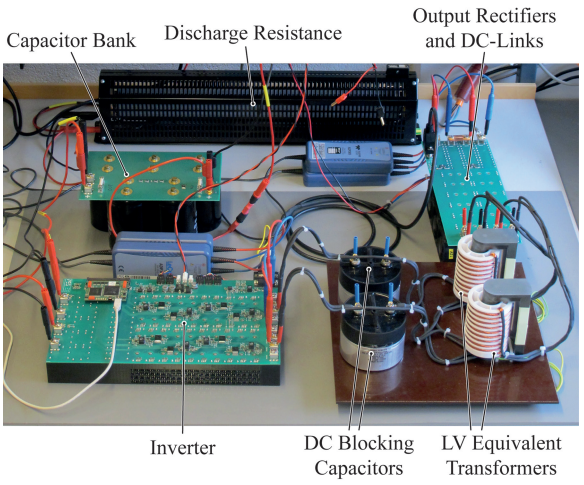


Fig. 18. Experimental set-up of the high voltage generator equipped with **n = 9 : 6** low voltage transformers using same cores and winding geometry as in the projected high voltage transformers.

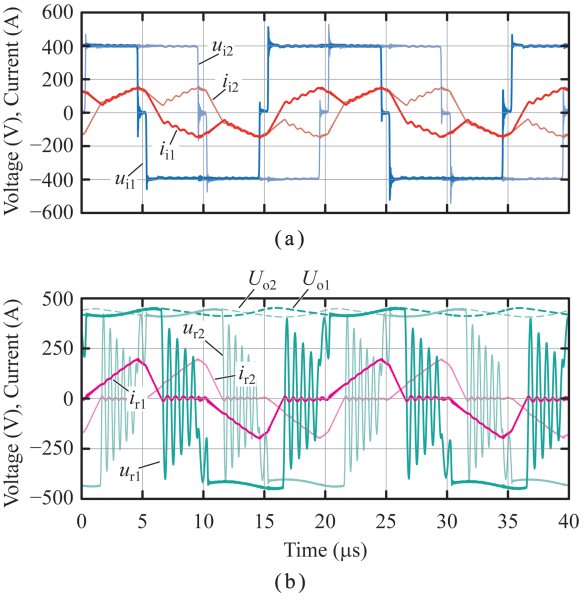


Fig. 19. Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point A of Fig. 20 with 853 V output voltage and 60 kW output power.

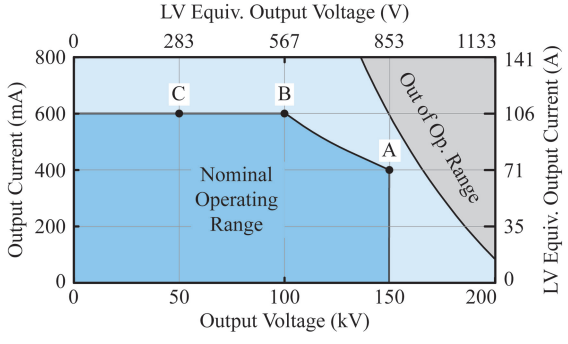


Fig. 20. Nominal operating range and experimentally tested working points shown with separate scales for voltage and current for the high voltage and the low voltage equivalent transformers.

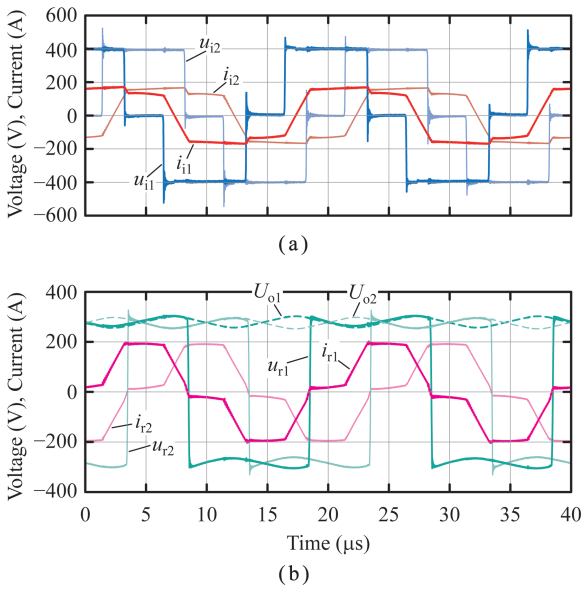


Fig. 21. Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point B of Fig. 20 with 567 V output voltage and 60 kW output power.

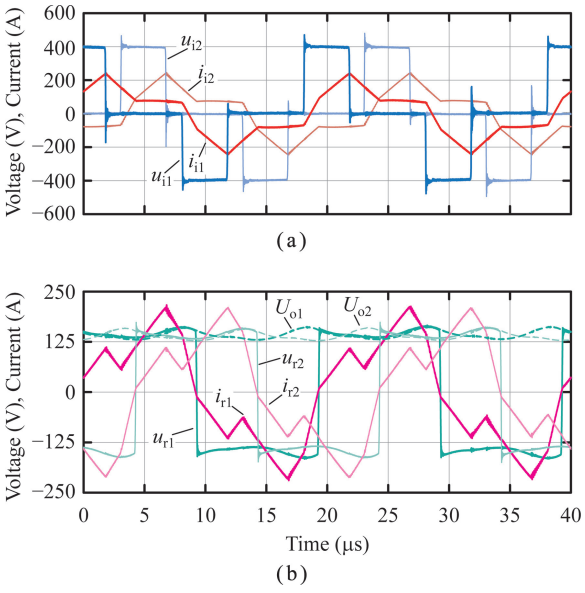


Fig. 22. Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point C of Fig. 20 with 283 V output voltage and 30 kW output power.

boundaries specified in Fig. 11. Also in this mode both inverters operate with ZVS. The waveforms representing operating point C, i.e. maximum specified output current at $\frac{1}{3}$ of the maximum output voltage are shown in Fig. 22. With the low voltage equivalent transformer the voltage set value is 283 V at 106 A output current, corresponding to 50 kV, 600 mA with the high voltage transformer. With a ratio of $\frac{U_o}{U_{o,max}} = 0.24$ and a duty cycle $d = 0.19$, according to Fig. 11 this operating point is located within the region of CCM3 as the shape of the rectifier current proves. The measurement also confirms ZVS for this operating point.

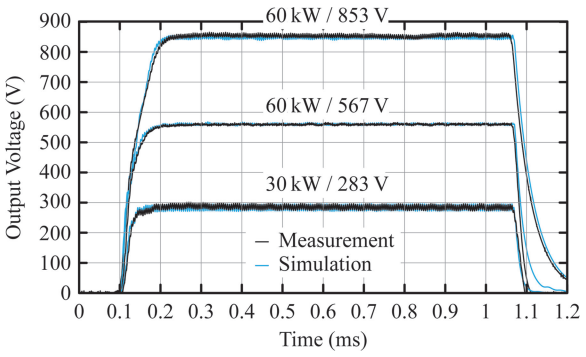


Fig. 23. Measured closed-loop controlled set value pulses for the low voltage equivalent operating points corresponding to Fig. 20 compared to circuit simulations.

B. Output Voltage Control

For the three operating points investigated in the previous section also set value step responses are measured. The results are shown in Fig. 23 and compared to the results obtained from a circuit simulation. As it is shown there is little deviation from the simulation, i.e. it is confirmed that all relevant parasitic elements are modelled. Note that the simulation applies exactly the same control algorithm as it is implemented in the FPGA, including models of the Delta-Sigma ADC (DS-ADC)s used for the output voltage measurements. Of the passive components only the leakage inductance $L_{\sigma s,tot} = 2.8$ µH, the output capacitance $C_o = 7.6$ µF and the load resistance R_o equalling 12 Ω in operating point A, 5.4 Ω in operating point B and 2.7 Ω in operating point C are modelled. Switches and diodes are modelled ideally. As can be seen the output voltage rise time for all operating points is less than 100 µs (5 switching cycles). The achievable rise time is lower for lower values of load resistance.

IV. Conclusion

A novel interleaved circuit variant of the ISABC, the CISABC, is proposed. The circuit connects two transformers, or at least one transformer with two magnetic paths, such that the no-load secondary voltages are obtained proportional to the sum respectively the difference of the two inverter voltages. The circuit exhibits three continuous and three discontinuous conduction modes which are analysed in detail with analytic expressions for the output current - duty cycle relationship and the boundaries between the conduction modes provided. The control strategy is demonstrated on a 60 kW, 50 kHz prototype, achieving 100 µs (five switching cycles) output voltage rise- and fall times.

The CISABC features several advantages over the ISABC and the SRC. Compared to the ISABC, the main advantage is the lower inverter RMS current. Depending on the operating point the inverter current of the CISABC can be as low as half the value obtained with the ISABC. Furthermore, the maximum possible output current which is limited by the leakage inductance is up to three times higher with the CISABC than with the SABC at the same core peak flux density. Compared to the SRC the CISABC mainly provides the advantage of ZVS (or at least ZCS) over the full operating range with constant switch-

ing frequency. Additionally, the non-resonant structure of the CISABC allows fast output voltage control. Finally, compared to non-interleaved circuits the low output voltage ripple of the CISABC allows a small output capacitance which is necessary to achieve short output voltage fall-times with passive rectifiers.

One main disadvantage of the proposed solution is that it requires two transformers, or at least a transformer with two flux paths. For the given application this is acceptable since using two transformers allows to reduce the 150 kV isolation requirement to only 75 kV between winding and core. Further, the CISABC exhibits slightly higher RMS currents on the rectifier side than the ISABC in sections of the operating range. However, since the losses in the rectifier diodes are mainly caused by the average current, which is the same as the one of the SABC, this is only a minor downside.

In summary the low inverter RMS currents and the ZVS or at least ZCS inverter commutation in the full operating range allow to keep the inverter losses low while constant switching frequency guarantees low control complexity. The interleaved operation allows to reduce the output capacitance, and double the duty cycle update rate, such that high output voltage control bandwidth is achieved. The proposed circuit and control structure is, therefore, a good choice for applications that allow only a passive secondary side (diode) rectifier but require fast output voltage rise- and fall times, as demonstrated on a prototype for a high-voltage X-ray supply.

Disclaimer

The concepts and information presented in this paper are based on research and are not commercially available.

Appendix

The derivation of the duty cycle-output current relationship for the different conduction modes and their boundaries are presented in the following.

A. Discontinuous Conduction Modes

1) Discontinuous Conduction Mode 1

For high values of duty cycle and high output voltage, as in working point A indicated in Fig. 14, the CISABC operates in DCM1. The characteristic waveforms of rectifier current, rectifier voltage and rectifier no-load voltage for this case are shown in Fig. 12(a). It is assumed, that the outputs are loaded symmetrically, therefore only the situation of one of the two rectifier sides is considered.

Furthermore, because of the half-cycle symmetry of the signals, only the positive rectifier current half-cycle is regarded. Assuming $0.5 > d > 0.25$ the rectifier no-load voltage varies between all five values. If it is also assumed that $nU_i > U_o > \frac{nU_i}{2}$, the rectifier current is only rising while the rectifier no-load voltage equals nU_i, its full-level. Hence, assuming the rectifier current is actually discontinuous, the rectifier current has to be zero when the rectifier no-load voltage value changes from half-level to full-level and this last rising edge of the rectifier no-load voltage marks the begin of the positive current half-cycle. Each current half-cycle is partitioned into three conduction intervals. During the first interval the rectifier current rises for

$$T_\mathrm{I} = \left(d - \frac{1}{4}\right) T_\mathrm{s} \text{ by } \Delta i_\mathrm{r,I} = \frac{nU_\mathrm{i} - U_\mathrm{o}}{2L_{\sigma\mathrm{s,tot}}} T_\mathrm{I} \tag{16}$$

with the switching period $T_s = 1/f_s$. As soon as the rectifier no-load voltage changes to the half its positive maximum level, interval II begins and the rectifier current changes for

$$T_\mathrm{II} = \left(\frac{1}{2} - d\right) T_\mathrm{s} \text{ by } \Delta i_\mathrm{r,II} = \frac{nU_\mathrm{i} - 2U_\mathrm{o}}{4L_{\sigma\mathrm{s,tot}}} T_\mathrm{II} \tag{17}$$

For DCM1 it is assumed, that the current does not reach zero during interval II. Therefore, after T_II has passed and the rectifier no-load voltage has changed to zero, the final conduction interval III is maintained until the current reaches zero. The total voltage time product applied to the leakage inductance between two current zero-crossings is zero, i.e. the voltage time product of rectifier voltage and rectifier no-load voltage during the three conduction intervals have to be equal, i.e.

$$nU_\mathrm{i} T_\mathrm{I} + \frac{nU_\mathrm{i}}{2} T_\mathrm{II} = U_\mathrm{o}(T_\mathrm{I} + T_\mathrm{II} + T_\mathrm{III}) \Rightarrow T_\mathrm{III}. \tag{18}$$

This expression yields the duration of the third conduction interval when the current decreases to zero for

$$T_\mathrm{III} = \left(\frac{nU_\mathrm{i}}{2U_\mathrm{o}} d - \frac{1}{4}\right) T_\mathrm{s} \text{ by } \Delta i_\mathrm{r,III} = -\frac{U_\mathrm{o}}{2L_{\sigma\mathrm{s,tot}}} T_\mathrm{III}. \tag{19}$$

Using expressions (16)-(19), the total charge Q_r transferred to the output during one half-cycle (Fig. 12(a)) is calculated which, multiplied by twice the switching frequency, finally leads to the average current transferred to the output in DCM1,

$$I_\mathrm{o,dcm1} = \frac{nU_\mathrm{i}}{2f_\mathrm{s} L_{\sigma\mathrm{s,tot}}} \left(\left(\frac{nU_\mathrm{i}}{4U_\mathrm{o}} - \frac{1}{2}\right) d^2 + \frac{d}{4} - \frac{1}{16}\right). \tag{20}$$

For the derivation of the output current in DCM1 it is assumed that the rectifier current does not reach zero during interval II. However, reducing the duty cycle in DCM1 also reduces the duration T_III, until interval III vanishes. With the assumed output voltage range, requiring that the rectifier current rises only when the full-level rectifier no-load voltage applies, and by requiring $T_\mathrm{III} > 0$, the conditions for DCM1,

$$\frac{U_\mathrm{o}}{2nU_\mathrm{i}} < d < \frac{1}{2} \text{ and } \frac{nU_\mathrm{i}}{2} < U_\mathrm{o} < nU_\mathrm{i}, \tag{21}$$

are obtained.

2) Discontinuous Conduction Mode 2

If the duty cycle at high output voltage ($U_\mathrm{o} > \frac{nU_\mathrm{i}}{2}$) is reduced below the minimum value for DCM1 the positive rectifier current half-cycle reaches zero already before the second no-load rectifier voltage falling edge. The rectifier side waveforms for this situation, DCM2, are shown in Fig. 12(b) for working point B of Fig. 14. As in DCM1, the positive rectifier current half-cycle begins with the last no-load rectifier voltage rising

edge. During the first conduction interval the rectifier current rises for

$$T_{\mathrm{I}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{22}$$

After the first rectifier no-load voltage falling edge the current decreases until it reaches zero. The duration of this second conduction interval is obtained by setting the voltage time products of rectifier no-load voltage and rectifier voltage during the two conduction intervals equal, i.e.

$$nU_{\mathrm{i}} T_{\mathrm{I}} + \frac{nU_{\mathrm{i}}}{2} T_{\mathrm{II}} = U_{\mathrm{o}}(T_{\mathrm{I}} + T_{\mathrm{II}}) \Rightarrow T_{\mathrm{II}}, \tag{23}$$

yielding the duration of conduction interval II,

$$T_{\mathrm{II}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2U_{\mathrm{o}} - nU_{\mathrm{i}}} \left(2d - \frac{1}{2}\right) T_{\mathrm{s}}. \tag{24}$$

With expressions (22) and (24) the average current transferred to the output in DCM2,

$$I_{\mathrm{o,dcm2}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}} \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2U_{\mathrm{o}} - nU_{\mathrm{i}}} \left(d - \frac{1}{4}\right)^2, \tag{25}$$

is obtained. Reducing the duty cycle to values less than $\frac{1}{4}$ while $U_{\mathrm{o}} > \frac{n}{2} U_{\mathrm{i}}$ results in a no-load rectifier voltage waveform not reaching the full-level (compare Fig. 9). Therefore, no interval is left with the rectifier current increasing and thus no power is transferred to the output. The conditions for DCM2 are consequently specified as

$$\frac{1}{4} < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} \text{ and } \frac{nU_{\mathrm{i}}}{2} < U_{\mathrm{o}} < nU_{\mathrm{i}} \tag{26}$$

3) Discontinuous Conduction Mode 3

With low values of both output voltage and duty cycle as in operating point C in Fig. 14, DCM3 occurs. The characteristic waveforms for operating point C are shown in Fig. 12(c). The rectifier no-load voltage consists of two pulses with same width and same polarity followed by two of opposite polarity. Since the durations of all pulses are the same and also the durations of all four zero intervals of the rectifier no-load voltage are equal; assuming that the current is discontinuous means that there are four symmetric rectifier current pulses separated by four current zero intervals. One such triangular current pulse is described by

$$T_{\mathrm{I}} = dT_{\mathrm{s}} \text{ and } \Delta i_{\mathrm{r}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{27}$$

Requiring equal voltage-time products of rectifier voltage and rectifier no-load voltage during the current pulse,

$$\frac{nU_{\mathrm{i}}}{2} T_{\mathrm{I}} = U_{\mathrm{o}}(T_{\mathrm{I}} + T_{\mathrm{II}}) \Rightarrow T_{\mathrm{II}}, \tag{28}$$

yields the duration of the current decrease during interval II,

$$T_{\mathrm{II}} = \left(\frac{nU_{\mathrm{i}}}{2U_{\mathrm{o}}} - 1\right) dT_{\mathrm{s}}. \tag{29}$$

Multiplying four times the charge transferred during one such pulse to the output with the switching frequency leads to the average current transferred to the output in DCM3,

$$I_{\mathrm{o,dcm3}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}} \left(\frac{nU_{\mathrm{i}}}{2U_{\mathrm{o}}} - 1\right) d^2. \tag{30}$$

Two conditions have to be fulfilled for DCM3 to occur. First, for the considered shape of the rectifier no-load voltage, the output voltage must be lower than half the input voltage reflected to the secondary side. Second, the duty cycle must be small enough such that the current is actually decreasing to zero during the rectifier no-load voltage zero interval, i.e. $T_{\mathrm{I}} + T_{\mathrm{II}} < \frac{T_{\mathrm{s}}}{4}$. Therefore, the conditions for DCM3 are

$$0 < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} \text{ and } 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{31}$$

B. Continuous Conduction Modes

1) Continuous Conduction Mode 1

A high duty cycle value together with low output voltage as in working point D indicated in Fig. 14 results in continuous current conduction, i.e. CCM. The waveforms of rectifier side voltages and current for this working point are shown in Fig. 13(a). The positive current half-cycle consists of two rising current intervals (T_{I}, T_{II}) followed by three falling current intervals (T_{III}, T_{IV}, T_{V}). While the durations of intervals T_{II}, T_{III}, T_{IV} are defined by the inverter duty cycle, the durations of the first and the last interval are determined by the current zero-crossings. The voltage time products of rectifier no-load voltage and rectifier voltage between two current zero-crossings have to be equal. Assuming that the rising edge current zero crossing is located between the last rectifier no-load voltage rising edge and the first rectifier no-load voltage falling edge this condition can be expressed as

$$nU_{\mathrm{i}} \left(T_{\mathrm{I}} - \left(d - \frac{1}{4}\right) \frac{T_{\mathrm{s}}}{2}\right) = U_{\mathrm{o}} \frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}, \tag{32}$$

yielding T_{I}. During interval I the full rectifier no-load voltage level is applied and the resulting rectifier current increase is described by

$$T_{\mathrm{I}} = \left(\frac{d - \frac{1}{4}}{2} + \frac{U_{\mathrm{o}}}{4nU_{\mathrm{i}}}\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{i,I}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{33}$$

The following interval durations are all directly derived from the inverter duty cycle (compare Fig. 9). For interval II only half of the maximum level of the rectifier no-load voltage applies, thus the rectifier current rises slower described by

$$T_{\mathrm{II}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,II}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \tag{34}$$

During the third interval the rectifier no-load voltage is zero

and the rectifier current is thus changing during

$$T_{\mathrm{III}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,III}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \quad (35)$$

During the fourth interval the rectifier current decreases faster with the rectifier no-load voltage now taking its half negative level.

$$T_{\mathrm{IV}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,IV}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{IV}} \quad (36)$$

Finally, during interval V the negative full-level of the rectifier no-load voltage drives the rectifier current back to zero for

$$T_{\mathrm{V}} = \left(\frac{d - \frac{1}{4}}{2} - \frac{U_{\mathrm{o}}}{4nU_{\mathrm{i}}}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}}. \quad (37)$$

Using (33)-(37) the charge transferred to the output during one current half-cycle is calculated. Multiplied with twice the switching frequency, the average current transferred to the output in CCM1,

$$I_{\mathrm{o,ccm1}} = \frac{nU_{\mathrm{i}}}{4f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}}\left(d - d^2 - \frac{1}{16} - \left(\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right)^2\right), \quad (38)$$

is obtained. By reducing the duty cycle in CCM1, according to (37), the duration of interval V is also reduced, until the current-zero crossings coincide with the last rising- and falling edges of the rectifier no-load voltage. For lower values of duty cycle, the assumption of the positive slope current zero-crossing being located between the last rising and first falling edge of the rectifier no-load voltage is no longer true. Setting $T_{\mathrm{V}} > 0$ yields the minimum duty cycle for CCM1, which reaches the maximum possible value of $d = 0.5$ at $U_{\mathrm{o}} = \frac{nU_i}{2}$. Therefore, also the maximum output voltage for CCM1 results from $T_{\mathrm{V}} > 0$ and the conditions for CCM1 can be summarized as

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} + \frac{1}{4} < d < \frac{1}{2} \text{ and } 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \quad (39)$$

2) Continuous Conduction Mode 2

Reducing the duty cycle to values lower than the minimum for CCM1 (39) results in rectifier voltage and current waveforms as shown in Fig. 13(b) simulated for working point E in Fig. 14. In this CCM2 the rectifier no-load voltage, same as in DCM1, utilizes all five levels, i.e. $d > 0.25$, but the positive slope current zero-crossing is located between the third and the fourth (last) rectifier no-load voltage rising edge. Each current half-cycle can be partitioned into five conduction intervals. The begin of the first interval, i.e. the time of the positive slope current zero-crossing, is located such that the voltage time product of the rectifier no-load voltage equals the voltage product of the rectifier voltage during the positive rectifier current half-cycle, i.e.

$$(T_{\mathrm{I}} + T_{\mathrm{II}})nU_{\mathrm{i}} = U_{\mathrm{o}}\frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}, \quad (40)$$

yields the duration T_{I} of the first interval. During that time the rectifier no-load voltage is at its half-level and the rectifier current is described by

$$T_{\mathrm{I}} = \left(\frac{1}{4} + \frac{U_{\mathrm{o}}}{2U_{\mathrm{i}}} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \quad (41)$$

The duration of the following intervals is determined solely by the edges of the rectifier no-load voltage, i.e. by the inverter duty cycle. During interval II, the rectifier no-load voltage full-level applies and the rectifier current rises during

$$T_{\mathrm{II}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,II}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \quad (42)$$

During interval III, the rectifier current continues to rise but the rectifier no-load voltage is back at its half-level. The interval is thus described by

$$T_{\mathrm{III}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,III}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \quad (43)$$

During interval IV the rectifier no-load voltage is zero and the rectifier current decreases for

$$T_{\mathrm{IV}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,IV}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{IV}}. \quad (44)$$

Finally, during interval V the negative half-level of the rectifier no-load voltage applies and the current decreases to zero,

$$T_{\mathrm{V}} = \left(\frac{1}{4} - \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}}. \quad (45)$$

Combining (41)-(45) allows to calculate the charge transferred to the output during one rectifier current half cycle, multiplied with twice the switching frequency yielding the average current transferred to the output in CCM2

$$I_{\mathrm{o,ccm2}} = \frac{nU_{\mathrm{i}}}{8f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}}\left(d - \left(\frac{U_{\mathrm{o}}}{nU_{\mathrm{i}}}\right)^2\right). \quad (46)$$

The region of CCM2 is limited by three conditions. First, (45) shows that with increasing output voltage the duration of interval V decreases until it reaches zero at $U_{\mathrm{o}} = \frac{n}{2}U_{\mathrm{i}}$. This limit marks the boundary to DCM1. Second, for the rectifier no-load voltage to utilize all five levels it is required (compare Fig. 9) that $d_{\mathrm{ccm2}} > \frac{1}{4}$. Finally, with increasing duty cycle the duration of interval I (41) approaches zero. Requiring $T_{\mathrm{I}} > 0$ places an upper bound on the duty cycle identical with the minimum duty cycle for CCM1 (39). The conditions for CCM2 are summarized as

$$\frac{1}{4} < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} + \frac{1}{4} \text{ and } 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \quad (47)$$

3) Continuous Conduction Mode 3

With duty cycle and output voltage as in working point F in Fig. 14 the CCM3 is entered. The corresponding waveforms of rectifier side current and voltages are shown in Fig. 13(c). The rectifier no-load voltage, as in DCM3, consists of two half-level

voltage pulses with same polarity followed by two pulses of opposite polarity. As in CCM1 and CCM2 five conduction intervals are identified for one rectifier current half-cycle. The first interval starts with the positive slope current zero-crossing, located between rising and falling edge of the first positive rectifier no-load voltage pulse, and ends with the falling edge of the first rectifier no-load voltage pulse. The duration of the first interval is determined by the condition of equal voltage time products of rectifier-no load voltage and rectifier voltage between two rectifier current zero-crossings, i.e.

$$T_{\mathrm{I}} n U_{\mathrm{i}} = U_{\mathrm{o}} \frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}. \tag{48}$$

During the first interval the positive half-level of the rectifier no-load voltage applies and the rectifier current changes during

$$T_{\mathrm{I}} = \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} T_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{49}$$

During the zero interval between the two positive pulses of the rectifier no-load voltage, interval II, the rectifier current decreases for

$$T_{\mathrm{II}} = \left(\frac{1}{4} - d\right) T_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,II}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \tag{50}$$

During the following interval III, the current rises at the same rate as in interval I for

$$T_{\mathrm{III}} = dT_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,III}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \tag{51}$$

The duration and the rectifier current change rate of interval IV are identical as in interval II, i.e.

$$T_{\mathrm{IV}} = T_{\mathrm{II}}, \ \Delta i_{\mathrm{r,IV}} = \Delta i_{\mathrm{r,II}}. \tag{52}$$

During interval V the rectifier current, while the negative half-level of the rectifier no-load voltage applies, decreases for

$$T_{\mathrm{V}} = \left(d - \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right) T_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}} \tag{53}$$

until it reaches zero. Using expressions (49)-(53) the charge transferred to the output during one positive current half-cycle is calculated and multiplied with twice the switching frequency to obtain the average current transferred to the output in CCM3

$$I_{\mathrm{o,ccm3}} = \frac{nU_{\mathrm{i}}}{8 f_s L_{\sigma\mathrm{s,tot}}} \left(d - \left(\frac{U_{\mathrm{o}}}{nU_{\mathrm{i}}}\right)^2\right). \tag{54}$$

Surprisingly, identical expressions for the output current in CCM2 (46) and CCM3 are obtained. Therefore, the boundary $d = 0.25$ between CCM2 and CCM3 could also be discarded. However, additionally a second condition limits the region of CCM3, since reducing the duty cycle also reduces the duration of interval V (53) until it vanishes completely. If the duty cycle is reduced further the current reaches zero before the first negative pulse of the rectifier no-load voltage begins and DCM3 is entered (compare Fig. 12(c)). Therefore setting $T_{\mathrm{V}} > 0$ yields the minimum duty cycle for operation in the region of CCM3, which coincides with the maximum duty cycle for operation in DCM3. Therefore, the conditions for CCM3 can be summarized as

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} < d < \frac{1}{4} \ \text{ and } \ 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{55}$$

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Attenuation of Conducted EMI for Three-Level Inverters Through PWM

Jianan Chen, Dong Jiang, and Qiao Li

Abstract—**This paper presents two typical modulations to reduce conducted electromagnetic interference (EMI) for three-level voltage-source inverters. The first modulation called variable switching frequency pulse-width modulation (VSFPWM) based on real-time current ripple prediction is used to reduce differential-mode (DM) EMI noise. This technique can make conducted EMI between kHz and MHz achieve great attenuation. The other method named zero common-mode (CM) PWM is used to decrease CM voltage and current. A comprehensive analysis and comparison between normal SVPWM and zero-CM PWM state that zero-CM PWM pays the prices of higher Total Harmowic Distortion (THD), serious neutral voltage unbalance, more switching loss and lower modulation index to achieve theoretical elimination of CM voltage. Then, combination of VSFPWM and zero-CM modulation is designed to avoid the disadvantages such as large switching loss produced by zero-CM PWM, and the new method has obvious predominance of reducing conducted EMI noise. Relevant experimental results validate the advantages of these modulations.**

Index Terms—**Conducted EMI, three-level inverters, variable switching frequency PWM, zero-CM PWM.**

I. Introduction

THREE-PHASE voltage-source-inverter (VSI) with pulse-width modulation (PWM) is one of the most widely used topologies for high power applications. With requirements for higher power and voltage rating as well as lower harmonics, multilevel VSI has its advantages over regular two-level VSI [1], [2]. Three-level neutral point clamped (NPC) inverter is a typical multilevel inverter and has been applied to high power applications in industrial fields, such as photovoltaic inverter power system, medium-voltage drive system, uninterrupted power system (UPS) and high voltage direct current transmission (HVDC) [3], [4].

PWM is the key technology for VSI regardless of application scenarios [5]-[7]. However, PWM can also bring three major by-products for the inverter. Firstly, the switching losses of power electronics devices will dramatically accumulate, accompanied by high switching frequency; secondly, the switching actions will generate current ripple for the inverter; finally yet importantly, PWM will generate electromagnetic interference (EMI) noise source, including differential-mode (DM) EMI and common-mode (CM) EMI. High-frequency harmonics in line-to-line, the typical representative for DM EMI, is capable of polluting power grid to make other electric equipment in an unsafe operating state and malfunction for microprocessors or automatic protective devices. Whereas, common-mode noise means the EMI noise conducted in the same direction together in the transmission line, which is usually representing as high frequency CM voltage. For motor drive applications, discharge current caused by CM voltage with high dv/dt will impair bearing and destroy the reliability of electrical machine. Therefore, the wide applications of PWM have put forward urgent requirements for EMI reduction [8]-[9].

With the requirement of EMI noise reduction, much research have been carried out in recent decades. The major approach of EMI mitigation in power electronics system is through two ways: the first is to block the EMI propagation path; the second is to mitigate the noise source. The first way is mainly through the design of EMI filter, which requires extra components to attenuate EMI before conducting into the objective [10]-[12]. Without applying extra filter, EMI can also be attenuated directly in the noise source: the switching pattern of power electronics inverters. For the noise source shaping, the high frequency EMI is mainly caused by the device switching pattern and is usually shaped through power electronics device and gate drivers [13], [14]. However, for the EMI spectrum between kHz and MHz range, the noise source is mainly determined by the pulse series. For this range, the shaping of EMI noise is mainly through converter topology and modulation schemes. For three-level inverter, the modulation freedom is more complicated than regular two-level inverter and is worthy with deep analysis, which is the major topic in this paper.

Many efforts have been made to develop novel PWM methods to reduce EMI noises. One typical approach is utilizing the freedom of switching frequency, which is variable switching frequency PWM (VSFPWM) [15]-[18]. Based on the current ripple prediction model for two-level VSI, switching frequency is controlled to meet the current ripple peak value requirement. Compared with regular constant switching frequency PWM (CSFPWM), VSFPWM can reduce switching losses and EMI noise peak and keep the same current ripple peak value. For three-level VSI, [19] has studied the current ripple through space vector analysis. Nevertheless, it is much complicated and VSFPWM has not been implemented for three-level inverters.

CM noise source is CM voltage, so the way to reducing CM noise is to re-shape output voltage pulses. However, PWM in widely used two-level inverter is only with capability to reduce the CM voltage amplitude but not eliminate CM voltage theo-

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retically since the phase voltage is either positive or negative in two-level inverter and 'three' is an odd number. Three-level inverter is able to reduce or even eliminate CM voltage theoretically since the phase voltage is with positive, negative or zero. [20]-[21] have studied the advanced modulation for CM voltage elimination, but the method is at the price of lower utilization of DC voltage and bigger switching losses. [22]-[23] have done research on the way to reduce CM voltage, whose effect on CM mitigation is not so good as zero-CM whereas the modulation index can still reach to 1.15 and even have lower switching losses in respect to normal SVPWM. Reference [24] has in-depth compared the EMI performance between two above-mentioned methods and normal space vector pulse-width modulation (SVPWM), which provides some useful information to roundly understand CM conducted EMI. Nevertheless, little subject matter literature introduce ideas to improve these methods.

Modeling and analysis of VSFPWM for two-level inverters with modulation have been done well. However, the study for three-level inverter is not sufficient since the modulation freedom is more and complicated to utilize. Based on the previous work of EMI reduction through modulation, this paper will introduce a general current ripple prediction method for three-level VSI with carrier-based PWM approach, and implement it into VSFPWM for three-level inverters in part II. The zero-CM modulation has been proposed for many year, whereas little literatures thoroughly research the equivalent relationship between space vector modulation and carrier based modulation of zero-CM PWM, which are presented in part III together with comprehensive comparison between normal SVPWM and zero-CM PWM. In addition, the combination of VSFPWM and zero-CM designed together to help improve the performance of zero-CM methods are introduced in part IV. Conclusions are summarized in part V.

II. Differential-Mode Conducted EMI Reduction

For the modulation based optimization of DM EMI noise, the major approach is making the switching frequency vary, which can re-distribute the EMI noise from concentrating near the harmonics of constant switching frequency to a wide range in frequency domain. Then the EMI noise peak can be reduced. Previous study of so called "random PWM" that changes the switching frequency randomly is highly depending on the statistic effect, and cannot control the current ripple and power losses [25], [26]. Based on the model predictive VSFPWM in two-level VSI [17], [18], this part will introduce the current ripple prediction model and model predictive VSFPWM for three-level inverter to reduce conducted EMI.

A. Current Ripple Prediction Model

Fig. 1 shows the topology of three-level NPC inverter. The three terminals (*A*, *B*, and *C*) are switching with voltage of $V_{dc}/2$, 0, and $-V_{dc}/2$ referring to the DC neutral point O_1. The load is representing general AC load, including inductors and balanced three-phase voltage sources. The AC voltage source can represent motor back-EMF for motor drive application

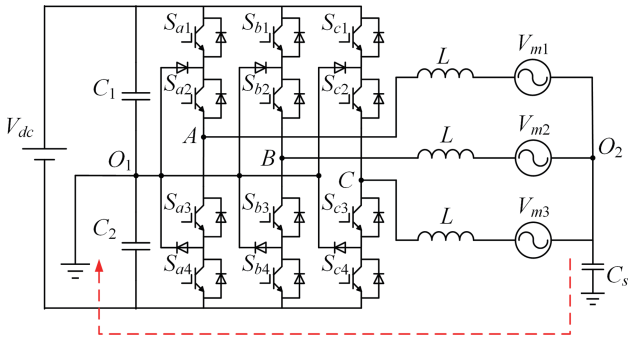

Fig. 1. Topology of three-level NPC inverter.

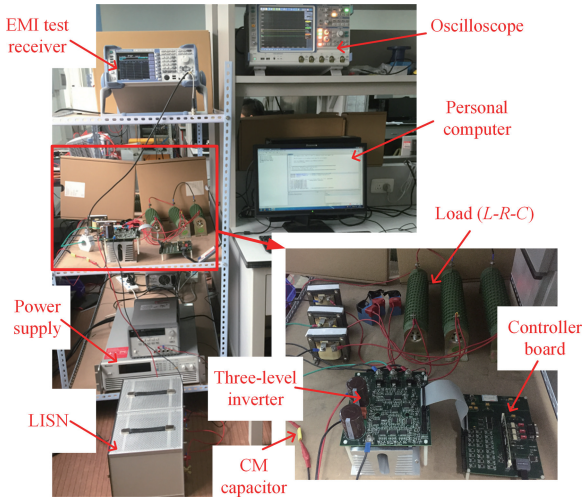

Fig. 2. Experimental platform.

or grid voltage for grid application. The voltage produced by inverter is rectangular pulse series whereas the terminal voltage of load is sinusoidal waveform, so their voltage difference imposed on inductance will result in affluent high frequency current ripple. According to three-level schematic diagram in Fig. 1, experimental platform is set up as shown in Fig. 2. The 10 Ω resistor in parallel with 35 μF capacitor is capable of representing three-phase balanced voltage [15]. Inductors with 0.5 mH connect inverter and three-phase voltage source to sustain the voltage difference.

Fig. 3 shows the phase currents and their 50 Hz fundamental component achieved by FFT analysis, which are the experimental results of the modulation with constant switching frequency called normal SVPWM. The experimental condition are with 270 V DC bus voltage, 20 kHz switching frequency, and modulation index of 0.85. These experiment parameters and condition mentioned above summarized in TABLE I will be applied to all experiments in this paper.

Obvious ripple can be found in the phase current, which is caused by switching events and is synchronous with PWM signals. Fig. 4 shows the three-phase output voltage together with phase-A current ripple during one switching cycle. The current ripple is following the switching actions of the three-phase rectangular pulse voltage. In addition, the variation of current ripple between each two adjacent switching actions is linear,

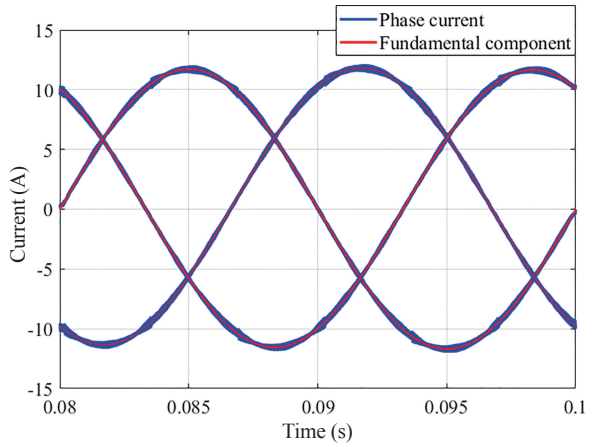

Fig. 3. Phase current and fundamental value of SVPWM (experimental result).

TABLE I
EXPERIMENTAL PARAMETERS AND CONDITION

Symbol	Parameters	Value
V_{dc}	DC voltage	270 V
C_1/C_2	DC side capacitance	470 μF
m	modulation index	0.85-1.00
f_s	constant switching frequency	20 kHz
f_0	fundamental frequency	50 Hz
L	filtering inductance	0.5 mH
R	load resistance	10 Ω
C	load capacitance	35 μF
C_s	parasitic capacitance for CM loop	10 nF
P	power	2.0 kW-2.8 kW

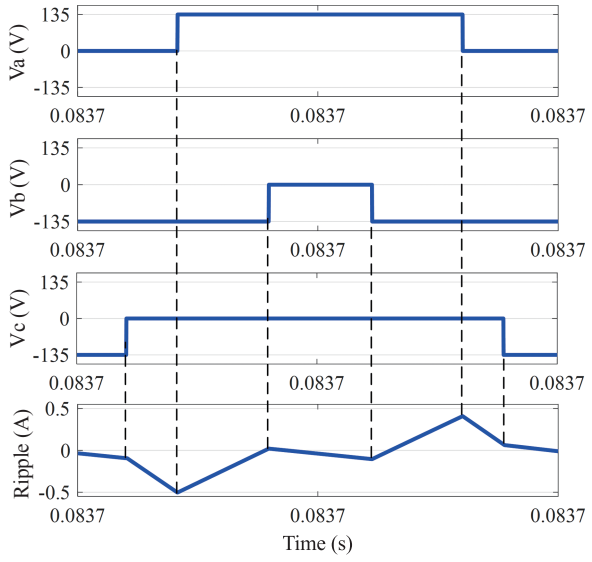

Fig. 4. Output voltage and current ripple during one switching cycle (simulation results).

which is the basic precondition for current ripple prediction. Nevertheless, three-level inverter's output voltage is switching between V_{dc} /2 and 0, or 0 and -V_{dc} /2, not between V_{dc} /2 and -V_{dc} /2, which is different from the current ripple generation in

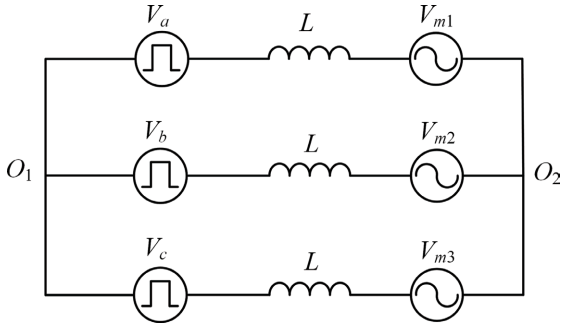

Fig. 5. Equivalent circuit for ripple prediction.

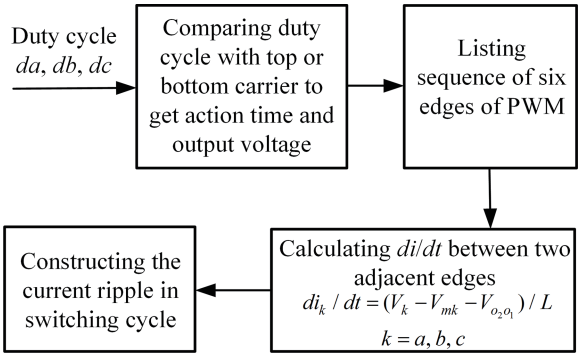

Fig. 6. Current ripple prediction diagram.

two-level VSI in [15]-[18]. Then, the switching voltage model should be re-constructed to predict current ripple.

SVPWM, a rather complicated modulation for multilevel converters, is still considered as the most useful technique for power electronics converters. Owing to equivalent theory [27], carrier-based PWM could replace SVPWM to simplify the modulation and obtain the same performance for multilevel converters. Therefore, this paper implement the modulation SVPWM with carrier-based PWM equivalently, rather than the complicated process of the vector synthesis with 27 space vectors for three-level inverters.

For the carrier-based PWM analysis of three-level inverters, there are two carriers in the modulator to compare with the reference value. Top carrier is used to generate output voltage of V_{dc} /2 and 0, the bottom carrier is for 0 and -V_{dc} /2. Then, the output voltage and action time in each switching cycle can be determined. With the output voltage model, the current ripple can be derived through the equivalent circuit in Fig. 5 [17], which is the equivalent model of Fig. 1. In each switching cycle, the pulse voltage sources (V_a, V_b, V_c) are determined by comparison between the duty cycles and carrier, the balanced three-phase load average voltage (V_{m1}, V_{m2}, V_{m3} are supposed to be constant value in a switching cycle) are directly determined by duty cycles. With the output voltage and action time, the current ripple can be predicted [28].

The current ripple prediction diagram is shown in Fig. 6. The duty cycles from the controller are the input. In each switching cycle, by comparing the duty cycles with the top and bottom carrier in the three-level inverter modulator, the action time for three phases will be determined as well as the terminal voltage.

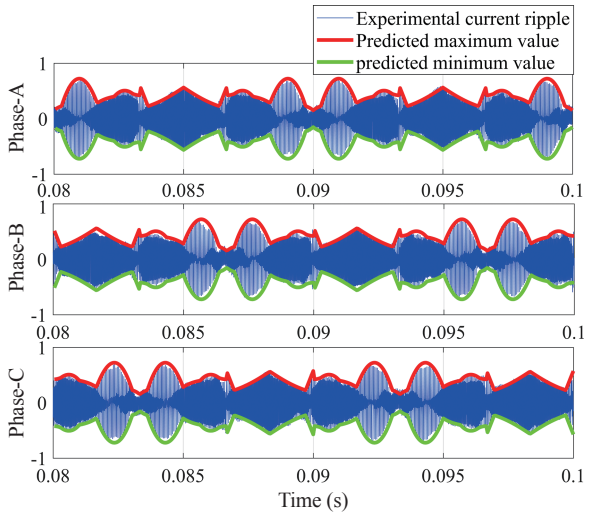

Fig. 7. Current ripple comparison between experiment and prediction (Normal SVPWM).

Then, by listing the six edges (three rising edges and three falling edges) in the switching cycle, the action time and output voltage between each two adjacent edges can be determined. With the equivalent model in Fig. 5, the di/dt between each two adjacent edges can also be calculated. With the di/dt and action time Δt between each two adjacent edges, the current ripple in the full switching cycle can be predicted.

Fig. 7 shows the comparison of current ripple between experiment and prediction for all three phases. The predicted current of maximum and minimum value in each switching cycle are matching well with the experimental current ripple. The experimental results indicate that the prediction model is effective and possesses real-time prediction capability.

B. Variable Switching Frequency PWM

The variable switching frequency PWM (VSFPWM) for three-level inverter is similar with the structure of VSFPWM for two-level VSC in [18]. The VSFPWM diagram is shown in Fig. 8. Duty cycle references (*da*, *db*, *dc*) are generated from controller. They are sent to the ripple prediction module, the predicted current ripple is calculated and sent to the switching period generation block. The generated triangle carriers with variable frequency (top and bottom) are used to compare with duty cycles and generate the gate drive signals for the power devices in the three-level VSI. At the same time, the variable switching frequency sampler is generated to the controller for control.

The core for the VSFPWM algorithm is the switching period calculation module. With the real-time prediction of current ripple in each switching cycle, the maximum ripple current in three phases with nominal switching cycle T_{sN} is calculated. The updated switching cycle T_s is calculated in (1). The updated switching period will control the maximum current ripple to be equal to the ripple requirement in each switching cycle.

$$T_s = T_{sN} \times \frac{I_{ripple\_require}}{I_{ripple\_\max}} \tag{1}$$

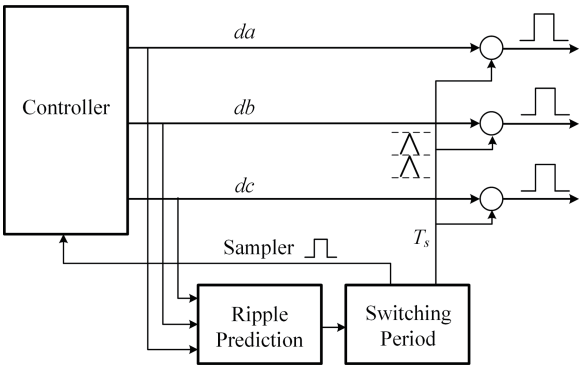

Fig. 8. Structure of VSFPWM generation.

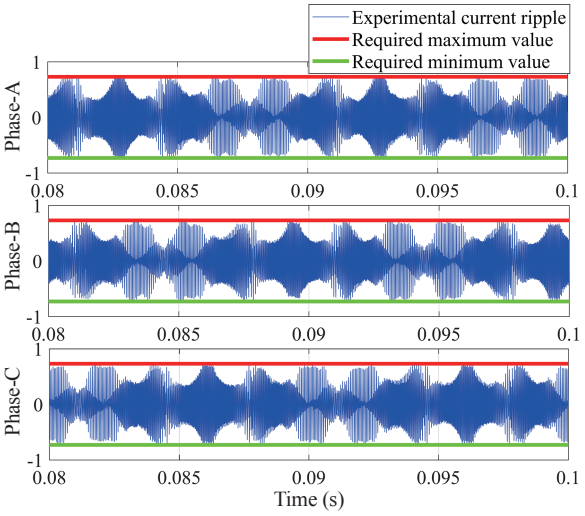

Fig. 9. Three-phase current ripple of VSFPWM (experimental result).

Compared with the model predictive VSFPWM in two-level inverter discussed in [15]-[18], the basic principle of VSFPWM in three-level inverter is similar: actively adjusting the switching frequency in each cycle to control the maximum current ripple clamped to the required value. The major difference for three-level inverter is double carrier, which makes prediction model more complicated than two-level. Because the variation range of current ripple in three-level inverter is big, there is a big range for switching frequency variation.

C. Experimental Results for Three-Level VSFPWM

In order to verify the variable switching frequency methods proposed in previous parts, the experiments have been implemented in a three-phase PWM three-level NPC inverter connected to the *L*-*R*-*C* load shown in Fig. 2. Three-phase currents are measured by high precision current probes and recorded as data. With FFT analysis of the current data, fundamental current and plenty of harmonics components can be re-constructed. By subtracting the fundamental component from three-phase full current, current ripple of VSFPWM is obtained in Fig. 9. Compared with ripple in Fig. 7 for normal SVPWM, the VSFPWM has better effective utilization rate of space limited by the identical required current peak value (± 0.73 A) apparently.

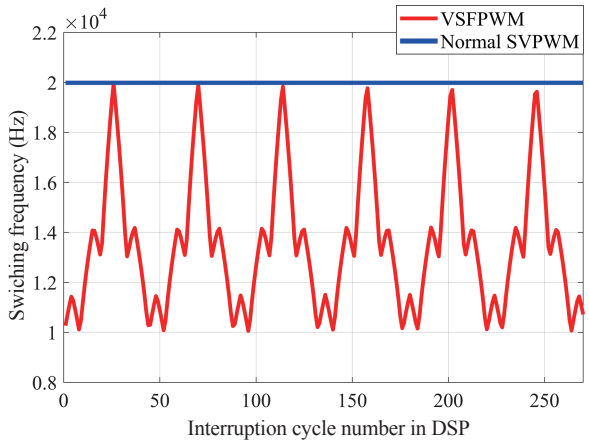

Fig. 10. Switching frequency variation of VSFPWM (experimental result).

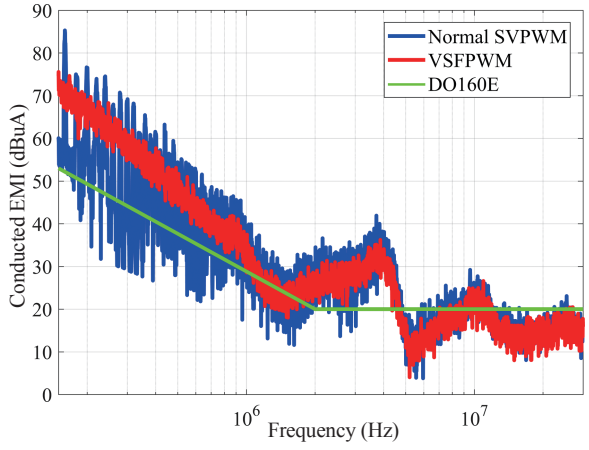

Fig. 11. Comparison of conducted EMI: VSFPWM and normal SVPWM (experimental result).

According to (1), the maximum current ripple of three-phase in carrier period and the required limitation of ripple determine the variation range of frequency. In Fig. 7, it is clear that the maximum ripple is not always clamped to required value (0.73A) when normal SVPWM is applied. Nevertheless, the VSFPWM methods can make the maximum ripple equal to required value in every switching cycle as shown in Fig. 9. Fig. 10 shows the switching frequency of VSFPWM, which is acquired from the register of DSP. Its switching frequency varies in a wide range from 10 kHz to 20 kHz other than being fixed at a constant switching frequency (20 kHz), leading to a large reduction in switching loss. The reason for reducing switching loss is that the average switching frequency related to switching loss and efficiency has reduced significantly with respect to the normal SVPWM (20 kHz).

DM conducted EMI of two cases are compared in Fig. 11 with frequency range from 150 kHz to 30 MHz measured by EMI test receiver, which adheres to the narrowband standard DO-160E. EMI noise energy spread into a broad range, which makes the peak value obviously smaller than normal SVPWM. The EMI peak value could nearly reduce 10 dB around the carrier harmonics. The limit of EMC standard is also plot in Fig. 11

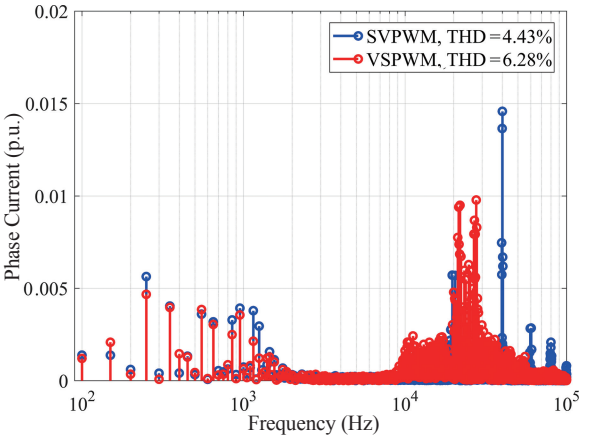

Fig. 12. Comparison of phase current spectrum: VSFPWM and normal SVPWM (experimental result).

where the green line is. Although the advanced modulation can make conducted EMI achieve great attenuation, the EMI filter is also need to satisfy the EMI requirement. However, reduction of EMI noise can increase cut-off frequency and decrease migration requirement for EMI filter, which could reduce the volume and weight of the passive components, finally increase the power density of whole system.

The variable frequency methods will have impact on the low frequency harmonics and the THD of the output currents. The THD increases from 4.43% to 6.28% after applying variable switching frequency method into normal SVPWM. The reason for the increase of THD is obvious that the switching frequency is keeping smaller than 20 kHz and resulting the current ripple bigger. Fig. 12 shows the current spectrum comparison between VSFPWM and normal SVPWM. Compared with normal SVPWM, VSFPWM not only spreads the spectrum around carrier harmonics, but also has little impact on low frequency harmonics.

III. Common-Mode Voltage Reduction

A. Review of Zero Common-Mode Modulation

The common-mode voltage elimination technology, is the predominance of multilevel converters, has been proposed for many years [20]. Common-mode voltage of three-phase converter can be calculated as (2).

$$V_{CM} = \frac{V_{AO_1} + V_{BO_1} + V_{CO_1}}{3} \tag{2}$$

There are 27 switching sequences for three-level inverters shown in Fig. 13. According to (2), different space vectors produces different common-mode voltage between AC neutral point and DC side. However, among the 27 space vectors, only the six medium vectors and one zero vector (ooo) is able to realize zero CM voltage output to decrease CM current that is the typical representative of CM conducted EMI. Fig. 1 shows CM loop and CM current i_{cm} in red dotted line, the CM current flows through stray capacitors and ground. The basic method

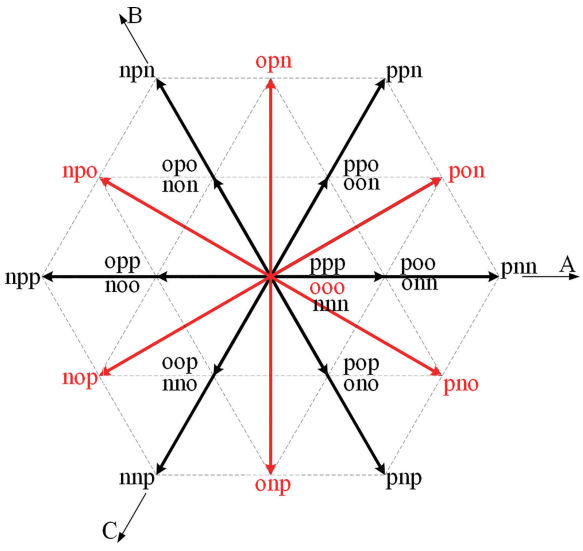

Fig. 13. Space vector map for three-level topology.

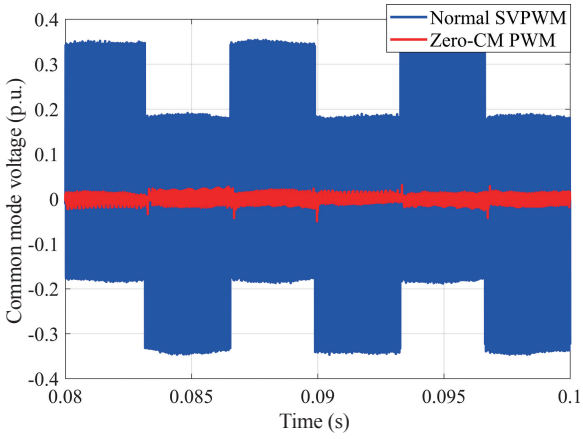

Fig. 14. CM voltage comparison between zero-CM PWM and normal SVPWM (experimental result).

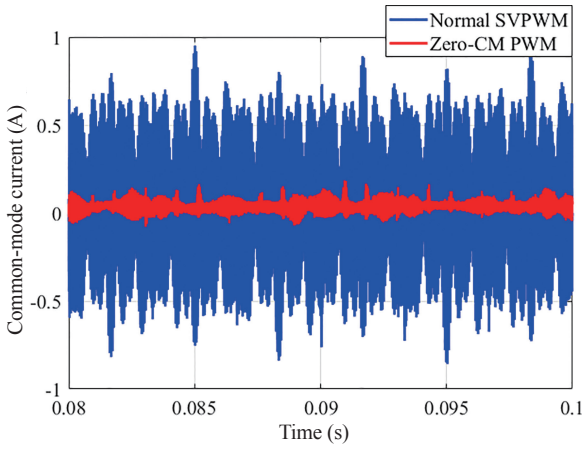

Fig. 15. CM current comparison between zero-CM PWM and normal SVPWM (experimental result).

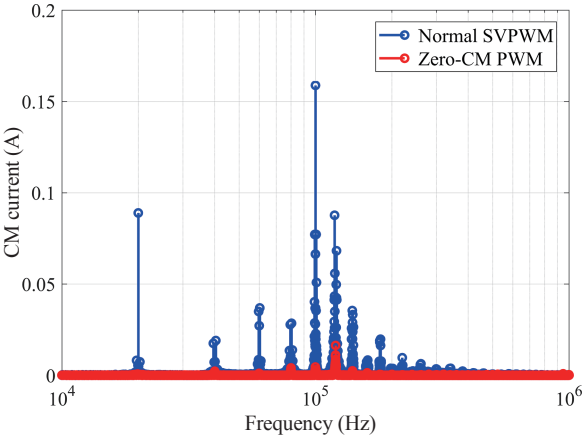

Fig. 16. Comparison of common-mode current spectrum: zero-CM PWM and normal SVPWM (experimental result).

for three-level to eliminate CM voltage is utilizing the seven vectors (the red vector in Fig. 13) to combine the rotary vector. It is obvious that this vector space with six effective vectors is similar to two-level, so its procedure of synthesizing reference vector can imitate the SVPWM of two-level converters.

Fig. 14 shows the experimental results of zero-CM modulation in comparison with normal SVPWM for three-level inverters concerning CM voltage. It can be observed that the zero-CM modulation could decrease common-mode voltage greatly compared with conventional SVPWM. The CM voltage nearly reduces to zero with common-mode elimination algorithm; consequently, weakening the source of CM conducted EMI.

The DC bus neutral point is connected to AC neutral point by capacitance with 10nF, which is designed to simulate stray capacitor of CM loop and conduct CM current. Fig. 15 is the CM current waveform comparison of the two modulations. CM current peak value of SVPWM nearly reach 800 mA, but the zero-CM PWM only with 150 mA. It is worth mentioning that non-ideal factors such as dead time and switching transient greatly affect the performance of CM elimination [21].

Fig. 16 is the CM current spectrum of two methods between 10 kHz and 1 MHz. As expected, the main harmonic component have decreased largely. For example, the biggest harmonic with 100 kHz can fall from 0.16 A to 0.005 A. Fig. 17 exhibits experimental frequency spectrum of CM current EMI. It is apparent that CM current EMI peak value can attenuate 15 dB during wide range of frequency spectrum (150 kHz-1 MHz), some points such as 180 kHz even more than 20dB. The experimental results indicate that zero-CM modulation succeeds in restraining CM voltage and current.

B. Analysis of Zero Common-Mode Modulation

Three-level inverter may effectively suppress CM noise whereas several problems still exist in zero-CM modulation. Firstly, THD increases under the circumstance of zero-CM modulation. Fig. 18 and Fig. 19 show the phase current waveforms and spectrums comparison respectively: blue waveform is the phase current and corresponding spectrum of conventional SVPWM with THD of 4.43%; the red one is zero-CM PWM

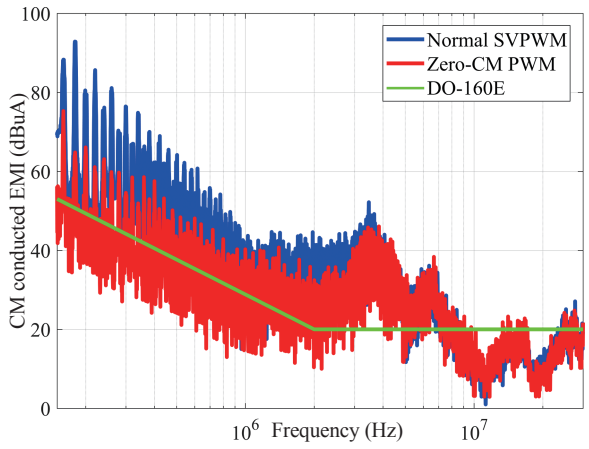

Fig. 17. CM Conducted EMI comparison between zero-CM PWM and SVPWM (experimental result).

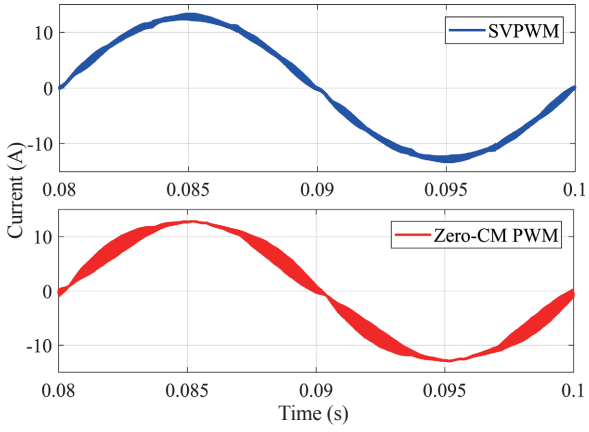

Fig. 18. Phase current comparison between normal SVPWM and zero-CM PWM.

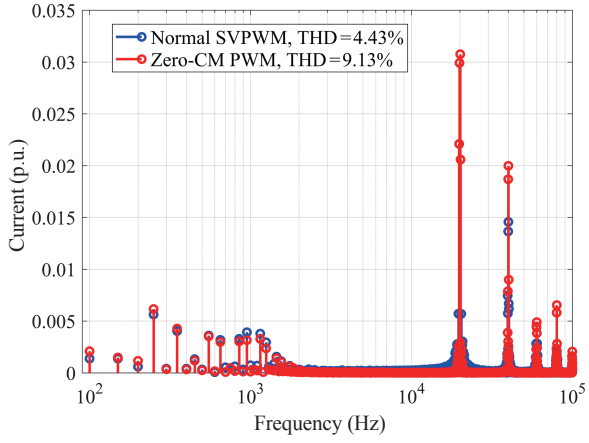

Fig. 19. Comparison of phase current spectrum: zero-CM PWM and normal SVPWM (experimental result).

with THD of 9.13%. Zero-CM modulation largely increases current ripple, whereas the current quality is acceptable with the experimental condition. Fig. 20(a) reveals the reference vector combination of normal SVPWM, and Fig. 20(b) depicts the process of vectors synthesis for zero-CM modulation, which

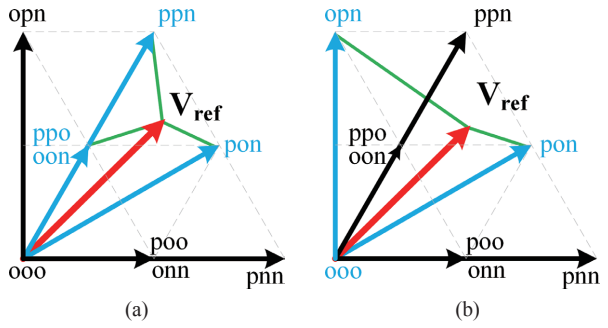

Fig. 20. Output voltage vectors combination comparison. (a) Normal SVPWM. (b) Zero-CM PWM.

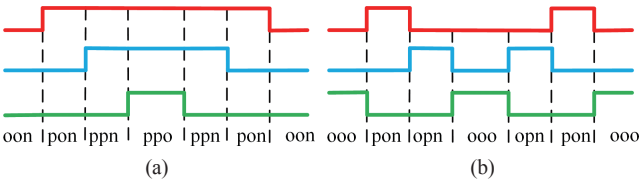

Fig. 21. Switching sequence combination comparison. (a) Normal SVPWM. (b) Zero-CM PWM.

chooses farther vector (opn) rather than the nearest one (oon or ppo) to synthesis the reference voltage vector. The reason for choosing farther vector in Fig. 20(b) is to eliminate CM voltage, but it will increase the voltage difference from the reference voltage and generate bigger current ripple. Then, the novel modulation loses the advantage of three-level such as lower harmonics for abandoning using the affluent vectors.

Secondly, switching loss is twice of the conventional SVPWM. For instance, Fig. 21 shows the switching sequence of reference vector in Fig. 20. There are four switching events during one switching period, which is twice of traditional SVPWM. Therefore, the switching loss of zero-CM PWM has doubled.

What's more, utilization of DC voltage is reduced to 0.866 while normal SVPWM is 1. The reason is that the combination does not select large vector and the length of reference vector bigger than 0.866 of DC voltage fails to combine.

Another important issue for three-level NPC inverter is neutral point voltage balancing. Large voltage vectors and zero vectors will not influence neutral point voltage since no phase is connected to neutral point [29]. Medium voltage vectors are not good choices for neutral point voltage balancing. Full load current is connected to the neutral point for the duration of the medium vector duty cycle and will cause low frequency neutral point voltage. Small voltage vectors appear in pairs for each identical vector. The two small vectors in each pair will provide exact opposite load current to the neutral point and can be used as a freedom to control the neutral point voltage balancing. For zero-CM PWM, only medium voltage vectors (and zero vector) are used and no small voltage vector can be used to help the balancing the neutral point voltage like normal SVPWM. Then, the neutral point voltage balancing for zero-CM will be more difficult than normal SVPWM. As shown in Fig. 22, the neutral point voltage of zero-CM PWM is much larger than normal SVPWM with DC side capacitor equaling to 470 uF.

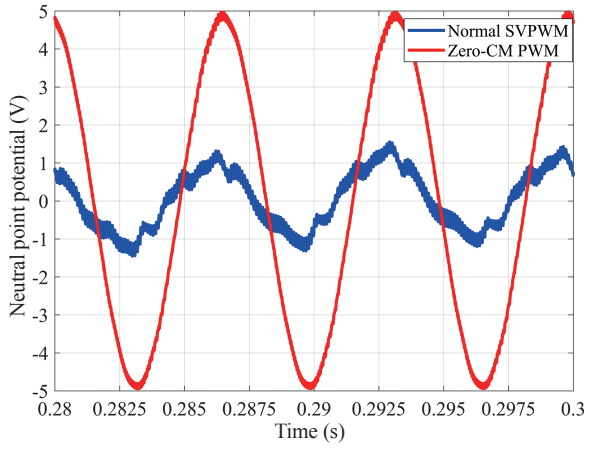

Fig. 22. Neutral point voltage comparison between normal SVPWM and zero-CM PWM.

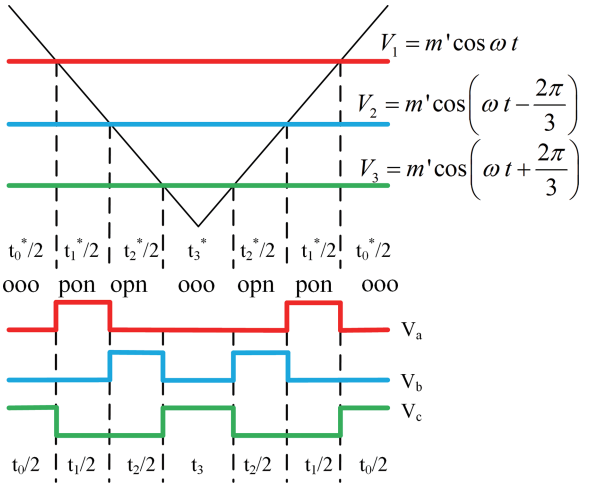

Fig. 23. Zero-CM SVPWM through carrier comparison.

In a word, zero-CM PWM pays the prices of higher THD, serious neutral voltage unbalancing and lower modulation index to achieve theoretical elimination of CM voltage.

C. Implement of Zero Common-Mode Modulation

All discussion above is based on space vector modulation (SVM), whose algorithm is tedious and difficult to implement. However, regular SVM is popular and widely applied by virtue of lower harmonics and higher modulation index. Another well-known modulation is called carrier-based PWM, whose typical representative is sinusoidal pulse width modulation (SPWM), possesses the advantage of easily being implemented. Normal SVPWM can be equivalently realized by injecting zero sequence voltage into balanced three-phase voltage reference of SPWM [27].

It is easy to prove the inherent relationship between the two zero-CM modulations and the result is similar to normal ones. Fig. 23 shows the principle of zero-CM SPWM in sector I, which involves the line-to-line reference transferred into gate drive signals for phase [21].

As shown in Fig. 23, take the gate drive signal of phase-A for example. Firstly, calculating three-phase balanced reference signal V_1, V_2, and V_3. Secondly, comparing the reference signals and triangular carrier to get signals g_1, g_2 and g_3 that must be either 0 or 1, whose progress is similar to the carrier-based PWM method for two level converters. Lastly, the signal $(g_1 - g_2)/2$ is as the reference of the gate drive for phase-A. The value 1, 0, and -1 of $(g_1 - g_2)/2$ represent the output voltage are $V_{dc}/2$, 0, and $-V_{dc}/2$ respectively. Therefore, the fundamental component of phase voltage is equal to $(V_1 - V_2)/2$, which means the real modulation index m is equal to 0.866* m'. The variable m' in V_1, V_2 and V_3 is not representing the modulation index, so m' is used to be distinguished from modulation index m.

The switching sequence in Fig. 23 for carrier-based modulation is the same as Fig. 20(a) for space vector modulation. Distinctly, the duration of effective vectors is equal for volt-second balance. Therefore, the only difference is the duration of zero vector arrangement between center and two side. The injected zero sequence can play the role of distributing transient time of zero vector to realize the equivalence. That is to say, the zero-CM SPWM can be equivalent to zero-CM SVPWM by injecting zero sequence voltage v_z into references V_1, V_2 and V_3. The zero sequence voltage is concluded as $v_z = -(v_{max} + v_{min})/2$, v_{max} (v_{min}) represents the instantaneous maximum (minimum) value of V_1, V_2 and V_3. The other five sectors are the same.

Owing to the equivalent theory, simple zero-CM SPWM is able to replace complicated zero-CM SVPWM without losing the predominance of SVPWM. In DSP controller, we observed that the calculation time for zero-CM SVPWM is 7.31 μs whereas only 4.30 μs for zero-CM SPWM.

IV. Conducted EMI Reduction

A. Variable Switching Frequency Theory for Zero-CM PWM

The zero-CM PWM assuredly reduces CM voltage and current whereas other aspects of performance degrade. Considering the merits of variable switching frequency, the advanced PWM introduced in part II and III can be incorporated together to improve the performance of zero-CM modulation. That is to say, the switching frequency of zero-CM PWM can change according to current ripple prediction model and the limit value for current ripple. The method of prediction model is based on Thevenin's equivalent circuit [16] rather than single-phase model [17] for briefness and convenience. There are only seven vectors in zero CM modulation while two pulses in one switching cycle, which makes the prediction model for single-phase more complicated. Fig. 24 shows four typical transient circuits and their Thevenin's equivalent circuit for phase-A. The current slope for this four different cases could be calculated by (3)-(6) (V_{sum} represents the sum of three-phase voltage) in the light of equivalent circuit and circuit theory.

The current rate for other space voltage vectors and phases is similar to the aforementioned four cases due to the symmetry of three-phase circuit and vectors. Therefore, the current slope for all situations is summarized in TABLE II (i_k represents the

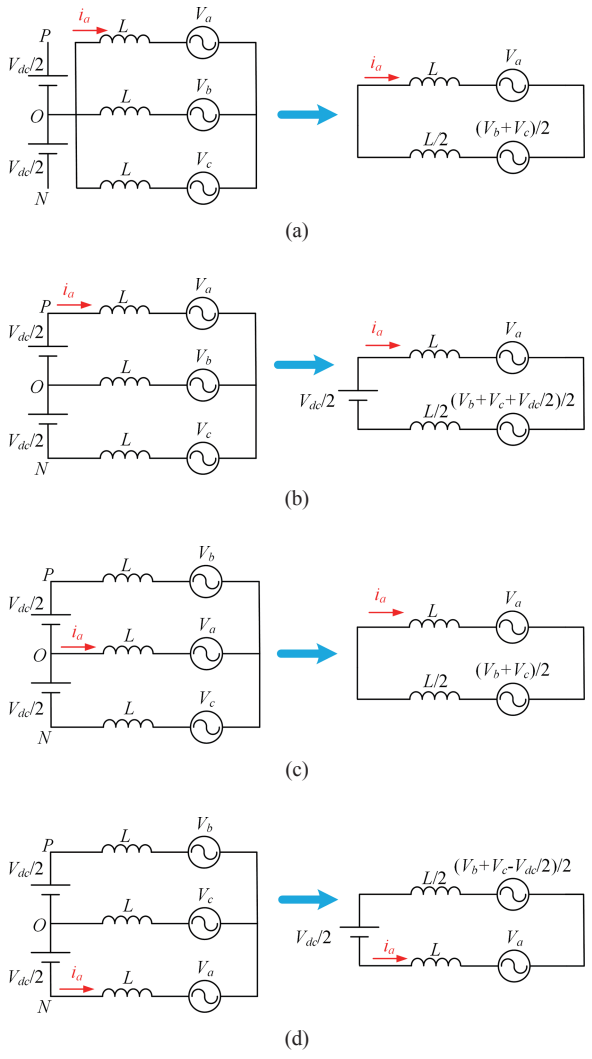

Fig. 24. Four typical transient circuits and their Thevenin's equivalent circuit. (a) vector ooo. (b) vector pon. (c) vector opn. (d) vector npo.

current for phase k, V_k is the same). It is apparent that the current slope is only related to the location of DC bus connected into the phase and phase voltage regardless of other two phases, which makes the model rather simple. Therefore, there are only three kinds of cases for each phase to predict its current ripple based on space vectors, which is rather simple.

$$\frac{di_a}{dt}(ooo)=\frac{1}{3L}(V_{sum}-3V_a) \tag{3}$$

$$\frac{di_a}{dt}(pon)=\frac{1}{3L}(\frac{3}{2}V_{dc}+V_{sum}-3V_a) \tag{4}$$

$$\frac{di_a}{dt}(opn)=\frac{1}{3L}(V_{sum}-3V_a) \tag{5}$$

$$\frac{di_a}{dt}(nop)=\frac{1}{3L}(-\frac{3}{2}V_{dc}+V_{sum}-3V_a) \tag{6}$$

Fig. 25 shows the comparison of high frequency current ripple of experiment and predicted results for model, which powerfully proofs the accuracy of prediction model. The

TABLE II
CURRENT RIPPLE SLOPE FOR ALL SITUATIONS

Condition	Current Ripple Slope
Phase k clamped to positive DC bus	$\frac{di_k}{dt}=\frac{1}{3L}(\frac{3}{2}V_{dc}+V_{sum}-3V_k)$
Phase k clamped to negative DC bus	$\frac{di_k}{dt}=\frac{1}{3L}(V_{sum}-3V_k)$
Phase k clamped to neutral point	$\frac{di_k}{dt}=\frac{1}{3L}(-\frac{3}{2}V_{dc}+V_{sum}-3V_k)$

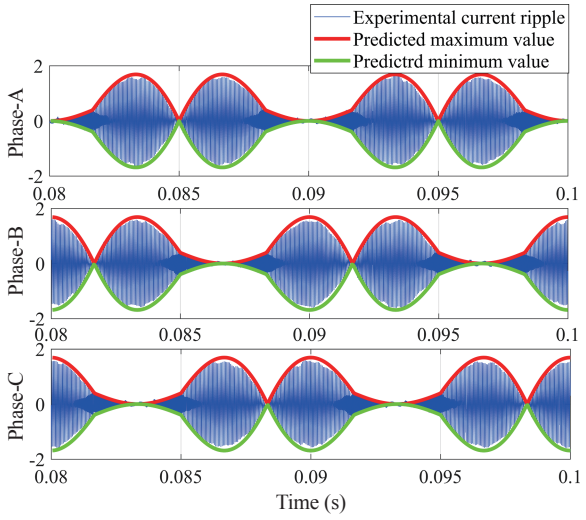

Fig. 25. Current ripple comparison between experiment and prediction (zero-CM SVPWM).

procedure of variable switching frequency is identical to the block diagram in Fig. 8, so the detail progress is not explained any more here. The proposed modulation combines zero-CM and VSFPWM is called zero-CM VSFPWM.

B. Experimental Result of Zero-CM VSFPWM

As mentioned above, zero-CM PWM possesses a big issue with higher switching loss, which may restrain its wide applications. In addition, its space vectors map degenerate to be like two-level makes DM conducted EMI problem serious. Fortunately, by utilizing the freedom of switching frequency, zero-CM VSFPWM can bring many benefits.

Firstly, it is capable of reducing switching loss and raising efficiency of system greatly. Fig. 26 shows the switching frequency for zero-CM VSFPWM, whose carrier frequency varies from 5 kHz to 20 kHz. The criterion to determine the range of switching frequencies is the maximum current ripple of three-phase in switching cycle, which will be made clamped to the required current ripple by changing switching frequency. In this paper, the required current ripple we selected is the maximum current ripple in line cycle. Then, the current ripple at any time is smaller than the required value for constant switching frequency PWM. Therefore, the switching frequency will be

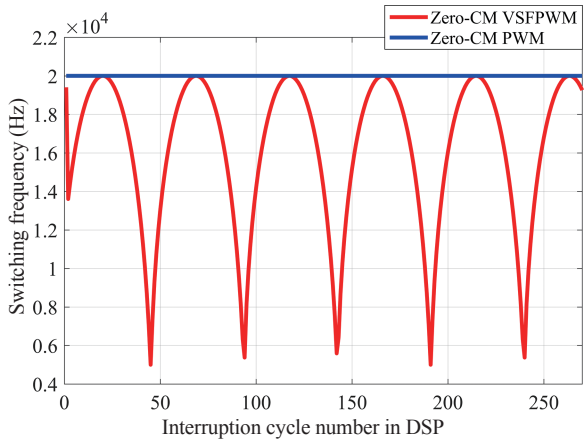

Fig. 26. Switching frequency variation of zero-CM VSFPWM in DSP .

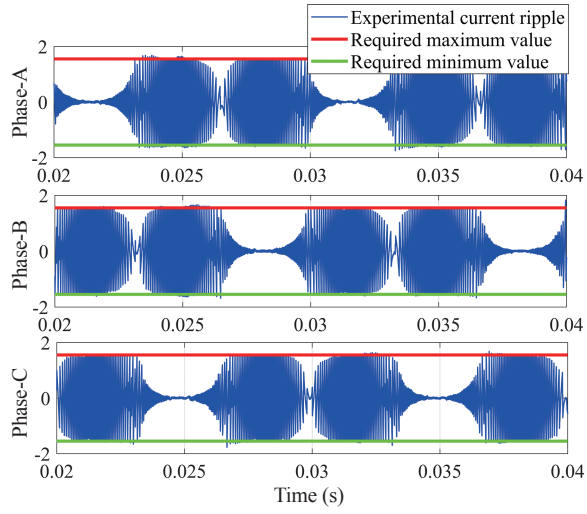

Fig. 27. Three-phase current ripple of zero-CM VSFPWM (experimental result).

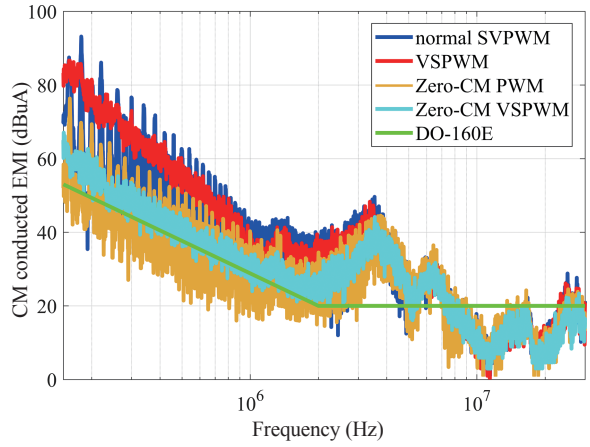

Fig. 28. Comparison of CM conducted EMI (experimental result).

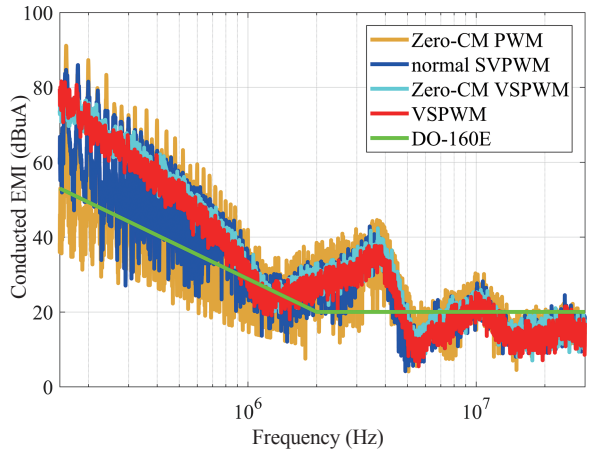

Fig. 29. Comparison of conducted EMI (experimental result).

smaller than the one for zero-CM PWM (20 kHz). Because the minimum three-phase current ripple (not the minimum current ripple for only one phase) is the one fourth of maximum current ripple in line cycle, the switching frequency range will be from 5 kHz to 20 kHz. This rather large range variation of switching frequency validates the huge advantage of VSFPWM and reduces the switching losses of zero-CM PWM. The current ripple of zero-CM VSFPWM is shown in Fig. 27. Compared with ripple in Fig. 25 for zero-CM PWM, zero-CM VSFPWM methods have better effective utilization rate of space limited by the identical required current peak value (±1.65 A) apparently.

Secondly, the CM conducted EMI can be further reduced. Fig. 28 shows CM conducted EMI for four modulations mentioned in this paper. It is apparent that the envelope curve of zero-CM VSFPWM is the lowest and reduces more than 20 dB in comparison with normal SVPWM.

Finally, the conducted EMI of zero-CM VSFPWM has huge superiority compared with other modulations. For conducted EMI test requirement, the current in line is conducted to EMI receivers for test, which do not distinguish DM and CM components. Fig. 29 shows the conducted EMI in transmission line considering CM loop. On the one hand, zero-CM VSFPWM EMI is smaller than zero-CM and SVPWM, and almost as big as VSFPWM. On the other hand, zero-CM VSFPWM spread spectrum, which would further reduce the damage caused by CM noise.

As mentioned above, the variable switching frequency methods have impact on low frequency harmonics and THD. Fig. 30 shows the FFT results of phase currents for both zero-CM PWM and zero-CM SVPWM. Apart from 2nd fundamental harmonics, variable switching frequency methods hardly have influence on other low frequency harmonics. Also, the THD only increases by 1.71%. In summary, zero-CM VSFPWM could improve the performance of zero-CM PWM, at the same time reduces CM problem furtherly.

C. Comprehensive Comparison of Four PWM Methods

Based on previous discussion of four mentioned PWM methods, TABLE III summaries their comprehensive comparison of SVPWM, VSFPWM, zero-CM PWM, and zero-CM VSFPWM. Firstly, variable switching frequency methods can decrease conducted EMI and switching loss compared with

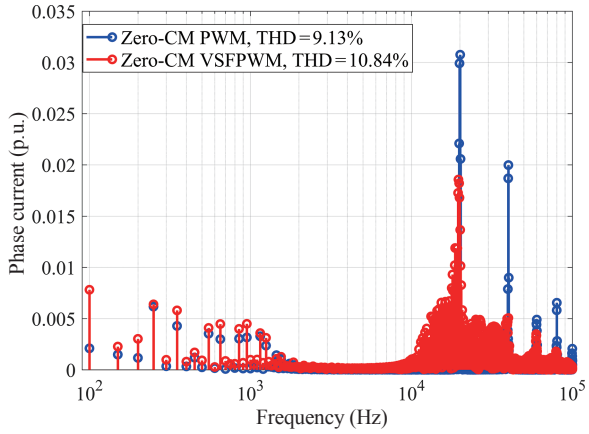

Fig. 30. Comparison of phase current spectrum: zero-CM PWM and zero-CM VSFPWM (experimental result).

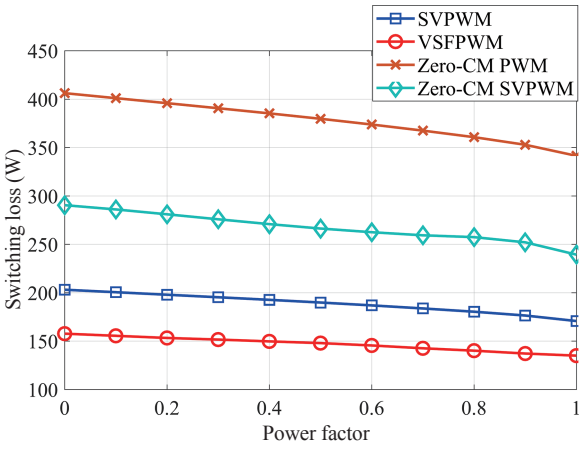

Fig. 31. Comparison of switching loss with different power factor (calculation result).

TABLE III
COMPARISON OF FOUR PWM METHODS

Performance	SVPWM	VSFPWM	Zero-CM SVPWM	Zero-CM VSFPWM
THD (a specific condition)	4.43%	6.28%	9.13%	10.84%
Average Switching Frequency	20 kHz	13.64 kHz	20 kHz	16.09 kHz
Efficiency (a specific condition)	98.15%	98.26%	97.61%	97.94%
Switching Loss	small	smallest	biggest	big
CM Current	big	big	small	small
Conducted EMI	bigger	small	biggest	small

invariable switching frequency methods. Then, zero-CM PWM methods pay the prices of higher THD, serious neutral voltage unbalancing and lower modulation index to achieve theoretical elimination of CM voltage. Lastly, zero-CM VSFPWM methods can improve the worse performance of zero-CM PWM, which contain bigger switching loss and higher conducted EMI.

In the TABLE III, we observed that the algorithm with variable switching frequency reduce switching loss greatly and increase the efficiency by 0.11% and 0.33% for VSFPWM and zero-CM VSFPWM respectively. In addition, zero-CM PWM makes the efficiency decreases by 0.54% for the double switching action compared with normal SVPWM during a switching cycle. Fortunately, the zero-CM VSFPWM can compensate the disadvantage with low efficiency for zero-CM PWM. In order to understand the efficiency of the four methods thoroughly, a switching loss curve with different operating points with calculation method is provided. The three-level converter module used in the platform is FS3L50R07W2H3F_B11 produced by Infineon. The operating point is DC voltage 600 V and phase current 50 A, whose parameters are selected to calculate switching loss of the module to increase the computational accuracy. The following Fig. 31 is the switching curve with different power factor. It is noticeable that the switching loss decreases with the increasing of power factor.

V. CONCLUSION

This paper gives a comprehensive study on EMI reduction methods for three-level voltage source inverter through PWM. It contains the study of both DM and CM EMI reduction.

For DM conducted EMI noise reduction, this paper introduced VSFPWM method based on the current ripple prediction model for three-level voltage source inverter. For three-level inverter, with carrier-based PWM analysis, current ripple prediction model has been proposed. Then, VSFPWM method has been developed for three-level inverter to control the current ripple peak value. Experimental result demonstrates the attenuation of EMI noise peak value for three-level inverter, with current ripple peak value to be the same with normal SVPWM.

Three-level inverters possess the freedom to restrain CM by selecting appropriate vectors to reduce common-mode voltage. However, the attenuation of CM conducted EMI pays the price of lower utilization of DC voltage, higher THD and more switching losses. The equivalence of two significant PWM contributes to simplify algorithm is introduced at the same time to optimize the algorithm for zero-CM modulation.

The variable switching frequency method successfully expands to zero common-mode modulation, whose mechanism is briefly illustrated with experimental results. This advanced method greatly reduces switching loss, decreases conducted EMI and has further improvement on CM problem.

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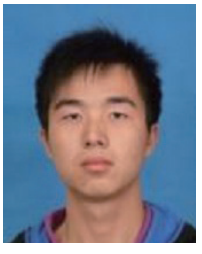

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Equivalent Modeling Method for Regional Decentralized Photovoltaic Clusters Based on Cluster Analysis

Hongbin Wu, Zhongqian Liu, Yu Chen, Bin Xu, and Xianjun Qi

***Abstract*—A large number of photovoltaic (PV) systems are decentralized and connected to distribution networks, leading to challenges in model simulation. This paper presents an equivalent modeling method for regional decentralized PV clusters based on cluster analysis. The proposed method is based on the grouping principle that PV systems have similar dynamic response characteristics, and grouping results are obtained using a fuzzy C-mean (FCM) clustering algorithm. Based on the clustering evaluation index, the optimal grouping number can then be determined and PV systems in the same group are combined into an equivalent PV system. The method to acquire equivalent parameters for PV arrays, transformers, and lines is also presented. A multi-machine equivalent model of regional decentralized PV clusters is established, and the precision and efficiency of the proposed method is demonstrated using an actual distribution network.**

***Index Terms*—Distribution network, equivalent modeling, fuzzy C-mean clustering, photovoltaic cluster, regional decentralization.**

I. Introduction

SOLAR energy is a clean, renewable energy that has undergone rapid development and large-scale application, with photovoltaic (PV) grid-connected systems being the most important solar energy application [1]-[3]. In China, with the implementation of PV power generation poverty reduction policies, many PV power stations are decentralized and connected to distribution networks, forming regional decentralized PV clusters [4]. This increases the complexity of the distribution network model and leads to challenges such as long simulation times, huge memory usages, and difficulty updating models. Therefore, it is necessary to establish a simplified equivalent model of regional decentralized PV clusters.

In recent years, equivalent modeling of PV system research has concentrated primarily on regional centralized PV systems or large-scale PV power stations. In [5], the authors propose an online clustering modeling method for large-scale PV power plants, using the control parameters of inverter as the clustering index. In [6], two equivalent modeling methods for PV system are proposed for partially shielded and unshielded PV cells. To study the transient characteristics of large-scale PV power stations and avoid constructing detailed models for every type of inverter, Mukherjee *et al*. [7] analyzed the effectiveness of the model reference adaptive control (MRAC) approach for modeling a grid connected inverter system. In [8], the equivalent dynamic model of an actual PV power station with virtual synchronous characteristics was studied, and a method was proposed to obtain the dynamic equivalent model of a group of PV converters based on the synchronous power controller.

The study of equivalent modeling of regional decentralized PV system is in its infancy. In the coherent-based equivalent method of large-scale power grids, the coherent generator group is equivalent to corresponding aggregates, and only key transmission lines and nodes are retained. Therefore, the power system scale can be reduced and the main dynamic characteristics can be preserved [9]-[11]. However, the PV power generation is different from conventional power generation, so the criterion for PV system coherency must be defined to benefit from a coherency-based equivalent method. PV systems with similar dynamic responses under the same disturbance are considered coherent, and they should be combined into an equivalent PV system to ensure the dynamic characteristics of the original system remain unchanged.

This paper proposes an equivalent modeling method for regional decentralized PV clusters. The clustering index is selected from the response curves of PV systems during a disturbance. Then, a fuzzy C-mean (FCM) clustering algorithm is used to obtain dynamic grouping results, and PV systems in the same group are combined into an equivalent PV system, establishing a multi-machine equivalent model of regional decentralized PV clusters. Finally, simulation analysis is performed using an actual distribution network in Anhui province.

II. Clustering Index

A. Model of Regional Decentralized PV Cluster

A PV cluster is a collection of PV systems that are near each other with only small differences in solar radiation, and the same point of interconnection (PCC). Taking the city of Jinzhai, Anhui province as an example, a total of 295 small village PV systems have been built and connected to a distribution net-

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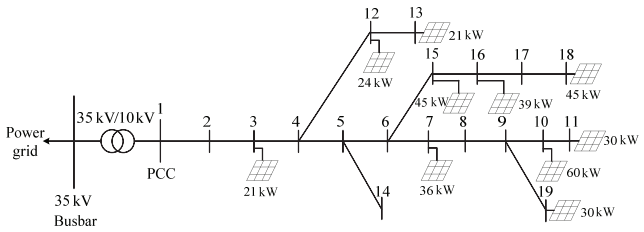


Fig. 1. Regional decentralized PV clusters.

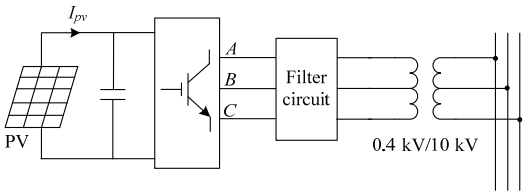


Fig. 2. The structure of a single PV system.

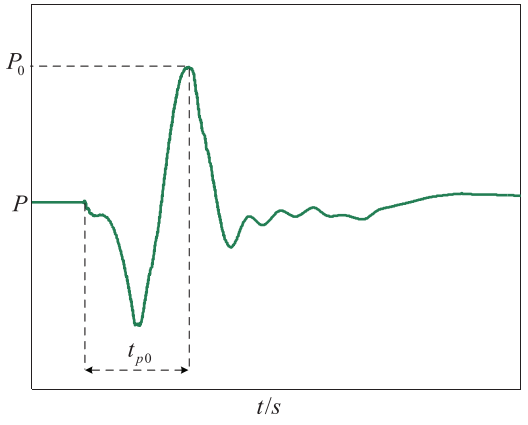


Fig. 3. Sketch of active power disturbance curve extraction.

work, forming several regional decentralized PV clusters. A typical PV cluster under a 35 kV substation is shown in Fig. 1, there are 10 PV systems in all, which is called the detailed model.

The common model of a single PV system is shown in Fig. 2, which contains a PV array, a grid-connected inverter, a filter, and other devices. The specific characteristic equation can be referred to in [12], but is not described in detail in this article.

B. Clustering Index of PV System

The basic idea of a regional decentralized PV cluster is to combine PV systems that have similar dynamic responses into an equivalent PV system. However, dynamic features of PV systems are influenced by many factors, including inverter controller parameters, the location and capacity of PV systems, and other parameters. Therefore, it is difficult to propose a reasonable clustering index from inherent parameters of a system model [13]. In this paper, the feature points extracted from the response curve of a PV system are taken as the clustering index. The active power response curve of a PV system under typical disturbance is shown in Fig. 3.

In Fig. 3, P_0 is the first peak and t_{p0} is the time from the start of the dynamic process to the first peak. For the reactive power response curve, extraction of feature points is the same as for active power, with the two feature points being recorded as Q_0 and t_{q0} , respectively.

Considering that under a three-phase short-circuit disturbance, the dynamic response of a PV system is generally the most obvious, when a three-phase short-circuit fault occurs at the PCC point, the vector $[P_0, t_{p0}, Q_0, t_{q0}]$ of each PV system is taken as the clustering index. Note that parameters must be normalized due to differences in dimensions and orders of magnitude of parameters.

III. Multi-Machine Equivalence of Regional Decentralized PV Clusters

A. Clustering Method of PV Systems Based on the FCM Algorithm

The clustering algorithm is an iterative optimization process, where the similarity between the clustering index which are in the same group is greater, and the similarity between clustering index of different groups is smaller[14]-[18]. On the basis of general clustering, the concept of fuzzy clustering is proposed. Through the FCM algorithm, n clustering indexes $x_j (j = 1,2,...,n)$ that corresponding to n PV systems are divided into c groups, it is determined which group each clustering index belongs to by the membership between [0,1], and the clustering centers of each group are calculated v_i (i = 1,2,...,c) to get the minimal value of the objective function. The objective function is as follows:

$$J_m(U,c) = \sum_{i=1}^{c}\sum_{j=1}^{n} \mu_{ij}^{\ m} \parallel v_i - x_j \parallel_2 \tag{1}$$

where $\|v_i\text{-}x_j\|_2$ is the Euclidean distance between the i^{th} cluster center v_i and the clustering index of the j^{th} PV system x_j, m is the weighting exponent, $m \in [1,\infty)$, usually m is 2, $c \in [2,\sqrt{n}]$, u_{ij} is the membership value that the j^{th} PV system belongs to the i^{th} cluster center, which satisfies normalization:

$$s.t.\begin{cases} \sum_{i=1}^{c} \mu_{ij} = 1, & 1 \le j \le n \\ \mu_{ij} \in [0,1], \quad 1 \le j \le n, & 1 \le i \le c \\ n > \sum_{j=1}^{n} \mu_{ij} > 0, & 1 \le i \le c \end{cases} \tag{2}$$

In order for (1) to achieve the minimum value, the following functions are constructed:

$$\overline{J}_m(U,c,\lambda) = J_m(U,c) + \sum_{j=1}^{n} \lambda_j (\sum_{i=1}^{c} u_{ij} - 1) \tag{3}$$

where λ_j is the Lagrange multiplier of (2). By taking the derivative of all input parameters, we can get the necessary condition for (1) to get the minimum value, which is as follows:

$$v_i = \sum_{j=1}^{n} \mu_{ij}^{\ m} x_j / \sum_{j=1}^{n} \mu_{ij}^{\ m} \tag{4}$$

$$\mu_{ij} = \frac{1}{\sum_{k=1}^{c} \left(\frac{\| x_j - v_i \|_2}{\| x_j - v_k \|_2} \right)^{\frac{2}{m-1}}} \tag{5}$$

Thus, the output of the FCM algorithm includes two parts: the first part is c clustering centers, and each clustering center represents the average characteristics of the clustering index of the PV systems, the second part is a $c \times n$ -order membership matrix, which represents the membership that each PV system belongs to each group. Generally, the rule of maximum membership determines which group the PV systems belong to.

To evaluate the clustering effect and determine the optimal grouping number, two evaluation indices, the partition coefficient(PC) and the classification entropy(CE), are defined as follows:

$$PC = \frac{1}{n} \sum_{i=1}^{c} \sum_{j=1}^{n} (\mu_{ij})^2 \tag{6}$$

$$CE = -\frac{1}{n} \sum_{i=1}^{c} \sum_{j=1}^{n} \mu_{ij} \log(\mu_{ij}) \tag{7}$$

where PC is used to evaluate the degree of separation of different PV groups, the larger the better, and CE is used to evaluate the degree of fuzziness of different PV groups, the smaller the better.

B. Multi-Machine Equivalent Model

Using the FCM algorithm to group PV systems in Fig. 1, the detailed steps are shown as follows:

Step1: The clustering index [P_0, t_{p0}, Q_0, t_{q0}] are constructed for all PV systems.

Step2: A membership matrix is generated randomly, which satisfy (2).

Step3: Updating the clustering centers through the membership matrix according to (4).

Step 4: Updating the membership matrix through the clustering centers according to (5).

Step5: Repeating steps 3 and 4 until the change of the value of the objective function calculated by (1) is less than the permissible value.

Step 6: Calculating the clustering evaluation indices and according to (6) and (7).

Step 7: Changing the number of groups c, and come back to step 2 to group the PV systems again. The best number of groups is determined by comparing the values of PC and CE under different number of groups, and the final grouping results of PV system are determined by the membership matrix at this time.

The n PV systems are divided into c groups through the above steps, then PV systems that are in the same group are merged into an equivalent PV system, all equivalent PV systems are then connected to the PCC. The equivalent model is shown in Fig. 4.

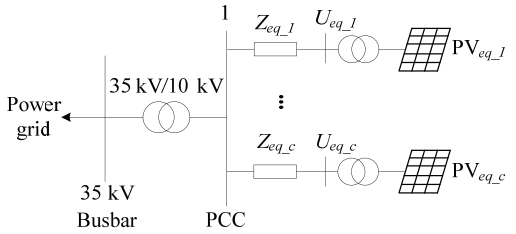


Fig. 4. Equivalent model of regional decentralized PV cluster.

The equivalent model of regional decentralized PV clusters is required to have the same external characteristics as the detailed model. That is to say, the two models should have similar dynamic response curves at the PCC point, including power, frequency, current, voltage, and so on.

IV. Equivalent Parameters Calculation

In Fig. 4, taking the x^{th} ($1 \le x \le c$) equivalent PV system as an example, and supposing that the x^{th} equivalent PV system is merged by M PV systems, the calculation method of the equivalent parameters is as follows.

A. Equivalence of PV Array

In the actual operation, it is difficult to ensure the power generation of PV systems due to partial shading and passing clouds, at this point, we can adopt parameter identification method to get the equivalent number of PV modules under ideal condition according to reference [19], thus the actual power generation of each PV array can be obtained, denoted as P_k(k = 1,2,...,M). The power generation of the x^{th} equivalent PV array is as follows:

$$P_{eq\_x} = \sum_{k=1}^{M} P_k \tag{8}$$

B. Equivalence of Line Parameters

Before equivalence, the voltage difference between the M PV systems and the PCC can be obtained by the power flow calculation, which is denoted as ΔU_k(k = 1,2,...,M). Then we can calculate the weighted average voltage difference of the M PV systems (the power of a PV system is used for weighting) as:

$$\Delta \bar{U}_x = \sum_{k=1}^{M} (\Delta U_k P_k) / \sum_{k=1}^{M} P_k \tag{9}$$

After equivalence, according to Fig. 4, the voltage difference between the x^{th} equivalent PV system and the PCC is calculated as follows:

$$\Delta \bar{U}_{eq\_x} = \frac{Z_{eq\_x} P_{eq\_x}}{\sqrt{3} U_{PCC}} \tag{10}$$

where U_{PCC} is the voltage of at the PCC point .

Solving the equation $\Delta \bar{U}_x = \Delta \bar{U}_{eq\_x}$, the impedance of the equivalent line is as follows:

$$Z_{eq\_x} = \frac{\sqrt{3}U_{pcc}\sum_{k=1}^{M}(\Delta U_k P_k)}{\left(\sum_{k=1}^{M} P_k\right)^2} \tag{11}$$

The above is the equivalent method of line impedance. Because the length of the line is short and the voltage is low, the influence of line capacitance can be ignored.

C. Equivalence of Transformer Parameters

According to Fig. 2, the equivalent impedance circuit of a single PV system can be simplified as shown in Fig. 5. where Z_{tr_k} is the impedance of the k^{th} PV transformer. Therefore, before equivalence, the total loss of the M transformers can be calculated by:

$$S_x = \sum_{k=1}^{M} {I_k}^2 Z_{tr\_k} \tag{12}$$

After equivalence, the loss of the transformer in the x^{th} equivalent PV system is:

$$S_{eq\_x} = {I_{eq\_x}}^2 Z_{tr\_eq\_x} \tag{13}$$

At the same voltage level, it is thought that $I \propto P$. Therefore, by solving the equation $S_x = S_{eq\_x}$, the impedance of the x^{th} equivalent transformer can be obtained:

$$Z_{tr\_eq\_x} = \frac{\sum_{k=1}^{M}(P_k^2 Z_{tr\_k})}{(\sum_{k=1}^{M} P_k)^2} \tag{14}$$

Due to the low voltage level, the loss of the transformer excitation branch is small and can be ignored.

D. Equivalence of Inverter Parameters

The equivalent PI controller parameter of grid-connected inverters can be calculated using the capacity weighted method [20] as follows:

$$X_{eq\_x} = \sum_{k=1}^{M}(X_k P_k) / \sum_{k=1}^{M} P_k \quad X = k_{pu}, k_{iu}, k_{pi}, k_{ii} \tag{15}$$

where k_{pu} and k_{iu} are the proportional and integral coefficients of the voltage outer loop, respectively, and k_{pi} and k_{ii} are the proportional and integral coefficients of the current inner loop, respectively.

To ensure the filtering effect of equivalent inverters, and that reactive power consumption remains unchanged before and after the equivalence, the equivalent filter inductance can be acquired by:

$$L_{eq\_x} = \sum_{k=1}^{M} L_k / M^2 \tag{16}$$

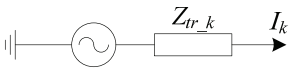


Fig. 5. Equivalent impedance circuit of a single PV system.

E. Error Analysis of Equivalent Model

In order to analyze the error of equivalent model proposed in this paper, the simulation results of the detailed model of PV cluster are taken as the reference, the error evaluation index of equivalent model is calculated as follows:

$$E = \int_{t_1}^{t_2} \left| \frac{Y_d - Y_e}{Y_d} \right| dt \tag{17}$$

where t_1 and t_2 are the start time and end time of simulation, respectively, Y_d and Y_e are the electrical quantity of the detailed model and the equivalent model at PCC, respectively, the electrical quantity here can be active power, reactive power, frequency and so on.

V. Numerical Examples

A. Example of the System

The simulation system is the same as shown in Fig. 1. A typical double-loop controller is used as the inverter controller model, which contains a power outer loop and a current inner loop. The reference value of reactive power is set to zero, making the power factor unity. The main parameters of the system are shown in TABLE I and TABLE II. The line model is LGJ-35.

B. Clustering Result Analysis

The FCM algorithm is used to group the above regional decentralized PV cluster, when the grouping number is different, the evaluation indices of PC and CE are shown in Fig. 6.

As can be seen in Fig. 6, when the regional decentralized PV cluster is divided into two groups, the evaluation index PC is at a maximum and CE is at a minimum. Therefore, the optimal grouping number is $c = 2$. Results are shown in TABLE III.

The equivalent model of the regional decentralized PV cluster was calculated based on the method presented in Section III and is given in TABLE III.

C. Equivalence Effect Verification

In order to verify the effect of the equivalent model, the following four cases are simulated:

1) Three-Phase Short Circuit Fault

This simulation will compare the proposed equivalent method with the traditional single-machine equivalent method to verify the method in this paper. A three-phase short circuit fault occurs at the PCC point at 0.3 s and the fault clears at 0.38 s. The response curves of the detailed model, the proposed equivalent model, and the traditional single-machine equivalent model at PCC are shown in Fig. 7, the error calculation results are shown

TABLE I
LINE PARAMETERS

Line	Length (m)	Line	Length (m)
1-2	1839	10-11	435
2-3	1266	4-12	241
3-4	1679	12-13	1180
4-5	583	5-14	146
5-6	115	6-15	1610
6-7	386	15-16	1528
7-8	1298	16-17	985
8-9	90	17-18	708
9-10	172	9-19	2319

TABLE II
PV NODE PARAMETERS

Node Number	Power (kW)	Inverter Parameters k_{pu}	k_{iu}	k_{pi}	k_{ii}	L_k(mH)	Transformer Type
3	21	0.51	0.86	150	10	0.125	S11-100/10
7	36	0.80	2.55	100	5	0.125	S11-125/10
10	60	0.62	1.23	400	1	0.125	S11-M-200/10
11	30	0.45	3.24	200	8	0.125	S11-M-200/10
12	24	0.75	1.05	300	2	0.125	S11-160/10
13	21	0.50	1.56	350	6	0.125	S11-100/10
15	45	0.42	0.65	250	1	0.125	S9-100/10
16	39	0.35	2.20	100	10	0.125	S11-M-100/10
18	45	0.62	1.64	400	4	0.125	S9-100/10
19	30	0.80	2.76	150	5	0.125	S11-M-100/10

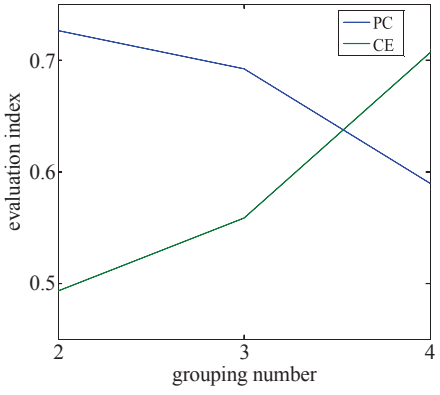


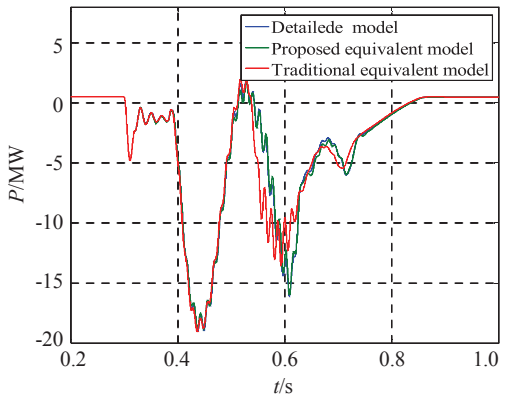
Fig. 6. Evaluation index of the clustering effect.

in TABLE IV, the actual time spent in the simulation process of the three models are shown in TABLE V.

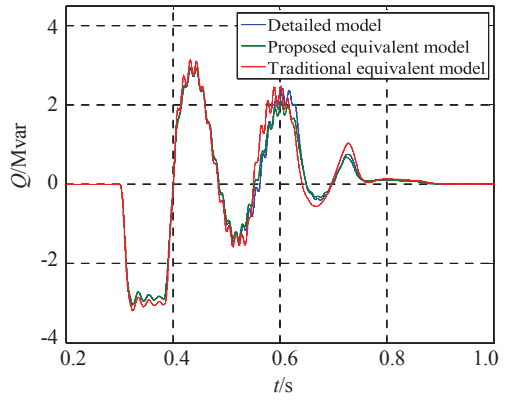
As shown in Fig. 7 and TABLE IV, the equivalent model in this paper has higher precision than the traditional single-machine model. TABLE V shows that the simulation time of the equivalent model in this paper is much lower than that of the detailed model, and is close to that of the traditional single-machine equivalent model. Therefore, the proposed equivalent model in this paper balances precision and simplification. However, this method also has some limitations, when the structure of distribution network or the capacity of PV systems changes,

TABLE III
BEST GROUPING RESULTS

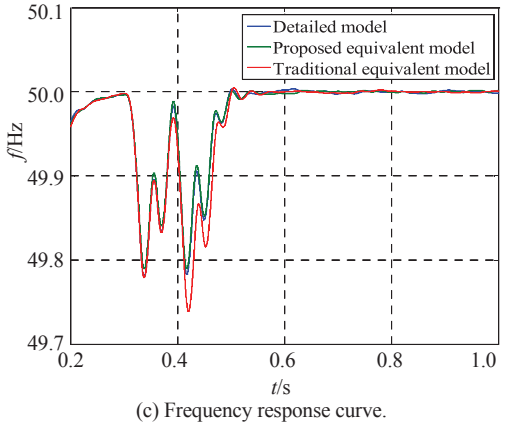
	PV System Node Number
Group 1	3, 7, 11, 12, 13, 19
Group 2	10, 15, 16, 18



(a) Active power response curve.



(b) Reactive power response curve.



(c) Frequency response curve.

Fig. 7. Response curves for three-phase short circuit.

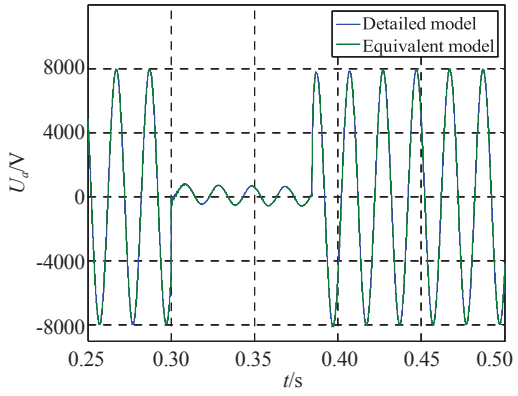
the power response curve under typical disturbance shown in Fig. 3 will also change, which leads to the change of clustering index, therefore we need to rebuild the clustering index for each PV system, it will increase much calculation burden.

TABLE IV
ERROR CALCULATION RESULTS

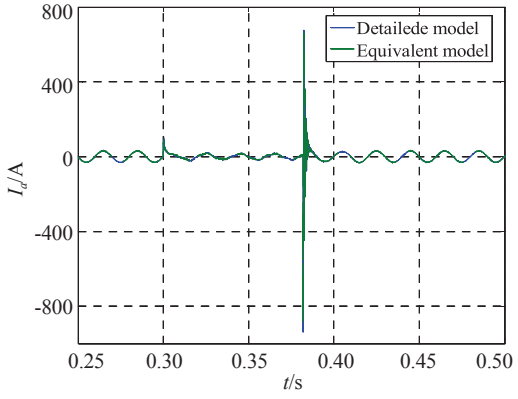
	Proposed equivalent model	Traditional equivalent model
Active power error	0.0041	0.0115
Reactive power error	0.0095	0.0340
Frequency error	0.0018	0.0044

TABLE V
MODEL SIMULATION TIME

	Detailed model	Proposed equivalent model	Traditional equivalent model
Time spent	25 s	7 s	5 s



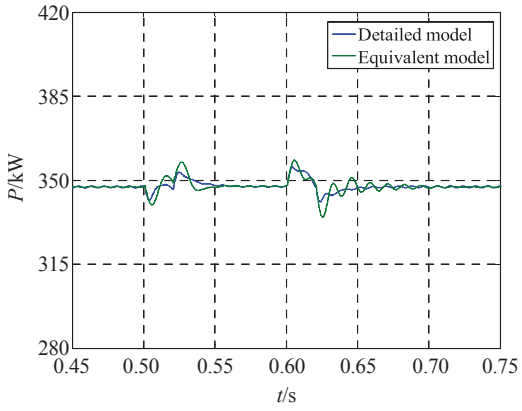
(a) Phase A voltage.



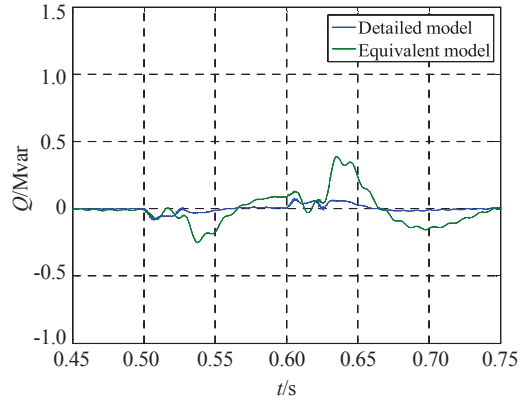
(b) Phase A current.

Fig. 8. Voltage and current response curves for single-phase short circuit.

As a final note, the equivalent model in this paper is a two-machine equivalent model based on TABLE III, but it does not mean that this equivalent model has the highest precision. In general, the more grouping number, the higher precision of the established equivalent model, but the model will be more complex correspondingly. In this paper, the best grouping number is chosen by the calculation of PC and CE, so the established equivalent model can best balance precision and simplification in theory.



(a) Active power response curve.



(b) Reactive power response curve.

Fig. 9. Response curves for voltage disturbance from power grid.

2) Single-Phase Short Circuit Fault

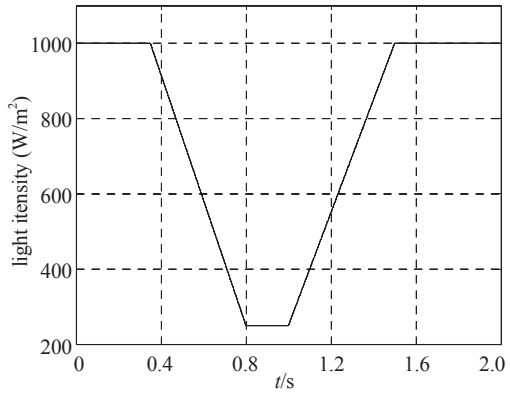
The clustering index of the PV system is constructed under the condition of a three-phase short circuit fault as shown in section II. To verify the application of the equivalent model to another fault situation, a single-phase ground fault occurs at PCC point at 0.3 s and the fault clears at 0.38 s. Voltage and current curves of the detailed model and the equivalent model at the PCC point are shown in Fig. 8.

Fig. 8 shows that the external characteristics of the equivalent model are in agreement with that of the detailed model. Therefore, the clustering index presented in this paper is reasonable, and a PV system with similar dynamic characteristics can be divided into the same group by the clustering algorithm.

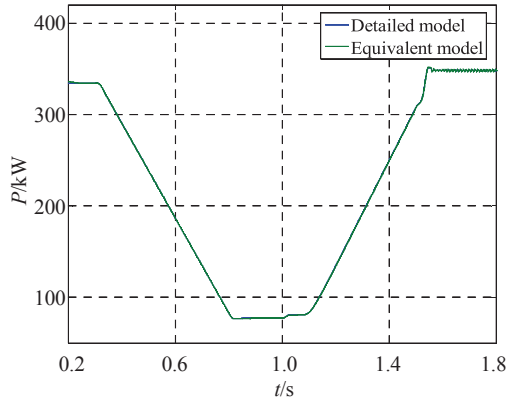
3) Voltage Disturbance From Power Grid

Three-phase short circuit fault and single-phase short circuit fault are both large disturbance, in order to verify the accuracy of the equivalent model under small disturbance, small disturbance of power grid voltage is set in this simulation: the power grid voltage change from 1.0 p.u to 0.9 p.u at 0.5 s, and the voltage is restored to 1.0 p.u at 0.6 s. The active and reactive power curves of the detailed model and the equivalent model at PCC are shown in Fig. 9.

As seen in Fig. 9, the response curve of equivalent model is still agreement with the detailed mode under small voltage disturbance from power grid, this comparison shows the effective-



(a) Light intensity curve.



(b) Reactive power response curve.

Fig. 10. Response curves for light intensity disturbance.

ness of the proposed clustering modeling method again.

4) Light Intensity Disturbance

In this section, a comparison is shown when the external environment changes. In the simulation, the light intensity of the system is shown in Fig. 10(a). The active power response curves of the detailed model and the equivalent model at the PCC point are shown in Fig. 10(b).

As seen in Fig. 10, the duration of interruption in light intensity is long, and the system response is not severe. Therefore, by using maximum power point tracking (MPPT), the active power of the PV cluster can effectively track the change in light intensity and the active power response curves of the two models are very similar.

VI. Conclusion

This paper presents an equivalent modeling method for regional decentralized PV clusters. By extracting feature points of response curves, the clustering index of a PV system is given. The PV systems are then divided into groups by a FCM clustering algorithm. PV systems that are in the same group are merged into an equivalent PV system by calculation of equivalent parameters, establishing an equivalent model of the regional decentralized PV cluster.

Simulation results and error analysis shows the effectiveness of the proposed method. The optimal grouping number is determined by the evaluation indices PC and CE, and the established equivalent PV system has a similar response to disturbances such as short-circuit faults, grid voltage fluctuation and external environment changes as the detailed model. Whether this method can be extended to other types of distributed generator cluster is a topic for further research.

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Power Quality Improvement Using VLLMS Based Adaptive Shunt Active Filter

Pravat Kumar Ray

***Abstract*—The power quality problem in the power system is increased with the use of non-linear devices. Due to the use of non-linear devices like power electronic converters, there is an increase in harmonic content in the source current. Due to this there is an increase in the losses, instability and poor voltage waveform. To mitigate the harmonics and provide the reactive power compensation, we use filters. There are different filters used in the power system. Passive filters provide limited compensation, so active filters can be used for variable compensation. In this paper, a shunt active filter has been made adaptive using a Variable Leaky Least Mean Square (VLLMS) based controller. Proposed adaptive controller can be able to compensate for harmonic currents, power factor and nonlinear load unbalance. DC capacitor voltage has been regulated at a desired level using a PI controller and a self-charging circuit technique. The design concept of proposed adaptive controller for shunt active filter has been verified through simulation and experimentation.**

***Index Terms*—APF, harmonics, neural network, power quality, Variable Leaky Least Mean Square (VLLMS).**

I. Introduction

OVER the past few years, rapid increase in the use of non-linear loads causes many power quality issues, like high current harmonics, low power factor and excessive neutral current. The increased harmonics, reactive power and unbalance cause increase in voltage distortion, line losses and instability when harmonic current travel upstream and produce drop across the line impedance, which leads distortion in power system. Usually, passive filters are used for suppression of harmonics but their applications are limited to fixed amount of compensation. Passive filters are also not capable in providing solutions in presence of unbalance and variable reactive power compensation. Another disadvantage with passive filter is the problem of resonance which amplifies current of certain harmonic frequencies. The solution to above mentioned problem can be realized using a shunt active power filter [1]-[4].

APF performance basically depends on the way of estimating the reference compensating signal. Instantaneous reactive power (IRP) theory [5], synchronous reference frame (SRF) theory [6] and modified p-q theory [7] etc. are the well-known methods of generating current reference by maintaining dc link voltage. These above cited methods are very attractive for their simplicity and ease of implementation but they are incapable in providing appropriate solution in presence of more harmonics, reactive power and unbalance or their combinations with limited power rating of voltage source inverter (VSI) used as APF. Soft computing techniques such as neural network have been discussed in [8]-[10]. So it can be seen that use of artificial intelligence has been used very often as a controller in shunt active filter. A model reference adaptive sliding mode control (MRASMC) using radial basis function (RBF) [11] has been used as a controller in single phase active power filter (APF). An adaptive sliding mode control with a double loop recurrent neural network (DLRNN) [12] structure has been used for nonlinear dynamics system. A new control using sliding mode control -2 [13] has also been implemented in Hybrid Series Active Power Filter (HSAPF) for making it robust and stable.

So far as signal processing techniques are concerned, Least Mean Square (LMS) is a favorable choice. Because of fixed step size in conventional LMS technique, it has slower rate of convergence. This can be overcome using time varying step size [14]. Since least mean square of error is taken as the cost function in LMS algorithm, weights are not bounded and it takes more time to respond because of stalling effect [14]. To overcome this, leaky LMS algorithm is employed where magnitudes of weights are also included in cost function to nullify the stalling and parameter drifting effect [15], [16].

This paper proposes a VLLMS based technique for shunt active filter. Harmonic currents and reactive component of nonlinear load can be extracted using a circuit based on above technique. Both harmonic and reactive current of nonlinear load together with signal from self-charging circuit [17] form the reference injection current of adaptive hysteresis controller for generating switching signal of three phase IGIT voltage source inverter. It becomes also able to compensate for unbalanced load currents and bring the power factor of the supply side to become unity. DC capacitance is also maintained at a desired level using a self-charging circuit. The main contribution of the paper is on the implementation of VLLMS in active power filter circuit for faster adaptation of active filter to any variations in operating conditions. Conventional weight updating algorithm is modified by replacing with VLLMS based weight updating algorithm, which greatly enhances the speed of algorithm and extraction. Another contribution of this paper is the use of Adaptive Hysteresis Band Current Control technique for avoiding acoustic noise uneven switching frequency in hysteresis band current control.

The paper is organized as follows. Section II discusses in detail about adaptive shunt active power filter. Section III shows the simulation results and discussion. Section IV experimentally

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verifies the proposed algorithm. Section V concludes the paper.

II. Adaptive Shunt Active Power Filter

A. System Configuration

The current source i_L is used to model the instantaneous current of the nonlinear load that can be represented by

$$i_L(t) = i_{L1}\sin(\omega t + \phi_{L1}) + \sum_{n=2}^{\infty} i_{Ln}\sin(n\omega t + \phi_{Ln})$$

$$i_L = i_{L1}\sin\omega t\cos\phi_{L1} + i_{L1}\sin\phi_{L1}\cos\omega t + \sum_{n=2}^{\infty} i_{Ln}\sin(\omega t + \phi_{Ln})$$

$$i_L = i_{L1,p} + i_{L1,q} + i_{Ln} \tag{1}$$

Where i_{L1} is the peak value of the fundamental component and i_{Ln} is the peak value of the harmonic component. ϕ_{L1} and ϕ_{Ln} are the phase angles of the fundamental and the harmonic components. Fig. 1 shows the circuit for shunt APF. Voltage source v represents the instantaneous supply voltage at the PCC with i_s as its instantaneous supply current. The injection current of the shunt active filter is denoted by i_{inj}. The first order low-pass filter in series with the VSI output is represented by inductor L_{sh} with resistor R_{sh} as the inverter losses. $V_{dc}/2$ denotes the voltage of each capacitor unit.

In (1) above, the instantaneous current of the nonlinear load is expanded into 3 terms. The first term is the load instantaneous fundamental phase current $i_{L1,p}$ which is always in phase with the supply voltage. The second term $i_{L1,p}$ is the load instantaneous fundamental quadrature current which is always 90° out of phase with the supply voltage. The third term i_{Ln} is the load instantaneous harmonic currents. From Fig. 1, it can be shown that

$$i_s + i_{inj} = i_{L1,p} + i_{L1,q} + i_{Ln} \tag{2}$$

In order to have i_s that is almost in phase with v and at the same time consists only of the fundamental component, from (2)

$$i_{inj} = i_{L1,q} + i_{Ln} \tag{3}$$

The dc voltage of each capacitor $V_{dc}/2$ is also measured and passed to the self-charging circuit to regulate to its reference voltage level $V_{dc}^*/2$. The output signal from the self-charging circuit i_{dc} together with $i_{L1,q}$ and i_{Ln} will form the reference injection current of the adaptive shunt active filter i_{inj}^*.

B. Adaptive VLLMS based Fundamental Active Component Extraction

Here a VLLMS algorithm is used for extraction of fundamental active component of current from load current. For that, signal can be modelled as

$$y(t) = \sum_{n=1}^{N} A_n \sin(n\omega t + \phi_n)$$

$$y(k) = \sum_{n=1}^{N} [A_n \sin(n\omega kT)\cos\phi_n + A_n \cos(n\omega kT)\sin\phi_n] \tag{4}$$

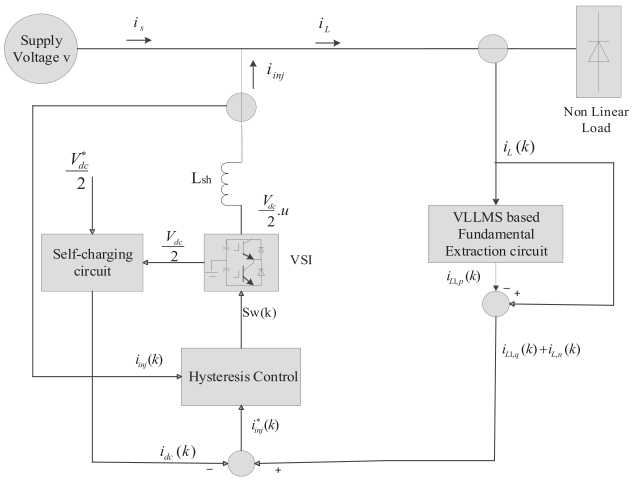


Fig. 1. System block diagram of single-phase adaptive shunt active filter.

(4) can be rewritten in parametric form as follows

$$y(k) = H(k)X \tag{5}$$

$$H(k) = [\sin(\omega kT)\ \cos(\omega kT)\ \ldots\ \sin(n\omega kT)\ \cos(n\omega kT)] \tag{6}$$

The vector of unknown parameter

$$X = [A_1\cos(\phi_1)\ \ A_1\sin(\phi_1)\ \ \ldots\ A_n\cos(\phi_n)\ \ A_n\sin(\phi_n)]^T \tag{7}$$

The VLLMS algorithm is applied to estimate the state. The algorithm minimizes the square of the error recursively by altering the unknown parameter X_k at each sampling instant using (8) given below

$$\hat{X}_{k+1} = (1 - 2\mu_k\gamma_k)\hat{X}_k + 2\mu_k e_k \hat{y}_k$$
$$\hat{y}_k = H(k)\hat{X}_k \tag{8}$$

where the error signal is

$$e_k = y_k - \hat{y}_k \tag{9}$$

Step size μ_k is varied for better convergence of the VLLMS algorithm in the presence of noise.

$$\mu_{k+1} = \lambda\mu_k + \gamma_k R_k^2 \tag{10}$$

where R_k represents the autocorrelation of e_k and e_{k-1}. It is computed as

$$R_k = \beta R_{k-1} + (1-\beta)e_k e_{k-1} \tag{11}$$

where β is an exponential weighting parameter and $0 < \beta < 1$, and $\lambda (0 < \lambda < 1)$ and $\gamma > 0$ control the convergence time.
The variable leakage factor γ_k can be adjusted as

$$\gamma_{k+1} = \gamma_k - 2\mu_k\rho e_k \hat{y}_k X_{k-1} \tag{12}$$

After the updating of the vector of unknown parameter using VLLMS algorithm,

$$i_{L1,p} = X_1 H_{11} \tag{13}$$

As seen from Fig. 1, the current output of the VLLMS based fundamental extraction circuit is subtracted from the load current. The subtracted output serves as a major component in reference current generation. Fig. 2 shows the flow chart of the active component of fundamental current extraction scheme using VLLMS algorithm.

C. DC Capacitor Self Charging Circuit

To regulate the dc capacitor voltage at the desired level, an additional real power has to be drawn by the adaptive shunt active filter from the supply side to charge the two capacitors. The energy E stored in each capacitor can be represented as

$$E = \frac{1}{2} C \left(\frac{V_{dc}}{2} \right)^2 \tag{14}$$

If the value of the dc capacitor voltage changes from V_{dc} to $V_{dc}^{'}$ the change in energy is represented by

$$\Delta E = \frac{1}{2} C \left[\left(\frac{V_{dc}^{'}}{2} \right)^2 - \left(\frac{V_{dc}}{2} \right)^2 \right] \tag{15}$$

The charging energy delivered by the three-phase supply side to the inverter for each capacitor will be

$$\begin{aligned} E_{ac} &= 3Pt \\ &= 3(V_{rms} I_{dc\,rms} \cos\phi)t \end{aligned}$$

P: additional real power required
t: charging time
V_{rms}: value of instantaneous supply voltage v
$I_{dc\text{-}rms}$: value of the instantaneous charging current i_{dc}
ϕ: phase difference between supply voltage and charging current

$$E_{ac} = 3 \frac{V}{\sqrt{2}} \frac{I_{dc}}{\sqrt{2}} \frac{T}{2} = \frac{3VI_{dc}T}{4} \tag{16}$$

Neglecting the switching losses in the inverter and according to the energy conservation law, the following equation holds from (15) and (16).

$$\Delta E = E_{ac}$$

$$\frac{1}{2} C \left[\left(\frac{V_{dc}^{'}}{2} \right)^2 - \left(\frac{V_{dc}}{2} \right)^2 \right] = \frac{3VI_{dc}T}{4} \tag{17}$$

$$I_{dc} = \frac{2C \left[\left(\frac{V_{dc}^{'}}{2} \right)^2 - \left(\frac{V_{dc}}{2} \right)^2 \right]}{3VT}$$

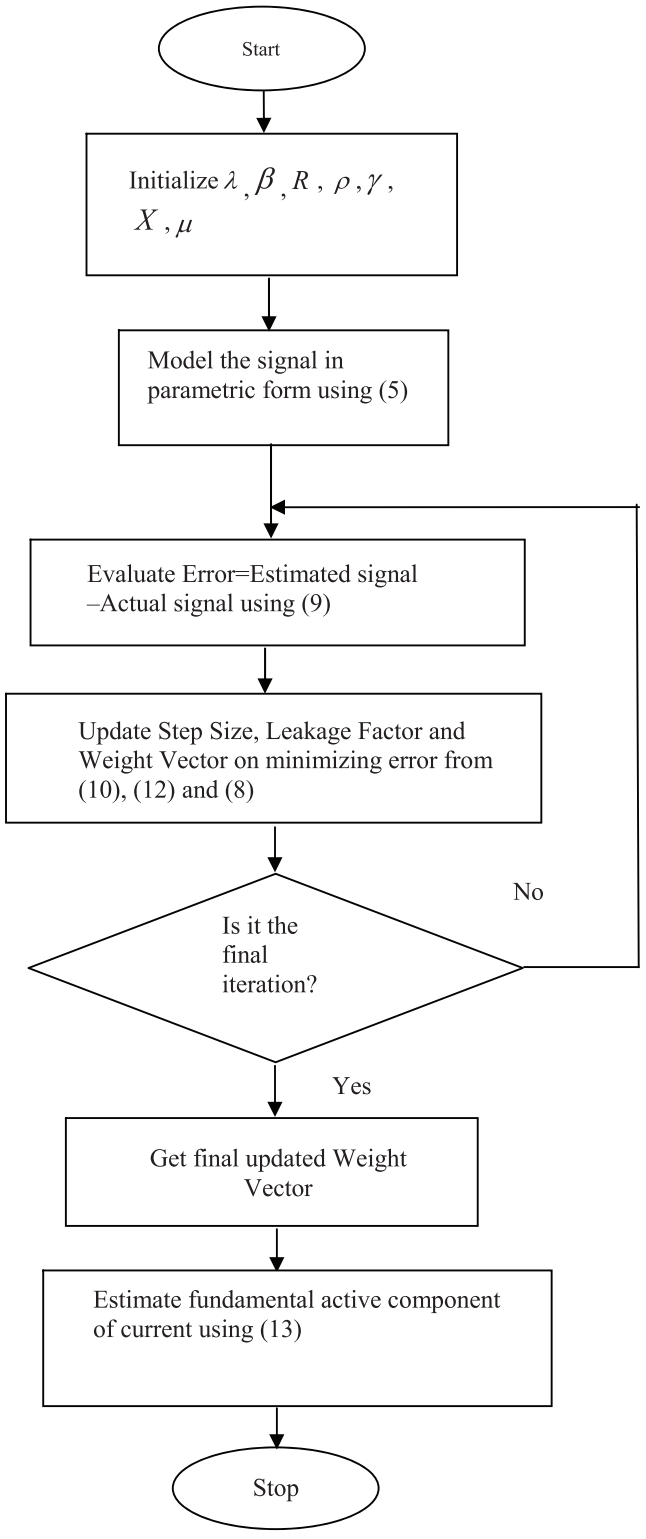


Fig. 2. Flow chart of the active fundamental current extraction scheme of VLLMS algorithm.

To maintain the value of each dc capacitor voltage at the reference level $V_{dc}^{*}/2$, $V_{dc}/2$ is measured and fed back to a PI controller as shown in Fig. 3 to manipulate $V_{dc}^{'}/2$. So that it can be used in (17) to compute the required peak value of the charging current I_{dc} from the supply side. The PI controller also helps in reducing

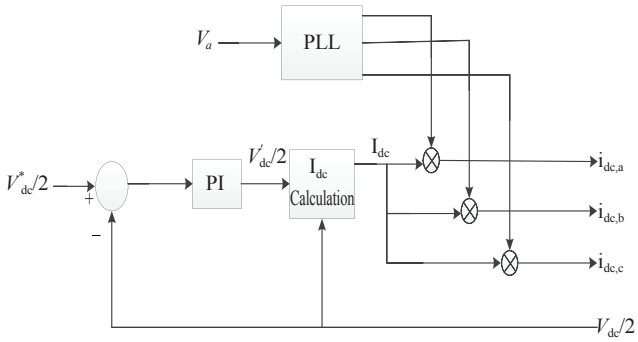


Fig. 3. Three phase self-charging circuit with PI controller.

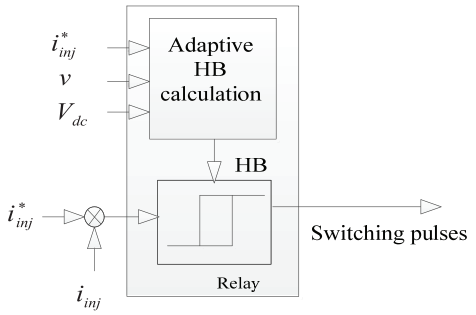


Fig. 4. Adaptive hysteresis band current controller.

the steady state offset between the reference $V^*_{dc}/2$ and the actual $V_{dc}/2$. The PLL synchronizes itself with the supply voltage of phase a i.e v_a and gives three output sinewaves which are 120° out of phase with each other. These sine waves are multiplied with I_{dc} to obtain three phase i_{dc}. In order to force the supply side to deliver i_{dc}, a term consisting of this i_{dc} is added to the three phase injection currents i_{inj} that can be represented by

$$\begin{aligned} i_{inj,a} &= i_{L1,qa} + i_{Ln,a} - I_{dc}\sin\omega t \\ i_{inj,b} &= i_{L1,qb} + i_{Ln,b} - I_{dc}\sin(\omega t - 120^\circ) \\ i_{inj,c} &= i_{L1,qc} + i_{Ln,c} - I_{dc}\sin(\omega t + 120^\circ) \end{aligned} \tag{18}$$

Fig. 3 shows the schematic of three phase self-charging circuit with PI controller. The negative sign indicates the flow of charging current into the VSI. For each phase it lags by an angle of 120°. The reference currents calculated shows that the adaptive shunt APF injects i_{Ln} and $i_{L1,q}$ into the line to compensate the harmonic currents and the reactive power respectively, and at the same time it receives the charging current i_{dc} from the supply to regulate the dc capacitor voltage.

An inductor which acts a low pass filter is connected in between the filter and the PCC to eliminate the higher order harmonics. The compensating signals along with the original injecting currents are given to a adaptive hysteresis current controller to generate the switching pulses for the IGBTs or switches in the inverter to produce the required currents.

D. Adaptive Hysteresis Current Controller

Adaptive hysteresis control has been used in this paper to actualize (18) at the output of VSI. The mathematical expression derived in (18) has been used as the reference signal i^*_{inj} for the adaptive hysteresis control. The injected current i_{inj} at the output of VSI is measured and fed back to the adaptive hysteresis control as it's another input. The adaptive hysteresis control will take the difference between i^*_{inj} and i_{inj} as given by

$$\Delta i_{inj} = i^*_{inj} - i_{inj} \tag{19}$$

Taking into account the value of Δi_{inj}, the adaptive hysteresis control will switch the IGBT of VSI as per the expression given in (20).

$$Sw = adaptive\ hys(\Delta i_{inj}) = \begin{cases} 1\ if\ \Delta i_{inj} > HB \\ 0\ if\ \Delta i_{inj} < -HB \end{cases} \tag{20}$$

Where *HB* is the hysteresis band and *Sw* is the status of the IGBT, "1" represents on and "0" represents off. The value of "*u*" shown in Fig. 1 will be "1" if *Sw* = "1" and "-1" if *Sw* = "0".

In hysteresis band current control, it has a fixed hysteresis band due to which the switching frequency is not constant, are uneven in nature. Due to this uneven switching frequency acoustic noise is produced. To overcome these drawbacks, an Adaptive Hysteresis Band Current Control technique has been used which adaptively changes the hysteresis band according to system parameters such as reference source current, source voltage, switching frequency and dc capacitor voltage, so that the switching frequency is maintained almost constant. The hysteresis band [18] can be calculated according to the following equation.

$$HB = \frac{0.125V_{dc}}{f_c L}\left[1 - \frac{4L^2}{V_{dc}^2}\left(\frac{v}{L} + m\right)^2\right] \tag{21}$$

Where, f_c is modulation frequency, $m = \dfrac{di^*_{inj}}{dt}$ is the slope of the command current wave and v is the supply voltage.

In adaptive hysteresis band current controller, since modulation frequency f_c, almost remains constant, this improves the PWM performances and APF substantially. Calculated hysteresis band using above (21), is applied to hysteresis band current controller as shown in Fig. 4 for switching pulse generation to be fed back to inverter.

III. Simulation Studies

Various simulations at different power system conditions have been carried out with the proposed VLLMS based controller. Simulations have been done using power system block set under MATLAB/Simulink environment.

A. Simulation Results With Three Phase Nonlinear Load

The performance of the system with non-linear load has been analysed by simulating the shunt APF filtering using both the

TABLE I
SYSTEM PARAMETERS

System Parameter	Value
Voltage	220 V
Frequency	50 Hz
L_s	3.5 mH
R_s	0.01
R_{load}	10 ohms
L_{load}	10 mH
R_f	1 ohm
L_f	0.3 mH

control strategies. The system data on which the simulation has been carried out is shown in the TABLE I.

The MATLAB /Simulink results are presented in Fig. 5. Fig. 5(a) shows the source current of phase-a without any compensation. The THD of this current as shown in Fig. 5(b) is 17.93%, which exceeds the IEEE standards. The source current of phase-a after compensation using proposed controller is shown in Fig. 5(c). The harmonics are reduced and the source current is almost sinusoidal. The THD of the source current has been reduced to very low value which is permissible (2.84%) and the harmonic analysis of the current is shown in Fig. 5(d).

The voltage of the DC side capacitor is maintained constant using a self-charging circuit in the VLLMS based current decomposer. The voltage of the single capacitor on the DC side is shown in the Fig. 6.

B. Simulation Results With Combination of Non-Linear Load and Unbalanced Linear Load

For another performance comparison simulation for combination of non-linear load and unbalanced linear load has been carried out. The phase-a source current before compensation is shown in the Fig. 7(a) and the harmonic analysis is shown in the Fig. 7(b). The THD of source current before compensation for the combination of loads is 14.23%.

The simulation is done using proposed VLLMS based controller and phase a source current after compensation is shown in Fig. 7(c) and the harmonic analysis of the phase a current is shown in the Fig. 7(d). DC Side capacitor voltage is shown in Fig. 7(e).

C. Simulation Results With Unbalanced Linear Load

To analyze the system performance, another condition has been taken into consideration. Linear load with unbalanced nature is connected to the source. The unbalanced load current is shown here in Fig. 8(a), whereas after compensation with the proposed technique it becomes more sinusoidal as shown in Fig. 8(b). Spectral analysis of load current is found to be 20.93% from Fig. 8(c) and with the proposed method, the THD has been reduced to 2.21% clearly shown in Fig. 8(d). Simulation parameter for this condition has been presented in TABLE II.

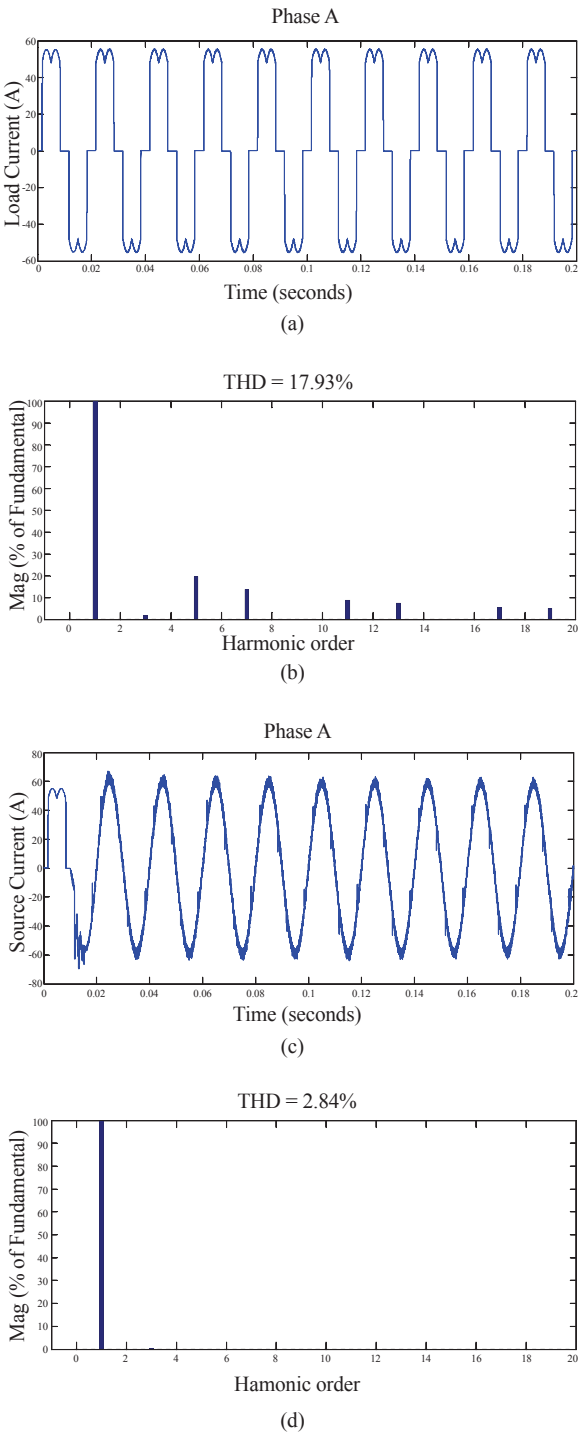


Fig. 5. (a) Phase-a source current before compensation, (b) Harmonic analysis of phase-a source current before compensation, (c) Phase-a source current after compensation using proposed controller, (d) Harmonic analysis of phase-a source current after compensation.

D. Simulation Results With Balanced Highly Inductive Load

This condition is very much essential to test the effectiveness of the proposed method. In this condition balanced and highly inductive loads are connected to the source. Parameters considered for this simulation are shown in TABLE III. Inductive load current

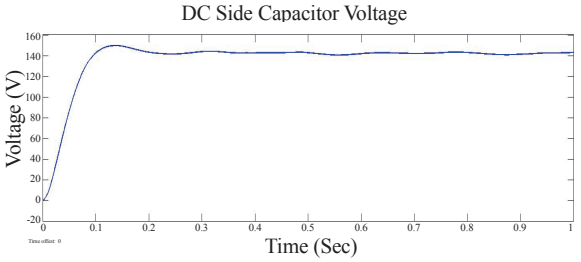


Fig. 6. Voltage of DC side capacitor in VLLMS based decomposer.

TABLE II
FILTER AND LOAD PARAMETERS FOR UNBALANCED CASE

Parameter	Value
Unbalanced load resistance (R_{labc})	10 ohms, 20 ohms, 30 ohms
Unbalanced load inductance (L_{labc})	0.2 H, 0.5 H, 0.65 H
R_f	1 ohm
L_f	0.3 mH

TABLE III
FILTER AND LOAD PARAMETERS FOR HIGHLY INDUCTIVE LOAD

Parameter	Value
Load resistance (R_{labc})	20 ohms, 20 ohms, 20 ohms
Load inductance (L_{labc})	10 H, 10 H, 10 H
R_f	1 ohm
L_f	0.3 mH

obtained from the simulation has been shown in Fig. 9(a), after compensation with the application of VLLMS decomposer control algorithm the source current become sinusoidal as shown in Fig. 9(b). From the spectrum analysis the harmonic content can be known, THD of the load current is 30.50% as per Fig. 9(c) which has been reduced to 2.61% for VLLMS decomposer control algorithm as shown in Fig. 9(d).

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The real validation of the proposed scheme has been verified by hardware experiment performed in the laboratory. DS1103 controller board has been used which is compatible with MATLAB to control the experimental setup, the controller has been developed in MATLAB/dSPACE interactive platform. The PWM signal generated from the control board are passed through the driver circuit which is fed to the inverter. The experimental setup developed in the laboratory includes voltage and current sensor boards, driver circuit, inverters. The hardware setup block diagram is shown in Fig. 10. Single phase shunt active power filter is connected in to the distributed system at the load end. The experiment is conducted in the following steps, first the source is feeding the load without the power conditioner connected to the system and the nonlinear load current is sensed which is highly rich in harmonics.

The shunt APF with the proposed control scheme has been designed and implemented. Various cases have been considered

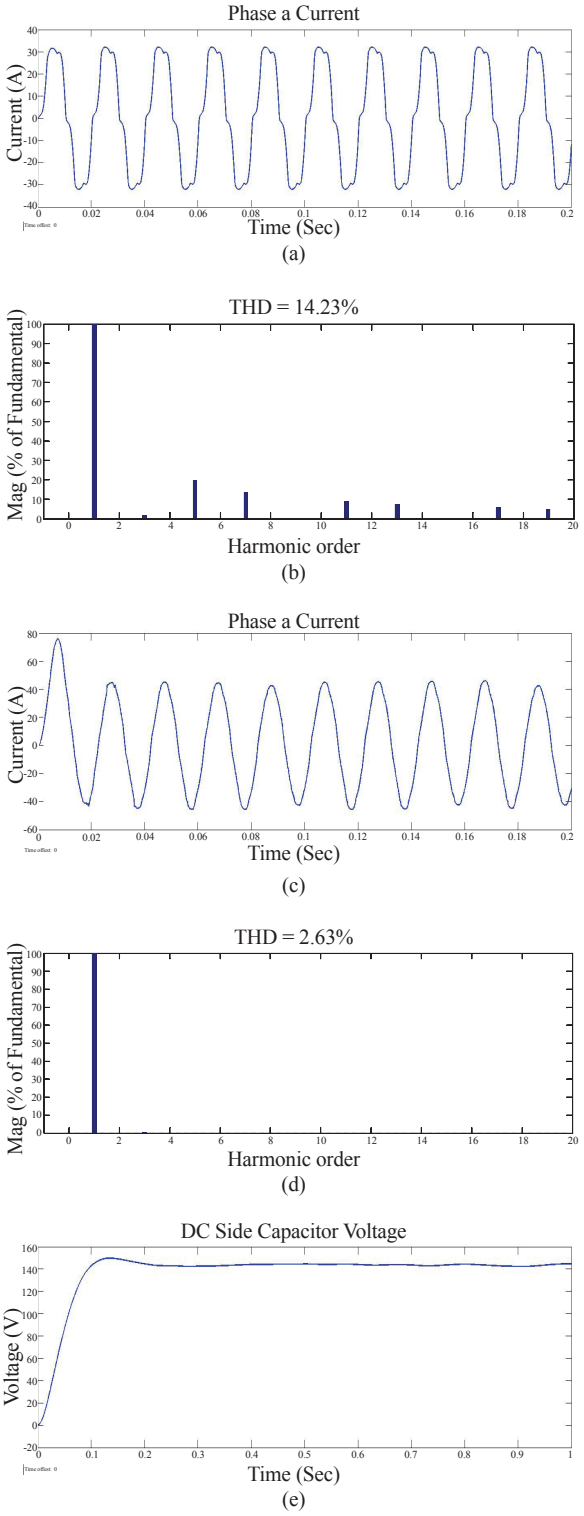


Fig. 7. (a) Phase-a source current before compensation for combination of load, (b) Harmonic analysis of the phase-a source current before compensation for combination of load, (c) Phase-a source current after compensation for combination of load using VLLMS based controller, (d) Harmonic analysis of phase-a source current after compensation for combination of load using VLLMS based controller, (e) DC side capacitor voltage after combination of load using VLLMS decomposer.

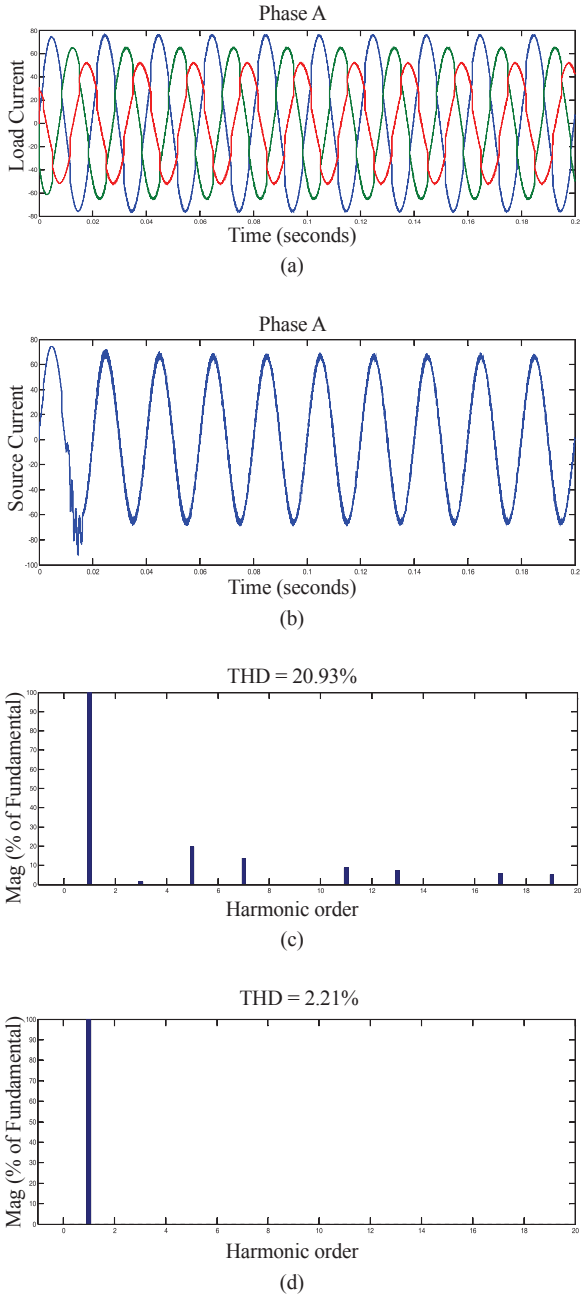


Fig. 8. (a)Unbalanced load current, (b) Phase-a source current after compensation after combination of load using VLLMS decomposer, (c) Harmonic analysis for load current, (d) Analysis for source current with VLLMS decomposer.

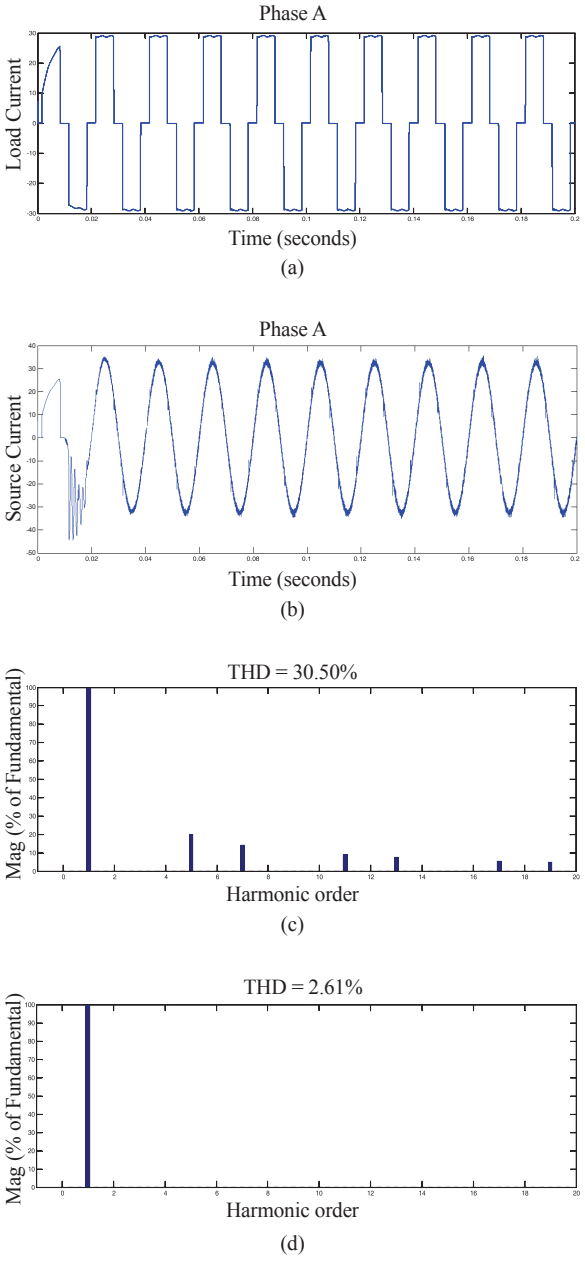


Fig. 9. (a) Balanced load current, (b) Phase-a source current after compensation after combination of load using VLLMS decomposer, (c) Harmonic analysis for load current, (d) Harmonic analysis for source current with VLLMS decomposer.

for the validation of the simulation work. The experimental parameters are listed in the TABLE IV.

A. Performance of Shunt APF based on VLLMS with Nonlinear Load

The three phase source is connected to the nonlinear load, which injects harmonics to the distribution system. The harmonic rich load current is measured and presented in Fig. 11(a). The VLLMS algorithm is applied for the compensation of load harmonics. The source current after compensation is presented in Fig. 11(b). The THDs before and after compensation have been given in Fig. 11(c) and Fig. 11(d) respectively.

B. Performance of Shunt APF Based on VLLMS Under Nonlinear Load and Unbalance Linear Load

The source is feeding a combination of linear and nonlinear load, where the linear load considered is unbalanced in this case. The measured load current is presented in Fig. 12(a) with nonlinear load and unbalance linear load. The shunt APF with VLLMS is employed for compensation, where the source current is compensated as shown in Fig. 12(b).

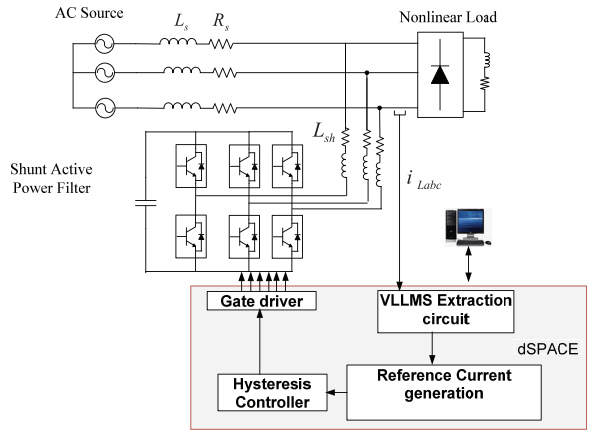
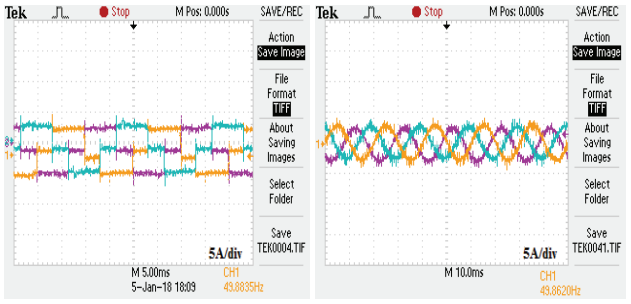


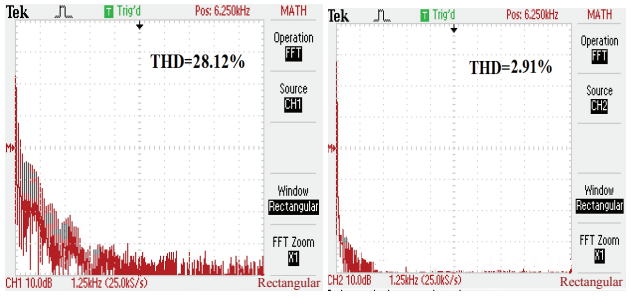
Fig. 10. Block diagram of experimental prototype compensation.

TABLE IV
SYSTEM PARAMETER FOR EXPERIMENTAL SETUP

System Voltage	110 V
Frequency	50 Hz
Non linear load	30 Ω, 50 mH
Unbalance Load	30 Ω, 50 mH 20 Ω, 40 mH 25 Ω, 30 mH
Coupling inductance source	0.2 Ω, 0.05 mH
Interfacing inductance shunt APF	0.02 Ω, 0.003 mH
DC link capacitor	2100 μF
Switching frequency	10 kHz

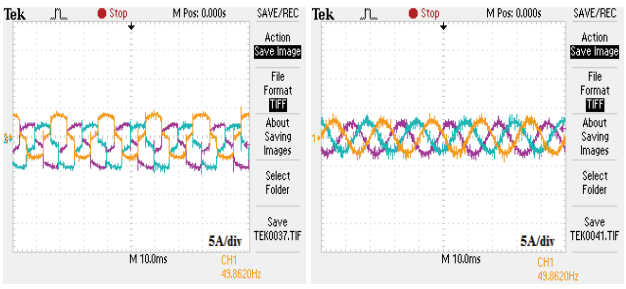


(a) (b)



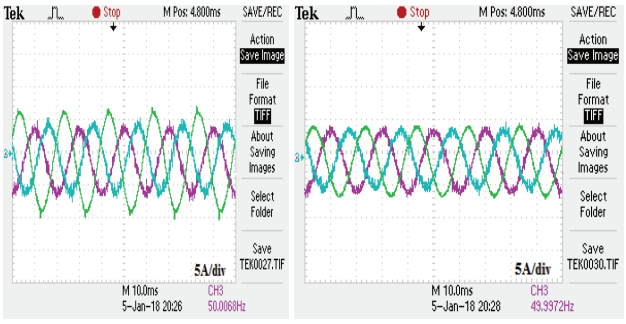
(c) (d)

Fig.11. Nonlinear load case (a) Load current, (b) Source current after compensation, (c) THD before compensation of load current, (d) THD after compensation source current.



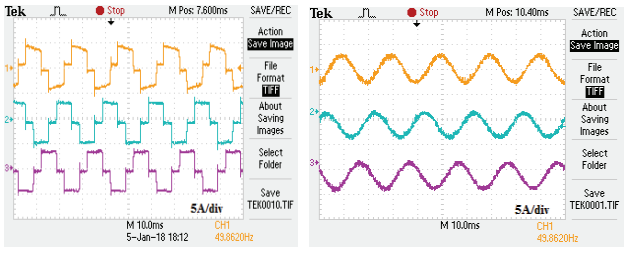
(a) (b)

Fig.12. Nonlinear load and unbalance linear load case (a) Load current, (b) Source current after compensation.



(a) (b)

Fig.13. Unbalance linear load case (a) Load current, (b) Source current after compensation.



(a) (b)

Fig.14. Highly inductive load case (a) Load current, (b) Source current after compensation.

C. Performance of Shunt APF Based on VLLMS Under Unbalance Linear Load

In this case, an unbalanced linear load has been connected to the main grid. The sensed load current is shown in Fig. 13(a). After compensation by Shunt APF with VLLMS, the compensated source current is shown in Fig. 13(b).

D. Performance of Shunt APF Based on VLLMS Under Highly Inductive Load Case

A highly inductive nonlinear load has been connected to the main grid where the load current is sensed and presented in Fig. 14(a). The highly inductive load current is rich in harmonics which need to be eliminated. The shunt APF with the proposed method is employed for the compensation of the harmonics and to

maintain the source current as sinusoidal. The source current after compensation is presented in Fig. 14(b).

V. Conclusions

In this paper, a new control design for the shunt active power filter has been presented. The controller design is based on VLLMS based algorithm for fundamental current extraction. With the use of this proposed algorithm, the performance of shunt active filter has been enhanced. The proposed shunt active power filter compensates balanced and unbalanced nonlinear load currents. Self-charging capability has also been integrated into the proposed shunt active power filter for regulating the dc capacitor voltage. Simulation and experimental results under various system operating conditions have verified the effectiveness and robustness of the proposed adaptive shunt active filter.

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On-State Voltage Measurement of Fast Switching Power Semiconductors

Mattia Guacci, Dominik Bortis, and Johann W. Kolar

***Abstract*—The on-state resistance $R_{ds,on}$ is a key characteristic of unipolar power semiconductors and its value depends on the operating conditions, e.g. junction temperature, conducted current and applied gate voltage. Hence, the exact determination of the $R_{ds,on}$ value cannot rely on datasheet information and requires the measurement of current and on-state voltage during operation. Besides the determination of the conduction losses, the on-state voltage measurement enables dynamic $R_{ds,on}$ analysis, device temperature estimation, condition monitoring and consequently time-to-failure prediction. However, in contrast to a switch current measurement, several challenges arise in the design of an on-state voltage measurement circuit (OVMC), i.e. high measurement accuracy (mV-range) during on-state, high blocking voltage capability (kV-range) during off-state and fast dynamic response (ns-range) during switching transitions are demanded. Different OVMC concepts are known from IGBT applications, however, the more severe requirements introduced from the high switching frequency and low OV characterizing the operation of fast switching power semiconductors, prevent their usage. Off-the-shelf products hardly satisfy the mentioned specifications, whereas the performance of state-of-the-art OVM research prototypes require further investigations and/or improvements. With this aim, an innovative OVMC concept is designed, analyzed, calibrated and tested in this paper. Furthermore, the conduction losses of different power semiconductors are measured as function of their operating conditions to validate the performance and highlight the potential of the proposed OVMC.**

***Index Terms*—Conduction loss measurement, on-state resistance, on-state voltage measurement circuit.**

I. Introduction

TODAY, the detailed experimental analysis of a power converter circuit is typically focused on the switching behavior of the power semiconductors, e.g. switching overvoltages and voltage oscillations occurring in hard-switching [1] and/or switching voltage and current time displacement relative to zero-voltage switching (ZVS) [2]. However, with the increasing switching speed enabled by wide bandgap devices and/or with employing ZVS concepts, the loss contribution of the semiconductors is more and more dominated by the conduction losses.

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The power converter operating conditions are significantly influencing the occurring conduction losses. Junction temperature, conducted current, applied gate voltage, switching frequency, manufacturing variability and aging take, in fact, a combined impact on the instantaneous value of the semiconductors on-state resistance $R_{ds,on}$. Despite this premise and contrary to switching loss analysis, no on-state behavior analysis and/or no experimental verification of the calculated $R_{ds;on}$ value is typically carried. Hence, worst-case approximations, based on datasheet information, are inferred to estimate the conduction losses. Performing online $R_{ds,on}$ measurements would allow to accurately verify conduction loss calculations and hence to improve optimization procedures for the design of power converters [3], [4]. In order to achieve this, the voltage across and the current through the device-under-test (DUT) have to be measured accurately and simultaneously. Several solutions are suitable to obtain the DUT current, i.e. it can be directly measured (e.g. with a series connected current shunt) or indirectly derived from the load current and the gate signals, both available for control purposes. In contrast, the usage of conventional voltage probes to accurately measure the DUT on-state voltage (OV) is prevented from the resulting dynamic range, i.e. the ratio between the maximum voltage (during off-state) and the minimum voltage (during on-state) applied at the input of the measurement circuit. The extreme required dynamic range limits the measurement resolution. This can be understood considering an example. If a conventional 12-bit oscilloscope is set to capture the voltage blocked (e.g. 1000 V) from a specimen power MOSFET (e.g. $R_{ds,on}$= 25 mΩ), the least significant bit, i.e. the measurement resolution, corresponds to $1000\ V/2^{12} \approx 250$ mV. This voltage is already half the OV of the mentioned MOSFET conducting 20 A (25 mΩ · 20 A = 500 mV) and the resulting accuracy is definitely insufficient. Ideally, in order to perform this measurement with an accuracy of 1%, the least significant bit should correspond to 5 mV (0.01 · 500 mV); in other words, an 18-bit oscilloscope ($1000\ V/2^{18} \approx 4$ mV) would be required [5]. Alternatively, the conventional oscilloscope full-scale voltage would have to be limited to 20 V ($20\ V/2^{12} \approx 5$ mV). The full-scale voltage reduces to 1 V if the same accuracy is desired while measuring only 1 A (25 mΩ · 1 A = 25 mV, 0.01 · 25 mV = 0.25 mV and 0.25 mV · 2^{12} = 1 V). However, if the oscilloscope range is limited to measure the sole OV (e.g. 1 V), the overdrive of the oscilloscope amplifiers caused by the voltage blocked in off-state significantly distorts the measurements and could damage the instrument.

It results clear that the achievable accuracy is insufficient because of the trade-off with the excessive dynamic range. Therefore, only dedicated on-state voltage measurement cir-

cuits (OVMCs), limiting the voltage during off-state to values within the oscilloscope input voltage range, allow accurate measurements during on-state. For example, a full-scale voltage of 10 V guarantees a measurement resolution of 10 V/$2^{12} \approx 2.5$ mV, sufficient in most cases.

Beside accuracy and resolution, also the bandwidth of OVMCs is of importance, since modern Gallium-Nitride (GaN) semiconductors often present dynamic $R_{ds,on}$ effects [6], [7], i.e. a high initial (i.e. immediately after a turn-on switching transition) $R_{ds,on}$ value which slowly (i.e. with time constants varying in the µs-range) settles to a constant value. In order to characterize this phenomenon, OVMCs should measure the correct OV immediately after the turn-on transition of the DUT. The dynamic $R_{ds,on}$ is a fundamental figure-of-merit in the evaluation of GaN semiconductors and it depends on the voltage blocked during off-state, as well as on the switching frequency [7]-[9]. Being this information not specified in the datasheet, the importance of the experimental on-state behavior analysis is remarked.

In addition to dynamic and stationary OV analysis, other application areas are envisaged in literature, resulting in requirements of an ideal OVMC. The OV is a promising temperature sensitive electrical parameter, i.e. a circuit parameter ensuring high sensitivity and good linearity with respect to temperature variations [10]. Measuring the OV offers the potential for replacing conventional temperature measurements in application with severe volume constraints. Furthermore, the OV is identified as a favorable aging indicator. E.g. in power modules, a crack in the metallization layer and/or the lift-off of a bond-wire cause an increase of the $R_{ds,on}$ value, i.e. of the OV [11], [12]. This establishes a positive feedback mechanism accelerating the aging process. Monitoring the OV allows a detection of the failure and potentially time-to-failure predictions, advantageous e.g. in reliability critical or remote applications. Accordingly, a trend towards intelligent gate drivers integrating OVMCs is traced [13] and, to facilitate this, compactness is generally demanded. As well the mentioned bandwidth requirement, associated to a fast dynamic response of the OVMC after a switching transition, is of importance in all the foreseen application areas, if fast switching semiconductors are considered.

Finally, the online measurement of conduction losses enabled by OVMCs can significantly improve the measurement accuracy of calorimetric switching loss measurement methods [14]-[16]. This application is commented in detail in Section IV-C, since it constitutes a main reason for this research work. Summarizing, high accuracy, fast dynamic response, low complexity, and high compactness are the desirable characteristics of OVMCs.

The nowadays most common OVM approaches can be traced back more than thirty years [17], [18]. Recently, the increased interest of the power electronic community in wide bandgap semiconductors, combining reduced $R_{ds,on}$ values with increased switching speeds, motivated the interest to derive solutions offering better accuracy and higher bandwidth, e.g. [19] and [20], where also a comprehensive

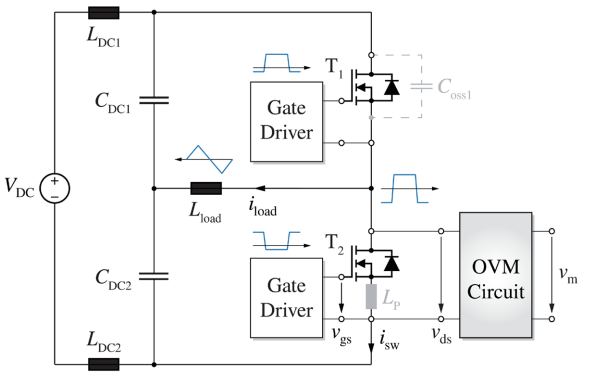

Fig. 1. Power converter setup considered as reference for the overall analysis. The two power semiconductors in half-bridge configuration T_1 and T_2 are operated with complementary 50% duty cycles. The output inductor L_{load} tapped to the split DC link capacitors C_{DC1} and C_{DC2} ensures symmetric triangular current mode (TCM) operation (blue waveforms). The parasitic inductance L_p and parasitic output capacitance of T_1 (i.e. C_{oss1}) are as well shown. An OVMC (gray) is connected in parallel to the low-side semiconductor T_2, enabling online $R_{ds,on}$ measurements.

overview of the state-of-the-art is discussed. However, these concepts still reveal limited performance: [20] suffers significantly from noise and common-mode disturbances, and is tested only at high OV values, while [18] and [19] have an intrinsic accuracy limitation, i.e. an unknown diode forward voltage drop in the OVM path, as discussed in Section II. A solution to the latter issue is proposed in [12], where a novel OVMC is presented to monitor the wear-out of high power IGBT in power modules. Unfortunately, the performance of this OVMC highlighted in [12], [21], [22] and the provided guidelines are insufficient and inadequate for fast switching power semiconductors, especially in terms of bandwidth and dynamic response. Significant distortions are introduced from this OVMC at its output for tens of µs and also the settling time of the designed analog circuitry itself is already in the range of 1 µs, i.e. comparable to a conduction period of a device operating with a switching frequency in the hundreds of kHz-range. Moreover, with respect to IGBTs, where the OV is rarely below 500 mV, when considering fast switching semiconductors with $R_{ds,on}$ values in the mΩ -range, it results significantly more challenging to guarantee the same OVM accuracy. Only limited information on the accuracy are provided in [12] and the performed OVMs are not completely validated with an alternative setup. Nevertheless, this OVMC is considered as a promising solution for the foreseen achievable accuracy enabled by the correction of the unknown diode forward voltage drop in the OVM path. Lately, also OVM probes became commercially available [23], [24], aiming to replace OVM integrated circuits [25]. A commercial solution is tested, but poor dynamic performance is experienced, as commented in Section III-D. Consequently, it results necessary to develop an OVMC able to satisfy all above-mentioned requirements in order to cover all applications.

The reference setup, supporting the analysis presented in this paper, is shown in Fig. 1. It highlights an OVMC (gray)

connected to the low-side power semiconductor (i.e. T_2, the DUT) of an half-bridge configuration. The same circuit could be connected to the high-side T_1, however, for simplicity, only the depicted solution is analyzed in the following. Different power semiconductors are then selected for T_2, enabling their comparison.

The proposed OVMC is presented in Section III, where the achieved accuracy and bandwidth are verified through measurements on a calibrated test-bench. Afterwards, the turnon behavior of different Silicon (Si), Silicon-Carbide (SiC) and Gallium-Nitride (GaN) power semiconductors is experimentally analyzed, validating the dynamic performance of this OVMC. The main challenges faced during the online measurement of conduction losses are commented in Section IV-A, anticipating the measurement results discussed in Section IV-B (conduction losses) and Section IV-C (switching losses). Conclusions are presented in Section V.

II. Conventonal On-State Voltage Measurement Circuits

The schematics depicted in Fig. 2 show the two most common implementations of OVMCs. They ideally perform as a shortcircuit (i.e. $v_{ds} \approx v_{1,a}$ and $v_{1,b}$) when the power transistor T_2 (i.e. DUT, see Fig. 1) is conducting (on-state) and as an open-circuit when it is blocking the DC-link voltage V_{DC} (offstate). As explained in the introduction, the accuracy of v_1 during on-state and the dynamic performance of the transition between the two states are the most important figures-of-merit of an OVMC. These two approaches are compared according to these criteria in the rest of this section. The final aim is to highlight their respective advantages in order to facilitate the design of a better performing solution.

The OVMC illustrated in Fig. 2(a) [18] is based on the MOSFET T_p. The gate of T_p is connected to a voltage source V_p and when T_p is in on-state, i.e. $V_p > v_{1,a} + V_{th,Tp}$, the measured voltage

$$v_{1,a} = \frac{R_1}{R_1 + R_{T_p}} v_{ds}. \tag{1}$$

$V_{th,Tp}$ and R_{Tp} are the threshold voltage and the on-state resistance of T_p, respectively. Typically $R_{Tp} \ll R_1$, therefore $v_{1,a} \approx v_{ds}$. Regarding the transition between the two states, two control strategies are possible:

- *active*: V_p is switched to 0V before T_2 is turned off and back to V_p after T_2 is completely turned on;
- *passive*: V_p is kept constant and T_p operates in its linear region during the off-state of T_2.

The active solution is intuitively effective but increases the complexity of this OVMC, e.g. logic and delay circuitry between the gate drivers of T_2 and T_p results necessary and introduces a blanking time. Therefore, the less intuitive passive solution is preferred and herein considered, however additional challenges need to be faced [20].

The OVMC of Fig. 2 (b) [17] is realized with the diode D_1 instead of the MOSFET T_p. When $v_{ds} < V_p - V_{fv,D1}$, D_1 conducts and

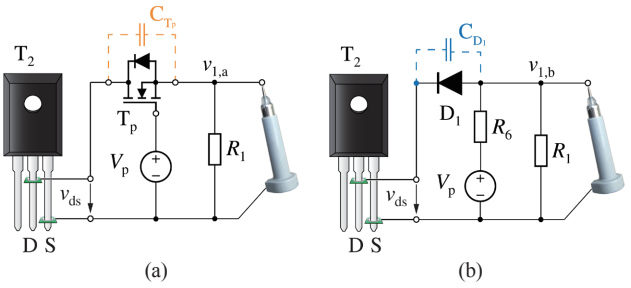

Fig. 2. Schematic representation of the two most common implementations of OVMCs. The input voltage v_{ds} is sensed at the DUT leads (see Fig. 1); by means of the MOSFET T_p (a) or of the diode D_1 (b), the output is decoupled during the DUT off-state and connected during its on-state. While the dynamic performance of (a) are affected from C_{Tp}, the accuracy of (b) is compromised by v_{D1}.

$$v_{1,b} = v_{ds} + v_{D_1}(T_{D_1}, i_{D_1}). \tag{2}$$

$V_{fv,D1}$, T_{D1} and i_{D1} are the forward voltage, the junction temperature and the current of D_1 respectively. During off-state, $v_{1,b}$ is fixed from V_p and D_1 naturally blocks V_{DC}. Differently from (1), a significant error term (i.e. v_{D1} in the range of hundreds of mV) appears in (2), causing an offset on $v_{1,b}$. As specified in (2), v_{D1} is function of T_{D1} and i_{D1} , however, an approximate value is commonly subtracted from $v_{1,b}$ to obtain v_{ds} [18], [19]. This only partially compensates it and compromises the accuracy of the measurement. Nevertheless, this OVMC is often preferred (e.g. in desaturation circuits) to the one previously described, giving lower importance to the achievable accuracy than to hardware complexity and dynamic performance. The latter aspect is the focus of the following paragraph.

The transition between the two DUT states, i.e. the commutation of the half-bridge (Fig. 1), implies charge and discharge of the parasitic output capacitances of T_1 and T_2 (i.e. C_{oss1} and C_{oss2} in Fig. 1) as well as of the input capacitance of the OVMCs. In fact, C_{T_p} (orange in Fig. 2(a)) and C_{D_1} (blue in Fig. 2(b)) are charged to V_{DC} when T_2 is in off-state while are discharged when T_2 is conducting. The charging/discharging network includes the resistor R_1 or R_6, whose range of suitable values is limited from the operation of the OVMCs (e.g. R_1 defines the off-state current in the MOSFET-based solution). Consequently, C_{T_p} and C_{D_1} should be minimized:

- compared to C_{oss} in order not to affect the switching transition of the half-bridge, i.e. slowing down the voltage slope of the switching node dv_{ds}/dt in soft-switching transitions or significantly increasing the capacitive energy dissipated in hard-switching transitions;
- accordingly minimizing the magnitude of the charging/discharging current spikes, potentially damaging measurement and/or supply circuitry;
- minimizing the time constant of the *RC*-network formed with R_1 or R_6, improving the dynamic performance of the OVMCs (cf. Section III-D).

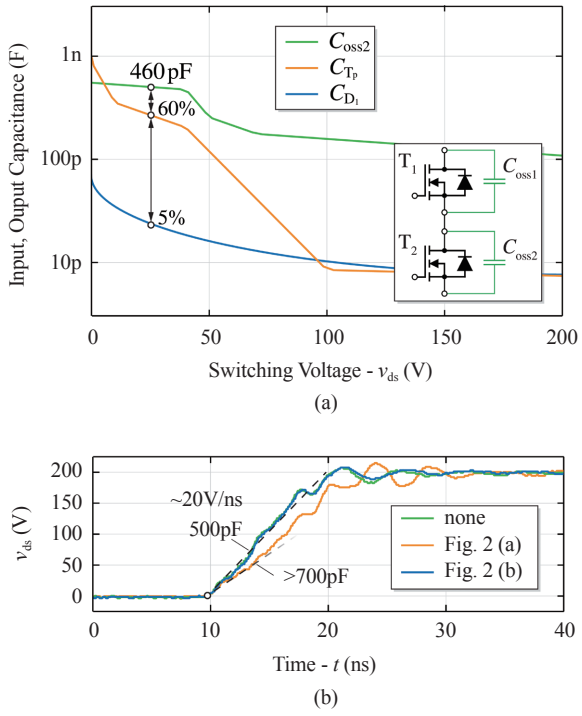

Fig. 3. (a) Comparison of the parasitic capacitances of the devices selected to realize the OVMCs of Fig. 2. For $v_{ds} < 100$ V, C_{D_1} is considerably smaller than C_{T_p} and, more important, negligible compared to C_{oss2}. This reflects on the switching behavior of the half-bridge (b): the presence of T_p, i.e. C_{T_p} (orange), significantly reduces dv_{ds}/dt during a soft-switching turn-off transition of T_2, whereas C_{D_1} (blue) does not have any influence.

These considerations clearly address the selection of T_p and D_1 towards devices featuring a small parasitic capacitance. Additionally, a low-inductance package and a short connection from the OVMC to the DUT are preferred in order to limit the voltage oscillations of v_1 inevitably excited from the switching transitions. According to these criteria, in the considered setups, a 800 V N-channel Si MOSFET [26] is selected for T_p as in [10] and a 600 V SiC Schottky diode [27] for D_1.

In order to prove the first statement, the parasitic capacitances of the selected devices are compared with the parasitic output capacitance C_{oss2} of a commercial 650 V E-mode GaN HEMT (Specimen C in TABLE II) as function of v_{ds} in Fig. 3(a). At $v_{ds} = 25$ V, C_{D_1} is a negligible fraction (i.e. 5%) of C_{oss2}, while C_{T_p} contributes to the overall capacitance (i.e. C_{oss2}+C_{T_p}) for more than 30%. As mentioned, this influences the switching behavior of the half-bridge where Specimen C is selected for T_2, e.g. in soft-switching operation. In Fig. 3 (b), measured waveforms of v_{ds} and dv_{ds}/dt for three different conditions are shown: without any OVMC (green), with the MOSFET-based approach (orange) and with the diode-based approach (blue) connected to T_2. While the presence of D_1 does not affect $dv_{ds}/dt \approx 20\ \frac{\text{V}}{\text{ns}}$, T_p slows it down especially in the first phase where C_{T_p} is comparable with C_{oss2}. This effect is clearly undesired and can be attributed to the selected T_p. However, depending on T_2, the range of suitable T_p (in terms of C_{T_p}) narrows, reaching a bottleneck in the case of interest of fast switching power semiconductors. Differently, parasitic capacitance of 600 V commercially available diodes can be in the range of few pF, enabling a more general OVM solution. Consequently, the approach presented in the next section is derived from the diode-based circuit. It aims to improve its accuracy, while benefiting from the reduced parasitic capacitance.

III. Proposed On-State Voltage Measurement Circuit

In Section II, strengths and weaknesses of the two most common OVM approaches are highlighted. In this section, a promising solution derived from the diode-based circuit and originally presented in [12], is analyzed in detail. As discussed in the introduction, it results significantly more challenging to perform OVMs in the case of fast-switching semiconductors compared to IGBTs, e.g. due to the higher switching frequency and lower OV. Considering the design guidelines proposed herein, relative in particular to the small input parasitic capacitance, the usage of a 50 Ω output stage, the high-bandwidth conditioning circuitry, the integrated generation of the supply voltages and the thoughtful design and calibration process, this OVMC is improved to combine high accuracy, outstanding dynamic performance and reduced circuit complexity. This ultimately enables its usage in the mentioned application areas of interest, as verified with the described measurement results. Initially, the operating principle of this OVMC is presented to better comprehend its possible limitations, providing the basis for its improvement.

A. Operating Principle

The schematic of the proposed OVMC for fast switching power semiconductors is depicted in Fig. 4(a) (a simplified version is in Fig. 4(c)) together with its hardware realization (Fig. 4(b)). The concept is derived from the approach shown in Fig. 2(b), but now two identical diodes (i.e. D_1 and D_2) are connected in series at the input. During the on-state of T_2 (see Fig. 2(c)), the same current i_D is assumed to flow through D_1 and D_2 ($i_{D_1} = i_{D_2}$), therefore, given the same operating point for the two diodes, the respective voltage drops v_D are assumed to be identical ($v_{D_1} = v_{D_2}$). Since thanks to the zener diode Z_1, only D_1 blocks V_{DC}, v_{D_2} can be measured and subtracted (with the operational amplifier Op_2) from v_1. Consequently, the offset v_{D_1} present in (2) can be, with this OVMC, exactly corrected rather than roughly compensated. During off-state, the operation is similar to the one of the OVMC in Fig. 2(b).

The transfer function of the complete OVMC (Fig. 4(a)) is herein derived. In the case of $v_{ds} < V_p - v_{D_2} - v_{D_1}$ and with Op_1 and Op_2 operating linearly (always assumed from here on),

$$\begin{cases} v_+ = \dfrac{R_{1b}}{R_{1a}+R_{1b}} v_1 \\ v_3 = \dfrac{R_{2b}}{R_{2a}+R_{2b}} v_2 \\ v_m = v_- - \dfrac{R_4}{R_3}(v_3 - v_-) \end{cases} \tag{3}$$

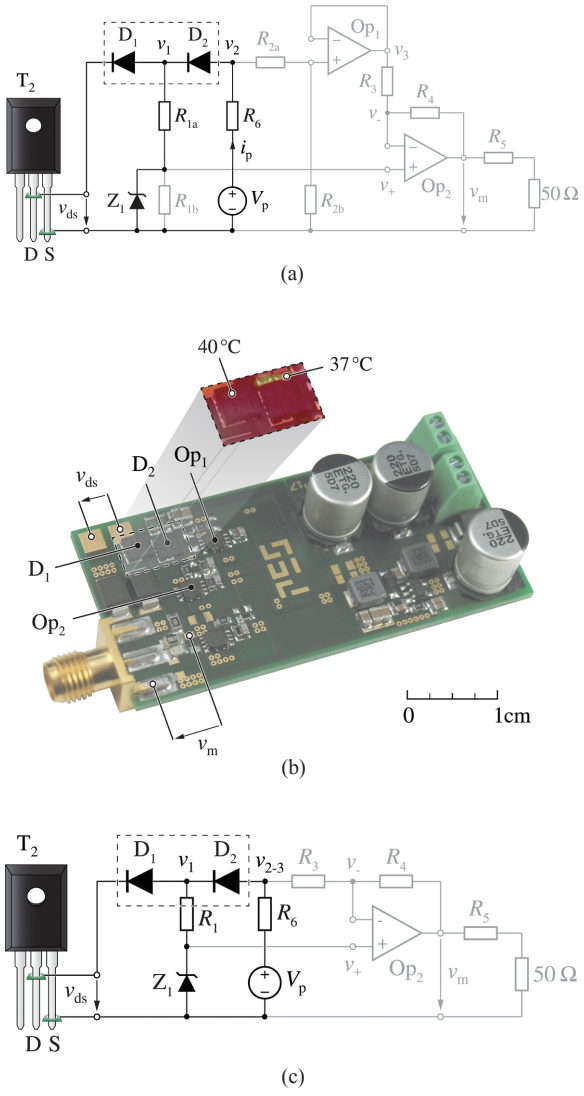

Fig. 4. Schematic representation of the realized (a) and simplified (c) versions of the proposed OVMC. (b) depicts the hardware realization of (a). D_1 and D_2 are thermally well coupled (dashed box) and electrically connected in series at the input of the OVMC in order to improve the measurement accuracy.

holds. The system of equations given in (3) can be solved for the output voltage v_m if $v_+ = v_-$ is assumed, obtaining

$$v_m \overset{(3)}{=} \frac{R_{1b}}{R_{1a}+R_{1b}}\left(1+\frac{R_4}{R_3}\right)v_1 - \frac{R_{2b}}{R_{2a}+R_{2b}}\frac{R_4}{R_3}v_2. \quad (4)$$

Defining $R_{1,b} = R_{2,b} \doteq R_\beta$ and $R_{1,a} = R_{2,a} \doteq \beta R_\beta$ so that

$$\frac{R_{1b}}{R_{1a}+R_{1b}} = \frac{R_{2b}}{R_{2a}+R_{2b}} = \frac{1}{1+\beta}$$

and selecting $R_3 = R_4$, (4) can be simplified to

$$v_m \overset{(4)}{=} \frac{1}{1+\beta}(2v_1 - v_2). \quad (5)$$

Finally, it must be noticed that the term

$$2v_1 - v_2 = v_1 - (v_2 - v_1) = v_1 - v_{D_2}, \quad (6)$$

under the assumption that $v_{D_2} = v_{D_1}$, can be used in (5) to obtain

$$v_m \overset{(6)}{=} \frac{1}{1+\beta}(v_1 - v_{D_1}) = \frac{1}{1+\beta}v_{ds}. \quad (7)$$

Hence, the proposed OVMC corrects the offset on v_1, i.e. v_{D1}, producing an output voltage v_m referred to the source potential of the DUT, exactly proportional to v_{ds} during its on-state.

In case the scaling of v_{ds} obtained by means of the voltage dividers formed by R_{1a}–R_{2a} and R_{1b}–R_{2b} is not needed, they can be bypassed (i.e. $R_{2,a}$= 0 Ω, $R_{1,b}$ and $R_{2,b}$ removed). Consequently Op_1 results unnecessary as well (Fig. 4(c)) and the system of equations given in (3) reduces to

$$v_m = v_1 - \frac{R_4}{R_3}(v_2 - v_1) \overset{(6)}{=} v_{ds}. \quad (8)$$

The degree of freedom given by β is lost, i.e. the input voltage range of the circuit is reduced, but the number of required components is halved.

To provide a better understanding of the proposed OVMC, additional considerations are herein reported to conclude the section. As in the diode-based circuit presented in Fig. 2(b), the values of V_p and R_6 fix the current in D_1 and D_2 during on-state. V_p = 10 V (Section III-B) and R_6 = 750 Ω (Section II) are selected. If the currents flowing in the voltage dividers formed by R_{1a}–R_{2a} and R_{1b}–R_{2b} are negligible (see Fig. 4(a)), the operating point of the OVMC when T_2 is in on-state is defined by

$$i_p = \frac{V_p - v_{D_2} - v_{D_1} - v_{ds}}{R_6}. \quad (9)$$

If v_{ds} = 0 V and $v_{D_1} = v_{D_2}$ = 1 V are assumed, $i_p \approx 10$ mA $\doteq I_{p,nom}$. Consequently, $P_{p,nom} = V_p I_{p,nom} \approx 100$ mW defines the power consumption of the OVMC from the main power source. It is important to limit i_p to a negligible fraction, e.g. 1%, of the current flowing through T_2 to avoid an increase and/or distortion of the OV (and to limit $P_{p,nom}$). This limit is strictly application dependent and, if exceeded, the additional OV should at least be considered in the calculation of $R_{ds,on}$. Moreover, a lower boundary of i_p is also set from the parasitic currents circulating in the OVMC, e.g. in the voltage divider formed by R_{1a}–R_{2a} and in the input of Op_2. If i_p is reduced below a certain threshold, it would result impossible to neglect them and the fundamental assumption $i_{D_1} = i_{D_2}$ would be violated, compromising the accuracy of the measurement. V_p defines as well, together with Z_1, the value of v_{ds} at which the circuit snaps. The blocking voltage of Z_1 is selected to be bigger than V_p to avoid its conduction during on-state of T_2, but on the other hand low enough to limit v_1 during off-state. Consequently the sole D_1 blocks the off-state voltage V_{DC}, protecting the measurement circuitry.

Finally, in order to facilitate the modular integration of the

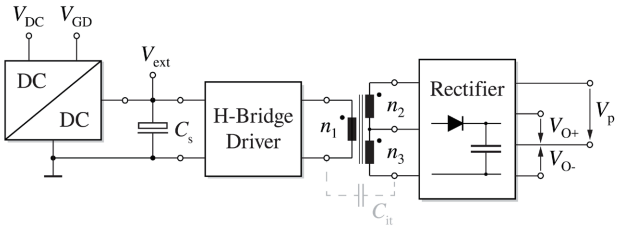

Fig. 5. Schematic representation of the OVMC supply circuitry. V_p, V_{O+} and V_{O-} can be generated from one of the supply voltages available in the power converter, e.g. V_{DC} and V_{GD}, facilitating the integration of the OVMC. Galvanic isolation is guaranteed and a small value of parasitic capacitance C_{it} ensures high common-mode rejection ratio.

OVMC in a power converter (e.g. towards intelligent gate drivers), Fig. 5 illustrates different options for the generation of the required supply voltages. In the proposed solution, V_p and the supply voltages of the operational amplifiers V_{O+} and $V_{O-} = -V_{O+}$ are galvanic isolated and generated from the gate driver supply voltage V_{GD}. A small value of parasitic capacitance C_{it} ensures high common-mode rejection ratio. Thanks to the isolated supplies, the proposed OVMC can be connected, without any additional precaution, as well to the high-side power semiconductor T_1 (Fig. 1). Hence, the OV of T_1 can be measured with respect to its source potential, i.e. v_{ds}. To avoid a differential measurement and common mode disturbances, it can be convenient to refer the OVM to a constant voltage, e.g. V_{DC}. To do so, the schematic of the proposed OVMC should be mirrored and referred to the drain potential of T_1. Afterwards, all the calculations performed for the low-side case remain valid.

B. Accuracy Measurement and DC Calibration

The accuracy of the proposed OVMC with respect to the assumptions made in Section III-A is herein verified and calibration measurements support the analysis.

The first requirement for a correct operation of this OVMC is based on the identity $v_{D_2} = v_{D_1}$. First, in order to guarantee $i_{D_1} = i_{D_2}$, the current flowing in the voltage divider formed by $R_{1,a}$–$R_{1,b}$ (if present) must be negligible. If this cannot be achieved by increasing the value of $R_{1,a}$+$R_{1,b}$, an operational amplifier Op_3 can be added between v_1 and R_{1a}.

However, even if $i_{D_1} = i_{D_2}$, the eventually different junction temperatures of the diodes (i.e. T_{D_1} and T_{D_2} respectively) and their manufacturing variability can cause a mismatch of v_D.

T_{D_1} can generally be higher than T_{D_2} because D_1 is exposed to a wide input voltage excitation and is also physically closer to T_2, where the major losses, i.e. heat, are dissipated. In order to minimize the problem, the nominal operating point of the circuit can be tuned at a temperature-independent point of the *V-I* characteristic of the diodes (if existing and coinciding between them). Alternatively, two diodes in the same package can be chosen in order to maximize their thermal coupling. Unfortunately, as explained in Section II, several constraints already drive the selection of the diodes (e.g. small parasitic output capacitances) if good dynamic performance are required and it results difficult to find devices combining all these characteristics. More realistically, as shown in Fig. 4(b) (dashed box), a sufficient and good practice is to thermally well couple D_2 with D_1 on the OVMC PCB (and if necessary provide separation between the OVMC and T_2 without excessively increasing the parasitic inductance of the connection). Hence, a $\Delta T_D = T_{D_1} - T_{D_2}$ of only 3 °C (Fig. 2(b)) is measured in the worst-case operating conditions of interest (i.e. maximum losses of 8 W in T_2 at the highest switching frequency of 1 MHz and off-state voltage of 400 V). In particular, depending on the operating conditions of T_2, T_{D_1} varies between $T_{D_1,min} = 30$ °C and $T_{D_1,max} = 40$ °C.

Concerning the device variability, before assembling the circuit, two diodes featuring the same v_D in the operating conditions of interest must be selected (a variability in the range of 10 mV is experienced in worst case among the available ones). To minimize this issue, it is convenient to reduce the variation of i_p from $i_{p,min} < I_{p,nom} < i_{p,max}$, caused by a variation of v_{ds} (according to (9)). For this reason, in [12], the voltage source V_p–R_6 is replaced with a current source I_p. However, considering the experiment presented in the introduction (i.e. a specimen power MOSFET with $R_{ds,on} = 25$ mΩ conducting ±20 A), the excursion of v_{ds} is in the range of ±500 mV and the current variation results

$$\Delta i_p = \frac{i_{p,max}}{i_{p,min}} \overset{(9)}{=} \frac{V_p - v_{D_2} - v_{D_1} - v_{ds,min}}{V_p - v_{D_2} - v_{D_1} - v_{ds,max}} \approx 1.1. \quad (10)$$

Even a worst-case ±15% variation, i.e. ±1.5 mA, is assumed not to have any influence on the OVMC accuracy. To quantitative support this statement, v_{D_1} and v_{D_2} are reported in TABLE I as a function of i_p and T_{D_1} . A worst-case mismatch in the diode voltage drops $v_{\Delta D} = v_{D_1} - v_{D_2} = 2$ mV and a temperature coefficient of 1 $\frac{mV}{°C}$ are observed. $v_{\Delta D}$ must be negligible compared to the measured vds not to affect the OVM accuracy. This becomes more and more difficult to achieve at low OV levels, e.g. with $v_{ds} < 40$ mV, and if desired an even more sophisticated diode matching and/or calibration procedure can be adopted. However, other problems arise when v_{ds}, i.e. the DUT current, approaches 0 V and are discussed in Section IV-A. Finally, it can be noticed that, due to the small value of i_p, the diode model provided in [27] is not valid. The proposed calibration procedure is required to enable the performance of the OVMC described in this section. Other interesting considerations regarding the precise tuning of the proposed OVMC are reported in Appendix A as guideline for its design.

To conclude, once the crucial aspects related to the design of the proposed OVM hardware are clarified and taken into account, the achieved accuracy is measured. Fig. 6 illustrates the relative error ε_r (right y-axis) from a DC input v_{ds} (*x*-axis) to a DC output v_m (left *y*-axis) in a range from −2 V to 2 V. ε_r is confined between ±2% with an absolute maximum error $\varepsilon_{max} = 5$ mV. Here, and in the rest of the analysis, the gain of the proposed OVMC is normalized to 1 for the sake of clarity.

TABLE I
MISMATCH IN THE DIODE VOLTAGE DROPS AS FUNCTION OF THEIR TEMPERATURE AND CURRENT

i_p	T_{D_1}	v_{D_1} (mV)	v_{D_2} (mV)	$v_{\Delta D}$ (mV)
$i_{p,min}$	$T_{D_1,min}$	831	832	-1
	$T_{D_1,max}$	820	818	2
$i_{p,max}$	$T_{D_1,min}$	838	839	-1
	$T_{D_1,max}$	828	826	2

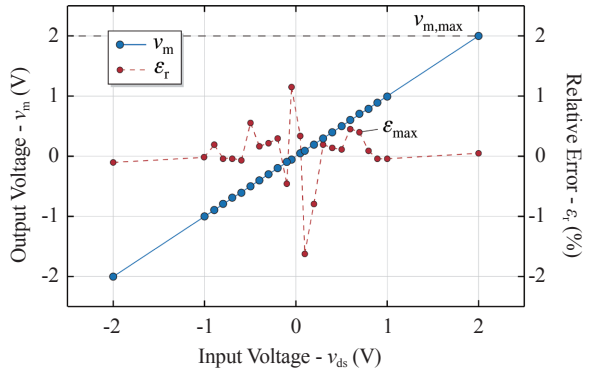

Fig. 6. Results of the DC calibration of the proposed OVMC. When a DC voltage $-2\ V < v_{ds} < 2\ V$ is applied at the input (x-axis), the output v_m (left y-axis) deviates less than 5 mV, corresponding to $\varepsilon_r < 2\%$ (right y-axis) in worst-case.

C. Bandwidth Measurement and AC Calibration

A severe bandwidth requirement is mandatory in all the application areas of OVMCs mentioned in the introduction when fast switching semiconductors are considered. The bandwidth and the accuracy in AC operation of the proposed OVMC are verified in this section to evaluate its applicability in the conditions of interest. Measurements are preceded from a brief discussion pointing out the most significant aspects enabling its performance.

Accurately sensing a high-frequency signal with a conventional oscilloscope probe (as in Fig. 2(a)-(b)) results in a challenge. In fact, when the high-impedance input (i.e. 1 MΩ) of the oscilloscope is used, precise tuning of the probe internal capacitance is required to have a flat gain for all the frequency range of interest. Hence, the 50 Ω input of the oscilloscope is preferred. $R_S \approx 50\ \Omega$ is added at the output of the proposed OVMC (cf. Fig. 4(a)-(c)) to match the output impedance of Op_2 with the characteristic impedance of the used cable (i.e. 50 Ω). This is possible only given the presence of Op_2, driving the necessary output current in the oscilloscope without affecting the circuit performance. Therefore, the selection range of operational amplifiers is limited from their output current and voltage capabilities. Among the available devices, a low-noise 1 GHz 10 V 40 mA operational amplifier [28] is selected to maximize the achievable bandwidth of the OVMC.

The results of the high-frequency calibration are described in Fig. 7. Three different triangular waveforms at 700 kHz

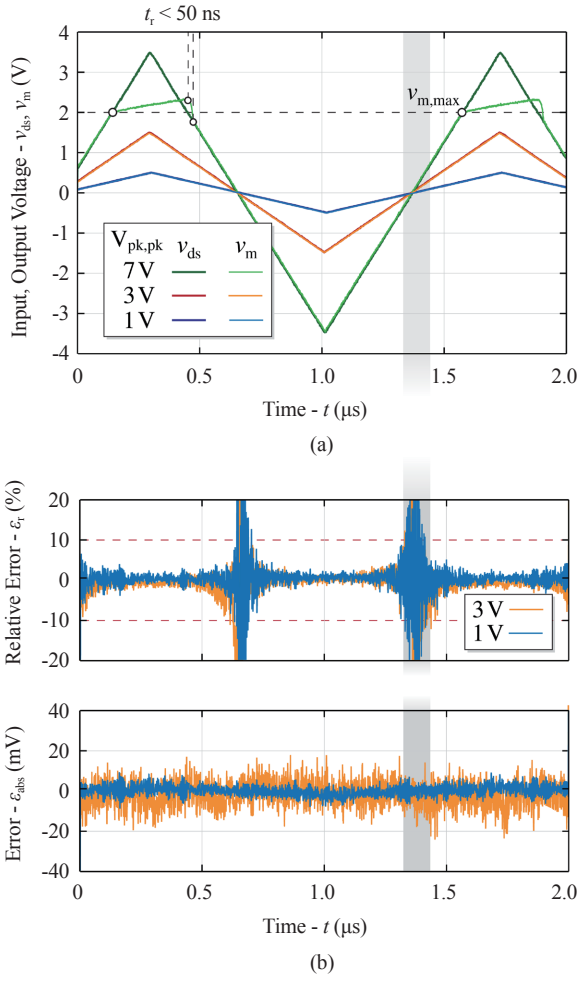

Fig. 7. Results of the AC calibration of the proposed OVMC. When AC voltage waveforms of different amplitudes are applied at the input v_{ds}, the output waveforms v_m are practically indistinguishable from them: ε_{abs} is limited by the oscilloscope resolution.

with peak-to-peak voltage amplitudes $V_{pk,pk}$ increasing from 1 V to 7 V are generated at the input v_{ds} and plotted (blue, red and dark green) on top of the measured output v_m (sky blue, orange and light green) in Fig. 7(a). When $v_{ds} < 2$ V the input and output waveforms are indistinguishable. At $v_{ds} = v_{m,max} = 2$ V, Op_1 saturates and v_m (light green) is distorted. In Fig. 7(b), the relative ε_r and absolute ε_{abs} errors are reported. ε_{abs} is limited between $\varepsilon_{abs;max} = \pm 10$ mV in the worst-case of $3V_{pk;pk}$ and has a zero mean. It must be mentioned that with a 10 bits oscilloscope on a 8 V vertical window, $\varepsilon_{abs;max}$ is in the range of the oscilloscope resolution ($8\ V/2^{10} \approx 8$ mV). ε_r is, for the same reason, mainly in a ±5% range; however, when v_{ds} approaches zero (gray shaded area), the division between two small numbers causes a numerical issue and ε_r diverges.

Finally, with a vector network analyzer, the bandwidth of the proposed OVMC is measured exciting it at the input v_{ds} with sinusoidal waveforms up to $2V_{pk,pk}$. The −3 dB bandwidth is outside the measurable frequency range of the instrument (i.e. 50 MHz) while the more intuitive normalized linear gain g_{lin} is 1.0 until 1 MHz and still 0.97 at 10 MHz,

TABLE II
SPECIFICATIONS OF THE POWER SEMICONDUCTORS CONSIDERED AS DUT FOR THE PROPOSED OVMC

Specimen	Type	$V_{dc,max}$ (V)	$I_{ds,max}$ (A)	$R_{ds,on}$ (mΩ)	Package	Figures
A	SiC Power MOSFET	1200	98	25	TO-247-3	14 (a), 13, 11 and 9
B	Si Super-Junction MOSFET	700	46	40	TO-247	14 (b) and 10 (b)
C	E-mode GaN HEMT	650	30	50	GaN*PX*™	14 (c), 10 (a) and 3

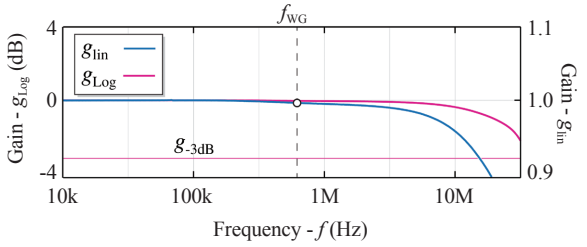

Fig. 8. Measured bandwidth of the proposed OVMC. The –3 dB bandwidth is above 50 MHz (magenta) while g_{lin} = 1.0 until 1 MHz and 0.97 at 10 MHz (blue).

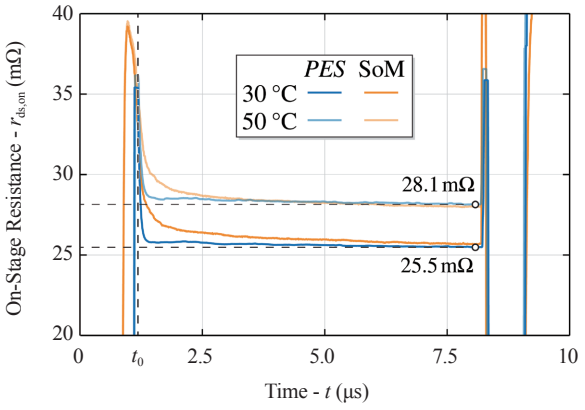

Fig. 9. Comparison in terms of dynamic response between the proposed OVMC (*PES*) and a state-of-the-market (SoM) commercial OVM probe. When the DUT turns on at t_0, the output of the proposed OVMC immediately measures the correct OV, i.e. the nominal $r_{ds,on}$ value, whereas the commercial device features a time constant in the µs-range. E.g. a fast dynamic response increases the maximum switching frequency at which an OVMC can perform useful measurements, since the dynamic transient must be negligible compared to the duration of the DUT on-state.

independently of the input signal amplitude (Fig. 8). In order to guarantee the linearity in these measurements, the input signal never exceeds $v_{m,max}$. The real bandwidth of the circuit is, instead, strongly influenced from its dynamic response after the DUT turn-on switching transition, which is the topic of the next section.

D. Dynamic Response

To conclude the characterization of the proposed OVMC, its outstanding dynamic response is analyzed in this section, accompanied by a discussion on the main features enabling this achievement.

As mentioned, it is important to perform accurate OVMs immediately after the turn-on transition of the DUT. This allows to capture eventual dynamic $R_{ds,on}$ effects, the diode conduction phase during dead-times and enables high-frequency measurements necessary in all the mentioned application areas. In fact, the time constant of the dynamic response must be negligible compared to the duration of the DUT on-state to obtain meaningful OVMs.

In Fig. 9, the dynamic response of the proposed OVMC is compared with the one of a state-of-the-market (SoM) commercial OVM probe. The two measured waveforms highlight the faster response of the proposed approach (blue). The measured signal is the on-state resistance $r_{ds,on}(t)$ (time dependency is omitted from now on) of a commercial 1200 V SiC Power MOSFET (Specimen A in TABLE II) for two different case temperatures. The value of $r_{ds,on}$ is obtained dividing the output of the OVMCs v_m by the DUT current i_{sw} (see Fig. 1) and must be limited to the time window where the DUT is in on-state (i.e. after t_0). The key design guidelines at the basis of the achieved performance rely on the selection of high bandwidth operational amplifiers and diodes with small parasitic capacitance, and on a low inductive PCB design (especially concerning the commutation loop of D_1). In order to quantify the dynamic response time of the proposed OVMC, two more measurements, showing the turn-on transition of different DUTs, are performed (Fig. 10). In Fig. 10(a), a commercial 650V E-mode GaN HEMT (Specimen C in TABLE II) is tested. The three voltage measurements are v_{ds} (yellow), v_{gs} (green) and v_m (blue). When the high-side transistor T_1 is turned off, v_{ds} drops from V_{DC} to 0 V because of a positive load current i_{load} (not shown, see Fig. 1). The anti-parallel body diode of T_2 (i.e. D_{T_2}) immediately conducts and $v_m = -V_{fv,BD} = -7$ V is clamped to the bottom of the oscilloscope screen. When v_{gs} reaches V_{th,T_2} (green dot), T_2 turns on and i_{sw} commutates from D_{T_2} to the channel of T_2. Consequently v_m changes from the forward voltage of D_{T2} (i.e. $-V_{fv,BD}$) to $r_{ds,on}i_{sw}$. As the white cursors highlight, the response time of the proposed OVMC is less than 50 ns if the real transition is assumed instantaneous.

The same situation is reproduced in Fig. 10(b) with a commercial Si Super-Junction MOSFET (Specimen B in TABLE II). In this condition, $V_{fv,BD} \approx 0.8$ V can be accurately measured during all the conduction time of D_{T_2}. In transparency a second measurement with a shorter dead-time is overlapped.

IV. ONLINE CONDUCTION LOSS MEASUREMENT

In this section, the integration of the proposed OVMC in a power converter (Fig. 1) is commented and the OV, i.e. $R_{ds,on}$,

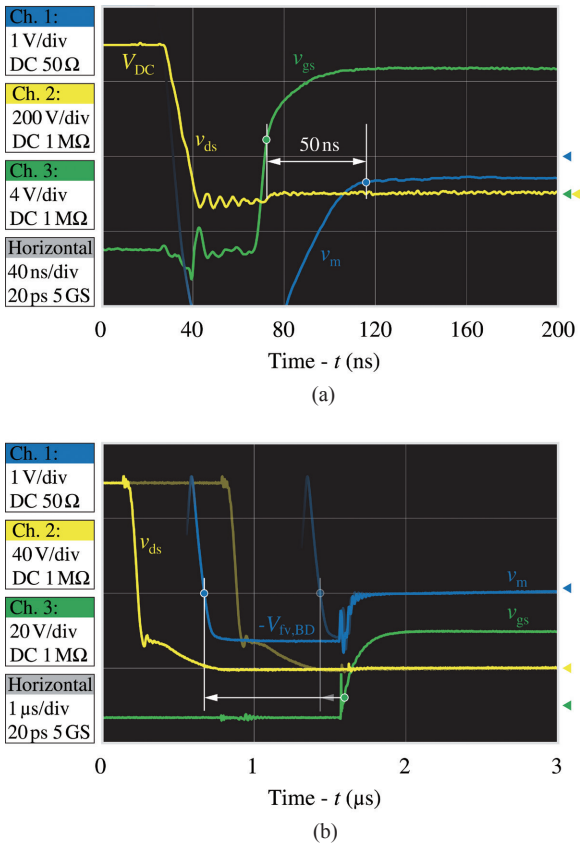

Fig. 10. Analysis of the dynamic response of the proposed OVMC. (a) less than 50 ns after v_{gs} has reached V_{th,T_2} (green dot), v_m (blue) is settled to the correct value, even in the case of significant $V_{fv,BD}$, e.g. > 2 V. (b) when $V_{fv,BD}$ is in the measurable range, the proposed OVMC allows to monitor the conduction time of D_{T_2}, evaluating the dead-time conduction losses and its effective duration.

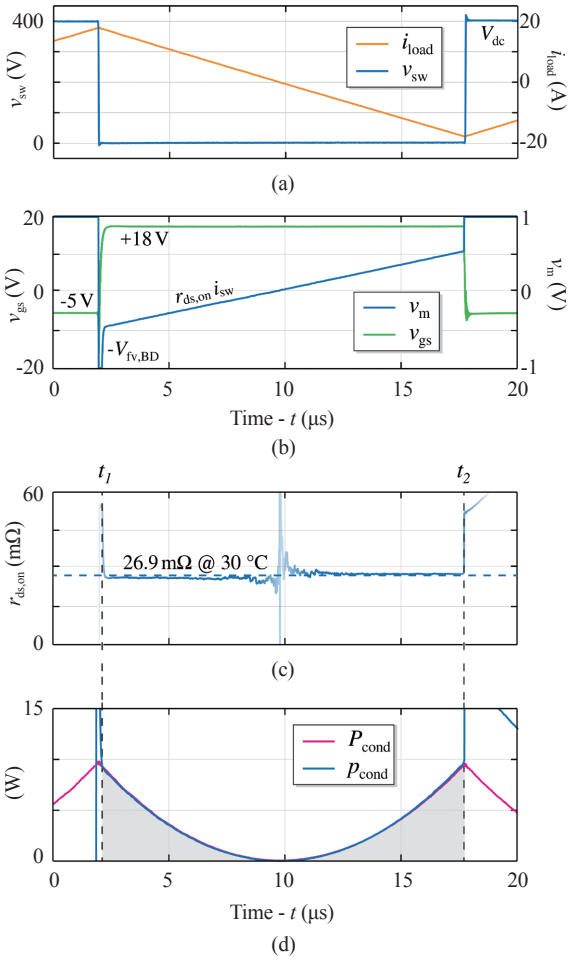

Fig. 11. Typical waveforms (a)-(b) measured on the half-bridge (Fig. 1) operating in triangular current mode (TCM). When $v_{gs} = V_{gs,ON}$ (green), T_2 conducts and v_m (blue) is proportional to i_{sw} (orange). In (c) $r_{ds,on}$ is calculated between t_1 and t_2 dividing v_m by i_{sw}, while in (d) p_{cond} is obtained multiplying v_m and i_{sw}.

of different power semiconductors is measured as function of their operating conditions. The measurement setup is initially described. The associated challenges are then addressed and the proposed solutions are ultimately commented. Finally, since the original reason motivating the development of this OVMC is the improvement of the measurement accuracy of calorimetric switching loss measurement methods, the presented results are discussed accordingly.

A. Conduction Loss Measurement Setup

The setup is equivalent to the schematic shown in Fig. 1. Assuming symmetrical triangular current mode (TCM) operation of the half-bridge (i.e. T_1 and T_2 are operated with complementary 50% duty cycles and no load is connected), the analysis can be limited to the conduction time of T_2. All the relevant measured waveforms are shown in Fig. 11 (a)-Fig. 11(b). In particular, the switch node voltage v_{ds} (blue in Fig. 11 (a)), the load current i_{load} (orange), the gate voltage v_{gs} (green, $V_{gs,ON}$ = 18 V and $V_{gs,OFF}$ = –5 V) and the output of the proposed OVMC v_m (blue in Fig. 11(b)). Inside the time window t_1–t_2, the on-state resistance $r_{ds,on}$ of T_2 can be determined dividing v_m by $-i_{load} = i_{sw}$ (Fig. 11(c)). The instantaneous conduction losses pcond can be calculated as $r_{ds,on}i^2_{sw}$ or equivalently $v_m i_{sw}$ (blue in Fig. 11(d)). Finally, the average conduction losses can be obtained as average of p_{cond} during on-state of T_2 (gray shaded area).

Similarly, an average $R_{ds,on}$ value can be obtained as average of $r_{ds,on}$. In this case, $R_{ds,on}$ = 26.9 mΩ (Fig. 11(c)) results for Specimen A in TABLE II. Consequently, the approximated conduction losses P_{cond} can be directly calculated as $R_{ds,on}i^2_{sw}$ (magenta in Fig. 11(d)). Given the almost perfect overlap between the blue and magenta curves in Fig. 11(d), when p_{cond} and P_{cond} are averaged, 3.6 W results in both cases. However, in general, the first approach is preferred, since it takes into account dynamic $R_{ds,on}$ effects and the eventual current dependency of $R_{ds,on}$.

In order to perform accurate measurements in this setup and operating conditions, two challenges, associated in particular with the reduced OV and high current slopes that needs to be measured, are faced. The first challenge to overcome is represented by the parasitic inductance L_P (Fig. 1) in series with T_2. Fig. 12(a) highlights the load current slope $di_{load}/dt = -di_{sw}/dt$ (up to tens of A/µs) that in combination with L_P causes a voltage offset (red in Fig. 12(b)) on v_m according to

$$v_{\mathrm{m}} = R_{\mathrm{ds,on}} i_{\mathrm{sw}} + L_{\mathrm{P}} \frac{\mathrm{d}i_{\mathrm{sw}}}{\mathrm{d}t} \tag{11}$$

(blue in Fig. 12(b)). Hence, calculating $r_{\mathrm{ds,on}}$ as

$$r_{\mathrm{ds,on}} = \frac{v_{\mathrm{m}}}{i_{\mathrm{sw}}} \overset{(11)}{=} R_{\mathrm{ds,on}} + \frac{L_{\mathrm{P}}}{t} = R_{\mathrm{ds,on}} \left(1 + \frac{\tau_{\mathrm{RL}}}{t}\right), \tag{12}$$

the term $\frac{\tau_{\mathrm{RL}}}{t}$ $\left(\tau_{\mathrm{RL}} \doteq \frac{L_{\mathrm{P}}}{R_{\mathrm{ds,on}}}\right)$ distorts the result. Therefore, in contrast to a constant $R_{\mathrm{ds,on}}$ (dashed in Fig. 12(c)), the waveform of $r_{\mathrm{ds,on}}$, solid in Fig. 12(c), is obtained. E.g. if L_{P} = 8 nH and $R_{\mathrm{ds,on}}$ = 50 mΩ then $\tau_{\mathrm{RL}} \approx$ 150 ns. Hence, after $t = 5\tau_{\mathrm{RL}}$ = 800 ns, $r_{\mathrm{ds,on}} = 1.2\, R_{\mathrm{ds,on}}$ = 60 mΩ. From (12) it can be concluded that L_{P} should be minimized, i.e. the connection from the DUT to the OVMC should start as close as possible from the drain and source terminals of T_2, excluding any additional path where i_{sw} flows. Unfortunately, part of L_{P} is located internally in the package of the DUT and no design expedient results helpful. A compensation network could be inserted and tuned, however it would negatively affect the dynamic performance of the proposed OVMC. Alternatively, the inductive voltage drop $v_{\mathrm{m,o}}$ can be isolated from the resistive one taking advantage of the zero crossing of i_{sw}.

I.e., measuring v_{m} and $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$ when i_{sw} = 0 A, (11) can be solved for L_{P}. Formally

$$v_{\mathrm{m,o}} \doteq v_{\mathrm{m}}|_{i_{\mathrm{sw}}=0} \overset{(11)}{=} L_{\mathrm{P}} \frac{\mathrm{d}i_{\mathrm{sw}}}{\mathrm{d}t}. \tag{13}$$

Repeating this measurement for different $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$, L_{P} can be calculated as average of several

$$L_{\mathrm{P_i}} = \frac{v_{\mathrm{m,o_i}}}{\mathrm{d}i_{\mathrm{sw_i}}/\mathrm{d}t} \tag{14}$$

and its value can be used to adjust $v_{\mathrm{m_i}}$. From the practical point of view, this results in subtracting $v_{\mathrm{m,o_i}}$ from $v_{\mathrm{m_i}}$ in each measurement, ensuring $v_{\mathrm{m_i}}$ = 0 V when $i_{\mathrm{sw_i}}$ = 0 A. Whereas this assumption sounds legit and sufficient by itself, calculating L_{P} as in (14) provides a physical motivation to this adjustment. Moreover, obtaining constant $L_{\mathrm{P_i}}$ across different measurements guarantees their correctness. This becomes more and more important when the zero crossing of i_{sw} is not present and/or measurable and the knowledge of L_{P} is the only option to correct the measurement result. Alternatively, $r_{\mathrm{ds,on}}$ can be calculated as the ratio between $\mathrm{d}v_{\mathrm{m}}/\mathrm{d}t$ and $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$. Even if not affected from $v_{\mathrm{m,o}}$, this approach loses accuracy when the voltage and current slopes become flatter.

The second challenge is easily highlighted applying the propagation of uncertainty rule on $r_{\mathrm{ds,on}} = v_{\mathrm{m}}/i_{\mathrm{sw}}$:

$$\begin{aligned} \sigma_{r_{\mathrm{ds,on}}} &= \sqrt{\left(\frac{\partial r_{\mathrm{ds,on}}}{\partial v_{\mathrm{m}}}\sigma_{v_{\mathrm{m}}}\right)^2 + \left(\frac{\partial r_{\mathrm{ds,on}}}{\partial i_{\mathrm{sw}}}\sigma_{i_{\mathrm{sw}}}\right)^2} \\ &= \frac{1}{i_{\mathrm{sw}}}\sqrt{\sigma_{v_{\mathrm{m}}}^2 + (r_{\mathrm{ds,on}}\sigma_{i_{\mathrm{sw}}})^2} \end{aligned} \tag{15}$$

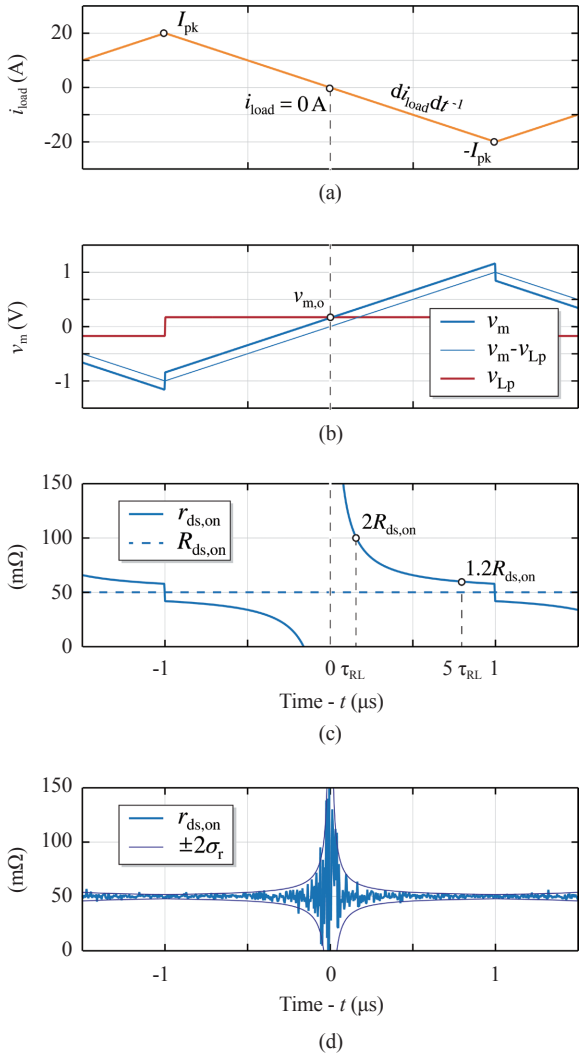

Fig. 12. Comparison of real and ideal waveforms simulated on the half-bridge (Fig. 1) operating in TCM. The combination of L_{P} and $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$ causes a distortion on v_{m} (b) and consequently on $r_{\mathrm{ds,on}}$ (c). Moreover, a measurement error on v_{m} translates into an error on $r_{\mathrm{ds,on}}$ (d) according to (16), particularly amplified for small i_{sw} as in (15).

and

$$\sigma\%_{r_{\mathrm{ds,on}}} = \frac{\sigma_{r_{\mathrm{ds,on}}}}{r_{\mathrm{ds,on}}} \overset{(15)}{=} \frac{\sigma_{v_{\mathrm{m}}}}{r_{\mathrm{ds,on}} i_{\mathrm{sw}}} = \sigma\%_{v_{\mathrm{m}}}. \tag{16}$$

σx and $\sigma\% x$ indicate the absolute and relative error on the measured quantity x, respectively. (15) proves why $\sigma_{r_{\mathrm{ds,on}}}$ and therefore $r_{\mathrm{ds,on}}$ diverges when i_{sw} approaches zero (see Fig. 11(c) and Fig. 12(c)-(d)). (16), instead, expresses how $\sigma\%_{r_{\mathrm{ds,on}}}$ coincides with $\sigma\%_{v_{\mathrm{m}}}$ when $\sigma_{i_{\mathrm{sw}}} = 0$. In other words, any error on v_{m} reflects one-to-one (relatively) on $r_{\mathrm{ds,on}}$ (i.e. on p_{cond}). An example of $r_{\mathrm{ds,on}}$, corrected from $v_{\mathrm{m,o}}$, but resulting from v_{m} with $\sigma_{v_{\mathrm{m}}}$ = 5 mV to highlight the effect, is shown in Fig. 12(d). Since the only expedient to minimize both phenomena described from (15) and (16) is to reduce $\sigma_{v_{\mathrm{m}}}$, this section clearly justifies the effort placed on the accuracy analysis of the proposed OVMC addressed in Section III. Moreover, it highlights how measurements of low $r_{\mathrm{ds,on}}$ and/or high $\mathrm{d}i_{\mathrm{load}}/\mathrm{d}t$ (e.g. wide bandgap semiconductors) introduce new

challenges in the OVMs.

B. Conduction Loss Measurement Results

Several measurements are performed with the proposed OVMC analyzing different DUTs in different operating conditions. The results are commented in this section.

Fig. 13 compares the nominal value of $R_{ds,on}$ reported in the datasheet of Specimen A in TABLE II with the values of $R_{ds,on}$ measured with the proposed OVMC during double pulse test (DPT) operation (in the same conditions described in the datasheet). The black dashed line R_{data} is plotted as function of the junction temperature $T_{j,data}$ (i.e. bottom x-axis) while the blue measurement points R_{DPT} are plotted as function of the measured case temperature $T_{c,DPT}$ (i.e. top x-axis). Since the DPT has electric dynamics which are assumed to be faster than the thermal dynamics of the DUT, $T_{c,DPT} \approx T_{j,DPT}$ is considered and the two x-axis coincide (i.e. $T_{j,DPT} \approx T_{j,data}$). R_{DPT}, measured with the proposed OVMC as described in Fig. 9, match R_{data} with an approximation of ±3% (blue confidence bar is ±5%). The discrepancy can be attributed mainly to the device manufacturing variability. However, the results are satisfactory and confirm the performance of the proposed OVMC.

Fig. 14(a), (b) and (c), instead, summarize the values of $R_{ds,on}$ measured in two different continuous operating conditions for all the Specimens of TABLE II. In particular, the orange points R_{TCM} are measured (with the proposed OVMC) in the conditions described in Section IV-A (i.e. TCM operation with $V_{DC} = 400$ V, $I_{pk} = 20$ A and $f_{sw} = 30$ kHz) while the green points R_{DC} are measured (with the proposed OVMC and a multimeter to monitor its accuracy) in DC operation. The DC current $I_{DC} = I_{pk}/(\sqrt{3}\sqrt{2}) = 8$ A is selected to ensure that approximately the same losses occur in the DUT in DC operation as in TCM operation (legitimately neglecting the soft-switching losses [15]), such that $T_{j,DC} \approx T_{j,TCM}$ when $T_{c,DC} = T_{c,TCM}$ is measured. All the circuit parameters are maintained the same in both the experiments, in particular matching the value recommended in the datasheet. For Specimen A, R_{TCM} (cf. also Fig. 11(c)) and R_{DC} (Fig. 14(a)) are slightly higher than R_{data} and R_{DPT} (cf. Fig. 13). The reason behind it is the difference in T_j between the two sets of measurements ($T_{j,DC} \approx T_{j,TCM} > T_{j,data} \approx T_{j,DPT}$) due to the losses continuously occurring in the DUT. As a consequence, the positive temperature coefficient of $R_{ds,on}$ affects the result. More interesting to notice is that R_{DC} is very close, i.e. within ±4% (orange confidence bar is ±5%), to R_{TCM} as expected, since $T_{j,DC} \approx T_{j,TCM}$ and the current dependency of $R_{ds,on}$ is practically negligible in this range. The discrepancy can be attributed to the accuracy of the current measurement and of the OVMC, and to slightly different operating conditions. An equivalent set of measurements is performed on Specimen B in Fig. 14(b) and identical conclusions can be drawn. Hence, the accuracy and the performance of the proposed OVMC are once more validated. Fig. 14(c) summarizes R_{TCM} and R_{DC} for Specimen C in TABLE II. In this case a significant

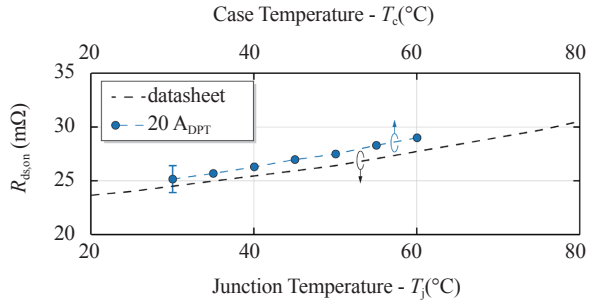

Fig. 13. Average value of $r_{ds,on}$ (i.e. R_{DPT}) measured with the proposed OVMC in double pulse test (DPT) operation for Specimen A in TABLE II compared with the nominal $R_{ds,on}$ values reported in its datasheet (i.e. R_{data}). The measured points match the nominal values within ±3%.

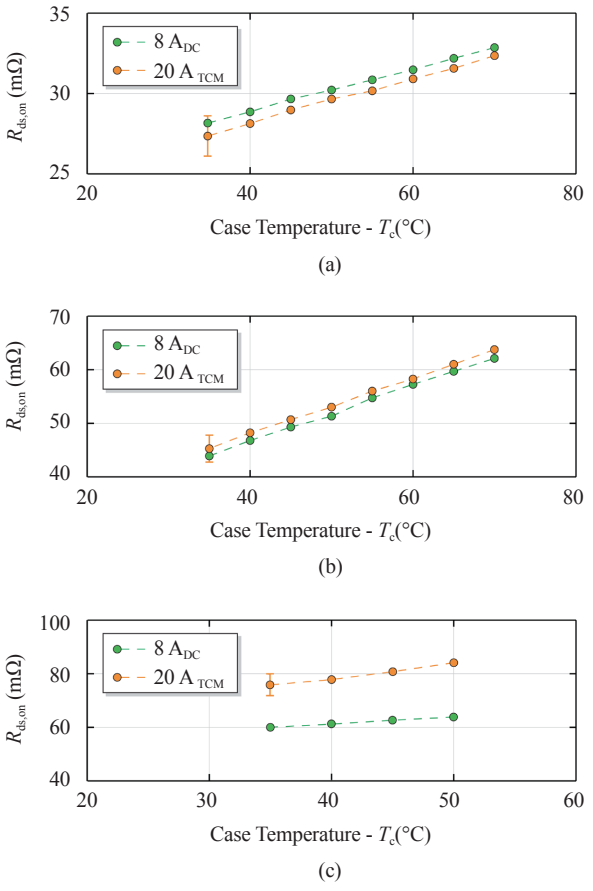

Fig. 14. Average value of $r_{ds,on}$ measured with the proposed OVMC for different operating conditions of the half-bridge, for different DUTs (TABLE II) and as a function of T_c. R_{TCM} (orange) and R_{DC} (green) are similar (within ±5%) for Specimen A (a) and B (b) when the power loss conditions are matched. In the case of Specimen C, a significant discrepancy (i.e. ≈ 50%) between the two measurement sets is observed (c).

discrepancy (i.e. ≈ 50%) between the two series is observed. $T_{j,DC} \approx T_{j,TCM}$ is not a true assumption anymore, since more losses are now unexpectedly occurring in the DUT in TCM operation. The discrepancy is attributed in this case to the DUT, i.e. to dynamic $R_{ds,on}$ effects, which are confirmed in [7].

C. Influence on Calorimetric Switching Loss Measurement

The results illustrated in the last section can be applied to improve the accuracy of the calorimetric switching loss measurements presented in [15]. Calorimetric switching loss measurement methods, in contrast to electric switching loss measurement methods, e.g. the DPT, determine the switching losses from the measurement of thermal quantities [14], [16]. The power semiconductor under test is installed in a calorimetric test-bench, whose thermal parameters (e.g. thermal resistance and thermal capacitance) are known. While the device operates, the occurring losses generate heat and cause a variation of temperature in the test-bench. The exact amount of losses can be derived from the temperature increase.

Both conduction losses and switching losses occur simultaneously in the DUT, hence only their sum can be thermally measured. However, initially operating the DUT in the test-bench at a switching frequency at which the switching losses (P_{sw}) can be neglected compared to the total losses (P_{th}), the conduction losses (P_{cond}) can be accurately measured. A set of measurements performed on Specimen C show an agreement between the two methods (i.e. calorimetric and OVMC) with an uncertainty in the range of 5%, mostly attribute to the calorimetric test-bench itself [15].

The measurement method proposed in [15] to perform calorimetric switching loss measurement consists of two phases. First, accurate calorimetric measurement of the total semiconductor losses are performed (P_{th}). Afterwards, P_{cond} are estimated and subtracted to isolate

$$P_{\mathrm{sw}} = P_{\mathrm{th}} - P_{\mathrm{cond}}. \tag{17}$$

It results immediately clear that the accuracy of the measured P_{sw} (σP_{sw}) is influenced both from the accuracy of the calorimetric measurement itself (σP_{th}) and of the P_{cond} estimation (σP_{cond}). If $\sigma P_{th} = 0$ is assumed for the purpose of this analysis, σP_{sw} can be expressed, applying the propagation of uncertainty rule, as

$$\sigma\%P_{\mathrm{sw}} = -\frac{P_{\mathrm{cond}}}{P_{\mathrm{sw}}}\sigma\%P_{\mathrm{cond}}. \tag{18}$$

The integration of the proposed OVMC in this measurement setup aims to improve σP_{cond}.

In [15], $R_{ds,on}$ is measured in DC operation as a function of P_{th}, similarly to R_{DC} in Fig. 14(a)-(c). Afterwards an opportune (i.e. for the same P_{th} conditions) value of $R_{ds,on}$ is considered to calculate and subtract P_{cond} from P_{th} in TCM operation. The proposed OVMC, enabling online measurement of R_{TCM}, has the potential to minimize σP_{cond} , but confirmed as well the validity of the approach developed in [15] against, for example, the usage of R_{data}. At least for Specimen A and B, in fact, R_{TCM} and R_{DC} (orange and green points in Fig. 14(a)-(b)) coincide with good approximation (within ±5%). Hence, the results shown in [15] are correct under this aspect. Differently, the discrepancy observed for Specimen C (cf. Fig. 14(c)) would introduce a significant error if the [15]-approach would be blindly adopted. Fig. 15(a) compares the results of the two conduction loss measurement methods (i.e. R_{TCM} and R_{DC}) for one of the DUTs analyzed in [15], similar to Specimen C. In this case, the two approaches give significantly different results and the importance of OVMCs for fast switching power semiconductors is again remarked. The accurate measurement of R_{TCM} at 1 MHz is the final achievement of this work, only enabled from the sophisticated design and calibration procedures described along this paper. R_{TCM} is up to 50% higher than R_{DC}, i.e. P_{cond} is 50% higher than previously estimated. According to (18), P_{sw} results up to 28% lower (see Fig. 15(b)). The physical cause behind the underlying loss mechanism is still under investigation [29].

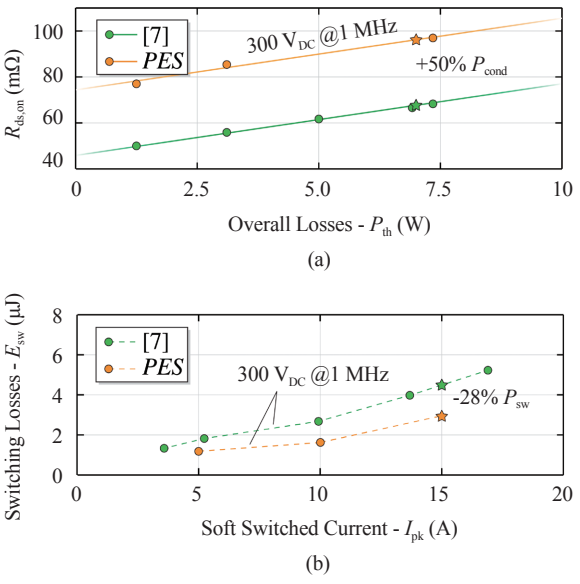

Fig. 15. Comparison between R_{TCM} (orange) and R_{DC} (green) as function of P_{th} (a). The online measurement of conduction losses enabled by the proposed OVMC, more representative of the real operating conditions, results in higher (i.e. ≈ 50%) P_{cond}. The mismatch results in lower estimated P_{sw} (i.e. ≈ –28%) according to the calculation reported in TABLE III (b).

TABLE III
DERIVATION OF THE ERROR ON THE SWITCHING LOSSES CAUSED BY THE INACCURACY ON THE CONDUCTION LOSS ESTIMATION

Parameter	[15]	proposed OVMC	Note
I_{pk} (A)	15		Fig. 15(b)
P_{th} (W)	6.90	6.90	Fig. 15(a)
$R_{ds,on}$ (mΩ)	65	95	Fig. 15(a)
P_{cond} (W)	2.40	3.60	$P_{sw} = R_{ds,on} I_{rms}^2$, $I_{rms} = I_{pk}/(\sqrt{3}\sqrt{2})$
P_{sw} (W)	4.50	3.30	$P_{sw} = f_{sw} E_{sw}$, (17) and Fig. 15(b)
$\sigma\%P_{cond}$	50%		$\left\lvert \frac{P_{cond,[7]} - P_{cond,OVMC}}{P_{cond,[7]}} \right\rvert$ and Fig. 15(a)
$\sigma\%P_{sw}$	-28%		(18) and Fig. 15(b)

The calculations for the case of I_{pk}= 15 A are reported in TABLE III as an example.

V. Conclusion

An on-state voltage measurement circuit (OVMC) for fast switching power semiconductors is presented and fully characterized in this paper. The correction of the offset voltage present in typical OVMCs, the small input parasitic capacitance, the usage of a 50 Ω output stage, the high-bandwidth conditioning circuitry, the integrated generation of the supply voltages and the thoughtful design and calibration process are key features and/or main improvements of the proposed approach when compared with state-of-the-art solutions.

The operating principle of this OVMC is described and detailed design guidelines are given. Furthermore, accurate DC and high-frequency calibration measurements are performed. Several challenges, e.g. measurement distortion due to the DUT parasitic inductance and noise amplification at low DUT current values, arise when the proposed OVMC is integrated in the measurement setup of interest considering fast switching power semiconductors. However, implementing the addressed precautions, the achieved accuracy (< ±2%), bandwidth (> 50 MHz) and dynamic response (< 50 ns) finally enable precise OVMs in the case of both low $R_{ds,on}$ values and at high switching frequencies, e.g. in applications featuring wide bandgap semiconductors. Ultimately, OVMs are performed on several power semiconductors for different operating conditions, and the results in terms of $R_{ds,on}$ are presented, underlying the advantageous practical applicability of the circuit.

In summary, the proposed OVMC generally enables on-state behavior analysis of power semiconductors (e.g. dynamic $R_{ds,on}$ effect investigation) and improves the accuracy of power converters loss breakdown models and of calorimetric switching loss measurement methods. Moreover, the OVM is envisaged as fundamental feature of next generation intelligent gate drivers, including temperature and condition monitoring, as well as time-to-failure prediction circuits.

Appendix

Considerations for the Accurate Tuning of the Proposed On-State Voltage Measurement Circuit

The influence of a mismatch in the diode (i.e. D_1 and D_2) voltage drops $v_{\Delta D}$ can be accurately characterized. In particular, if

$$v_{\mathrm{D}_1} \neq v_{\mathrm{D}_2} = v_{\mathrm{D}_1} \pm v_{\Delta \mathrm{D}},$$

then

$$v_{\mathrm{m}} \overset{(7)}{=} \frac{1}{1+\beta}(v_{\mathrm{ds}} \mp v_{\Delta \mathrm{D}}). \tag{19}$$

As in the diode-based approach of Fig. 2 (b), a mismatch in the correction of v_{D_1} translates in an offset of $v_{\Delta D}$ on v_m. However, Section III-B proved how, with the necessary precautions, a good accuracy can be reached. An offset on v_m can results also from resistive mismatches. First, if

$$R_3 \neq R_4 \quad \longrightarrow \quad \frac{R_3}{R_4} = 1 \pm \delta_{\mathrm{R}}$$

then

$$\begin{aligned} v_{\mathrm{m}} &\overset{(4)}{=} \frac{1}{1+\beta}\left((2 \pm \delta_{\mathrm{R}})v_1 - (1 \pm \delta_{\mathrm{R}})v_2\right) \\ &\overset{(6)}{=} \frac{1}{1+\beta}(v_{\mathrm{ds}} \mp \delta_{\mathrm{R}} v_{\mathrm{D}_2}). \end{aligned} \tag{20}$$

Second, if

$$\frac{R_{1\mathrm{b}}}{R_{1\mathrm{a}} + R_{1\mathrm{b}}} \neq \frac{R_{2\mathrm{b}}}{R_{2\mathrm{a}} + R_{2\mathrm{b}}} = (1 \pm \rho_{\mathrm{R}}) \frac{R_{1\mathrm{b}}}{R_{1\mathrm{a}} + R_{1\mathrm{b}}}$$

then

$$\begin{aligned} v_{\mathrm{m}} &\overset{(4)}{=} \frac{1}{1+\beta}\left(2v_1 - (1 \pm \rho_{\mathrm{R}})v_2\right) \\ &\overset{(6)}{=} \frac{1}{1+\beta}(v_{\mathrm{ds}} \mp \rho_{\mathrm{R}} v_2). \end{aligned} \tag{21}$$

These information are relevant for the calibration of the proposed OVMC, e.g. understanding the causes of inaccuracy from the error trends. In particular, while $v_{\Delta D}$ in (19) and $\delta_R v_{D_2}$ in (20) are practically constant error terms, $\rho_R v_2$ in (21) is proportional to the variable measured voltage. Moreover, it results clear that precise resistors should be used for R_1–R_4.

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