EXCLUSIVELY AVAILABLE VIA IEEE Xplore® DIGITAL LIBRARY

ISSN 2475-742X

CPSS Transactions on Power Electronics and Applications

VOLUME 3 NUMBER 3 SEPTEMBER 2018

SPECIAL ISSUE ON VEHICLE ELECTRIFICATION

A PUBLICATION OF THE CHINA POWER SUPPLY SOCIETY

CPSS TRANSACTIONS ON POWER ELECTRONICS AND APPLICATIONS

CPSS Transactions on Power Electronics and Applications (CPSS TPEA) is sponsored and published by China Power Supply Society and technically co-sponsored by IEEE Power Electronics Society. It publishes original and high quality peer reviewed papers in the field of power electronics and its applications. With the goal of promoting the technology of power electronics including concepts, theory, modeling and control, analysis and simulation, emerging technology and applications, CPSS TPEA is expected to be a favorable platform to strengthen information exchange in this area. Interested authors are welcome to submit your papers via the Manuscript Central (https://mc03.manuscriptcentral.com/tpea-cpss) online submission system. You can find more information on our website: http://tpea.cpss.org.cn.

CPSS and PELS Joint Advisory Committee

Editor-in-Chief

JINJUN LIU
Xi'an Jiaotong University, China
E-mail: jjliu@xjtu.edu.cn

Editorial Office

Tel: +86-22-27680796-18#
Fax: +86-22-27687886
E-mail: tpea@cpss.org.cn
Website: tpea.cpss.org.cn

Editorial for the Special Issue on Vehicle Electrification

ELECTRIC, hybrid and fuel cell vehicles have attracted significant attention in the past decades due to the exhaustion of fossil fuel consumption and their environmental concerns. Electric vehicles use electronic subsystems—in comparison to conventional vehicles, which include electric machines, power electronics, electronic continuously variable transmissions (CVT), onboard chargers, and embedded powertrain controllers. Advanced energy storage systems, such as Li-ion batteries, ultra-capacitors, and fuel cells, together with intelligent energy management algorithms, are introduced in the next generation powertrains. In addition to these electrification components or subsystems, conventional internal combustion engines (ICE), mechanical and hydraulic systems may still present. As a result, the complexity of new powertrain designs and dependence on embedded software is a cause of concern to automotive research and development efforts. This leads to an increasing difficulty in predicting interactions among various vehicle components and systems.Therefore, the design and implementation of the mechanical and electrical components need to be considered carefully. In order to understand the difficulty and prospected challenge of the vehicle electrification, this Special Issue is a review of the state-of-art contributions and new discoveries in the field of power electronics and applications for the electric vehicle.

The Special Issue on Vehicle Electrification collected 4 papers on diverse topics, ranging from the overview to the new contributions on the power electronics for vehicle electrification. The first paper entitled "Parameter Identification of Capacitive Power Transfer System Based on Spectrum Analysis" as written by Chen Chen and his colleagues at the Institute of Electrical Engineering, Chinese Academy of Science (China). The multi-parameter identification method based on spectral information which using the rational fractional fitting algorithm and network synthesis theory is proposed in this paper. Some known-parameters are added to this method, the noise tolerance of the identification result is highly improved, resulting in z better accuracy. The experiment of the double-sided LC matched CPT system model with the vector network analyzer to collect the spectrum information of the circuit shows good results in effectively identifying the unknown parameters in the system model and achieving high accuracy.

The second paper on the "Adaptive DC-Link Voltage Control of LLC Resonant Converter" was proposed by Li-Chung Shih, Yi-Hua Liu and Yi-Feng Luo from National Taiwan University of Science and Technology, Taiwan. In this control technique, the DC-link voltage increases to compensate the voltage drop caused by load variation, which facilities the LLC resonant operates near the resonant frequency. Therefore, the frequency variation range can be reduced, and the efficiency is improved under different load conditions. Moreover, it also decreases the circulating energy and makes the optimal design of LLC converter possible. An experimental prototype was built to verify the feasibility of the controller.

The third paper contributed by Tuopu Na and his colleagues from Harbin Institute of Technology (China) is the "Active Power Filter for Single-Phase Quasi-Z-Source Integrated On-Board Charger". The paper proposes an active power filter (APF) quasi-z-source single phase integrated on-board charger for EV application which can eliminate the second harmonic power on the DC-link. Compared with the conventional quasi-z-source network, this proposed topology only need a small capacitance and inductance, results in space and weight savings. This paper also discussed the design of the APF, and the experimental prototype was built to verify this design.

The last paper is the "Adaptive Charging Strategy with Temperature Rise Mitigation and Cycle Life Extension for Li-ion Batteries" from Shun-Chung Wang and his colleagues from Lunghwa University of Science and Technology, Taiwan. The digitally controlled Li-ion battery charger with an adaptive charging strategy has been employed in this paper. The devised charger can generate the desired charging profile depending on the battery SOC state and temperature variation. Accordingly, the proposed strategy remains the capacity charging with fuzzy temperature control approach that can avoid using the high C-rate current to charge the battery with high RSOC; thus, the phenomenon of the battery aging aggravation due to the extreme electrochemical stress can be subdued. The control strategy is implemented in the power stage of synchronous rectified buck converter for further conduction loss reduction. The GUI is also employed by a low-cost microcontroller and LabVIEW software. The experimental results show the significant improvement of the average temperature-rise, charging efficiency, estimated cycle life compared with the conventional CC-CV control strategy.

We would like to express our big appreciation to the industriousness and carefulness of the guest associate editors for this Special Issue in the selection of these high-quality papers from numerous submitted manuscripts in consideration for publication. We would like to appreciate the tremendous efforts of the expert reviewers who have provided invaluable, in-depth comments and suggestions to improve papers into the highest quality.We also would like to thank all the authors who have a great passion to achieve the best goal of their research for this Special Issue publication.

Chris Mi
Huang-Jen Chiu
Guest Editors-in-Chief

Chris Mi is a fellow of IEEE and SAE, Professor and Chair of the Department of Electrical and Computer Engineering, and the Director of the US DOE funded GATE Center for Electric Drive Transportation at San Diego State University, San Diego, California, USA. He was previously a professor at the University of Michigan, Dearborn from 2001 to 2015. He received the B.S. and M.S. degrees from Northwestern Polytechnical University, Xi'an, China, and the Ph.D. degree from the University of Toronto, Toronto, Canada, all in electrical engineering. Previously he was an Electrical Engineer with General Electric Canada Inc. He was the President and the Chief Technical Officer of 1Power Solutions, Inc. from 2008 to 2011. He is the Co-Founder of SNC Technology.

His research interests are in electric and hybrid vehicles. He has taught tutorials and seminars on the subject of HEVs/PHEVs for the Society of Automotive Engineers (SAE), the IEEE, workshops sponsored by the National Science Foundation (NSF), and the National Society of Professional Engineers. He has delivered courses to major automotive OEMs and suppliers, including GM, Ford, Chrysler, Honda, Hyundai, Tyco Electronics, A&D Technology, Johnson Controls, Quantum Technology, Delphi, and the European Ph.D. School. He has offered tutorials in many countries, including the U.S., China, Korea, Singapore, Italy, France, and Mexico. He has published more than 250 articles and delivered 100 invited talks and keynote speeches and as a panelist in major IEEE and SAE conferences.

Dr. Mi is the recipient of "Distinguished Teaching Award" and "Distinguished Research Award" of University of Michigan Dearborn. He is a recipient of the 2007 IEEE Region 4 "Outstanding Engineer Award," "IEEE Southeastern Michigan Section Outstanding Professional Award." and the "SAE Environmental Excellence in Transportation (E2T) Award." He was also a recipient of the National Innovation Award and the Government Special Allowance Award from the China Central Government. He received two Best Paper Awards from IEEE Transactions on Power Electronics.

Dr. Mi was the Chair (2008-2009) and Vice Chair (2006-2007) of the IEEE Southeastern Michigan Section. Dr. Mi was the general Chair of the 5th IEEE Vehicle Power and Propulsion Conference held in Dearborn, Michigan, USA in September 6-11, 2009. Dr. Mi is one of the three Area Editors of *IEEE Transactions on Vehicular Technology,* Associate Editor of *IEEE Transactions on Power Electronics*, Associate Editor of *IEEE Transactions on Industry Applications.* He served on the review panel for the NSF, the U.S. Department of Energy (2007–2010), the Natural Sciences and Engineering Research Council of Canada (2010), Hong Kong Research Grants Council, French Centre National de la Recherche Scientifique, Agency for Innovation by Science and Technology in Flanders (Belgium), and the Danish Research Council. He is the topic chair for the 2011 IEEE International Future Energy Challenge, and the General Chair for the 2013 IEEE International Future Energy Challenge. Dr. Chris Mi is a Distinguished Lecturer (DL) of the IEEE Vehicular Technology Society.

He is Guest Editor-in-Chief of *IEEE Journal of Emerging and Selected Topics in Power Electronics – Special Issue on WPT*, Guest Co-Editor-in-Chief of *IEEE Transactions on Power Electronics Special Issue on WPT*, Guest Editor of *IEEE Transactions on Industrial Electronics – Special Issue on Dynamic Sireless Power Transfer,* and steering committee member of the IEEE Transportation Electrification Conference (ITEC- Asian). He is Program Chair or General Chair of a number of international conferences, including Workshop on Wireless Power Transfer (WoW), IEEE International Electric Vehicle Conference (IEVC), and IEEE International Transportation Electrification Conference – Asia-Pacific. He is also the chair for the IEEE Future Direction's Transportation Electrification Initiative (TEI) e-Learning Committee and developed an e-learning module on wireless power transfer.

Huang-Jen Chiu has been with the Department of Electronic and Computer Engineering, National Taiwan University of Scienceand Technology, Taipei, Taiwan, where he is a Distinguished Professor and the Director of Center for Power Electronic Technologies, now. His research interests include high efficiency/high power density bidirectional DC/DC converters, PFC topologies, PV inverters, and DSP control in renewable energy applications.

His work brought him several distinctive awards including the Young Researcher Award in 2004 from the Ministry of Science and Technology, Taiwan, the Outstanding Teaching Award in 2009 and 2017, the Excellent Research Award in 2009 and 2011, the Excellent Academic-industry collaboration Award in 2015 and 2017 from the NTUST, the Y. Z. Hsu Scientific Paper Award in 2010 and Google Little Box Academic Awards. His student teams won the grand prize of the IEEE International Future Energy Challenge (IFEC) in 2013 and 2015, respectively. Dr. Chiu is an IEEE senior member and serves as an Associate Editor of the *IEEE Transactions on Industry Applications* and an Associate Editor of the *IEEE Transactions on Circuits and Systems Part II: Express Letters (TCAS-II)*. He served as the Taipei Chapter Chair of IEEE Industrial Electronics Society (2015-2016), the General Co-chair of 2017 IEEE International Future Energy Electronics Conference (IFEEC 2017-ECCE Asia), the Program Chair of 2015 IEEE International Future Energy Electronics Conference (IFEEC 2015), the Topic Co-Chair of 2016 International Future Energy Challenge (IFEC 2016) and the Secretary of IEEE PELS/ IES Taipei Joint Chapter during 2010-2014. Dr. Chiu is a Fellow of the Institute of Engineering and Technology (IET) and selected as the Distinguished Lecturer of IEEE Power Electronics Society (2017-2018).

Parameter Identification of Capacitive Power Transfer System Based on Spectrum Analysis

Chen Chen, Chenhui Li, Chenglin Liao, and Lifang Wang

***Abstract*—Capacitive power transfer (CPT) technology is a newly emerging research focus for EV charging applications. Due to the absence of eddy current loss and light weight of the capacitive coupling metal plates, CPT technology is considered to be a promising alternative to the inductive power transfer (IPT) technology. However, the parameter identification of the CPT system has not been well studied. In this paper, a multi-parameter identification method based on spectral information is proposed, which based on rational fractional fitting algorithm and network synthesis theory. By adding some known parameters to this method, the parameter identification algorithm under constraint is proposed to improve the noise tolerance of the identification results, and at the same time, it can also have better identification accuracy. The experimental results show that the parameter identification algorithm based on spectrum information can effectively identify the parameters of the circuit model of the CPT system, and the identification accuracy is less than 10%.**

***Index Terms*—Capacitive power transfer, frequency spectrum, network synthesis, noise tolerance, parameter identification.**

I. Introduction

CAPACITIVE power transfer (CPT) [1], [2] technology transfers energy through the electric field between the air gap. This idea can be traced back to Nikola Tesla's bold idea of transferring wireless energy through the capacitance of the ionosphere. Recently, with the increase of the power capacity of the CPT system, it has become a new research focus in the field of wireless charging for electric vehicles.

CPT technology has several unique advantages against the widely-used inductive power transfer (IPT) technology. First, the electric fields do not generate eddy current in the metal material nearby as the magnetic fields do. Besides, the capacitive coupling is usually composed of several conductive plate pairs with no ferrite required, so the coupling part of the CPT is in low cost and light in weight [3]. With these advantages, CPT is considered to be a promising technology in wireless EV charging [4].

Jiejian Dai proposed a design composed of conducting foil at the rear of the EV and a foam-based bumper at the charging station. This technique allows for simple mechanical implementation and avoids the pitfalls associated with alignment and air gap maintenance usually encountered with CPT systems [5].

The double-sided LCLC CPT system proposed by Lu is a breakthrough in designs of high-power long-distance CPT system, and this prototype system can transfer 2.4 kW power at a distance of 150 mm. This work provides a complete design of CPT system for EV charging which reaches a DC-to-DC efficiency of over 90% and works on a relatively low frequency of 1 MHz [6].

Lu also refined LCLC compensation to CLLC compensation, which reduces the inductance needed for compensation [7]. A simpler LC compensation is also analyzed comparing with the LCLC topology which seemed to be more feasible as it has less components to tune [8]. Due to its simplicity, it is more likely to be realized on EV charging scenario [9].

However, during the wireless charging process of EV, wireless power transfer (WPT) system often needs to work under different coupling conditions due to the uncertainty of the placement position and external conditions of the coupling device. Therefore, the same transmitter-end device may need to have the ability to supply power to multiple receiver devices with different parameters. At present, many parameter identification methods have been developed in inductively coupled power transfer (ICPT) systems, but there are few studies on the parameter identification of the CPT system [10].

In the parameter identification study of ICPT system, most of the identification algorithms are only for a single unknown parameter under the premise of known circuit model parameters. Reference [11] is based on the principle of energy conservation, using the circuit model of the matching circuit to derive the relationship between the voltage and current at the output of the inverter and the load at the receiving end, so as to realize parameter identification of the load at the output. The reference [12] realizes the parameter identification of the output load by measuring the decay speed of the circuit's free oscillation.

For the case where the coupled inductance and the load resistance are unknown, the reference [12] uses the standard load resistance at the output end. First, the coupled inductor is identified under the operating condition of the standard load, and then the actual load resistance is performed under the condition that the coupled inductor identification value is obtained, thereby achieving multi-parameter identification.

In the ICPT system, the change of the coupled inductance does not affect the phase of the reflected impedance. The reference [13] measures the voltage and current output from the inverter, and uses the phase of the reflected impedance to identify the load resistance, and then uses the reflection im-

Manuscript received July 26, 2018. (*Corresponding author: Chenglin Liao.*)

The authors are with the Key Laboratory of Power Electronics and Electric Drive, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing 100190, China (e-mail: chenchen@mail.iee.ac.cn; lichenhui@mail.iee.ac.cn; liaocl@mail.iee.ac.cn; wlf@mail.iee.ac.cn).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00017

pedance amplitude to identify the coupled inductance. This realizes the identification of coupled inductance and output load.

The identification methods used in the above ICPT system often rely on accurate measurement of known parameters of the circuit or directly interpolate fitting results directly from the experimental results. Each identification method is often designed independently according to a specific identification target, and the unknown parameter is also limited to the coupled inductance and the load resistance.

At present, the parameter identification of the CPT system is not well study, this is due to its higher operating frequency and higher requirements on the sampling circuits. On the one hand, there is a coupling relationship between the coupling capacitance and the reflected impedance of CPT, which leads us to be unable to use the method mentioned in reference [13]. On the other hand, the resonant operating frequency of the capacitive system is narrower, and its working state is greatly affected by the matching parameters, if the circuit parameters cannot be accurately measured, it is difficult to obtain good estimation accuracy by using the method described in the reference [12].

Therefore, this paper proposes a more general parameter identification algorithm for the CPT system. Since the result obtained by directly using the driving-point function is very sensitive to noise, in order to improve the applicability of parameter identification, the partial loss resistance and matching circuit component parameters in the model circuit are taken as known values, and by adding these known values as constraints to the identification system model, the noise tolerance of the algorithm can be improved.

II. Parameter Identification Method Using Frequency Spectrum Information

The circuit model of CPT system is shown in Fig. 1, where L_1, C_1, L_2, C_2 respectively for the transmitter and receiver matching circuit inductance and capacitance, Cm for the coupling capacitor, R_{load} for the load resistance. By analyzing its circuit model, we can know that when the output load is stable, the system can be seen as a single-port network driven by the inverter output, and the internal components of the network are lumped-parameter linear components. Therefore, the problem of parameter identification for CPT systems can be abstracted as a parameter identification problem for a single-port network. According to the circuit network theory, for a linear single-port network, its external characteristics are fully determined by the driving-point function of the port, the driving-point function can select admittance functions or impedance functions [14]. Here, taking the admittance function as an example, the driving-point function can be expressed in a rational fractional form:

$$Y(\mathrm{s}) = \frac{I_{in}(\mathrm{s})}{U_{in}(\mathrm{s})} = \frac{\sum a_i s^i}{\sum b_j s^j} \tag{1}$$

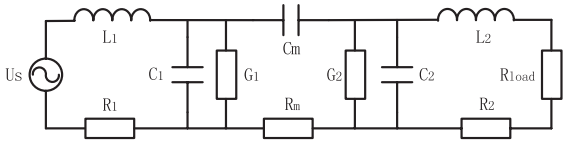


Fig. 1. Circuit model of CPT system.

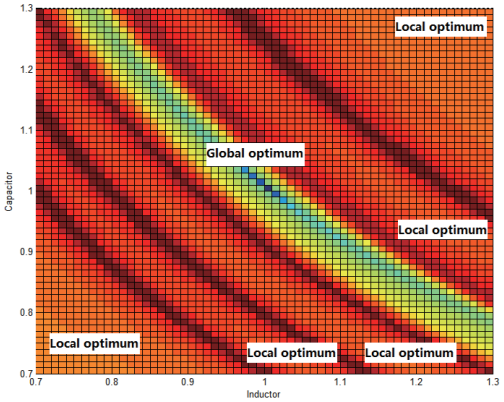


Fig. 2. Solution space map.

where, I_{in} and U_{in} represent the input current and voltage of the network port respectively, the parameters a and b in the above equation are real numbers, and the order of the numerator and denominator is determined by the topology and component parameters of the circuit.

Next, we need to fit the finite discrete points you have collected, it can generally be assumed that the noise distribution of the sampled values follows a normal distribution, and the sum of the squares of the fitting errors can be used as a criterion.

Since the fitting function is a nonlinear function, if the network is fitted directly using the second-order error minimum principle, the nonlinear least squares problem will be obtained.

$$\min \left\| \tilde{Y}(\mathrm{j}\omega_i) - Y(\mathrm{j}\omega_i) \right\|_2 \tag{2}$$

where $\tilde{Y}(\mathrm{s}) = \frac{\sum k_i s^i}{\sum d_j s^j}$ means the fitted function, k_i and d_j are the undetermined coefficients of the function.

Directly using the sum of squared errors as an optimization index, the optimization problem is that the function is not non-convex, and the fitting error has multiple local optima in the search space, as shown in Fig. 2. Therefore, directly using ordinary nonlinear optimization algorithms, such as the Levenberg-Marquardt method or the trust region method, it is difficult to converge to the optimal value for nonlinear optimization.

In order to solve the problem of a locally optimal solution of nonlinear least squares fitting algorithm in rational fractional fitting, we use the Vector Fitting algorithm [15] to solve the nonlinear least squares problem. First, transform $\tilde{Y}(\mathrm{s})$ in (2) into a fractional representation by partial fractionation,

$$\tilde{Y}(\mathrm{s}) = \frac{\sum(\mathrm{s}-\mathrm{z}_i)}{\sum(\mathrm{s}-\mathrm{p}_j)} \tag{3}$$

then multiplied by the weight $\frac{\sum(\mathrm{s}-\mathrm{p}_i)}{\sum(\mathrm{s}-\tilde{\mathrm{p}}_i)}$ to get the linearized least squares problem, in the formula, z_i and p_j represent the zero point and the pole, respectively, and $\tilde{\mathrm{p}}_i$ is expressed as the estimated pole.

$$\min\left\|(\sigma\tilde{Y})(\mathrm{j}\omega_i) - Y(\mathrm{j}\omega_i)\sigma(\mathrm{j}\omega_i)\right\|_2 \tag{4}$$

where $(\sigma\tilde{Y})(\mathrm{s}) = \frac{\sum(\mathrm{s}-\mathrm{z}_i)}{\sum(\mathrm{s}-\mathrm{p}_j)}$, $\sigma(\mathrm{s}) = \frac{\sum(\mathrm{s}-\mathrm{p}_i)}{\sum(\mathrm{s}-\tilde{\mathrm{p}}_i)}$. Therefore, the Vector Fitting algorithm can be used to fit the driving-point function. After using the Vector Fitting algorithm to fit the system's driving-point function, we need to find actual circuit parameters from the function expression. In the CPT system, since the topology of the matching circuit is mostly a ladder network structure, the Cauer synthesis method [16] can be used to get the synthesis of the circuit network. The driving-point function expression of the system regarding the circuit component is obtained as follows:

$$Y(\mathrm{s}) = \cfrac{1}{L_1 s + R_1 + \cfrac{1}{C_1 s + G_1 + \cfrac{1}{\cfrac{1}{C_m s} + R_m + \cfrac{1}{C_2 s + G_2 + \cfrac{1}{L_2 s + R_2 + R_{load}}}}}} \tag{5}$$

Expand (5) to get the admittance function expression of the (1), the highest order of the obtained molecular terms is 4 times, and the denominator term is 5 times, as shown in (6).

$$Y(\mathrm{s}) = \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{6}$$

Using Vector Fitting algorithm as a rational fractional fitting algorithm, Cauer synthesis method is used as a network synthesis method to identify the parameters in the circuit, then the correlation coefficients in (6) can be obtain derived, which means that the effective parameters of the actual circuit are obtained.

To sum up, the input parameter identification of the CPT system consists of two parts:

1) Fitting of driving-point function. By applying the excitation and measuring the system response, the external characteristics of the network in the form of the driving-point function are obtained by fitting.
2) Integration of network parameters. According to the expression of the driving-point function, the realization of the circuit network in the corresponding topology is obtained, take this implementation value as an estimate of the parameter.

Through simulation, the parameter identification results under noiseless sampling are shown in TABLE I.

According to the simulation experiment under the noise, if we want to achieve 10% estimation error in the experiment, the sampled value noise needs to be higher than 70dBm, as shown in Fig. 3, where shows the relationship between the error rate of the identification parameters and the noise. It can be clearly seen from the Fig. 3 that the sensitivity of Cm and R_{load} to noise is higher than other parameters, and once the noise exceeds 70dBm, the identification error rate of R_{load} will exceed 10%.

TABLE I
NOISELESS LOSSY MODEL IDENTIFICATION RESULTS

Circuit Parameters	Loss Model Identification Results When R_m = 100 Ω	Model Parameters
L_1 (H)	8.2240e-005	82.24 uH
R_1 (Ω)	3.4401	3.44 Ω
C_1 (F)	2.8800e-010	288 pF
G_1 (S)	1.0000e-005	10e-6S
C_m (F)	1.9995e-011	20 pF
R_m (Ω)	1.0003e+002	100 Ω
C_2 (F)	2.8801e-010	288 pF
G_2 (S)	9.9966e-006	10e-6S
L_2 (H)	8.2277e-005	82.24 uH
R_{load}+R_2 (Ω)	36.5561	36.54 Ω

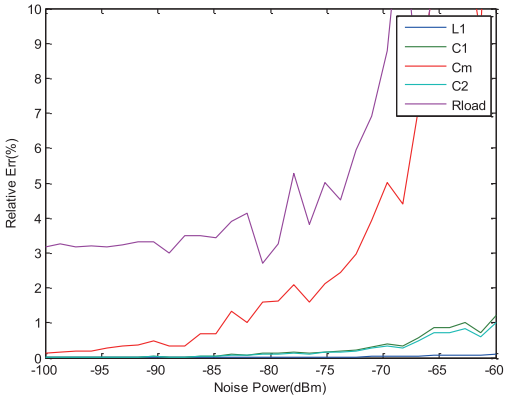


Fig. 3. Identification error of partial lossless model under different sampling noise power.

III. PARAMETER IDENTIFICATION ALGORITHM UNDER CONSTRAINTS

Taking a CPT system with double-sided LC matching as an example, assuming that the inductance L1, L2, coupling capacitance Cm, and load resistance R_{load} in the circuit parameters are unknown, the circuit model is shown in Fig. 4. The transmitter resistor and capacitor parameters are known to form a two-port circuit Np, the receiver resistor and capacitor parameters are known to form a two-port circuit Ns.

In this algorithm, the unknown variables are modeled in a two-port network, the circuit is decomposed according to the unknown part and the known part, and the unknown parts are separately solved in an iterative manner, and at the same time, the rational fractional fitting method is used, the fol-

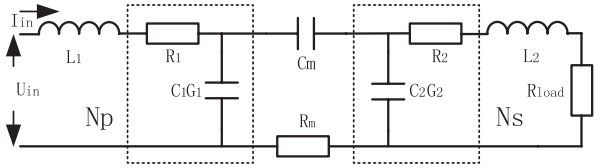


Fig. 4. The parameter identification model under the constraint of double-sided LC matched CPT system.

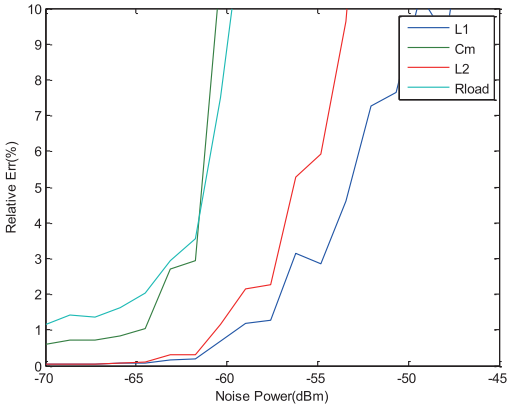


Fig. 5. Identification error of identification algorithm under constraint with different sampling noise power.

lowing fitting algorithm can be designed.

1) Given the initial value of load resistance and coupling capacitance $\tilde{R}_{load}$, $\tilde{C}_m$ and the inductance $\tilde{l}_1$, $\tilde{l}_2$ at both ends.
2) Taking $\tilde{R}_{load}$, $\tilde{C}_m$ and $\tilde{l}_2$ as known variables, the back-end circuit of the inductor l_1 is known, and the inductor l_1 is fitted and solved under the back-end constraint as a new front-end inductance estimated value $\tilde{l}_1 = l_1$.
3) Taking $\tilde{R}_{load}$, $\tilde{l}_1$ and $\tilde{l}_2$ as known variables, the front and back-end circuits of the coupling capacitor C_m are known, and the coupling capacitor C_m is fitted and solved under the front and rear end constraints as a new coupling capacitor estimate $\tilde{C}_m = C_m$.
4) Taking $\tilde{l}_1$ and $\tilde{C}_m$ as known variables, the front-end circuits of the inductor and load resistors l_2 and R_{load} are known, and the inductance and load resistance l_2 and R_{load} are fitted and solved under the front-end constraints as a new coupling capacitor estimate $\tilde{l}_2 = l_2$, $\tilde{R}_{load} = R_{load}$.
5) If the fitting error is less than the threshold, it ends, otherwise, it returns to 2).

In the above algorithm, by modeling the unknown variables in the form of a two-port network, the circuit is decomposed according to the position part and the known part, and the unknown parts are separately solved in the form of iterations.

Though the simulation experiment under the noise, we can see that if we want to achieve 10% estimation error in the experiment, the sample value noise needs to be higher than 60dBm, as shown in Fig. 5, compared to the identification algorithm based on spectrum information without constraint, the new algorithm can reduce signal-to-noise ratio requirements of approximately 10 dB.

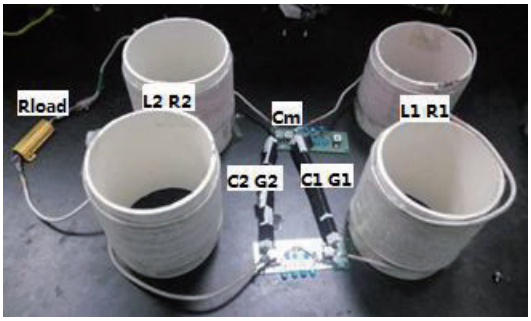


Fig. 6. Double-sided LC matched CPT system model circuit physical map.

TABLE II
PARAMETER IDENTIFICATION EFFECT OF PARAMETER IDENTIFICATION ALGORITHM ON MODEL PHYSICAL CIRCUIT

Circuit Parameters	Constraint Model Identification Results	Component Measurement
L_1	7.6887e-005	77.1773 uH
R_1	-	3.6928 Ω
C_1	-	265.7394 pF
G_1	-	5e-6S
C_m	2.0501e-011	20 pF
R_m	-	-
C_2	-	252.2711 pF
G_2	-	6e-6
L_2	7.8756e-005	78.8456 uH
R_2	-	3.43 Ω
R_{load}	20.9163	20 Ω

IV. MODEL CIRCUIT PARAMETER IDENTIFICATION EXPERIMENT

In order to verify the applicability of the algorithm in the actual circuit parameter identification. According to the circuit model of the double-sided LC matching coupling capacitor shown in Fig. 1, the circuit physical map is shown in Fig. 6. The electronic system is used to build the circuit system and the equivalent model physical circuit is made.

A hollow flat wound coil made of 600 strands x 0.1 mm Litz wire is used in the circuit as an inductor in the matching circuit. A plurality of EPCOS film capacitors with a capacitance of 1nF are used in series as the capacitance in the matching circuit, and the coupling capacitance is replaced with a 15pF ceramic capacitor. The actual parameters of the above components were measured using an Agilent E4980A LCR digital bridge, and the actual parameters of the system were as shown in the measured values of the components in TABLE II.

Comparing the constraint model fitting results with the measurement results, the constraint model is constrained by the measured values of the known components, and the identification results are close to the actual circuit parameters, as shown in Fig. 7, where the red line is the result of the vector network analyzer measurement, while the green line

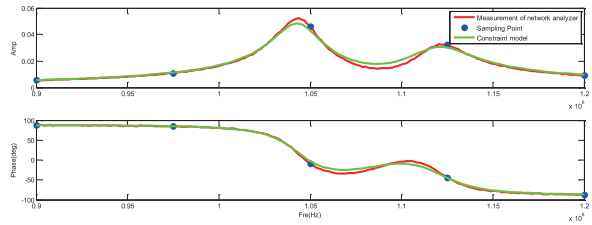


Fig. 7. Comparison of the results of the constraint model fitting and the measurement results.

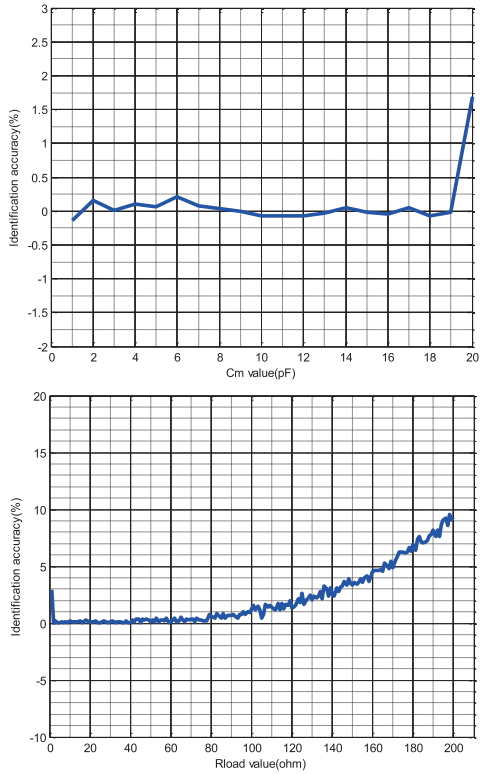


Fig. 8. (a) Relationship between coupling capacitance change and identification accuracy. (b) Relationship between load resistance change and identification accuracy.

is the result of fitting the five blue sampling points using our proposed identification algorithm. It can also be seen from TABLE II that the constraint model can accurately identify the value of the circuit component and the identification accuracy is less than 10%. At the same time, the noise is set to 65dBm. By changing the value of the load resistance and keeping the other parameters of the circuit unchanged, a curve about the load value and the identification accuracy can be obtained, as shown in Fig. 8(b). Keeping the noise at 65dBm, by changing the value of the coupling capacitor and keeping the other parameters of the circuit unchanged, a curve about the coupling capacitance value and the identification accuracy can be obtained, as shown in Fig. 8(a).

V. Conclusion

This paper proposes a method of parameter identification based on spectrum information, by adding known parameters of the circuit, the accuracy and noise tolerance of the identification algorithm are improved. In order to verify the proposed algorithm, this paper firsts builds a double-sided LC matched CPT system model physical circuit as shown in Fig. 6. Then, the vector network analyzer is used to collect the spectrum information of the circuit, and the parameter identification algorithm is applied on it. The final result verifies that the parameter identification algorithm based on spectrum information can achieve good results, which not only can effectively identify the unknown parameters in the system model, but also achieve the identification result with less than 10% accuracy.

References

[1] J. T. Boys and G. A. Covic, "The inductive power transfer story at the university of auckland," *IEEE Circuits and Systems Magazine,* vol. 15, no. 2, pp. 6-27, May 2015.

[2] A. Karalis, J. D. Joannopoulos, and M. Soljačić, "Efficient wireless non-radiative mid-range energy transfer," *Annals of Physics*, vol. 323, no. 1, pp. 34-48, Jan. 2008.

[3] C. H. Li, X. M. zhao, C. L. Liao, and L. F. Wang, "A graphical analysis on compensation designs of large-gap CPT systems for EV charging applications," *CES Transactions on Electrical Machines and Systems,* vol. 3, no. 2, pp. 232-242, Jul. 2018.

[4] C. Mi, "High power capacitive power transfer for electric vehicle charging applications," in *6th International Conference on Power Electronics Systems and Applications (PESA)*, 2015, pp. 1-4.

[5] J. Dai and D. C. Ludois, "Wireless electric vehicle charging via capacitive power transfer through a conformal bumper," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 3307-3313.

[6] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A double-sided LCLC-compensated capacitive power transfer system for electric vehicle charging," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6011-6014, Nov. 2015.

[7] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A CLLC-compensated high power and large air-gap capacitive power transfer system for electric vehicle charging applications," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC),* 2016, pp. 1721-1725.

[8] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A double-sided LC-compensation circuit for loosely coupled capacitive power transfer," *IEEE Transactions on Power Electronics,* vol. 30, no. 2, pp. 1633-1643, Feb. 2018.

[9] F. Lu, H. Zhang, and C Mi, "A two-plate capacitive wireless power transfer system for electric vehicle charging applications," *IEEE Transactions on Power Electronics,* vol. 33, no. 2, pp. 964-969, Feb. 2018.

[10] H. Y. Zhang, "Load and mutual inductance identification method of ICPT system based on switching capacitors," Chongqing University, 2015.

[11] X. Dai, Y. Sun, and C. Tang, "Dynamic parameters identification method for inductively coupled power transfer system," *IEEE International Conference on Sustainable Energy Technologies*, Dec. 2010.

[12] Z. H. Wang, Y. P. Li, and Y. Sun, "Load detection model of voltage-fed inductive power transfer system," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5233-5243, Nov. 2013.

[13] J. F. Li, C. L. Liao, and L. F. Wang, "Decoupling method of maximum efficiency and transferring power for electric vehicle wireless charging system via LCCL circuit," *Transactions of China Electrotechnical Society,* pp. 199-203, 2010.

[14] V. Belevitch, "Summary of the history of circuit theory," *Proceeding of the Ire,* vol. 50, no. 5, pp.848-855, May 1962.

[15] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions on Power Delivery,* vol. 14, no. 3, pp. 1052-1061, Jul. 1999.

[16] W. Cauer, "Die Verwirklichung von Wechselstromwiderständen vor-

geschriebener Frequenzabhängigkeit," *Archiv Für Elektrotechnik,* vol. 17, no. 4, pp. 355-388, Apr. 1926.

Chen Chen received the B.E. degree in automation from Tianjin Polytechnic University, Tianjin, China, in 2016. He then completed studies in power electronics and electric drives at the University of Chinese Academy of Sciences, Beijing, China. He is currently working towards the M. S. degree in power electronics and electric drives at the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. His research topic focuses on wireless power transfer for electric vehicle charging and aided inertial navigation system for vehicles.

Chenhui Li received the B.E. degree in automation from Tsinghua University, Beijing, China, in 2015. He received the M.S. degree in power electronics and electric drives at the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2018. His research topic focuses on wireless power transfer for electric vehicle charging. He is working on the high power capacitive power transfer through air-gap distance and measurement technology of the wireless power transfer system.

Chenglin Liao received the Ph.D. degree in power machinery and engineering from Beijing Institute of Technology, Beijing, China, in 2001. He then spent two years as a Postdoctoral Researcher with Tsinghua University, Beijing, China. He is currently the Deputy Director of the Department of Vehicle Energy System and Control Technology, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. He had been involved in research on battery management systems, vehicle control, and wireless charging systems for electric vehicles for the past nine years at the Institute of Electrical Engineering. His research interests include the development of high-power wireless charging systems for commercial electric vehicles.

Lifang Wang received the Ph.D. degree in automobile engineering from Jilin University, Jilin, China, in 1997. She then joined the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. During the Chinese 10th five-year plan (2001–2005), she was a member of the National Specialist Group of the Key Special Electric Vehicle Project of the National 863 Program, and she was the Head of the 863 Special EV Project Office. She is currently the Director of the Department of Vehicle Energy System and Control Technology, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. She is also the Vice Director of the Key Laboratory of Power Electronics and Electric Drives, Chinese Academy of Sciences. Her research interests include electric vehicle control systems, EV battery management systems, wireless charging systems for EVs, electromagnetic compatibility and smart electricity use. She has directed more than 15 projects in these fields and has published more than 60 papers and 30 patents.

Adaptive DC-Link Voltage Control of LLC Resonant Converter

Li-Chung Shih, Yi-Hua Liu, and Yi-Feng Luo

***Abstract*—In this study, an adaptive DC-link voltage control of a two-stage switching power supply with LLC resonant converter is proposed. With this control method, the frequency variation range can be reduced and the conversion efficiency under different load conditions can be improved compared with the conventional variable frequency control technique. By operating the LLC resonant converter near its resonant frequency, circulating loss as well as the conduction loss can be reduced and optimal design of LLC resonant converter can be made possible. Moreover, no additional auxiliary circuits are required for the proposed method. The operational principle of the proposed control scheme is verified with a 350 W prototyping circuit. The switching-frequency-variation range is reduced from 12 to 4 kHz and the efficiency is improved from 89.4 % to 90.2 % at full load.**

***Index Terms*—Adaptive DC-link control, LLC resonant converter, two-stage switching power supply.**

I. Introduction

With the prevalence of the Internet and advancements in telecommunication technology, demand for power supply fields, such as server and telecom power supplies, has increased. Additionally, consumers have high requirements for power supply efficiency, volume, power density, and reliability [1]-[3]. Regarding the application of server and telecom power supplies, two-stage switching power supply (SPS) remains the mainstream architecture [4], [5]. In addition, two-stage SPS can also be employed in plug-in electrical vehicle (PEV) applications. Power factor correction (PFC) is usually the first stage of two-stage SPS, allowing the input current to become sinusoidal and in phase with the input voltage to increase the usage of mains electricity. The PFC stage usually utilizes a typical boost converter architecture that converts alternating current (AC) mains electricity to high-voltage direct current (DC). The second stage utilizes a DC-DC converter architecture to provide isolation as well as a stable output voltage. For two-stage SPS, digital signal controllers have increasingly been employed because of advancements in their functionalities. The block diagram for two-stage digital SPS is shown in Fig. 1.

Because most conventional DC-DC converters do not possess soft switching mechanisms [6], power supply efficiency is

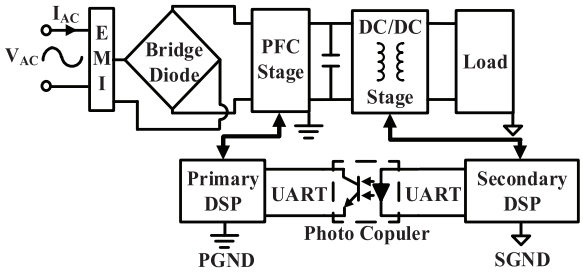


Fig. 1. Block diagram of a two-stage digital SPS.

difficult to improve. Hence, current DC-DC converters typically use the phase shift full bridge (PSFB) converter or LLC resonant converter, which has soft switching characteristics. PSFB converters can achieve zero voltage switching (ZVS) and are suitable for medium- and high-power applications; therefore, they are often used in the DC-DC converters of server, telecom or PEV power supply systems. Compared with conventional full bridge converters, PSFB converters have higher efficiency; however, PSFB converters exhibit problems such as difficulty in achieving ZVS at light load, duty cycle loss, circulating-current loss, and the parasitic ringing phenomenon [7]-[10].

Compared with PSFB converters, LLC resonant converters can not only achieve ZVS on the primary side but also attain zero current switching (ZCS) on the secondary side. In addition, problems related to the circulating current on the primary side of the LLC resonant converter are less severe. Thus, LLC resonant converters are more efficient than PSFB converters and have gradually become more prevalent for DC-DC converter applications. However, LLC resonant converters possess deficiencies. Generally, the optimal performance of an LLC resonant converter occurs when the switching frequency equals the resonant frequency [11]-[16]. However, this is difficult to achieve without adding mechanisms such as changes to the resonant tank parameters [12], [13] or modulation of the LLC resonant converter input voltage [14]-[16]. In addition, the LLC resonant converter relies on a frequency control mechanism to achieve voltage regulation. In conditions of improper design or applications where a wide input/output range is required [17]-[20], the switching frequency of LLC resonant converter may vary excessively, causing inefficiency and even leading to problems in designing magnetic components.

Numerous studies have adopted measures to enhance the overall efficiency of LLC resonant converters. A dual-transformer strategy was utilized in [19] to handle relatively wide input voltage ranges. Compared with the conventional LLC resonant converter, this design developed more operating modes, such as the increased flexibility to minimize the magnetizing

Manuscript received July 30, 2018. This work was financially supported by the Taiwan Building Technology Center from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education in Taiwan.

The authors are with the Department of Electrical Engineering, National Taiwan University of Science and Technology (e-mail: yhliu@mouse.ee.ntust.edu.tw; d10102204@mail.ntust.edu.tw; YF.Luo@mail.ntust.edu.tw).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00018

current and reducing copper and iron loss from the transformer to enhance overall efficiency; however, the auxiliary circuit, winding of the dual transformers, and two rectification output stages complicate the circuit. An auxiliary LC circuit (containing an inductor and a capacitor) was used in [21], which functioned as a variable inductor, providing substantial magnetizing inductance at all times according to the switching frequency to reduce the circulating current of the LLC resonant converter, thereby improving the overall efficiency. Nonetheless, the transformer size becomes larger than that of a conventional LLC resonant converter if the LC auxiliary coil should be winded into the transformer. The research team in [22] modified the design of the transformer and the winding method to improve the overall efficiency of the LLC resonant converter; however, the improvement was limited. In [23], researchers suggested a dynamic adjustment of the dead time (DT) of LLC resonant converters to enhance overall efficiency; this means DT is short when the load is large, and vice versa. This method detected the center point voltage between the high side and low side MOSFET to determine the optimal timing for ZVS. However, this DT adjustment method is only suitable for region 1 operation of the LLC resonant converter, in which the frequency is higher than the resonant frequency. If employed in other regions of the LLC resonant converter, this method improves efficiency only to a limited extent. When operating in a region with a frequency lower than the resonant frequency, the resonant current value that enables the MOSFET to achieve ZVS is irrelevant to load level but is related to the value of the magnetizing inductance.

Studies have improved LLC resonant converter efficiency by adjusting LLC input voltage to keep the switching frequency close to the resonant frequency. This methodology comprises three methods: The first method controls LLC resonant converter in an open loop manner [14]-[16]; this method adjusts the input voltage by detecting variations of the output voltage, ensuring that the input-to-output voltage gain of LLC resonant converter stays at 1, as shown in Fig. 2.

The first method is often employed in systems with a variable output voltage, such as battery charging, where an LLC resonant converter only has to provide system isolation and high-efficiency voltage conversion. Additionally, this type of system does not need to consider the transient response.

The second method lets the switching frequency track the resonant frequency [3]. When the switching frequency of the LLC resonant converter deviates from the resonant frequency, step-size adjustment is used to adjust the input voltage step by step. This process continues until the switching frequency falls into the setting frequency range, as shown in Fig. 3. However, the step-by-step adjustment of the PFC's input voltage may cause the PFC's output voltage to change frequently, which is unfavorable for regulating voltages at subsequent stages, and the output voltage may oscillate.

The third method is the use of a variable resonant inductor [13], which engender unsaturated, partially saturated, and saturated resonant inductance values according to various loads and operating points. In addition to the difficulty in controlling the saturation point, this method is unfavorable for realizing commercialization of mass production. The block diagram regarding the function of this architecture is shown in Fig. 4.

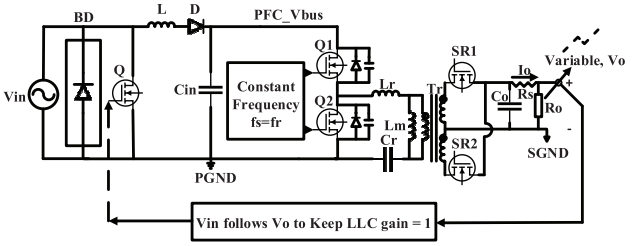


Fig. 2. Block diagram of the first method.

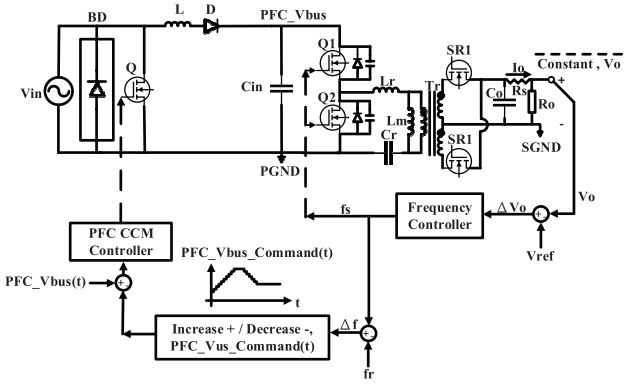


Fig. 3. Block diagram of the second method.

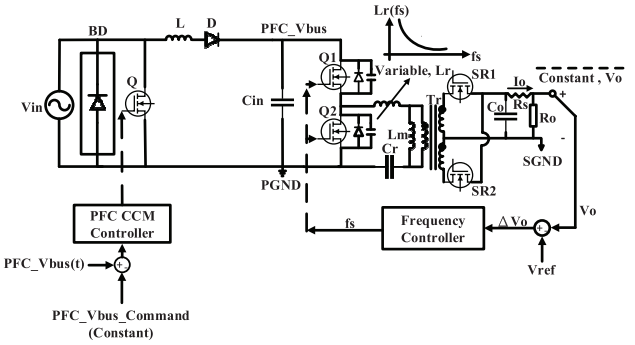


Fig. 4. Block diagram of the third method.

This study proposed a novel method for improving efficiency that does not require changes in system architecture and resonant tank components. The proposed method simply utilizes the LLC resonant converter's voltage gain and the switching frequency's open loop relationship under various loads to rapidly estimate the required input voltage compensation, enabling the switching frequency to stay consistent with the resonant frequency. When the load varies, the variable frequency control of the conventional LLC resonant converter changes the switching frequency to alter the voltage gain to compensate for the drop (rise) in the output voltage caused by the increase (decrease) of the load. If the input voltage can be altered while the load changes, voltage gain can thus be changed to achieve optimal operational efficiency under the premise of little variation in the switching frequency. The proposed method is presented in Fig. 5. Because the proposed method does not require a step-by-step

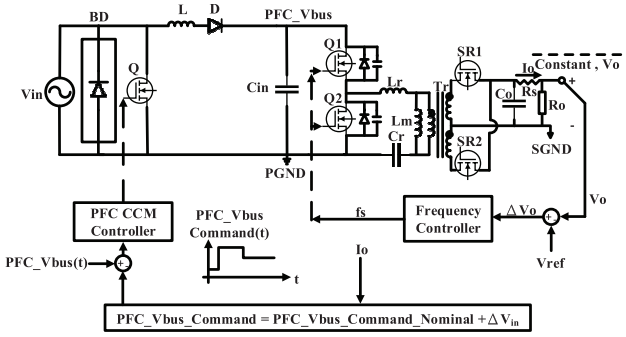


Fig. 5. Block diagram of the proposed method.

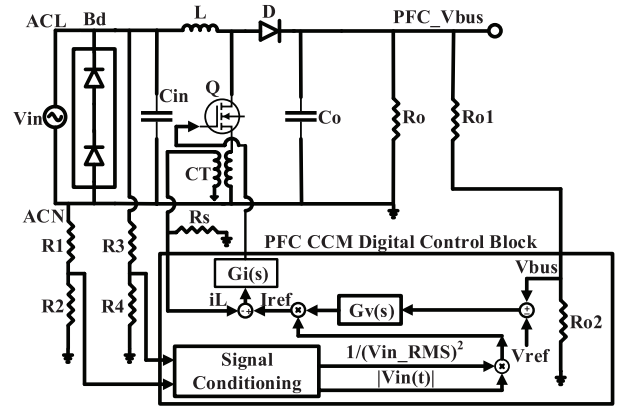


Fig. 6 Block diagrams of the PFC stage utilized in this study.

adjustment mechanism, the output response is relatively rapid. Compared with the variable frequency control of a conventional LLC resonant converter, the proposed technology can increase efficiency by 0.8% at full load.

This paper is organized as follows. Section II describes the relationship between the conversion efficiency and the output voltage of PFC. Section III presents the loss analysis of LLC resonant converter operating at the resonant frequency. Section IV derives the proposed control technique. Section V reports the experimental results. Section VI draws some conclusions.

II. The Relationship Between the Efficiency and Output Voltage of the PFC Stage

In this paper, an adaptive DC-link voltage control technique is proposed to keep the switching frequency of the LLC resonant converter close to the designed resonant frequency. That is, the output voltage of the PFC stage should be adjustable. In this subsection, the relationship between the conversion efficiency and the output voltage value of the PFC stage is investigated. Fig. 6 shows the block diagram of the PFC stage used in this study.

From Fig. 6, the utilized PFC is a boost converter operated in average current mode [24], [25]. The input voltage range of the utilized 380 W PFC stage is from 90 V_{AC} to 264 V_{AC} with AC line frequency ranges from 47 Hz to 63 Hz, the nominal output voltage is 380 VDC (programmable), and the full load current is 0.92 A. According to [26], the losses of the power MOSFET

TABLE I
Key Components of the Utilized PFC Stage

Key Components	Manufacturer and Parts	Specifications
Bridge diode (Bd)	Fairchild, GBU8J	V_{RRM} : 600 V, $I_{F(AV)}$: 8 A
MOSFET (Q)	Infineon, IPP60R199CP	V_{DS}: 650 V, $R_{DS(on)}$:0.199 Ω, I_D:9 A
Freewheeling diode (D)	Cree, C3D10060G	V_{RRM}: 600 V, I_F:10 A
Output Capacitor (Co)	Panasonic, ECOS2WP221CX	450 V/220 μF
Controller	TI, UCD3138	Integrated Digital Controller

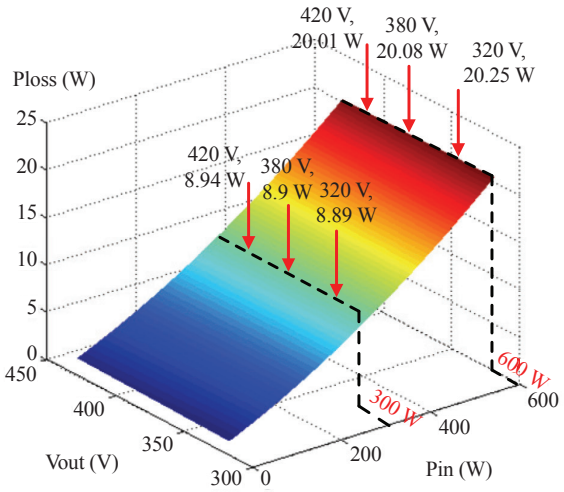


Fig. 7. Total losses of the PFC stage utilized in this study.

Q, freewheeling diode D, and output capacitor C_o relate to the value of the output voltage V_o. TABLE I shows the key components of the implemented PFC stage. Using the parameters in TABLE I, total losses of the PFC stage can be obtained [26].

Fig. 7 shows the calculated total losses of the PFC stage under different output voltage V_o and power level P_{in}. From Fig. 7, the power losses become larger/smaller when V_o increases under 300 W/600 W power level. Nonetheless, it can also be observed from Fig. 7 that the variation of power losses for the full voltage swing (V_o = 320 V to V_o = 420 V) is rather small (0.045 W (0.015 %) for 300 W level and -0.25 W (0.042 %) for 600 W level). Therefore, changing the output voltage of PFC will have little effect on the overall efficiency.

III. Optimal Operating Point and Loss Analysis of LLC Resonant Converter

A. Comparison of Three Operating Points of the LLC Resonant Converter

The key waveforms of the resonant current of LLC converter operating at different switching frequencies are depicted in Fig. 8. If the switching frequency is lower than the resonant frequency as shown in Fig. 8(a), a large circulating current exists in the

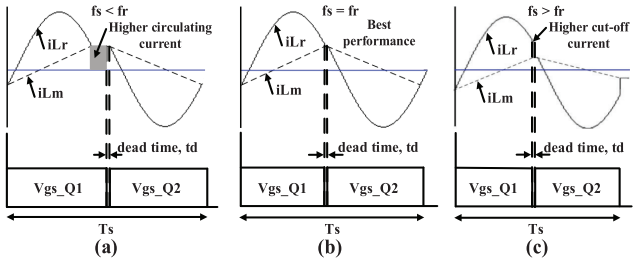


Fig. 8. Key waveforms of the resonant current i_{Lr} of LLC resonant converter operating under different switching frequency.

TABLE II
COMPARISON OF THE LLC RESONANT CONVERTER OPERATING UNDER DIFFERENT SWITCHING FREQUENCY

LLC Performances	fs < fr	fs = fr	fs > fr
Turn on loss of primary MOSFET	ZVS	ZVS	ZVS
Turn off loss of primary MOSFET	Low	Low	High
Circulating current in the primary side	High	Low	Medium
Secondary diode	ZCS	ZCS	No
Conduction loss	High	Low	Medium
Switching loss	Low	Low	High
Harmonics	Low	Low	High
Overall performance	Medium	Best	Medium

resonant tank, and it will cause high conduction loss. When the switching frequency equals the resonant frequency, the switching loss and conduction loss are reduced as seen in Fig. 8(b). When the switching frequency is higher than the resonant frequency, the MOSFETs are turned off with higher current as shown in Fig. 8(c); hence, the switching loss increases. TABLE II shows the comparison of the LLC resonant converter operating under different switching frequency [14]. From TABLE II, the LLC resonant converter achieves its best efficiency when operating at the resonant frequency.

B. Loss Analysis for LLC Resonant Converter Operating at the Resonant Frequency

For the proposed control technique, the DC-link voltage will be adjusted to keep the switching frequency of LLC resonant converter near its resonant frequency. Therefore, loss analysis for LLC resonant converter operating at its resonant frequency will be performed first. For the LLC resonant converter utilized in this study, as shown in Fig. 9, the loss model for each component will be briefly derived and described as follows:

1) Losses of MOSFET Q1 and Q2

Conduction loss of MOSFET Q1 and Q2 can be expressed as [15]:

$$P_{LLC-cond} = I_{p-rms}^2 \cdot R_{DS\_on} = \left(\frac{2P_o}{V_o} \sqrt{\frac{R_L^2 T_s^2}{32n^4 L_m^2} + \frac{\pi^2}{8}} \right)^2 \cdot R_{DS\_on} \quad (1)$$

where I_{p_rms} is the RMS current of the primary side, transformer

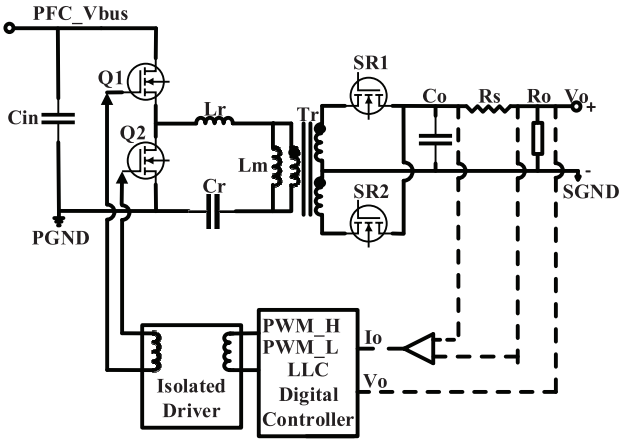


Fig. 9. LLC resonant converter utilized in this study.

turns ratio $n = N_p/N_s$, N_p is the number of turns on the primary side, N_s is the number of turns on the secondary side, L_m is the magnetizing inductance, V_o is the output voltage, R_L is the equivalent load resistance and T_s is the switching period.

Due to its ZVS nature, the turn-on loss of Q1 and Q2 can be neglected. However, there still exists a turn-off loss. The turn-off loss of MOSFETs can be depicted as [14]

$$P_{LLC-sw\_off} = 2\left(\frac{I_{peak}^2 t_f^2 f_s}{48C_{oss}}\right) = \frac{I_{peak}^2 t_f^2 f_s}{24C_{oss}} \quad (2)$$

where I_{peak} is the peak value of the magnetizing current, t_f is the rise time of the MOSFET, f_s is the switching frequency, COSS is the output capacitance of MOSFET.

2) Losses of the Isolation Transformer

According to [31], the AC-to-DC resistance ratio $F_{R\_n\_Tr}$ can be calculated by Dowell's equation, as shown in (3)

$$\begin{aligned} F_{R\_n\_Tr} &= \frac{R_{ac\_Tr}}{R_{dc\_Tr}} \\ &= X_n \frac{\sinh 2X_n + \sin 2X_n}{\cosh 2X_n - \cos 2X_n} + 2X_n \frac{m^2 - 1}{3} \frac{\sinh X_n - \sin X_n}{\cosh X_n - \cos X_n} \end{aligned} \quad (3)$$

where $F_{R\_n\_Tr}$ is the AC-to-DC resistance ratio at *nth* harmonic frequency, R_{ac_Tr} and R_{dc_Tr} are the AC and DC resistance of the transformer, respectively. $X_n = h/\delta_n$ is the ratio of wire thickness h and the skin depth of *nth* harmonic current, m is the layer number.

Hence, the AC copper loss of primary and secondary side can be obtained by summing the losses from DC to *nth* harmonics.

$$P_{Copper\_pri} = \sum_{n=0}^{n} F_{R\_n\_pri} R_{dc} \cdot I_{RMS\_pri}^2 \quad (4)$$

$$P_{Copper\_sec} = \sum_{n=0}^{n} F_{R\_n\_sec} \cdot R_{dc} \cdot I_{RMS\_sec}^2 \quad (5)$$

From (4) and (5), the total copper loss of the transformer can be derived as:

$$P_{Copper\_T_r} = P_{Copper\_pri} + P_{Copper\_sec} \tag{6}$$

The core loss of the transformer can be calculated using the empirical Steinmetz equation [27], [28], as shown in (7):

$$P_{Core} = K_{core} \cdot f^{\alpha} \cdot \Delta B_{Tr}{}^{\beta} \cdot V_e \tag{7}$$

where K_{core} is the Steinmetz coefficient of the core, V_e is the volume of the core and ΔB_{Tr} is the flux swing of the transformer and can be calculated as:

$$\Delta B_{Tr} = \frac{V_{LM} \cdot D \cdot T_s}{N_p \cdot A_e} = \frac{nV_o \cdot T_s}{4 \cdot N_p \cdot A_e} \tag{8}$$

where V_{LM} is the voltage of magnetizing inductance, D is the duty ratio, T_s is the switching period, A_e is the effective cross-sectional area of the core.

3) Losses of the Resonant Inductor

The losses in the resonant inductor include copper loss and core loss, and can be obtained as [14], [31]:

$$P_{Copper\_Lr} = \sum_{n=0}^{n} F_{R\_n\_Lr} \cdot R_{dc\_Lr} \cdot I_{Lr}{}^2 \tag{9}$$

where the AC-to-DC resistance ratio $F_{R\_n\_Lr}=R_{ac\_Lr}/R_{dc\_Lr}$, R_{ac_Lr} and R_{dc_Lr} are the AC and DC resistance of the resonant inductor, respectively. I_{Lr} is the RMS value of the resonant inductor current.

Similarly, the core loss of the resonant inductor can be obtained using the empirical Steinmetz equation [14], [27], [28], as depicted in (10)

$$P_{Core\_Lr} = K_{core\_Lr} \cdot f^{\alpha} \cdot \Delta B_{Lr}{}^{\beta} \cdot V_{e\_Lr} \tag{10}$$

where K_{core_Lr} is the Steinmetz coefficient of the resonant inductor, V_{e_Lr} is volumn of the resonant inductor, and ΔB_{Lr} is the flux swing of the resonant inductor, as shown in (11)

$$\Delta B_{Lr} = \frac{L_r}{n_{Lr} A_{e\_Lr}} \sqrt{\left(\frac{nV_o T}{4L_m}\right)^2 + \left(\frac{\pi V_o I_o}{2V_{dc}}\right)^2} \tag{11}$$

where n_{Lr} is the number of turns on the resonant inductor, A_{e_Lr} is the effective cross-sectional area of the resonant inductor and V_{dc} is the input voltage of the LLC converter.

4) Losses of the Synchronous Rectifier (SR) S1 and S2

The conduction loss of synchronous rectifier can be calculated as:

$$P_{LLC\_SR\_cond} = I_{s\_rms}{}^2 \cdot R_{DS\_on} \tag{12}$$

where I_{s_rms} can be expressed as [35]

$$I_{s\_rms} = \frac{\sqrt{3}}{24\pi} \frac{V_o}{R_L} \sqrt{\frac{(5\pi^2 - 48) n^4 R_L{}^2 T_s{}^2}{L_m{}^2} + 12\pi^2} \tag{13}$$

When operating at its resonant frequency, the SR of LLC resonant converter exhibits ZCS; hence, the switching loss of SR is neglected.

5) Total Losses of the LLC Resonant Converter

Based on the above derivation, the total losses of the LLC resonant converter can be obtained by summing up the losses of each component shown in Fig. 9.

IV. Operating Principle of the Proposed Method

In this paper, a novel adaptive DC-link control technique is proposed. With this approach, the LLC resonant converter will automatically adjust its input voltage to keep the switching frequency of the LLC resonant converter close to the resonant frequency so that the conversion efficiency of the LLC resonant converter can be optimized across the whole load range. According to the First Harmonic Approximation (FHA) technique, the voltage gain of the LLC resonant converter can be expressed as:

$$M(f_n) = \frac{V_o}{V_{in} \big/ (2 \cdot n)} = \left| \frac{L_n \cdot f_n{}^2}{[(L_n + 1) \cdot f_n{}^2 - 1] + j[(f_n{}^2 - 1) \cdot f_n \cdot Q_e \cdot L_n]} \right| \tag{14}$$

where $L_n = L_m/L_r$ is the ratio of the magnetizing inductance and resonant inductance, $f_n = f_s/f_r$ is the ratio of switching frequency and resonant frequency. In (14), the quality factor Q_e can be depicted as

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} \tag{15}$$

where the equivalent load resistance R_e can be obtained as

$$R_e = \frac{8 \cdot n^2}{\pi^2} R_o = \frac{8 \cdot n^2}{\pi^2} \frac{V_o}{I_o} \tag{16}$$

Fig. 10 shows the voltage gain curves of different values of load current. From Fig. 10, the voltage gain is irrelevant to the load current if the switching frequency is fixed at the resonant frequency. However, if non-idealities such as losses in power switches, magnetics, and diodes are taken into account, the actual output voltage will vary according to the load current [36]. When load increases/decreases, the output voltage will drop/rise accordingly. Hence, a closed-loop controller is typically required to adjust the switching frequency to compensate the voltage variation. That is, to compensate for the effect of the varied load value, a conventional LLC resonant converter operates under a wide switching frequency variation range. However, wide frequency variation complicates the design of the LLC resonant converter and leads to a decrease of efficiency.

To deal with this problem, an adaptive DC-link voltage control method is proposed in this study. From (14), the output voltage under ideal condition can be expressed by:

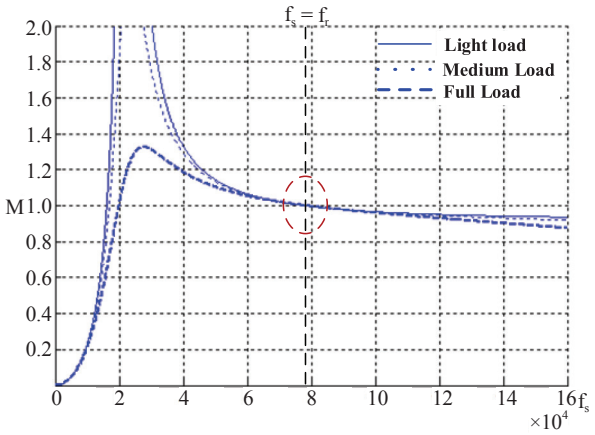


Fig. 10. Gain curves of the LLC resonant converter under different load conditions (ideal case).

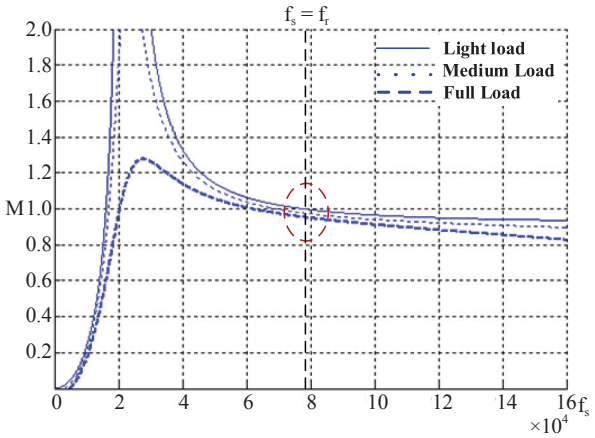


Fig. 11. Gain curves of the LLC resonant converter under different load conditions (non-ideal case).

$$V_o = \frac{V_{in}}{2 \cdot n} \cdot M = \frac{V_{in}}{2 \cdot n} \cdot \left| \frac{L_n \cdot f_n^{\,2}}{[(L_n + 1) \cdot f_n^{\,2} - 1] + j[(f_n^{\,2} - 1) \cdot f_n \cdot Q_e \cdot L_n]} \right| = \frac{V_{in}}{2 \cdot n} \cdot M(f_n, Q_e) \tag{17}$$

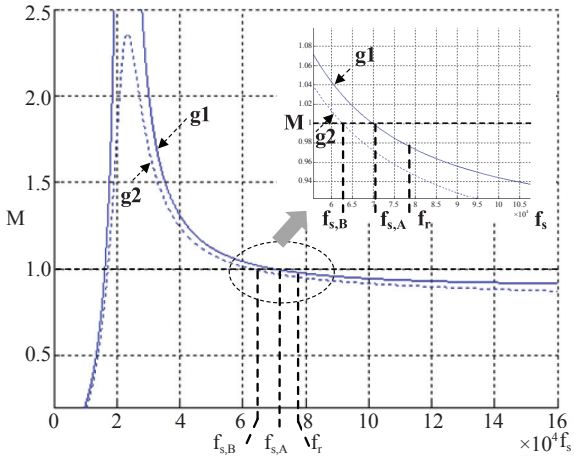
Taking all the non-idealities into consideration, the actual output voltage can be modified as:

$$V_o = \frac{V_{in}}{2 \cdot n} \cdot M(f_n, Q_e) - I_o \cdot R_T \tag{18}$$

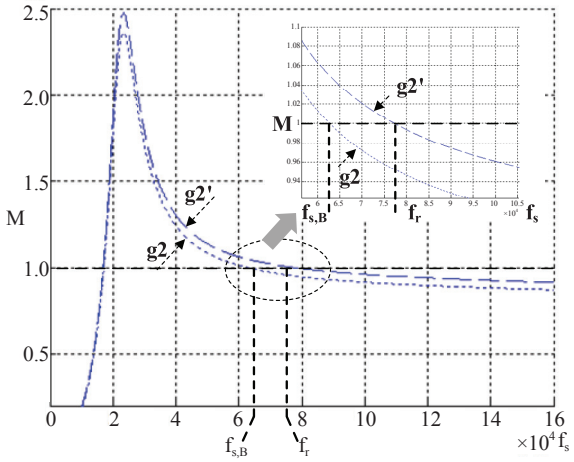
where R_T is the equivalent resistance represents the cumulative effect of all losses and can be obtained through experiments.

Fig. 11 shows the gain curve of the utilized LLC resonant converter under different load conditions when taking all the non-idealities into account. From Fig. 11, the gain value varies even when the operating frequency is fixed at the resonant frequency. Therefore, some control technique should be employed to compensate for this gain variation.

Fig. 12 shows the changes of the gain curves of the LLC resonant converter to explain the concept of the proposed control.



(a)



(b)

Fig. 12. Changes of gain curve under load variation in conventional and proposed control methods.

In conventional frequency control, when the load current varies from light load to heavy load condition, the gain curve changes from g1 (solid line) to g2 (dotted line). To maintain the output voltage, the controller adjusts the switching frequency of the main switches Q1 and Q2 from $f_{s,A}$ to $f_{s,B}$ to regulate the output voltage, as shown in Fig. 12 (a). On the other hand, when the load current changes from light load to heavy load in the proposed control, the output voltage is regulated by adjusting the input voltage (which consequently changes the gain curve) instead of the switching frequency as shown in Fig. 12 (b). That is, the gain curve changes from g2 (dotted line) to g2' (dashed line) to achieve a constant gain at the resonant frequency f_r.

The derivation of the proposed control mechanism can be explained as follows. According to (18), the output voltage variation $V_{o,\,drop}$ equals to the voltage drop across R_T, that is, $V_{o,drop} = I_o * R_T$. To compensate for this voltage drop, the required voltage variation of input voltage ΔV_{in} can be calculated as

$$\Delta V_{in} = \frac{2 \cdot n \cdot V_{o,drop}}{M(f_n, Q_e)} = \frac{2 \cdot n \cdot I_o \cdot R_T}{M(f_n, Q_e)} \tag{19}$$

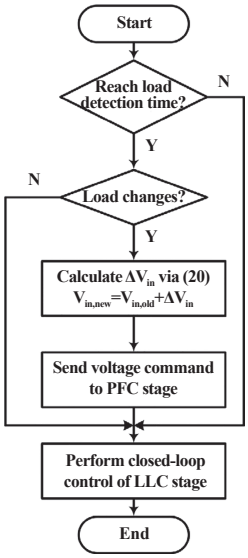


Fig. 13. Flowchart of the proposed method.

Since the gain value of the LLC resonant converter is always close to 1.0 when operating at the resonant frequency, (19) can be approximated as

$$\Delta V_{in} = 2 \cdot n \cdot I_o \cdot R_T \tag{20}$$

Fig. 13 shows the flowchart of the proposed method. At first, the controller will determine whether the load detection time has been reached. In this study, the load detection time is 0.3 second. If yes, the load current value I_o will be measured and the controller will check if the load change has occurred or not. Otherwise, only original closed-loop control will be performed. If the load level changes, the required compensation voltage can be obtained using (20). In (20), the equivalent resistance R_T which represents the cumulative effect of all losses can be obtained by operating the LLC resonant converter at the resonant frequency using open loop control and recording voltage drop value under various load conditions. By adjusting the input voltage value and hence changing the gain curve shape, switching frequency of the resonant LLC converter can be kept around its resonant frequency. Since the adaptive DC-link voltage control scheme leads to reduced frequency variation range, optimal design of the LLC resonant converter and high efficiency under all-load conditions can be guaranteed. It should be noted that the load detection time should be slower than the bandwidth of the voltage control loop of PFC stage; otherwise the proposed method may fail to perform correctly.

The block diagram of the realized two-stage SPS with adaptive DC-link voltage control is illustrated in Fig. 14. From Fig. 14, the only measured signals are the output voltage V_o and output current I_o. After calculating the required input voltage variation ΔV_{in}, this command will be sent to PFC front stage via universal asynchronous receiver transmitter (UART) and the PFC stage will adjust its output voltage accordingly. Instead of continuously adjusting the input voltage as proposed in [3], the input voltage only changes once for the proposed method each time the load changes. Hence, the transient response can be improved and the output voltage oscillation phenomenon can be avoided.

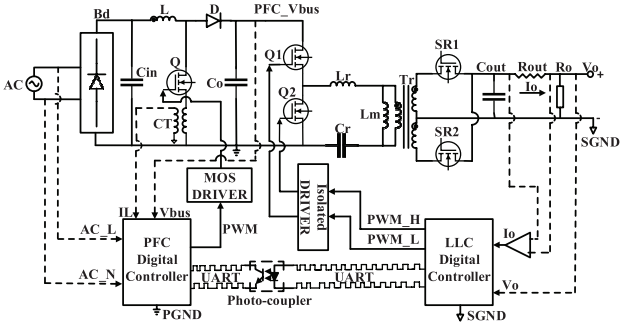


Fig. 14. Block diagram of the proposed method.

TABLE III
COMPONENTS UTILIZED IN THE IMPLEMENTED LLC RESONANT CONVERTER

Key Components	Manufacturer and Parts	Specifications
MOSFET (Q)	Infineon, SPW20N60CFD	V_{DS}: 650 V, $R_{DS(on)}$: 0.22 Ω, I_D: 20.7A
Synchronous Rectifier	Infineon, IRLB3036GPbF	V_{DS}: 60 V, $R_{DS(on)}$: 1.9 mΩ, I_D: 195 A
Transformer	Np:48, Ns:3, Ns:3	L_m: 520 μH
Output Capacitor (Co)	Nichicon, PLF1C471MD01	16 V/470 μF * 5
Controller	TI, UCD3138	Integrated Digital Controller

V. EXPERIMENTAL RESULTS

In order to validate the correctness and effectiveness of the proposed method, a 350 W prototyping circuit is first constructed. The input voltage range of the implemented LLC resonant converter is from 350 V_{DC} to 420 V_{DC}, the output voltage is fixed at 12 V_{DC} and the full load current is 29 A. Table III shows the specific components utilized in the implemented prototyping circuit and their corresponding values.

Fig. 15 displays the procedure for obtaining the equivalent resistance R_T. In Fig. 15, the realized LLC resonant converter operates at the resonant frequency using open loop control, and the load current changes from 1 A to full-load 29 A with an interval of 1 A. After measuring the voltage variation $V_{o,drop}$, R_T can be approximated by calculating the slope of the $V_{o,drop}$ versus I_o curve. In this study, R_T = 37.9 mΩ when load current is lower than 5 A and R_T = 15.0 mΩ when load current is higher than 5 A, as shown in Fig. 15.

Fig. 16(a) and (b) shows the key waveforms of the conventional and proposed converters in full load condition, respectively. From Fig. 16, the operating frequency of the conventional LLC resonant converter is 57.25 kHz and the operating frequency of the proposed method is 78.64 kHz, which reduces

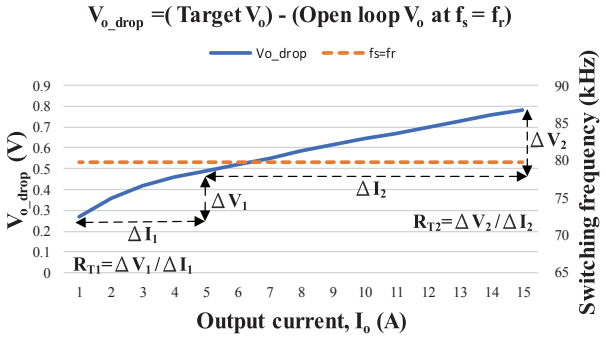
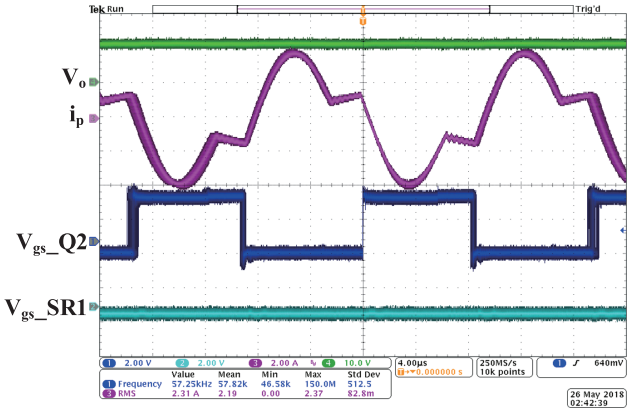
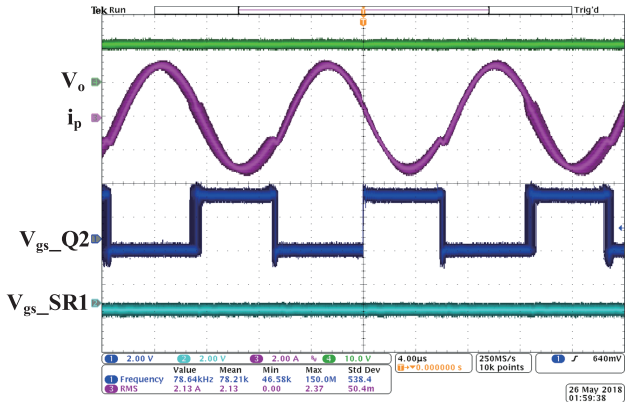


Fig. 15. Obtaining R_T via experiments.



(a)



(b)

Fig. 16. Key waveforms at full load. (a) Conventional control (b) Proposed control.

the circulating loss and the switch turn-off loss in the primary side. Moreover, the proposed converter achieves ZVS over the entire load conditions. In Fig. 16(b), the input voltage changes from 380 V to 407 V to maintain the switching frequency near the resonant frequency.

Fig. 17 shows the operating frequency range and the input voltage variation of the LLC resonant converter for both the conventional and the proposed method. As shown in Fig. 17, the frequency range of the convention technique is from 85 kHz to 73 kHz. In contrast, the frequency variation is from 76 kHz to

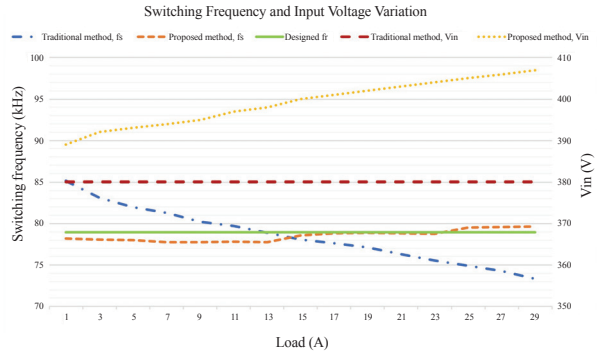


Fig. 17. Comparison of the operating frequency range and input voltage variation.

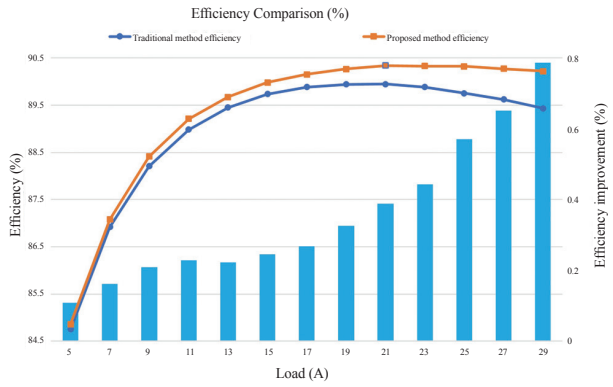


Fig. 18. Measured efficiency curves of the proposed adaptive DC-link voltage control method.

80 kHz for the proposed control method. It can also be observed from Fig. 17 that the input voltage of the conventional LLC resonant converter is fixed at 380 V while the input voltage of the proposed scheme changes from 389 V at light load to 407 V at full load. From Fig. 17, the DC-link voltage can be effectively adjusted to keep the switching frequency of LLC resonant converter near its resonant frequency.

Fig. 18 shows the measured efficiency curves of the proposed adaptive DC-link voltage control method and the conventional variable frequency control technique as load changes from 5 A to 29 A. From Fig 18, the proposed control technique achieves higher efficiency under all load conditions as compared to conventional LLC resonant converter, the efficiency improvement percentages are 0.13%, 0.27% and 0.88% under light-load, half-load and full-load conditions, and the averaged efficiency improvement is 0.427%. In addition, the highest measured efficiency is 90.22%.

VI. Conclusion

In this study, an adaptive DC-link voltage control technique for a two-stage SPS with LLC resonant converter is proposed. With this presented technique, the DC-link voltage increases to compensate for the voltage drop caused by load variation, which facilitates the resonant LLC converter to operate near its resonant frequency. This decreases the circulating energy and makes

the optimal design of an LLC resonant converter possible. Consequently, efficiency improvement can be achieved without any additional auxiliary circuits. According to the experimental results, the switching-frequency-variation range is reduced from 12 kHz to 4 kHz and the efficiency of the proposed method can be improved up to 0.13%, 0.27% and 0.88% under light-load, half-load, and full-load conditions, respectively.

References

[1] M. Kasper, D. Bortis, G. Deboy, and J.W. Kolar, "Design of a highly efficient (97.7%) and very compact (2.2 kW/dm3) isolated AC-DC telecom power supply module based on the multicell ISOP converter approach," *IEEE Transactions on Power Electronics,* vol. 32, no. 10, pp. 7750-7769, Oct. 2017.

[2] Y. S. Lai and Z. J. Su, "New integrated control technique for two-stage server power to improve efficiency under the light-load condition," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6944-6954, Nov. 2015.

[3] Z. I. Su and Y. S. Lai, "On-line DC-link voltage control of LLC resonant converter for server power applications," in *IEEE ECCE Conf. Rec.*, Nov. 2014, pp. 5422-5428.

[4] Y. S. Lai and Z. J. Su, "Novel on-line maximum duty point tracking technique to improve two-stage server power efficiency and investigation into its impact on hold-up time," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2252-2263, May 2014.

[5] J. B. Lee, J. K. Kim, J. I. Baek, J. H. Kim, and G.W. Moon, "Resonant capacitor on/off control of half-bridge LLC converter for high-efficiency server power supply," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 9, pp. 5410-5415, Sep. 2016.

[6] G. N. B. Yadav and N. L. Narasamma, "An active soft switched phase-shifted full-bridge DC-DC converter: Analysis, modeling design, and implementation," *IEEE Transactions on Power Electronics,* vol. 29, no. 9, pp. 4538-4550, Sep. 2014.

[7] I. H. Cho, K. M. Cho, J. W. Kim, and G. W. Moon, "A new phase-shifted full-bridge converter with maximum duty operation for server power system," *IEEE Transactions on Power Electronics,* vol. 26, no. 12, pp. 3491-3500, Dec. 2011.

[8] B. Gu, J. S. Lai, N. Kees, and C. Zheng, "Hybrid-switching full-bridge DC-DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," *IEEE Transactions on Power Electronics,* vol. 55, no. 3, pp. 1132-1144, Mar. 2013.

[9] Y. D. Kim, K. M. Cho, D. Y. Kim, and G. W. Moon, "Wide-range ZVS phase-shift full-bridge converter with reduced conduction loss caused by circulating current," *IEEE Transactions on Power Electronics,* vol. 28, no. 7, pp. 3308-3316, Jul. 2013.

[10] K. B. Park, C. E. Kim, G. W. Moon, and M. J. Youn, "Voltage oscillation reduction technique for phase-shift full-bridge converter," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 5, pp. 2779-2790, Oct. 2007.

[11] U. Kundu and P. Sensarma, "A unified approach for automatic resonant frequency tracking in LLC DC-DC converter," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 12, pp. 9311-9321, Dec. 2017.

[12] S. K. Chung, B. G. Kang, and M. S. Kim, "Constant frequency control of LLC resonant converter using switched capacitor," *IEEE Electronics Letters,* vol. 49, no. 24, pp. 1556-1558, Nov. 2013.

[13] H. H. Nien, C. K. Huang, C. C. Chou, C. H. Chan, and S. K. Changchien, "Design and implementation of an LLC resonant converter with saturable resonant inductor," *An International Journal of Research and Survey, ICIC Express Letters,* vol. 9, no. 3, pp. 691-697, Mar. 2015.

[14] H. Wang, S. Dusmez, and A. Khaligh, "Maximum efficiency point tracking technique for LLC-based PEV chargers through variable DC link control," *IEEE Transactions on Industrial Electronics,* vol. 61, no. 11, pp. 6041-6049, Nov. 2014.

[15] J. Y. Lee, Y. S. Jeong, and B. M. Han, "An isolated DC/DC converter using high-frequency unregulated LLC resonant converter for fuel cell applications," *IEEE Transactions on Industrial Electronics,* vol. 58, no. 7, pp. 2926-2934, Jul. 2011.

[16] B. C. Kim, K. B. Park, C. E. Kim, B. H. Lee, and G. W. Moon, "LLC resonant converter with adaptive link-voltage variation for a high-power-density adapter," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2248-2252, Sep. 2010.

[17] J. Jang, M. Joung, B. Choi, S. Hong, and S. Lee, "Dynamic analysis and control design of optocoupler-isolated LLC series resonant converters with wide input and load variations," *IET Power Electron.,* vol. 5, no. 6, pp. 755-764, Jan. 2012.

[18] W. Sun, Y. Xing, H. Wu, and J. Ding, "Modified high-efficiency LLC converters with two split resonant branches for wide input-voltage range applications," *IEEE Transactions on Power Electronics,* Early Access, 2017.

[19] H. Hu, X. Fang, F. Chen, Z. J. Shen, and I. Batarseh, "A modified high-efficiency LLC converter with two transformers for wide input-voltage range applications," *IEEE Transactions on Power Electronics,* vol. 28, no. 4, pp. 1946-1960, Apr. 2013.

[20] S. M. S. I. Shakib and S. Mekhilef, "A frequency adaptive phase shift modulation control based LLC series resonant converter for wide input voltage applications," *IEEE Transactions on Power Electronics,* vol. 32, no. 11, pp. 8360-8370, Nov. 2017.

[21] D. K. Kim, S. C. Moon, C. O. Yeon, and G. W. Moon, "High-efficiency LLC resonant converter with high voltage gain using an auxiliary LC resonant circuit," *IEEE Transactions on Power Electronics,* vol. 31, no. 10, pp. 6901-6909, Oct. 2016.

[22] C. Fei, Y. Yang, Q. Li, and F. C. Lee, "Shielding technique for planar matrix transformers to suppress common-mode EMI noise and improve efficiency," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 2, pp. 1263-1272, Feb. 2018.

[23] C. C. Wang, Y. C. Chang, Y. K. Lo, and H. J. Chiu, "Efficiency improvement in adjust dead-time of LLC resonant converters" *IGBSG Conf. Rec.*, April. 2014, pp. 1-4.

[24] L. H. Dixon, "Average current mode control of switching power supplies," Unitrode Power Supply Design Seminar Manual SEM700, 1990.

[25] S. Choudhury, "Average current mode controlled power factor correction converter using TMS320LF2407A," Texas Instrument application note, 2009.

[26] S. A. Rahman, F. Stuckler, and K. Siu, "PFC boost converter design guide" Infineon application note, 2016.

[27] C. P. Steinmetz, "On the law of hysteresis," in *Proc. IEEE,* Feb. 1984, vol. 72, pp. 197-221.

[28] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *IEEE Transactions on Industry Applications,* vol. 37, no. 4, pp. 1055-1061, Jul/Aug. 2001.

[29] X. Wang, C. Jiang, B. Lei, H. Teng, H. Bai, and J. L. K. Jr, "Power-loss analysis and efficiency maximization of a silicon-carbide MOSFET-based three-phase 10-kW bidirectional EV charger using variable DC-Bus control," *IEEE Transactions on Power Electronics,* vol. 4, no. 3, pp. 880-892, Sep. 2016.

[30] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end dc/dc conversion," in *IEEE APEC Conf. Rec.*, Aug. 2002, pp. 1108-1112.

[31] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W. K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency LLC series resonant converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3243-3256, Jul. 2012.

[32] J. W. Kim, and G. W. Moon, "A new LLC series resonant converter with a narrow switching frequency variation and reduced conduction losses," *IEEE Transactions on Power Electronics,* vol. 29, no. 8, pp. 4278-4287, Aug. 2014.

[33] C. Shi, H. Wang, S. Dusmez, and A. Khaligh, "A SiC-based high-efficiency isolated onboard PEV charger with ultrawide DC-link voltage range," *IEEE Transactions on Industrial Applications,* vol. 53, no. 1, pp. 501-511, Jan./Feb. 2017.

[34] Y. Jeong, G. W. Moon, and J.K. Kim, "Analysis on half-bridge LLC resonant converter by using variable inductance for high efficiency and power density server power supply," in *IEEE APRC Conf. Rec.,* May 2017, pp. 170-177.

[35] Y. Liu, "High efficiency optimization of LLC resonant converter for wide load range," Master's thesis, Virginia Polytechnic Institute and State University, Dec. 2007.
[36] "6th Generation CoolSiC™, 650V SiC Schottky Diode, IDH-20G65C6" Infineon datasheet, 2016.

Li-Chung Shih was born in Yilan, Taiwan, R.O.C., in 1975. He received the B.S. and M.S. degree in electrical engineering at Yuan Ze University, Chung Li, Taiwan, R.O.C. He is currently working toward the Ph.D. degree in the department of electronic and computer engineering in the Nationl Taiwan University of Science and Technology (NTUST). His research interests include power electronics, control system engineering, and digital power control.

Yi-Hua Liu received the Ph.D. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1998. He joined the Department of Electrical Engineering, Chang-Gung University, Taoyuan, Taiwan, in 2003. He is currently in the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan. His current research interests include the areas of power electronics and battery management.

Yi-Feng Luo received the Ph.D. degree in electrical engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2010. He is currently an assistant professor in the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan. His current research interests include the battery management and renewable energy.

Active Power Filter for Single-Phase Quasi-Z-Source Integrated On-Board Charger

Tuopu Na, Qianfan Zhang, Jiaqi Tang, and Jinxin Wang

***Abstract*—Single-phase quasi-Z-source rectifiers have second harmonic currents and corresponding ripple voltages on the dc bus. To filer the voltage ripple, bulky capacitor bank is needed. This paper proposed an active power filter (APF) for single-phase quasi-Z-source rectifier. It eliminated the second harmonic power with small capacitor and inductor. This topology is suitable to integrated electric vehicle (EV) on-board charger, which can use EV's inverter hardware as its own rectifier hardware. Thus, this proposed topology can save much space and weight. Simulation and experimental results verified the proposed system.**

***Index Terms*—Active power filter, integrated charger, quasi-Z-source, single-phase rectifier.**

I. Introduction

ELECTRICAL vehicles (EVs) have been widely used recently. The charger of EVs plays an important role in EVs system. An onboard charger makes it convenient for customers to charge. Thus, an onboard charger is necessary for EVs. An integrated onboard charger is proposed in [1]. The integrated charger and the EV's traction system share the hardware including three IGBT bridges, circuits and sensors. Besides, the integrated charger uses motor windings as filter inductor. The integrated charger costs less and takes less space. The quasi-Z-source network is suitable for single-phase integrated charger because it can realize bi-directional power flowing.

Since single-phase PWM rectifier has dc-side second harmonic current, it needs not only larger dc-side capacitor but also larger quasi-Z-source inductor and capacitor to suppress ripple. These inductors and capacitors will increase the charger's weight and take much space. And the dc-side second frequency ripple will reduce the battery life. So it is necessary to eliminate second frequency ripple. Many APFs [2]-[10] have been proposed to solve the problems for traditional single-phase converters. APF uses auxiliary circuit to convert the ripple power from the dc link to other energy storage components. [10] uses an inductor as energy storage, which includes one bridge circuit and one inductor. [6] also uses inductor as energy storage. In this system, a third IGBT bridge is added and one inductor is used which cost much. Capacitor is also can be used as energy storage for APF. [9] proposed a topology which adds a third IGBT bridge, a capacitor and an inductor. Two capacitors are used as energy storage in [8]. These APFs are suitable for single-phase PWM rectifier, and some methods have been proposed to solve the second harmonic current in single-phase z-source inverters [11]-[13].

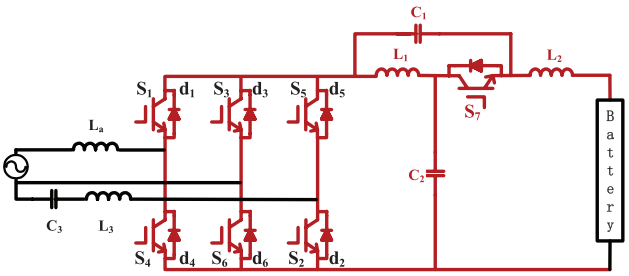


Fig. 1. The topology of single phase quasi-Z-source integrated charger with APF control.

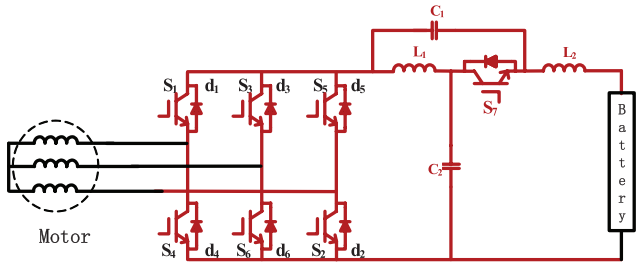


Fig. 2. The topology of EV traction system.

However, there is not a method proposed for single-phase z-source PWM rectifier. In this paper, a topology is proposed for eliminating the second harmonic current of the system, as shown in Fig. 1. And this topology is suitable for single-phase EV on-board integrated charger. The proposed topology uses extra IGBT S5 and IGBT S2 to control C3 and L3 to absorb the second harmonic power. The traction system of one electric vehicle is shown in Fig. 2. So the proposed APF single-phase z-source rectifier can use three IGBT bridges and the quasi-Z-source network to eliminate the second harmonic. The red topologies in Fig. 1 and Fig. 2 share the hardware including three IGBT bridges, quasi-Z-source network and control circuits. The integrated single-phase on-board charger saves much space, costs less and reduces weight.

II. Proposed APF Single-Phase Quasi-Z-Source Rectifier

A. Existing Problem Analysis

The topology of traditional single-phase quasi-z-source rectifier is shown in Fig. 3. With PFC, the grid-side voltage and cur-

Manuscript received July 31, 2018.

The authors are with Harbin Institution of Technology, Harbin, China (email: natuopu@126.com; zhang_qianfan@hit.edu.cn; tang_jiaqi@outlook.com; 1141420310@hit.edu.cn).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00019

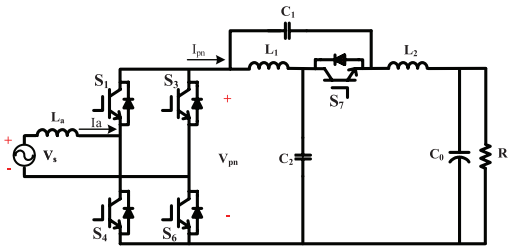


Fig. 3. The traditional quasi-Z-source single-phase rectifier.

rent can be controlled in the same phase. And the voltage and current are

$$v_s = V_s \sin(\omega t) \tag{1}$$

$$i_a = I_a \sin(\omega t) \tag{2}$$

and we can get the input power

$$p_{in} = v_s i_a - L_a \frac{di_a}{dt} i_a = \frac{V_s I_a}{2} - \frac{V_s I_a}{2}\cos(2\omega t) - \frac{wL_a I_a^2}{2}\sin(2\omega t) \tag{3}$$

so the dc component and the second harmonic component are,

$$p_0 = \frac{V_s I_a}{2} \tag{4}$$

$$p_{2\omega} = -\frac{V_s I_a}{2}\cos(2\omega t) - \frac{\omega L_a I_a^2}{2}\sin(2\omega t) \tag{5}$$

The second harmonic voltage and current will flow through the quasi-Z-source network, the huge capacitor and inductor of the quasi-Z-source network are needed to make the second harmonic voltage and current ripple small. It costs much and takes much space. The input power of quasi-Z-source network is

$$p_{pn} = (1-D) v_{pn} i_{pn} \tag{6}$$

where D is the shoot-through duty cycle[12]. [13] has analyzed the second harmonic ripple of quasi-Z-source network, that is

$$\begin{aligned} i_{L1} &= i_{L2} = I_{L1} + i_L \cos(2\omega t - \lambda) \\ v_{C1} &= V_{C1} + v_C \sin(2\omega t - \lambda) \end{aligned} \tag{7}$$

where I_{L1} and V_{C1} are the average current of inductor L1 and the average voltage of capacitor C1, respectively. The amplitudes of the second ripple of voltage and current are

$$i_L = \frac{1-2D}{\sqrt{[4\omega^2 LC - (1-2D)^2 + [\frac{4\omega L I_{pn}(D-1)}{V_{pn}}]^2]}} \cdot \frac{V_s I_a}{2V_{pn}} \tag{8}$$

$$v_C = \frac{2\omega L}{\sqrt{[4\omega^2 LC - (1-2D)^2 + [\frac{4\omega L I_{pn}(D-1)}{V_{pn}}]^2]}} \cdot \frac{V_s I_a}{2V_{pn}} \tag{9}$$

where L and C are the inductor and capacitor of the quasi-Z-source network.

When the parameters of the system have been designed, the quasi-Z-source network inductor and capacitor can be calculated by

$$L = \frac{v_C^*(1-2D)}{2\omega i_L^*} \tag{10}$$

$$C = \frac{(1-2D)^2 + \sqrt{(1-2D)^2 (\frac{V_s I_a}{2V_{pn} i_L^*})^2 - [\frac{4\omega L I_{pn}(D-1)}{V_{pn}}]^2}}{4\omega^2 L} \tag{11}$$

where v_c^* is the voltage ripple amplitude, i_L^* is the desired current ripple amplitude.

B. Proposed System Design

The APF circuit has no relationship with the quasi-Z-source network, so we only need to analyze APF single-phase rectifier at first. And the APF circuit is shown in Fig. 4.

Suppose the capacitor C3 and inductor L_3 to be

$$v_{C3} = V_{C3} \sin(\omega t + \theta) \tag{12}$$

$$i_{C3} = I_C \cos(\omega t + \theta) = \omega C_3 V_{C3} \cos(\omega t + \theta) \tag{13}$$

We can get the power of the APF

$$p_{APF} = L_3 \frac{di_C}{dt} i_C + v_{C3} i_C = (\frac{1}{2\omega C_3} - \frac{\omega L_3}{2}) I_C^2 \sin(2\omega t + 2\theta) \tag{14}$$

To eliminate sencond harmonic power in DC link, the power of APF should be

$$p_{APF} = p_{2\omega} \tag{15}$$

Submitting (5) and (14) into (15) yields

$$\frac{V_s I_a}{2} + (\frac{1}{2\omega C_3} - \frac{\omega L_3}{2}) I_C^2 \sin(2\theta) = 0 \tag{16}$$

$$\frac{\omega L_a I_a^2}{2} + (\frac{1}{2\omega C_3} - \frac{\omega L_3}{2}) I_C^2 \cos(2\theta) = 0 \tag{17}$$

The voltage of the capacitor C3 is controlled in the APF single-phase rectifier system, and the voltage and current of C3 can be get based on (16) and (17)

$$v_{C3} = \sqrt{\frac{\sqrt{V_s^2 I_a^2 + \omega^2 L_a^2 I_a^4}}{\omega C_3 - \omega^3 L_C C_3^2}} \sin(\omega t + \theta) \tag{18}$$

$$i_C = \sqrt{\frac{\sqrt{V_s^2 I_a^2 + \omega^2 L_a^2 I_a^4}}{1/\omega C_3 - \omega L_C}} \cos(\omega t + \theta) \tag{19}$$

$$\theta = \frac{\pi}{2} + \frac{1}{2}\tan^{-1}(\frac{V_s}{\omega L_a I_a}) \tag{20}$$

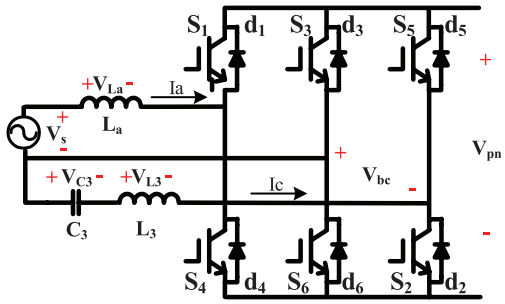


Fig. 4. The APF circuit.

When the voltage and current of the C3 satisfy the above conditions, the second harmonic power on DC link can be eliminated.

Because the second harmonic power ripple has been completely eliminated, the capacitor and inductor of the quasi-Z-source network are designed only to limit the switching frequency ripple. Therefore, the value of capacitor and inductor can be smaller, and the value will be

$$L_1 = L_2 = \frac{D(1-D)V_{pn}}{2f_s(1-2D)I_{L1}\delta_{\Delta i}} \tag{21}$$

$$C_1 = C_2 = \frac{I_{L1}D(1-2D)}{f_s V_{pn}\delta_{\Delta v}} \tag{22}$$

where $\delta_{\Delta v}$ and $\delta_{\Delta i}$ are the ratio of peak to peak ripple.

III. Control Strategy and Modulation

A. Control Strategy for APF

In section two, we have got the reference voltage of the capacitor C3. Then we can control this voltage to make the system working with no second harmonic power.

First, we can get the transfer function

$$G_v(s) = \frac{V_{C3}}{V_{bc}} = \frac{1}{L_3C_3s^2+1} \tag{23}$$

where V_{bc} is the voltage between phase B and phase C, and the equivalent resistance has been ignored. Because the proposed APF single-phase rectifier quasi-Z-source network is used as electric vehicle on-board integrated charger, the voltage and current sensors are enough to get the voltage and current of C3. Then we can use the V_{C3} and I_C as the poles to get a very stable system. The capacitor voltage control system is shown in Fig. 5. When the V_{bc} is obtained, it is easy to get the voltage of phase C. Then we can control the S2 and S5 to modulate the voltage.

B. Modulation for Quasi-Z-Zource Network

The modulation for the quasi-z-source network is shown in Fig. 6. In the paper [14], a novel modulation for soft-switching three-phase quasi-Z-source rectifier was proposed. The proposed modulation can be used in this APF single-phase quasi-Z-source system. When the S7 is turned off, the voltages across other switches (S1-S6) are clamped to zero. So the switches can be turned on or turned off under ZVS at the beginning of the system working in shoot-through state.

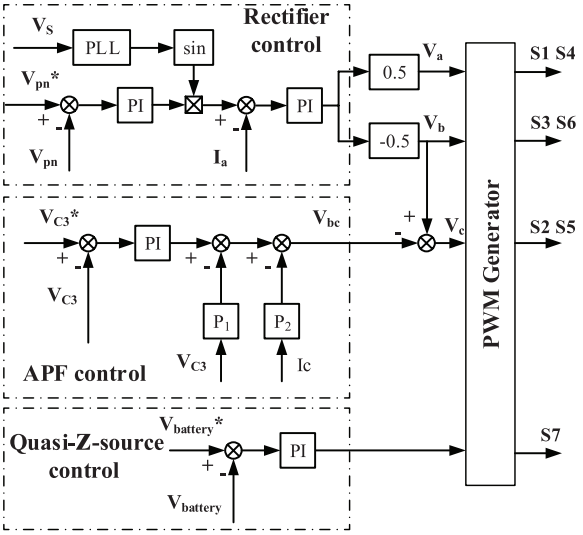


Fig. 5. The control strategy.

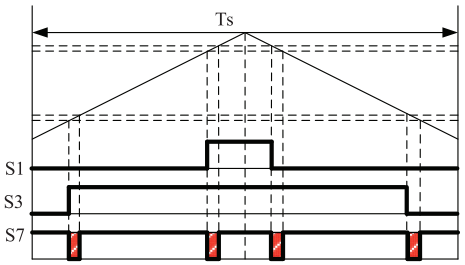


Fig. 6. The modulation for quasi-Z-source network.

IV. Simulation and Experimental Verification

The simulation and experimental results have been done to verify that the proposed APF single-phase quasi-Z-source rectifier can eliminate the second harmonic power.

A 750-W system has been designed with the parameters: V_s = 50 V, I_a = 30 A, L_a = 3 mH, V_{pn} = 190 V, R = 30 Ω, D = 0.1, f_s = 10 k. According to (10) and (11), the single-phase rectifier without APF needs quasi-Z-source impendence with L = 43 mH and C = 780 uF to make the second harmonic ripple smaller than 5%. The inductors and capacitors are huge. While, based on (21) and (22), the capacitance and inductance are C = 26 uF and L = 0.85 mH, respectively. In this paper, the values of C = 50 uF and L = 1 mH were used as the quasi-Z-source impendence.

A. Simulation Results

The traditional single phase quasi-Z-source rectifier suffers from the second harmonic ripple, so the voltage of C2 and the current of L1 have the second harmonic ripple. Fig. 7 shows the simulation result. The current of L1 and the voltage of C2 have

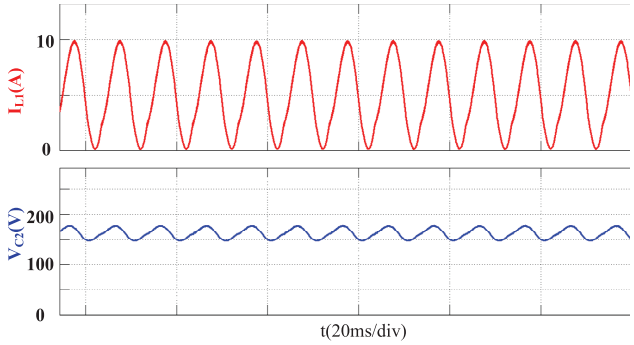


Fig. 7. Simulation results without APF: the inductor L1 current and the capacitor C2 voltage.

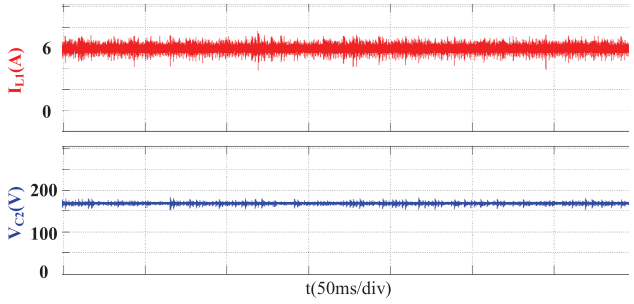


Fig. 8. Simulation results with APF: the inductor L1 current and the capacitor C2 voltage.

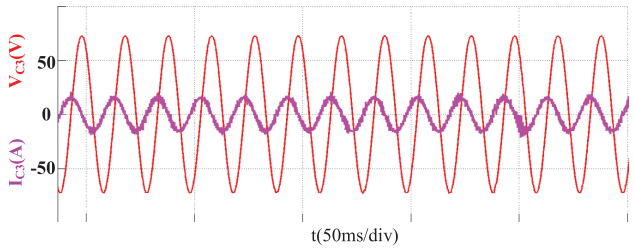


Fig. 9. Simulation results wih APF: the current and voltage of C3.

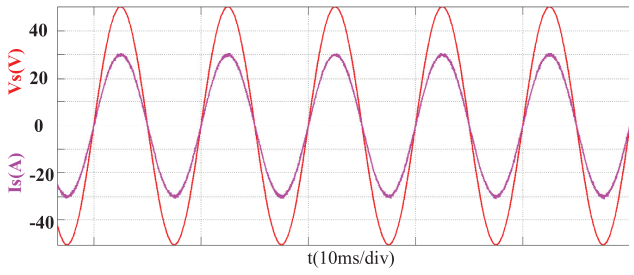


Fig. 10. Simulation results: grid-side voltage and grid-side current.

the large second harmonic ripple. Large capacitor and inductor are needed to suppress ripple. And when we use the proposed APF topology, the harmonic ripple can be eliminated, and the simulation result is shown in Fig. 8. From the simulation results, it can conclude that the APF topology absorbs all the second harmonic power.

The current and the voltage waveforms of the APF topology are shown in Fig. 9. And when the proposed APF single-phase

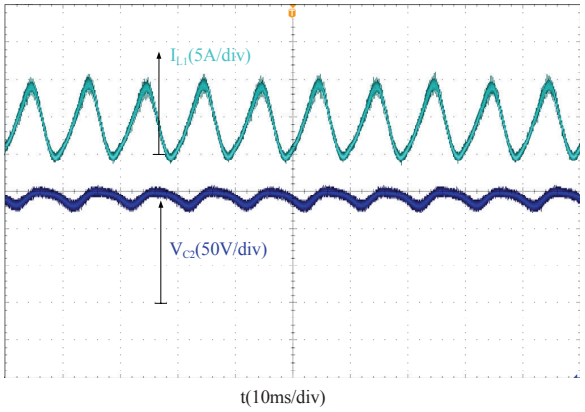


Fig. 11. Experimental results: L1 current and C2 voltage.

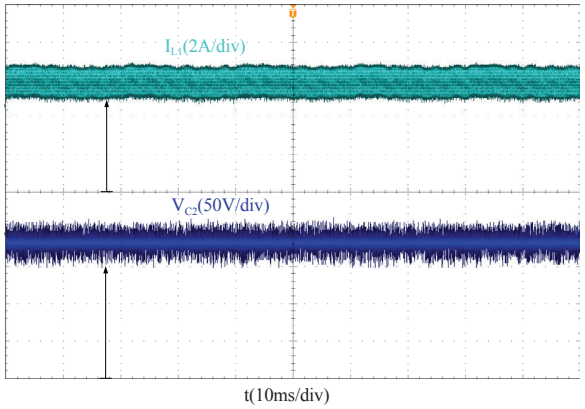


Fig. 12. Experimental results: L1 current and C2 voltage.

quasi-Z-source rectifier works, the grid-side current and voltage are with the same phase angle, as shown in Fig. 10. The efficiency of the system is high, and the harmonic of the grid-side current is small.

B. Experimental Results

Fig. 11 shows the experimental result of the quasi-Z-source single-phase rectifier without APF. From the Fig. 11, we can see that the current ripple of L1 and the voltage ripple of C2 are huge. And the waveforms are the same as the simulation result. The large current ripple will increase device loss and decrease the efficiency of the system. The APF topology is used to eliminate the second harmonic power, so the second harmonic current and voltage ripple can also be eliminated, the experimental result is shown in Fig. 12.

The experimental results of the current through APF and the voltage across C3 are shown in Fig. 13. Fig. 14 shows the grid-side current and voltage waveforms.

V. Conclusion

This paper proposed an APF quasi-Z-source single-phase integrated on-board charger which can eliminate the second harmonic power on DC link. Compared with the quasi-Z-source single-phase rectifier without APF, the quasi-Z-source network

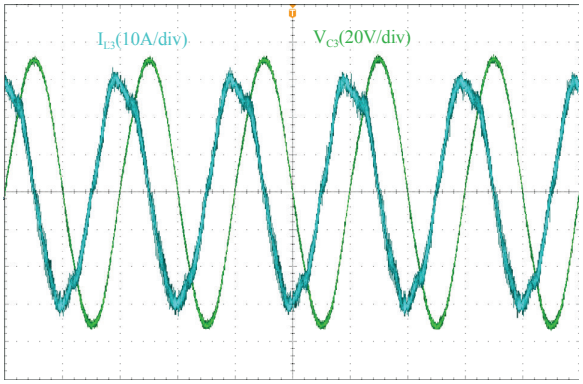


Fig. 13. Experimental results: C3 current and C3 voltage.

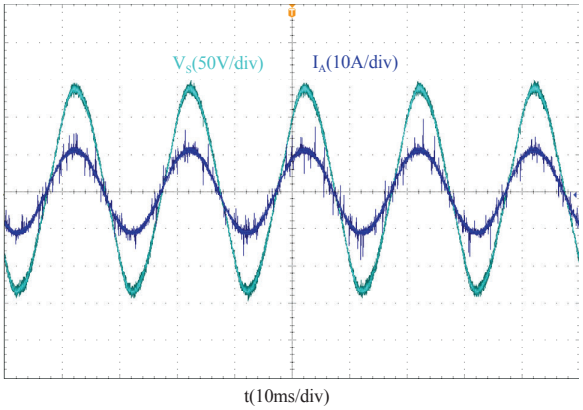


Fig. 14. Experimental results: grid-side current and grid-side voltage.

of the proposed system only need very small inductor and capacitor. The paper has provided the method how to design the parameters. Because this system can be used as an integrated on-board electric vehicle charger, it can make full use of the devices. Therefore, another advantage is that it saves much space and costs less. And a 750-W prototype has been designed. The simulation and experimental results have verified the theory of the proposed system.

References

[1] S. Haghbin, S. Lundmark, M. Alakula, and O. Carlson, "Grid-Connected integrated battery chargers in vehicle applications: review and new solution," *Industrial Electronics, IEEE Transactions on,* vol. 60, no. 2, pp. 459-473, 2013.

[2] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, "A unity power factor PWM rectifier with DC ripple compensation," *IEEE Transactions on Industrial Electronics,* vol. 44, no. 4, pp. 447-455, 1997.

[3] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1308-1319, 2013.

[4] M. Su, P. Pan, X. Long, Y. Sun, and J. Yang, "An active power-decoupling method for single-phase AC/DC converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 1, pp. 461-468, 2014.

[5] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in 2014 *IEEE Applied Power Electronics Conference and Exposition - APEC 2014,* pp. 89-95.

[6] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Transactions on Industry Applications,* vol. 36, no. 5, pp. 1419-1429, 2000.

[7] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Transactions on Power Electronics,* vol. 31, no. 7, pp. 4778-4794, 2016.

[8] R. Wang *et al.,* "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Transactions on Power Electronics,* vol. 26, no. 5, pp. 1430-1443, 2011.

[9] K. H. Chao, P. T. Cheng, and T. Shimizu, "New control methods for single phase PWM regenerative rectifier with power decoupling function," in *2009 International Conference on Power Electronics and Drive Systems (PEDS),* 2009, pp. 1091-1096.

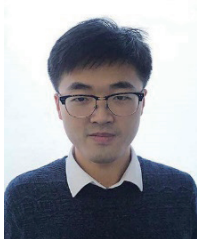
[10] T. Larsson and S. Ostlund, "Active DC link filter for two frequency electric locomotives," in *1995 International Conference on Electric Railways in a United Europe*, 1995, pp. 97-100.

[11] Y. Yu, Q. Zhang, B. Liang, and S. Cui, "Single-phase Z-Source inverter: Analysis and low-frequency harmonics elimination pulse width modulation," in *2011 IEEE Energy Conversion Congress and Exposition,* 2011, pp. 2260-2267.

[12] D. Sun *et al.*, "Modeling, impedance design, and efficiency analysis of quasi-Z-source module in cascaded multilevel photovoltaic power system," *IEEE Transactions on Industrial Electronics,* vol. 61, no. 11, pp. 6108-6117, 2014.

[13] B. Ge *et al.*, "An active filter method to eliminate DC-side low-frequency power for a single-phase quasi-Z-source inverter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4838-4848, 2016.

[14] Q. Zhang, T. Na, L. Song, and S. Dong, "A novel modulation for soft-switching three-phase quasi-Z-source rectifier without auxiliary circuit," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 6, pp. 5157-5166, 2018.



Tuopu Na received the B.S. and M.S. degree in Electrical Engineering from the Harbin Institute of Technology, Harbin, China, in 2012 and in 2014, respectively. He is current a Ph.D. in the school of electrical engineering, Harbin Institute of Technology, Harbin, China. His research interests include electric vehicle integrated charger, Z-source converter/inverter, etc.

Qianfan Zhang was born in Heilongjiang province, China. He received B.S. and Ph.D. from the Harbin Institute of Technology, Harbin, China, in 1999 and 2004, respectively, both in electrical engineering. In 1999, he joined department of electrical engineering in Harbin Institute of Technology as a faculty. He is professor since 2010. His research interesting includes electric machine and drives, power electronics applied on EV, HEV, integrated charging system, and wireless power transfer system.

Jiaqi Tang received the B.S. degree in electrical engineering from Harbin Institute of Technology, Harbin, China, where he is currently working toward the Ph.D. degree. His research interests include wireless power transfer.

Jinxin Wang was born in Chongqing, China, in 1996. He received the B.Sc degree in electrical engineering from the Harbin Institute of Technology, Harbin, China in 2018, where he is currently pursuing the M.Sc degree in electrical engineering. His current research interests include power electronics and electric machine drives, particularly the thermal behaviors of those devices.

Adaptive Charging Strategy With Temperature Rise Mitigation and Cycle Life Extension for Li-ion Batteries

Shun-Chung Wang, Guan-Jhu Chen, and Yi-Hua Liu

***Abstract*—Charging battery with a large C-rate current to shorten the charging time (CT) will induce the drastic electrochemical reaction, and thus bring about the significant temperature rise (TR), energy loss, performance degradation, and safety concern as well. To tackle this problem, an adaptive charging strategy with TR mitigation and cycle life extension is proposed in this study. Based on the relationship between the charging current and remaining state of charge (RSOC) which is extracted experimentally, a baseline charging current is determined first. To control the temperature rise further, a fuzzy TR controller (FTC) is devised to fine-tune the charging current according to the temperature gradient. Thus an adaptive charging current with temperature rise suppression mechanism can be generated dynamically in the entire charging process. The proposed charging strategy is validated by means of experimental studies and compared with the conventional constant current-constant voltage (CC-CV) method. The results show that the average temperature rise, charging efficiency, and estimated cycle life have 31.24%, 2.06%, and 57.3% of improvement respectively as compared with that of the conventional CC-CV obtained.**

***Index Terms*—Adaptive charging strategy, cycle life extension, fuzzy temperature-rise controller.**

Nomenclature

CT	Charging time.
TR	Temperature rise.
SOC	State of charge.
RSOC	Remaining state of charge.
FTC	Fuzzy temperature-rise controller.
CC-CV	Constant current-constant voltage.
HEV	Hybrid electric vehicle.
EV	Electric vehicle.
ESS	Energy storage system.
Li-ion	Lithium-ion.
RCC	Remaining capacity charging.
4S2P	Four series two parallel.
SBC	Synchronous buck converter.
MCU	Microcontroller unit.
GUI	Graphic user interface.
I^2C	Inter-integrated circuit.
ADC	Analog to digital converter.
FIR	Finite impulse response.
PID	Proportional integral differential.
DPWM	Digital pulse width modulation.
CTR	Charging time ratio.
MF	Membership function.
UOD	Universe of discourse.
COS	Center of sum.
RCFTC	Remaining capacity with FTC.

Manuscript received August 1, 2018. This work was financially supported by the Taiwan Building Technology Center from the Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education in Taiwan.

S. -C. Wang is with the Department of Electrical Engineering, Lunghwa University of Science and Technology, Taoyuan, 33306 Taiwan (e-mail: wangsc@mail.lhu.edu.tw).

G. -J. Chen and Y. -H. Liu are with the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, 10607 Taiwan (e-mail: D10707003@mail.ntust.edu.tw; yhliu@mail.ntust.edu.tw).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00020

I. Introduction

To deal properly with problems of energy shortage and global warming, the objective of cut in carbon emissions intended by governments is getting stricter. As a result, powertrain electrification has been regarded as the most promising substitute for a vehicle driven by an internal combustion engine to fulfill the international anticipation on eco-friendly and energy-efficient transportation [1]-[3]. Accordingly, automakers now are devoted to developing vehicle electrification using electronic components or subsystems in the form of hybrid electric vehicles or electric vehicles (HEVs/EVs). Power battery is a key component for the success of transportation electrification, in which the relevant issues concerned most by users include safety, endurance anxiety, charging time, and cost-effectiveness. Therefore, advanced energy storage systems (ESSs) together with intelligent energy management algorithms will be the essential technology for the electrification in the next generation EVs [4].

Commercial batteries based on Lithium-ion (Li-ion) chemistry, in particular the LiFePO4 one, has been confirmed that their performances are very suitable for use in the ESS due to many remarkable characteristics [5], [6]. For a battery storage system in EVs, a well-designed on-board charger [7]-[9] must be equipped with advanced charging strategies to ensure efficient and safe operations. On the other hand, excessive fast charging not only gives rise to the extreme electrochemical stresses but also results in the aging aggravation and significant performance degradation [10], [11]. These degenerative effects arise from the increasing internal resistance of the battery caused by substantial temperature rise due to the increase in energy losses. The battery temperature rise is closely connected

to the charging profile used and it is a competing factor to the charging time and energy loss generally. Nowadays, one of the commonly adopted methods for charging Li-ion batteries is the constant current–constant voltage (CC-CV) strategy [12]. This method applies a fixed current to charge the battery in CC mode till a predefined voltage limit is reached, and then the charging process is switched to CV mode whose voltage is kept at the predefined voltage until the end-of-charge condition, which drops the current below a cut-off threshold, is met. The CC-CV charging method is easy to implement and can fully charge the battery. However, its performance is related to the pre-defined limit values. Therefore, how to select a proper charging current in the CC stage and the best time to transit CC to CV to reach preferable charging efficiency is still a challenging problem [13]. In addition, energy loss increased in CC mode leads to higher temperature rise. The CV stage substantially extends the charging time and thus will degrade the charging efficiency. Fast charging has always been an indispensable design of the battery employed in EVs [14]-[16]. Hence, how to make fast charging achievable yet still maintain safety, efficacy and longevity is a substantial challenge.

To meet the rapid charging criteria, various ameliorations or variants based on the standard CC-CV method have been proposed [17]-[19]. Experimental results demonstrate that these methods can attain a charging profile similar to the CC-CV in a simple and low-cost way, and obtain shorter charging time and higher charging efficiency than the standard CC-CV method. A series of studies on charging strategy, profile, or topology to meet the fast charging criteria were addressed by Chen et al. [20]-[22]. Improvements in charging efficiency and speed have been verified experimentally by these devised schemes. Comparing with the standard CC-CV, the multistage constant current charging method can offer better charging efficiency [23]-[25]. Intelligent control algorithms, such as fuzzy control [26], neural network [27], gray-prediction control [28], and genetic approaches [29], have also been adopted to elevate the accuracy of the parameter estimation and operating performance of the charger. Accurate characterization of the battery parameter and behavior is necessary for these algorithms. Besides, a model which exhaustively reflects the battery dynamic behavior in real time is difficult to construct, because the reaction process of the electrochemical, thermoelectric, and aging phenomena are sophisticated and unmeasurable. Therefore, development in charging modes alone could not promise to obtain best charging profiles and raise the charging efficacy significantly. Furthermore, the cycle life issues are seldom discussed in these researches. In recent, studies on optimal charging strategies based on battery equivalent circuit model, electrochemical and/or electrothermal models integrated with optimization control algorithms to find the optimum charging pattern out have become a focus. Such a problem can be regarded as a combinatorial optimization problem which is difficult to resolve with traditional methods. Several optimization techniques, such as particle swarm optimization (PSO) [30], non-dominated sorting genetic algorithm II [31], the ant colony system [32], and advanced optimal approaches with battery health-aware charging strategies formulated by the analysis and computation of accurate battery behavior models [10], [33]-[37] have been applied to obtain the best compromise among the competing objectives and achieve charging performance amelioration. However, sophisticated models with real-time parameters update are necessary. High implementation complexity and computational burden make these optimal approaches more difficult to realize online and use low-end microprocessor chips. The Taguchi-based approach cooperated with fuzzy control have also been validated to be feasible and effective in searching for the optimal charging pattern of the five-step CC charging method [38]-[40].

In this paper, a remaining capacity charging method with fuzzy TR control is proposed to determine proper charging currents adaptively as facing with different charging conditions. A corresponding baseline charging current is first selected depending on the relationship between the current SOC and charging current that is extracted from actual charging and discharging test data. Then an FTC is designed to fine-tune the charging current according to the battery temperature variation. By adding the fine-tuning incremental current to the baseline one, a charging current with TR alleviation can be obtained. The proposed adaptive charging strategy can regulate the charging current adaptively on the basis of changes in current SOC status and battery temperature to achieve performance promotion during the entire charging phase. Moreover, the adverse condition of using high C-rate current to charge battery with high SOC can be avoided. In addition, without need to model the exhaustive battery behavior, depending on the change of the charging condition, the proposed charging method has taken the nonlinearity of the battery electrothermal behavior and the circuit parameter non-ideality into account to attain the temperature rise suppression effectively via charging current dynamic regulation using fuzzy-based decision-making mechanism. The rest of this paper is organized as follows. Section II introduces the architecture of the proposed charger. Fundamental and implementation of the proposed remaining capacity charging and fuzzy TR control strategy are described in Section III. Section IV shows experimental results, and comparisons with the traditional CC-CV method are given to highlight the performance improvement of the studied charging method. Finally, this paper is concluded in Section V.

II. Battery Charger Architecture

Fig. 1 shows the architecture of the studied digitally-controlled Li-ion battery pack charger. The input voltage of the charger derived from a front-end ac-dc rectifier with a regulable output voltage which is adaptable to the applications of battery-powered devices. The battery pack used in this paper is made up of 4-series-2-parallel (4S2P) Li-ion battery cells, in which each cell has nominal capacity of 2200 mAh. The range of the pack voltage is 12 V~16.8 V, and all cells are screened beforehand to ensure that each cell has the similar characteristics. The synchronous buck converter (SBC) was adopted as the power stage. The gas gauge IC bq20Z45 [41] was used to estimate the SOC of the battery pack. Temperatures of the bat-

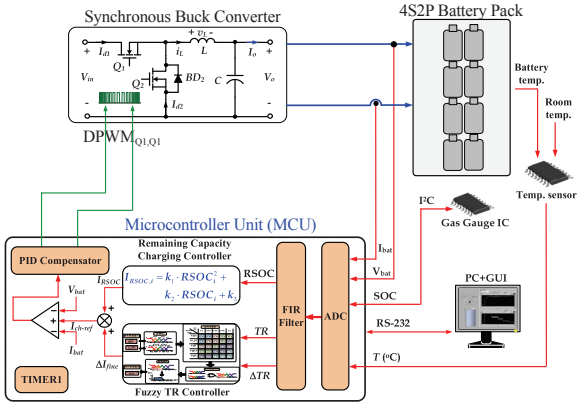


Fig. 1. Proposed charger configuration.

tery exterior and room were detected by the temperature sensor. The proposed adaptive charging approach was implemented by a low-cost dsPIC microcontroller unit (MCU) from Microchip [42]. The firmware written in the MCU carries out the remaining capacity charging strategy, fuzzy temperature rise control, and quantizes the detected battery voltage V_{bat}, current I_{bat}, SOC, battery and room temperatures T (°C), and the feedback signals to reduce the circuit complexity.

The PC with developed graphic user interface (GUI) records and monitors various battery data and waveforms online during the charging process. The SOC gauge IC communicates with the MCU through the inter-integrated circuit (I^2C) protocol, andthe connection between the MCU and PC is via the universal asynchronous receiver transmitter standard RS-232. The data of the RSOC and TR are sampled and quantized by the analog to digital converter (ADC) and filtered by finite impulse response (FIR) filter, respectively, and then these data are sent to the remaining capacity charging controller and fuzzy TR controller, which are realized by firmwares in the MCU. Based on the variation of the pack RSOC and temperature, the RCC controller outputs a corresponding coarse-tuning current and the FTC outputs a fine-tuning incremental charging current ΔI_{fine}, which is added to the coarse-tuning current to generate areference value $I_{ch\text{-}ref}$ that is the desired charging profile. Comparing the reference value with actual charging current, an error is obtained and routed to the proportional integral differential (PID) compensator to calculate the required duty cycles of the digital pulse width modulation (DPWM) gating signals. Simultaneously, the data are recorded by PC and displayed on the GUI.

In low-voltage and high-current applications, the power consumption of the diode in buck converter due to the forward voltage drop V_{FD} and the equivalent resistance R_D has become one of the main reasons for the decrease in efficiency. The conduction loss will increase with the increase in output current. An SBC, which replaces the diode with a synchronous rectifier (a MOSFET with very low on-resistance $R_{ds\text{-}on}$), is adopted to further reduce the conduction loss of the diode. As shown in Fig. 1, the conduction loss and switching loss of switch Q_1 can be expressed as

$$P_{con-Q_1} = DI_{rms}^2 R_{ds1-on} \tag{1}$$

$$P_{sw-Q_1} = \frac{1}{2} V_{in} I_{rms} (t_{ri} + t_{fv}) f_s \tag{2}$$

Where D is the duty cycle, I_{rms} is the RMS value of the switch current, t_{ri} is the current rise time, t_{fv} is the voltage fall time, and f_s is the switching frequency. The conduction losses of the synchronous rectification MOSFET Q_2 and the conventional diode can be expressed by

$$P_{con-Q_2} = \underbrace{(1-D) I_{rms}^2 R_{ds2-on}}_{MOSFET\ Q_2} + \underbrace{2 I_{rms} V_{FBD_2} t_{delay} f_s}_{body\ diode\ BD_2} \tag{3}$$

$$P_D = V_{FD} I_{rms} (1-D) + (1-D) I_{rms}^2 R_D \tag{4}$$

Where V_{FBD2} is the turn-on voltage drop of the body diode BD_2 in Q_2, and t_{delay} is the turn-on delay time of the body diode.

When Q_2 is on, the relationship between the RMS current I_{rms} and I_o is

$$I_{rms} = \frac{\pi}{4} I_o \tag{5}$$

Then, in (3), if the loss of the body diode is neglected, the power consumption caused by the resistor $R_{ds2\text{-}on}$ can be approximated as

$$P_{con-Q_2} = (1-D)\left(\frac{\pi}{4} I_o\right)^2 R_{ds2-on} = (1-D) P_o \frac{\pi^2 \cdot R_{ds2-on}}{16 \cdot R} \tag{6}$$

Substituting (5) into (4), the diode conduction loss can be obtained by

$$P_D = (1-D) P_o \left(\frac{\pi^2}{16} \frac{R_D}{R} + \frac{\pi}{4} \frac{V_{FD}}{V_o}\right) \tag{7}$$

From (6) and (7), if $R_D = R_{ds2\text{-}on}$, then the diode will have one more forward voltage drop loss than the synchronous rectifier. Therefore, if the output is low voltage and large current, the efficiency of the buck converter with conventional diode will be much lower than that of using the synchronous rectifier. According to the rating of the battery pack, an 85 W charger adopting the above-mentioned topology was designed. The design specifications of the charger are listed in TABLE I.

III. Proposed Charging Strategy

A novel adaptive charging profile control strategy combining the residual capacity charging with a fuzzy temperature-rise controller is proposed in this paper. In order to achieve the control objectives, firstly it is necessary to know the time required for fully charging battery with different charging C rates at different remaining capacities and the temperature rise obtained by the same charging process through the experimental tests. Then the relationships between the CT and RSOC as well as the TR and RSOC with different charging C rates can be derived, respectively. Next, a commensurate charging current I_{RSOC} (or called corase-tuning charging current) can be determined prop-

TABLE I
DESIGN SPECIFICATIONS OF THE STUDIED CHARGER

Input voltage (V_{in})	24 V
Output voltage (V_o)	12~16.8 V
Output power (P_o)	85 W
Efficiency (η)	> 90%
Switching frequency (f_s)	100 kHz
Output voltage ripple ($\Delta V_o/V_o$)	< 5%
Output current ripple ($\Delta I_o/I_o$)	< 20%

erly based on the current RSOC gauged correspondingly, thus the situation of charging high SOC battery with high C rate can be avoided. The CT required for full charge can also be shorten because the selected corase-tuning charging current has a good charging time ratio (CTR), which is defined as the ratio of full charge time required for 1 C charging current to that required for the selected coarse-tuning current in the CC-CV method. In addition, in order to further control the battery temperature rise, a fuzzy temperature-rise controller is developed to fine tune the charging current based on the dynamic change in battery temperature. When the battery temperature rises, the charging current is reduced, otherwise, the charging current is increased. By imposing the fine-tuning current ΔI_{fine} on the coarse-tuning current I_{RSOC}, the desired charging current with TR control can be obtained. Thus the battery can be fully charged in an acceptable charging time, and the temperature rise is controllable to relieve the performance degradation.

The proposed method is adaptable because, during the charging process, the charging current can be dynamically regulated according to the changes of the battery SOC status and battery temperature to achieve TR alleviation and lifespan extension. That is, a proper baseline (coarse) charging current, in accordance with the gauge of the current RSOC, can be first determined through the studied curve-fitting relationship between the charging current and the RSOC variation. Thus the adverse condition of using high C-rate current to charge battery with high SOC can be avoided. Next, an incremental current is generated through the devised fuzzy temperature controller and imposed on the coarse current to finely regulate the charging current to control the temperature variation further. Therefore, the adaptability of the presented method derives from the charging profile can be controlled dynamically by following the changes of current charging state and temperature to fully charge battery with reasonable charging time and low temperature rise. In the following subsections, the philosophy of the studied remaining capacity charging method and the design principle of the FTC are described respectively.

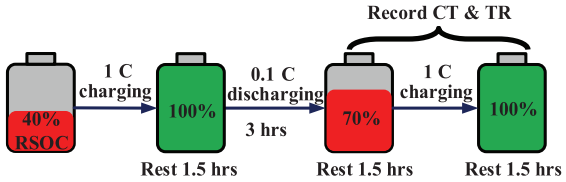
A. Philosophy of Remaining Capacity Charging

The remaining capacity charging (RCC) method can measure a battery current SOC to adjust how much charging current must be used. Before implementing this method, several experiments must be done to determine the best charging profil required for each gauged SOC. Through the experimental test, relevant information and data for fully charging a battery at different remaining capacity with different C rates can be acquired, then the relationships between the CT and RSOC as well as the TR and RSOC can be extracted from the meaured records. Accordingly, for a battery with any initial RSOC, an evaluation criterion for determination of the suitable charging current to reach the acceptable CT and lower TR can be established via the analysis and exploration of the derived relationship among the charging time, temperature rise, and remaining state of charge. To obtain the data required for the RCC method, different C-rate (0.2 C ~ 1 C with a step of 0.1 C) charging currents are used to charge a battery with different initial RSOCs (0% ~ 100% with a step of 10%). Using Fig. 2 as an example to illustrate the experimental test procedure. In Fig. 2(a), assuming that the battery has 40% of initial RSOC. The test process needed to charge the battery from 70% to 100% of RSOC with 1 C rate is shown in Fig. 2(b). from Fig. 2(a), the battery is first charged with 1 C rate until the voltage reaches 4.2 V, the CV mode with 4.2 V is run until the current drops below 0.01 C, then stop charging and rest 1.5 hours. The next, discharge with 0.1 C is carried out. After discharging for 3 hours, stop discharging and rest 1.5 hours. At this time, the battery RSOC is about 70%. The next step is to charge the battery with 1 C rate again. As the battery voltage reaches 4.2 V, it is switched to CV mode until the end of charging is reached, then stop charging and rest 1.5 hours. From this test, the CT and TR required for charging the battery from 70% to 100% of RSOC with 1 C rate can be measured. Similarly, other datum acquired for charging battery from different percent remaining capacity to 100% using different C rates can be obtained by running the similar test procedures.

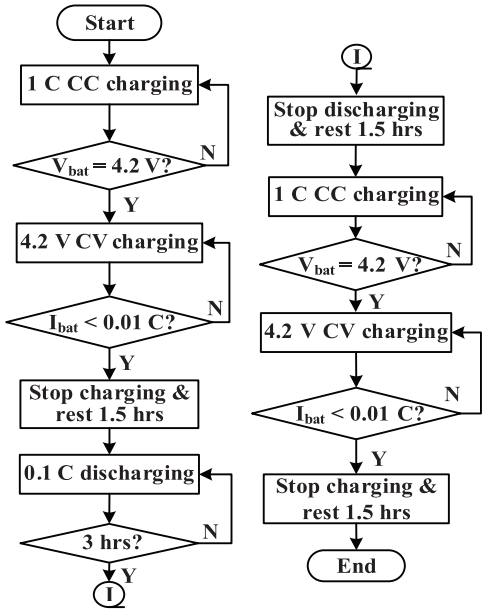
As mentioned above, the test results of the CT and RT obtained by charging a battery with specified initial RSOCs to full charge using different C rates are shown in TABLE II and Fig. 3, respectively. From the measured charging time listed in TABLE II, a charging time ratio (CTR) is defined as the ratio of the full-charge time required for 1 C rate to those required for the other 0.2 C to 0.9 C ones. The calculated CTR and the differences of full-charge tme between the 0.2 C to 0.9 C and 1 C is tabulated in TABLE III, in which the Δt is the charging-time differencebetween charging with 0.2 C~0.9 C and with 1 C, and the corresponding CTR cureves is ploted in Fig. 4. The design objective is to shorten the CT as possible but still maintain the acceptable TR and satisfy safety constraints, therefore the CTRs more than 0.9 (coloring fields in TABLE III) are chosen as the evaluation criterion in this study. It can be noted that, from TABLE III, when the remaining capacity is 0%, the difference of charging time between using 0.9 C charge and using 1 C charge is only 5 minutes and 37 seconds; additionally, as the remaining capacity is 90%, the difference of CT between using 0.4 C charging and 1 C charging is only 2 minutes and 50 seconds. As a result, there is no need to charge battery using the highest C rate always, and a proper charging current can be determined based on the current remaining capacity, which can reduce the adverse effect of excessive TR on battery life.The 4400 mAh battery pack was used in this study to do experimental confirmation. Based on the evaluation criterion as shown in TABLE III, the charging currents with CTRs over 0.9 are listed in TABLE IV.

TABLE II
REQUIRED CHARGING TIME FOR FULLY CHARGING BATTERY PACK

SOC \ C rate	0.2 C	0.3 C	0.4 C	0.5 C	0.6 C	0.7 C	0.8 C	0.9 C	1 C
0%	5:33:27	4:00:21	3:13:28	2:42:03	2:25:16	2:12:11	2:03:30	1:56:07	1:50:30
10%	5:03:58	3:41:56	3:00:16	2:21:46	2:17:17	2:05:20	1:57:13	1:52:29	1:46:59
20%	4:33:35	3:19:46	2:44:08	2:20:43	2:07:27	1:57:02	1:49:03	1:48:13	1:40:52
30%	3:53:20	2:58:44	2:28:44	2:08:06	1:56:07	1:47:50	1:43:19	1:39:28	1:33:59
40%	3:31:53	2:39:06	2:01:51	1:55:18	1:46:17	1:38:03	1:34:41	1:32:13	1:27:17
50%	2:51:33	2:18:56	1:46:38	1:42:59	1:34:56	1:30:01	1:27:18	1:24:13	1:21:02
60%	2:31:39	1:56:43	1:38:25	1:29:57	1:25:13	1:20:38	1:18:41	1:16:50	1:13:52
70%	1:49:32	1:32:58	1:22:33	1:15:43	1:11:51	1:08:46	1:07:49	1:04:57	1:04:28
80%	1:24:13	1:10:04	1:04:05	0:58:36	0:57:41	0:54:27	0:54:18	0:54:14	0:53:07
90%	0:52:21	0:47:01	0:44:27	0:42:39	0:42:12	0:42:00	0:41:50	0:41:45	0:41:38



(a)



(b)

Fig. 2. Experimental test procedure: (a) Illustration for testing 70% residual capacity using 1 C rate for battery with 40% initial capacity; (b) Test procedure flowchart.

Where the I_{bat} is the charging current at 1 C, i.e. I_{bat} = 4.4 A in this paper. The given charging current $I_{RSOC,i}$ is equivalent to the desired coarse-tuning current whose CTR is greater than 0.9 at each corresponding RSOC in this research. Furthermore, to fulfill practical charging application, a mathematical model is built from the limited experimental samples. The curve fitting was employed to formulate the relationship between the $I_{RSOC,i}$ and the $RSOC_i$. Fig. 5 illustrates the dependence of the desired charging current on different RSOCs. The curve function fitted

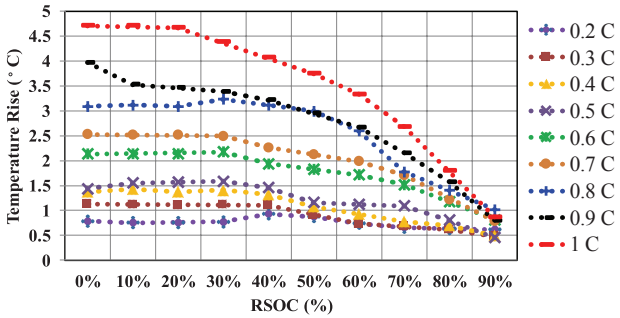


Fig. 3. Measured temperature rise obtained by fully charging battery pack.

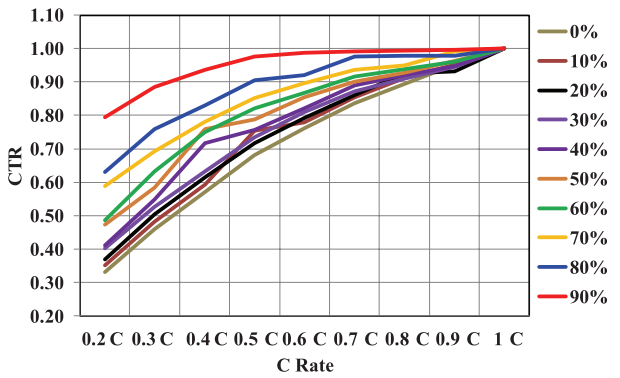


Fig. 4. Plot of CTR curves under different initial RSOCs.

by the quadratic polynomial is expressed by

$$I_{RSOC,i} = k_1 RSOC_i^2 + k_2 RSOC_i + k_3 \quad (8)$$

For the specifications of the battery pack used here, the coefficient k_1 is -2.5×10^{-4}, k_2 is 0.001167, and k_3 is 3.74.

B. Design Principle of Fuzzy Temperature-Rise Controller

In order to alleviate the battery aging effect, a fuzzy temperature-rise controller (FTC) is designed to fine modulate the charging current. This fine tuning current is imposed on the coarse-tuning current to produce the desired charging current, which features ability of temperature rise control. In other

TABLE III
CTR AND DIFFERENCE OF FULL-CHARGE TIME WITH 1 C

SOC \ C rate	0.2 C	0.3 C	0.4 C	0.5 C	0.6 C	0.7 C	0.8 C	0.9 C	1 C	Δt
0%	0.33	0.46	0.57	0.68	0.76	0.84	0.89	0.95	1	0:05:37
10%	0.35	0.48	0.59	0.75	0.78	0.85	0.91	0.95	1	0:10:13
20%	0.37	0.50	0.61	0.72	0.79	0.86	0.92	0.93	1	0:08:11
30%	0.40	0.53	0.63	0.73	0.81	0.87	0.91	0.94	1	0:09:20
40%	0.41	0.55	0.72	0.76	0.82	0.89	0.92	0.95	1	0:07:24
50%	0.47	0.58	0.76	0.79	0.85	0.90	0.93	0.96	1	0:08:59
60%	0.49	0.63	0.75	0.82	0.87	0.92	0.94	0.96	1	0:06:46
70%	0.59	0.69	0.78	0.85	0.90	0.94	0.95	0.99	1	0:07:23
80%	0.63	0.76	0.83	0.91	0.92	0.98	0.98	0.98	1	0:05:29
90%	0.80	0.89	0.94	0.98	0.99	0.99	1.00	1.00	1	0:02:50

TABLE IV
CORRESPONDING CHARGING CURRENT AS CTR ABOVE 0.9

$RSOC_i$	0%	10%	20%	30%	40%
$I_{RSOC,i}$	$I_{RSOC,0}=0.9I_{bat}$	$I_{RSOC,1}=0.8I_{bat}$	$I_{RSOC,2}=0.8I_{bat}$	$I_{RSOC,3}=0.8I_{bat}$	$I_{RSOC,4}=0.8I_{bat}$
$RSOC_i$	50%	60%	70%	80%	90%
$I_{RSOC,i}$	$I_{RSOC,5}=0.7I_{bat}$	$I_{RSOC,6}=0.7I_{bat}$	$I_{RSOC,7}=0.6I_{bat}$	$I_{RSOC,8}=0.5I_{bat}$	$I_{RSOC,9}=0.4I_{bat}$

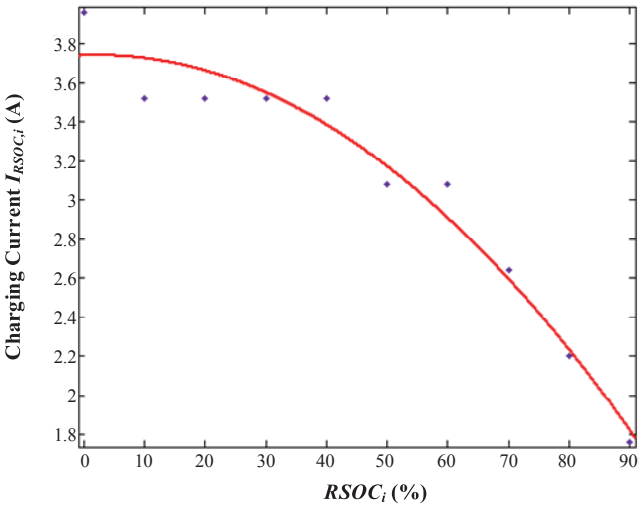


Fig. 5. Plot of charging current versus RSOC and the fitting curve.

words, an incremental current ΔI_{fine} was generated by the fuzzy temperature controller and added to the $I_{RSOC,i}$ to further regulate the charging current according to the variation of the working temperature. When the TR was increasing during charging process, the charging current will be reduced for a ΔI_{fine} step consecutively to drop the temperature rise and diminish impact on the battery. On the other hand, as the TR was decreasing, the charging current will be increased for a ΔI_{fine} step each time to shorten the charging time.

The scheme of the proposed FTC is shown in Fig. 6. From Fig. 6, the input variables of the FTC are the temperature rise (TR) and the 2-second temperature rise (ΔTR). In which the TR was defined as the difference between the battery surface temperature and the room temperature.The ΔTR was the difference

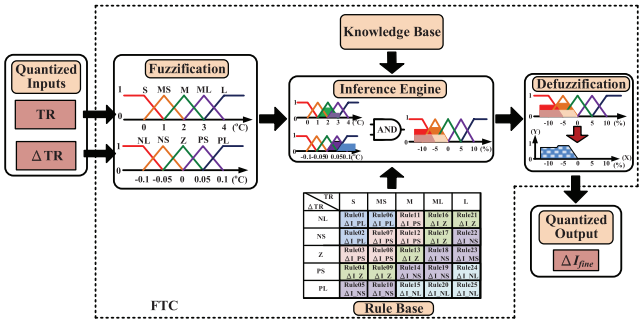


Fig. 6. Scheme of the proposed FTC.

between the present TR and the TR before two seconds.The output variable was the incremental current ΔI_{fine}. The Mamdani-type Minimum inferential method cooperating with the center of sum (COS) defuzzification procedure was utilized in this paper to obtain the crisp output.The membership functions (MFs) corresponding to the TR, ΔTR, and ΔI_{fine} are illustrated in Fig. 7(a)-(c), respectively. According to the experience of the lithium-ion battery charging, five fuzzy subsets are designated for the input and output variables respectively. The universe of discourse (UOD) in the MFs of TR and ΔTR aredefined on the domain [0°C, 4°C] and [-0.1°C, 0.1°C], respectively. On the other hand, the UOD of the output variable is defined on the domain [-20%, 20%]. In Fig. 7(a), the linguistic values S, MS, M, ML, and L represent temperature rise small, medium small, medium, medium large, and large, respectively. From Fig. 7(b) and (c), the NL, NS, Z, PS, and PL stand for ΔTR and ΔI_{fine} negative large, negative small, zero, positive small, and positive large, respectively. Except for the two fuzzy subsets (trapezoidal MFs are considered) at the outmost ends, symmetric triangles with equal bases and 50% overlap with adjacent MFs are chosen.

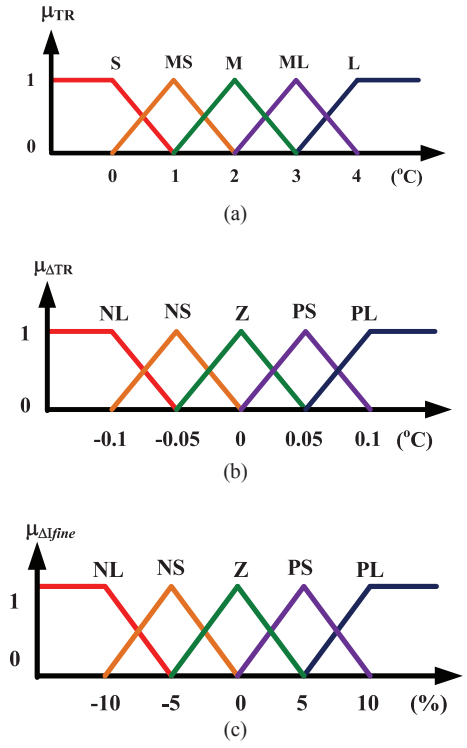


Fig. 7. MFs corresponding to (a) TR, (b) ΔTR, and (c) ΔI_{fine}.

In addition, according to the expert experience and knowledge base, the rule base of the incremental current ΔI_{fine} are derived in Fig. 8. From Fig. 8, the rule base consists of 25 IF-THEN inference rules (Rule01~Rule25) to derive the ΔI_{fine}.To do the fuzzy reasoning, fuzzy logic principles are applied to combine IF-THEN rules from the rule base into a mapping from fuzzy input sets to output sets. For example, the deducing rule can be described as if TR is small and ΔTR is negative large, then the ΔI_{fine} is positive large (PL, Rule 01) and so on. From Rule01, the fuzzy implication can be interpreted that the electrochemical reaction inside the battery was not severe and the temperature was low. Then the charging current can be increased to accelerate the chargingprocess. In this study, the COS defuzzification is utilized to convert the output subsets with different degrees of MF into quantized outputs. The gravity of the area activated can be computed by

$$Center = \frac{\sum_{i=1}^{n} Y(X_i) \cdot X_i}{\sum_{i=1}^{n} Y(X_i)} \tag{9}$$

Where the denominator term is the cumulative sum of each point function value $Y(X_i)$, and the numerator term is the position of each point on the X axis multiplied by the function value $Y(X_i)$.

IV. Experimental Results

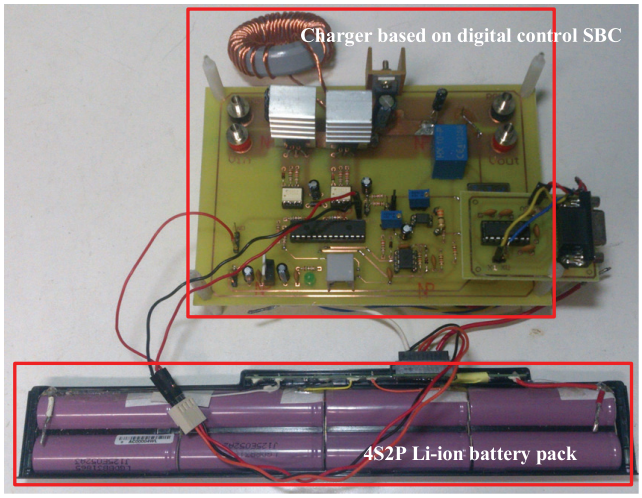
This section provides experimental results and waveform

TR / ΔTR	S	MS	M	ML	L
NL	PL (Rule01)	PL (Rule06)	PS (Rule11)	Z (Rule16)	Z (Rule21)
NS	PL (Rule02)	PS (Rule07)	PS (Rule12)	Z (Rule17)	NS (Rule22)
Z	PS (Rule03)	PS (Rule08)	Z (Rule13)	NS (Rule18)	NS (Rule23)
PS	Z (Rule04)	Z (Rule09)	NS (Rule14)	NS (Rule19)	NL (Rule24)
PL	NS (Rule05)	NS (Rule10)	NL (Rule15)	NL (Rule20)	NL (Rule25)

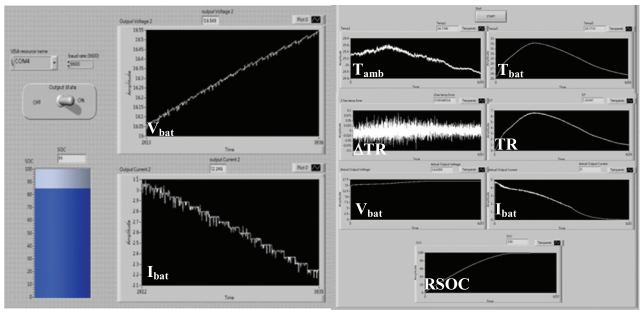
Fig. 8. Derivation of rule base for ΔI_{fine}.

measurements to verify the correctness and feasibility of the designed charger and proposed charging strategy. Test results obtained by the studied remaining capacity with fuzzy TR control (RCFTC) charging, remaining capacity charging (RCC), and conventional CC-CV method are analyzed and compared to emphasize the effectiveness and performance boost of the devised scheme in terms of temperature mitigation, charging efficiency, and life cycle. Fig. 9 shows the implemented charger prototype and the main menu of the developed GUI. From Fig. 9(a), the prototype consisits of a SBC-based power circuit with a MCU control core, the SOC and temperature guage ICs with communication protocoal interfaces, and the 4S2P battery pack under charge. The GUI, constructed by the LabVIEW software as illustrated in Fig. 9(b), shows the records of the pack voltage (V_{bat}), charging current (I_{bat}), battery external temperature (T_{bat}) and room temperature (T_{amb}), calculated temperature rise (TR) and 2-second temperature rise (ΔTR), and the remaining SOC (RSOC) online during the charging phase. To verify the designed charger, the waveforms of the output current (I_o), voltage (V_o), two gating signals (V_{GS1}, V_{GS2}) of the power switches generated by the MCU, and the efficiency are measured. The input voltage is 24 V. Fig. 10(a) and (b) show the measured V_{GS1} and V_{GS2} waveforms when the I_o is 4.4A and the V_o is equal to the minimal and maximum voltages of the battery pack, 12 V and 16.8 V, respectively. Obviouly, the charger current can maintain stable output in the variation range of the pack voltage. The measured waveforms prove that the circuit functions completely meet the demand of design specifications. The measured efficiency of the charger is depicted in Fig. 10(c). It can be observed that the design requirement with charger efficiency above 90% has been achieved in all load output range due to the use of the synchronous rectifier has reduced the conduction losses significantly. The maximum efficiency is 94.39% that occurs at near 17 W output power.

Two variable steps of the incremental current ΔI_{fine} (i.e. $\Delta I_{fine\_10\%}$ and $\Delta I_{fine\_20\%}$) were studied for the proposed RCFTC charging method to further check and clarify the effect of the temperature rise suppression. Fig. 11 illustrates the regulation mechanism of charging currents for different charging strategies. The variation of the generated TR obtained from different charging methods was shown in Fig. 12. The maximum and



(a)

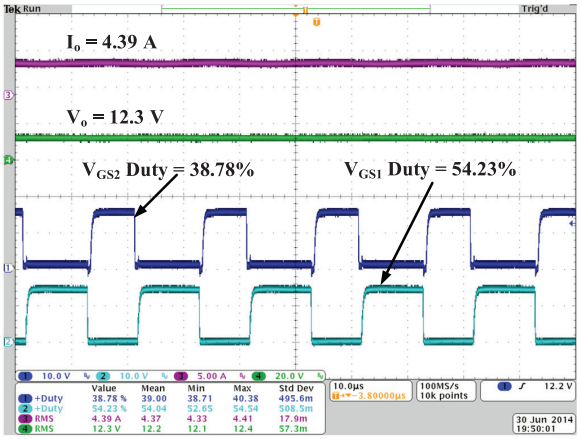


(b)

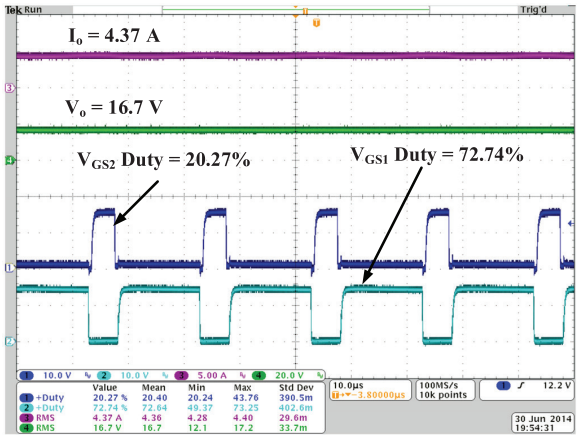
Fig. 9. (a) The implemented charger prototype, (b) The developed GUI.

average TRs obtained by different charging methods in three tests were tabulated in TABLE V. The charging time (CT), charging capacity (C_c), discharge capacity (C_d), and charging efficiency (η_c) measured with different charging approaches are summarized in TABLE VI. Where the charging efficiency η_c is defined as the ratio of the discharge capacity to capacity charged into battery during charging process. It can be observed that, from Fig. 11, in the initial stage of charging, the magnitude of the charging current modulation of the proposed RCFTC methods (for steps of $\Delta I_{fine\_10\%}$ and $\Delta I_{fine\_20\%}$) is less than other methods, thus drastic electrochemical stresses can be avoided. On the other hand, in spite of the full-charge terminated time is slightly longer than that of the counterpart methods, however, in the later phase of charging, the magnitude of the charging current regulation of the proposed RCFTC method is larger than other methods, so as to shorten the charging time. Therefore, the provided adaptive charging current profile can accomplish the research objectives successfully to subdue battery's TR and aging phenomenon. Accordingly, from Fig. 12, under the control of the TR suppression, the proposed RCFTC with 20% ΔI_{fine} step shows the remarkablere lieved effect on temperature rise and the charging efficiency also outperforms those of other counterpart methods obtained.

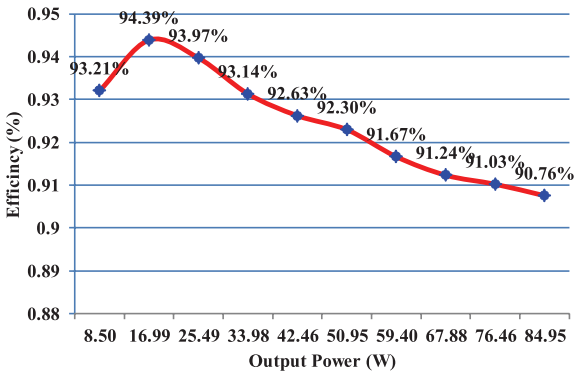
Furthermore, from TABLE V, as comparing the average TR of the three studied methods (RCC, RCFTC with $\Delta I_{fine\_10\%}$ and



(CH1:10 V/div, CH2:10 V/div, CH3:5 A/div, CH4:20 V/div)
(a)



(CH1:10 V/div, CH2:10 V/div, CH3:5 A/div, CH4:20 V/div)
(b)



(c)

Fig. 10. (a) Measured waveforms at 12 V output voltage, (b) Measured waveforms at 16.8 V output voltage, (c) Measured conversion efficiency of the utilized synchronous buck converter.

$\Delta I_{fine\_20\%}$) with that of the conventional CC-CV method, the average TRs have reduction of 18.5%, 23.2% and 31.24%, respectively. Obviously, the experimental results exactly reflect the theoretical argument and effectiveness of the proposed charging method. It is noted that, refer to TABLE V and VI, although the

TABLE V
MAXIMUM AND AVERAGE TRS OBTAINED BY DIFFERENT CHARGING METHODS

	CC-CV		RCC		RCFTC with $\Delta I_{fine\_10\%}$		RCFTC with $\Delta I_{fine\_20\%}$	
Test no.	Max. TR (°C)	Avg. TR (°C)	Max. TR (°C)	Avg. TR (°C)	Max. TR (°C)	Avg. TR (°C)	Max. TR (°C)	Avg. TR (°C)
1	9.382	5.451	7.328	4.550	7.232	4.338	6.634	3.879
2	9.567	5.547	6.954	4.454	7.081	4.231	6.310	3.661
3	9.495	5.551	7.527	4.480	6.857	4.140	6.500	3.839
Avg.	9.481	5.516	7.270	4.495	7.057	4.236	6.481	3.793

TABLE VI
MEASURED CT, CHARGING CAPACITY (C_C), DISCHARGING CAPACITY (C_D), AND CHARGING EFFICIENCY (η_C)

	CC-CV				RCC				RCFTC with $\Delta I_{fine\_10\%}$				RCFTC with $\Delta I_{fine\_20\%}$			
no.	CT(s)	C_c (Ah)	C_d (Ah)	η_c (%)	CT(s)	C_c (Ah)	C_d (Ah)	η_c (%)	CT(s)	C_c (Ah)	C_d (Ah)	η_c (%)	CT(s)	C_c (Ah)	C_d (Ah)	η_c (%)
1	7376	4.650	4.456	95.84	8461	4.665	4.541	97.35	8504	4.550	4.450	97.80	8765	4.661	4.549	97.60
2	7392	4.662	4.452	95.51	8369	4.657	4.535	97.39	8651	4.695	4.564	97.22	8849	4.663	4.558	97.75
3	7403	4.646	4.455	95.90	8216	4.657	4.537	97.38	8687	4.735	4.616	97.50	8839	4.651	4.562	98.09
Avg.	7390	4.653	4.455	95.75	8349	4.660	4.538	97.37	8614	4.660	4.544	97.51	8818	4.658	4.556	97.81

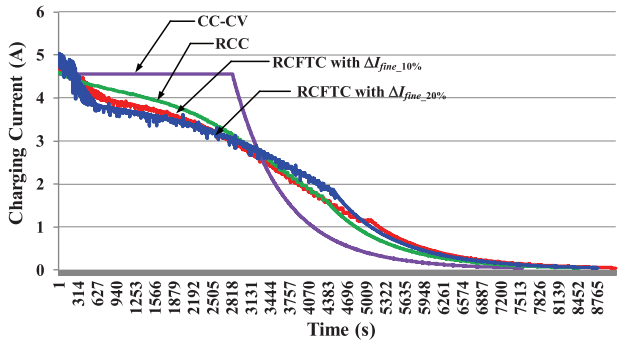


Fig. 11. Regulation of the charging current for different charging methods.

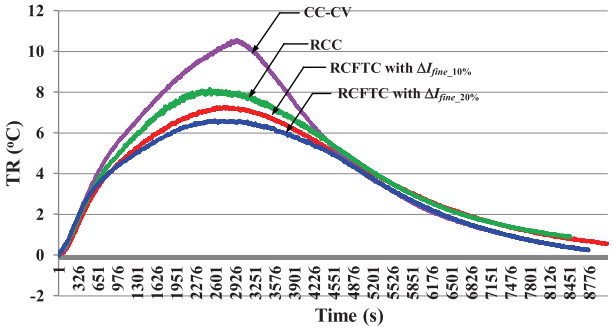


Fig. 12. Measured TR with different charging methods.

traditional CC-CV method has the shortest charging time, the temperature is high and the charging efficiency is low. The ratio of the RCC charging time to the CC-CV charging time, i.e. the CTR is 0.885, which is close to the expected 0.9. The CTRs of the RCFTC with $\Delta I_{fine\_10\%}$ and $\Delta I_{fine\_20\%}$ methods are 0.858 and 0.838, respectively. In addition, due to the less TR leads to the less energy loss and aging effect. Hence, the average charging efficiencies of the studied methods, as shown in TABLE VI, have 1.62%, 1.76% and 2.06% of improvements respectively as compared with that of the conventional CC-CV method. Therefore, the RCFTC charging mechanism proposed in this paper can effectively improve the charging efficiency and reduce the most temperature rise.

Finally, to prove the performance of the proposed method, battery cycling test was conducted. The studied RCFTC with $\Delta I_{fine\_10\%}$ and conventional CC-CV charging methods have been run to evaluate their service time. Two brand new cells with identical nominal capacity (2200 mAh) produced by the same manufacturer are used. Both cells were put into the thermostatic containerin which the operating temperature is maintained at 25°C to control the impact of the temperature factor on cycle life. Test conditions of one cycle period are set up as follows: for conventional CC-CV method, a 1-C current is used to charge one cell in CC mode, and then a CV mode is applied to fully charge battery. The next, discharge with 0.1 C is conducted until the discharge cut-off voltage is reached. Analogously, the proposed RCFTC with $\Delta I_{fine\_10\%}$ is run to fully charge the other cell, and then discharge with 0.1 C is done until the discharge cut-off voltage is reached. Fig. 13 illustrates the estimated relationship between RSOC drop (in %) and cycle numbers. From Fig. 13, the cycling numbers of the proposed RCFTC and CC-CV methods when the capacity drop to 97.3% of the original capacity are 151 and 96, respectively. Although the test has not been run until the battery capacity drops to the specified unusable level (e.g. 80%), yet under normal situation, the trend of capacity drop will remain fixed in the long-term cycling test with the same charging/discharging patterns. Consequently, the charging algorithm proposed in this paper can be estimated to provide 57.3% more cycle-life count than that of the conventional CC–CV method. The comparison result of the estimated cycle number test again demonstrates that the high temperature rise has severe impact on battery lifetime.

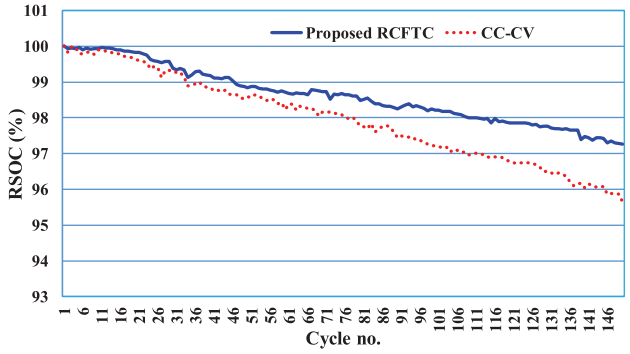


Fig. 13. Comparison of cycle life test between the proposed and the conventional CC-CV methods.

V. Conclusions

A digitally-controlled Li-ion battery charger with an adaptive charging strategy has been studied and developed in this paper. The devised charger can dynamically generate the desired charging profile depending on the battery SOC state and temperature variation, that is, the temperature changes of the battery and ambient have been considered in the proposed method. Accordingly, the proposed remaining capacity charging with fuzzy temperature control approach can avoid using high C-rate current to charge battery with high RSOC, and thus the phenomenon of the battery aging aggravation due to the extreme electrochemical stress can also be subdued.The power stage of the charger is implemented by the synchronous-rectified buck converter to further reduce the conduction loss. The firmware and GUI of the proposed system are constructed by a low-cost micro controllercore and LabVIEW software.

Experimental results validate the feasibility and effectiveness of the proposed charger and charging control strategy. The largest 31.24% reduction of the average temperature rise, 2.06% improvement of the charge efficiency, and estimated 57.3% increase in cycle-life count have been accomplished, while maintaining reasonable charging time, as compared-with the conventional CC-CV method. In addition, without need to build the exhaustive battery model, depending on the change in charging condition, the proposed strategy has taken the nonlinearity of the battery electrothermal behavior and the circuit parameter non-ideality into consideration to effectively achieve the temperature rise mitigation and lifespan extension through charging current dynamic regulation using fuzzy-based decision-making procedure. On the other hand, the proposed charging strategy reaches the charging performance melioration at the cost of a longer charging time needed than that of the CC-CV method, even though the CTR above 0.9 is chosen and the charging time increase still lies in an acceptable range. Accordingly, the future work will focus on exploring the optimum charging profile to substitute for the curve-fitting function in (8). Then a multi-objective function consisting of the charging time, energy loss, and temperature rise will be formulated and solved through advanced optimization algorithms to obtain the best trade-off among the competing objectives for efficient charging management.

References

[1] S. Habib *et al*., "A comprehensive study of implemented international standards, technical challenges, impacts and prospects for electric vehicles," *IEEE Access,* vol. 6, pp. 13866-13890, 2018.

[2] V. del Razo and H. A. Jacobsen, "Smart charging schedules for highway travel with electric vehicles," *IEEE Trans. on Transportation Electrification,* vol. 2, no. 2, pp. 160-173, June 2016.

[3] L. Lu, X. Han, J. Li, J. Hua, and M. Ouyang, "A review on the key issues for lithium-ion battery management in electric vehicles," *Journal of Power Sources*, vol. 226, pp. 272-288, Mar. 2013.

[4] A. Stippich *et al.*, "Key components of modular propulsion systems for next generation electric vehicles," *CPSS Trans. Power Electronics and Applications,* vol. 2, no. 4, pp. 249-257, Dec. 2017.

[5] M. A. Hannan, M. M. Hoque, A. Hussain, Y. Yusof, and P. J. Ker, "State-of-the-art and energy management system of Lithium-ion batteries in electric vehicle applications: issues and recommendations," *IEEE Access*, vol. 6, pp. 19362-19378, 2018.

[6] R. Xiong, J. Cao, Q. Yu, H. He, and F. Sun, "Critical review on the battery state of charge estimation methods for electric vehicles," *IEEE Access,* vol. 6, pp. 1832-1843, 2018.

[7] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151-2169, May 2013.

[8] V. Monteiro *et al*., "Experimental validation of a novel architecture based on a dual-stage converter for off-board fast battery chargers of electric vehicles," *IEEE Trans. Vehicular Technology,* vol. 67, no. 2, pp. 1000-1011, Feb. 2018.

[9] I. Subotic, N. Bodo, and E. Levi, "Single-phase on-board integrated battery chargers for EVs based on multiphase machines," *IEEE Trans. Power Electronics,* vol. 31, no. 9, pp. 6511-6523, Sept. 2016.

[10] K. Liu, K. Li, Z. Yang, C. Zhang, and J. Deng, "An advanced Lithium-ion battery optimal charging strategy based on a coupled thermo-electric model," *Electrochimica Acta*, vol. 225, no. 5, pp. 330-344, Jan. 2017.

[11] C. Zhang, K. Li, and J. Deng, "Real-time estimation of battery internal temperature based on a simplified thermoelectric model," *Journal of Power Sources*, vol. 302, pp. 146-154, Jan. 2016.

[12] F. Hoffart, "Proper care extends Li-ion battery life," *Power Electron. Technol. Mag.*, vol. 34, no. 4, pp. 24-28, Apr. 2008.

[13] C. H. Lin, C. Y. Hsieh, and K. H. Chen, "A Li-ion battery charger with smooth control circuit and built-in resistance compensator for achieving stable and fast charging," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 57, no. 2, pp. 705-712, Feb. 2010.

[14] B. M. Conlon, "How much capability do electric vehicles need to meet customer demands? Viewpoint," *IEEE Electrification Magazine,* vol. 5, no. 1, pp. 4-73, March 2017.

[15] R. Shi, S. Semsar, and P. W. Lehn, "Constant current fast charging of electric vehicles via a dc grid using a dual-inverter drive," *IEEE Trans. Industrial Electronics,* vol. 64, no. 9, pp. 6940-6949, Sept. 2017.

[16] S. A. El-Batawy and W. G. Morsi, "Optimal design of secondary distribution system considering electric vehicles high-power residential fast chargers," *IET Generation, Transmission & Distribution*, vol. 11, no. 14, pp. 3475-3484, 2017.

[17] K. M. Tsang and W. L. Chan, "Current sensorless quick charger for lithium-ion batteries," *Energy Conversion and Management*, vol. 52, no. 3, pp.1593-1595, 2011.

[18] P. H. L. Notten, J. H. G. Op het Veld, J. R. G. van Beek, "Boost-charging Li-ion batteries: A challenging new charging concept", *Journal of Power Source*, vol. 145, no. 1, pp. 89-94, Feb. 2005.

[19] L. R. Chen, J. J. Chen, N. Y. Chu, and G. Y. Han, "Current pumped battery charger," *IEEE Trans. Ind. Electron.,* vol. 55, no. 6, pp. 2482-2488, Jun. 2008.

[20] L. R. Chen, C. S. Liu, and J. J. Chen, "Improving phase-locked battery charger speed by using resistance-compensated technique," *IEEE Trans. Ind. Electron.,* vol. 56, no. 4, pp. 1205-1211, Apr. 2009.

[21] L. R. Chen, "Design of duty-varied voltage pulse charger for improv-

ing Li-ion battery-charging response," *IEEE Trans. Ind. Electron.,* vol. 56, no. 2, pp. 480-487, Feb. 2009.
[22] L. R. Chen, "A design of an optimal battery pulse charge system by frequency-varied technique," *IEEE Trans. Ind. Electron.,* vol. 54, no. 1, pp. 398-405, Feb. 2007.
[23] T. Ikeyaa, N. Sawadab, J. I. Murakamic, K. Kobayashi, M. Hattori, N. Murotani, S. Ujiie, K. Kajiyama, H. Nasu, H. Narisoko, Y. Tomaki, K. Adachi, Y. Mita, and K. Ishihara, "Multi-step constant-current charging method for an electric vehicle nickel/metal hydride battery with highenergy efficiency and long cycle life," *J. Power Sources,* vol. 105, no. 1, pp. 6-12, 2002.
[24] P. C. Lin, Y. H. Liu, Y. H. Liu, J. K. Chen, and C. H. Chen, "A fully digital rapid charger for electric scooters," in *Proc. Eighteenth Symp. Electrical Vehicles,* 2001, Session D7A, pp. 1-13.
[25] J. W. Huang, Y. H. Liu, S. C. Wang, and Z. Z. Yang, "Fuzzy-control-based five-step Li-ion battery charger," in *Proc. IEEE Power Electronics and Drive Systems Conf.,* Nov. 2009, pp. 1547-1551.
[26] F. J. Lin, M. S. Huang, P. Y.Yeh, H. C. Tsai, and C. H.Kuan, "DSP-based probabilistic fuzzy neural network control for Li-ion battery charger," *IEEE Trans. Power Electron*., vol. 27 no. 8, pp. 3782-3794, Aug. 2012.
[27] M. Charkhgard and M. Farrokhi, "State-of-charge estimation for lithium-ion batteries using neural networks and EKF," *IEEE Trans. Ind. Electron.,* vol. 57, no. 12, pp. 4178-4187, Dec. 2010.
[28] L. R. Chen, R. C. Hsu, and C. S. Liu, "A design of a grey-predicted Li-ion battery charge system," *IEEE Trans. Ind. Electron*., vol. 55, no. 10, pp. 3692-3701, Oct. 2008.
[29] H. Surmann, "Genetic optimization of a fuzzy system for charging batteries," *IEEE Trans. Ind. Electron*., vol. 43, no. 5, pp. 541-548, Oct.1996.
[30] S. C. Wang and Y. H. Liu, "A PSO-based fuzzy-controlled searching for the optimal charge pattern of Li-ion batteries," *IEEE Trans. Ind. Electron.,* vol. 62, no. 5, pp. 2983-2993, May 2015.
[31] S. Bashash, S. J. Moura, J. C. Forman, and H. K. Fathy, "Plug-in hybrid electric vehicle charge pattern optimization for energy cost and battery longevity," *J. Power Sources*, vol. 196, no. 1, pp. 541-549, 2011.
[32] Y. H. Liu, J. H. Teng, and Y. C. Lin, "Search for an optimal rapid charging pattern for lithium-ion batteries using ant colony system algorithm," *IEEE Trans. Ind. Electron*., vol. 52, no. 5, pp. 1328-1336, Oct. 2005.
[33] A. Abdollahi *et al*., "Optimal battery charging, Part I: Minimizing time-to-charge, energy loss, and temperature rise for OCV-resistance battery model," *Journal of Power Sources,* vol. 303, pp. 388-398, Jan. 2016.
[34] C. Zhang *et al*., "Charging optimization in lithium-ion batteries based on temperature rise and charge time," *Applied Energy,* vol. 194, pp. 569-577, 2017.
[35] H. Fang, Y. Wang, and J. Chen, "Health-aware and user-involved battery charging management for electric vehicles: linear quadratic strategies," *IEEE Transactions on Control Systems Technology,* vol. 25, no. 3, pp. 911-923, May 2017.
[36] C. Zou, X. Hu, Z. Wei, T. Wik, and B. Egardt, "Electrochemical estimation and control for lithium-ion battery health-aware fast charging," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 8, pp. 6635-6645, Aug. 2018.
[37] H. E. Perez, X. Hu, S. Dey, and S. J. Moura, "Optimal charging of Li-ion batteries with coupled electro-thermal-aging dynamics," *IEEE Transactions on Vehicular Technology,* vol. 66, no. 9, pp. 7761-7770, Sept. 2017.
[38] Y. H. Liu and Y. F. Luo, "Search for an optimal rapid-charging pattern for Li-ion batteries using the Taguchi approach," *IEEE Trans. Ind. Electron*., vol. 57, no. 12, pp. 3963-3971, Dec. 2010.
[39] Y. H. Liu, C. H. Hsieh, and Y. F. Luo, "Search for an optimal five-step charging pattern for Li-ion batteries using consecutive orthogonal arrays," *IEEE Trans. Energy Convers.,* vol. 26, no. 2, pp. 654-661, Jun. 2011.
[40] C. L. Liu, Y. S. Chiu, Y. H. Liu, Y. H. Ho, and S. S. Huang, "Optimization of a fuzzy-logic-control-based five-stage battery charger using a fuzzy-based Taguchi method," *Energies,* vol. 6, no. 7, pp. 3528-3547, 2013.
[41] M. Yu, Y. Barsukov, and M. Vega, "Theory and implementation of impedance track™ battery fuel-gauging algorithm in bq2750x family," *TI. Application Report,* 2008.
[42] Microchip Technology Inc, "dsPIC33FJ06GS101/X02 and dsPICF J16GSX02/X04," [Online]. Available: //http://www.microchip.com.

Shun-Chung Wang received the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1995.

He is currently with the Department of Electrical Engineering, Lunghwa University of Science and Technology, Taoyuan, Taiwan. His current research interests include power electronics and their applications.

Guan-Jhu Chen was born in Taichung, Taiwan, R.O.C., in 1990. He received the B.S. degree in electrical engineering from Kun Shan University in 2012, and M.S. degree in electrical engineering from National Taiwan University of Science and Technology (NTUST) in 2014. He is currently pursuing a Ph.D. degree in the department of electrical engineering at NTUST. His research interests include power electronics, digital power control and Li-ion battery charging algorithm.

Yi-Hua Liu received the Ph.D. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1998. He joined the Department of Electrical Engineering, Chang-Gung University, Taoyuan, Taiwan, in 2003. He is currently in the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan. His current research interests include the areas of power electronics and battery management.

Control of Neutral-Point Voltage in Three-Phase Four-Wire Three-Level NPC Inverter Based on the Disassembly of Zero Level

Chenchen Wang, Zhitong Li, Xiahe Si, and Hongliang Xin

***Abstract*—It is important to maintain the neutral-point (NP) voltage balanced for the three-phase four-wire three-level neutral-point clamped (NPC) inverter. In this paper, after detailed discussion, a mathematical model of the neutral-point voltage are derived. Then a novel control strategy is proposed based on the disassembly of zero level (*O* Level) to maintain the neutral-point potential. A variable named neutral-point control margin (NPCM) is defined to represent the disassembly margin of each phase. The zero level of one of the three phase is disassembled quantitatively after calculation. Furthermore, the neutral-point voltage can keep balanced while the average output voltage remains unchanged. The proposed control strategy is verified by simulation and experiments.**

***Index Terms*—Neutral-point control margin, neutral-point voltage balance, three-level NPC converters, three-phase four-wire.**

I. Introduction

THREE-PHASE four-wire inverter is widely adopted in industrial applications, such as active power filter (APF), distribution static compensator (DSTATCOM) and uninterrupted power source (UPS). This is mainly because it can generate and control zero-sequence component independently [1]-[3].

Among all the three-phase four-wire inverters, the three-level neutral-point-clamped (NPC) inverter is one of the most popular type because of less switching stress, switching loss and lower EMI [4]. In three-phase four-wire applications, there are mainly two ways to provide the neutral line: one is to use the three-level four-leg NPC topology [5]-[7]; and the other is to connect the neutral-point of the DC bus to the midpoint of the three-phase load. This is called three-leg split capacitor NPC inverter [8]. Although it is easier to control the zero-sequence component in the four-leg topology, it needs more switching components, diodes, pulse-triggered terminals and drives, which increase the cost and complexity of implementation. The three-leg split capacitor NPC inverter is a more economical solution, and is easier to control. Hence, the three-level three-leg NPC inverter, as shown in Fig. 1, is researched in this paper.

Due to the structural characteristics, the NP voltage must be maintained balanced to ensure the normal operation of three-level NPC inverter. Many strategies have been proposed to balance the NP voltage, which can be mainly divided into the two categories. The first one is based on space vector modulation (SVPWM). There are 27 vectors of 19 kinds in a three-level NPC converter. As a result, the balance of NP voltage can be achieved by modifying the appropriate redundant small vectors and adjusting the dwell time [9]-[10]. The other one is based on carrier pulse width modulation. The balance of NP voltage can be realized by injecting zero-sequence voltage into the modulation voltages [11]-[13]. However, those strategies cannot fully eliminate the low-frequency fluctuation of NP voltage. To solve this problem, a strategy named two modified modulation algorithm has been proposed in [14]-[15]. Low-frequency fluctuation can be fully eliminated while it will also increase the switching frequency and harmonic component.

The strategies introduced above cannot be used in three-phase four-wire system because of the additional fourth wire. There are also some solutions proposed to control the NP voltage of three-phase four-wire NPC inverter. In [16]-[18], the zero-sequence voltage/current injection method based on carrier-based modulation is proposed to control the NP voltage. Although it can balance the NP voltage, it cannot reduce the amplitude of NP voltage fluctuation, and what's worse, it changes the output voltage of each phase. In [19]-[21], the control methods based on vectors selection in α-β-o coordinates and a-b-c coordinates are proposed. However, this method is complex and not easy for the digital implementation.

In this paper, based on the fluctuation mechanism of NP voltage in three-phase four-wire three-level NPC inverter, a new control strategy based on the disassembly of zero level is proposed. The validity of the strategy is verified through the simulation and experiments.

II. Principle Analysis of the Neutral-Point Voltage Fluctuation

The three-phase four-wire three-level NPC inverter is presented in Fig. 1, where V_{dc} is the DC-bus voltage. Phase j ($j = a$, b, c) outputs P level when T_{j1} and T_{j2} are on and T_{j3} and T_{j4} are off, O level when T_{j2} and T_{j3} are on and T_{j1} and T_{j4} are off, and N level when T_{j3} and T_{j4} are on and T_{j1} and T_{j2} are off.

$V_{dc}/2$ is chosen as the base value to calculate the Per-Unit value of the three-phase output voltages, which are defined as follows:

Manuscript received November 18, 2017.

The authors are with Beijing Jiaotong University, Beijing, China (email: chchenwang@bjtu.edu.cn; zhitonglir@bjtu.edu.cn; 13121463@bjtu.edu.cn; xinhongliang@bjtu.edu.cn).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00021

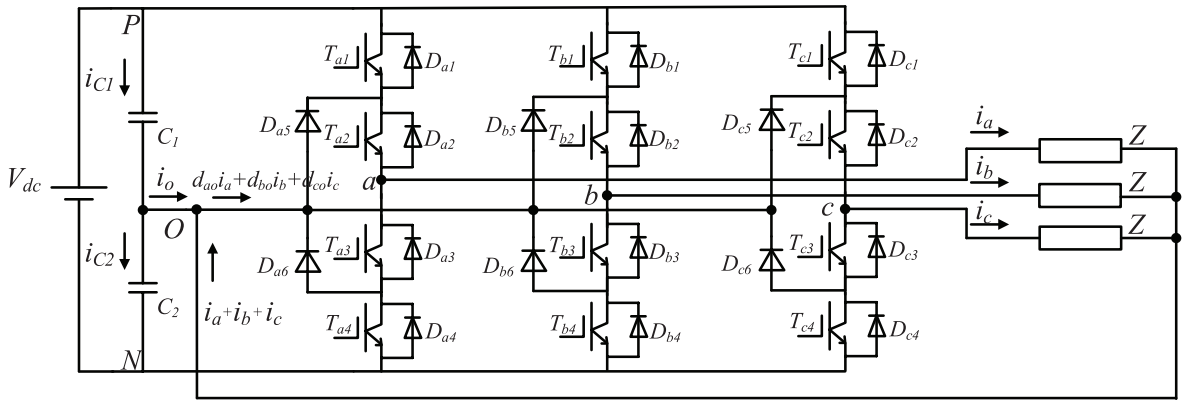


Fig. 1. Three-phase four-wire three-level NPC inverter.

$$\begin{cases} v_{ao} = M\cos(\theta) \\ v_{bo} = M\cos(\theta - 2\pi/3) \\ v_{co} = M\cos(\theta + 2\pi/3) \end{cases} \tag{1}$$

Where M is the modulation ratio ($0 \le M \le 1$).

Different from the three-wire topology, the neutral wire in four-wire structure is connected directly to the neutral-point of the DC bus. As a result, the three-phase four-wire three-level NPC inverter can be regarded as the combination of three single-phase inverters. It can be analyzed that when phase j outputs O level, the phase current i_j will flow through D_{j5} and T_{j2} or T_{j3} and D_{j6}, and return to or from the neutral point of the DC-bus capacitors through the neutral wire. The NP current i_o will not be influenced in this case. When phase j outputs P level, i_j will flow through the neutral wire and DC-bus capacitors. Thus, it will have an influence on i_o. Similarly, when phase j outputs N level, i_j will change i_o. Thus, it can be drawn that when one of the three phases outputs P or N level, i_o will be changed and lead to the drift of NP voltage. For convenience, define the variable S_{jo} that indicate the state of inverter output as follows:

$$S_{jo} = \begin{cases} 1, & \text{when outputs } O \text{ level} \\ 0, & \text{when outputs } P \text{ or } N \text{ level} \end{cases} \tag{2}$$

And then, the instantaneous value of the neutral current i_o shown in Fig. 1 can be achieved:

$$i_o = S_{ao}\cdot i_a + S_{bo}\cdot i_b + S_{co}\cdot i_c - (i_a + i_b + i_c) \tag{3}$$

When the switching frequency is high enough, it can be regarded that the current remains unchanged during every switching period. The average current can be given according to Fig. 1. according to the Kirchhoff's law:

$$\begin{aligned} \overline{i_o} &= d_{ao}\cdot i_a + d_{bo}\cdot i_b + d_{co}\cdot i_c - i_a - i_b - i_c \\ &= -i_a\cdot|v_{ao}| - i_b\cdot|v_{bo}| - i_c\cdot|v_{co}| \\ &= -\sum_{j=a,b,c} i_j\cdot|v_{jo}| \end{aligned} \tag{4}$$

Where d_{jo} is the duty ratio of O level in one switching period. i_j is the phase current. The relationship between d_{jo} and v_{jo} is as follows [22]:

$$d_{jo} = 1 - |v_{jo}| \tag{5}$$

It can be found that the three-wire and four-wire topology share the same average neutral-point current expression, as is shown in (4) [11]. However, the principles of NP voltage imbalance between these two structures are different.

Based on the discussion above, the control of NP voltage can be converted to the control of NP current i_o. Thus, as long as the NP current i_o can be kept to zero through a certain control strategy, the NP voltage can keep balanced.

III. The Neutral-Point Voltage Control Strategy Based on the Disassembly of Zero Level

The purpose of NP voltage control is to compensate the voltage offset between the upper and lower capacitors. This voltage offset consists of two parts, one is the voltage offset at the beginning of each switching period, and the other is the voltage offset during this switching period, which needs to be predicted.

A. Principle of O Level Disassembly

It can be seen from (4) that the NP current i_o is related to the output voltage and current of each phase. In [14], the author proposes a strategy to balance the NP voltage for the three-wire NPC inverter. It keeps the average NP current to zero during each switching period. Consequently, the average voltage of the DC-bus capacitors can be maintained constant. Although this strategy can only be applied to the three-wire NPC inverter, its idea can be migrated to the four-wire NPC inverter.

In a three-phase four-wire three-level NPC system, the NP voltage will be affected by phase current i_j only when phase j outputs P or N level. As a result, if the duty ratio of O level is disassembled to P and N level according to the NP voltage offset, the average NP current will be changed. The fluctuation of the NP voltage can be decreased or even eliminated through this process.

This can be described by Fig. 2. The original modulation sig-

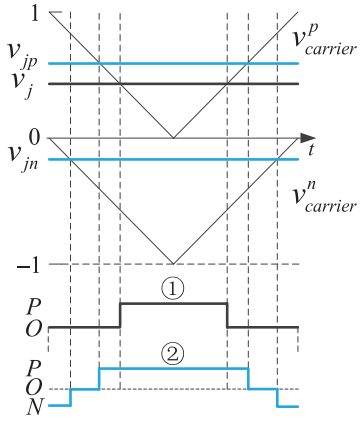


Fig. 2. Modulation based on disassembly of *O* level.

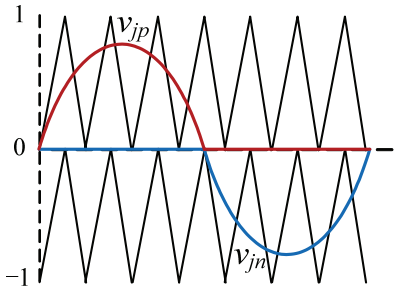


Fig. 3. Waveforms of modulation and carrier signals.

nal v_j is disassembled to v_{jp} and v_{jn} as follows:

$$v_j = v_{jp} + v_{jn} \quad (j = a, b, c) \tag{6}$$

The modulation principle is shown in (7):

$$V_j = \begin{cases} P, & v_{jp} > v^p_{carrier} \;\&\&\; v_{jn} > v^n_{carrier} \\ O, & v_{jp} < v^p_{carrier} \;\&\&\; v_{jn} > v^n_{carrier} \\ N, & v_{jp} < v^p_{carrier} \;\&\&\; v_{jn} < v^n_{carrier} \end{cases} \tag{7}$$

As is shown in Fig. 2, the output pulse ① is transferred to ② in this method. The *O* level has been disassembled to *P* and *N* level, so that the disassembly of *O* level can be achieved.

Actually, the phase disposition (PD) SPWM in [23] can be regarded as a kind of two modified modulation signals to some extent. In Fig. 3, the modulation signal of the PD-SPWM can be divided into the red (upper) and blue (lower) signals. Define the upper and lower signals as v_{jp} and v_{jn}. It can be found that they follow the rule given in (7), and also satisfy $v_{jp} >= 0$, $v_{jn} <= 0$ and $v_{jn}+1 >= v_{jp}$.

B. The Proposed Neutral-Point Control Strategy

Define V_{C1_mea}, V_{C2_mea} as the initial voltage of the upper and lower capacitors. Assume $\bar{i}_{C1}$, $\bar{i}_{C2}$ are the average currents that flow through the upper and lower capacitors respectively during one switching period. The NP voltage offset between the upper and lower capacitors during one switching period can be expressed as follows:

$$\begin{aligned} \Delta V_{dc\_pre} &= \frac{T_s}{C}(\bar{i}_{C1} - \bar{i}_{C2}) = \frac{T_s}{C}\bar{i}_o \\ &= -\frac{T_s}{C}\left(i_a|v_a| + i_b \cdot |v_b| + i_c \cdot |v_c|\right) \end{aligned} \tag{8}$$

Where *C* is the capacitance value of each DC capacitor. The total offset value of the NP voltage difference is:

$$\Delta V_{dc} = \Delta V_{dc\_pre} + V_{C1\_mea} - V_{C2\_mea} \tag{9}$$

So, the NP voltage offset needed to compensate will be:

$$\Delta V_{dc\_com} = -\Delta V_{dc} \tag{10}$$

In order to minimize the switching loss, only one phase will be selected to disassembled its *O* level. The time needed to be disassembled is obtained as:

$$\Delta t_{dis\_j} = -C \cdot \Delta V_{dc\_com} / i_j \quad (j = a, b, c) \tag{11}$$

Δt_{dis_j} is theoretical disassembly time of phase *j*. It can be positive or negative. Only a phase with positive Δt_{dis_j} can be chosen to disassemble its *O* level. Also, only when Δt_{dis_j} is smaller than the *O* level time of phase *j*, the NP voltage offset can be fully compensated. As a result, proper phase should be chosen to compensate the NP voltage offset.

According to the analysis above, a variable indicating the neutral-point control margin (*NPCM*) is defined as follows:

$$NPCMj = -sign(\Delta V_{dc\_com}) \cdot \left[1 - |v_j|\right] \cdot i_j \quad (j = a, b, c) \tag{12}$$

NPCM is related to the phase current, initial duty ratio of *O* level and the polarity of the compensation voltage. It represents the ability to compensate the offset. If *NPCMj* is positive, the NP voltage offset can be suppressed through disassembling *O* level of phase *j*. Moreover, the greater the *NPCMj* is, the more voltage offset it can be compensated. In order to select the proposer phase to compensate the NP voltage offset, the following cases are discussed:

1) If *NPCM* of all the three phases are smaller than zero. The NP voltage offset cannot be compensated and no phases need to be disassembled in this case.
2) If any of the three *NPCM* are greater than zero, phase with the largest *NPCM* will be selected to disassemble the *O* level.

Assume phase *j* is selected, then the practical disassembling time $\Delta t'_{dis\_j}$ can be obtained by the following discussion:

1) If the theoretical disassembling time Δt_{dis_j} is smaller than the *O* level time of phase *j*, the practical disassembly time is equal to the theoretical disassembly time:

$$\Delta t'_{dis\_j} = \Delta t_{dis\_j} \quad \left(\Delta t_{dis\_j} < \left(1 - |v_j|\right) \cdot T_s\right) \tag{13}$$

2) If the theoretical disassembling time Δt_{dis_j} is larger than the *O* level time of phase *j*, all the *O* level needs to be dis-

assembled:

$$\Delta t'_{dis\_j} = \left(1-\left|v_j\right|\right)\cdot T_s - t_0 \quad \left(\Delta t_{dis\_j} \geq \left(1-\left|v_j\right|\right)\cdot T_s\right) \tag{14}$$

Meanwhile, in order to avoid switching from *N* level to *P* level directly and causing a greater *dv*/*dt*, a short time named t_0 should be subtracted from the practical disassembly time in this case.

In conclusion, the practical disassembly time of phase *j* can be expressed as follows:

$$\Delta t'_{dis\_j} = \min\left\{\Delta t_{dis\_j},\ \left(1-\left|v_j\right|\right)\cdot T_s - t_0\right\} \tag{15}$$

Where t_0 can be defined as the double of the dead time.

C. Implementation of Proposed Strategy With O Level Disassembling

According to Fig. 2, the relationship between disassembly value Δv_j and practical disassembly time $\Delta t'_{dis\_j}$ is:

$$\Delta v_j = \Delta t'_{dis\_j} / T_s \quad (j = a,b,c) \tag{16}$$

The duty ratio of *O* level is disassembled to *P* and *N* level equally. As a result, the modulation signal v_{jp} and v_{jn} can be obtained as:

$$v_{jp} = \begin{cases} v_j + \Delta v_j/2, & v_j \geq 0 \\ \Delta v_j/2, & v_j < 0 \end{cases} \tag{17}$$

$$v_{jn} = \begin{cases} -\Delta v_j/2, & v_j \geq 0 \\ v_j - \Delta v_j/2, & v_j < 0 \end{cases} \tag{18}$$

The modulation principle is the same as discussed above. For example, the switching state of T_{j1} and T_{j3} is determined by the upper modulation signals v_{jp} and carrier signals $v^p_{carrier}$, and the switching state of T_{j2} and T_{j4} is determined by the lower modulation signals v_{jn} and carrier signals $v^n_{carrier}$.

In conclusion, the NP voltage control strategy can be subdivided into following steps, just as the Fig. 4 shows:

1) Compute the three-phase reference voltages, and measure the three-phase output currents and voltage offset between upper and lower capacitors.
2) Compute the compensation voltage ΔV_{dc_com}.
3) Obtain the *NPCMa*, *NPCMb* and *NPCMc* by (12). Select the proper phase to be disassembled.
4) Determine the disassembly value Δv_j, and obtain the modified modulation signals.
5) Generate the modulation signals.

IV. Comparison Between the Control Strategy and 3-D SVM Control Strategy

In [20], a control strategy based on 3-D SVM is proposed and could suppress the fluctuation of NP voltage.

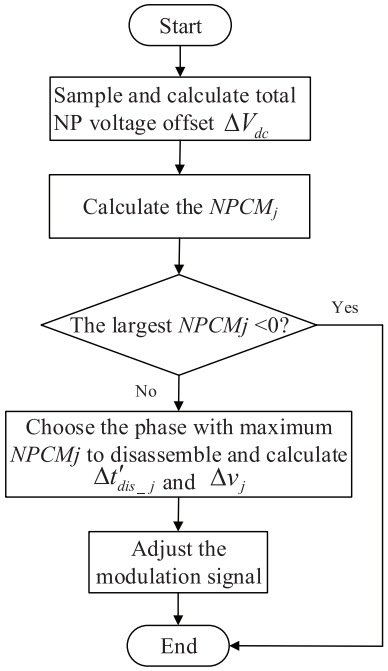


Fig. 4. The processing flowchart of the proposed algorithm and the whole modulation flow.

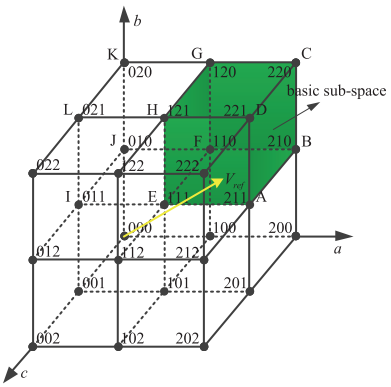


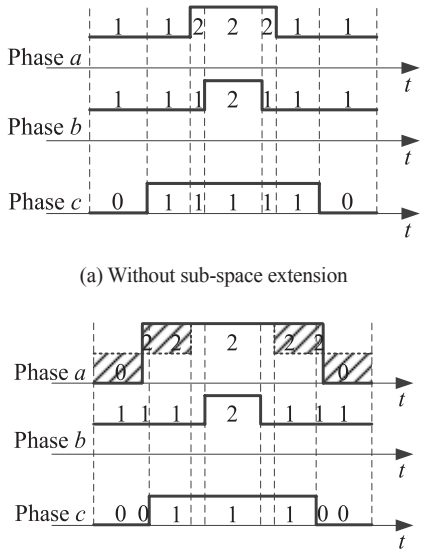
Fig. 5. Distribution of space vectors in *a*-*b*-*c* coordinates.

The distribution of space vectors in *a*-*b*-*c* coordinates is shown in Fig. 5. The number 2, 1 and 0 stand for the switching states when the inverter outputs *P, O* and *N* level, respectively. In order to suppress the NP voltage offset, vectors used to composite the reference vector $\boldsymbol{V}_{ref}$ are not limited to the tetrahedron. The sub-space needs to be extended so that more vectors can be selected. The strategy proposed in [20] extends the sub-space of $\boldsymbol{V}_{ref}$ based on the theory of *Factor of Neutral-point Balance (Fn)*. It selects the vectors which can suppress the offset of NP voltage to synthesize $\boldsymbol{V}_{ref}$.

Assume the three-phase reference voltages are $v_a = 0.3$, $v_b = 0.2$, $v_c = -0.4$, and the coordinate of $\boldsymbol{V}_{ref}$ is (1.3,1.2,0.6) which is located in the tetrahedron ADEF of sub-space A~H. Originally, the four space vectors located at the vertexes of tetrahedron ADEF are selected to synthesize $\boldsymbol{V}_{ref}$. The pulse sequence is as the Fig. 6(a) shows. In order to suppress the offset of NP voltage, when the maximum of *Fns* is larger than zero, e.g., *Fna*,

TABLE I
SIMULATION AND EXPERIMENT PARAMETERS

Item	Parameter	Item	Parameter
DC-bus voltage	V_{dc} = 540 V	Symmetrical reference voltages	$\begin{cases} v_a = 0.5\sin\theta \\ v_b = 0.5\sin(\theta - 2\pi/3) \\ v_c = 0.5\sin(\theta + 2\pi/3) \end{cases}$
Upper/lower capacitor	$C_1 = C_2$ = 1000 μF		
Output frequency	50 Hz	Asymmetrical reference voltages	$\begin{cases} v_a = 0.5\sin\theta \\ v_b = 0.5\sin(\theta - 2\pi/3) \\ v_c = 1.0\sin(\theta + 2\pi/3) \end{cases}$
Switching frequency	4 kHz		
LC filter	L = 5 mH, C = 20 μF	Resistive load	Balanced load: $R_a = R_b = R_c = 12\,\Omega$ Unbalanced load: $R_a = R_b = 12\,\Omega$, $R_c = 24\,\Omega$



(a) Without sub-space extension

(b) With sub-space extension

Fig. 6. Example of output waveforms by 3-D SVM strategy.

the sub-space needs to be extended along the direction of axis *a*. As a result, the sub-space is extended to the cuboid A~L, and $\boldsymbol{V}_{ref}$ is located in the tetrahedron ABDJ. The pulse sequence is as shown in Fig. 6(b). Similarly, other axis can be analyzed from the way mentioned above.

It can be seen from Fig. 6 that the duty ratio of *O* level is fully and equally disassembled to *P* and *N* level for the phase selected for sub-space extension. Actually, it can be considered that 3D-SVM is a special case of the proposed method. However, the *O* level can only be fully disassembled to *P* and *N* level in the 3-D SVM method, and it cannot be quantitative. What's more, under some conditions, 3-D SVM would disassemble two phases in one switching period to balance the DC side. This would increase the switching loss a lot. The control strategy proposed in this paper solves the defect of 3-D SVM: it can compensate the offset of NP voltage accurately and what's more, quantitatively.

V. SIMULATION AND EXPERIMENTAL RESULTS

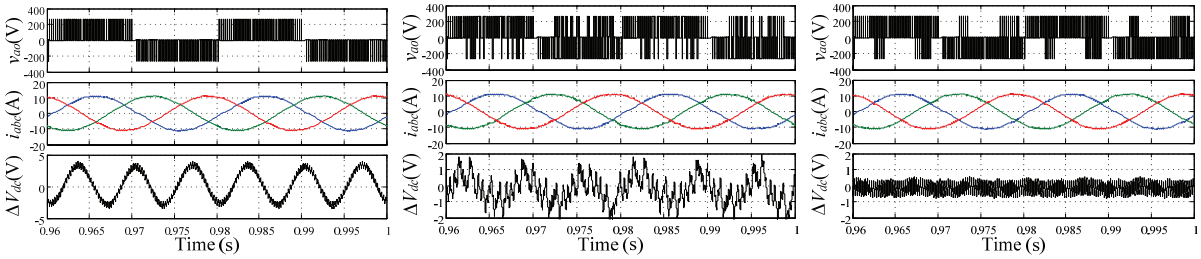
To validate the proposed NP voltage control strategy and compare its NP voltage control performance with the 3-D SVM method, simulation and experiments are carried out in this section. The system parameters are shown in TABLE I. Fig. 7 and Fig. 8 present the simulation and experimental results respectively under the balanced load and symmetrical three-phase reference voltages. Fig. 9 and Fig. 10 present the simulation and experimental results respectively under the unbalanced load and symmetrical three-phase reference voltages. Fig. 11 and Fig. 12 present the simulation and experimental results respectively under the unbalanced load and asymmetrical three-phase reference voltages. It can be seen that the NP voltage fluctuation is suppressed under all the three conditions. Moreover, the proposed strategy has a better control performance over the 3-D SVM method.

The FFT analysis for current of phase *a* under the three conditions are shown in Fig. 13. It can be seen that the THD is a little worse when adopting the proposed strategy. It is mainly because the switching frequency is higher than before and there are more low-order harmonics in the output current.

In practical applications, the nominal capacitance of capacitor is different from its actual value. Usually, for a capacitor with accuracy of "K", there will be a ±10% error. In order to find out the impact of accuracy of capacitor value on the proposed control performance, simulation is taken below under all the three conditions mentioned in TABLE I. For each figure, the capacitance is 900 μF in the upper one and 1100μF in the lower one.

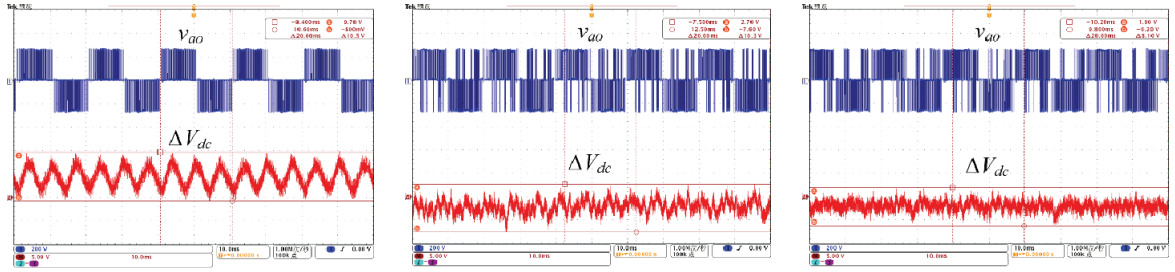
Compared Fig. 14 with Fig. 7(c), Fig. 9(c), Fig. 11(c), it can be found that the accuracy of capacitors do not have an obvious impact on the proposed strategy. The offset of NP voltage is compensated and the ripple is eliminated to a certain extent. However, when the actual capacitance is bigger than its nominal value, the control effect is a little better than the other condition.

What's more, the dynamic performance of the proposed strategy has been verified under sudden change of phase currents. Simulations have been carried out under two circumstances: (a) initially, Ra = Rb = Rc = 12 Ω, and changes to Ra = Rb = Rc =



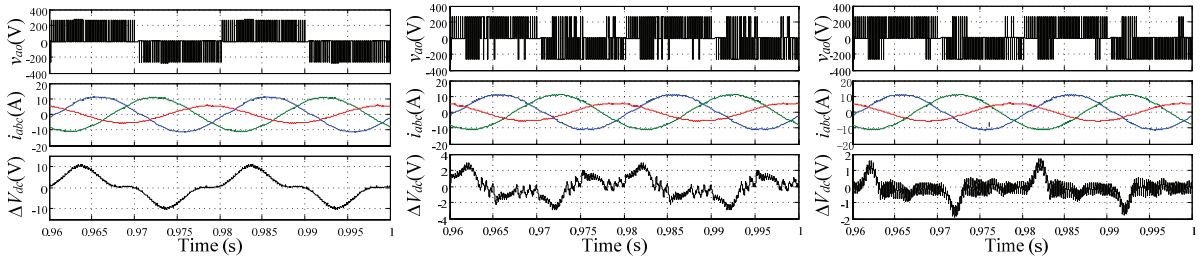
(a) Without neutral-point voltage control (b) 3-D SVM control strategy (c) Proposed control strategy

Fig. 7. Simulation results under the balanced load and symmetrical three-phase reference voltages.



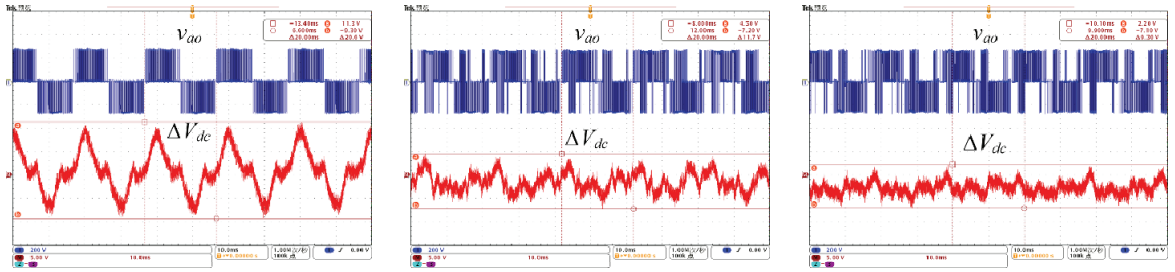
(a) Without neutral-point voltage control (b) 3-D SVM control strategy (c) Proposed control strategy

Fig. 8. Experimental results under the balanced load and symmetrical three-phase reference voltages.



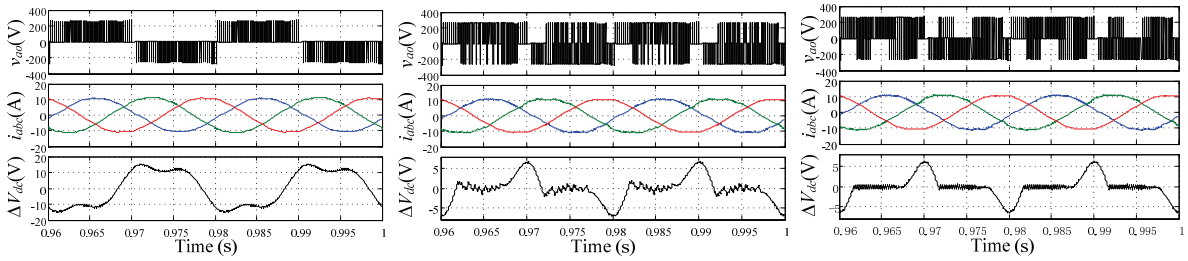
(a) Without neutral-point voltage control (b) 3-D SVM control strategy (c) Proposed control strategy

Fig. 9. Simulation results under the unbalanced load and symmetrical three-phase reference voltages.



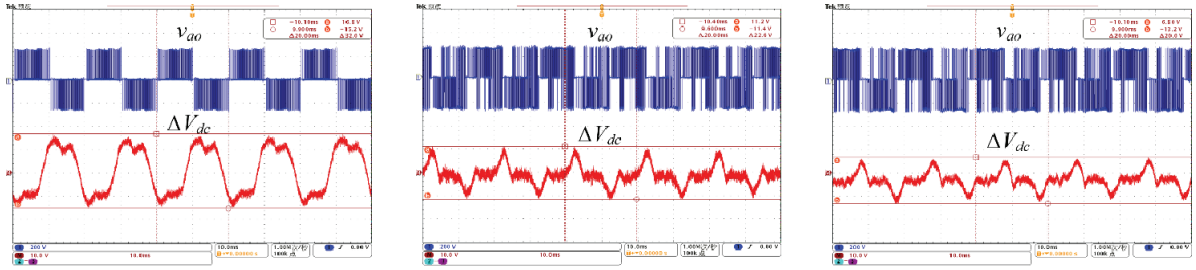
(a) Without neutral-point voltage control (b) 3-D SVM control strategy (c) Proposed control strategy

Fig. 10. Experimental results under the unbalanced load and symmetrical three-phase reference voltages.



(a) Without neutral-point voltage control (b) 3-D SVM control strategy (c) Proposed control strategy

Fig. 11. Simulation results under the unbalanced load and asymmetrical three-phase reference voltages.



(a) Without neutral-point voltage control (b) 3-D SVM control strategy (c) Proposed control strategy

Fig. 12. Experimental results under the unbalanced load and asymmetrical three-phase reference voltages.

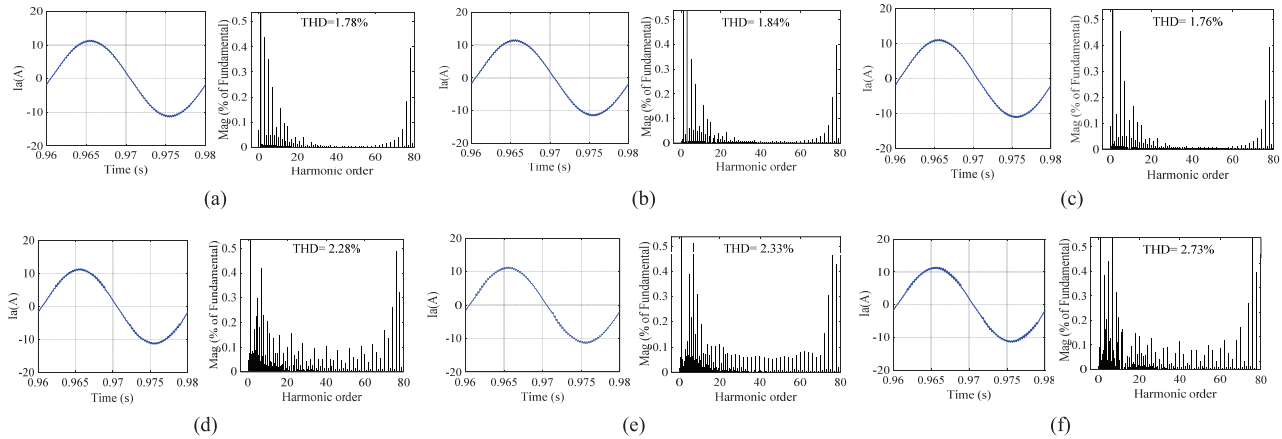


Fig. 13. FFT analysis results of output current of phase a: (a) and (d) are under the balanced load and symmetrical three-phase reference voltages. (b) and (e) are under the unbalanced load and symmetrical three-phase reference voltages. (c) and (f) are under the unbalanced load and asymmetrical three-phase reference voltages. (a), (b) and (c) show the results without NP voltage control. (d), (e) and (f) show the results with proposed control strategy.

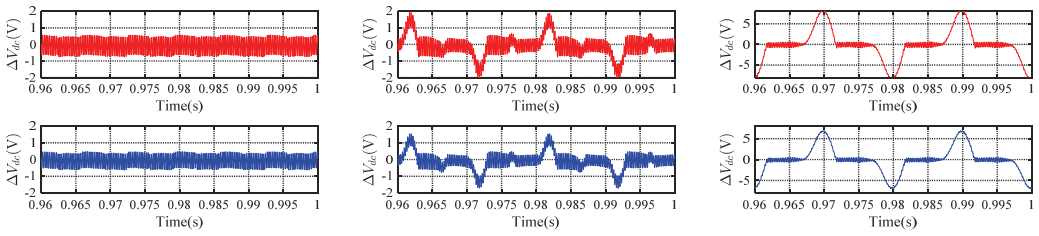


Fig. 14. Simulation results for testing the impact of capacitor accuracy on proposed control strategy: (a) Balanced load and symmetrical reference voltage. (b) Unbalanced load and symmetrical reference voltage. (c) Unbalanced load and asymmetrical reference voltage.

24 Ω when t = 0.98s; (b) initially, Ra = 24 Ω, Rb = Rc = 12 Ω, and changes to Ra = Rb = Rc = 12 Ω when t = 0.98 s. The simulation results are shown in Fig.15. The images from top to bottom is v_{ao}, i_{abc}, and ΔV_{dc} . It can be seen that the transitional process of NP voltage is very short, and the NP voltage ripple is well controlled under the new steady state. The proposed strategy has a good dynamic performance.

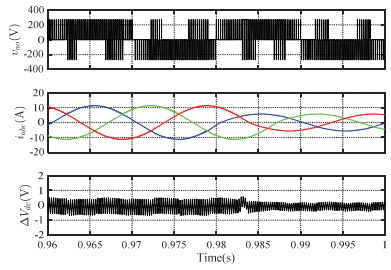
The power losses of the proposed strategy are analyzed in the following part. Power device used in this study is the F3L75R07W2E3_B11 from INFINEON, rated at 650 V, 75 A. The power losses of the converter can be classified into two parts: conduction and switching losses from the IGBT and its freewheeling diodes. Calculation method adopted in this paper is similar to the one adopted in [24]. The threshold voltage and on-state resistance of IGBT and diode are calculated based on the V_{CE} versus I_C and V_F versus I_F figures provided in the technical information book of the IGBT modules. Results are given in TABLE II. In this analysis, the gate voltage is assumed to be 15 V which is a typical one and the junction temperature is 150 °C which is the worst case.

Then the conduction losses of the power devices can be approximated as:

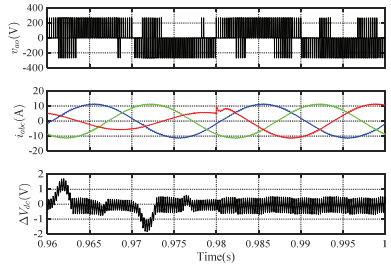
$$P_{T\_conduct} = \frac{1}{T}\int_0^T (V_T + i_F R_T) i_F dt \tag{19}$$

$$P_{D\_conduct} = \frac{1}{T}\int_0^T (V_D + i_F R_D) i_F dt \tag{20}$$

where $P_{T\_conduct}$ and $P_{D\_conduct}$ is the conduction losses of transistor



(a)



(b)

Fig. 15. Simulation results for testing the dynamic performance of the proposed control strategy: (a) Ra = Rb = Rc = 12 Ω, changes to Ra = Rb = Rc = 24 Ω. (b) Ra = 24 Ω, Rb = Rc = 12 Ω, changes to Ra = Rb = Rc =12 Ω.

TABLE II
PARAMETERS OF THE IGBT FOR CALCULATION OF CONDUCTION LOSSES

Parameters	Value
V_T IGBT threshold voltage	0.42 V
R_T IGBT on-state resistance	15.3 mΩ
V_D Diode threshold voltage	1.45 V
R_D Diode on-state resistance	8.53 mΩ

and diode, respectively. T is the period of fundamental frequency.

To calculate the switching losses, Matlab curve fitting tool is adopted to obtain the Energy curves provided in the datasheet. E_{on} and F_{off} are the energies dissipation during the turn-on and turn-off process of the transistor. E_{rec} is the energy dissipation during the turn-off process of the diode. The energy dissipation in the diode during the turn-on process is very small and is neglected. The estimated curves are shown in TABLE III.

Thus, the switching losses can be calculated as:

$$P_{T\_switching} = \frac{1}{T}\sum_{j=1}^{n}\left[E_{on}\left(i_F, v\right) + E_{off}\left(i_F, v\right)\right] \tag{21}$$

$$P_{D\_switching} = \frac{1}{T}\sum_{j=1}^{n}\left[E_{rec}\left(i_F, v\right)\right] \tag{22}$$

After calculation, the total losses of the converter are shown in TABLE IV. It can be seen that the proposed algorithm will increase the switching losses, but not too much. Meanwhile, the conduction loss has decreased.

VI. ANALYSIS OF NEUTRAL-POINT VOLTAGE FLUCTUATION

It can be seen from the simulation and experimental results that there are some uncontrollable regions of NP voltage when the inverter connects to an unbalanced load. Actually, the proposed strategy suppresses the offset of NP voltage by controlling the NP current to zero. NP current i_o is given in (4) when none of the three phases are disassembled. When phase *a, b* and c are selected separately to fully disassemble its *O* level, the NP current can be obtained in (23).

TABLE III
ENERGY DISSIPATION CURVES

Energy	Expression
E_{on} (mJ)	$\frac{V_{CE}}{300}\left(0.0075I_C + 0.1625\right)$
E_{off} (mJ)	$\frac{V_{CE}}{300}\left(0.0275I_C + 0.3375\right)$
E_{rec} (mJ)	$\frac{V_{CE}}{300}\left(\begin{array}{l}5.686\times10^{-7}{I_C}^3 - 0.0001681{I_C}^2 + \\ 0.02486I_C + 0.5779\end{array}\right)$

TABLE IV
SIMULATION OF POWER LOSSES UNDER DIFFERENT CONDITIONS

Test Condition	Proposed Method (Conduction/Switching)	Without NP Control (Conduction/Switching)
Balanced load, Symmetrical voltage	15.2025/0.6258 W	18.2217/0.1128 W
Unbalanced load, Symmetrical voltage	16.6818/0.6045 W	18.4419/0.1128 W
Unbalanced load, Asymmetrical voltage	15.1383/0.6249 W	17.8656/0.1131 W

In a three-phase four-wire three-level NPC system, the offset of NP voltage can be fully compensated only when the NP current can keep to zero in a switching period. If the polarities of i_o and $i_{o(j)}$ are opposite, NP current can keep to zero by disassembling *O* level of phase *j*, that is to say, the offset of NP voltage can be fully compensated.

$$\begin{aligned} i_{o(a)} &= -i_a - i_b \cdot \left|v_b\right| - i_c \cdot \left|v_c\right| \\ i_{o(b)} &= -i_b - i_a \cdot \left|v_a\right| - i_c \cdot \left|v_c\right| \\ i_{o(c)} &= -i_c - i_a \cdot \left|v_a\right| - i_b \cdot \left|v_b\right| \end{aligned} \tag{23}$$

Consequently, in order to fully compensated the NP voltage, it is required that there exists at least one phase, which satisfies:

$$i_{o(j)} \cdot i_o < 0 \tag{24}$$

Fig. 16 shows the NP current $i_{o(j)}$, i_o and the NP voltage differential under the three operation conditions. It can be seen from the Fig. 16(a) that (20) is satisfied when the inverter is under the condition of balanced load and symmetrical three-phase reference voltages. Thus, it does not have the uncontrollable region. While in Fig. 16(b) and Fig. 16(c), Fig. (20) is not established in the shadow region, where the NP current cannot be

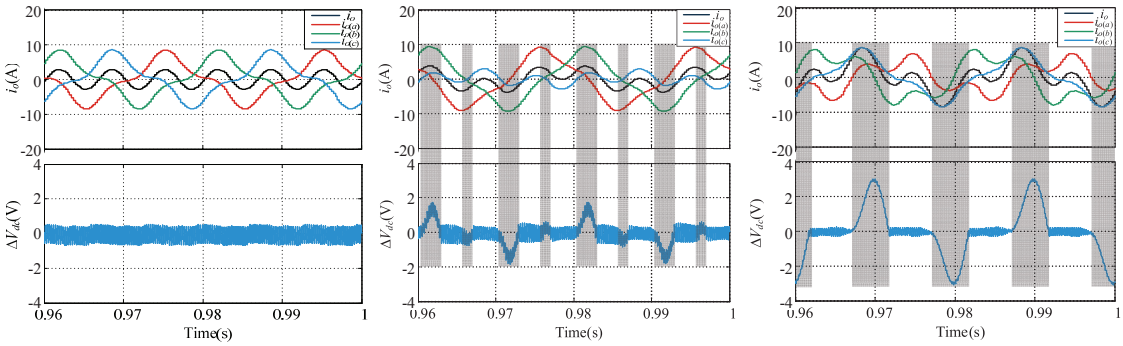


Fig. 16. Analysis of NP current and voltage fluctuation. (a) is under the balanced load and symmetrical three-phase reference voltages. (b) is under the unbalanced load and symmetrical three-phase reference voltages. (c) is under the unbalanced load and asymmetrical three-phase reference voltages.

controlled to zero. The uncontrollable region is larger when the inverter is under the unbalanced load and asymmetrical three-phase reference voltages.

VII. Conclusion

A novel neutral-point voltage control strategy for a three-phase four-wire three-level NPC inverter is proposed in this paper. Proper phase is selected to disassemble the zero level and suppress the offset of NP voltage. Compared with the 3-D SVM, it can disassemble the zero level quantitatively and compensate the drift of NP voltage accurately. The offset of NP voltage cannot be fully compensated. However, it improves the stability of NP voltage without increasing too much switching frequency. The validity of this strategy is verified by simulation and experiments.

References

[1] O. Vodyakho, T. Kim, and S. Kwak, "Three-level inverter based active power filter for the three-phase, four-wire system," in *Power Electronics Specialists Conference*, 2008, pp. 1874-1880.

[2] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 2, pp. 2768-2775, Apr. 2008.

[3] R. A. Modesto, D. S. S. A. Oliveira, and A. A. De Oliveira, "Line-interactive UPS system applied to three-phase four-wire systems with universal filtering capabilities," in *IEEE International Symposium on Industrial Electronics,* 2014, pp. 1858-1865.

[4] B. R. Lin, C. H. Huang, T. Y. Yang, and Y. C. Lee, "Analysis and implementation of shunt active power filter with three-level PWM scheme," in *International Conference on Power Electronics and Drive Systems*, 2003, vol. 2, pp. 1580-1585.

[5] J. H. Kim and S. K. Sul, "A carrier-based PWM method for three-phase four-leg voltage source converters," *IEEE Transactions on Power Electronics*, vol. 19, No. 1, pp. 66-75, Jan. 2004.

[6] R. Zhang, V. H. Prasad, D. Boroyevich, and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Transactions on Power Electronics,* vol. 17, no.3, pp. 314-326, May 2002.

[7] N. Y. Dai, C. S. Lam, M. C. Wong, and Y. D. Han, "Application of 3D direct PWM in parallel power quality compensators in three-phase four-wire systems," in *IEEE Power Electronics Specialists Conference,* 2008, pp. 3220-3225.

[8] M. C. Wong, N. Y. Dai, and Y. D. Han, "Study of tri-level neutral point clamped inverter for 3-phase 3-wire and 3-phase 4-wire applications," in *International Conference on Power Electronics and Drive Systems,* 2003, vol. 1, pp. 380-385.

[9] J. Wang, Y. Gao, and W. Jiang, "A carrier-based implementation of virtual space vector modulation for neutral point clamped three-level inverter," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 12, pp. 9580-9586, Dec. 2017.

[10] A. Choudhury, P. Pillay, and S. S. Williamson, "DC-bus voltage balancing algorithm for three-level neutral-point-clamped (NPC) traction inverter drive with modified virtual space vector," *IEEE Transactions on Industry Applications,* vol. 52, no. 5, pp. 3958-3967, Sept.-Oct. 2016.

[11] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2262-2271, 2010.

[12] J. Pou, J. Zaragoza, S. Ceballos, and M. Saeedifard, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Transactions on Power Electronics,* vol. 27, no. 7, pp. 642-651, July 2012.

[13] H. C. Chen, M. J. Tsai, Y. B. Wang, and P. T. Cheng, "A novel neutral point potential control for the three-level neutral-point-clamped converter," in *Energy Conversion Congress and Exposition*, 2017, pp. 1-7.

[14] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos, and D. Boroyevich, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 4, pp. 2288-2294, Aug. 2007.

[15] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 2, pp. 305-314, Feb. 2009.

[16] J. Hu, Z. Sun, A. Farooq, and G. Chen, "A three-phase four-wire three-level active power filter based on one-cycle control," in *Industrial Electronics Society, IECON 2014 - Conference of the IEEE,* 2014, pp. 1143-1147.

[17] B. Kedjar and K. Al-Haddad, "LQ control of a three-phase four-wire shunt active power filter based on three-level NPC inverter," in *Electrical and Computer Engineering, 2008. CCECE 2008. Canadian Conference,* 2008, pp. 001297-001302.

[18] N. Y. Dai, M. C. Wong, Y. D. Han, and C. S. Lam, "A 3-D generalized direct PWM for 3-phase 4-wire APFs," in *Industry Applications Conference, 2005. Fourtieth Ias Meeting,* 2005, pp. 1261-1266, vol. 2.

[19] X. J. Wang, Z. Xiao, and W. U. Yuan, "A simplified modulation strategy for three-phase four-wire tri-level converter," *Power Electronics,* vol. 4, pp. 002, 2017.

[20] J. Tang, X. Zou, Y. Xu, and X. She, "Novel 3-DSVM scheme for three-phase four-wire tri-level APFs," in *IEEE 6th International Power Electronics and Motion Control Conference*, 2009, pp. 882-886.

[21] F. Li, F. He, and Z. Ye *et al.*, "A simplified PWM strategy for three-level converters on three-phase four-wire active power filter," *IEEE Transactions on Power Electronics,* vol. 33, no. 5, pp. 4396-4406, May 2018.

[22] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Industry Applications Society Meeting*, 1993, pp. 965-970.
[23] D. Holmes and T. Lipo, in *Pulse Width Modulation for Power Converters: Principles and Practice.* New Jersey: Wiley & Sons, 2003, pp. 71-77.
[24] J. Pou, J. Zaragoza, and S. Ceballos *et al.*, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Transactions on Power Electronics,* vol. 27, no. 2, pp. 642-651, Feb. 2012.

Chenchen Wang was born in Anhui Province, China, in 1981. He received the B.S. and Ph.D. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 2003 and 2008, respectively. He is an Associate Professor at the School of Electrical Engineering, Beijing Jiaotong University, Beijing, China. His current research interests include motor control and multilevel converters.

Zhitong Li was born in Liaoning Province, China, in 1993. He received the B.S. degrees in Electrical Engineering from Northeast Agricultural University, Heilongjiang, China. Now he is currently working towards M.S. degree in Electrical Engineering in Beijing Jiaotong University, Beijing, China. His current research interests include multilevel converters.

Xiahe Si was born in Gansu Province, China, in 1991. He received the B.S. and M.S. degrees in Electrical Engineering in Beijing Jiaotong University, Beijing, China. His current research interests include multilevel converters.

Hongliang Xin was born in Fujian Province, China, in 1991. He received the B.S. and M.S. degrees in Electrical Engineering in Beijing Jiaotong University, Beijing, China. His current research interests include multilevel converters.

Three Phase Trans-Quasi-Z-Source Inverter

Xupeng Fang, Bolong Ma, Guanzhong Gao, and Lixin Gao

***Abstract*—In this paper, a new type of single-stage boost Trans-quasi-Z-source inverter topology is presented. The basic structure and working principle of the inverter are analyzed and its voltage gain is deduced. The model of the Trans-quasi-Z-source network is established by using Laplace transform. The dynamic characteristics of the system are analyzed, and the switching loss is explored by comparing the different shoot-through injection methods. In order to verify the dynamic boost characteristics, the Matlab/Simulink simulation is performed. Finally, the hardware circuit is built on the basis of theoretical analysis and simulation verification. The experimental results verify the feasibility and stability of the circuit.**

***Index Terms*—Dynamic boost characteristics, single-stage boost, switching loss, trans-quasi-Z-source inverter.**

I. Introduction

As the fossil fuel is not renewable and the pollution it causes to the environment, new energy technologies, such as fuel cell, solar energy and wind energy, have attracted more and more attention and application. However, most of the output of the new energy generation is unstable DC or AC power; it has to be converted to a usable DC or AC power. The traditional inverter can better meet the requirement of users only when the DC bus voltage is large enough, otherwise, a DC-DC converter must be added to achieve the boosting purpose.

The Z-source inverter topology was presented by Professor Fangzheng Peng in 2002 [1], once it has been put forward, it has aroused widespread concern in the power electronics area and became a hotspot in the field, and it has been studied on the solar photovoltaic generation, fuel cell generation, motor drive and so on [2]-[4]. However, there are some defects in the circuit, such as discontinuous input current, excessive voltage stress of capacitor, too large surge current when the circuit starts [5]-[7]. In 2008, Professor Fangzheng Peng proposed an improved circuit topology on this basis--the Quasi-Z-source inverter; it can overcome the problem that the capacitor voltage or the inductor current is too large in the impedance source network of the Z-source inverter, and also attracted wide concern in the power electronics field [8]-[10]. However, there is a common defect in the Z-source and quasi-Z-source inverter: the actual attainable boost gain is small. When the input voltage is low and the required voltage gain is large, the inverter needs to work in a larger shoot-through duty cycle, so the modulation index must be reduced correspondingly, resulting in poor output voltage quality[11]-[13].

To solve the above problems, many domestic and foreign scholars have proposed many modified Z-source inverter circuit topology, such as switched-inductor Z-source inverter, Y-source inverter, Delta-source inverter, Trans-Z-source inverter and so on[14]-[18]. However, these inverters also has some defects, for example, some circuit topologies have good boost capacity, but the capacitor suffers large voltage stress; some circuit topology's capacitor has small voltage stress, but the boost ability has been limited; some circuit topology's capacitor has small voltage stress and has good boost capacity, but has a complex structure, large volume and high cost, etc.

This manuscript presents a Trans-quasi-Z-source inverter circuit topology, it is a new type of inverter circuit, based on the traditional quasi-Z-source inverter, it changes an inductor of the quasi-Z-source network into a coupling form, and leads a capacitor in the middle, by changing the turn ratio of the coupled inductors to adjust the boost ratio, and it can make up the defects of the traditional quasi-Z-source inverter that the duty ratio and modulation index restrict each other, and has good boost capacity, and eliminate the influence of the dead time to the output voltage ripple. The following is the structure of the manuscript: the second part is the analysis of the operating principle of the circuit, the third part analyzes the boost characteristics of the circuit, the fourth part is control strategy analysis, the fifth part gives the switching times and switching loss analysis, in the end the simulation and experimental verification are given.

II. Circuit Principle Analysis

The proposed Trans-quasi-Z-source inverter is improved based on the traditional Trans-Z-source inverter, and only an inductor and a diode are added, which is shown in Fig. 1. Same as other Z-source inverter topologies, the shoot-through zero states are inserted in the two traditional zero-states of the inverter, thus it does not affect the normal operation of the inverter, but the inverter has the better buck-boost function. Assuming that all the devices are ideal, the conduction voltage drop of the diode and IGBT is zero. When the inverter operates in the shoot-through zero-states, the diode on the input side is subjected to reverse voltage and turned off. When the inverter operates in the non-shoot-through states, the diode is turned on, and the reference directions of the voltages and currents in the circuit are shown in Fig. 1.

It is assumed that the duration of a switching period is T, the shoot-through time is T_0 (corresponding time t_0 to t_1), the non-shoot-through time is T_s (corresponding time t_1 to t_2), and the

Manuscript received January 2, 2018. This work was supported in part by the Shandong Province National Science Foundation under Grant ZR2016EEP10 and in part by the Graduate Education High-Quality Course Construction Project of Shandong Province under Grant SDYKC17032.

The authors are with the College of Electrical Engineering and Automation, Shandong University of Science and Technology, Qingdao 266590, China (e-mail: xpfang@sdust.edu.cn; 1570630609@qq.com; 994848330@qq.com; 371440520@qq.com).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00022

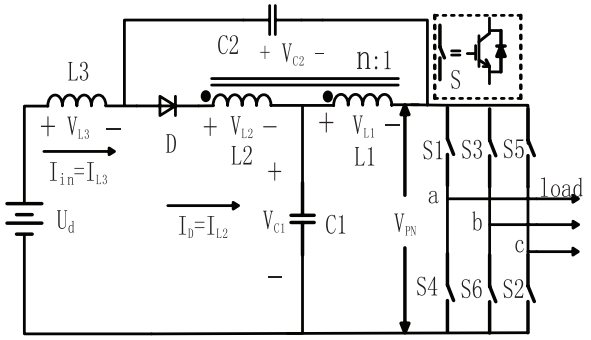


Fig. 1. The Trans-QZ-source inverter topology.

shoot-through duty ratio is D, we have

$$T_0 = DT \tag{1}$$

$$T_s = (1-D)T \tag{2}$$

The equivalent circuit of the Trans-quasi-Z-source inverter working in the shoot-through mode is shown in Fig. 2(a), the inverter bridge is short-circuit, the diode is turned off, the power supply and capacitor C_2 charge the inductor L_3, and the capacitor C_1 recharges the inductor L_1, the magnetization current of the inductor increases gradually. Because the inductors L_1 and L_2 are coupled tightly, the excitation current is reflected to the secondary windings of the coupled inductor, the voltage of the L_2 is gradually increased from a small value to $V_{L2}=nV_{L1}$, the inductor L_2 is charged. At this point, the potential of the left of the inductor L_2 is high, and the diode withstands the reverse voltage.

$$V_{L1} = V_{C1} \tag{3}$$

$$V_{L2} = nV_{L1} = nV_{C1} \tag{4}$$

$$V_{L3} = U_d + V_{C2} \tag{5}$$

The equivalent circuit of the inverter working in the non-shoot-through mode is shown in Fig. 2(b), the diode is turned on and the inverter bridge can be equivalent to a controlled current source. The coupling inductors L_1, L_2 and the input inductor L_3 power the load together, while charge the capacitor, and the voltage of the inverter bridge is improved [19]. Now, we have,

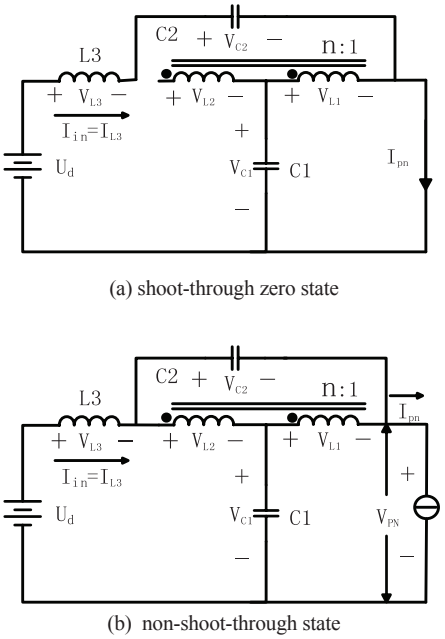
$$-V_{C2} = V_{L1} + V_{L2} \tag{6}$$

$$V_{L3} = \mathrm{U}_d - V_{L2} - V_{C1} \tag{7}$$

$$V_{PN} = V_{C1} - V_{L1} \tag{8}$$

From the above analysis, we know that the Trans-quasi-Z-source inverter is to control the on-off of the diode by controlling the shoot-through and non-shoot-through state of the inverter bridge, and to transfer the energy stored in the coupling inductor and the input inductor to achieve the boosting purpose.

For the inductors L_1, L_2, L_3, the average voltage on them in a switching period is zero, we can have,



(a) shoot-through zero state

(b) non-shoot-through state

Fig. 2. The operating principle of the Trans-QZ-source inverter.

$$\frac{1}{T}\left[\int_{t_0}^{t_1} V_L d_t + \int_{t_1}^{t_2} V_L d_t\right] = 0 \tag{9}$$

From the above analysis, and based on the "Volt-Second" balance relation, we can have,

$$DV_{C1} - (1-D)(V_{C2} + V_{L2}) = 0 \tag{10}$$

$$nDV_{C1} - (1-D)(V_{C2} + V_{L1}) = 0 \tag{11}$$

$$D(V_{dc} + V_{C2}) + (1-D)(U_d - V_{L2} - V_{C1}) = 0 \tag{12}$$

$$V_{L2} = nV_{L1} \tag{13}$$

From the formulas (10) and (11) , we can have,

$$V_{C2} = \frac{(1+n)D}{1-D} V_{C1} \tag{14}$$

$$V_{C2} = \frac{(1+n)D}{1-(2+n)D} U_d \tag{15}$$

$$V_{C1} = \frac{1-D}{1-(2+n)D} U_d \tag{16}$$

The DC-link peak voltage of the inverter can be obtained through (10), (11), (14) and (15).

$$V_{PN} = \frac{1}{1-(2+\mathrm{n})D} U_d = BU_d \tag{17}$$

The boost ratio B can be expressed as:

$$B = \frac{1}{1-(2+\mathrm{n})D} \tag{18}$$

The voltage gain G can be expressed as:

$$G = MB = \frac{M}{1-(2+\mathrm{n})D} \tag{19}$$

Wherein M is the modulation index of the inverter.

From the above analysis, we can see that the voltage gain of the Trans-quasi-Z-source inverter is not only related to the shoot-through duty cycle D, but also to the turn ratio n of the coupling inductors and the modulation index M of the inverter. When the n is fixed, the DC bus voltage increases with the increase of D; When the D is fixed, the DC bus voltage will increases with the increase of the turn ratio n; When the modulation index M and the duty cycle D of the inverter are mutually restricted, and the ideal DC bus voltage cannot be achieved, the voltage can be compensated by changing the turn ratio n, so as to achieve the required DC bus voltage. Usually, we can try to reduce the duty ratio D by increasing the turn ratio n, so as to increase the modulation index M of the inverter, improve the conversion efficiency, and suppress the harmonic effect brought by the boost network.

III. Analysis of Circutt Boost Characteristics

The boost ratio of the traditional Z-source inverter is related to the shoot-through duty ratio D and the modulation index M. The boost ratio B is influenced by the circuit structure, and the boost capacity is limited. The Trans-Z-source inverter adopts the coupling inductor form [19]-[21]; its boost ability is not only related to the shoot-through duty ratio D, but also related to the turn ratio n, obviously, it improves the boost capacity of the circuit.

The Trans-quasi-Z-source inverter is improved on the basis of the traditional Z-source inverter and the Trans-Z-source inverter, so that it has a higher boost capacity. The relationship among the boost ratio B, the duty ratio D and the turn ratio n of the Trans-quasi-Z-source inverter are shown in Fig. 3, the boost effect is not very obvious at n = 1, which is almost the same as that of the traditional Z-source or quasi-Z-source inverter, however, when the n is increased to 3, the boost capacity of the Trans-quasi-Z-source inverter will be greatly improved. When the D is close to 0.2, the boost gain is close to infinity, which overcomes the defect that the traditional quasi-Z-source inverter must increase the duty ratio D by reducing the modulation index M to improve the output voltage [22]-[24].

The boost ratio correlation curves of the Trans-quasi-Z-source inverter, Z-source inverter and Trans-Z-source inverter, are shown in Fig. 4 and Fig. 5, When n = 1, the boost ratio of the Trans-Z-source inverter is the same as that of the traditional Z-source inverter. The two curves coincide fully, and the two inverters have limited boost capacity. Only when the shoot-through duty ratio D is close to 0.5, can a larger boost ratio be

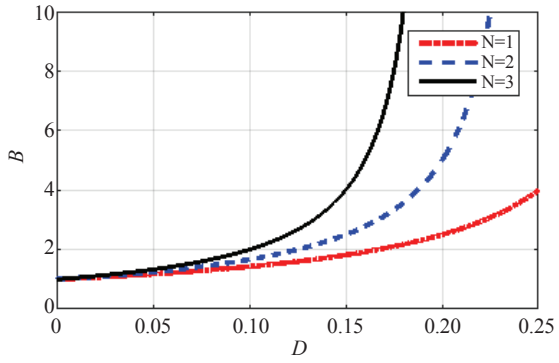


Fig. 3. The relationship between the voltage gain and the shoot-through duty cycle of the Trans-QZSI.

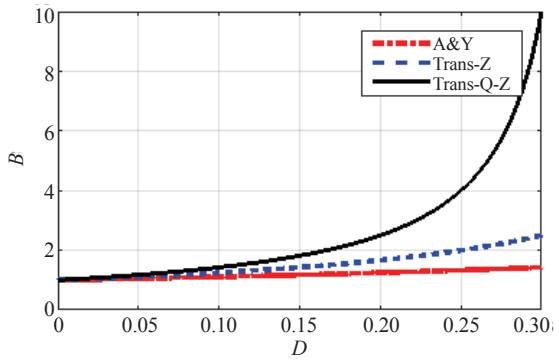


Fig. 4. The correlation curves of the boost ratio when n = 1.

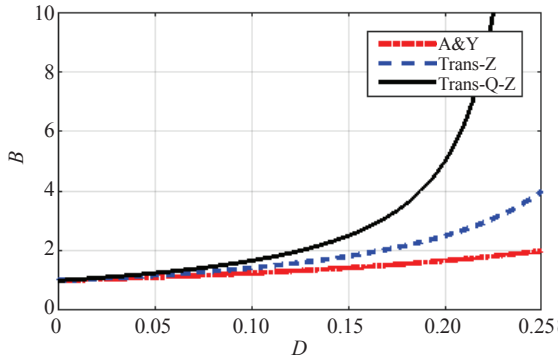


Fig.5. The correlation curves of the boost ratio when n = 2.

achieved. The boost ratio of the Trans-quasi-Z-source inverter has reached 4 when D = 0.25, compared with the other two kinds of inverters, the boost capacity of the Trans-quasi-Z-source inverter is greatly enhanced. When n = 2 and in the same duty ratio D, the Trans-quasi-Z-source inverter has the best boost ability, the Trans-Z-source inverter is the next, and the traditional Z-source inverter is the least, the gap in the boost capacity of the three inverters is becoming more and more obvious with the increase of the shoot-through duty ratio D.

IV. Analysis of Circuit Control Strategy

If we adopt the simple boost control method, from the oper-

ating principle analysis, we can see that the shoot-through zero vector can only be inserted to the traditional zero vector, while the traditional zero vector in sinusoidal pulse width modulation (SPWM) shows the effect of the difference between the modulation wave and the carrier peak in time [25]-[27]. Two equal and opposite polarity voltages V_n and V_p are taken, the value of the two voltages are between the modulation wave and the carrier. The comparison results of the voltage V_n or V_p and the carrier is the switching time of the shoot-through vector. The value of V_n and V_p determines the size of the duty ratio D, by adding V_n and V_p into each group of modulated waves, the shoot-through states are injected. When V_n or V_p acts individually, the duty ratio is D_0, and the duty ratio is $2D_0$ when V_n and V_p act simultaneously. The principle of the simple boost control is shown in Fig. 6.

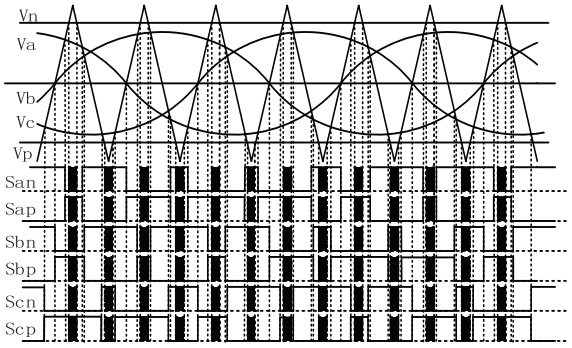


Fig. 6. The simple boost control method.

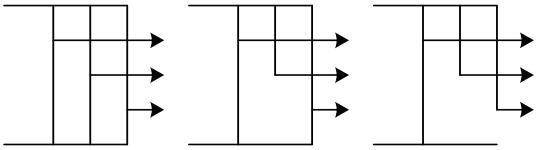


Fig.7. The three different shoot-through methods.

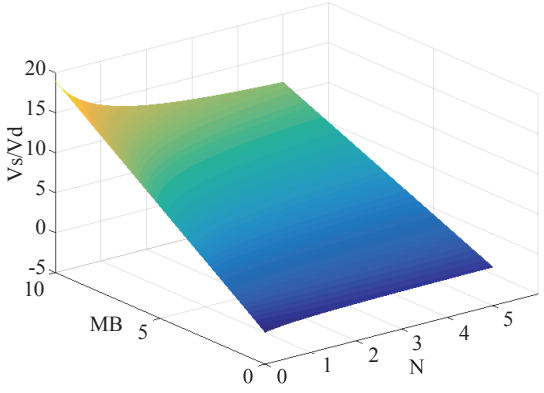


Fig. 8. The relationship of V_s versus n and MB.

V. Analysis of Switching Times and Switching Loss

From the principle diagram shown in Fig. 6, it can be seen that the order of the switch of the SPWM signal is fixed, that is to say, it is impossible to reduce the switching times by changing the order of the switch. But the injection of the shoot-through signal will certainly increase the switching times in a switching period. There exists a problem in the process of the injection of the shoot-through signal; the shoot-through states may be implemented by one bridge arm, or by two bridge arms, and even by three bridge arms [28], [29]. Although these three shoot-through modes achieve the same results, single arm shoot-through mode only increases one time of switching, and the two arms shoot-through mode increases two times of switching. Similarly, the three arms simultaneous shoot-through mode has the largest number of switching times and the corresponding shoot-through state is shown in Fig. 7. The three arms shoot-through mode is chosen in the following simulation and experiments of the manuscript.

The switch voltage stress of the three-phase Trans-quasi-Z-source inverter is equal to the input voltage of the inverter bridge, that is, the DC-link voltage,

$$V_s = V_{PN} = BU_d \tag{20}$$

Suppose that under the maximum boost condition $D = 1-M$, from the formulas (18), (19) and (20), we can have

$$V_s = \frac{(2+n)G-1}{(1+n)} U_d \tag{21}$$

The relationship between the voltage stress of the switch and the voltage gain is plotted by the Matlab/Figure software, as shown in Fig. 8. It indicates that the voltage stress of the power switches is related to the voltage gain MB and the turn ratio n, and with the increase of MB and n, the voltage stress of the power switches will increase either. Thus, don't to increase the voltage gain and the turn ratio blindly, it is essential to consider the voltage withstanding ability of the power switches.

According to the working principle of the Z-source inverter, the larger the shoot-through duty ratio D, the larger the voltage gain, and the higher the voltage stress of the power switch. Therefore, the duty ratio D should be reduced under the condition that the modulation index M is as large as possible, in order to reduce the voltage stress of the power switches. In addition, the switch voltage stress can be reduced by the modulation method, such as the SVPWM control strategy, the maximum boost SPWM control strategy and so on.

The current stress of the switch is different from the voltage stress of the switch, because the inductor current and the load current are all circulated through the shoot-through bridge arm, the parallel connection of the bridge arms has the function of shunt and no partial voltage. So the effect of the different three types of the shoot-through modes on the current stress of the power switch is very great. The same as the traditional Z-source inverter, when the load power angle is $\theta \leq 30°$, the current stress of the switch in the shoot-through vector is two times the peak of the inductor current [4].

$$I_{max} = 2I_L \tag{22}$$

Suppose the phase current of the three-phase inverter is

$$\begin{cases} i_a = I_{out}\sin(\omega t-\theta) \\ i_b = I_{out}\sin(\omega t-2\pi/3-\theta) \\ i_c = I_{out}\sin(\omega t+2\pi/3-\theta) \end{cases} \quad (23)$$

When θ>30°, the current stress of the switch in the shoot-through state is the largest.

$$I_{\max} = 2I_L + I_{out}\sin(\theta-30°) \quad (24)$$

The maximum current stress of the switch in the shoot-through state is I_{max}, for the single bridge arm shoot through mode, the maximum current stress is $I_{max1} = I_{max}$; for the two bridge arms shoot-through mode, the maximum current stress is $I_{max2} = I_{max}/2$; for the three bridge arms shoot-through mode, the maximum current stress is $I_{max3} = I_{max}/3$. For the two bridge arms simultaneously conduct mode, the current stress of each bridge arm is reduced to 1/2 of the original value. And for the three bridge arms simultaneously conduct mode, the current stress of each bridge arm is reduced to 1/3 of the original value. It is assumed that the internal resistance of the switch is R, the average conduction current of each bridge arm is I_{avmax} and the conduction loss is P_0.

When the three bridge arms simultaneously shoot-through:

$$I_{av\max} = I_{\max}/3 \quad (25)$$

$$P_0 = (I_{av\max})^2 R = (I_{\max}/3)^2 R*3 = \frac{1}{3}I^2{}_{\max}R \quad (26)$$

When the two bridge arms simultaneously shoot-through:

$$I_{av\max} = I_{\max}/2 \quad (27)$$

$$P_0 = (I_{av\max})^2 R = (I_{\max}/2)^2 R*2 = \frac{1}{2}I^2{}_{\max}R \quad (28)$$

When the single bridge arm shoot-through:

$$I_{av\max} = I_{\max} \quad (29)$$

$$P_0 = (I_{av\max})^2 R = I^2{}_{\max}R \quad (30)$$

From the above analysis, we can see that the three bridge arms shoot-through mode can decrease the average conduction current, reduce the switch current stress, and therefore can reduce the conduction loss.

VI. The Circuit Simulation Verification and Analysis

The turn ratio of the Trans-quasi-Z-source inverter only affects the boost ratio of the system and has no effect on the stability and response speed of the system. Also in the case of $n = 1$, to analyze the influence of the system response when the inductors and capacitors change in the Trans-quasi-Z-source network. The load is assumed to be a purely resistive load when analyzing the network stability of the Trans-quasi-Z-source inverter, and the inverter bridge is replaced with a switch S. The equivalent small signal model structure of the Trans-quasi-Z-source inverter topology is shown in Fig. 9. Under the condition of $n = 1$, the voltage regulation process is accurately analyzed by comparing different inductance and capacitance within the allowable variation range, and the network element parameters that are most suitable for the Trans-quasi-Z-source inverter are selected according to actual conditions.

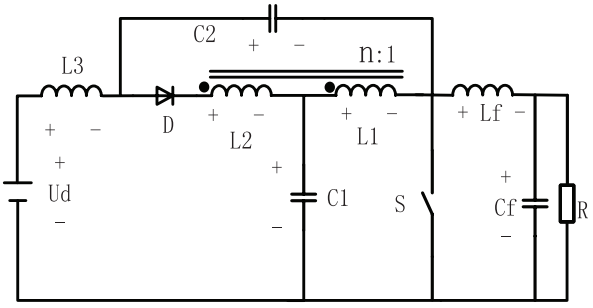


Fig. 9. The circuit model of the Trans-quasi-Z-source inverter.

In order to establish the circuit model of the Trans-quasi-Z-source inverter, adds a disturbance signal on the input voltage U_d and d_0. Let $X = x+\hat{x}$, x and $\hat{x}$ are variable after adding perturbation to the DC side and d_0, I_{load}, I_{L1}, I_{L3}, V_{C1}, V_{C2}. The transfer function of the multi-input multi-output Trans-quasi-Z-source network is deduced by Laplace transform. The transfer function is the same from d_0 to the capacitor voltage V_{C1} and V_{C2}, and it can be expressed as:

$$G_{\hat{d}_0}^{\hat{v}_c}(s) = \frac{\hat{v}_c(s)}{\hat{d}_0(s)}\Big|_{\substack{\hat{i}_{load}(s)=0 \\ \hat{V}_{in}(s)=0}} = \frac{(V_{C1}+V_{C2}-RI_{load})(1-3D_0)+(I_{load}-I_{L1}-I_{L2})(LS+R+r)}{LCS^2+C(r+R)S+(1-3D_0)^2} \quad (31)$$

The second-order transfer function for the capacitor voltage versus the input voltage can be expressed as:

$$G_{\hat{V}_{dc}}^{\hat{v}_{cs}}(s) = \frac{\hat{v}_{cs}(s)}{V_{dc}(s)}\Big|_{\substack{\hat{i}_{load}(s)=0 \\ \hat{d}_0(s)=0}} = \frac{1-3D_0}{LCS^2+C(r+R)S+(1-3D_0)^2} \quad (32)$$

The effect of the inductance and capacitance variation on the system is shown in Fig. 10 to Fig. 11. As can be seen from Fig. 10, as the inductance increases, the maximum overshoot of the system will be gradually reduced, the system oscillation amplitude and the voltage fluctuation is relatively small and the voltage adjustment process is relatively flat. It is suitable for stable voltage output. However, as the inductance increases, the rise time of the system will become longer at the same time, the voltage tends to be steady for a longer time and the system voltage response is relatively slow. Thus, the large inductance can make the system respond process becomes smooth, but will pay the cost of extending the system response time, so the reasonable choice of the inductance parameters will make the system response to the best. It can be seen from Fig. 11 that the performance index of the rise time, maximum overshoot, and

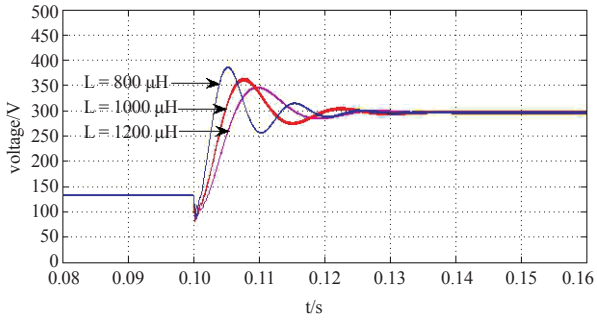


Fig. 10. The response process of the system when L changed.

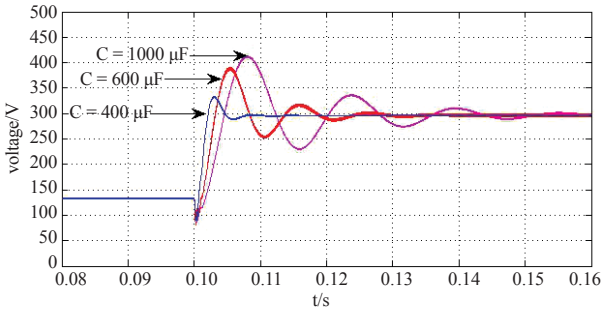


Fig. 11. The response process of the system when C changed.

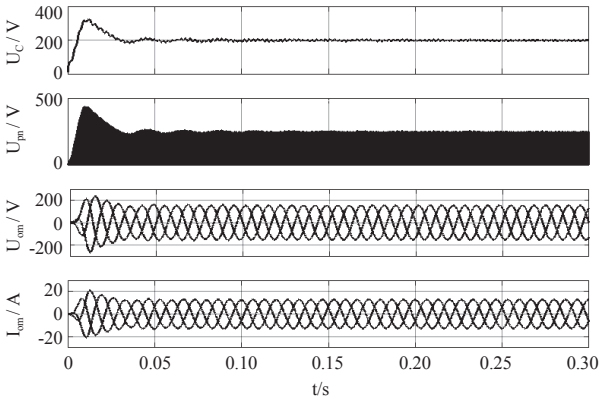


Fig. 12. The output voltage waveforms when $n = 1$, $D = 0.2$.

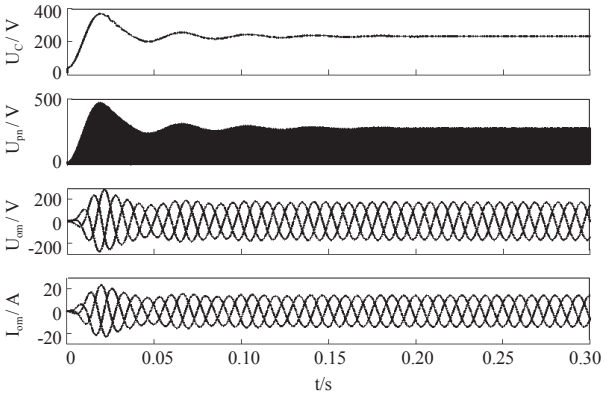


Fig. 13. The output voltage waveforms when $n = 2$, $D = 0.15$.

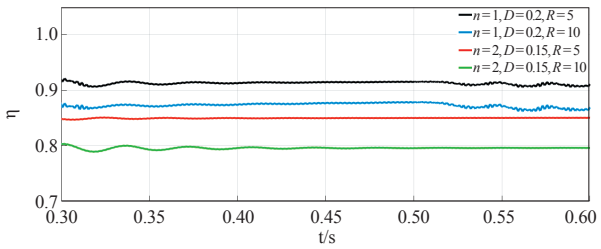


Fig.14. The efficiency curves in different n, D and R.

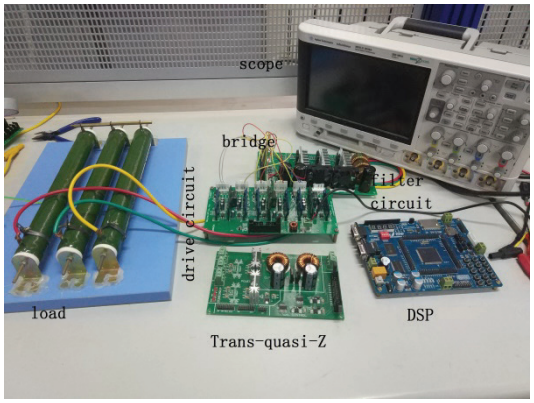


Fig. 15. The prototype of the experiment circuit.

oscillation amplitude is good and the system responds quickly when the capacitance parameter is relatively small. Therefore, the capacitance of the capacitor should be selected smaller within the allowable range.

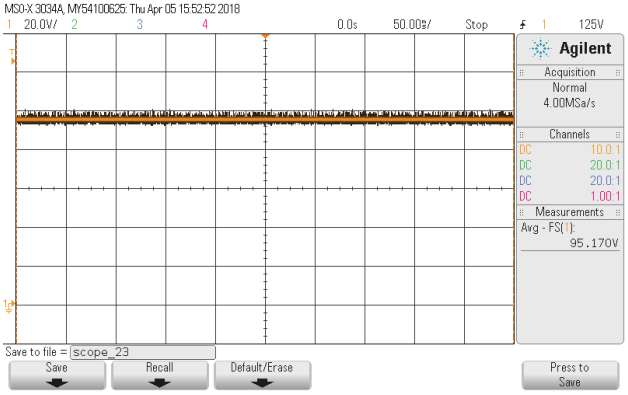
According to Fig. 10 and Fig. 11, the capacitance of the C_1 and C_2 is 470 μF, the inductance of the L_1 and L_3 is 800 μH and the switching frequency f_s is 20 kHz.The simulated output voltage waveforms of the Trans-quasi-Z-source inverter are shown in Fig. 12 and Fig. 13 when the input DC voltage U_d is 100 V, the modulation index $M = 0.7$.

When $n = 1$, $D = 0.2$, the three-phase voltage waveforms are shown in Fig. 12, the measured values of capacitor voltage, DC link voltage, AC output line voltage and line current are close to their theoretical values of 200 V, 250 V, 151.56 V and 12.5 A.

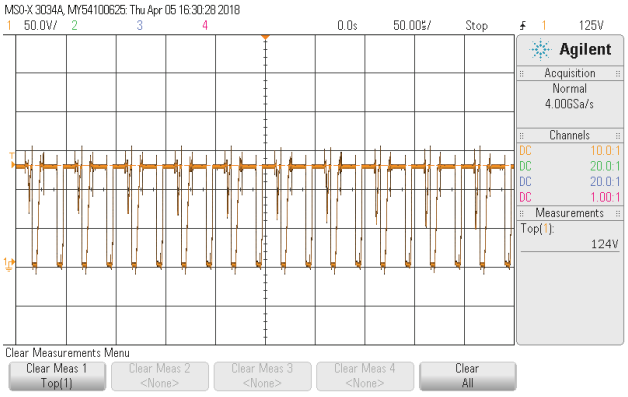
When $n = 2$ and $D = 0.15$, the three-phase voltage waveforms are shown in Fig. 13. The measured values of capacitor voltage, DC link voltage, AC output line voltage and line current are close to their theoretical values of 212.5 V, 250 V, 151.56 V and 12.5 A.

The efficiency curves of the proposed inverter under different turn ratio, different shoot-through duty cycle and different load are shown in Fig. 14, it is shown clear that under the condition of same turn ratio and shoot-through duty cycle, the heavier the load, the higher the efficiency, and when $n = 1$, $D = 0.2$, $R = 50\ \Omega$, the efficiency of the inverter will be higher than 92%; under the condition of the same load, the smaller the turn ratio, the higher the efficiency, this dues to that with the larger turn ratio of the couple transformer, the more power loss in the transformer, so in the actual engineering applications, it is unsuitable to blindly increase the turn ratio to pursue the boost ability.

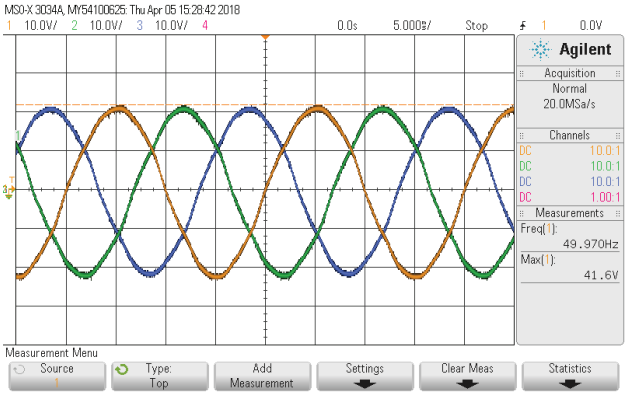
Based on the analysis of the simulation results, the simulation results are close to the theoretical values within the



(a) Capacitor C_1 voltage

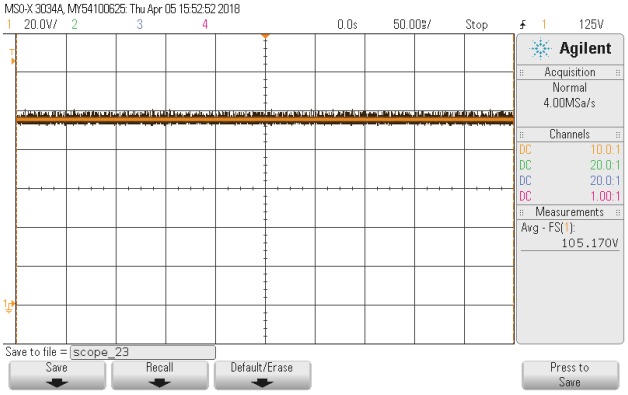


(b) DC link voltage

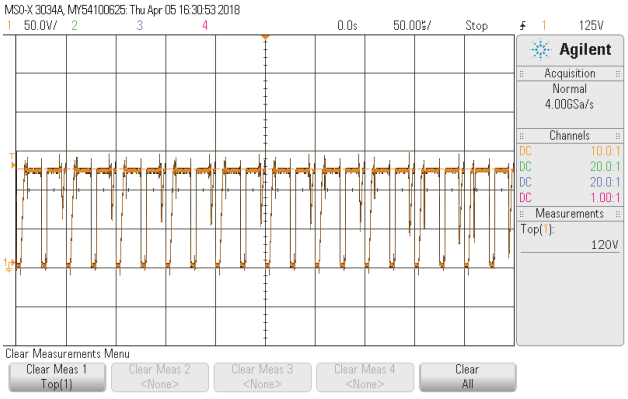


(c)Output AC voltage

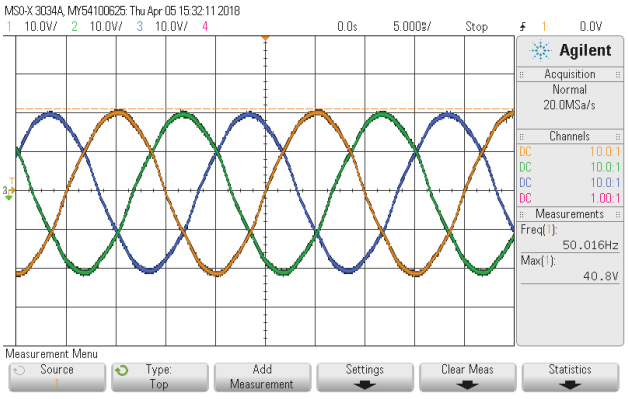
Fig.16. The output voltage waveforms when $n = 1$, $D = 0.2$.



(a) capacitor C_1 voltage



(b) DC link voltage



(c) Output AC voltage

Fig. 17. The output voltage waveforms when $n = 2$, $D = 0.15$.

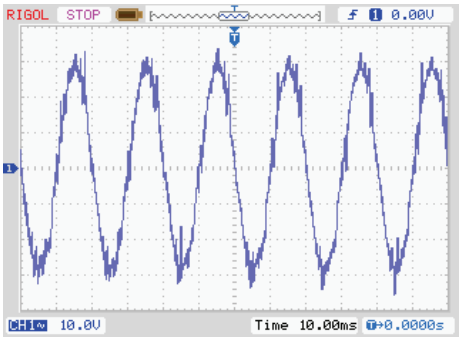
allowable range of errors, which verifies the correctness of the theoretical analysis.

VII. Experimental Verification of the Circuit

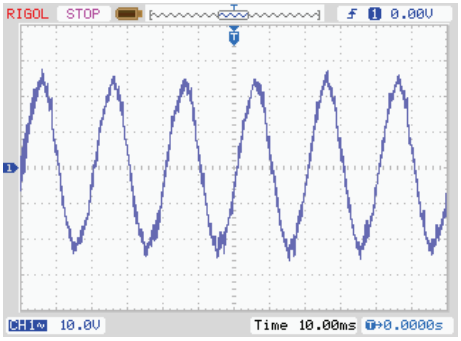
A hardware circuit is built based on the simulation, which is shown in Fig. 15, the hardware circuit verifies the boost waveform at $n = 1$ and $n = 2$. With the same parameters in the simulation circuit, $L_1 = 800$ μH and $L_3 = 800$ μH, capacitor $C_1 = 470$ μF and $C_2 = 470$ μF, DC voltage $U_d = 50$ V, the inverter modulation index M is 0.7 and the switching frequency f_s is 20 kHz, the rated power level of the prototype can achieve 3 kW, and the experiments is performed based on the smaller power level. The oscilloscope intercepts the output voltage waveforms and the experimental results are shown in Fig. 16-Fig. 17.

When $n = 1$, $D = 0.2$, the three-phase output voltage waveforms are shown in Fig. 16. The theoretical voltage value of the capacitor C_1, DC link and the output AC voltage is 100 V, 125 V and 44 V, respectively. And the actual experimental result is about 98 V, 123 V, 42 V, respectively.

When $n = 2$, $D = 0.15$, the three-phase output voltage waveforms are shown in Fig. 17. The theoretical voltage value of



(a) Delta-source inverter



(b) Trans-Z-source inverter

Fig. 18. Output voltage of phase A of Delta-source inverter and Trans-Z-source inverter.

capacitor C_1, DC link, and the output AC voltage is 106 V, 125 V, 44 V, respectively. And the actual experimental result is 104 V, 122 V, 42 V, respectively. The experimental results are very close to the theoretical value, which verifies the correctness of the theoretical analysis. Additionally, there are lots of voltage spikes on the DC-link voltage in Fig. 16(b) and Fig. 17(b); this dues to the leakage inductance and its effect on the circuit, some measures will be explored to reduce it in the future.

In the case of the same turn ratio $n = 2$ and shoot-through duty cycle $D = 0.15$, the prototypes of the Trans-Z-source inverter and the Delta-source inverter are constructed, and some experiments are performed, the experimental results of the output voltage of phase A are shown in Fig. 18. Under this condition, the output phase voltage of the two inverters is 31.8 V or 25 V. Compared with the proposed Trans-quasi-Z-source inverter, the output phase voltage of the aforementioned two inverters is lower. It can be verified that the proposed inverter has the advantage of stronger boost ability, and it has potential advantages in the applications requiring higher boost voltage gain.

VIII. Conclusions

In this paper, a new type of Trans-quasi-Z-source inverter topology is introduced, which directly couples the DC side and the inverter side through a Trans-quasi-Z-source network to form a single-stage controllable voltage regulation inverter. Compared with the traditional inverters and the quasi-Z-source inverters, it achieves the single-stage buck-boost function that is lacking in the traditional inverters as well as overcoming the defects of the modulation index and shoot-through duty cycle restrict each other in the quasi-Z-source inverters, and it has higher voltage gain than the traditional quasi-Z-source inverter. Due to the unique circuit structure of the Trans-quasi-Z-source inverter, it has broad application prospect in uninterruptible power supply, electric vehicle and photovoltaic power generation system. Research on this aspect will be carried out in the future work.

References

[1] F. Z. Peng, "Z-source inverter," in *Proceedings of Industry Applications Conference, 2002. 37th IAS Annual Meeting Conference Record of the*, 2002, pp. 775-781.

[2] F. Z. Peng, "Z-Source Inverter," *IEEE Transactions on Industry Applications.*, vol. 39, no. 2, pp. 504-510, Mar./Apr. 2003.

[3] F. Z. Peng, X. P. Fang, and B. Gu *et al*., "Z-source converter," *Transactions of China Electrotechnical Society,* vol. 19, no. 2, pp. 47-51, Feb. 2004.

[4] X. P. Fang, "Research on Z-source inverter," Ph.D. dissertation, Zhejiang University, 2005.

[5] X. P. Fang, Z. Qian, Q. Gao, B. Gu, F. Z. Peng, and X. M. Yuan, "Current mode Z-source inverter-fed ASD system," in *Proceedings of IEEE PESC'04*, Aachen, 2004, pp. 2805-2809.

[6] F. Z. Peng, X. Yuan, X. P. Fang, and Z. Qian, "Z-source inverter for adjustable speed drives," *Power Electronics Letters, IEEE*, vol. 1, no. 2, pp. 33-35, 2003.6.

[7] Y. Tang, S. Xie, C. Zhang, and Z. Xu, "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability," *IEEE Transactions on Power Electronics,* vol. 24, no. 2, pp. 409-415, Feb. 2009.

[8] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 833-838, Aug. 2005.

[9] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Transactions on Industry Applications,* vol. 42, no. 3, pp. 770-778, May/Jun. 2006.

[10] C. J. Gajanayake, L. Lin, G. Hoay, S. P. Lam, and S. L. Kian, "Extended-boost Z-source inverters," *IEEE Transactions on Power Electronics,* vol. 25, no. 10, pp. 2642-2652, Oct. 2010.

[11] Y. Zhou, W. Huang, and J. Zhao *et al*., "Switched coupled inductor quasi-Z-source inverters," *Transactions of China Electrotechnical Society,* vol. 29, no. 6, pp. 31-39, Dec. 2014.

[12] S. Huang, Y. Zhang, and F. Rong, "A ride-through strategy of D-permanent magnet synchronous generator system based on Z-Source inverter during the asymmetrical faults," *Transactions of China Electrotechnical Society,* no. S1, pp. 92-101, 2016.

[13] Y. He, L. Zhang, and J. Chen, "Voltage drop suppression of Z-source inverter using space vector PWM method," *Transactions of China Electrotechnical Society,* vol. 32, no. 2, pp. 228-237, Apr. 2017.

[14] M. Zhu, D. Li, P. C. Loh, and F. Blaabjerg, "Tapped-inductor Z-source inverters with enhanced voltage boost inversion abilities," in *Proc. IEEE Int. Conf. Sustainable Energy Technol*., Dec. 2010, pp. 1-6.

[15] V. Jagan and S. Das, "Two-tapped inductor quasi impedance source inverter (2TL-qZSI) for PV applications," in *Proc. IEEE Int. Conf. on Power Systems (ICPS 2016)*, Mar. 2016, pp. 1-6.

[16] M. Adamowicz, R. Strzelecki, F. Z. Peng, J. Guzinski and H. A. Rub, "New type LCCT-Z-source inverters," in *Proc. EPE*, Sep. 2011, pp. 1-10.

[17] M. K. Nguyen, Y. C. Lim, and S. J. Park, "Improved trans-Z-source inverter with continuous input current and boost inversion capability," *IEEE Transactions on Power Electronics,* vol. 28, no. 10, pp. 4500-4510, Oct. 2013.

[18] M. K. Nguyen, Y. C. Lim and Y. G. Kim, "TZ-source inverters," *IEEE Transactions on Industry Electronics*, vol. 60, no. 12, pp. 5686-5695, Dec. 2013.

[19] J. J. Soon and K. S. Low, "Sigma-Z-source inverters," *IET Power*

Electronics, vol. 8, no. 5, pp. 715-723, May 2015.
[20] S. S. Nag and S. Mishra, "A coupled inductor based high boost inverter with sub-unity turns-ratio range," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7534-7543, Nov. 2016.
[21] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Y-source impedance network," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3250-3254, July 2014.
[22] Y. P. Siwakoti, F. Blaabjerg, V. P. Galigekere, A. Ayachit, and M. K. Kazimierczuk, "A-source impedance network," *IEEE Transactions on Power Electronics,* vol. 31, no. 12, pp. 8081-8087, Dec. 2016.
[23] R. Strzelecki, M. Adamowicz, N. Strzelecka, and W. Bury, "New type T-source inverter," in *Proc. CPE 2009,* May 2009, pp. 191-195.
[24] W. Qian, F. Z. Peng, and H. Cha, "Trans-Z-source inverters," *IEEE Transactions on Power Electronics,* vol. 26, no. 12, pp. 3453-3463, Dec. 2011.
[25] P. C. Loh, D. Li, and F. Blaabjerg, "Γ-Z-source inverters," *IEEE Transactions on Power Electronics,* vol. 28, no. 11, pp. 4880-4884, Nov. 2013.
[26] P. C. Loh and F. Blaabjerg, "Magnetically coupled impedance-source inverters," *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 2177-2187, Sept./Oct. 2013.
[27] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Effects of leakage inductances on magnetically coupled Y-source network," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5662-5666, Nov. 2014.
[28] H. Fathi and H. Madadi, "Enhanced-Boost Z-source inverters with switched Z-impedance," *IEEE Transactions on Industry Electronics*, vol. 63, no. 2, pp. 691-703, Feb. 2016.
[29] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion Part I: A topological review," *IEEE Transactions on Power Electronics,* vol. 30, no. 2, pp. 699-716, Feb. 2015.

Xupeng Fang was born in Shandong Province, China, in 1971. He received the B.S. and M.S. degrees from the Shandong University of Science and Technology of China, Qingdao, in 1994 and 1997, respectively, majored in industry automation, electrical drive and its automation, respectively, and the Ph.D. degree from the Zhejiang University of China, Hangzhou, in 2005, in electrical engineering. He joined the Shandong University of Science and Technology, Qingdao, China, in 1997 and now he is an Associate Professor in the College of Electrical Engineering and Automation. He was a visiting scholar in the Power electronics and Motor drive center of Michigan State University from March, 2013 to March, 2014. He has published over 90 papers, wherein includes over 30 papers in IEEE Transactions and IEEE conference proceedings, and held 14 patents, and has applied for 2 invention patents that in the examination stage. His research interests include Z-source converter and its applications, utility applications of power electronics such as active filters and FACTs devices, renewable resources generation. Dr. Fang is a senior member of China Electrotechnical Society Power Electronics Society and an invited reviewer of *IEEE Transactions on Power Electronics, IEEE Transactions on Industrial Electronics, IEEE Transactions on Circuits and Systems, IEEE Transactions on Transportation Electrification* and *Transactions of China Electrotechnical Society.*

Bolong Ma was born in Shandong Province, China, in 1984. He received the B.S. degree from the Shengli College of China University of Petroleum, Dongying, in 2015, majored in electrical engineering and its automation, and now he is pursuing his Master's degree in the Shandong University of Science and Technology, majored in electrical engineering.

Guanzhong Gao was born in Shandong Province, China, in 1993. He received the B.S. from the Shandong University of Agricultural of China, Taian, in 2016, majored in electrical engineering and its automation, and now he is pursuing his Master's degree in the Shandong University of Science and Technology, majored in electrical engineering.

Lixin Gao was born in Shandong Province, China, in 1992. She received the B.S. from the Shandong University of Agricultural of China, Taian, in 2015, majored in electrical engineering and its automation, and now she is pursuing her Master's degree in the Shandong University of Science and Technology, majored in electrical engineering.

Evaluation of Level-Shifted and Phase-Shifted PWM Schemes for Seven Level Single-Phase Packed U Cell Inverter

Mohd Tariq, Mohammad Meraj, Abdul Azeem, Ali I. Maswood, Atif Iqbal, and Bharatiraja Chokkalingam

***Abstract*—An evaluation of level shifted and phase shifted triangular and sawtooth carrier modulation schemes for a seven level packed U cell (PUC) inverter is presented in this paper. The investigated PUC is the recently introduced topology for multilevel inverter having reduced switch count in comparison to the conventional topologies of multilevel inverters. The PUC inverter has six switches for 7 level inverter which is very less in comparison to the conventional topologies. In this paper, the level-shifted pulse width modulation (LS-PWM) and phase-shifted PWM (PS-PWM) for triangular and sawtooth carrier are presented and compared. A comparative harmonic analysis for all the cases is performed and results are presented in the paper. The difference in harmonics of the two modulation methods given by the theoretical approach for both the carrier is validated by the experimental results. DC voltage controller and load current controller of the PUC inverter are also designed and presented. The investigated PUC topology is tested in dynamic and steady state conditions and results obtained are presented. The analysis is done and validated using simulation in MATLAB® Simulink environment and experimental approaches using FPGA platform.**

***Index Terms*—Level shift, multilevel inverter, modulation, phase shift, PI controller, PUC inverter.**

I. Introduction

In the last two decades the risk and reality of environmental degradation have become more apparent. Fossil fuel which is the main source of energy, has led to the degradation of environment. For all these degradation and problem in environment, renewable energy sources can provide a solution [1], [2]. To meet the environmental challenges and depletion of fossil fuels, Photovoltaic (PV) source presents a highly attractive energy source during the last two decades. Multilevel inverter is required for connecting the PV sources which generates DC power to AC loads. Multilevel inverter circuits switch multiple DC sources in sequence at fundamental frequency to generate nearly sinusoidal stepped AC output voltage [3], [4].

In literature many traditional multilevel converters topologies like neutral point clamped converters (NPC), flying capacitors converters (FCC) and classic cascaded H-bridges [4]-[6] are available which enhanced the harmonic profile of the voltage and current but they offers high number of switching devices and capacitors which increases the cost and decreases the reliability. In [7], many new topologies of multilevel converter is given which offers less no. of switching device but the Packed U Cell (PUC) multilevel inverter topology is symmetrical and easy to control. For low and medium power applications where a PV panel installed at home is connected to local grid etc., a single-phase transformer-less DC-AC converter with minimum number of switch devices, capacitors and DC sources are required [8], [9]. PUC topology introduced in [10], [11] is working with only one DC source and having high power quality using a small number of passive and active components. The capacitors acts as auxiliary DC source in the PUC inverter. PUC inverter is suggested for PV application in [12] as it offers high efficiency. Many papers on control of PUC inverter are available in literature [13], [14], but a comparative analysis of different modulation carrier schemes is missing in the literature. Analysis of different carriers is essential as in local grid connected PV applications, the total harmonic distortion (THD) generated by the switching element should be minimum [15].

There are two modulation methods in the multicarrier PWM schemes: level shifted PWM (LS-PWM) [16] and phase shifted PWM (PS-PWM) [17]. Combination of the level-shifted PWM (LS-PWM) and the phase-shifted PWM (PS-PWM) is reported in [18]. It is called "level- and phase-shifted PWM (LPS-PWM)". The LPS-PWM realizes low voltage ripple on the capacitors. In [19], the comparison between the Phase-Shifted PWM and Level-Shifted PWM is done on a Modular Multilevel Single Delta Bridge Converter (SDBC) Inverter whereas in the proposed work the comparison is done on recently introduced Packed U Cell (PUC) Inverter. Since till date no such work is available on PUC inverter wherein different modulation techniques have been evaluated, hence in the proposed work, the authors wanted to investigate the effects of different modulation techniques/methods on the PUC inverter. In this paper a comparison between triangular and sawtooth carrier is done

Manuscript received January 3, 2018. This work is supported by NPRP-EP grant # X-033-2-007 from the Qatar National Research Fund (a member of Qatar Foundation). *(Corresponding author: Atif Iqbal.)*

M. Tariq and A. I. Maswood are with the School of Electrical and Electronic Engineering, Nanyang Technological University, 639798, Singapore, and M. Tariq is presently with the Department of Electrical Engineering, Aligarh Muslim University, Aligarh, 202002, India (e-mail: tariq.iitkgp@gmail.com; eamaswood@ntu.edu.sg).

M. Meraj and A. Iqbal are with the Department of Electrical Engineering, Qatar University, Doha, 2713, Qatar (e-mail: meraj@qu.edu.qa; atif.iqbal@qu.edu.qa).

A. Azeem is with the Department of Electrical Engineering, Aligarh Muslim University, Aligarh,202002, India (e-mail: azeem.abdul25@gmail.com).

B. Chakkolingam is with the Department of Electrical Engineering SRM University, Chennai, 603203, India (e-mail: bharatiraja@gmail.com).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00023

using level shifted and phase shifted PWM methods for PUC inverter. This study is important keeping in view the need to understand the operation of PUC inverter under different modulation schemes for achieving low THD.

The rest of the paper is organized as follows: In Section II operation of PUC inverter is explained. The generalized PWM spectral modeling is presented in Section III. Analysis of phase shifted and level shifted for triangular carrier is presented in Section IV whereas in Section V, analysis of phase shifted and level shifted for sawtooth carrier is presented. Section VI details the controller design for dc link and capacitor voltages and load current. Simulation and experimental results are presented in Section VII and VIII respectively. Conclusion is given in Section IX.

II. Operation of PUC Inverter

A seven level single-phase voltage source inverter with packed U-cell topology is shown in Fig. 1. This is called Packed U-cell because each unit of the inverter is of U shape. Depending upon the number of capacitors in the PUC topology different level of voltages can be achieved. In the PUC topology two capacitors (one is DC link capacitor and the second is the floating or flying or auxiliary capacitor) have been used to obtain seven levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$). The Voltage across second capacitor (C_2) i.e. V_b must be maintained at one-third of the voltage of the first capacitor (C_1) i.e. V_a. The relation between number of voltages level achieved and number of auxiliary capacitors used can be represented by (1).

$$N_v = 2^{Nc+2} - 1 \tag{1}$$

Where: N_v is number of voltage levels and N_c is number of auxiliary capacitors used.

The numbers of devices for different types of inverters (NPC, FLC, CHB and PUC) are shown in TABLE I. Six IGBTs have been used in the PUC topology for achieving 7 levels. These 6 IGBTs are subdivided into two legs, hence only three switches form one leg. Number of possible states can be given by (2).

$$N_p = 2^{Ns} \tag{2}$$

Where, N_p is number of possible states and N_s is number of switches in one leg.

There are 8 possible switching states in a single-phase PUC inverter as shown in Fig. 2 and listed in TABLE II. It is seen that there are three positive levels and three negative levels while two states yield zero voltage, namely state 4 and state 5. Zero voltage is produced when load is short circuit either though main switches or complimentary switches.

The switching function of the PUC inverter can be defined by (3) and the inverter output voltage can be defined by (4). The points x, b, c and y are shown in Fig. 1.

Based on the switching function shown in TABLE II, each voltage can be represented as given in (5) to (8).

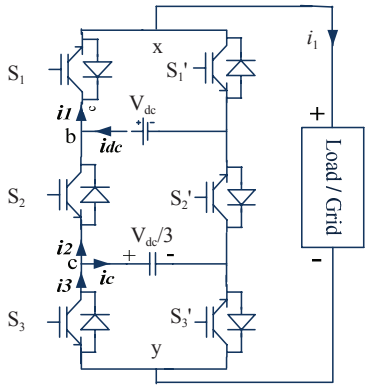


Fig. 1. Packed U-cell converter topology.

TABLE I
Seven Level Single Phase Inverter Topologies

Components	NPC	FLC	CHB	PUC
Power Switches (IGBTs)	24	24	12	6
Capacitors	6	30	3	2
Clamping Diodes	20	0	0	0

$$\begin{matrix} S_j = 0 \text{ if } S_j \text{ is Off} \\ 1 \text{ if } S_j \text{ is On} \end{matrix} \quad j = 1, 2, 3 \tag{3}$$

$$V_{xy} = V_{xb} + V_{bc} + V_{cy} \tag{4}$$

$$V_{xb} = V_1 (S_1 - 1) \tag{5}$$

$$V_{bc} = (V_1 - V_2)(1 - S_2) \tag{6}$$

$$V_{cy} = V_2 (1 - S_3) \tag{7}$$

$$V_{xy} = V_1 (S_1 - S_2) + V_2 (S_2 - S_3) \tag{8}$$

III. Generalized PWM Spectral Modeling

The distortion in the output current or voltage waveform with respect to an ideal sine wave is often used in comparing the effectiveness of different modulation processes. Since the output voltage of an inverter is a periodic function having time period (T), the root-mean-square (RMS) value of the function can be defined as:

$$V_{rms} = V_{1,rms} \sqrt{1 + THD^2} \tag{9}$$

From (9), it is to be noted that if the THD is zero then the RMS value of the waveform is equal to the fundamental RMS voltage. Hence, it is clear that the modulation technique has to be designed in such a way so as to obtain the minimum THD or ideally zero THD. Moreover, when the inverter is connected to the induction motor operating pump for standalone solar PV pumping application, it is to be noted that the total copper loss

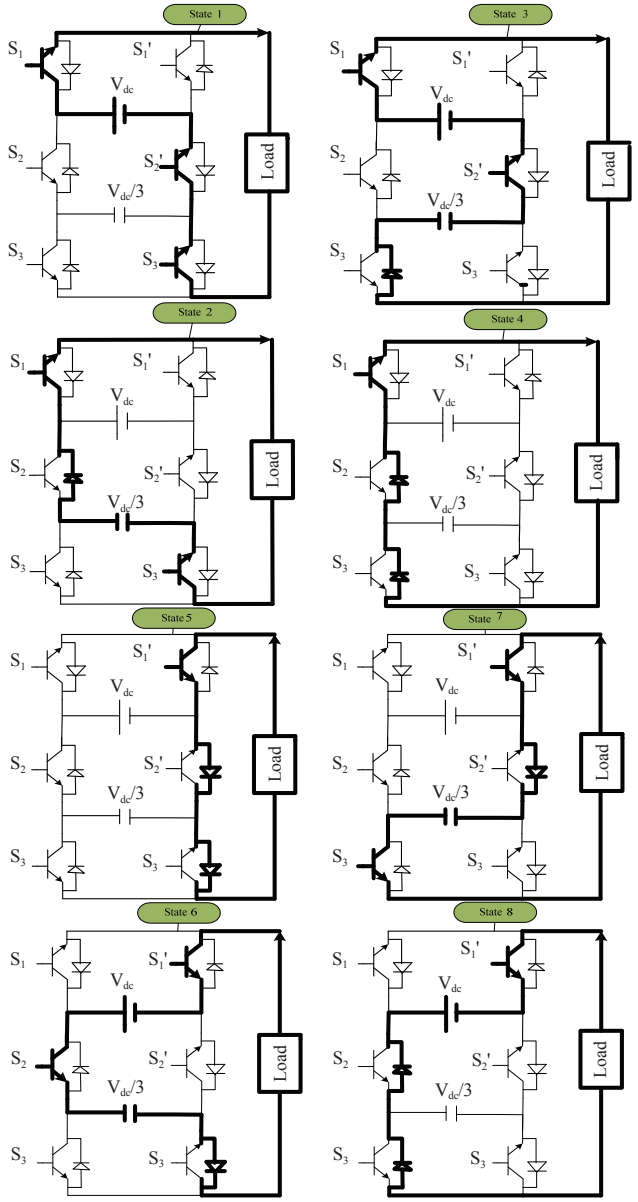


Fig. 2. Switching states for single-phase AFLC/PUC.

TABLE II
SWITCHING COMBINATION FOR ONE LEG OF PUC

State	Voltage	S_1	S_2	S_3
0	V_a	1	0	0
1	V_a - V_b	1	0	1
2	V_b	1	1	0
3	0	1	1	1
3'	0	0	0	0
4	-V_a	0	0	1
5	V_b - V_a	0	1	0
6	-V_b	0	1	1

due to the harmonic content in the quasi-square-wave inverter can be 0.5-1% of the rating. Hence all these leads to the formulation of modulation strategies for reducing the component of harmonics in the inverter output voltage.

The mathematical model is developed for PWM triangular and sawtooth carrier signals for the defined reference here for better understanding of the subject. The PWM output spectrum is described using the analytical models when different carrier signals (triangular/sawtooth) are used.

Fourier series is used to represent a periodic function. For the presented application, Fourier analysis is performed on the PWM waveform for 50 Hz (20 milliseconds period) which corresponds to one cycle of the reference. The switching point as shown in the pulse width modulation waveform of Fig. 6(I)(a), Fig. 6(I)(b), Fig. 6(I)(c), and Fig. 6(I)(d) is described using the trigonometry equation given in (10). The trigonometric equation involves both the linear function of time (which basically represent carrier signal) and a sinusoidal reference.

$$s(t) = S_0 + S_1 \cos(2\pi f_1 t + \theta_1) \tag{10}$$

In the next two sections, (10) is used for doing the spectral analysis of various pulse width modulation methods. Depending upon the application under study, in (10), S_0 and S_1 are set to zero. For solving (10), a new two-dimensional function (double Fourier series for decomposing the function) given in (11) is introduced in the literature wherein the reference fundamental and the carrier frequency are corresponding to an independent variable respectively [20]. A periodical 2 (two) dimensional function f (x, y) having periodicity in x and y both, with a time period equal to 2π for both the axes, is represented by a double Fourier series which is mathematically expressed here in (11).

$$\begin{aligned} f(x,y) = \frac{A_{00}}{2} + \sum_{n=1}^{+\infty} \left(A_{0n} \cos ny + B_{0n} \sin ny \right) \\ + \left(A_{m0} \cos mx + B_{m0} \sin mx \right) \\ + \sum_{m=1}^{+\infty} \sum_{n=\pm 1}^{\pm\infty} \left(A_{mn} \cos(mx+ny) + B_{mn} \sin(mx+ny) \right) \end{aligned} \tag{11}$$

Where the coefficients A_{mn} and B_{mn} are defined as follows in (11) and (12)

$$A_{mn} = \frac{1}{2\pi^2} \int_0^{2\pi} \int_0^{2\pi} f(x,y) \cos(mx+ny)\, dx\, dy, \tag{12}$$

$$B_{mn} = \frac{1}{2\pi^2} \int_0^{2\pi} \int_0^{2\pi} f(x,y) \sin(mx+ny)\, dx\, dy. \tag{13}$$

In (11), the PWM waveform contains the fundamental sine, the DC and many harmonics components described (grouped) as follows:

(i) Carrier frequency and its associated harmonics.
(ii) Sideband harmonics of the carrier and its associated harmonics. The sideband harmonics appears because of the modulated reference.

For sawtooth carrier modulation the sideband harmonic amplitude at frequency $f = mf_c + nf_1$ equals to as given in (14),

whereas for triangular carrier modulation it equals to as given in (15). In (14) and (15), the $J_n(z)$ which is a Bessel function is defined as given in (16):

$$\frac{J_n(m\pi M)}{m\pi} \tag{14}$$

$$\frac{2}{m\pi}J_n\left(\frac{m\pi M}{2}\right) \tag{15}$$

$$J_n(z)=\frac{j^{-n}}{\pi}\int_0^{2\pi} e^{jz\cos\theta}\, e^{jn\theta}\, d\theta \tag{16}$$

In (16), the argument z can be a complex or real number. If z is real, the function will also be real. Whereas, "n" will be an integer always. Bessel functions $J_0(x)$ through $J_{10}(x)$ is shown in the Fig. 3. The double Fourier series and Bessel functions are used in the analysis of the triangular and sawtooth carrier modulation techniques in the next two sections.

IV. Triangular Carrier Level Shifted and Phase Shifted PWM Analysis

The triangular carrier based modulation scheme is given in Fig. (4) wherein the formulation of double Fourier series is shown. Fig. 4(a) shows the triangular and reference signals. Fig. 4(b) shows the resulting PWM output which is expressed mathematically in (17). As shown in Fig. 4(c) the original carrier along with the reference are sequenced in the correct and inverted position alternatively. The stacked carriers are mathematically written as c(t), $2C_m-c(t)$, $2C_m+c(t)$, $4C_m-c(t)$, whereas the stacked references can be mathematically expressed as r(t), $2C_m - r(t)$, $2C_m + r(t)$, $4C_m - r(t)$. As seen in Fig. 4(c), line AB is the extension of the rising edge of the first triangle of the original carrier, c(t). It can be observed that the PWM generated by the interaction between the original carrier and reference signal and PWM generated with the intersection of the line AB with the references shifted (stacked).

$$\begin{aligned} b_{pwm}(t) &= D+\frac{M}{2}\cos(\omega_1 t+\theta_1) \\ &+\sum_{m=1}^{+\infty}\frac{2}{m\pi}J_0\left(\frac{m\pi M}{2}\right)\sin(Dm\pi)\cos\left[m(\omega_c t+\theta_c)\right] \\ &+\sum_{m=1}^{+\infty}\sum_{n=\pm1}^{\pm\infty}\frac{2}{m\pi}J_n\left(\frac{m\pi M}{2}\right)\sin\left(\frac{(2Dm+n)\pi}{2}\right) \\ &.\cos\left[m(\omega_c t+\theta_c)+n(\omega_1 t+\theta_1)\right]. \end{aligned} \tag{17}$$

The phase voltage of an inverter with natural sampled PWM and triangular carrier can be described by (18). (18) is derived in [21] using the expression given in the works of Black in [22]. The three terms in (18) are explained as: a) Term 1 is directly proportional to the modulation index and it represents the fundamental frequency amplitude; b) Term 2 represents the carrier frequency harmonics amplitude and multiples of the carrier frequency and it is due to the presence of the sin (mt/2); c) Term 3

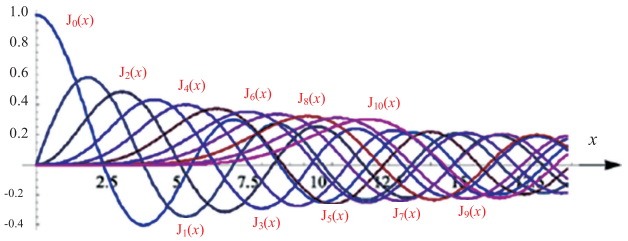


Fig. 3. Bessel functions plot for $J_0(x)$ to $J_{10}(x)$ [20].

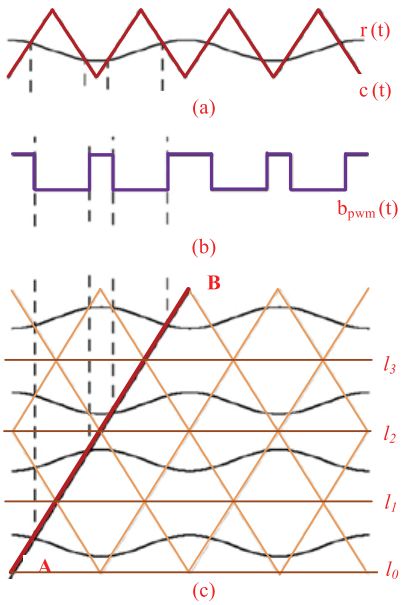


Fig. 4. Triangular carrier and development of a double Fourier series.

gives the amplitudes of the harmonics in the sidebands around each multiple of the carrier frequency.

$$\begin{aligned} F(t) &= \frac{MV}{2}\cos(\omega_F t)+\frac{2V}{\pi}\sum_{m=1}^{\infty}J_o\left(mM\frac{\pi}{2}\right)\sin\left(m\frac{\pi}{2}\right).\cos(m\omega_c t) \\ &+\frac{2V}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{J_n\left(mM\frac{\pi}{2}\right)}{m}.\sin\left((m+n)\frac{\pi}{2}\right)\cos(m\omega_c+n\omega_F t) \end{aligned} \tag{18}$$

Fig. 6(I)(a), Fig. 6(I)(b), Fig. 6(I)(c), and Fig. 6(I)(d), shows level shifted and phase shifted triangular carrier and sinusoidal reference signal generation of PWM signals for IGBT switches of inverter.

V. Sawtooth Carrier Based Level Shifted and Phase Shifted PWM Analysis

The sawtooth carrier based modulation scheme is given in Fig. 5 wherein the formulation of double Fourier series is shown. Fig. 5(a) shows the triangular and reference signals. Fig. 5(b) shows the resulting PWM output which is expressed mathematically in (19). As shown in Fig. 5(c) the original carrier along with the reference are stacked equidistantly. The stacked carriers are

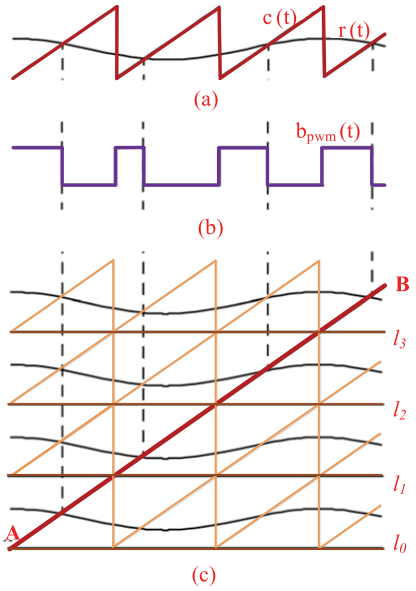


Fig. 5. Sawtooth carrier and development of a double Fourier series.

mathematically written as c(t), C_m + c(t), $2C_m$ + c(t), whereas the stacked references can be mathematically expressed as r(t), C_m + r(t), $2C_m$ + r(t). As seen in Fig. 5(c), line AB is the extension of the first slope of the original sawtooth signal. The lines l_1, l_2, l_3 and l_4 (shown horizontally) is separating the different stacked carriers with a spacing of C_m between them. It can be observed that the PWM generated by the interaction between the original carrier and reference signal and PWM generated with the intersection of the line AB with the references shifted (stacked).

The sawtooth carrier wavesas shown in Fig. 6(II)(a), Fig. 6(II)(b), Fig. 6(II)(c), and Fig. 6(II)(d) consists of sawtooth carrier as well as inverted sawtooth carrier. This arrangement is done so as to produce the trailing edge modulation in the positive cycle and to produce the leading edge modulation in the negative cycle. The trailing-edge modulation scheme has a wave having the leading (rising) edge of PWM output occurs at fixed instants in time while the position of the trailing (falling) edge is modulated as the reference signal level varies. Similarly, for leading edge modulation scheme has the trailing (falling) edge of PWM output occurs at fixed instants in time while the position of the leading (rising) edge is modulated as the reference signal level varies.

$$b_{pwm}(t) = D + \frac{M}{2}\cos(\omega_1 t + \theta_1) + \sum_{m=1}^{+\infty}\frac{1}{m\pi}\begin{Bmatrix}\sin\left[m(\omega_c t+\theta_c)\right] \\ -J_0(m\pi M)\sin\left[m(\omega_c t+\theta_c)-2mD\pi\right]\end{Bmatrix} + \sum_{m=1}^{+\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin\begin{bmatrix}\frac{n\pi}{2}-m(\omega_c t+\theta_c) \\ -n(\omega_1 t+\theta_1)+2mD\pi\end{bmatrix} \quad (19)$$

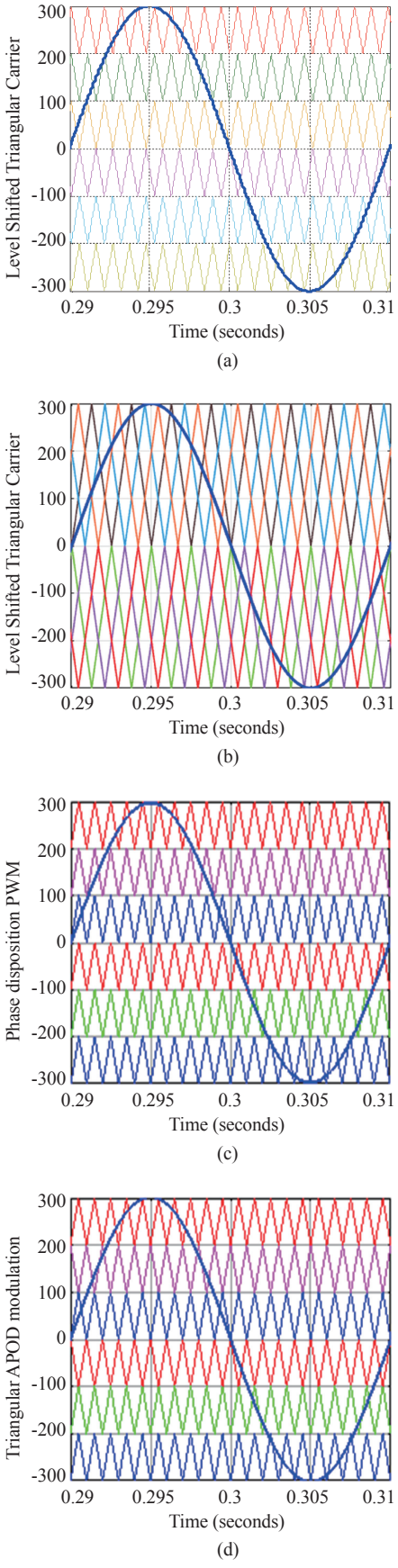
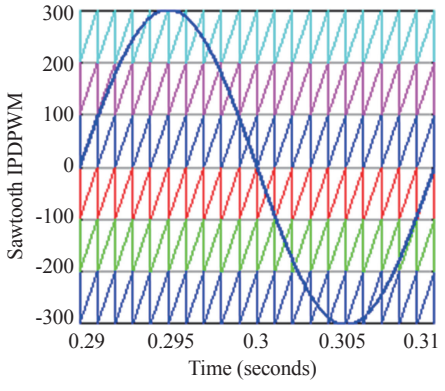
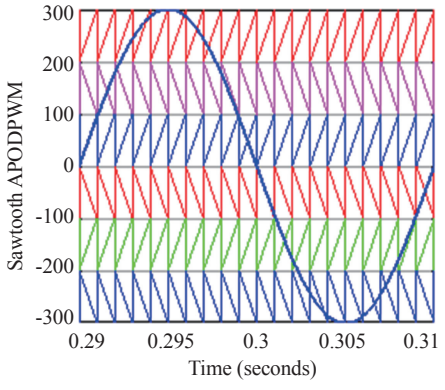


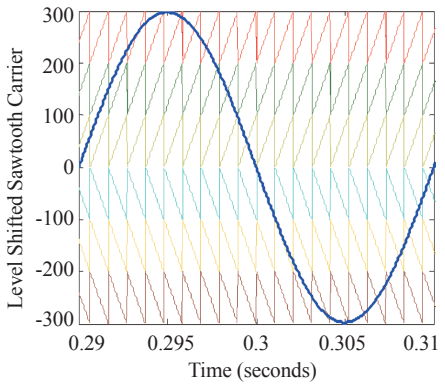
Fig. 6(I). Triangular carrier waves. (a) Phase opposition disposition. (b) Phase shifted. (c) Phase disposition. (d) Alternate phase opposition disposition.



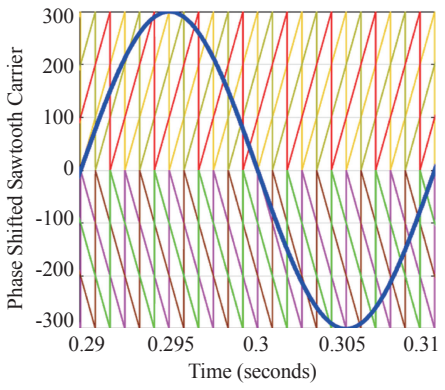
(a)



(b)



(c)



(d)

Fig. 6(II). Sawtooth carrier waves. (a) Phase disposition. (b) Alternate phase opposition disposition. (c) Phase opposition disposition. (d) Phase shifted.

$$F(t)=\frac{MV}{2}\cos(\omega_F t)+\frac{V}{\pi}\sum_{m=1}^{\infty}\frac{\sin(m\omega_c t)}{m} - \frac{V}{\pi}\sum_{m=1}^{\infty}\frac{J_o(mM\pi)}{m}\left[\cos(m\pi)\sin(m\omega_c t)\right] - \frac{V}{\pi}\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{J_n(mM\pi)}{m}[\cos(m\pi+n\pi/2).\sin(m\omega_c+n\omega_F t) - \sin(m\pi+n\pi/2).\cos(m\omega_c t+n\omega_F t)]. \quad (20)$$

The phase voltage of an inverter with natural sampled PWM and sawtooth carrier can be described by (20).

(10) is derived in [21] using the expression given in the works of Black [22]. Here again, the amplitude of the fundamental is directly proportional to modulation index. Whereas the second and third term shows that all harmonics of the carrier frequency is existing in the phase voltage.

In (18) and (20):

ω_F = frequency of the fundamental (reference)

ω_c = frequency of the carrier signal (rad/s),

M = modulation index, V= value of the dc supply voltage,

J_o, J_n = Bessel functions of the first kind.

VI. Design of DC-Link Volatge, Auxiliary Capacitor Voltage and Load Curremt Controllers

A. Voltage Controllers

The solar PV is considered as the source (DC link) of the analysed PUC inverter. In PV applications, using capacitors of electrolytic type will be less desirable because of short lifetime mainly when installed in outdoor temperatures. Film capacitors have very long life time hence these can replace electrolytic capacitors, however they have very high prices. This makes practical limitation for dc link capacitor, establishing significant doubly frequency ripple on dc link and clamping capacitor voltages. This doubly frequency ripple further couples with control loop & causes distortions in output current.

Therefore, a notch filter (stop band filter) is placed on the feedback signal of DC voltage to attenuate ripple component. Notch filter is given as in (21).

$$H(s)=\frac{s^2+2\varepsilon_1\omega_n s+\omega_n^2}{s^2+2\varepsilon_2\omega_n s+\omega_n^2} \quad (21)$$

Where ω_n is double of fundamental frequency. For getting maximum number of output voltage levels from the inverter, the auxiliary capacitor or holding capacitor voltage should be held at one third of dc link voltage. A simple PI controller is used to control the voltage of the auxiliary capacitor voltage and dc link voltage. The load current is represented as in (22).

$$i_L = c\,\frac{dv_c}{dt} \quad (22)$$

Assuming a phase margin of 75° and critically damped system with damping factor ε=1.The transfer function of the sys-

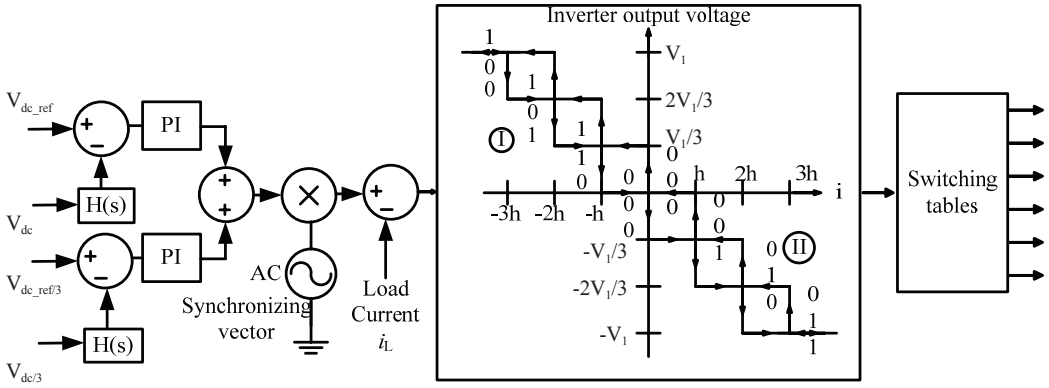


Fig. 7. Control block diagram for generation of gate pulses.

tem is given as in (23), (24):

$$G(s) = \left(K_p + \frac{K_I}{s}\right) * \left(\frac{1}{sC}\right) \tag{23}$$

$$G(j\omega) = \frac{K_I + j\omega K_p}{-\omega^2 C} \tag{24}$$

The phase of the system can be written as in (25):

$$Phase\,(G\,(j\omega)) = -180° + \tan^{-1}\left(\frac{\omega K_p}{K_I}\right) \tag{25}$$

$$\begin{aligned} -180° + 75° &= -180° + \tan^{-1}\left(\frac{\omega K_p}{K_I}\right) \\ (3.73^2 + 1)\,K_I^2 &= (10)^4 * 2.2^2 * 10^{-6} \end{aligned} \tag{26}$$

The phase margin of the system is 75°. Thus, $K_I = 0.06$, $K_p = 0.02$ as calculated from (26).

B. Current Controller

From Fig. 1, on applying KVL on the load or grid side, (27) and (28) are achieved:

$$\text{For RL load: } V_{an} = R * i_L + L\frac{di_L}{dt} \tag{27}$$

$$\text{For grid load: } V_{an} = R_f * i_L + L_f\frac{di_L}{dt} + V_{ac} \tag{28}$$

Here R & L are load resistor & reactor and R_f & L_f are filter inductor internal resistance & inductance. For generationof seven level output voltage, one should control the DC-link & auxiliary capacitor voltages to V_{dc} and $V_{dc}/3$, respectively. This has been done by voltage controllers as shown in Fig. 7. When actual injected current into grid or load is lower than reference (current error) then positive voltage across the load is applied thus Fig. 7 sector I are applied.When actual injected current into grid or load is greater than reference (current error) then negative voltage across the load is applied thus Fig. 7 sector II are applied.

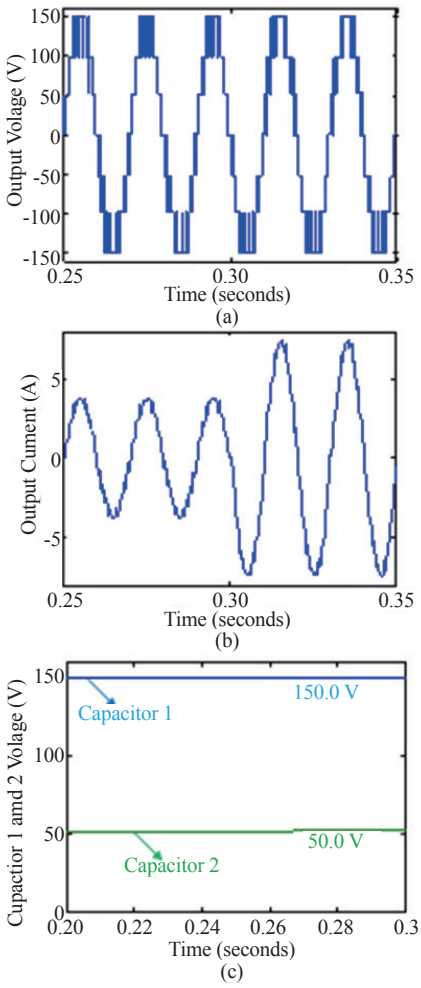


Fig. 8. (a) Output voltage; (b) Output current; (c) Capacitor voltage.

VII. Simulation Results and Discussion

The PUC inverter model is built using MATLAB®/Simulink simulation software package to verify the performance of different triangular and sawtooth carrier-based PWM modulation schemes. In line to the above, single DC source is selected of 150 V. The second capacitor has the voltage rating of 1/3rd of the DC source. Fig. 8(c) shows the capacitor voltages to be 150 V

TABLE III
THE OPERATING CONDITIONS FOR SIMULATION

Simulation Set up Parameters	Rating
Capacitors	4700 μF
Load Resistance	40 Ω
Load Inductance	12 mH
Modulating Frequency	1 kHz
Load Change (at time)	0.3 seconds

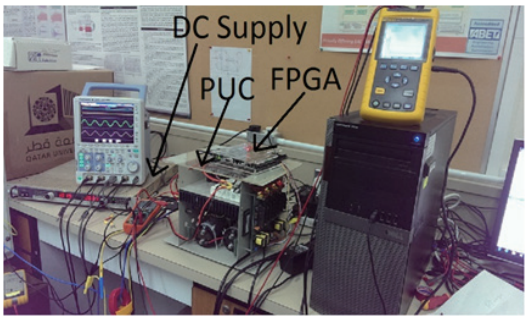


Fig. 9. Experimental set up.

and 50 V. Seven level output voltage (shown in Fig. 8 (a)) is obtained using TABLE II switching combination. TABLE III outlines the operating condition of PUC inverter for simulation. The value of inductor andresistance at the load is 12 mH and 40 ohm respectively. At 0.3 seconds the load was doubled, hence the current doubles at 0.3 seconds (as shown in Fig. 8(b)). At 0.3 seconds, two 40 ohm resistors were connected in parallel to make 20 ohm effective resistance. It can be observed that the output voltage is unchanged at 0.3 seconds thus verifying the effectiveness of the closed loop control.

VIII. EXPERIMENTAL RESULTS AND DISCUSSION

Experimental investigation is done to validate the theoretical findings and simulation results presented in the paper so far. Experiment is conducted with customised hardware comprising of Semikron modules SKM75GB12T4 as shown in Fig. 9. Control code is written in system generator and processed using FPGA board Vortex 5. Fluke 42B power analyser is used to to record the total harmonic distortion (THD) in the voltage and current waveform.The experimental parameters is presented in TABLE IV where the parameters are chosen to match with the available components. Fig. 10 shows the experimental result showing 7 level waveform and sinusoidal fundamental of PUC inverter output voltage and sinusoidal load current. It can be observed from the figure that the load current is in phase with the fundamental output of the PUC waveform. The dynamics of DC link voltage control loop and load current loop is tested and the resulting waveforms are presented in Fig. 11, Fig. 12, Fig. 13. The DC link voltage is ramped down from 54 V to 36 V (33% decrease in the initial value) and the transients are recorded in Fig. 11. The DC link voltage is seen to quickly drops to the new value and correspondingly the auxiliary capacitor voltage follows the change. The output voltage level drops and the current magnitude drops accordingly. Further test is conducted by increasing the DC link voltage value and the corresponding results are shown in Fig. 13. The DC link voltage is ramped up from 36 V to 54 V (50% increase in the initial value). The auxiliary capacitor voltage is seen to follow the change and settle to the new value and the voltage and current follows the change quickly. Hence it is concluded that both the DC voltage control loop and load current loop have large control bandwidth with fast dynamics. The THD is calculated using Fluke 42B power analyser for different modulation schemes and are shown in Fig. 12(a) to Fig. 12(p). The THD obtained are tabulated in TABLE V wherein the THD for voltage and current both are shown to be minimum for the case of level shifted triangular carrier.

TABLE IV
EXPERIMENTAL SET UP PARAMETERS

Parameter	Value
Auxiliary Capacitor	4700 μF
Load Resistance	4 Ω
Load Inductance	10 mH
Modulating Frequency	1 kHz
Sinusoidal Reference Frequency	50 Hz
DC link voltage	54 V
Dead-band period	2μS

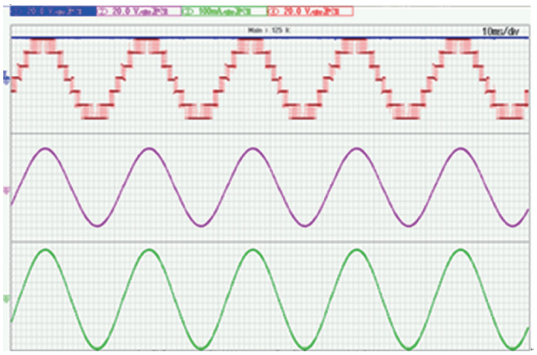


Fig. 10. Experimental result showing 7 level waveform and sinusoidal fundamental of PUC inverter output voltage and sinusoidal load current.

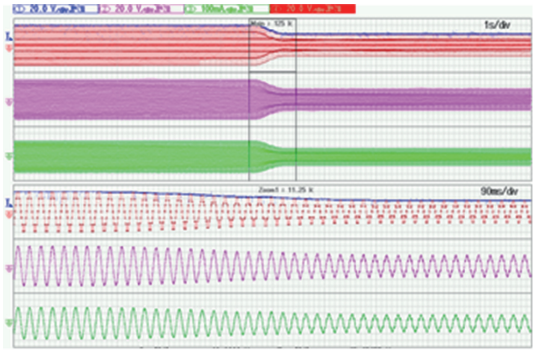


Fig. 11. Experimental result showing dynamic condition when load current is decreased.

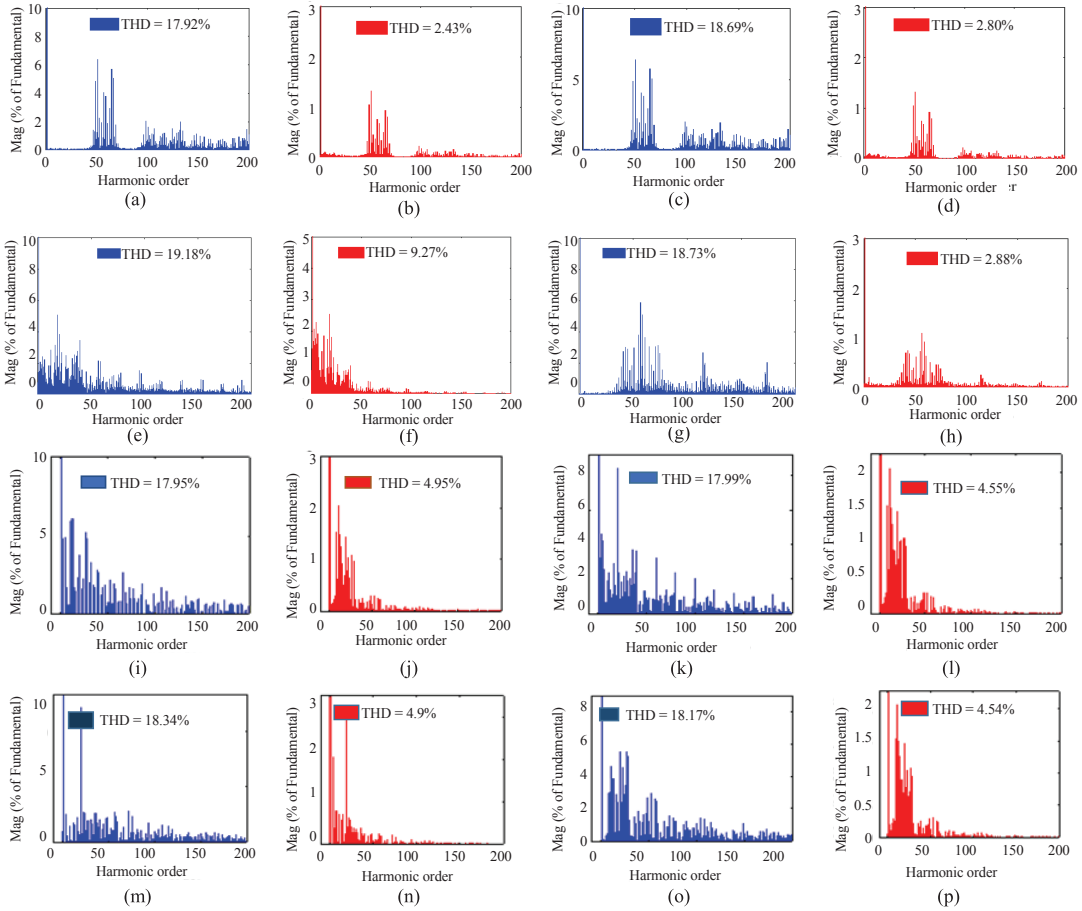


Fig. 12 (a) FFT of voltage for triangular PD-PWM scheme; (b) FFT of current for triangular PD-PWM scheme; (c) FFT of voltage for triangular phase shifted scheme; (d) FFT of current for triangular phase shifted scheme; (e) FFT of voltage for sawtooth PD-PWM scheme; (f) FFT of current for sawtooth PD-PWM scheme; (g) FFT of voltage for sawtooth phase shifted scheme; (h) FFT of current for sawtooth phase shifted scheme; (i) FFT of voltage for sawtooth AOPD; (j) FFT of current for sawtooth APOD; (k) FFT of voltage for sawtooth IPD; (l) FFT of current for sawtooth IPD; (m) FFT of voltage for triangular IPD; (n) FFT of current for triangular IPD; (o) FFT of voltage for triangular APOD; (p) FFT of current for triangular APOD.

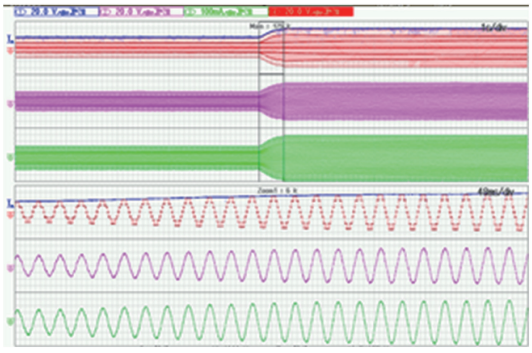


Fig. 13. Experimental result showing dynamic condition when load current is increased.

TABLE V
FFT Results for Different Modulation Schemes

Particulars	THD (in %)	
	Triangular Carrier	
PWM Schemes	*Voltage*	*Current*
PD-PWM	18.34	4.90
POD-PWM	17.92	2.43
APOD-PWM	18.17	4.54
Phase-Shifted	18.69	2.80
	Sawtooth Carrier	
PD-PWM	17.99	4.54
POD-PWM	19.18	9.27
APOD-PWM	17.95	4.54
Phase-Shifted	18.73	2.88

IX. Conclusion

The paper has presented the comparison of different PWM schemes which can be applied to the PUC inverter. Investigating the suitable modulation schemes is very essential with respect to local grid integration, as the power quality is directly dependent on THD. Triangular carrier based PWM schemes is exhibiting the better result than the sawtooth carrier based PWM schemes as the triangular level shifted carrier PWM scheme is better as compared to sawtooth level shifted carrier because in triangular level shifted carrier both edges (falling and rising) of pulses are modulated which improves the harmonic spectrum. However, in the sawtooth level shifted carrier only rising edges are mod-

ulated. Hence triangular level shifted carrier PWM scheme can be applied for integrating the PUC inverter with PV and local grid systems. Triangular level shifted carrier PWM scheme for PUC inverter has been suggested based on observing the THD in voltage and current which are respectively just 17.92% and 2.43%. The whole system i.e. solar panel, boost converter with PUC inverter will be very cost effective, besides having good reliability and power quality as it has the minimum number of power electronics devices compared to previously introduced multilevel inverter topologies. With reduced number of capacitors and power switches seven levels of voltages have been achieved for PUC inverter.

References

[1] F. A. Rahman, M. M. A. Aziz, R. Saidur, W. A. A. Bakar, M. R. Hainin, R. Putrajaya, and N. A. Hassan, "Pollution to solution: Capture and sequestration of carbon dioxide (CO2) and its utilization as a renewable energy source for a sustainable future", *Renewable and Sustainable Energy Reviews,*vol. 71, pp. 112-126, May 2017.

[2] Y. Yang, A. Sangwongwanich, and F. Blaabjerg, "Design for reliability of power electronics for grid-connected photovoltaic systems," in *CPSS Transactions on Power Electronics and Applications,* vol. 1, no. 1, pp. 92-103, Dec. 2016..

[3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 724-738, 2002.

[4] Q. M. Attique, Y. Li, and K. Wang, "A survey on space-vector pulse width modulation for multilevel inverters," in *CPSS Transactions on Power Electronics and Applications,* vol. 2, no. 3, pp. 226-236, Sept. 2017.

[5] Z. Mohzani, B. P. McGrath, and D. G. Holmes, "A generalized natural balance model and balance booster filter design for three-level Neutral-Point-Clamped converters," in *IEEE Transactions on Industry Applications,* vol. 51, no. 6, pp. 4605-4613, Nov.-Dec. 2015.

[6] A. Kulkarni and V. John, "HF transformer based grid-connected inverter topology for photovoltaic systems". *IETE Technical Review.* Vol. 33, no. 1, pp. 69-75, Jan 2016.

[7] K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A rReview," in *IEEE Transactions on Power Electronic*s, vol. 31, no. 1, pp. 135-151, Jan. 2016.

[8] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 2703-2712, 2008.

[9] H. Vahedi, P.-A. Labbe, and K. Al-Haddad, "Sensor-Less five-level packed U-Cell inverter operating in stand-alone and grid-connected modes," *Industrial Informatics, IEEE Transactions on,* vol. 12, no. 1, pp. 361-370, 2017.

[10] K. Al-Haddad, Y. Ounejjar, and L.-A. Gregoire, "Multilevel electric power converter," U.S. Patent 2743085, 2010ed: Google Patents, 2009.

[11] Y. Ounejjar, K. Al-Haddad, and L. A. Gregoire, "Packed U cells multilevel converter topology: theoretical study and experimental validation," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 1294-1306, 2011.

[12] A. Sheir, M. Orabi, M. E. Ahmed, A. Iqbal, and M. Youssef, "A high efficiency single-phase multilevel packed U cell inverter for photovoltaic applications," in *Telecommunications Energy Conference (INTELEC), 2014 IEEE 36th International*, 2014, pp. 1-6.

[13] Y. Ounejjar, K. Al-Haddad, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: experimental validation," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 3808-3816, 2012.

[14] A. Iqbal, M. Tariq, K. Rahman, and A. Al-qahtani, "Control of packed U-cell multilevel five-phase voltage source inverter," *Qatar Foundation Annual Research Conference*, p. ITPP0493, 2014.

[15] M. Sidrach-de-Cardona, and J. Carretero, "Analysis of the current total harmonic distortion for different single-phase inverters for grid-connected pv-systems," *Solar Energy Materials and Solar Cells,* vol. 87, pp. 529-540, 5// 2005.

[16] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 858-867, 2002.

[17] Y. Hinago and H. Koizumi, "A modulation method for capacitor voltage ripple reduction of the switched-capacitor inverter using series/parallel conversion," *in Industrial Technology (ICIT), 2011 IEEE International Conference on*, 2011, pp. 105-109.

[18] A. Tsunoda, Y. Hinago, and H. Koizumi, "Level-and phase-shifted PWM for seven-level switched-capacitor inverter using series/parallel conversion," *Industrial Electronics, IEEE Transactions on,* vol. 61, pp. 4011-4021, 2014.

[19] P. Sochor and H. Akagi, "The oretical and experimental comparison between phase-shifted PWM and level-shifted PWM in a modular multilevel SDBC inverter for utility-scale photovoltaic applications," in *IEEE Trans. Ind. Appl.,* vol. 53, no. 5, pp. 4695-4707, Sept.-Oct. 2017

[20] J. Sun, (Jan. 2012), "Pulse-width modulation," in *Dynamics and Control of Switched Electronic Systems (Advances in Industrial Control Series), F. Vasca and L. Iannelli, Eds. London, U.K.: Springer*, [Online].Jan. 2012, pp. 25–61. [Online]. Available: http://link.springer.com/chapter/10.1007/978-1-4471-2885-4_2.

[21] J. Hamman and F. S. Van Der Merwe, "Voltage harmonics generated by voltage-fed inverters using PWM natural sampling,"*Power Electronics, IEEE Transactions on,* vol. 3, pp. 297-302, 1988.

[22] H. S. Black, Modulation theory: van Nostrand, 1953

Mohd Tariq obtained a B. Tech in electrical engineering from Aligarh Muslim University and M. Tech in machine drives and power electronics from the Indian Institute of Technology (IIT)-Kharagpur. He pursued his Ph.D. from Nanyang Technological University, Singapore. Before joining his PhD, he has worked as a Scientist in an autonomous institute (NIOT, Chennai) under ministry of earth sciences, govt. of India and also worked as an Assistant Professor at National Institute of Technology (NIT) – Bhopal, India. Currently, he is working as an Assistant Professor at Department of Electrical Engineering, Aligarh Muslim University, Aligarh, India.

He is a recipient of the best paper award from the IEEE Industrial Applications Society's (IAS) and Industrial Electronic Society, Malaysia Section – Annual Symposium (ISCAIE-2016) held in Penang, Malaysia. His research interest includes power converters, energy storage devices and its optimal control for the electrified transportation and renewable energy application.

Mohammad Meraj has completed M.Tech from IIT Kharagpur. Presently he is pursuing his Ph.D. from Qatar University, Qatar. His interest is in the area of power electronics converters and its control.

Abdul Azeem has completed his M.Tech from Aligarh Muslim University, Aligarh, India. His interest is in the area of power electronics converters and its control. He has published a number of papers in international journals and conferences.

Ali I. Maswood received the B.Eng. and M.Eng. degrees (with first class honors) from the Moscow Power Engineering Institute, Moscow, Russia, and the Ph.D. degree from Concordia University, Montreal, QC, Canada. Having taught in Canada for a number of years, he joined Nanyang Technological University, Singapore, in 1991, where he is currently an Associate Professor. His research interests include power electronics, particularly in converter generated harmonics, novel inverter topologies, advanced PWM switching, and power quality. He has authored numerous international journal and conference publications. He is also the Chapter Author of the Power Electronics Handbook(Academic, 2002).

Dr. Maswood is actively involved in the local IEEE Industry Applications Society/Power Electronics Society Chapter.

Atif Iqbal, Ph.D. (UK), Senior Member IEEE, Fellow IET (UK), Fellow IE (India)- Associate Professor at Electrical Engineering, Qatar University and Former Full Professor at Electrical Engineering, Aligarh Muslim University (AMU), Aligarh, India. Recipient of Outstanding Faculty Merit Award AY 2014-2015 and Research excellence award at Qatar University, Doha, Qatar. He received his B.Sc. (Gold Medal) and M.Sc. Engineering (Electrical) degrees in 1991 and 1996, respectively, from the Aligarh Muslim University (AMU), Aligarh, India and PhD in 2006 from Liverpool John Moores University, Liverpool, UK. He has been employed as a Lecturer in the Department of Electrical Engineering, AMU, Aligarh since 1991 where he served as Full Professor until Aug. 2016. He is recipient of Maulana Tufail Ahmad Gold Medal for standing first at B.Sc. Engg. Exams in 1991 from AMU. He has received best research papers awards at IEEE ICIT-2013 and IET-SESICON-2013. He has published widely in International Journals and Conferences his research findings related to Power Electronics and Renewable Energy Sources. Dr. Iqbal has authored/co-authored more than 270 research papers and one book and two chapters in two other books. He has supervised several large R&D projects. His principal area of research interest is modeling and simulation of power electronic converters, control of multi-phase motor drives and renewable energy sources.

He is an Associate Editor of IEEE Transaction of Industrial Applications and Guest Associate Editor of IEEE Transaction of Power Electronics.

Bharatiraja Chokkalingam was born in Namakkal, India on Jan 08, 1980. B. Eng. from KCT, Coimbatore, India, M. Eng. from GCT, India, and Ph.D. degree from the SRM University, India (all in electrical engineering) in 2002, 2006 and 2015, respectively. He completed his Postdoctoral Fellow at Centre for Energy and Electric Power, Faculty of Engineering and the Built Environment, Tshwane University of technology, South Africa in 2016. He is currently working as an Assistant Professor at SRM University, Kattankulathur, Chennai, India. His research interest includes multilevel inverters, control of power converters, SVPWM techniques for power converters and adjustable speed drives, electrical vehicle and smart grid. He has authored several International Journal and Conference publications on these topics.

Power Quality Improvement Utilizing PV Fed Unified Power Quality Conditioner Based on UV-PI and PR-R Controller

Santanu Kumar Dash and Pravat Kumar Ray

***Abstract*—This paper presents control and configuration of photovoltaic fed unified power quality conditioner for the purpose of power quality enhancement. Literature studies convey that fixed PI gains used in the control schemes of Unified Power Quality Conditioners (UPQC) and PV-UPQC cannot easily adapt to various dynamic conditions. In this paper a novel online tunings method for PI control gains is adopted in the controllers of series and shunt converters of PV-UPQC. Unlike the previously implemented JAYA algorithm which has a single objective function utilized in the controller of DSTATCOM for improvement of only current quality, the new adaptive JAYA algorithm has two separate objective function, employed in shunt and series inverter control of PV-UPQC system for improvement of both current and voltage quality under various operational scenarios for power quality issues. The experimental results verify that implementation of JAYA based auto tuning PI controller increases the adaptivity of PV-UPQC system towards various dynamic conditions. Results obtained are compared with conventional optimization algorithms with fixed PI gains pertaining to a distribution system for validating its efficacy.**

***Index Terms*—Adaptive JAYA Optimization, current harmonics, power quality, PV-UPQC, voltage sags/swells.**

I. Introduction

THE sudden increase in application of non-linear loads in distribution system has induced power quality issues related to voltage and current which has become a serious concern among researchers. The advanced semiconductor technology based systems are the primary cause of current perturbations in the distributed system. Moreover, these nonlinear loads behave abnormally in presence of voltage disturbances. Thereby power quality enhancement devices or power conditioners have received much concentration towards power quality enhancement applications [1], [2]. Among various power types of conditioners unified power quality conditioner (UPQC) has earned enormous interest due to high performance capability for mitigation of voltage and current perturbations in the distribution system [2], [3]. Moreover, increased proliferation of renewable energy systems like solar and wind to the distribution systems have become major concern due to their intermittent nature. Various topologies for grid connected PV systems are reported along with active filtering solution to maintain the current quality in the supply system [4]. PV grid integration adds advantage to the conventional system but due to the presence of nonlinear loads, voltage perturbations which appear at the point of common coupling (PCC). Therefore the demand of the future energy systems to acquire improved power quality can be achieved through suitable grid integration topology with satisfactory cost effective solutions. The utilization of UPQC for grid integration of PV systems has increased the functionality of conventional UPQC which provide desired solution for issues related to power quality and protection of critical loads from voltage fluctuations [5], [6].

Power control of inverters of UPQC has been traditionally implemented with SRF, modified SRF theory [7], resonant controllers (PR-R and V-PI) [9], and UVTG controller [8], [10] for the generation of reference signals. Despite of good performance of advanced controllers for UPQC, conventional PI controllers fail to operate satisfactorily in dynamic conditions of voltage and current, due to its non zero steady state error. The utilization of PI controller for conventional control algorithm for PV interfaced UPQC system may not provide satisfactory performance during dynamic conditions. As the PV interfaced UPQC system is responsible for simultaneous elimination of various voltage and current power quality issues. Therefore the need to design an advanced controller and perfect PI controller gains in concern with adaptavity towards severe conditions of grid cannot be ignored.

The drawback of the utilized optimization schemes for PV-DSTATCOM lies in the selection of appropriate parameter to reach the optimum solution [11], [12]. On the contrary, finding the optimum solution by selection of proper system parameters becomes difficult, for complex system like PV-UPQC. In this regard, a rigorous literature survey have been done, which clearly reveals that many attempts have adopted for the performance enhancement of UPQC but there are very few literatures reported for PV-UPQC systems for performance and efficiency enhancement through the utilization of optimization schemes which is specifically free from algorithmic parameters. The conventional optimization schemes may be inactive during the dynamic conditions and there is much chance to converge at local minima due to inappropriate selection of the control parameters. Utilizing advanced optimization algorithms for PV-DSTATCOM in [11], solution for only current quality issues with fixed PI controller gains have been presented. Therefore an initiative

Manuscript received February 14, 2018.

The authors are with the Department of Electrical Engineering, National Institute of Technology Rourkela, 769008 India (e-mail: santanu4129@gmail.com; rayp@nitrkl.ac.in).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00024

has been taken by the authors to enhance the performance of PV-UPQC system.

Traditional evolutionary optimization algorithms have common controlling parameters like population size, number of generations and they also require algorithm specific parameters like PSO uses inertia weight, cognitive parameters; Ant colony bee uses number of onlooker bees, employed bees [11]. Considering all these facts, JAYA optimization algorithm has an advanced solution, which doesn't use the algorithm specific parameters, but it only depends on the common controlling parameters. The JAYA algorithm also has major advantage over Teaching Learning Based Optimization (TLBO) such as economical in computation, provides easy platform for discrete optimization and suitable for fewer design variables [11]. The proposed JAYA optimization scheme converges comparatively faster than TLBO to reach the global optimum solution.

To cope with the severe dynamic conditions of voltage and current, PV interfaced UPQC system requires an online and automatic tuning approach. Therefore authors have proposed a novel JAYA optimization scheme with a feature of auto tuning capability of PI controller gain values for PV interfaced UPQC system. Inspired from the auto tuning JAYA optimization scheme in [13] for efficient MPPT tracking and the critic based self tuning PI structure for voltage source converters in [14], the research work has been developed for the PV-UPQC system. The implementation of JAYA algorithm in online manner for PV interfaced UPQC systems have not been reported so far for performance and power quality improvement. The previously proposed JAYA algorithm for DSTATCOM has utilized single cost function useful for improvement of current quality [11]; however the authors have presented a new JAYA optimization algorithm, which has separate objective function for shunt and series inverter control useful for simultaneous current and voltage quality improvement in the PV interfaced UPQC system. The present novel JAYA optimization methodology is introduced in this research work to reach the optimum values for PI gains in accordance with the aforementioned grid disturbances by increasing the adaptavity of the system. Adaptive JAYA optimization based Proportional Resonant and Resonant (PR-R) controller for series converter and Unit Vector PI controller (UV-PI) for shunt converter of PV-UPQC have been implemented, which are presented in Section III. New JAYA adaptive optimization technique explained in Section IV is useful for determination of suitable PI gain values on occurrence of severe grid conditions. Furthermore, PV interfaced UPQC (PV-UPQC) system presented in Section II is integrated with grid by utilizing a LCL filter at the output of shunt converter of PV-UPQC to minimize harmonics in PWM switching. The experimental prototype development, discussion on obtained experimental results by the implementation of proposed algorithm is clearly presented in Section V. The conclusion of the research work presented in the paper is included in Section VI.

II. System Configuration

Photovoltaic interfaced UPQC topology as proposed by the author in the paper is shown in Fig. 1. The grid is connected to

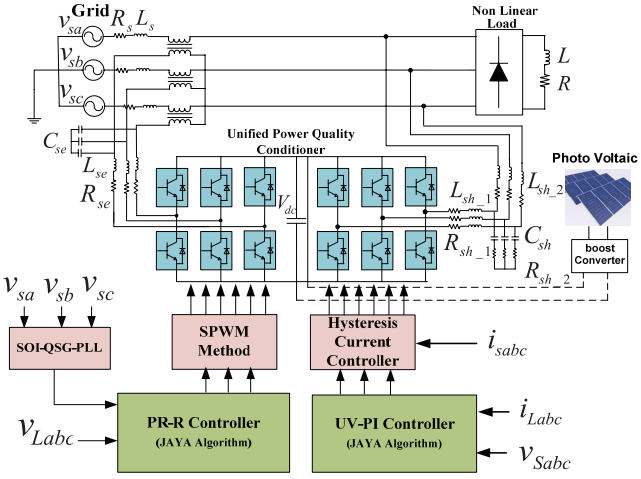


Fig.1. Block diagram of proposed photovoltaic fed-UPQC.

a linear as well as a nonlinear load. UPQC system is installed in the distribution line where shunt inverter is placed at load side and the series inverter is present close to source side through series transformers. The series and shunt inverter of the UPQC share a common dc-link. The PV system containing a boost converter is interfaced to the grid through the dc-link of the UPQC. The grid voltage and the voltage required by the load can be represented here as v_s and v_L. The current consumed by the load is given as i_L and the grid current is presented as i_s.

III. Proposed Control Scheme of PV-UPQC

The complexity arises in the UPQC when photovoltaic system is fed to the grid through UPQC. As PV-UPQC system is new therefore, most of the conventional control scheme applied to the UPQC system may be applied to the present configuration. However the present complex system becomes more complex with the conventional algorithm and may not perform satisfactorily. The control configuration of the PV-UPQC includes shunt inverter control, series inverter control and maximum power point tracking controller. The system utilizes UV-PI controller for shunt inverter based on novel JAYA optimization to determine the best values for PI gains. The controller of PV-UPQC utilizes P&O (Perturb and Observer) MPPT method for maximum power extraction from the PV [13] for the regulation of dc link voltage.

A. MPPT Controller for the Boost Converter

The MPPT algorithms are utilized for boost converter of the PV System to extract maximum power. In the present paper authors have adopted P&O scheme of MPPT [13] to extract maximum power from PV array. The utilization of MPP controller is associated with shunt inverter controller is shown in Fig. 2(a).

B. UV-PI Controller Along With JAYA Optimization for Shunt Inverter

In the present paper authors have proposed UV-PI controller based on JAYA Optimization for the control of shunt inverter of

UPQC as shown in Fig. 2. The measured amplitude of the three phase voltage (v_{sa}, v_{sb}, v_{sc}) is given as

$$v_t = \sqrt{\frac{2}{3}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)} \tag{1}$$

Evaluation of unit templates for instantaneous phase voltage is given as (v_{ap}, v_{bp}, v_{cp})

$$v_{ap} = \frac{v_{sa}}{v_t}, \qquad v_{bp} = \frac{v_{sb}}{v_t}, \qquad v_{cp} = \frac{v_{sc}}{v_t} \tag{2}$$

Another set of unit templates are formed with a phase shift of 90° is given as (v_{aq}, v_{bq}, v_{cq})

$$v_{aq} = -\frac{v_{bp}}{\sqrt{3}} + \frac{v_{cp}}{\sqrt{3}}, \quad v_{bq} = \frac{(3v_{ap} + v_{bp} - v_{cp})}{2\sqrt{3}}$$
$$v_{cq} = (-3v_{ap} + v_{bp} - v_{cp})/2\sqrt{3} \tag{3}$$

Optimization of the perfect PI gain is required for the performance enhancement of present system. Thereby JAYA optimization is employed with the controller to find perfect PI gains. The evaluated error between terminal voltage (v_t) and the reference of terminal voltage is the input to the discussed JAYA optimization based PI controller block. The active power component of grid current is determined by comparison of measured actual dc link voltage and reference dc bus voltage. The regulation of dc voltage is highly essential which is maintained through PI controller (I_{cdp}). In Fig. 2(b) amplitude of active power component of reference source current is given. The amplitude of the active power is generated by subtraction of feed forward component of PV (I_{Fpv}) from the summation of active power component of self generated dc bus of PV-UPQC and average magnitude of active power component of load current (I_{Lap}). In presence of voltage sag and voltage swell in the grid voltage, adjustment in the grid currents are necessary to maintain the power balance in the system. Thereby feed forward signal of PV is essential for the control algorithm for fast dynamic response and to suppress oscillations in the grid currents. The feed forward signal of PV (I_{Fpv}) is evaluated from amplitude of terminal voltage (v_t) and power extracted from PV array, which is represented as (P_{pv}/v_t) .

$$I_{dp}^* = I_{cdp} + I_{Lap} - I_{Fpv} \tag{4}$$

Comparison of output obtained from dc bus voltage of PI controller and average load reactive power component results in amplitude of reactive power component of reference source current.

$$I_{dq}^* = I_{cdq} - I_{Laq} \tag{5}$$

Where reactive power component of load current average is presented as I_{Laq} is the output obtained from the output of low pass filter. The evaluated terminal voltage is compared with a

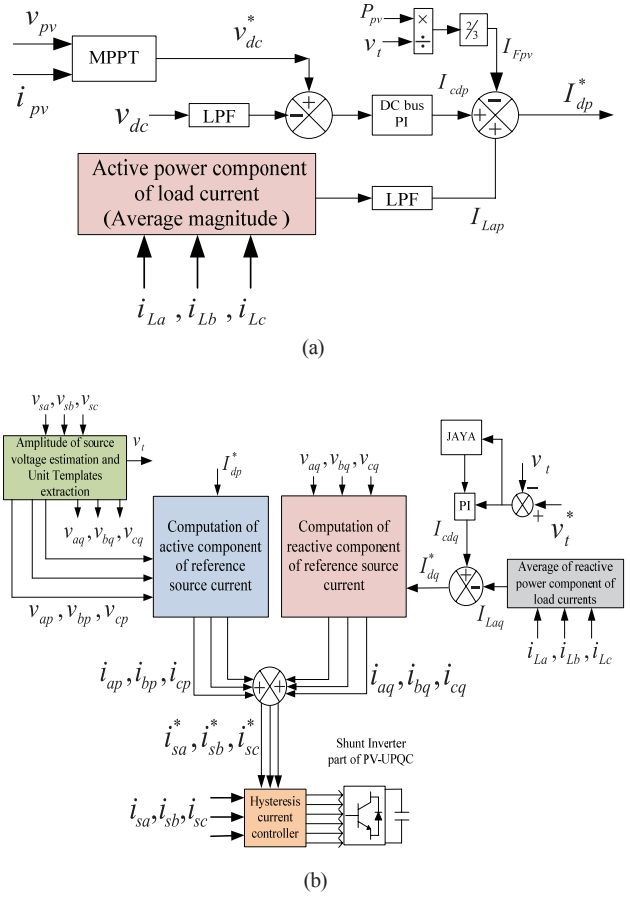


Fig. 2. Approximate diagram of shunt inverter controller (a) block diagram of DC link controller, (b) proposed controller for shunt inverter.

reference terminal voltage (v_t^*) to generate errors corresponding to grid voltage conditions (voltage sags and voltage swells). The generated error is given to PI controller supported by proposed JAYA algorithm to provide suitable output. As the proposed JAYA optimization is implemented, PI controller is tuned according to the sensed voltage distortions. The output of JAYA based PI controller (I_{cdq}) is compared with average reactive power component of load current (I_{Laq}) to provide the reactive power component of the reference source current (I_{dq}^*) as given in (9).

So the present shunt controller computation method provides error free evaluation of reactive power component of the reference source current (I_{dq}^*). The active current component and reactive current component per phase is evaluated as

$$i_{ap} = I_{dp}^* v_{ap}, i_{bp} = I_{dp}^* v_{bp}, i_{cp} = I_{dp}^* v_{cp} \tag{6}$$

$$i_{aq} = I_{dq}^* v_{aq}, i_{bq} = I_{dq}^* v_{bq}, i_{cq} = I_{dq}^* v_{cq} \tag{7}$$

The total reference source currents can be evaluated for PV-UPQC are represented as

$$i_{sa}^* = i_{ap} + i_{aq}, \quad i_{sb}^* = i_{bp} + i_{bq}, \quad i_{sc}^* = i_{cp} + i_{cq} \tag{8}$$

The considered PV-UPQC system has the responsibility to supply active component as well as reactive component, both the components are added. The generated reference currents are passed through hysteresis current controller, which is employed to provide desired gate pulses for the shunt inverter of PV-UPQC. The tuning of PI controller gains is desired to improve the PV-UPQC performance which affects the controller efficiency and improvement of power quality. Therefore the proposed optimization is utilized to obtain the gain of PI controller.

C. Controller Based on JAYA Optimization for Series Inverter

Presence of voltage sags and voltage swells in the distribution line make the load voltage distorted. Therefore series inverter of PV-UPQC plays significant role in elimination of voltage distortions from the load voltages for steady state behaviour of loads. In the present scenario, control of series inverter is much necessary for better elimination of voltage distortions. Thereby the authors have proposed a new PR-R controller utilizing an adaptive JAYA optimization as given in Fig. 3 and is implemented for PV-UPQC. The present controller has the ability for regulation of positive sequence components. Even in highly distorted grid conditions, it is desired that series inverter of PV-UPQC has to provide suitable injecting voltage signal to regulate the load voltage magnitude.

$$v_L = v_s + v_i \tag{9}$$

Where v_L is sensed load voltage, v_i is the injected voltage and v_s is the source voltage. It is assumed that during steady state condition, measured grid voltage remains sinusoidal with phase angle of θ_s. The supply voltage is reduced from $V_s^{'}$ to $V_s^{''}$, with voltage sag condition without having phase jump. On the contrary, the condition of voltage sag with a phase jump of δ, the series inverter controller of PV-UPQC injecting voltage signal with phase angle of $(\theta_s+\delta)$. The voltage controller of PV-UPQC in d-q reference frame has been implemented. In the present controller an advanced PLL has been utilized to obtain the phase angle of supply voltage for the desired transformation. The SOI-QSG-PLL is discussed in the following section. The switching signals for the series inverter are provided by the voltage reference signal generated by the proposed series inverter controller of PV-UPQC as given in Fig. 3.

The transfer function to explain the PR-R controller [9] is given as

$$G_{PR-R} = K_P + \frac{K_{r1}\omega_c s}{s^2 + 2\omega_c s + (\omega_s)^2} \tag{10}$$

Where K_{r1} denotes the resonant gain, proportional gain is presented as K_P, ω_s is selected resonant frequency, cut-off frequency is represented as ω_c. The configuration and development of a nonlinear controller is seems to be difficult. Therefore PR-R controller is developed to enlarge the bandwidth and quick action against voltage disturbances. The present series inverter controller shows its performance to achieve unity gain and zero phases at the respective resonant frequency.

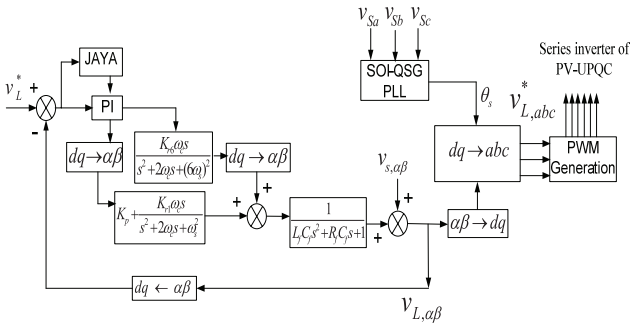


Fig. 3. Approximate block diagram of JAYA based voltage controller for series inverter.

The series inverter controller of the system utilizes new adaptive JAYA optimization as shown in Fig. 3. The PI controller gains are important for the operation of PR-R voltage controller for the generation of the reference voltages useful for switching signal generation for series inverter. To find suitable of PI controller gains, proposed JAYA optimization has been employed. The presence of LC filter in PV-UPQC at the output of series inverter is represented by the transfer function G_{LC}. The disturbances in the grid voltages are measured to evaluate the error for the updating the parameter values.

To determine the suitable values of proportional gain and integral gain, implementation of proposed new JAYA algorithm in the PV-UPQC controller has been achieved. The selected parameters for the PR-R series inverter controller are given here as $K_P = 2$, $K_{r1} = 2000$, $\omega_c = 10$ rad/sec, which are selected before optimization [9]. The suitable optimization parameters obtained from computation of JAYA optimization is given in TABLE II. The developed transfer function can be represented as

$$G_C = \frac{G_{PR-R}(s)G_{LC}(s)}{1+G_{PR-R}(s)G_{LC}(s)}, \tag{11}$$ where $$G_{LC}(s) = \frac{1}{L_f C_f s^2 + R_f C_f s + 1}$$

The present research work proposes a new and adaptive JAYA optimization algorithm to reach the best optimal values for the enhancement of efficiency of the present system.

D. SOI-QSG Based PLL

Grid synchronization of PV-UPQC is important in the present complex system; therefore double second order integral-quadrature signal generator based phase locked loop SOI-QSG-PLL block is implemented in the present system. The advanced PLL technique of SOI-QSG-PLL is employed in the present series inverter controller. The SOI-QSG-PLL is utilized for filtering function to determine signals with 90° phase shift which act as input to the positive sequence calculator. The effective utilization of synchronous reference frame based PLL provides adaptive characteristic to system for any frequency change condition. A detailed explanation of SOI-QSG is given in [15].

IV. JAYA Optimization Algorithm and Formulation

Celebration at defeating an opponent by neglecting the failure

at any condition to become victorious is termed as victory. Following this culture, an optimization method is named as JAYA (means victory) optimization tool. The speciality of this algorithm is to have the control parameters which propel its result more nearer to the best solution by eliminating the worst one. Due to its less implementation complexity, faster convergence and little computation time over other optimization schemes, the authors have considered JAYA optimization for the present system. Combining the features of JAYA algorithm and online tuning process of the PI controller, inspired from literatures [11], [13] and [14], the JAYA based auto tuning PI controller is proposed. The system feedback, evaluated by the actual and reference signals is considered as the objective function of the system. As the shunt converter is responsible for current quality in the grid, thereby objective function is defined as presented in (14). Similarly for the series converter the objective function is defined which depends on the actual load voltage and reference load voltage signals as presented in (15). The computation at iterations or steps of implementation of JAYA optimization is shown in the flow chart of Fig. 4.

A. JAYA Based Algorithm

In the JAYA based methodology, considered objective function is required to be minimized or maximized. Before the computation of the algorithm, population size is needed to be addressed clearly which is denoted as (y =1, 2, 3...n). It is assumed in the algorithm that at any of the iteration "i", the determination of the design variables can be given as (d =1, 2, 3...k). At the initialization point the termination criteria is also required to be defined. After initialization of the population size and determination of design variables, a random population is generated. Determination of the best candidate solution from the selected range of the candidate solution for the objective function of $f(x)$ is the priority of the algorithm. Finding the worst solution from the range of candidate solution is required for the computation. After considering minimizing function, lowest value of $f(x)$ is selected as the solution which is best among the range. The random variable selected for the algorithm are r_1 and r_2 of the range [0,1]. It is assumed that $D_{d,y,i}$ value of d^{th} variable, y^{th} candidate and i^{th} iteration, which can be presented as

$$D'_{d,y,i} = D_{d,y,i} + r_{1,d,i}\left(D_{d,best,i} - \left|D_{d,y,i}\right|\right) - r_{2,d,i}\left(D_{d,worst,i} - \left|D_{d,y,i}\right|\right) \quad (12)$$

where $D_{d,y,i}$ denoted as the value of d^{th} variable for y^{th} candidate at i^{th} iteration. $D_{d,best,i}$ is represented as the best candidate obtained and $D_{d,worst,i}$ is considered as the worst candidate. The important characteristic of proposed JAYA algorithm has shown its tendency to move towards the best solution by dominating over the worst solution. The concept utilized for the present algorithm is represented by (12). The positive term present in (12) clearly denotes that the candidate moves towards the best solution. Similarly the negative part of (12) reveals the truth that the candidate solution is away from the worst. After evaluation of all the particles present in the solution, it is required that the convergence criteria should be met. According to the change in grid disturbances, the algorithm again looks for the new best solution by generating a fresh initialization command. Again upon finding the new values of design variables, objective function is evaluated which is compared with previously obtained value.

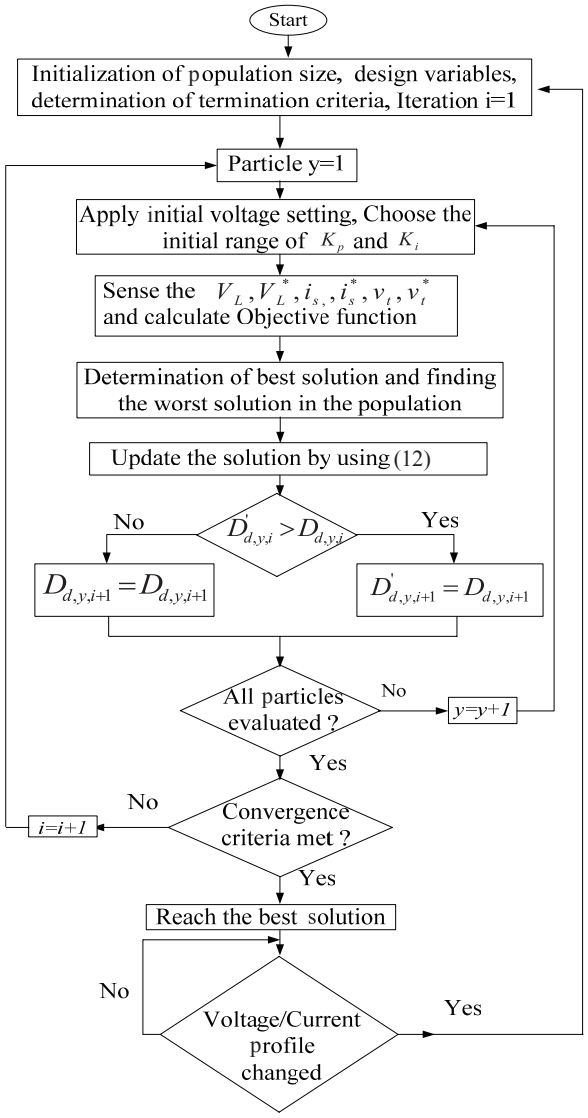


Fig. 4. Proposed flow chart for JAYA optimization based auto tuned PI controller.

B. Implementation of JAYA Based Algorithm for PI Controller

As the PV-UPQC system is open to voltage and current disturbances, so novel JAYA optimization scheme is employed to determine the PI controller gains (K_p and K_i) in the present paper. Therefore the algorithm should have adaptive nature to sense the type of disturbances; thereby it can define the objective function. The tuning of the PI controller gains and evaluation in this study relies on the grid disturbances according to grid situations. The reduction on the updates of negative solution and thereby auto tuning of PI gains lead to enhancement of

the controller performance. The updated solution will be considered as the best solution if it satisfies the convergence criteria. Otherwise, the considered solution is discarded and new updated solution of the algorithm will be generated. The flow chart of the proposed JAYA methodology for PV–UPQC is presented in Fig. 4.

Step 1 Initialization and parameter setting: The population size as n has been considered for the proposed JAYA algorithm. The initial values of the K_p and K_i is set within the range of [1.2, 3.8] and [0.6, 2.4].

Step 2 Objective function evaluation: Two different objective functions are selected for the PV-UPQC for shunt converter and series converter as both are employed for different function with separate controller.

Problem defined in the present paper signifies the formulation of a minimizing function. Therefore a candidate solution providing the lowest value of $f(x)$ has been selected as the required best solution. The evaluated mean square error (MSE) is considered as the objective function is given as

$$J = MSE = \sum_{i=1}^{iter} e_r^2 \tag{13}$$

Where e_r is different for both shunt and series inverter of PV-UPQC as they have different control algorithms. Therefore e_r for shunt and series inverter can be presented as

$$e_{r\_shunt} = \frac{\left|i_{sa}^* - i_{sa}\right| + \left|i_{sb}^* - i_{sb}\right| + \left|i_{sc}^* - i_{sc}\right| + \left|v_t^* - v_t\right|}{iter} \tag{14}$$

$$e_{r\_series} = \frac{\left|v_{La}^* - v_{La}\right| + \left|v_{Lb}^* - v_{Lb}\right| + \left|v_{Lc}^* - v_{Lc}\right|}{iter} \tag{15}$$

Step 3 Fitness solution evaluation: The implementation of JAYA optimization in PV-UPQC system controller is to determine minimum constraints values. The application of JAYA algorithm has a randomly generated initial condition which is evaluated according to predefined cost function. At the time of initialization command for JAYA algorithm, require selection of initial population size or candidate solution, is defined as (y=1,2,3...n). Considering the candidate solution controller gains are determined through ith iteration and dth variable for choosing the best and worst solutions. Therefore $D_{d,y,i}$ is directly related to the proposed inverter controllers of PV-UPQC. This method is selected to find controller gains to increase the performance and efficiency to achieve power quality standards.

Step 4 Convergence criterion: The proposed JAYA algorithm will conclude with the best solution if the error between the best candidate solution and the worst candidate solution is less than the threshold ε.

Step 5 Re-initialization of JAYA algorithm: The proposed JAYA algorithm will be initialized again, when a different grid perturbations occurs. The occurrence of current harmonics, voltage sags, voltage swells, and voltage unbalance will activate the proposed JAYA algorithm.

Determination of optimized PI controller gains values are achieved through the aforementioned method. (12) plays major role in this process, where $D'_{d,y,i}$ is the value of optimized parameter. Previously obtained value of PI controller gain is considered as $D_{d,y,i}$ for this algorithm. In accordance with new JAYA optimization methodology, the worst performing gain values are eliminated which is related to the negative term of (12) presented as "$-r_{2,d,i}(D_{d,worst,i} - |D_{d,y,i}|)$".

The best performing gain values are accepted by the optimization algorithm presented as the positive term of (12) "$D_{d,y,i} + r_{1,d,i}(D_{d,best,i} - |D_{d,y,i}|)$".

In accordance with various grid distortions, the controller of PV-UPQC requires specific value of PI controller gains to provide satisfactory performance. By utilization of conventional PI gain tuning method, certain values of PI gains have been obtained for particular type of grid distortion.

These values of PI gains have been considered to provide a valid range for proposed JAYA based optimization algorithm, useful for accurate gain tuning on the appearance of different distortion levels. The initialization of JAYA optimization for the computation to find the PI controller gains has been done with selection of the range of PI controller gains is presented as k_p (1.2→3.8) and k_i (0.6→2.4).

V. Results and Discussion

The proposed JAYA based auto tuned PI controller is applied to the controller of PV-UPQC system for the performance improvement. Simulation models are developed for the proposed system and methodology in MATLAB/Simulink environment to verify the efficiency and performance of the proposed controller. The superiority of the JAYA based auto tuned PI controller is claimed by comparing the results from the proposed controller with the conventional PSO and TLBO based fixed PI gain optimization method. The comparative evaluations of the methodologies considered are quantitatively evaluated in TABLE I. Various cases are considered for different grid conditions, represented as the mean and standard deviation of PI gain error values are presented the TABLE I.

A detail discussion on prototype development and results are presented in this section. Prototype developed for PV-UPQC is shown in Fig. 5. The PV system is interfaced to the UPQC at the dc link. SEMIKRON inverters are implemented for UPQC, which share a common dc-link. The grid voltages, PV voltage and grid currents are sensed by the calibrated Hall effect transducer. The measured signals are utilized by dSPACE 1103 processor for implementation of the control algorithm for the generation of the switching signals. Proposed JAYA optimization scheme has shown its capability to update the PI controller parameters according to the sensed disturbance, the variations in measured PI controller gains are listed in TABLE II. Variation in sampling time can directly affect the controller performance to achieve desired results. Sampling time considered for the proposed algorithm is 31.4 μs which is selected in accordance with the complexity of the overall algorithm to achieve satisfactory performance. It has been analysed with the proposed controller that upon increasing or decreasing the sampling time, the sys-

TABLE I
EXPERIMENTAL SIMULATION RESULTS, CONVERGENCE TIME (MEAN, STANDARD DEVIATION) FOR VARIOUS CASES

Case	Performance of PV-UPQC Under Various Conditions	With PSO		With TLBO		With Proposed JAYA	
		mean	SD	mean	SD	mean	SD
A	Linear and Nonlinear Load	5.88	1.90	4.02	1.65	1.32	0.36
B	Unbalanced Linear Load	6.52	1.65	3.87	0.92	1.27	0.19
C	Voltage Sag	5.96	1.86	3.43	0.99	1.58	0.21
D	Voltage Swell	6.74	1.72	3.77	1.05	1.31	0.14
E	Unbalance Voltage Sag	5.91	1.7	3.32	1.83	1.69	0.34
F	Irradiance Variation	5.81	1.92	4.04	1.61	1.34	0.38

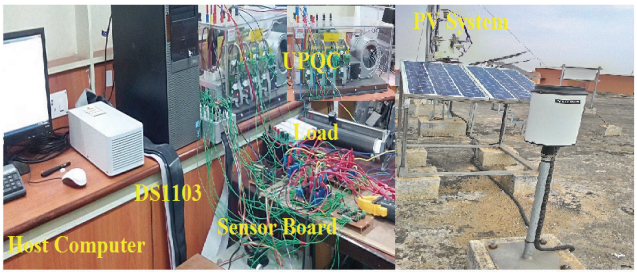


Fig.5. Hardware Prototype developed for PV-UPQC.

TABLE II
VARIATION OF PI CONTROLLER GAINS WITH PROPOSED JAYA ALGORITHM

Type of Disturbances	Kp	Ki
Voltage swell	2.3	0.85
Voltage sag	1.8	2.1
Current harmonics	2	1.3
Linear and nonlinear	3.7	1.2
Unbalanced linear load	1.5	0.8

tem has performed in an average manner and results obtained are worst than with selected sampling time.

A. Performance of PV-UPQC Under Linear and Nonlinear Load Conditions

In the PV connected mode to the grid through UPQC under linear and nonlinear load conditions, controllers are implemented for developed prototype and experimental results are analyzed in this section. The measured nonlinear load currents rich in harmonics are presented in Fig. 6(a). For the elimination of the harmonics, PV-UPQC is employed and current waveforms at the PCC side based on implemented controllers are depicted in Fig. 6(b) to Fig. 6(e). Despite of controllers implemented, performance of the system varies with PI gains. Fig. 6(b) shows the PCC side currents with UV-PI controller with fixed value of PI gains without any optimization (Scenario I). PCC side currents with PSO algorithm (Scenario II), TLBO algorithm (Scenario III) after compensation of harmonics are shown in Fig. 6(c) and Fig. 6(d) respectively. The PV-UPQC with proposed JAYA based auto tuning PI controller (Scenario IV) eliminates the harmonics and maintains nearly sinusoidal current at PCC is shown in Fig. 6(e). The total harmonic distortion of load and PCC currents of the present case is presented in TABLE IV.

TABLE III
EXPERIMENTAL PARAMETERS FOR PROTOTYPE DEVELOPMENT

Selected Parameters	Value
Grid voltage	110 V
Fundamental frequency	50 Hz
Source inductance	0.4 mH
DC bus capacitor, dc bus voltage	3.5 mF, 200 V
Series inverter coupling inductance	0.5 mH
Ripple filter at series inverter	20 μF,10 Ω
Shunt inverter coupling inductance	3.5 mH
Non linear load	100 Ω/40 mH
Unbalanced load	50 Ω/30 mH,100 Ω/40 mH,80 Ω/50 mH
Switching frequency	10 kHz
Sampling time	31.4 μs
Parameters of PV array	
Maximum power of PV(Ppv)	600 W
Open-circuit voltage (Voc)	250 V
Short circuit current (Isc)	4.5 A
Voltage at maximum power (Vmpp)	150 V
Current at Maximum power (Impp)	4.1 A

TABLE IV
PERFORMANCE ANALYSIS OF PSO,TLBO, PROPOSED JAYA FOR PV-UPQC

Parameters		With PSO	With TLBO	With Proposed JAYA
Dependancy on algorithm specific parameters		Highly dependent	Independent	Independent
Algorithemic phases		>2	2	1
THD in %		4.2	3.1	1.4
Settling time after switch on		1	0.5	0.5
Switching harmonics		Very High	High	Low
Reference tracking under load unbalance condition		Avarage	Good	Exact
Reference tracking under voltage sag		Avarage	Good	Exact
Reference tracking under voltage swell		Avarage	Good	Exact
Dynamic response		Poor	Avarage	Better
Convergence time	Mean	Comparatively high	Avarage	Reduced
	Standard Deviation	Comparatively high	Avarage	Reduced

B. Performance of PV-UPQC Under Unbalanced Linear Load Conditions

Fig. 7(a) presents experimental results of load side currents under unbalanced load conditions. The unbalanced load parameters are given in the TABLE III. As UPQC is installed in the grid with proposed controller, sensed currents at the PCC side are balanced and sinusoidal. The source currents after compensation without optimization are presented in Fig. 7(b). Experimental results of source currents with PSO algorithm, TLBO algorithm and JAYA based auto tuning PI controller are given in Fig. 7(c), Fig. 7(d), and Fig. 7(e) respectively.

C. Performance of PV-UPQC Under Voltage Sag Condition

Fig. 8(a) shows the PCC side voltage during voltage sag condition and Fig. 8(b) present the load side voltage after compensation of voltage sag by PV-UPQC for phase a. During the

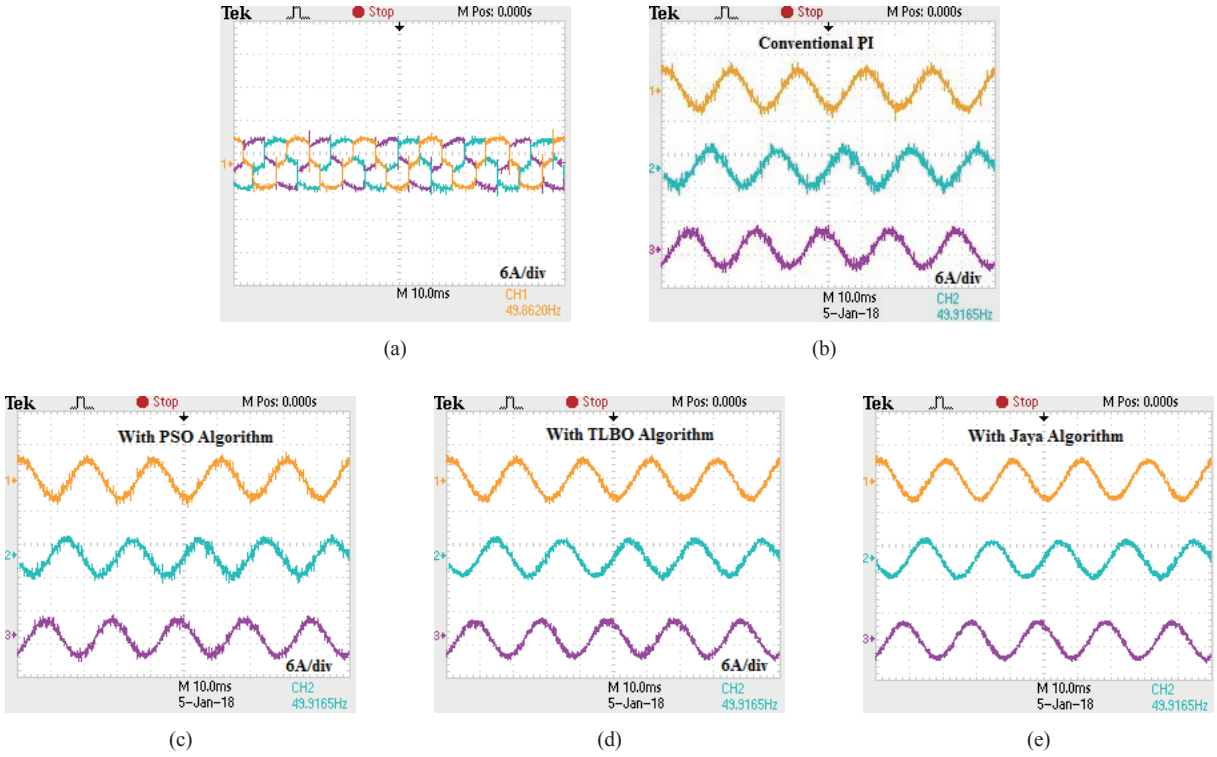


Fig. 6. Performance of PV-UPQC under linear and nonlinear load condition: (a) Load side current, PCC side current after compensation; (b) with conventional PI controller (without optimization); (c) with PSO algorithm; (d)with TLBO algorithm; (e) with JAYA based auto tuning PI controller.

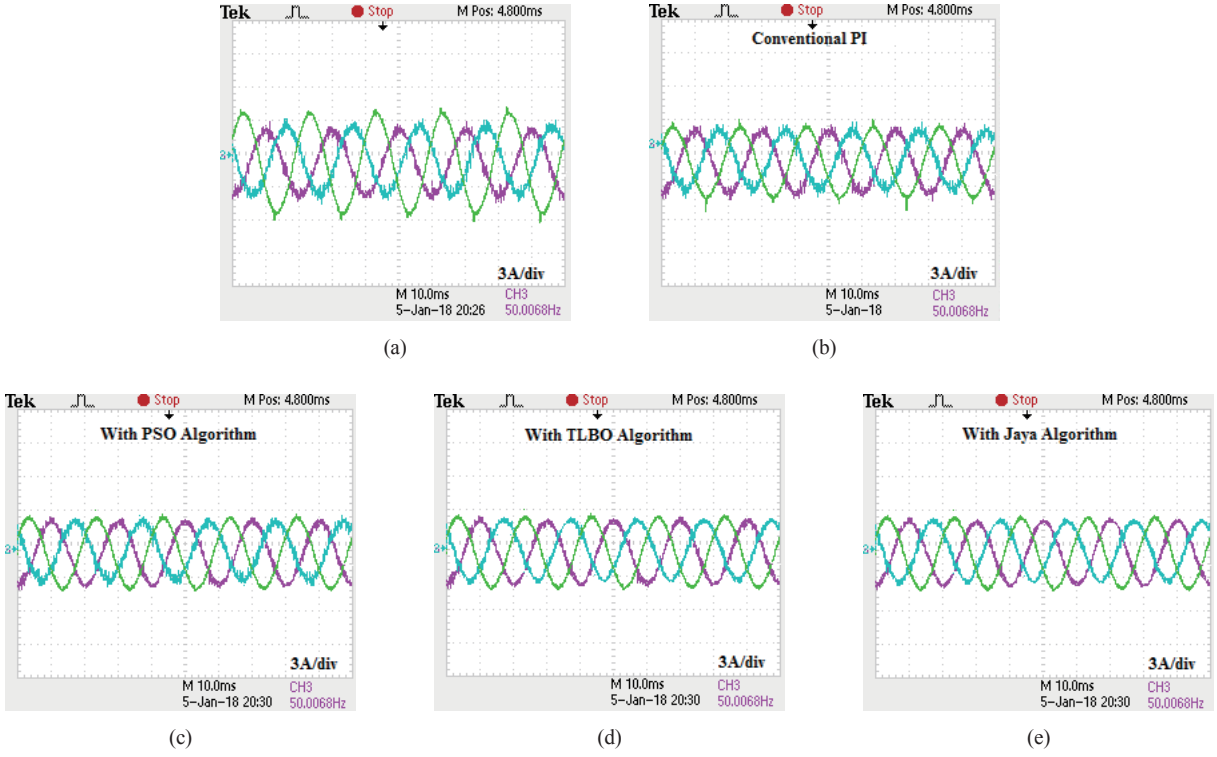
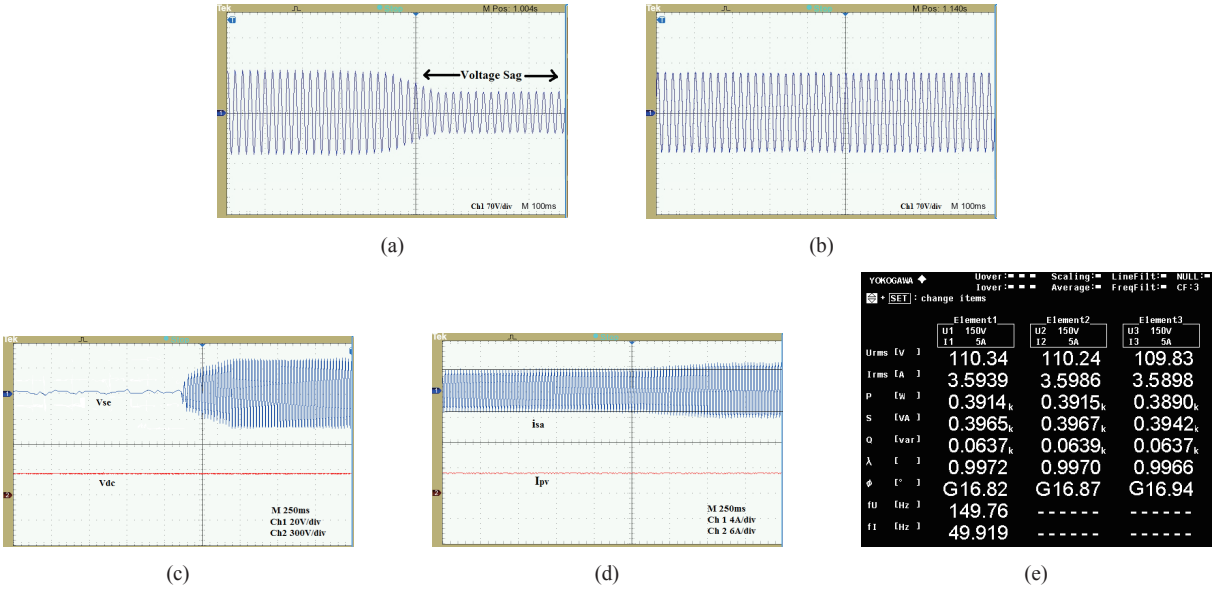
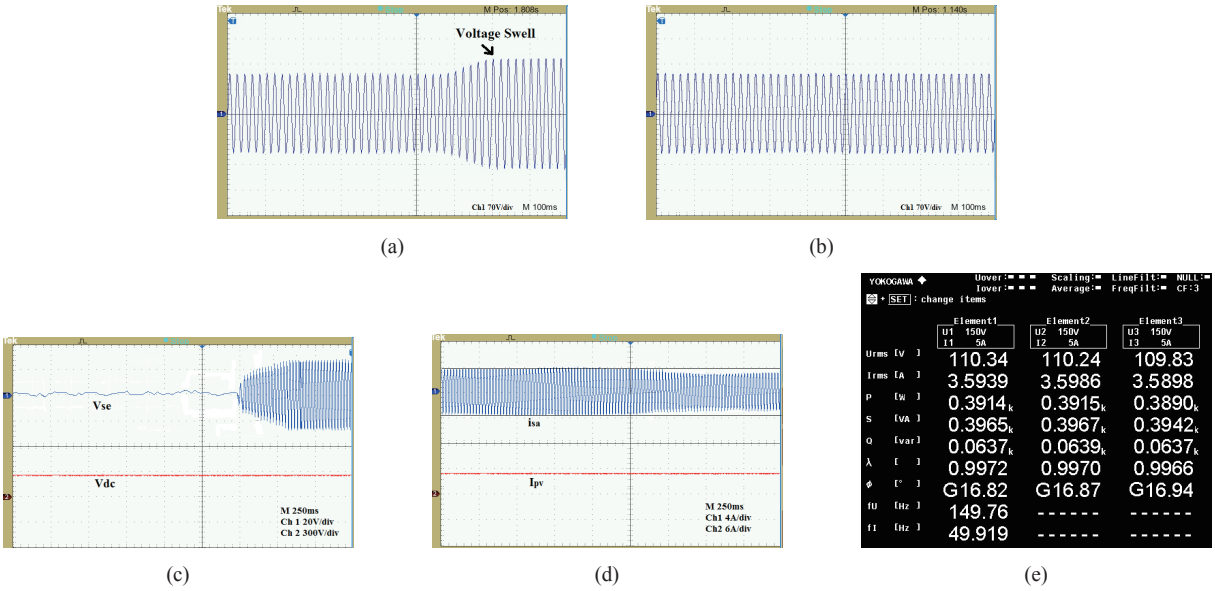


Fig. 7. Performance of PV-UPQC under unbalanced linear load condition: (a) Load side current, PCC side current after compensation; (b) with conventional PI controller (without optimization); (c) with PSO algorithm; (d) with TLBO algorithm; (e) with JAYA based auto tuning PI controller.



(a) (b) (c) (d) (e)

Fig. 8. Performance of PV-UPQC under voltage sag condition: (a) PCC side voltage with sag; (b) Load side voltage after sag compensation with JAYA based auto tuning PI controller; (c) Injecting voltage from series APF and dc-link voltage; (d) PCC current during voltage sag and PV current at constant irradiation; (e) Load side power analyzer three phase voltage and current.



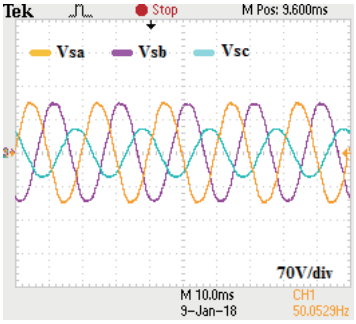
(a) (b) (c) (d) (e)

Fig. 9. Performance of PV-UPQC under voltage swell condition: (a) PCC side voltage with swell; (b) Load side voltage after swell compensation with JAYA based auto tuning PI controller; (c) Injecting voltage from series APF and dc-link voltage; (d) PCC current during voltage swell and PV current at constant irradiation; (e) Load side power analyzer three phase voltage and current.

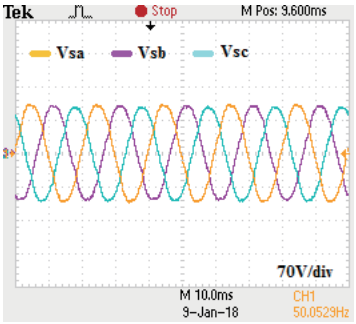
voltage sag, the series inverter voltage injected and the regulated DC-Link voltage is presented in Fig. 8(c). To maintain the power balance at the load, there is increase in grid current as presented in Fig. 8(d). The load side voltages are measured by three phase power analyzer (YOKOGAWA WT500) as shown in Fig. 8(e). From the power analyzer, measured signals are analyzed and it is seen that λ is at near to unity power factor.

D. Performance of PV-UPQC Under Voltage Swell Condition

Voltage swells occurs due to PCC voltage rises to 130 V as shown in Fig. 9(a). The series converter of PV-UPQC injects compensating signal to PCC to regulate the load voltage at 110 V as presented in Fig. 9(b) with the proposed JAYA based controller. The series inverter injecting voltage for load voltage regulation is given in Fig. 9(c), which also shows the constant DC-link voltage. During voltage swell condition, there is decrease in grid current to maintain power balance in the system as shown in Fig. 9(d). The results obtained from the experimentation prove the efficiency of proposed JAYA based auto tuned PI controller for the controller of PV-UPQC. Fig. 9(e) shows the power analyzer signals for regulation of the load voltages.

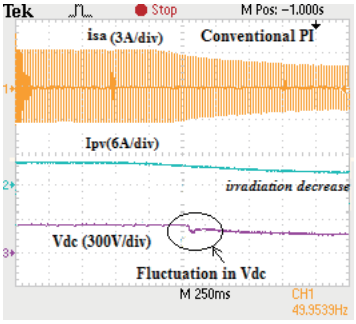


(a)

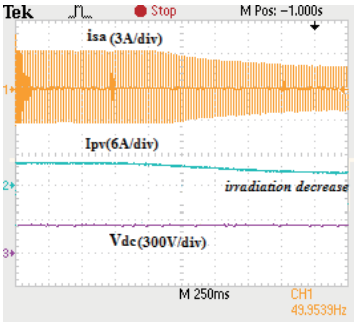


(b)

Fig. 10. Performance of PV-UPQC under unbalanced voltage sag condition: (a) PCC side voltage with unbalanced phase C; (b) Load side voltage after swell compensation with JAYA based auto tuning PI controller.



(a)



(b)

Fig. 11. PV-UPQC performance under irradiation variations: (a) Irradiation decrease from at 1000 W/m^2 to 500 W/m^2 (conventional PI method); (b) Irradiation decrease from 1000 W/m^2 to 500 W/m^2 (proposed JAYA based PI tuning method) .

E. Performance of PV-UPQC Under Unbalance Voltage Sag Condition

Unbalance voltage sag is a practical scenario taken into consideration in this section to analyze the results of PV-UPQC performance. There is a voltage dip in V_{sc} (Phase C) which is presented in Fig. 10(a). The load voltage is maintained by PV-UPQC based on JAYA based auto tuning PI controller as shown in Fig. 10(b). PV-UPQC with proposed method has shown its performance by maintaining the load voltage at desired level.

F. Behaviour of PV-UPQC Under Irradiation Variation

From the Fig. 11(a), it is clearly revealed that decrease in irradiation condition from 1000 W/m^2 to 500 W/m^2 helps in decrease in the grid current. By the utilization of conventional PI in Fig. 11(a) under decrease in irradiation condition, fluctuation in DC-Link voltage appears. However, the dc-bus voltage is maintained at the desired level, proves the effectiveness of the proposed controller and performance of the PV-UPQC system as presented in Fig. 11(b).

The analytical comparison of adopted optimization methodologies PSO, TLBO and proposed JAYA based algorithm for PV-UPQC topology is presented in nutshell in TABLE IV.

VI. Conclusion

The dynamic performance of proposed JAYA based auto tuned PI controller for PV-UPQC system has been analyzed in detail in this present study. An online JAYA optimization methodology is implemented for PV-UPQC to determine the best value of PI controller gains. UV-PI and PR-R controllers of shunt and series converters, based on JAYA optimization technique have enhanced the PV-UPQC performance. The performance and efficiency of the considered method is studied in multiple operational scenarios of the grid and the responses are compared with PSO, TLBO optimization methods. In the verge of increasing efficiency of the system PV-UPQV, an LCL filter is employed at the output of shunt converter to handle the undesired harmonics of PWM switching of converter. The experimental results verify the effectiveness of the proposed novel control method and prove that JAYA based auto tuned PI controller has significantly raised the PV-UPQC performance by reducing the convergence time, settling time, switching harmonics, complexity and effective dynamic response.

References

[1] H. Fujita and H. Akagi, "The unified power quality conditioner: The integration of shunt and series filters," *IEEE Trans on Power Electron,* vol. 13, no. 2, pp. 315-322. Mar.1998.

[2] S. K. Dash and P. K. Ray, "Platform specific FPGA based hybrid active power filter for power quality enhancement," *Int. J. of Emerging Electric Power Sys.* vol. 18, no. 1, Feb. 2017.

[3] K. A. Chandra, A.O. Barry, and T.D. Nguyen, "Power quality enhancement utilizing single-phase unified power quality conditioner: digital signal processor-based experimental validation," *IET Power Electron.* vol. 4, no.3, pp. 323–331, 2011.

[4] N. D. Tuyen and G. Fujita "PV-active power filter combination supplies power to nonlinear load and compensates utility current," *IEEE*

Power and Energy Technology Systems Journal, vol. 2, no. 1, pp. 32-42, March 2015.

[5] S. Devassy and B. Shing "Modified p-q theory based control of solar PV integrated UPQC-S," in Proc. *IEEE Industry Application Society Annual Meeting*, Oct. 2016, pp.1-8.

[6] S. K. Dash, P. K. Ray, S. Mishra, and G. H. Beng, "UPQC-PV solving power quality issues based on system generator FPGA controller," *in Proc. IEEE ICPEICES*, July 2016, pp.1-6.

[7] M. Kesler and E. Ozdemir, "Syncronous reference frame based control method for UPQC under unbalanced and distorted load conditions," *IEEE Trans. On Inds. Electronics.* vol. 58, no. 9, pp. 3967-3975, Sep. 2011.

[8] Y. Pal, A Swarup, and B. Shing, "Performance of UPQC for power quality improvement" in *Proc. IEEE PEDES* . Dec. 2010, pp.1-7.

[9] Q. N. Trinh and H. H. Lee, "Improvement of unified power quality conditioner performance with enhanced resonant control strategy," *IET Generation, Trans. and Distr.* vol.8, no.12, pp. 2114-2123, 2014.

[10] B. Subudhi, P. K. Ray, and A. M. Panda, " Parameter estimation technique applied to power networks," in *Proc. IEEE TENCON*, Nov. 2008, pp. 1-5.

[11] S. Mishra and P. K. Ray, "Power quality improvement using photovoltaic fed DSTATCOM based on JAYA Optimization" *IEEE Trans. on Sustainable Energy*, vol. 7, no. 4, pp.1672-1680, Oct. 2016.

[12] P. Gong, Z. Lu, Z. Li, and D. Wang, "PI-PSO algorithm based voltage controller of STATCOM for self excited induction generator," in *Proc. 34th IEEE Chinese Control Conference,* July 2015, pp. 4349-4354.

[13] H. Chao, L. Wang, R. S.Yeung, Z. Zhang, and H. S. Chung, "A prediction model guided Jaya algorithm for the PV system maximum power point tracking," *IEEE Trans. on Sustainable Energy,* vol. 9, no. 1, pp.45-55, Jan. 2018.

[14] S. S. Khorramabadi and A. Bakhshai, "Critic-based self-tuning PI structure for cctive and reactive power control of VSCs in microgrid systems," *IEEE Trans. on Smart Grid*, vol. 6, no. 1, pp. 92-103, Jan. 2015.

[15] P. Rodríguez, R. Teodorescu, I. Candela, A.V. Timbus, M. Liserrel, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *Proc .37th IEEE PESC June* 2006, pp. 1-7.

Santanu Kumar Dash received the B.Tech degree in Electronics from Biju Pattnaik University of Technology Rourkela in 2011 and M.Tech from Sambalpur University, Burla, India in 2013. He is currently working toward the Ph.D. degree with the Department of Electrical Engineering, National Institute of Technology Rourkela, India. His research interest include power quality, grid connected systems, distributed generations and embedded system application for power converter control.

Pravat Kumar Ray received the B.E. degree in Electrical Engineering from Indira Gandhi Institute of Technology Sarang, Odisha, India, in 2000, the M.E. degree in Electrical Engineering from Indian Institute of Engineering Science and Technology, Shibpur, Howrah, India, in 2003, and the Ph.D. degree in Electrical Engineering from National Institute of Technology (NIT) Rourkela, Rourkela, India, in 2011.

He was also a Postdoctoral Fellow at Nanyang Technological University, Singapore during Jan. 2016 to June 2017. He is currently an Associate Professor with the Department of Electrical Engineering, NIT Rourkela. His research interests include system identification, signal processing and soft computing applications to power system, power quality, solar irradiance forecasting using sky images and grid integration of renewable energy systems.

Methodology for Analysis and Design of Discrete Time Current Controllers for Three-Phase PWM Converters

Christoph H. van der Broeck, Sebastian A. Richter, Jochen von Bloh, and Rik W. De Doncker

***Abstract*—In this work, a methodology for the analysis and design of robust, high bandwidth current controllers for three phase converters is presented. The overall goal is to demonstrate how the proposed model based control structure and the design methodology lead to an optimized digital current controller that exhibits fast and smooth dynamics as well as an excellent disturbance rejection ability. First, accurate discrete time models are derived and used to review classical current control from the perspective of the synchronous and stationary reference frame. Then, implementation options for the synchronous frame proportional integral (SFPI) regulator and the proportional resonant (PR) regulator are discussed and systematically compared in the stationary frame leading to the formulation of a general controller framework based on space vector resonators. It embodies multiple complex resonators and can represent the SFPI regulator, the PR regulator and beyond that any higher order regulator structure. For this framework, a step by step design procedure based on the complex root locus is proposed that allows an insightful optimization of its feedback gains. Finally, the performance of the presented control design techniques is evaluated experimentally.**

***Index Terms*—Control design, current control, digital control, PWM converter, root-locus method.**

I. Introduction

THE aim of this work is to provide an insightful framework for the design and efficient implementation of discrete time current control structures for grid-tied three-phase PWM converters. The synchronous-frame PI (SFPI) regulator [1] and the proportional-resonant (PR) regulator [2] are the most common regulators used for three-phase PWM converters, e.g. in active rectifiers or inverters for distributed power generation [3]. In a consistent control structure with proper state feedback decoupling and command feedforward [25], [29] they provide high bandwidth current control with infinite stiffness and zero steady state error at grid frequency.

For PWM converters operating at low switching frequencies accurate discrete time modeling is necessary for high bandwidth control design [24]. Basic discrete time modeling and control techniques for SFPI regulators and PR regulators have been explored in [4], [5]. They offer high accuracy, since they allow analyzing and designing the dynamics of a computer controlled system in its natural domain. For example, the latched characteristics of the voltage pattern generated by a PWM modulated converter and the update delay can be modeled accurately. Based on these models widely explored design tools like state space control [6] or the root locus method [7] can be used to obtain optimized feedback gains. This is not possible working with continuous time models where typically the open loop transfer function is used to design the controller. The optimization of the phase margin and the crossover frequency [8] only guarantee the stability of the closed loop system, but both cannot be directly related to certain closed loop characteristics e.g. damping, bandwidth or stiffness properties.

With the stronger integration of power electronics in the distribution grid, the harmonic content of the grid voltage increases in many grid areas [26], [27]. Without any further measures, neither SFPI nor PR regulators can reject the effect of voltage components of higher order and the emission of higher order current harmonics is the consequence. Thus, for the accurate control of the converter current at fundamental frequency and the rejection of higher order disturbance voltages multiple SFPI/PR regulators are used in [9], [10], [26] and [32] or alternatively repetitive control structures are applied as in [11], [27], [28] and [12].

Especially at a small carrier to fundamental frequency ratio, it is important to design the current control structure strategically in such a way that the fundamental current is smoothly controlled with high bandwidth and higher order voltage harmonics and disturbances are effectively rejected [25], [27]. In the literature most research approaches the control design in the continuous time domain [3], [13], [14], [31], [32]. However, a control design in the discrete time domain allows more realistic insight in the converter operation if the control bandwidth reaches close to the sampling frequency of the system, as illustrated in [5],[29] and [30]. For this reason, this paper aims to present a consistent discrete time modeling and design methodology to optimize the control structure and feedback gains for current controllers in grid tied applications.

This work, which is based on [22], firstly derives an accurate discrete time model for grid tied converters. Based on this model suitable decoupling structures and a trajectory generator are implemented together with a SFPI regulator using classical design methods and assuming ideal decoupling. To compare the SFPI and the PR regulator, the SFPI regulator is first formulated in the stationary frame [13]. It is demonstrated how the

Manuscript received April 17, 2018.

C. H. van der Broeck and R. W. De Doncker are with Institute for Power Electronics and Electrical Drives(ISEA), RWTH Aachen University, Aachen, Germany (e-mail: post@isea.rwth-aachen.de).

S. A. Richter and J. von Bloh are with AixControl GmbH, Aachen, Germany (e-mail: info@aixcontrol.de).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00025

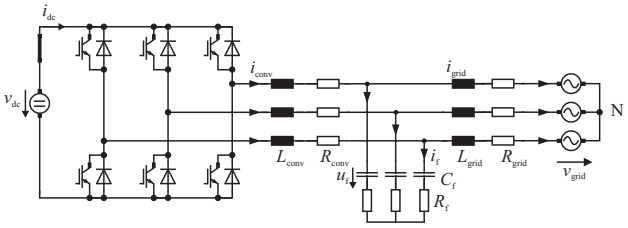


Fig. 1. Three-phase PWM converter with LCL filter.

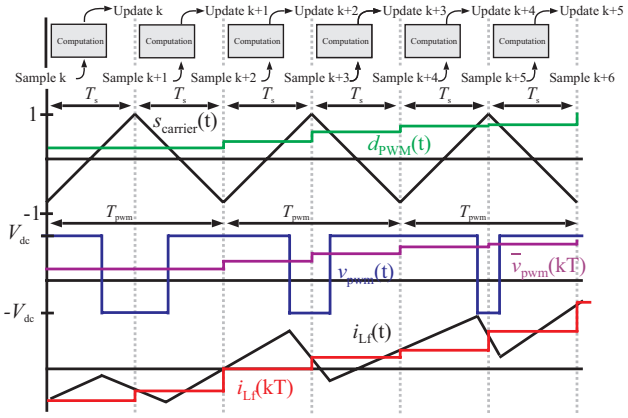


Fig. 2. Pulse width modulation of one converter half-bridge.

root locus method can be generalized for complex single-input single-output (SISO) systems in order to make it an effective design tool for any three phase control design. With this tool, the PR and SFPI regulator are optimized and compared. Finally, it is demonstrated how multiple space vector resonators can be tied together in a regulator structure called "Resonant Space Vector (RSV) regulator". This structure allows an efficient implementation and a consistent design of higher order current regulators. The discussed implementation and design concepts are validated in simulation and experiments.

II. Model Development

In this section, a discrete time model of a PWM converter with LCL filter (Fig. 1) is developed. In a first modeling step, the converter circuitry is replaced by ideal voltage sources, which represent the average voltage applied to the filter (Fig. 3). The control bandwidth of most converters is significantly below the resonance frequency of the LCL filter. Thus, in the frequency range of the control loops the capacitor C_f behaves like an open circuit and can be omitted in the control model (Fig. 4). This model only consists of an inductance $L_f = L_{conv} + L_{grid}$ and a parasitic resistance $R_f = R_{conv} + R_{grid}$, which form a so called L-filter model The neutral point of the converter system is isolated. Thus, the three phase currents and voltages can be transformed to two orthogonal space vector components [3] via the αβ-transform resulting in the simplified equivalent circuit of the three phase converter shown in Fig. 5. The αβ-space vectors can be formulated as complex quantities to reduce the system complexity. Thereby, the converter, which is oritignally a scalar multiple-input multiple-output (MIMO) system is reduced to a complex

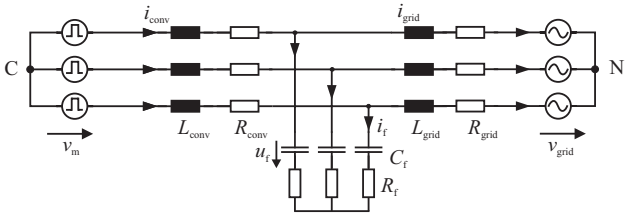


Fig. 3. Simplified model of the converter with LCL filter.

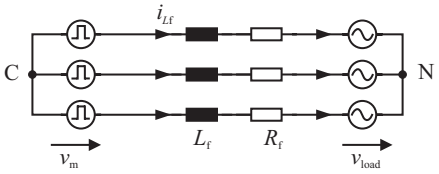


Fig. 4. Control model.

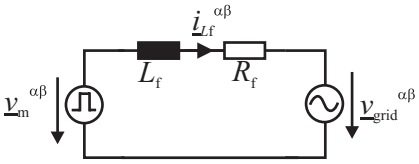


Fig. 5. Model in the αβ frame.

single-input single-output (SISO) system like it is presented in [14] and [15].

Most control analysis and synthesis tools in the Laplace- and z-domain can be adopted for these complex systems as it is illustrated in [16] and [17]. Based on the differential equation of the simplified system

$$L_f \frac{d}{dt} \underline{i}_{Lf}^{\alpha\beta} = \underline{v}_m^{\alpha\beta} - R_f \underline{i}_{Lf}^{\alpha\beta} - \underline{v}_{grid}^{\alpha\beta}, \qquad (1)$$

which describes the dynamics of the current $\underline{i}_{Lf}^{\alpha\beta}$ in the inductance L_f and the resistance R_f as a function of the modulated converter voltage $\underline{v}_m^{\alpha\beta}$ and the grid voltage $\underline{v}_{grid}^{\alpha\beta}$, the transfer function $\underline{G}_{filter}(s)^{\alpha\beta}$ (2) of the L-filter can be determined as a function of the time constant $\tau_f = L_f/R_f$.

$$\underline{G}_{filter}(s)^{\alpha\beta} = \frac{\underline{I}_{Lf}(s)^{\alpha\beta}}{\underline{V}_m(s)^{\alpha\beta} - \underline{V}_{grid}(s)^{\alpha\beta}} = \frac{1}{R_f} \frac{1}{s\tau_f + 1} \qquad (2)$$

For the voltage modulation, a classical asymmetrical regular sampled PWM [18] is used to realize a space vector modulation [20], which allows applying an arbitrary three-phase average voltage to the filter. The voltage modulation process for one half bridge of the converter is depicted in Fig. 2. At the top and bottom of the carrier signal $s_{carrier}$ the duty cycle d_{PWM} is updated and the converter current i_{Lf} is measured and sampled. This synchronous sampling allows capturing the average current. The computer control system can be operated at a sampling frequency of twice the PWM frequency. However, as the duty cycle is only updated twice per PWM interval, there is a constant update delay of $T_{update} = T_s$.

A. Discrete Time Converter Model

The discrete time model of a PWM converter connected to the utility grid is developed based on the state block diagram of the plant depicted in Fig. 6. It takes into account the low bandwidth filter dynamics of the LCL filter (2), the update delay of the controller $\underline{G}_{\text{update}}(z) = z^{-1}$, and the modulator dynamics. The low-pass characteristic of the inductive load ensures that only the average voltage contributes to the average rate of change of the current. Therefore, the applied voltage pulses are approximated as a latch with a zero-order hold model in the stationary frame [5]. The zero-order hold model is applied according to (3) following [23].

$$\underline{G}_{\text{conv}}(z)^{\alpha\beta} = \frac{\underline{I}_{Lf}(z)^{\alpha\beta}}{\underline{V}_{\text{m}}(z)^{\alpha\beta}} = \left(1 - z^{-1}\right) Z\left\{\frac{\underline{G}_{\text{filter}}(s)^{\alpha\beta}}{s}\right\}. \tag{3}$$

For a negligible small resistance, the plant time constant $\tau_f = L_f / R_f$ approaches inifity and the discrete time transfer function can be simplified via (4) using L'Hopital's rule. The same results can also be obtained by directly discretizing the transfer function of an inductance and can be found in [24].

$$\underline{G}_{\text{conv}}(z)^{\alpha\beta} = \frac{1}{R_f}\frac{\left(1 - e^{-T_s/\tau_f}\right) z^{-1}}{1 - e^{-T_s/\tau_f} z^{-1}} \overset{Rf \to 0}{=} \frac{1}{L_f}\frac{z^{-1}}{1 - z^{-1}} \lim_{\tau f \to \infty} \left\{\left(1 - e^{-T_s/\tau_f}\right)\tau_f\right\}$$

$$\underline{G}_{\text{conv}}(z)^{\alpha\beta} = \frac{1}{L_f}\frac{T_s z^{-1}}{1 - z^{-1}} \tag{4}$$

The discrete time model of the plant is completed by adding the update delay $\underline{G}_{\text{update}}(z)$, which takes into account the delay between the sampling of the currents and voltages and the update of the PWM duty cycle.

$$\underline{G}_{\text{p}}(z)^{\alpha\beta} = \frac{\underline{I}_{Lf}(z)^{\alpha\beta}}{\underline{V}_{\text{m}}^{*}(z)^{\alpha\beta}} = \frac{1}{L_f}\frac{T_s z^{-1}}{1 - z^{-1}} z^{-1}. \tag{5}$$

For most common control designs, the plant is transformed into the synchronous reference frame, which rotates with the grid frequency ω_e, to design a PI regulator for dc-quantities. This model transformation can be done by back shifting of the coordinate transformation (6) and applying the z-transformation on the backshifted difference (7) resulting in (8).

$$\underline{x}^{\alpha\beta}(k) = \underline{x}^{\text{dq}}(k)\, e^{j\omega_e k T_s} \tag{6}$$

$$\underline{x}^{\alpha\beta}(k-1) = \underline{x}^{\text{dq}}(k-1)\, e^{j\omega_e k T_s}\, e^{-j\omega_e T_s}. \tag{7}$$

$$\underline{X}^{\alpha\beta}(z)\, z^{-1} = \underline{X}^{\text{dq}}(z)\, z^{-1} e^{-j\omega_e T_s} \tag{8}$$

Consequently, a discrete time transfer function can be transferred from the stationary to the synchronous reference frame, which rotates at an angular frequency of ω_e, by replacing all z^{-1} with $z^{-1} e^{-j\omega_e T_s}$. The transfer function of the system in the synchronous frame (9), which is derived following this procedure, exhibits complex coefficients due to the crosscoupling between d- and q-component which results from the reference frame transformation.

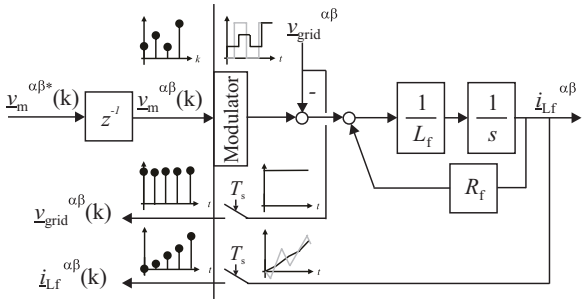


Fig. 6. State block diagram of the converter connected to the grid.

$$\underline{G}_{\text{conv}}(z)^{\text{dq}} = \frac{1}{L_f}\frac{T_s e^{-j\omega_e T_s} z^{-1}}{1 - e^{-j\omega_e T_s} z^{-1}} z^{-1} e^{-j\omega_e T_s}. \tag{9}$$

B. Discrete Time Grid Voltage Model

Another part of the converter model that needs to be derived is the discrete time system response to the grid voltage. It describes the impact of the sampled grid voltage $\underline{v}_{\text{grid}}(k)$ on the sampled current $\underline{i}_{\text{Lf}}(k)$. The discrete time grid voltage model cannot be developed from the stationary frame inductor model (5), because this does not accurately model the sinusoidal characteristics of the grid voltage. Instead the grid voltage applied to the L-filter

$$\underline{G}_{\text{grid}}(s)^{\text{dq}} = \frac{\underline{I}_{Lf}(s)^{\text{dq}}}{\underline{V}_{\text{grid}}(s)^{\text{dq}}} \overset{Rf \to 0}{=} \frac{1}{sL_f + j\omega_e L_f} \tag{10}$$

can be latched in the dq-frame (11). This corresponds to a perfect construction of a sinusoidal voltage in the stationary frame.

$$\underline{G}_{\text{grid}}(z)^{\text{dq}} = \frac{\underline{I}_{Lf}(z)^{\text{dq}}}{\underline{V}_{\text{grid}}(z)^{\text{dq}}} = \left(1 - z^{-1}\right) Z\left\{\frac{\underline{G}_{\text{grid}}(s)^{\text{dq}}}{s}\right\} \tag{11}$$

$$\underline{G}_{\text{grid}}(z)^{\text{dq}} = \text{sinc}\left(\frac{\omega_e T_s}{2}\right)\frac{T_s e^{-j\omega_e T_s/2} z^{-1}}{1 - e^{-j\omega_e T_s} z^{-1}} \tag{12}$$

The resulting transfer function (12) can be simplified, as the sinc-function is approximately 1 for the cases of interest

$$\underline{G}_{\text{grid}}(z)^{\text{dq}} = \frac{\underline{I}_{Lf}(z)^{\text{dq}}}{\underline{V}_{\text{grid}}(z)^{\text{dq}}} \approx \frac{1}{L_f}\frac{T_s e^{-j\omega_e T_s/2} z^{-1}}{1 - e^{-j\omega_e T_s} z^{-1}}. \tag{13}$$

Comparing the converter and grid voltage model (9) and (13), it is important to realize that the sampled grid voltage and the converter voltage exhibit a different rotation in steady state.

The knowledge about the discrete time dynamics of the system can be assembled to a discrete time converter model as depicted in the grey box in Fig. 7.

III. Current Control Implementation in the DQ-Frame

The developed model is the basis for the current control implementation, which is discussed in the following section. It is discussed in many publications, e.g. in [3] and [8], that it is important to make the dynamics of the d- and q-current unaffected

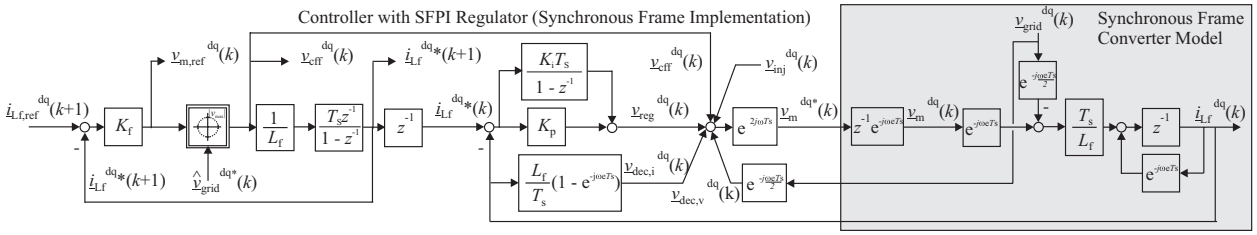


Fig. 7. State block diagram of the discrete time current control structure with command filter in the synchronous frame.

from each other. The elimination of crosscoupling allows to reduce oscillations and increases the bandwidth and stiffness of the control system. However, this decoupling is typically done based on continuous time models, and does not take into account the discrete nature of the control algorithm. To overcome this limitation in the following section accurate discrete time decoupling measures are discussed, their performance is analyzed with a standard control design and the command tracking is improved with a command trajectory filter and a feedforward path.

A. State Feedback Decoupling Structure

The required decoupling structure can be developed based on the system model. If no additional predictor or observer structure is applied, due to the update delay introduced in (5), the decoupling can only be done quasi stationary, which was discussed in [21]. The forward decoupling path

$$\underline{v}_{\mathrm{m}}^{*\mathrm{dq}}(k) = \mathrm{e}^{2\mathrm{j}\omega_{\mathrm{e}}T_{\mathrm{s}}}\,\underline{v}_{\mathrm{m,dec}}^{\mathrm{dq}}(k) \tag{14}$$

compensates for the phase shift of the delays, whereas the feedback $\underline{v}_{\mathrm{dec,iLf}}^{\mathrm{dq}}$ decoupling compensates the current crosscoupling, while a minor error causes by the update delay remains.

$$\underline{v}_{\mathrm{dec,i}}^{\mathrm{dq}}(k) = L_{\mathrm{f}}/T_{\mathrm{s}}(1 - \mathrm{e}^{-\mathrm{j}\omega_{\mathrm{e}}T_{\mathrm{s}}})\ \underline{i}_{\mathrm{Lf}}^{\mathrm{dq}}(k) \tag{15}$$

The grid voltage is decoupled in steady state with phase compensation according to (16)

$$\underline{v}_{\mathrm{dec,v}}^{\mathrm{dq}}(k) = \mathrm{e}^{-\mathrm{j}0.5\omega_{\mathrm{e}}T_{\mathrm{s}}}\,\underline{v}_{\mathrm{grid}}^{\mathrm{dq}}(k), \tag{16}$$

taking into account the combined grid voltage converter model. The entire state feedback decoupling structure is depicted in the state block diagram of the controlled plant in Fig. 7 together with the SFPI regulator.

B. Classical SFPI Regulator Design and Performance Analysis

After the decoupling, the control design of K_{p} and K_{i} can be pursued in the dq-frame e.g. based on the phase margin [8], the root-locus method [5] or the technical or symmetrical optimum (SO) [19]. As the focus of this section is set on the control structure, the feedback gains are designed with the symmetrical optimum, which is a very common control design method. For this design the converter dynamics are assumed to be ideally

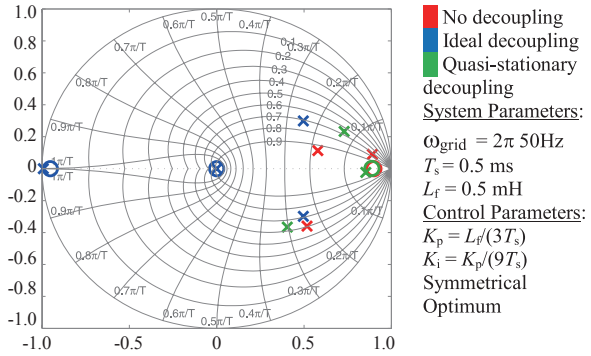


Fig. 8. SFPI control design with the symmetrical optimum ($a = 2$).

decoupled and approximated by a 1st order lag element with the time constant $T_{\mathrm{d}} = T_{\mathrm{update}} + T_{\mathrm{latch}} = 1.5\ T_{\mathrm{s}}$, which results from the update delay and the characteristics of the modulator that is moded as a latch with $T_{\mathrm{latch}} = 0.5\ T_{\mathrm{s}}$. The open loop transfer function

$$\underline{G}_0(s) = \underline{G}_{\mathrm{c}}(s)\,\underline{G}_{\mathrm{p}}(s) = \frac{1}{sT_{\mathrm{d}}+1}\,\frac{1}{s\,L_{\mathrm{f}}}\left(K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s}\right) \tag{17}$$

for $R_{\mathrm{f}} = 0$ is used for the control design. The symmetrical optimum design for the continuous time model leads to the following SFPI regulator gains:

$$K_{\mathrm{p}} = \frac{1}{a}\,\frac{L_{\mathrm{f}}}{T_{\mathrm{d}}}\ ;\ K_{\mathrm{i}} = K_{\mathrm{p}}\frac{1}{a^2}\,\frac{1}{T_{\mathrm{d}}} \tag{18}$$

The gains obtained from this quasi continuous control design are used as feedback gains for the discrete time control structure depicted in Fig. 7. Typically, these gains are computed for $a = 2$ as this optimizes the disturbance rejection ability and the robustness of the simplified closed loop system. In Fig. 8 the closed loop poles and zeros for this particular control design are shown for 3 scenarios: The plant without any decoupling measures between d- and q-axis, the ideally decoupled plant (18), which does not exhibit cross coupling between d- and q-quantities, and the quasi-stationary decoupled plant as it is depicted in Fig. 7.

For the ideally decoupled plant, which is purely a reference scenario for the control design and not a realizable scenario, complex conjugated poles with a damping of $\xi = 1/\sqrt{2}$ are realized. This placement is desirable, as the so called optimal damping of $\xi = 1/\sqrt{2}$ provides the strongest disturbance rejection possible without overshoot, which can be observed in Fig. 9. If only a PI regulator in the synchronous reference frame is used and

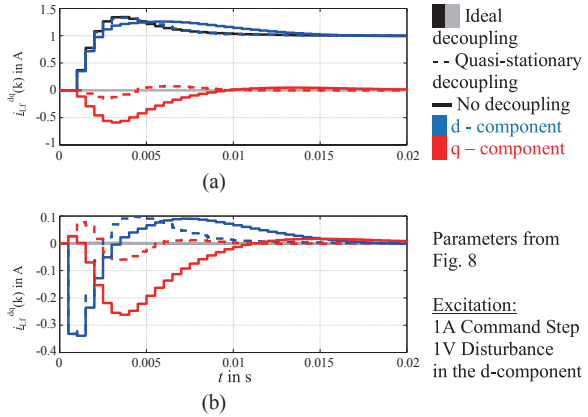


Fig. 9. Command response (a) and disturbance response (b).

no decoupling measures are applied, the dominating pole pair is significantly shifted and rotated. In addition, both poles are not complex conjugated anymore. This phenomenon of complex poles without conjugated counterparts occurs as a consequence of the complex SISO system with significant crosscoupling between d- and q-axis. This crosscoupling between d- and q-current and voltages can be observed from the disturbance step response of the system in Fig. 9. If the quasi stationary decoupling structure proposed on Fig. 7 is applied, the poles in Fig. 8 slightly move back towards their ideal complex conjugated placement. As a result, the excitation of the current in the q-axis is significantly reduced and also the d-axis current settles much faster. A similar effect can be observed looking at the command response of the regulator in Fig. 9.

This investigation shows that the proposed decoupling structures significantly improves the system dynamics, but cannot entirely eliminate the crosscoupling between d- and q-axis. To optimize the PI regulator feedback gains, in the next section it is shown dynamics of the cross coupled system can be taken into account in the regulator design, which is not possible following the symmetrical optimum design rule.

C. Trajectory Generation and Command Feedforward

Before the focus is set to the more accurate design of the regulator, for the improvement of the command tracking performance a consistent command trajectory filter is added to the control, which is depicted in Fig. 7. It consists of a model of the physical system, in this case an inductor, with a feedback path. The feedback gain K_f is selected to adjust the bandwidth of the generated current reference and command feedforward voltage. The command trajectory is constraint to the available voltage margin to ensure that any voltage command from the controller remains within the system limits, i.e. $|\underline{v}_m^{dq}| < V_{dc}/\sqrt{3}$. Consequently, the resulting current reference is always feasible. In addition, a voltage command $\underline{v}_{cff}^{dq}$ is generated, which is directly passed as a feedforward to the voltage modulator. Note that it is very important to delay the current reference by one sampling step, as shown in Fig. 7, to ensure that the applied command feedforward voltage $\underline{v}_{cff}^{dq}$ leads to the desired current at the exact time instant when the corresponding current reference is applied.

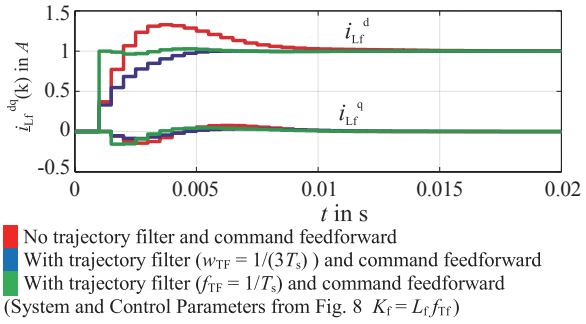


Fig. 10. Command tracking with different command filter bandwidths.

As a result of the command filter and the feedforward path, the control error stays zero during command tracking transients. Consequently, the controller just needs to compensate disturbances and model inaccuracies and it can be designed for disturbance rejection only. The command tracking bandwidth can be set with the gain of the command trajectory filter independent of the controller. In Fig. 10 the command response with and without command filter and command feedforward are compared. It can be seen that these measures eliminate the overshoot during transients and allow to achieve deadbeat command tracking within 2 time steps.

IV. Discrete Time Regulator Design

In this section, the efficient implementation of synchronous-frame proportional integral (SFPI) regulators, proportional-resonant (PR) regulators and higher order current regulators is discussed. It is illustrated how to optimize the design of these control structures. After an optimization, the PR and SFPI regulator are compared to outline advantages and disadvantages of both for different application areas.

A. Implementation Options for Current Regulators

The SFPI regulator (19) is usually designed and implemented in the synchronous reference frame

$$\underline{G}_{SFPI}(z)^{dq} = K_p + \frac{K_i T_s}{1 - z^{-1}} = K_p \left(1 + \frac{K_i T_s}{K_p} \frac{1}{1 - z^{-1}}\right). \quad (19)$$

However, the design and the implementation of the regulator can be done in any other reference frame achieving identical system dynamics: For example, in [13], the continuous time domain SFPI regulator has been implemented in the stationary reference frame. This can also be done for the discrete time control structure, presented in Fig. 7 using the discrete time coordinate transformation given by (8). The entire control structure from Fig. 7 implemented in the stationary frame is shown in Fig. 8. For the SFPI regulator the transformation leads to

$$\underline{G}_{SFPI}(z)^{\alpha\beta} = K_p + \frac{K_i T_s}{1 - e^{j\omega_e T_s} z^{-1}}. \quad (20)$$

This expression exhibits a resonator for space vectors, which

is therefore called space-vector resonator. It results from the integrator which is shifted from the dq- into the αβ-coordinate system and guarantees the control of the current at its resonant frequency with infinite stiffness and zero steady state error due to the internal model principle. It can be efficiently implemented on a DSP similar to a discrete time integrator as complex difference equation using the backshift operator of the z-transform:

$$\begin{aligned} \underline{v}_{\mathrm{SFPI,reg}}{}^{\alpha\beta}(k) &= K_\mathrm{p}\,\Delta\underline{i}_{\mathrm{Lf}}{}^{\alpha\beta}(k) + \underline{v}_{\mathrm{res}}{}^{\alpha\beta}(k) \\ \underline{v}_{\mathrm{res}}{}^{\alpha\beta}(k) &= K_\mathrm{i}\,T_\mathrm{s}\;\;\Delta\underline{i}_{\mathrm{Lf}}{}^{\alpha\beta}(k) + \underline{v}_{\mathrm{res}}{}^{\alpha\beta}(k-1)\,\mathrm{e}^{\mathrm{j}\omega_\mathrm{e}T_\mathrm{s}} \end{aligned} \tag{21}$$

The stationary frame implementation of grid current regulators brings the benefit of a very simple and efficient implementation without any reference frame transformation.

Based on this concept, a PI regulator on the positive sequence and one on the negative sequence of the current can be combined in the stationary frame resulting in the discrete time implementation of the so called proportional-resonant (PR) regulator [2], which ensures the rejection of positive and negative sequence voltage disturbances:

$$\begin{aligned} \underline{G}_{\mathrm{PR}}(z)^{\alpha\beta} &= K_\mathrm{p} + \frac{K_\mathrm{i}{}^{+}T_\mathrm{s}}{1-\mathrm{e}^{\mathrm{j}\omega_\mathrm{e}T_\mathrm{s}}z^{-1}} + \frac{K_\mathrm{i}{}^{-}T_\mathrm{s}}{1-\mathrm{e}^{-\mathrm{j}\omega_\mathrm{e}T_\mathrm{s}}z^{-1}} \\ K_\mathrm{i}{}^{-}=K_\mathrm{i}{}^{+}=K_\mathrm{i} &\;\;\underset{\rightarrow}{} \;\; K_\mathrm{p} + \frac{2K_\mathrm{i}T_\mathrm{s}\left(1-\cos(\omega_\mathrm{e}T_\mathrm{s})\,z^{-1}\right)}{1-2\cos(\omega_\mathrm{e}T_\mathrm{s})z^{-1}+z^{-2}}. \end{aligned} \tag{22}$$

Consequently, an arbitrary number of SFPI regulators can be implemented in the stationary frame as space-vector resonators, which guarantee infinite stiffness and zero steady state error on multiple harmonics e.g. on the dominant -5$^{\mathrm{th}}$, 7$^{\mathrm{th}}$, -11$^{\mathrm{th}}$ and 13$^{\mathrm{th}}$ grid harmonic. This controller framework is referred to as resonant space-vector (RSV) regulator in the following:

$$G_{\mathrm{RSV}}(z)^{\alpha\beta} = \frac{\underline{V}_{\mathrm{reg}}{}^{\mathrm{dq}}(z)}{\underline{\Delta i}_{\mathrm{Lf}}{}^{\mathrm{dq}}(z)} = K_\mathrm{p} + \sum_{\mathrm{n=-k}}^{\mathrm{k}} \frac{K_{\mathrm{i,n}}\,T_\mathrm{s}}{1-z^{-1}\,\mathrm{e}^{\mathrm{jn}\omega_\mathrm{e}T_\mathrm{s}}} \tag{23}$$

For a digital implementation, the difference equations of the RSV regulator can be formulated analogously to (21). To compensate the delay of the update and latch at higher harmonics it is advisable to include a phase shift into the gain of each resonator, which results in (24). This measure enhances damping and stability of the closed loop system.

$$G_{\mathrm{RSV}}(z)^{\alpha\beta} = K_\mathrm{p} + \sum_{\mathrm{n=-k}}^{\mathrm{k}} \frac{K_{\mathrm{i,n}}\,T_\mathrm{s}}{1-z^{-1}\,\mathrm{e}^{\mathrm{jn}\omega_\mathrm{e}T_\mathrm{s}}}\,\mathrm{e}^{\mathrm{j2(n-1)}\omega_\mathrm{e}T_\mathrm{s}} \tag{24}$$

B. Design and Comparison of SFPI and PR regulators

It has been discussed in section III that the regulator design only needs to focus on providing robustness as well as a fast and strong disturbance rejection ability. This requires the feedback regulator design to include the correct model as well as the already discussed quasi stationary decoupling measures. In most publications, a quasi-continuous design of the regulator, which has conveniently been used in section III, is applied. This is usually based on the symmetrical optimum [3] or the phase margin [8]. Unfortunately, this does not allow insight into the design process if a system with certain crosscoupling between d- and q-components is given.

To overcome this limitation, this work proposes the generalization of the root-locus method, which has previously only been used for transfer functions with scalar coefficients, to transfer functions with complex coefficients. Thereby, it is applicable for the discussed design task. In case of the SFPI regulator, a state feedback decoupling according to Fig. 11 is applied. However, if the PR regulator is used, a decoupling is not meaningful, because typically neither negative nor positive sequence should not be preferred. The following regulator design of the three phase PWM converter, modeled as complex SISO system, picks up on the root-locus design metric presented in [7]. To achieve insights into the regulator design options for SFPI (20) and PR regulator (22) in Fig. 12 the root loci of the open loop transfer function (25) is plotted for various gains $r_\tau = K_\mathrm{i}T_\mathrm{s}/K_\mathrm{p}$ of both regulators.

$$\underline{G}_{\mathrm{o}}(z)^{\alpha\beta} = \underline{G}_{\mathrm{plant}}(z)^{\alpha\beta}\,K_\mathrm{p}\left\{\begin{array}{c}\left(1+\frac{K_\mathrm{i}T_\mathrm{s}}{K_\mathrm{p}}\frac{1}{1-\mathrm{e}^{\mathrm{j}\omega_\mathrm{e}T_\mathrm{s}}z^{-1}}\right) \\ \left(1+\frac{K_\mathrm{i}T_\mathrm{s}}{K_\mathrm{p}}\frac{2\left(1-\cos(\omega_\mathrm{e}T_\mathrm{s})\,z^{-1}\right)}{1-2\cos(\omega_\mathrm{e}T_\mathrm{s})z^{-1}+z^{-2}}\right)\end{array}\right. \tag{25}$$

Due to the complex transfer function of plant and regulator the root loci are not complex conjugated with respect to each other. It is the design goal to find a controller with high bandwidth and disturbance rejection ability that does neither causes significant overshoot nor excites resonances. Thus, it is required to

- Maximize the dynamic stiffness $|\underline{V}_{\mathrm{grid}}{}^{\mathrm{dq}}(j\omega)/\underline{I}_{\mathrm{Lf}}{}^{\mathrm{dq}}(j\omega)|$
- Keep the damping in the range of $\xi_{\mathrm{opt}} > 1/\sqrt{2}$.

To optimize the regulator with respect to these design goals for each root locus the open loop gain is maximized via K_p until the damping constraint $\xi_{\mathrm{opt}} > 1/\sqrt{2}$ is hit. The resulting final poles are marked with black crosses in Fig. 12. They all lead to a design of the proportional state feedback gain with $K_\mathrm{p} \approx L_\mathrm{f}/(3T_\mathrm{s})$. For these designs the dynamic stiffness and the disturbance step response are also plotted in Fig. 12. The dynamic stiffness is used to evaluate the disturbance response properties in the frequency domain, as it indicates what disturbance voltage it takes at each frequency to change the current at that frequency by 1 A. To find the optimal regulator, the design scenario with the highest tuning factor that still keeps the damping constraint is selected. Thereby, it is guaranteed that the stiffness around grid frequency is maximized, which is desired to ensure a fast rejection of disturbances at the fundamental frequency and a certain robustness with respect to grid frequency variations. The design shown in red for $r_{\tau,\mathrm{SFPI}} = 0.16$ and $r_{\tau,\mathrm{PR}} = 0.08$ is a design optimum. A bigger r_τ would lead to undesirable lower damping and overshoot. The resulting optimized feedback gains, which are universally applciable for this current control structure, are summarized in TABLE I.

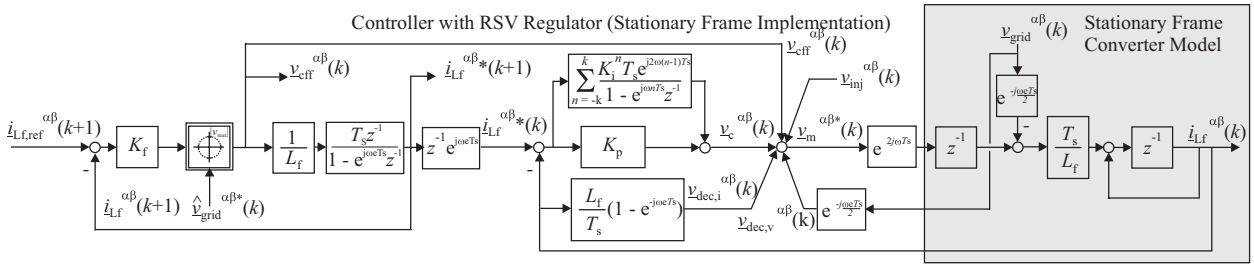


Fig. 11. State block diagram of the discrete time current control structure implemented in the stationary frame.

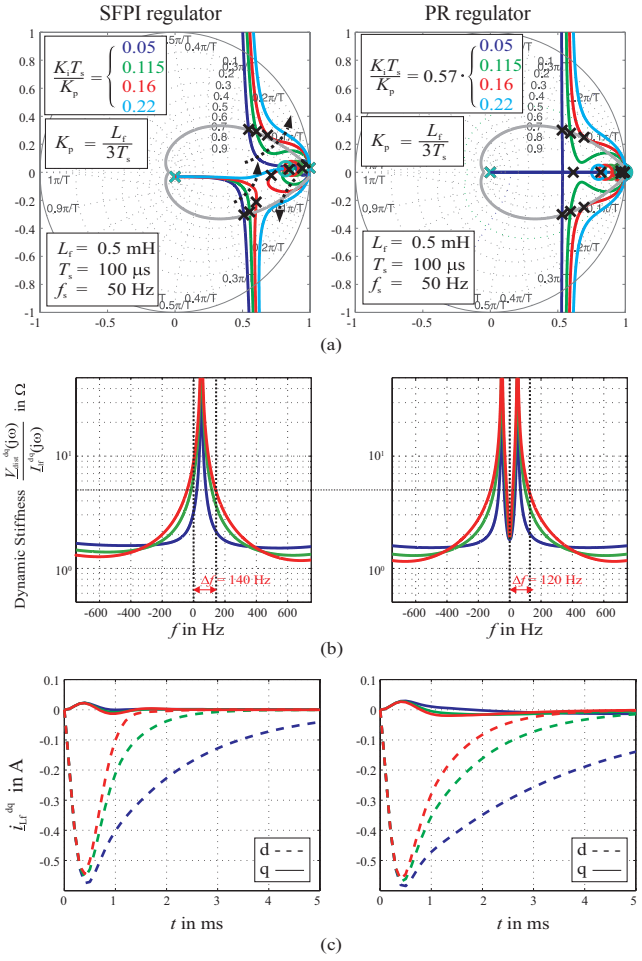


Fig. 12. Control design of the complex SISO system based on (a) Root locus plot of the complex SISO system, (b) double sided dynamic stiffness plot, (c) disturbance response to 1 V step in the d-axis.

An important question to be answered is if there is any benefit from using the PR or the SFPI regulator. From the optimized design it is clear that if no control of the negative component is necessary, the SFPI regulator is always a better choice. The reason for this is that, given similar damping constraints, the SFPI regulator can be built with a higher resonant gain K_i and thus provides as faster settling time after disturbances in the fundamental grid voltage. If both regulators are analyzed over a sampling frequency range from 1 kHz to 20 kHz, which is used in most medium and high power application, the advantage of the SFPI regulator over the PR regulator nearly entirely vanishes at very low sampling frequencies. which has been illustrated in [22] in detail.

TABLE I
OPTIMIZED FEEDBACK GAINS FOR SFPI AND PR REGULATOR

Gains	SFPI Regulator	PR Regulator
K_p	$L_f/(3T_s)$	$L_f/(3T_s)$
$K_i = K_r$	$0.16 \cdot K_p/T_s$	$0.08 \cdot K_p/T_s$

C. Design and Implementation of the RSV Regulator

The introduced RSV regulator is a compact way to formulate a regulator on multiple harmonics. One limitation of higher order regulator structures is that it is not intuitive to design multiple state feedback gains such that the overall system dynamics are stable, provide reasonable bandwidth and are well behaved. To overcome this limitation, it is shown how the root-locus method for complex SISO systems can be used to optimize the state feedback gains of multiple space vector resonators. A properly tuned SFPI regulator is used as a starting point that is augmented by space vector resonators achieving infinite stiffness at the -5th, +7th, -11th and +13th grid harmonic.

The design goal for the entire regulator is to augment the bandwidth of high stiffness around the desired frequencies while keeping the effective damping of the system above a certain level such that resonance do not become dominant. First, the RSV regulator state feedback gains rejecting the -5th and +7th grid voltage harmonic are synthesized. The gain on -5th and +7th harmonic are kept identical ($K_{i,+5} = K_{i,-7} = K_{r,-5,+7}$) to limit the complexity of the design. The root locus in Fig. 13 (left) shows the possible pole placements for an increasing $K_{r,-5,+7}$. For the red and black marked poles two design options are shown in detail, whose dynamic stiffness plot is shown below in comparison to the dynamic stiffness of the pure SFPI regulator used as starting point. The poles resulting from the space vector resonators on the –5th and +7th harmonic, which are close to the stability margin, are balanced by zeros and are not critical for the design as long as they remain stable. The same is true for the critically damped pole on the real axis. However, when increasing the $K_{r,-5,+7}$ gains the poles resulting from the proportional state feedback path are further pulled to weaker damping. Thus, the design decision for $K_{r,6}$ is a compromise between high system damping and a bigger bandwidth of the resonant state feedback

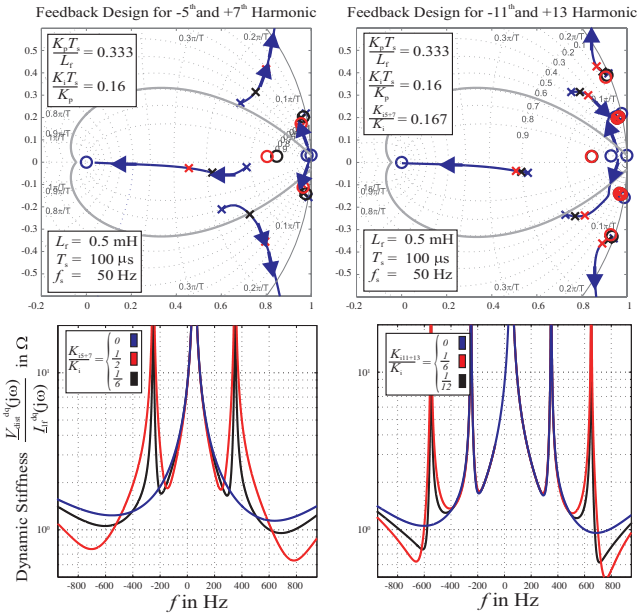


Fig. 13. Design of the RSV regulator with -5th, +7th -11th and 13th harmonic based on the root-locus method.

loop. This is illustrated for two cases: $K_{r,5,6}/K_i = 1/2$ and 1/6. As $K_{r,5,6}/K_i = 1/2$ reduces the damping quiet significantly resulting in a reduction of the worst case stiffness by a factor of 2, a design with $K_{r,6}/K_i = 1/6$ is a reasonable choice.

After the successful resonant state feedback loop design of the –5th and +7th harmonic, the resulting closed loop system dynamics are used as starting point to design the –11th and +13th harmonic resonant feedback loop. The root locus for an increasing ($K_{i,-11} = K_{i,+13} = K_{i,-11,+13}$) depicted in Fig. 13 (right) shows that this time the complex conjugated pole pair corresponding to the proportional state feedback loop is not leading to weak damping. The critically damped pole and also the poles resulting from the space vector resonator on 5th and 7th harmonic do not limit the feedback gain. However, the pole resulting from the additional space vector resonators on the -11th and +13th harmonic reveal a low system damping for higher values of $K_{i,-11,+13}$. This effect is a result from the growing distance and weaker balancing between pole and zero. Thus, a design with $K_{r,-5,+7}/K_i = 1/6$, marked in red, is not desirable as it results in a very weakly damped pole close to the unity circle, whereas state feedback gains of $K_{i,-11,+13}/K_i = 1/12$ seem to be a good design compromise. This exemplary design shows how a RSV regulator structure is designed systematically and consistently generalizing the root locus method for complex SISO system.

V. Simulation and Experimental Results

Based on the introduced control framework a current control structure according to Fig. 11 has been designed and implemented in C++. It was first tested on a Software-in-the-Loop (SiL) test bench using MATLAB Simulink and PLECS. Afterwards, the control classes were implemented on an AixControl XCS2000 rapid control prototyping system to evaluate the control algorithm experimentally.

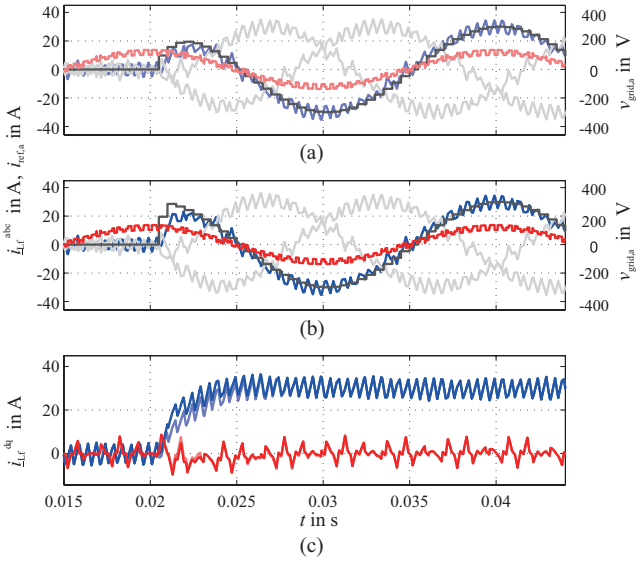


Fig. 14. Simulation of the command response with a trajectory generator gain $K_f = Lf/(3Ts)$ (a) and $K_f = Lf/Ts$.

A. Evaluation of the Command Tracking Performance

First, the performance of the SFPI regulator and the command filter is investigated for the system parameters summarized as Setup I in TABLE II. The simulation in Fig. 14 shows the system command response. The trajectory generator, which includes the voltage limit, shapes a feasible current command and applies a consistent command feedforward leading to a high command tracking bandwidth without overshoot. With the gain of the trajectory generator K_f the bandwidth of the system can be properly adjusted independent of the regulator gains. The simulation results can nearly perfectly be transferred to the experiment, which is shown in Fig. 15. The major difference in current between simulation and experiment occurs due to a small grid voltage imbalance and minor pulsations of the dc-link. This shows that an accurate simulation of a grid tied PWM converter reaches nearly the precision of an experimental setup.

B. Comparison of SFPI and PR Regulator

It has been discussed in Section IV B that the PR regulator gains needs to be detuned compared to the SFPI regulator to keep a desired damping level. As a consequence, the regulator analysis showed that the SFPI regulator can provide a higher stiffness compared to the PR regulator. The PR and the SFPI regulator are designed according to section IV for an experimental demonstration. To keep the damping at $\xi = 0.707$ the resonant feedback gain of the PR regulator needed to be set to approximately ½ of the resonant feedback gain of the SFPI regulator.

To analyze and compare the disturbance rejection performance of both regulators a chopped load resistance is transiently applied in series to the filter of the converter. The parameters of the experimental setup are summarized in TABLE II. (Setup

TABLE II
PARAMETERS OF THE THREE EXPERIMENTAL SETUPS

	L_f	L_{grid} / R_{chop}	f_{pwm}	T_s	V_{dc}	$V_{grid,l\text{-}n}$	K_p	K_i
Setup I	2 mH	0.2 mH	1 kHz	500 µs	300 V	130 *V*	1.33 Ω	K_i = 426 Ω/s
Setup II	0.5 mH	1 Ω	5 kHz	100 µs	250 V	-	1.7 Ω	variable
Setup III	2 mH	0.2 mH	4 kHz	250 µs	420 V	200 *V*	2.6 Ω	1750 Ω/s

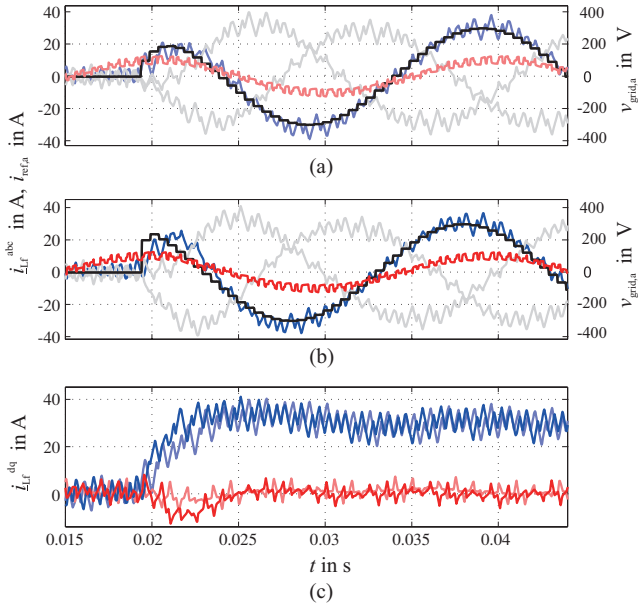


Fig. 15. Measurement results of the command response with a trajectory generator gain $K_f = Lf/(3Ts)$ (a) and $K_f = Lf/Ts$.

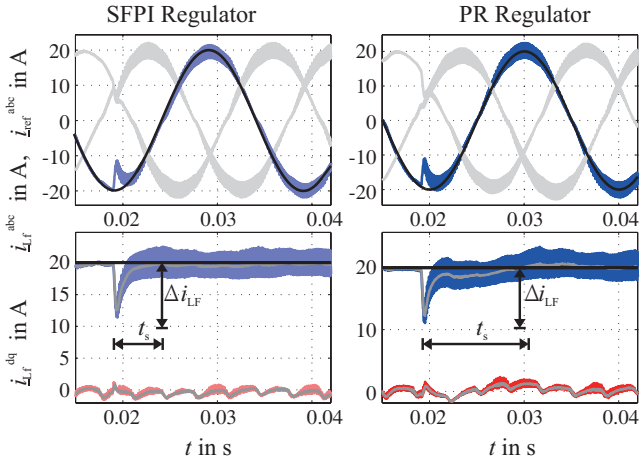


Fig. 16. Measured response of the SFPI (K_i = 2500 Ω/s) and the PR regulator (K_r = 1400 Ω/s) to a chopped resistive load of 1 Ω that is transiently connected in series to the inductance.

II) and the measurement resutls are illustrated in Fig. 16. The current sag Δi_{Lf} that can be observed for both controllers are identical. This is because of the equal proportional feedback gains. However, the PR regulator needs more than twice the settling time t_s compared to the SFPI regulator due to the reduced

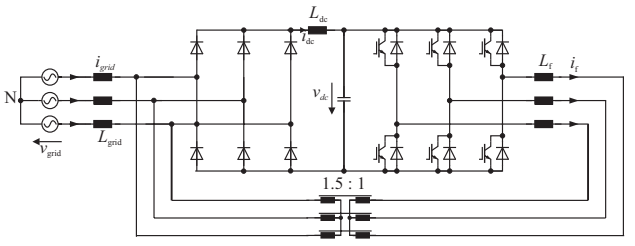


Fig. 17. Experimental setup for performance evaluation of the resonant space vector.

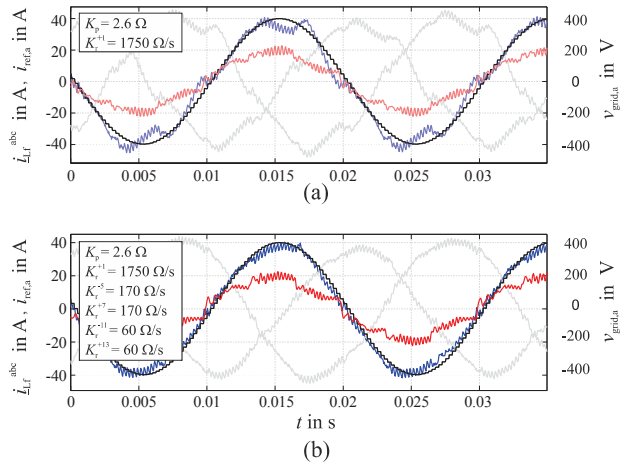


Fig. 18. Experimental comparison of the SFPI regulator only (top) and the resonant space vector regulator structure with state feedback on the 1st, 5th, 7th, 11th and 13th harmonic (down) under distorted grid conditions.

resonant feedback gain. This reveals, that the SFPI regulator is more effective for most current controllers. Only if the rejection of negative sequence voltages is required, e.g. in the case of grid imbalances, the PR regulator is a better choice, as it can entirely reject negative sequence voltage disturbances.

C. Multiple Harmonic Rejection With the RSV Regulator

Finally, the ability of the resonant space vector regulator to reject multiple harmonics is evaluated experimentally. Therefore, the active converter (TABLE II Setup III) is paralleled with a passive three phase rectifier, as illustrated in Fig. 17. This

specific setup allows operating the PWM converter at a grid with artificially excited grid harmonics.

In Fig. 18 the performance of the SFPI regulator structure and the resonant space vector regulator structure are compared under these grid conditions with artificially excited grid harmonics. In case of the SFPI regulator, the grid voltage harmonics excite the current, in particular the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic. This is because the SFPI current regulator exhibits a finite stiffness at these harmonics, which can be seen in Fig. 12. Therefore, it cannot entire reject this disturbance voltage. However, the fundamental harmonic is controlled such that it accurately follows the current reference in amplitude and phase.

In contrast, the space vector regulator structure, which enhances the single space-vector resonator of the SFPI regulator by additional higher order space-vector resonators, rejects the higher order voltage harmonics due to the infinite stiffness at the higher order harmonics. As a consequence, the regulated current is purely sinusoidal and smoothly follows the reference. This elimination of the high order current harmonics is of great importance, especially if multiple converters are operated at a weak utility grid, because it prevents a stronger excitation of the voltage harmonics that is reflected at the coupling point of the converters.

VI. Conclusion

In this work, an insightful design and implementation methodology for discrete-time current control of PWM converters has been proposed and analyzed. Therefore, an accurate discrete-time model for the control of a three-phase converter has been derived. This has been used to develop proper decoupling paths and a consistent command filter structure. The root-locus method has been generalized for the control design of SISO systems with complex coefficeints and used to optimize the SFPI and the PR regulators for three-phase current control. Thereby, both regulator structures have been compared systematically. Based on the SFPI implementation in the stationary frame, the resonant space-vector regulators concept has been developed. It allows to handle various regulators e.g. SFPI, PR and regulators on multiple harmonic in one framework leading to consistent tuning and an efficient implementation. Experimental results are presented to validate the introduced control implementation and design framework.

References

[1] D. Schauder and R. Caddy, "Current control of voltage-sourceinverters for fast four-quadrant drive performance," *IEEE Transactions on Industry Applications*, vol. IA-18, pp. 163-171, Mar./Apr. 1982.

[2] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Transactions on Industry Applications,* vol. 37, no. 2, pp. 601-610, Mar./Apr. 2001.

[3] V. Blasko, V. Kaura, "A new mathematical model and control of a three-phase AC-DC voltage source converter," *IEEE Transactions on Power Electronics,* vol. 12, no. 1, pp. 116-123, Jan. 1997.

[4] S. A. Richter and R. W. De Doncker, "Digital proportional-resonant (PR) control with anti-windup applied to a voltage-source inverter," in *Proc. 14th Eur. Conf. Power Electron*. Appl., 2011, pp. 1-10.

[5] K. Hongrae, M. W. Degner, J. M. Guerrero, F. Briz, and R. D. Lorenz, "Discrete-time current regulator design for AC machine drives," *IEEE Transactions on Industry Applications,* vol. 46, no. 4, pp. 1425-1435, Jul.-Aug. 2010.

[6] S. A. Richter, J. von Bloh, C. P. Dick, D. Hirschmann, and R. W. De Doncker, "Control of a medium-voltage test generator," in *IEEE Power Electronics Specialists Conference 2008*, 2008, pp. 3787-3793.

[7] C. H. van der Broeck, R.W. De Doncker, S. A. Richter, and J. von Bloh, "Unified control of a buck converter for wide load range applications," in *IEEE APEC 2014*, March 2014, pp. 2788-2795.

[8] J. Shen, S. Schröder, H. Stagge, and R. W. De Doncker, "Precise modeling and analysis of DQ-frame current controller for high power converters with low pulse ratio," in *IEEE Energy Conversion Congress and Exposition, September 2012,* Raleigh, NC, USA.

[9] P. Mattavelli, "A closed-loop selective harmonic compensation for active filters," *IEEE Transactions on Industry Applications*, vol. 37, no. 1, pp. 81-89, Jan./Feb. 2001.

[10] M. Hausmann, N. Grass, and B. Piepenbreier, "Harmonic compensation in a load emulation system using different control techniques," in *IEEE 34th International Telecommunications Energy Conference INTELEC,* Sept. 30-Oct. 4, 2012, pp. 1-7.

[11] S. Engel, K. Rigbers, and R. W. De Doncker, "Digital repetitive control of a three-phase flat-top-modulated grid tie solar inverter," in *13th European Conference on Power Electronics and Appl., EPE '09,* 8-10 Sept., 2009, pp. 1-10.

[12] P. Schülting, C. H. van der Broeck, and R. W. De Doncker, "A generalized control design approach for a repetitive controller on current harmonics," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL),* Vancouver, BC, 2015, pp. 1-8.

[13] T. M. Rowan and R. J. Kerkman, "A new synchronous current regulator and an analysis of current-regulated PWM inverters," *IEEE Transactions on Industry Applications,* vol. IA-22, no. 4, pp. 678-690, July 1986.

[14] F. B. del Blanco, M. W. Degner, and R. D. Lorenz , "Dynamic analysis of current regulators for AC motors using complex vectors," *IEEE Transactions on Industry Applications,* vol. 35, no. 6, pp. 1424-1432, Nov./Dec. 1999.

[15] F. Briz, M. W. Degner, and R. D. Lorenz, "Analysis and design of current regulators using complex vectors," *IEEE Transactions on Industry Applications,* vol. 36, no. 3, pp. 817-825, May/Jun. 2000.

[16] S. Gataric and N. R. Garrigan, "Modeling and design of three-phase systems using complex transfer functions," in *Proc. IEEE Power Electron. Spec. Conf.,* vol. 2, June/July 1999, pp. 691-697.

[17] L. Harnefors, "Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 4, pp. 2239-2248, Aug. 2007.

[18] G. D. Holmes and T. Lipo, "Pulse width modulation for power converters - principles and practice," *IEEE Press Series on Power Engineering,* Piscataway, NJ, USA: John Wiley and Sons.

[19] V. Blasko and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three phase voltage source converter," in *IEEE APEC 1996,* vol. 2, 3-7 Mar. 1996, pp. 545-551.

[20] H. van der Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," *IEEE Transactions on Industry Applications,* vol. 24, no. 1, pp. 142-150, Jan./Feb. 1988.

[21] O. Kukrer, "Discrete-time current control of voltage-fed three-phase PWM inverters," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 260-269, Mar 1996.

[22] C. H. van der Broeck, R. W. De Doncker, S. A. Richter, and J. von Bloh, "Discrete time modeling, implementation and design of current controllers," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE),* Pittsburgh, PA, 2014, pp. 540-547.

[23] R. Isermann, "Digital control systems", vol. 1, Springer Press 1989.

[24] S. Buso and P. Mattavelli, "Digital control in power electronics," *Lectures of Power Electronics Morgan & Claypool Publishers,* 2006.

[25] C. H. van der Broeck, M. Biskoping, and R. W. De Doncker, "Discrete time control design of three phase PWM rectifiers," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe),* Geneva, 2015, pp. 1-10.

[26] J. He, Y. W. Li, F. Blaabjerg, and X. Wang, "Active harmonic filtering using current-controlled, grid-connected DG units with closed-loop

power control," *IEEE Transactions on Power Electronics,* vol. 29, no. 2, pp. 642-653, Feb. 2014.

[27] P. Schuelting, C. H. van der Broeck, and R. Doncker, "Analysis and design of repetitive controllers for applications in distorted distribution grids," *IEEE Transactions on Power Electronics*, 2018.

[28] M. Rosekeit, C. van der Broeck, and R. W. De Doncker, "Dynamic control of a dual active bridge for bidirectional AC charging," in *2015 IEEE International Conference on Industrial Technology (ICIT),* Seville, 2015, pp. 2085-2091.

[29] N. Hoffmann, F. W. Fuchs, M. P. Kazmierkowski, and D. Schröder, "Digital current control in a rotating reference frame - Part I: System modeling and the discrete time-domain current controller with improved decoupling capabilities," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5290-5305, July 2016.

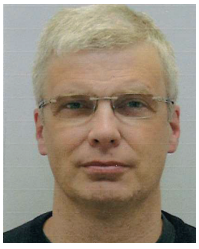
[30] M. Rivera, V. Yaramasu, A. Llor, J. Rodriguez, B. Wu, and M. Fadel, "Digital predictive current control of a three-phase four-leg inverter," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 11, pp. 4903-4912, Nov. 2013.

[31] A. G. Yepes, A. Vidal, J. Malvar, O. López, and J. Doval-Gandoy, "Tuning method aimed at optimized settling time and overshoot for synchronous proportional-integral current control in electric machines," *IEEE Transactions on Power Electronics,* vol. 29, no. 6, pp. 3041-3054, June 2014.

[32] J. Xu, T. Tang, and S. Xie, "Research on low-order current harmonics rejections for grid-connected LCL-filtered inverters," *IET Power Electronics,* vol. 7, no. 5, pp. 1227-1234, May 2014.

Christoph H. van der Broeck received the B. Sc. and M. Sc. degree in electrical engineering from RWTH Aachen University, Germany, in 2010 and 2013. From 2011 to 2012 he joined the Wisconsin Electric Machine and Power Electronic Consortium at the University of Wisconsin, Madison, as a Fulbright Scholar. Between 2012 and 2013 he worked with AixControl GmbH on control design of power converters. Since January 2014, he has been working towards the Ph.D. degree at the Institute for Power Electronics and Electrical Drives (ISEA), RWTH Aachen University. His research interests include the modeling and control of power electronic converters and drives.

Sebastian A. Richter received the Ph.D. degree in electrical engineering from RWTH Aachen University, Germany, in 2013. Since his time as research associate at the Institute for Power Electronics and Electrical Drives (ISEA), RWTH Aachen University, he manages the group Control & Simulation at AixControl GmbH, Aachen, Germany. His research interests include control of power electronic converters, renewable energy and power quality.



Jochen von Bloh received the Ph.D. degree in electrical engineering from RWTH Aachen University, Germany, in 2001. Until 2002 he led the research group for power electronics as chief engineer at the Institute for Power Electronics and Electrical Drives (ISEA). In 2002 he founded the AixControl GmbH, a company specialized in Rapid Power Prototyping tools, power electronic design and test systems for power electronic application. His research interests include control of power electronic converters, power quality and EMI issues.

Rik W. De Doncker received the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1986. In 1987, he was appointed as a Visiting Associate Professor at the University of Wisconsin, Madison. After a short stay as an Adjunct Researcher with Interuniversity Microelectronics Centre, Leuven, he joined, in 1989, the Corporate Research and Development Center, General Electric Company, Schenectady, NY. In 1994, he joined Silicon Power Corporation, a former division of General Electric Inc., as the Vice President of Technology. In 1996, he became a Professor at RWTH Aachen University, Aachen, Germany, where he currently leads the Institute for Power Electronics and Electrical Drives. Since 2006, he has been the Director of the E.ON Energy Research Center, RWTH Aachen University. Dr. De Doncker was the President of the IEEE Power Electronics Society (PELS) in 2005 and 2006. He was the founding Chairman of the German IEEE Industry Applications Society PELS Joint Chapter. In 2002, he was the recipient of the IEEE IAS Outstanding Achievement Award. In 2008, he received the IEEE PES Nari Hingorani Custom Power Award. In 2009, he led a VDE/ETG Task Force on Electric Vehicles. In 2010, he received an honorary doctor degree of TU Riga, Latvia. In 2013, he received the IEEE William E. Newell Power Electronics Award.

Call for Papers

CPSS Transactions on Power Electronics and Applications

Special Issue on Applications of Wide Bandgap Devices, 2018

Scheduled Publication Time: December 31, 2018

The emergence of wide bandgap (WBG) semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN) devices promises to revolutionize next-generation power electronics converters. Featuring high breakdown electric field, low specific on-resistance, fast switching speed, and high junction temperature capability, these devices are beneficial for the efficiency, power density, reliability, and/or cost of power electronics converters. Applications of WBG devices have been seen in the electric utility grid, transportation, industrial motor drives, power supplies, and consumer electronic products. And more emerging applications can be expected. However, extremely fast switching and other superior characteristics of WBG device, and high switching frequency/high voltage/high junction temperature operation, present new design challenges in gate drive, packaging and layout, EMI suppression, converter control, etc. Addressing these design and application issues is critical to the adoption, commercialization, and success of WBG based power electronics. This special issue intends to publish the latest results on these important application topics.

Prospective researchers are invited to submit original contributions or survey papers for peer review for publication in CPSS Transactions on Power Electronics and Applications. Topics of interest of this Special Issue include, but are not limited to:

- Application in motor drives
- Applications in renewable energy, energy storage, and grid
- Transportation applications
- Applications in communications, digital systems, and data centers
- Emerging applications of WBG devices
- Gate drive, protection and other auxiliary circuits
- Packaging and passive components
- EMI issues and solutions
- High-quality sensing and control
- Design methodologies for WBG power electronics

The manuscripts should be submitted through Manuscript Central at https://mc03.manuscriptcentral.com/tpea-cpss. Submissions must be clearly marked “Special Issue on Applications of Wide Bandgap Devices, 2018” on the cover page. The information about manuscript preparation and requirements is provided on http://tpea.cpss.org.cn/a/For_Authors/. Manuscripts submitted to this Special Issue will be reviewed and handled by the guest editorial board as noted below.

Deadline for Submission of Manuscripts: November 11, 2018

Guest Editor-in-Chief: Fei (Fred) Wang, University of Tennessee, Knoxville, USA
Guest Co-Editor-in-Chief: Bo Liu, University of Tennessee, Knoxville, USA

Guest Associate Editors:

- Layi Alatise, The University of Warwick, UK
- Hua (Kevin) Bai, University of Tennessee, Knoxville, USA
- Dong Cao, North Dakota State University, USA
- Dong Dong, Virginia Tech, USA
- Ben Guo, United Technologies Research Center, USA
- Shiqi Ji, University of Tennessee, Knoxville, USA
- Puqi Ning, Chinese Academy of Sciences, China
- Edward Jones, Efficient Power Conversion, USA
- Hui (Helen) Li, Florida State University, USA
- Qiang Li, Virginia Tech, USA
- Fang Luo, University of Arkansas, USA
- Dong Jiang, Huazhong University of Science and Technology, China
- Jin Wang, The Ohio State University, USA
- Jun Wang, Virginia Tech, USA
- Laili Wang, Xi’an Jiaotong University, China
- Mengqi (Maggie) Wang, University of Michigan-Dearborn, USA
- Shuo Wang, University of Florida, USA
- Jing Xu, ABB Corporate Research, USA
- Xibo Yuan, University of Bristol, UK
- Zheyu Zhang, General Electric Global Research, USA

Proposed Timeline:

- November 11, 2018 – Manuscripts submission deadline
- December 5, 2018 – Final acceptance notification
- December 31, 2018 – Camera-ready manuscripts for publication

CHINA POWER SUPPLY SOCIETY

China Power Supply Society (CPSS) founded in 1983 is a nonprofit, non-governmental academic and professional organization of scientists and engineers in the power supply & power electronics fields. CPSS is dedicated to achieving scientific and technological progress of power supply and the advancement of the power supply industry. CPSS website is www.cpss.org.cn.

ADMINISTRATIVE OFFICE

Add: 16th Floor, Datong Building, No.467 Huanghe Road, Nankai District, Tianjin, 300110, China

Tel: +86-22-27680796 Fax: +86-22-27687886

E-mail: cpss@cpss.org.cn Website: www.cpss.org.cn

CPSS TRANSACTIONS ON
POWER ELECTRONICS AND APPLICATIONS

(Quarterly, Started in 2016)

Vol.3 No.3 Sept. 30, 2018

Sponsored by: China Power Supply Society (CPSS)

Technically Co-Sponsored by: IEEE Power Electronics Society (IEEE PELS)

Supported by: Sungrow Power Supply Co., Ltd.
Xiamen Kehua Hengsheng Co., Ltd.
Shenzhen Inovance Technology Co., Ltd.
StarPower Semiconductor Ltd.

Editor-in-Chief: Jinjun Liu

Published by: Editorial Office of CPSS TPEA

Address: 16th Floor, Datong Building, No.467 Huanghe Road,
Nankai Dist., Tianjin, 300110, China

Tel: +86-22-27680796-18#

Fax: +86-22-27687886

E-mail: tpea@cpss.org.cn

Website: tpea.cpss.org.cn