

Three Phase Trans-Quasi-Z-Source Inverter

Xupeng Fang, Bolong Ma, Guanzhong Gao, and Lixin Gao

Abstract—In this paper, a new type of single-stage boost Trans-quasi-Z-source inverter topology is presented. The basic structure and working principle of the inverter are analyzed and its voltage gain is deduced. The model of the Trans-quasi-Z-source network is established by using Laplace transform. The dynamic characteristics of the system are analyzed, and the switching loss is explored by comparing the different shoot-through injection methods. In order to verify the dynamic boost characteristics, the Matlab/Simulink simulation is performed. Finally, the hardware circuit is built on the basis of theoretical analysis and simulation verification. The experimental results verify the feasibility and stability of the circuit.

Index Terms—Dynamic boost characteristics, single-stage boost, switching loss, trans-quasi-Z-source inverter.

I. INTRODUCTION

As the fossil fuel is not renewable and the pollution it causes to the environment, new energy technologies, such as fuel cell, solar energy and wind energy, have attracted more and more attention and application. However, most of the output of the new energy generation is unstable DC or AC power; it has to be converted to a usable DC or AC power. The traditional inverter can better meet the requirement of users only when the DC bus voltage is large enough, otherwise, a DC-DC converter must be added to achieve the boosting purpose.

The Z-source inverter topology was presented by Professor Fangzheng Peng in 2002 [1], once it has been put forward, it has aroused widespread concern in the power electronics area and became a hotspot in the field, and it has been studied on the solar photovoltaic generation, fuel cell generation, motor drive and so on [2]-[4]. However, there are some defects in the circuit, such as discontinuous input current, excessive voltage stress of capacitor, too large surge current when the circuit starts [5]-[7]. In 2008, Professor Fangzheng Peng proposed an improved circuit topology on this basis—the Quasi-Z-source inverter; it can overcome the problem that the capacitor voltage or the inductor current is too large in the impedance source network of the Z-source inverter, and also attracted wide concern in the power electronics field [8]-[10]. However, there is a common defect in the Z-source and quasi-Z-source inverter: the actual attainable boost gain is small. When the input voltage is low and

the required voltage gain is large, the inverter needs to work in a larger shoot-through duty cycle, so the modulation index must be reduced correspondingly, resulting in poor output voltage quality[11]-[13].

To solve the above problems, many domestic and foreign scholars have proposed many modified Z-source inverter circuit topology, such as switched-inductor Z-source inverter, Y-source inverter, Delta-source inverter, Trans-Z-source inverter and so on[14]-[18]. However, these inverters also has some defects, for example, some circuit topologies have good boost capacity, but the capacitor suffers large voltage stress; some circuit topology's capacitor has small voltage stress, but the boost ability has been limited; some circuit topology's capacitor has small voltage stress and has good boost capacity, but has a complex structure, large volume and high cost, etc.

This manuscript presents a Trans-quasi-Z-source inverter circuit topology, it is a new type of inverter circuit, based on the traditional quasi-Z-source inverter, it changes an inductor of the quasi-Z-source network into a coupling form, and leads a capacitor in the middle, by changing the turn ratio of the coupled inductors to adjust the boost ratio, and it can make up the defects of the traditional quasi-Z-source inverter that the duty ratio and modulation index restrict each other, and has good boost capacity, and eliminate the influence of the dead time to the output voltage ripple. The following is the structure of the manuscript: the second part is the analysis of the operating principle of the circuit, the third part analyzes the boost characteristics of the circuit, the fourth part is control strategy analysis, the fifth part gives the switching times and switching loss analysis, in the end the simulation and experimental verification are given.

II. CIRCUIT PRINCIPLE ANALYSIS

The proposed Trans-quasi-Z-source inverter is improved based on the traditional Trans-Z-source inverter, and only an inductor and a diode are added, which is shown in Fig. 1. Same as other Z-source inverter topologies, the shoot-through zero states are inserted in the two traditional zero-states of the inverter, thus it does not affect the normal operation of the inverter, but the inverter has the better buck-boost function. Assuming that all the devices are ideal, the conduction voltage drop of the diode and IGBT is zero. When the inverter operates in the shoot-through zero-states, the diode on the input side is subjected to reverse voltage and turned off. When the inverter operates in the non-shoot-through states, the diode is turned on, and the reference directions of the voltages and currents in the circuit are shown in Fig. 1.

It is assumed that the duration of a switching period is T , the shoot-through time is T_0 (corresponding time t_0 to t_1), the non-shoot-through time is T_s (corresponding time t_1 to t_2), and the

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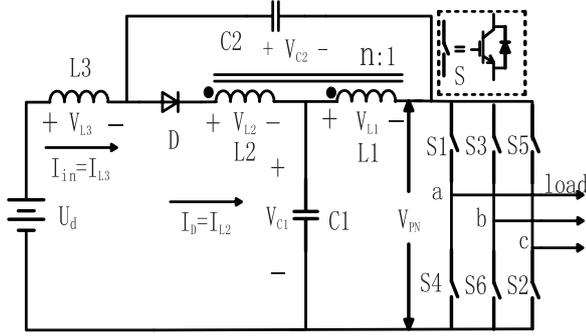


Fig. 1. The Trans-QZ-source inverter topology.

shoot-through duty ratio is D , we have

$$T_0 = DT \quad (1)$$

$$T_s = (1-D)T \quad (2)$$

The equivalent circuit of the Trans-quasi-Z-source inverter working in the shoot-through mode is shown in Fig. 2(a), the inverter bridge is short-circuit, the diode is turned off, the power supply and capacitor C_2 charge the inductor L_3 , and the capacitor C_1 recharges the inductor L_1 , the magnetization current of the inductor increases gradually. Because the inductors L_1 and L_2 are coupled tightly, the excitation current is reflected to the secondary windings of the coupled inductor, the voltage of the L_2 is gradually increased from a small value to $V_{L2}=nV_{L1}$, the inductor L_2 is charged. At this point, the potential of the left of the inductor L_2 is high, and the diode withstands the reverse voltage.

$$V_{L1} = V_{C1} \quad (3)$$

$$V_{L2} = nV_{L1} = nV_{C1} \quad (4)$$

$$V_{L3} = U_d + V_{C2} \quad (5)$$

The equivalent circuit of the inverter working in the non-shoot-through mode is shown in Fig. 2(b), the diode is turned on and the inverter bridge can be equivalent to a controlled current source. The coupling inductors L_1, L_2 and the input inductor L_3 power the load together, while charge the capacitor, and the voltage of the inverter bridge is improved [19]. Now, we have,

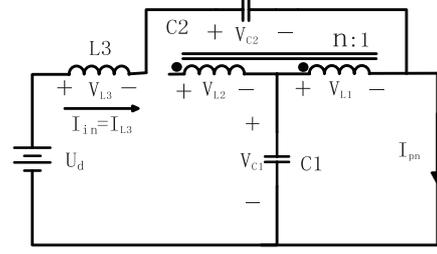
$$-V_{C2} = V_{L1} + V_{L2} \quad (6)$$

$$V_{L3} = U_d - V_{L2} - V_{C1} \quad (7)$$

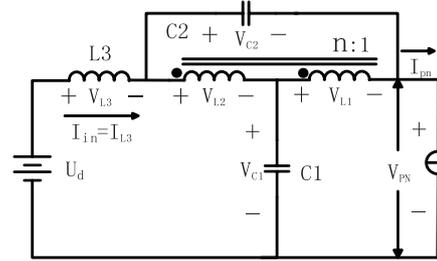
$$V_{PN} = V_{C1} - V_{L1} \quad (8)$$

From the above analysis, we know that the Trans-quasi-Z-source inverter is to control the on-off of the diode by controlling the shoot-through and non-shoot-through state of the inverter bridge, and to transfer the energy stored in the coupling inductor and the input inductor to achieve the boosting purpose.

For the inductors L_1, L_2, L_3 , the average voltage on them in a switching period is zero, we can have,



(a) shoot-through zero state



(b) non-shoot-through state

Fig. 2. The operating principle of the Trans-QZ-source inverter.

$$\frac{1}{T} \left[\int_{t_0}^{t_1} V_L d_t + \int_{t_1}^{t_2} V_L d_t \right] = 0 \quad (9)$$

From the above analysis, and based on the ‘‘Volt-Second’’ balance relation, we can have,

$$DV_{C1} - (1-D)(V_{C2} + V_{L2}) = 0 \quad (10)$$

$$nDV_{C1} - (1-D)(V_{C2} + V_{L1}) = 0 \quad (11)$$

$$D(V_{dc} + V_{C2}) + (1-D)(U_d - V_{L2} - V_{C1}) = 0 \quad (12)$$

$$V_{L2} = nV_{L1} \quad (13)$$

From the formulas (10) and (11), we can have,

$$V_{C2} = \frac{(1+n)D}{1-D} V_{C1} \quad (14)$$

$$V_{C2} = \frac{(1+n)D}{1-(2+n)D} U_d \quad (15)$$

$$V_{C1} = \frac{1-D}{1-(2+n)D} U_d \quad (16)$$

The DC-link peak voltage of the inverter can be obtained through (10), (11), (14) and (15).

$$V_{PN} = \frac{1}{1-(2+n)D} U_d = BU_d \quad (17)$$

The boost ratio B can be expressed as:

$$B = \frac{1}{1 - (2 + n)D} \quad (18)$$

The voltage gain G can be expressed as:

$$G = MB = \frac{M}{1 - (2 + n)D} \quad (19)$$

Wherein M is the modulation index of the inverter.

From the above analysis, we can see that the voltage gain of the Trans-quasi-Z-source inverter is not only related to the shoot-through duty cycle D , but also to the turn ratio n of the coupling inductors and the modulation index M of the inverter. When the n is fixed, the DC bus voltage increases with the increase of D ; When the D is fixed, the DC bus voltage will increase with the increase of the turn ratio n ; When the modulation index M and the duty cycle D of the inverter are mutually restricted, and the ideal DC bus voltage cannot be achieved, the voltage can be compensated by changing the turn ratio n , so as to achieve the required DC bus voltage. Usually, we can try to reduce the duty ratio D by increasing the turn ratio n , so as to increase the modulation index M of the inverter, improve the conversion efficiency, and suppress the harmonic effect brought by the boost network.

III. ANALYSIS OF CIRCUIT BOOST CHARACTERISTICS

The boost ratio of the traditional Z-source inverter is related to the shoot-through duty ratio D and the modulation index M . The boost ratio B is influenced by the circuit structure, and the boost capacity is limited. The Trans-Z-source inverter adopts the coupling inductor form [19]-[21]; its boost ability is not only related to the shoot-through duty ratio D , but also related to the turn ratio n , obviously, it improves the boost capacity of the circuit.

The Trans-quasi-Z-source inverter is improved on the basis of the traditional Z-source inverter and the Trans-Z-source inverter, so that it has a higher boost capacity. The relationship among the boost ratio B , the duty ratio D and the turn ratio n of the Trans-quasi-Z-source inverter are shown in Fig. 3, the boost effect is not very obvious at $n = 1$, which is almost the same as that of the traditional Z-source or quasi-Z-source inverter, however, when the n is increased to 3, the boost capacity of the Trans-quasi-Z-source inverter will be greatly improved. When the D is close to 0.2, the boost gain is close to infinity, which overcomes the defect that the traditional quasi-Z-source inverter must increase the duty ratio D by reducing the modulation index M to improve the output voltage [22]-[24].

The boost ratio correlation curves of the Trans-quasi-Z-source inverter, Z-source inverter and Trans-Z-source inverter, are shown in Fig. 4 and Fig. 5, When $n = 1$, the boost ratio of the Trans-Z-source inverter is the same as that of the traditional Z-source inverter. The two curves coincide fully, and the two inverters have limited boost capacity. Only when the shoot-through duty ratio D is close to 0.5, can a larger boost ratio be

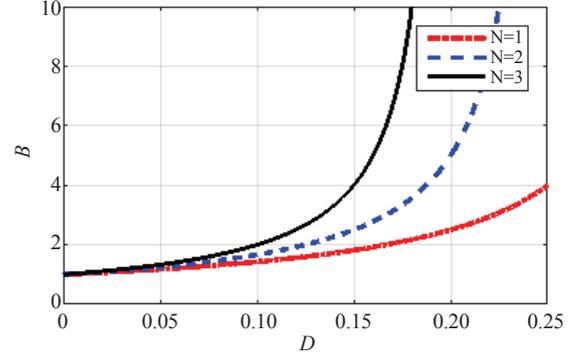


Fig. 3. The relationship between the voltage gain and the shoot-through duty cycle of the Trans-QZSI.

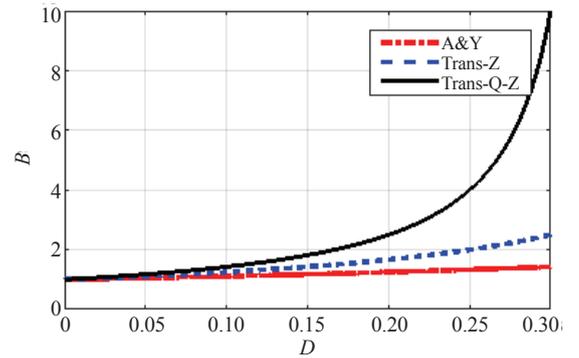


Fig. 4. The correlation curves of the boost ratio when $n = 1$.

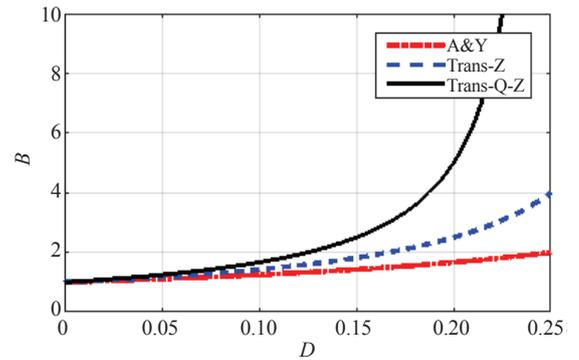


Fig. 5. The correlation curves of the boost ratio when $n = 2$.

achieved. The boost ratio of the Trans-quasi-Z-source inverter has reached 4 when $D = 0.25$, compared with the other two kinds of inverters, the boost capacity of the Trans-quasi-Z-source inverter is greatly enhanced. When $n = 2$ and in the same duty ratio D , the Trans-quasi-Z-source inverter has the best boost ability, the Trans-Z-source inverter is the next, and the traditional Z-source inverter is the least, the gap in the boost capacity of the three inverters is becoming more and more obvious with the increase of the shoot-through duty ratio D .

IV. ANALYSIS OF CIRCUIT CONTROL STRATEGY

If we adopt the simple boost control method, from the oper-

ating principle analysis, we can see that the shoot-through zero vector can only be inserted to the traditional zero vector, while the traditional zero vector in sinusoidal pulse width modulation (SPWM) shows the effect of the difference between the modulation wave and the carrier peak in time [25]-[27]. Two equal and opposite polarity voltages V_n and V_p are taken, the value of the two voltages are between the modulation wave and the carrier. The comparison results of the voltage V_n or V_p and the carrier is the switching time of the shoot-through vector. The value of V_n and V_p determines the size of the duty ratio D , by adding V_n and V_p into each group of modulated waves, the shoot-through states are injected. When V_n or V_p acts individually, the duty ratio is D_0 , and the duty ratio is $2D_0$ when V_n and V_p act simultaneously. The principle of the simple boost control is shown in Fig. 6.

V. ANALYSIS OF SWITCHING TIMES AND SWITCHING LOSS

From the principle diagram shown in Fig. 6, it can be seen that the order of the switch of the SPWM signal is fixed, that is to say, it is impossible to reduce the switching times by changing the order of the switch. But the injection of the shoot-through signal will certainly increase the switching times in a switching period. There exists a problem in the process of the injection of the shoot-through signal; the shoot-through states may be implemented by one bridge arm, or by two bridge arms, and even by three bridge arms [28], [29]. Although these three shoot-through modes achieve the same results, single arm shoot-through mode only increases one time of switching, and the two arms shoot-through mode increases two times of switching. Similarly, the three arms simultaneous shoot-through mode has the largest number of switching times and the corresponding shoot-through state is shown in Fig. 7. The three arms shoot-through mode is chosen in the following simulation and experiments of the manuscript.

The switch voltage stress of the three-phase Trans-quasi-Z-source inverter is equal to the input voltage of the inverter bridge, that is, the DC-link voltage,

$$V_s = V_{PN} = BU_d \quad (20)$$

Suppose that under the maximum boost condition $D = 1 - M$, from the formulas (18), (19) and (20), we can have

$$V_s = \frac{(2+n)G-1}{(1+n)} U_d \quad (21)$$

The relationship between the voltage stress of the switch and the voltage gain is plotted by the Matlab/Figure software, as shown in Fig. 8. It indicates that the voltage stress of the power switches is related to the voltage gain MB and the turn ratio n , and with the increase of MB and n , the voltage stress of the power switches will increase either. Thus, don't to increase the voltage gain and the turn ratio blindly, it is essential to consider the voltage withstanding ability of the power switches.

According to the working principle of the Z-source inverter, the larger the shoot-through duty ratio D , the larger the voltage gain, and the higher the voltage stress of the power switch.

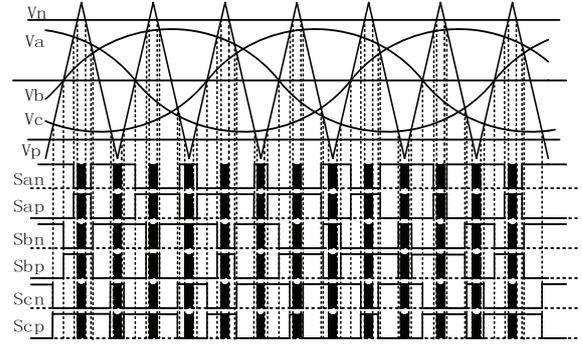


Fig. 6. The simple boost control method.

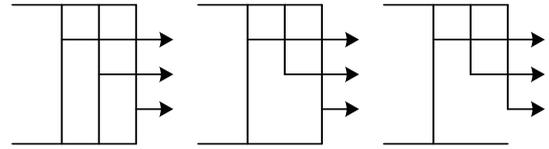


Fig.7. The three different shoot-through methods.

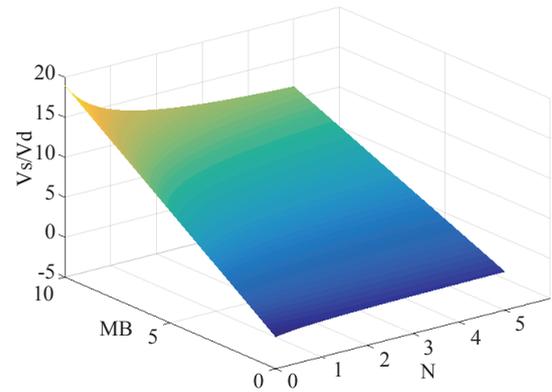


Fig. 8. The relationship of V_s versus n and MB .

Therefore, the duty ratio D should be reduced under the condition that the modulation index M is as large as possible, in order to reduce the voltage stress of the power switches. In addition, the switch voltage stress can be reduced by the modulation method, such as the SVPWM control strategy, the maximum boost SPWM control strategy and so on.

The current stress of the switch is different from the voltage stress of the switch, because the inductor current and the load current are all circulated through the shoot-through bridge arm, the parallel connection of the bridge arms has the function of shunt and no partial voltage. So the effect of the different three types of the shoot-through modes on the current stress of the power switch is very great. The same as the traditional Z-source inverter, when the load power angle is $0 \leq \theta \leq 30^\circ$, the current stress of the switch in the shoot-through vector is two times the peak of the inductor current [4].

$$I_{\max} = 2I_L \quad (22)$$

Suppose the phase current of the three-phase inverter is

$$\begin{cases} i_a = I_{out} \sin(\omega t - \theta) \\ i_b = I_{out} \sin(\omega t - 2\pi/3 - \theta) \\ i_c = I_{out} \sin(\omega t + 2\pi/3 - \theta) \end{cases} \quad (23)$$

When $\theta > 30^\circ$, the current stress of the switch in the shoot-through state is the largest.

$$I_{max} = 2I_L + I_{out} \sin(\theta - 30^\circ) \quad (24)$$

The maximum current stress of the switch in the shoot-through state is I_{max} , for the single bridge arm shoot through mode, the maximum current stress is $I_{max1} = I_{max}$; for the two bridge arms shoot-through mode, the maximum current stress is $I_{max2} = I_{max}/2$; for the three bridge arms shoot-through mode, the maximum current stress is $I_{max3} = I_{max}/3$. For the two bridge arms simultaneously conduct mode, the current stress of each bridge arm is reduced to 1/2 of the original value. And for the three bridge arms simultaneously conduct mode, the current stress of each bridge arm is reduced to 1/3 of the original value. It is assumed that the internal resistance of the switch is R , the average conduction current of each bridge arm is I_{avmax} and the conduction loss is P_0 .

When the three bridge arms simultaneously shoot-through:

$$I_{avmax} = I_{max}/3 \quad (25)$$

$$P_0 = (I_{avmax})^2 R = (I_{max}/3)^2 R * 3 = \frac{1}{3} I_{max}^2 R \quad (26)$$

When the two bridge arms simultaneously shoot-through:

$$I_{avmax} = I_{max}/2 \quad (27)$$

$$P_0 = (I_{avmax})^2 R = (I_{max}/2)^2 R * 2 = \frac{1}{2} I_{max}^2 R \quad (28)$$

When the single bridge arm shoot-through:

$$I_{avmax} = I_{max} \quad (29)$$

$$P_0 = (I_{avmax})^2 R = I_{max}^2 R \quad (30)$$

From the above analysis, we can see that the three bridge arms shoot-through mode can decrease the average conduction current, reduce the switch current stress, and therefore can reduce the conduction loss.

VI. THE CIRCUIT SIMULATION VERIFICATION AND ANALYSIS

The turn ratio of the Trans-quasi-Z-source inverter only affects the boost ratio of the system and has no effect on the stability and response speed of the system. Also in the case of $n = 1$, to analyze the influence of the system response when the inductors and capacitors change in the Trans-quasi-Z-source network. The load is assumed to be a purely resistive load when analyzing the network stability of the Trans-quasi-Z-source

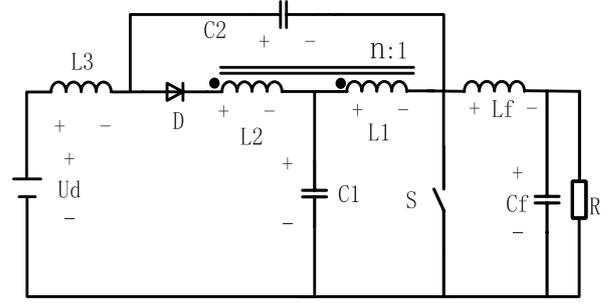


Fig. 9. The circuit model of the Trans-quasi-Z-source inverter.

inverter, and the inverter bridge is replaced with a switch S . The equivalent small signal model structure of the Trans-quasi-Z-source inverter topology is shown in Fig. 9. Under the condition of $n = 1$, the voltage regulation process is accurately analyzed by comparing different inductance and capacitance within the allowable variation range, and the network element parameters that are most suitable for the Trans-quasi-Z-source inverter are selected according to actual conditions.

In order to establish the circuit model of the Trans-quasi-Z-source inverter, adds a disturbance signal on the input voltage U_d and d_0 . Let $X = x + \hat{x}$, x and \hat{x} are variable after adding perturbation to the DC side and d_0 , I_{load} , I_{L1} , I_{L3} , V_{C1} , V_{C2} . The transfer function of the multi-input multi-output Trans-quasi-Z-source network is deduced by Laplace transform. The transfer function is the same from d_0 to the capacitor voltage V_{C1} and V_{C2} , and it can be expressed as:

$$\begin{aligned} G_{d_0}^{v_{c_2}}(s) &= \left. \frac{\hat{v}_{c_2}(s)}{\hat{d}_0(s)} \right|_{\substack{i_{load}(s)=0 \\ V_{c_1}(s)=0}} \\ &= \frac{(V_{C1} + V_{C2} - RI_{load})(1 - 3D_0) + (I_{load} - I_{L1} - I_{L2})(LS + R + r)}{LCS^2 + C(r + R)S + (1 - 3D_0)^2} \end{aligned} \quad (31)$$

The second-order transfer function for the capacitor voltage versus the input voltage can be expressed as:

$$G_{v_{dc}}^{v_{cs}}(s) = \left. \frac{\hat{v}_{cs}(s)}{V_{dc}(s)} \right|_{\substack{i_{load}(s)=0 \\ d_0(s)=0}} = \frac{1 - 3D_0}{LCS^2 + C(r + R)S + (1 - 3D_0)^2} \quad (32)$$

The effect of the inductance and capacitance variation on the system is shown in Fig. 10 to Fig. 11. As can be seen from Fig. 10, as the inductance increases, the maximum overshoot of the system will be gradually reduced, the system oscillation amplitude and the voltage fluctuation is relatively small and the voltage adjustment process is relatively flat. It is suitable for stable voltage output. However, as the inductance increases, the rise time of the system will become longer at the same time, the voltage tends to be steady for a longer time and the system voltage response is relatively slow. Thus, the large inductance can make the system respond process becomes smooth, but will pay the cost of extending the system response time, so the reasonable choice of the inductance parameters will make the system response to the best. It can be seen from Fig. 11 that the performance index of the rise time, maximum overshoot, and

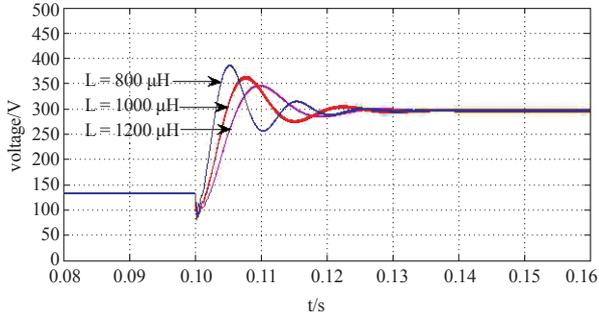


Fig. 10. The response process of the system when L changed.

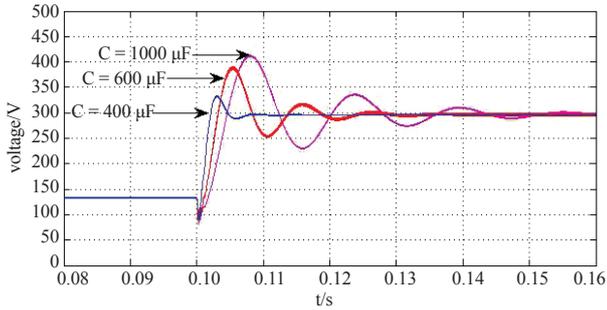


Fig. 11. The response process of the system when C changed.

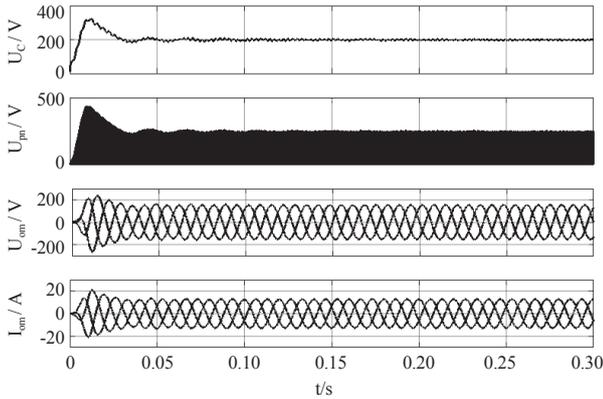


Fig. 12. The output voltage waveforms when $n = 1, D = 0.2$.

oscillation amplitude is good and the system responds quickly when the capacitance parameter is relatively small. Therefore, the capacitance of the capacitor should be selected smaller within the allowable range.

According to Fig. 10 and Fig. 11, the capacitance of the C_1 and C_2 is $470 \mu\text{F}$, the inductance of the L_1 and L_3 is $800 \mu\text{H}$ and the switching frequency f_s is 20 kHz . The simulated output voltage waveforms of the Trans-quasi-Z-source inverter are shown in Fig. 12 and Fig. 13 when the input DC voltage U_d is 100 V , the modulation index $M = 0.7$.

When $n = 1, D = 0.2$, the three-phase voltage waveforms are shown in Fig. 12, the measured values of capacitor voltage, DC link voltage, AC output line voltage and line current are close to their theoretical values of $200 \text{ V}, 250 \text{ V}, 151.56 \text{ V}$ and 12.5 A .

When $n = 2$ and $D = 0.15$, the three-phase voltage waveforms are shown in Fig. 13. The measured values of capacitor voltage,

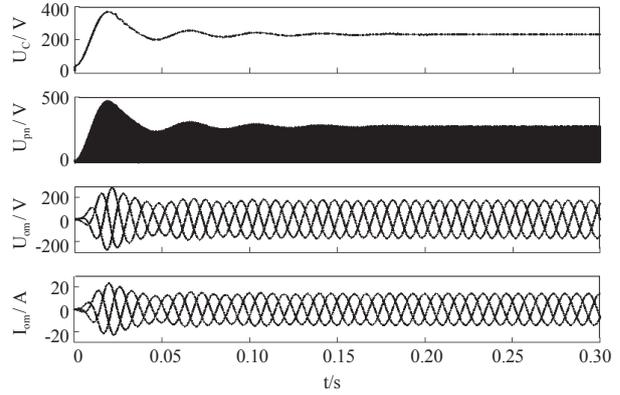


Fig. 13. The output voltage waveforms when $n = 2, D = 0.15$.

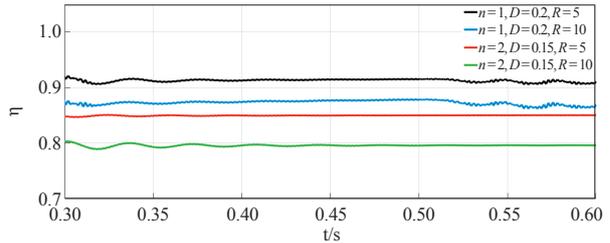


Fig.14. The efficiency curves in different n, D and R .

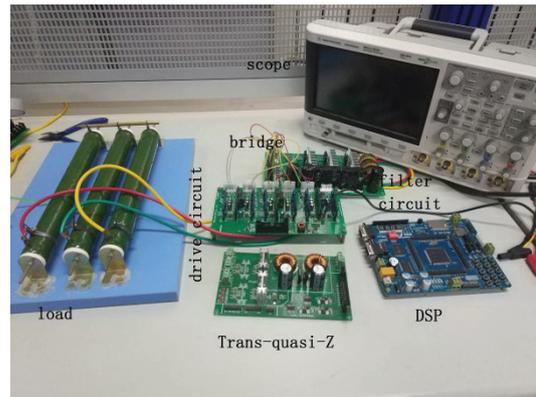
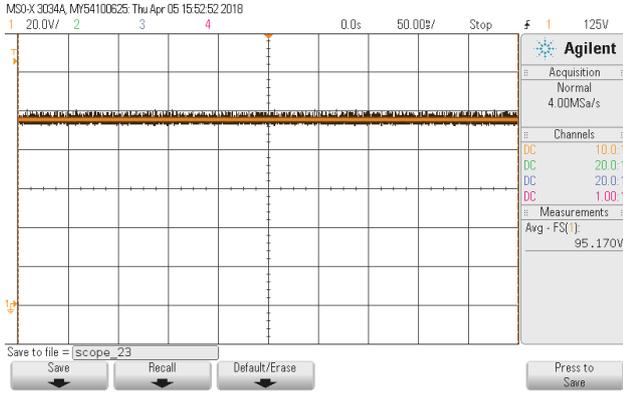


Fig. 15. The prototype of the experiment circuit.

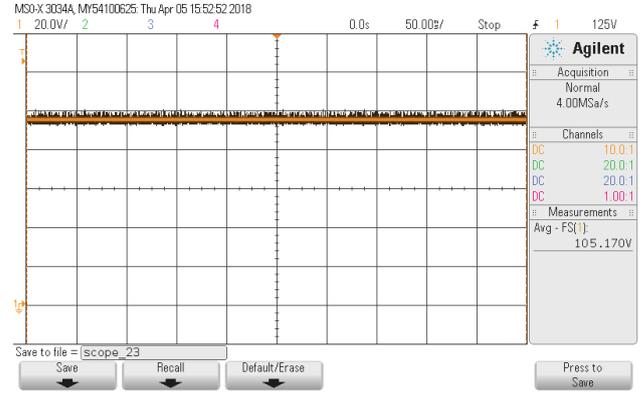
DC link voltage, AC output line voltage and line current are close to their theoretical values of $212.5 \text{ V}, 250 \text{ V}, 151.56 \text{ V}$ and 12.5 A .

The efficiency curves of the proposed inverter under different turn ratio, different shoot-through duty cycle and different load are shown in Fig. 14, it is shown clear that under the condition of same turn ratio and shoot-through duty cycle, the heavier the load, the higher the efficiency, and when $n = 1, D = 0.2, R = 50 \Omega$, the efficiency of the inverter will be higher than 92% ; under the condition of the same load, the smaller the turn ratio, the higher the efficiency, this dues to that with the larger turn ratio of the couple transformer, the more power loss in the transformer, so in the actual engineering applications, it is unsuitable to blindly increase the turn ratio to pursue the boost ability.

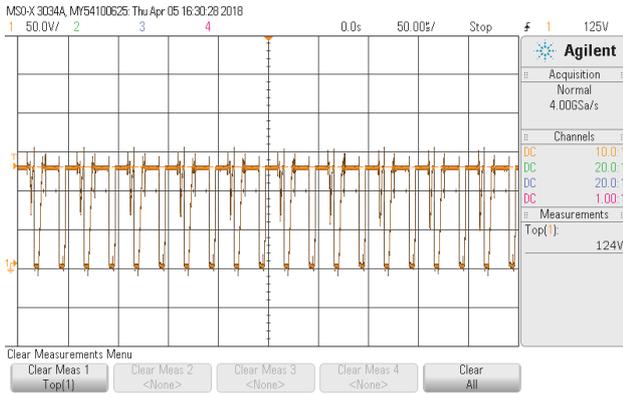
Based on the analysis of the simulation results, the simulation results are close to the theoretical values within the



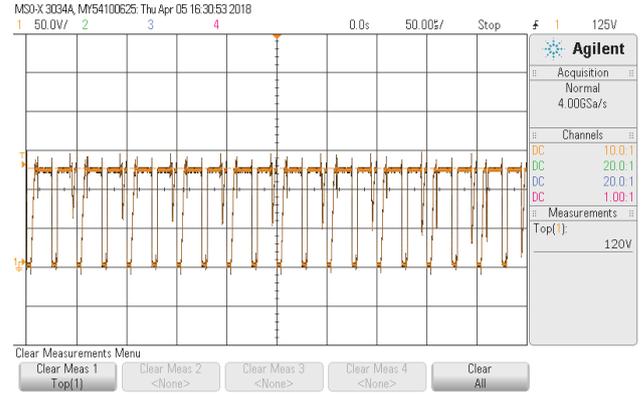
(a) Capacitor C_1 voltage



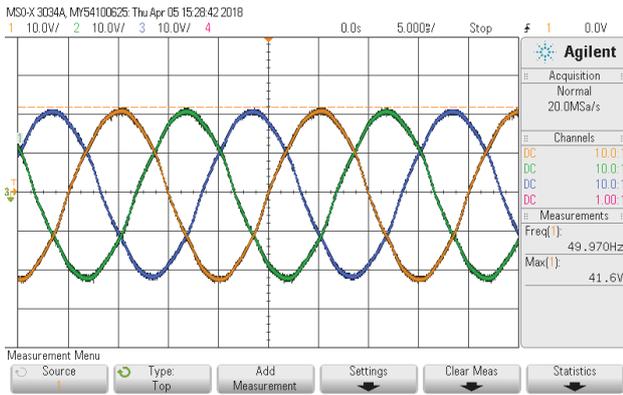
(a) capacitor C_1 voltage



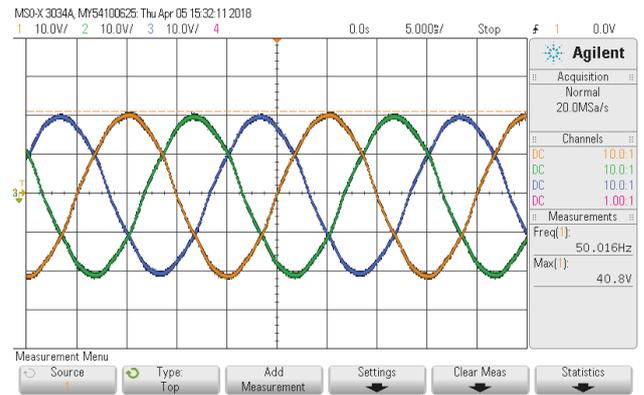
(b) DC link voltage



(b) DC link voltage



(c) Output AC voltage



(c) Output AC voltage

Fig. 16. The output voltage waveforms when $n = 1, D = 0.2$.

Fig. 17. The output voltage waveforms when $n = 2, D = 0.15$.

allowable range of errors, which verifies the correctness of the theoretical analysis.

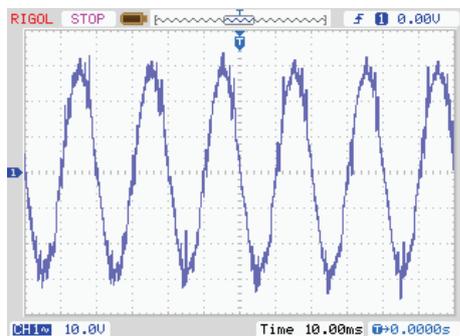
VII. EXPERIMENTAL VERIFICATION OF THE CIRCUIT

A hardware circuit is built based on the simulation, which is shown in Fig. 15, the hardware circuit verifies the boost waveform at $n = 1$ and $n = 2$. With the same parameters in the simulation circuit, $L_1 = 800 \mu\text{H}$ and $L_3 = 800 \mu\text{H}$, capacitor $C_1 = 470 \mu\text{F}$ and $C_2 = 470 \mu\text{F}$, DC voltage $U_d = 50 \text{V}$, the inverter modulation index M is 0.7 and the switching frequency f_s is 20

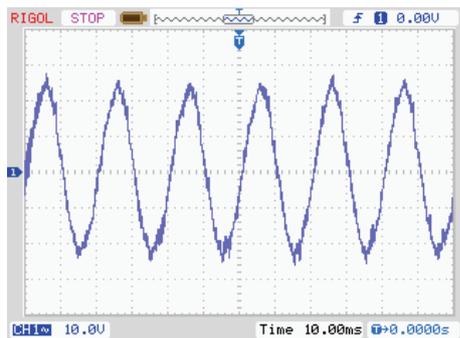
kHz, the rated power level of the prototype can achieve 3 kW, and the experiments is performed based on the smaller power level. The oscilloscope intercepts the output voltage waveforms and the experimental results are shown in Fig. 16-Fig. 17.

When $n = 1, D = 0.2$, the three-phase output voltage waveforms are shown in Fig. 16. The theoretical voltage value of the capacitor C_1 , DC link and the output AC voltage is 100 V, 125 V and 44 V, respectively. And the actual experimental result is about 98 V, 123 V, 42 V, respectively.

When $n = 2, D = 0.15$, the three-phase output voltage waveforms are shown in Fig. 17. The theoretical voltage value of



(a) Delta-source inverter



(b) Trans-Z-source inverter

Fig. 18. Output voltage of phase A of Delta-source inverter and Trans-Z-source inverter.

capacitor C_1 , DC link, and the output AC voltage is 106 V, 125 V, 44 V, respectively. And the actual experimental result is 104 V, 122 V, 42 V, respectively. The experimental results are very close to the theoretical value, which verifies the correctness of the theoretical analysis. Additionally, there are lots of voltage spikes on the DC-link voltage in Fig. 16(b) and Fig. 17(b); this dues to the leakage inductance and its effect on the circuit, some measures will be explored to reduce it in the future.

In the case of the same turn ratio $n = 2$ and shoot-through duty cycle $D = 0.15$, the prototypes of the Trans-Z-source inverter and the Delta-source inverter are constructed, and some experiments are performed, the experimental results of the output voltage of phase A are shown in Fig. 18. Under this condition, the output phase voltage of the two inverters is 31.8 V or 25 V. Compared with the proposed Trans-quasi-Z-source inverter, the output phase voltage of the aforementioned two inverters is lower. It can be verified that the proposed inverter has the advantage of stronger boost ability, and it has potential advantages in the applications requiring higher boost voltage gain.

VIII. CONCLUSIONS

In this paper, a new type of Trans-quasi-Z-source inverter topology is introduced, which directly couples the DC side and the inverter side through a Trans-quasi-Z-source network to form a single-stage controllable voltage regulation inverter. Compared with the traditional inverters and the quasi-Z-source inverters, it achieves the single-stage buck-boost function that is lacking in the traditional inverters as well as overcoming the

defects of the modulation index and shoot-through duty cycle restrict each other in the quasi-Z-source inverters, and it has higher voltage gain than the traditional quasi-Z-source inverter. Due to the unique circuit structure of the Trans-quasi-Z-source inverter, it has broad application prospect in uninterruptible power supply, electric vehicle and photovoltaic power generation system. Research on this aspect will be carried out in the future work.

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