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SPECIAL ISSUE ON APPLICATIONS OF WIDE BANDGAP DEVICES

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Editorial for the Special Issue on Applications of Wide Bandgap Devices

THE emergence of wide bandgap (WBG) semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN) devices promises to revolutionize next-generation power electronics converters. Featuring high breakdown electric field, low specific on-resistance, fast switching speed, and high junction temperature capability, these devices are beneficial for the efficiency, power density, reliability, and/or cost of power electronics converters. WBG devices have been employed in some commercial and industrial products with more applications expected in near future. However, extremely fast switching and other superior characteristics of WBG device, and high switching frequency/high voltage/high junction temperature operation, present new design challenges in gate drive and protection, packaging and layout, EMI suppression, and converter control, etc. Addressing these design and application issues is critical to the adoption, commercialization, and success of WBG based power electronics. This special issue intends to report the latest progress in these important areas.

The Special Issue on Applications of Wide Bandgap Devices collected four papers on diverse topics, ranging from device performance degradation study, device gate drive and protection, to power module design, and eventually to sensing and control of converters in practical applications. The first paper is entitled "Performance Degradation of GaN HEMTs Under Accelerated Power Cycling Tests" written by Chi Xu and his colleagues at the University of Texas at Dallas, USA. This paper presents a comprehensive analysis of degradation performance in cascode and E-mode p-GaN gate devices under cyclic electrical and thermal stresses. The parametric variations show that the on-state resistance in both GaN device types gradually changes, which provides promising results as a degradation precursor. Furthermore, for the p-GaN gate device, the threshold voltage increases and transconductance decreases as the device ages, which offers an alternative degradation precursor. Failure analyses were also conducted on both devices. The cascode GaN devices show both short and open circuit failure modes, and a weak point in the drain-side bond wires is detected. For the p-GaN gate device, the electrical parameter shifts indicate a possible gate degradation after the device is aged.

The second paper on the "Highly Compact Isolated Gate Driver With Ultrafast Overcurrent Protection for 10 kV SiC MOSFETs" was contributed by Daniel Rothmund and his colleagues at the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland. A highly compact isolated gate driver with a 20 kV isolation voltage is implemented and tested in order to simplify the use of 10 kV high-voltage SiC devices for a future intelligent medium voltage SiC module. The gate driver utilizes an encapsulated isolation transformer for its isolated power supply. This transformer with its primary winding and the secondary winding wound on separate ferrite core halves and separated by silicone insulation material, shows a volume of only 3.1 cm^3 and a coupling capacitance of only 2.6 pF, and has been successfully tested at 20 kV dc. Furthermore, an ultrafast overcurrent protection (OCP) circuit is implemented to protect the expensive SiC module from destruction due to overcurrent. The OCP circuit reacts within 22 ns to a fault and measurements prove that it can successfully clear a hard switching fault (HSF) and even a flashover fault (FOF), where one of the two switches of a bridge-leg configuration is subject to a flashover, in less than 200 ns for a dc-link voltage of 7 kV.

The third paper contributed by Lei Li and his colleagues from the Chinese Academy of Sciences, China is "A 1200 V/200 A Half-bridge Power Module Based on Si IGBT/SiC MOSFET Hybrid Switch". In this paper, a compact hybrid switch (HyS) half-bridge power module, rated at 1200 V/200 A, was fabricated in house and fully tested for the first time. An electrothermal model of the HyS was set up to determine the optimal gate sequence for the HyS. To minimize the HyS power loss, the turn-on and turn-off timing sequences for the Si IGBTs and the SiC MOSFETs were discussed. And a novel index was proposed to select the optimal prior turn-off period. Compared with the pure Si IGBTs, the HyS module can operate at a higher switching frequency with a reduced power loss. A 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were developed and tested for verification.

The last paper is "Impacts of High Frequency, High di/dt, dv/dt Environment on Sensing Quality of GaN Based Converters and Their Mitigation" from Bo Liu and his colleagues from the University of Tennessee, Knoxville, USA. This paper has reported a common phenomenon from a GaN based battery charger design, i.e., the high switching frequency, and high di/dt and dv/dt noise inside GaN converters may induce a dc drift or low frequency distortion on sensing signals. It provided a systematic study on different sensing distortions and their mechanisms. The identified mechanisms of different errors are strongly impacted by di/dt, dv/dt and switching frequency, all related to undesired high frequency behaviors of different amplifiers. Practical noise minimization techniques from noise source, propagation-path, and receptor are developed and experimentally verified. These techniques can improve the sensing quality and minimize the influences on feedback control.

We would like to express our sincere thanks to the guest associate editors for their efforts spent selecting these high-quality papers for this Special Issue and the expert reviewers who have provided invaluable comments and inputs to assess and enrich the quality of the submitted manuscripts.

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Dr. Liu recently joins United Technologies Research Center, East Hartford, CT, as a Senior Design Engineer. He has authored or coauthored 40 journal and conference papers and a book chapter on GaN in AC/DC power converters. His research interests include wide bandgap device based high-frequency high-density converters for aircraft application, conducted EMI, power quality control, high power transmission system, power grid emulation, and grid-tied solar inverters.

Performance Degradation of GaN HEMTs Under Accelerated Power Cycling Tests

Chi Xu, Fei Yang, Enes Ugur, Shi Pu, and Bilal Akin

***Abstract*—In this paper, performance degradations of enhancement mode (E-mode) gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) under accelerated power cycling tests are presented. For this purpose, a DC power cycling setup is designed to accelerate the aging process in a realistic manner. In order to evaluate the aging-related parameter shifts and corresponding precursors, electrical parameters are periodically monitored through a high-end curve tracer. Both the cascode device and *p*-GaN gate GaN devices are evaluated during these tests. In the experimental results, it is observed that the on-state resistance gradually increases in both devices. Meanwhile, the threshold voltage of the *p*-GaN gate GaN device gradually increases over the aging cycles and a remarkable variation in the transfer characteristics is observed. At the end of the tests, failure analyses are conducted on both devices. The cascode GaN devices show both short and open circuit failure modes, and a weak point in the drain-side bond wires is detected. For the *p*-GaN gate GaN device, the electrical parameter shifts indicate a possible gate degradation after the device is aged.**

***Index Terms*—Aging precursor, failure analysis, failure mode, failure model, GaN device, power cycling.**

I. Introduction

GALLIUM nitride (GaN) devices are one of the most promising power devices in high frequency, high efficiency and high power density power conversions [1], [2]. Compared to Si and SiC counterparts, GaN high-electron-mobility transistors (HEMTs) exhibit a better figure of merit. The GaN HEMTs can be categorized into normally-on and normally-off devices [3]. Normally-on GaN device is less desirable in power converters due to its reliability concerns. For normally-off GaN devices, there are several methods to implement, including recessed Schottky gate, *p*-GaN gate, plasma treatment under the gate and cascode structure [4]. Among them, the cascode GaN and *p*-GaN gate GaN are mainly applied in commercially available GaN devices as shown in Fig. 1.

Both these types of GaN devices show different characteristics from the conventional Si devices. For cascode GaN devices, there are two primary heat sources, i.e., the GaN HEMT and Si MOSFET devices. These two devices are purposely overlapped in the stacked-die package to reduce the package related parasitics [5]. However, this makes it more difficult to dissipate the heat compared to the conventional design where each die sits on the base plate. On the other side, for E-mode GaN HEMTs, since there is no wire and die attachment compared to the conventional wire bond process [6]–[12], the common failure regarding package, such as bond-wire cracks, lift-off and die attachment delamination won't be observed. Hence it is quite necessary to study the reliability of these newly developed devices [13].

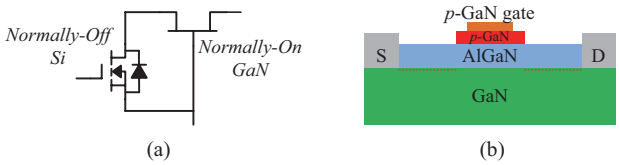

Fig. 1. Structure of GaN device: (a) Cascode GaN. (b) E-mode GaN.

Recent studies mainly focus on exerting stress directly on the device, including the high electric field, high temperature and high drain bias [14]–[18]. These stressors can result in current collapse [19], drain current degradation, threshold voltage shift and gate leakage current increase. To simulate the device's real operation in power converters, the device reliability under the power cycling test (PCT) is also studied. In [20], [21], the results show that the bond wire lift-off at the drain side of Cascode GaN (C-GaN) devices is the main cause of failure. In [22]–[24], both of the forward and reverse conduction operation modes of *p*-GaN gate GaN HEMTs are studied. There is no significant difference in the failure modes of these two operation conditions, and the common failure of the devices under test (DUTs) is solder delamination. In [20], similar results of *p*-GaN gate GaN devices are given, i.e., the solder joint delamination. However, comprehensive analysis of the static electrical parameter shifts throughout the aging process is not adequately addressed in the literature. This paper aims to evaluate the reliability of existing commercially available GaN devices by applying accelerated power cycling tests to mimic aging-related degradation. The investigation regarding the electrical parameters' change throughout the aging process is provided to identify the aging precursors, which can be used to prevent costly shutdowns and realize device condition monitoring.

The paper is organized as follows: in Section II, a power cycling test setup is designed and its operation principle is briefly discussed. With the proposed test setup, power cycling is implemented and the electrical parameter variations throughout the aging process are provided in Section III. In Section IV,

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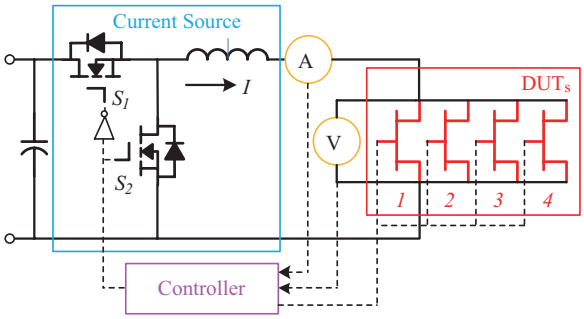

Fig. 2. Schematic overview of the accelerated aging test setup.

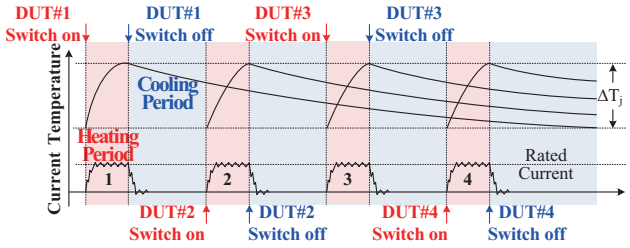

Fig. 3. Switching sequence of the test setup.

physical inspections are provided to investigate the causes of failures and discussions are given regarding parameter variations. Finally, the conclusions are provided in Section V summarizing the experimental results.

II. Accelerated Aging Test Setup

Power cycling test is commonly used to accelerate the aging process, which can trigger various failure mechanisms due to junction temperature swings, sheer stress, thermal expansion coefficient mismatch and enables aging precursors identification for health monitoring and lifetime estimation. In [22], a constant current is injected into the DUT by controlling a MOSFET. A bypass MOSFET is paralleled with the DUT branch for current free-wheeling. However, the current source is not fully used as it heats up the bypass MOSFET during the cooling period. To increase the utilization of the current source, a new power cycling test setup is designed to heat up all the DUTs sequentially.

The circuit diagram of the system is shown in Fig. 2, and it consists of five parts: a current source (CS), a DSP controller, a measurement board, a temperature controlled cold-plate and the DUTs. Among them, the output capacitor-less buck converter is applied as a current source for actively heating up the devices. Specifically, when one of the DUTs is turned on, S_2 is kept in off-state, and the duty cycle of high side switch S_1 is adjusted to regulate the load inductor's current to the rated current value of the DUT. The current value of the inductor is measured through a current sensor for feedback control. As the DUT is heated up by the inductor's current, the junction temperature is estimated through one of the temperature sensitive electrical parameters, i.e., the on-state resistance, which is calculated in real time with the measured drain-to-source voltage and the drain current. When the junction temperature of DUT reaches

TABLE I
Specification of Aging Test Setup

Item	Value
CS MOSFET	40 V/100 A
CS Inductor	40 μH
Maximum Junction Temperature	150 °C
Heat Sink Temperature	25 °C

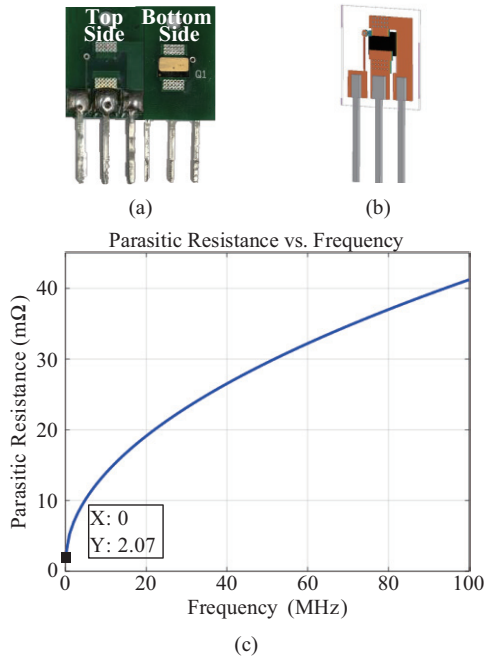

Fig. 4. TO-package adaptor: (a) PCB. (b) Q3D model. (c) Parasitics resistance vs. frequency.

the maximum temperature limit of 150 °C, the current is set to zero immediately. Here, the temperature is kept within SOA to avoid triggering unrealistic aging modes. When the inductor current becomes low, the DUT is turned off for cooling down to the cold plate temperature, i.e., 25 °C. The remaining small current ripple, as shown in Fig. 3, is dissipated by the output capacitance C_{oss} and the body diode of low side switch S_2. While cooling down the previous DUTs, the next DUT is heated up. The switching sequence is given in Fig. 3 and the detailed specifications are listed in TABLE I.

In order to measure the device's parameters on the curve tracer, a dedicated TO-247 PCB adaptor is designed as shown in Fig. 4(a). The adaptor model is imported to Ansys Q3D as shown in Fig. 4(b), and the added resistance of the PCB adaptor is simulated to be 2.07 mΩ at DC as indicated in Fig. 4(c). This value is negligible on the device's parameter measurement. Fig. 5 shows the system hardware and the devices with the adaptor mounted on the cold-plate are given in the zoomed-in box.

III. Parametric Analyses of Thermally Aged GaN Devices

In this study, 650 V cascode [25] and 650 V *p*-Gate gate

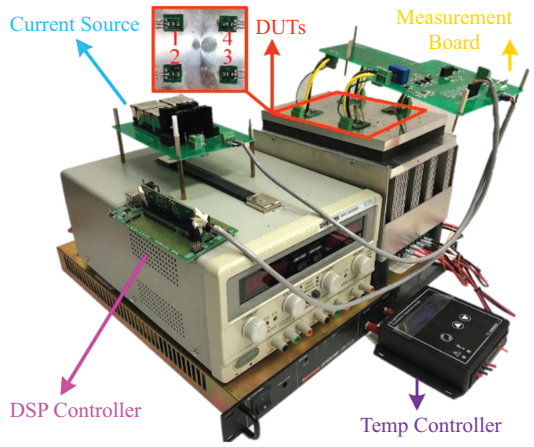

Fig. 5. Accelerated aging test setup hardware.

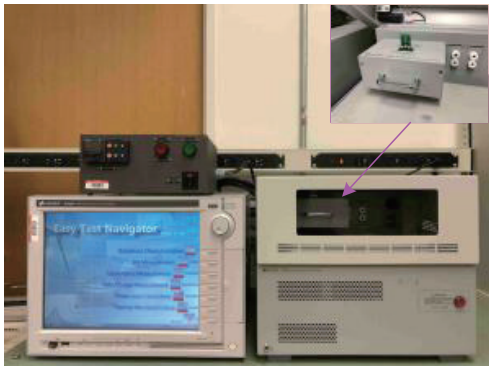

Fig. 6. Photo of the B1506A curve trace.

device [26] are used. The electrical parameters such as the gate-source leakage current I_{gss}, the drain-source leakage current I_{dss}, the threshold voltage V_{th}, the on-state resistance $R_{ds,on}$, the device capacitances (C_{iss}, C_{oss}, C_{rss}), the transfer characteristics (I_d-V_{gs}) and the output characteristics (I_d-V_{ds}), are periodically measured over the aging cycles with the Keysight B1506A curve tracer as shown in Fig. 6. In the following sections, the parameter shifts of each device are presented in detail.

A. Gate-to-Source Leakage Current I_{gss}

I_{gss} is measured by applying 15 V voltage on gate-source to the cascode GaN and 5 V voltage to the *p*-GaN device. The gate leakage current versus the number of power cycles is plotted for the cascode and *p*-GaN device respectively in Fig. 7(a) and (b).

Before the devices are aged, I_{gss} is very low, i.e., a maximum of 50 pA for cascode GaN and 50 μA for the *p*-GaN device. After certain aging process, I_{gss} of C-GaN 2, 3 and E-mode GaN (E-GaN) 2, 3 reach the compliance value of 1 mA. There is no gradual increase of I_{gss} before the device fails. Therefore, it is difficult to rely on the I_{gss} change as an aging precursor to predict the device's remaining useful lifetime. In fact, a high gate leakage current increase in the cascode GaN device suggests a failure in the Si MOSFET.

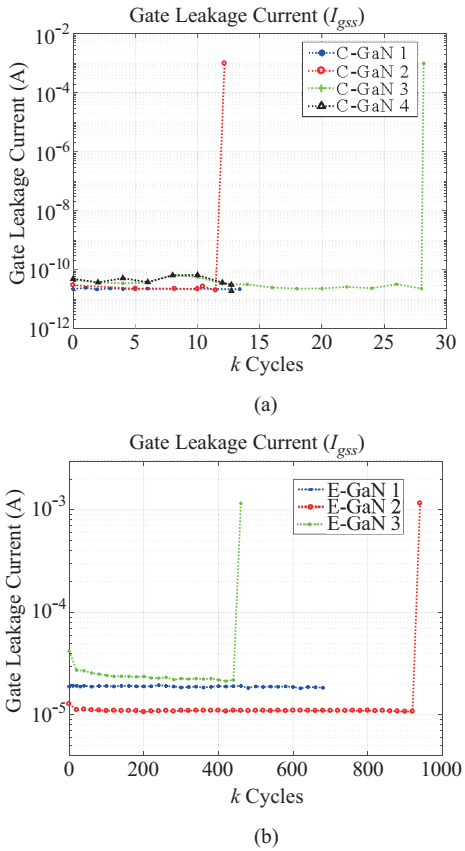

Fig. 7. Gate leakage current change during the aging process: (a) Cascode GaN. (b) E-mode GaN.

B. Drain-to-Source Leakage Current I_{dss}

I_{dss} is defined as the drain leakage current when the rated voltage is applied to the drain-source. As shown in Fig. 8, initially I_{dss} of cascode GaN and *p*-GaN device are also very low, i.e., a maximum of 40 μA for cascode GaN and less than 1 μA for the *p*-GaN device. Similar to the gate leakage current change, the I_{dss} of C-GaN 2, 3 reaches the compliance value of 400 μA and loses the blocking voltage ability. For the cascode device, since two devices are in series, it is necessary to decapsulate the device to find out the root cause of the failure, which is discussed later in the failure analysis.

For the *p*-GaN device, the leakage current of E-GaN 2, 3 reaches the compliance value of 40 μA after certain aging cycles and also loses the blocking ability. Similar to the gate leakage current, the drain leakage current does not gradually increase which makes it non-ideal for aging detections.

C. Threshold Voltage V_{th}

V_{th} is defined as the minimum gate-source voltage that is needed to create a drain current conducting between the drain and source terminals, i.e., 250 μA for cascode GaN and 7 mA for the *p*-GaN device. Fig. 9 gives the threshold voltage versus power cycles. For the new devices, the typical threshold voltage of the cascode GaN is 2.1 V. Before the devices fail, V_{th} doesn't change much for all cascode GaN devices.

On the other side, typical threshold voltage of the new *p*-GaN

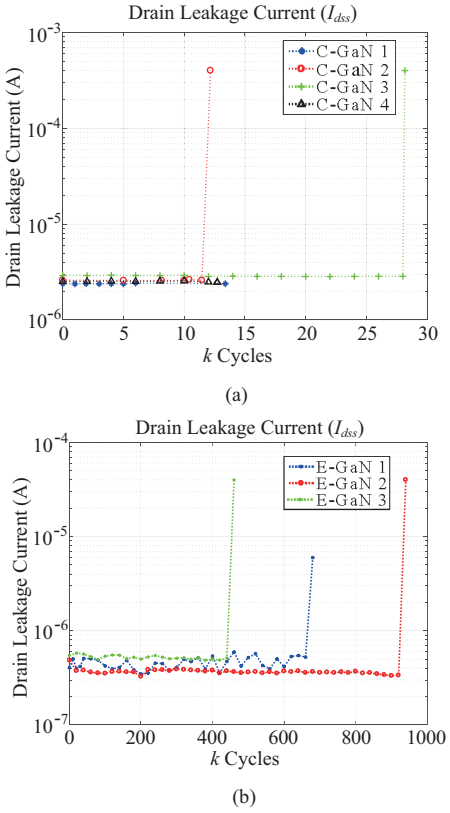

Fig. 8. Drain leakage current change during the aging process: (a) Cascode GaN. (b) E-mode GaN.

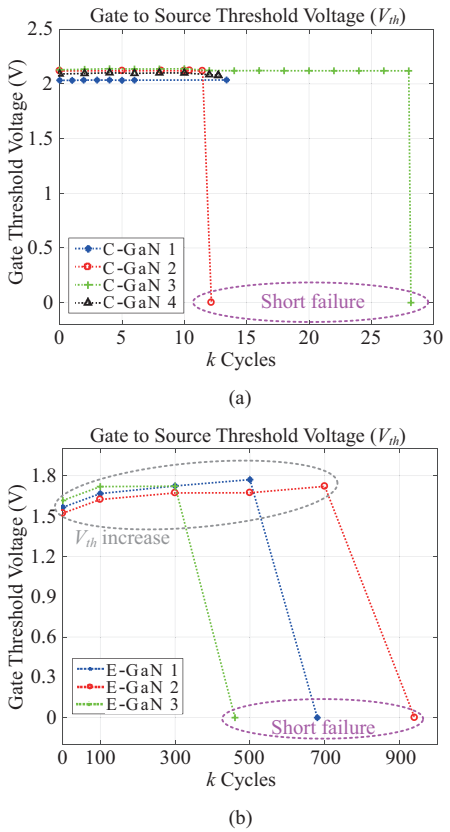

Fig. 9. Threshold voltage change during the aging process: (a) Cascode GaN. (b) E-mode GaN.

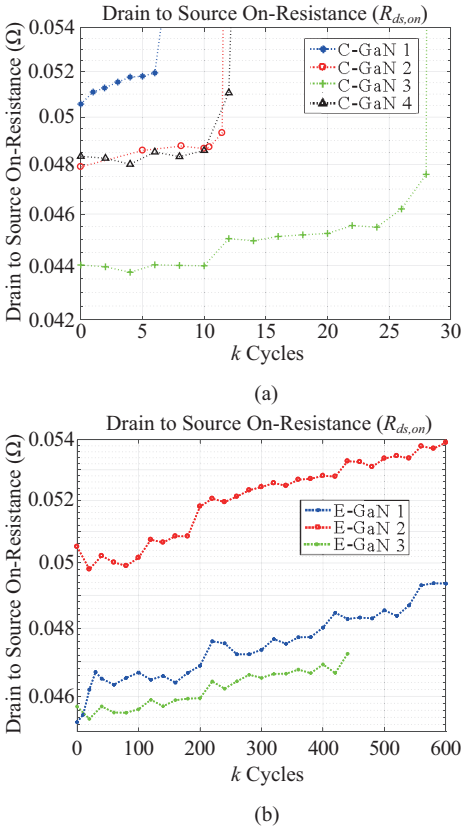

Fig. 10. On-state resistance change with respect to power cycles: (a) Cascode GaN. (b) E-mode GaN.

devices is around 1.5 V. V_{th} increases for all p-GaN devices during the aging process and the maximum increase of V_{th} is by 20%. As can be seen in Fig. 9(b), the incremental increase in V_{th} makes it a good candidate for aging detections. The threshold voltage increase can potentially be caused by the traps under the gate and the AlGaN/GaN interface layer as the device is aged [27]. After the devices lose the blocking capability, a large drain leakage current is observed and the threshold voltage drops significantly.

D. On-State Resistance $R_{ds,on}$

The on-state resistance $R_{ds,on}$ versus power cycles is shown in Fig. 10. It is observed that $R_{ds,on}$ curves for both cascode GaN and p-GaN devices increase gradually. The maximum increase of $R_{ds,on}$ for these two types of devices are about 8% and 10% compared to the initial values.

To find out the cause of the on-resistance variation toward the end of the lifetime, the on-resistance differences between the healthy and aged conditions for C-GaN 3 and E-GaN 2 are displayed in Fig. 11 under different gate-source voltages. As can be seen, the $\Delta R_{ds,on}$ of cascode GaN device does not change too much with the V_{gs}. This implies that the on-resistance change is not caused by the channel resistance degradation. It is suspected that the on-resistance increase is mainly due to the package related degradations. However, for the p-GaN device, the $\Delta R_{ds,on}$ increases significantly as V_{gs} is reduced. Therefore, it is concluded that the channel resistance mainly contributes to this

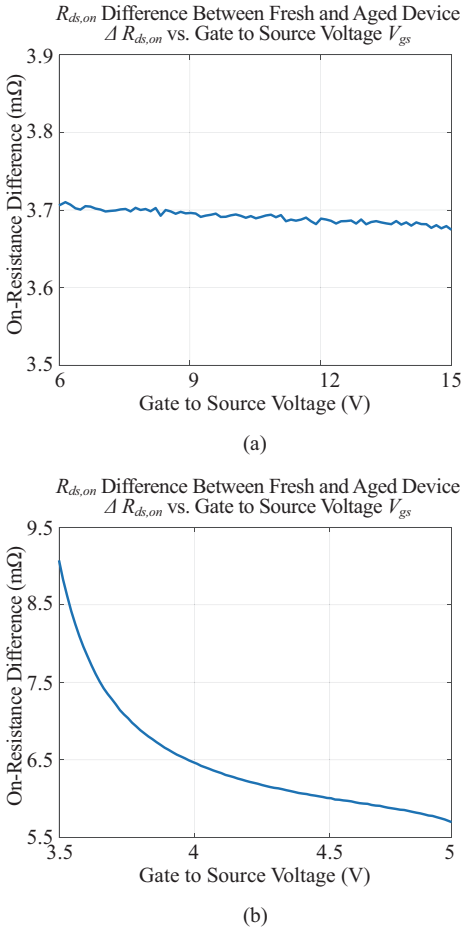

Fig. 11. On-resistance difference between fresh and aged device vs. gate to source voltage: (a) C-GaN 3. (b) E-GaN 2.

on-resistance increase as the *p*-GaN device is aged.

From the experimental results, the on-state resistance is found to be a good candidate for health condition monitoring as it changes gradually, especially for the *p*-GaN device.

E. Device Capacitances: C_{iss}, C_{oss}, C_{rss}

Since all the tested cascode GaN devices exhibit a similar result regarding the capacitance, only the input capacitance C_{iss}, the output capacitance C_{oss} and the reverse transfer capacitance C_{rss} of the C-GaN 3 throughout the power cycles are given in Fig. 12(a). As can be seen, no significant change is observed. Similarly, the *p*-GaN devices show little change on the capacitances except there is only a slight decrease of C_{rss} as shown in Fig. 12(b).

F. Transfer Characteristics I_d-V_{gs}

Fig. 13 and Fig. 14 illustrate the I_d-V_{gs} curve of the C-GaN 3 and E-GaN 2 respectively with respect to the number of power cycles. The transconductance $g_m = \frac{\Delta I_d}{\Delta v_{gs}}$ is derived from the curves.

As can be seen from Fig. 13, there is little change in the transfer characteristics and transconductance of the cascode GaN device. However, for the *p*-GaN device, a shift of transfer curve

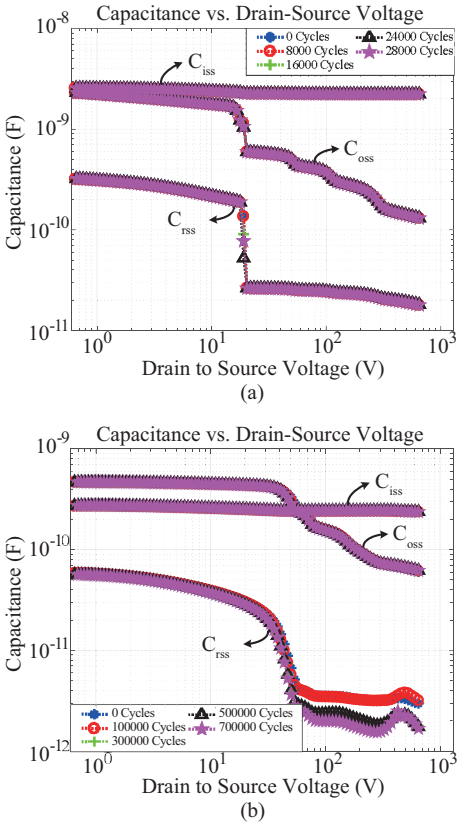

Fig. 12. Device capacitance change during power cycles: (a) Cascode GaN. (b) E-mode GaN.

is observed as the device is aged as shown in Fig. 14(b). It is also found that the transconductance g_m is gradually decreasing during the aging process. For the *p*-GaN devices, the theoretical equation for I_d-V_{ds} in the saturation region is given as:

$$I_d = K(V_{gs} - V_{th})^2 \tag{1}$$

Where K depends on the device dimension and mobility. The variation of K and V_{th} can be derived by fitting the transfer characteristics curve with the equation

$$y = K(x - V_{th})^2 \tag{2}$$

TABLE II summarizes the change of K and V_{th} at different numbers of aging cycles. It can be seen that the threshold voltage increases and K decreases during the aging process. Since the device's dimension does not change so much, the decrease in K suggests that the electron mobility decreases during the power cycle test. The decrease in mobility can potentially be caused by the trapped electrons as the device is aged.

G. Output Characteristics I_d-V_{ds}

The output characteristics are defined as the relation between the drain current and drain-source voltage. Fig. 15 gives the I_d-V_{ds} curves of C-GaN 3 and E-GaN 2 with respect to the power

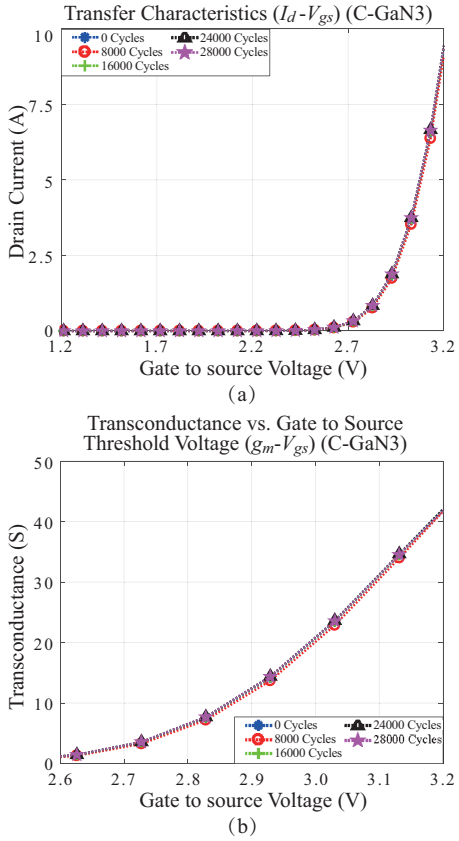

Fig. 13. Transfer characteristics and g_m curves of C-GaN 3 with respect to gate to source voltage: (a) Transfer characteristics. (b) g_m vs. V_{gs}.

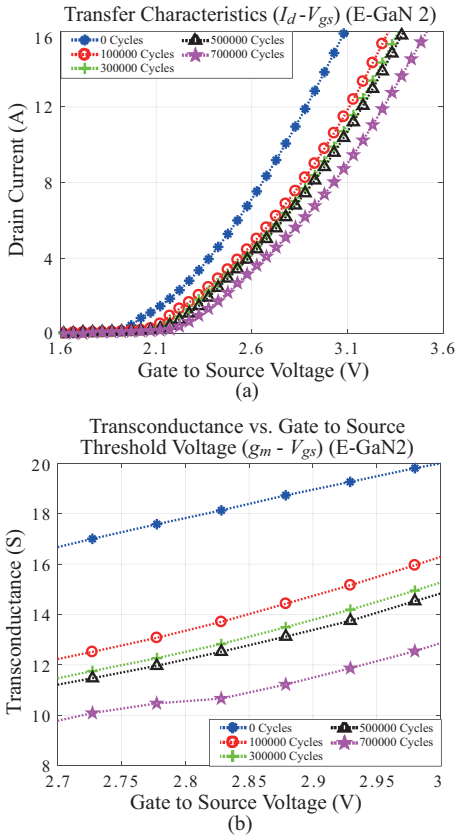

Fig. 14. Transfer characteristics and g_m curves of E-GaN 2 with respect to gate to source voltage: (a) Transfer characteristics. (b) g_m vs. V_{gs}.

TABLE II
I_d-V_{gs} OF E-GAN CURVE FITTING PARAMETERS

Cycles	K	V_{TH}
0	8.164	1.674
10k	6.308	1.737
30k	6.035	1.754
50k	6.005	1.772
70k	5.196	1.799

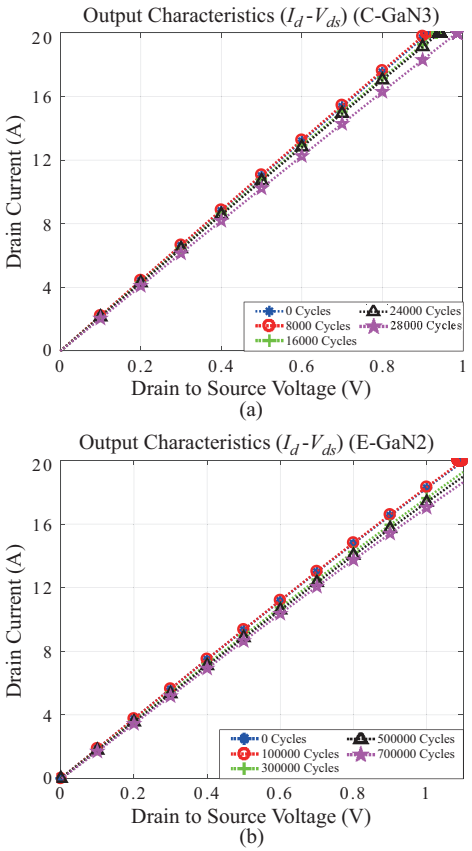

Fig. 15. Output characteristics curve with respect to power cycles: (a) Cascode GaN. (b) E-mode GaN.

cycles. Both types of GaN devices show a noticeable shift as the devices age. Specifically, for the *p*-GaN device, the theoretical equation for I_d-V_{ds} in the triode region is given as:

$$I_d = K[2(V_{gs} - V_{TH})V_{ds} - V_{ds}^2] \tag{3}$$

As summarized previously in TABLE II, the threshold voltage increases and K decreases as the device is aged. Consequently, the I-V curve tends to shift to the right according to (3).

IV. FAILURE ANALYSIS

A. Cascode GaN Devices

The failure modes of the C-GaN devices are summarized

TABLE III
FAILURE MODES OF C-GAN

Device	Failure mode
C-GaN 1	Doubled on-state resistance
C-GaN 2, 3	High gate-source and drain-source leakage current
C-GaN 4	Open circuit

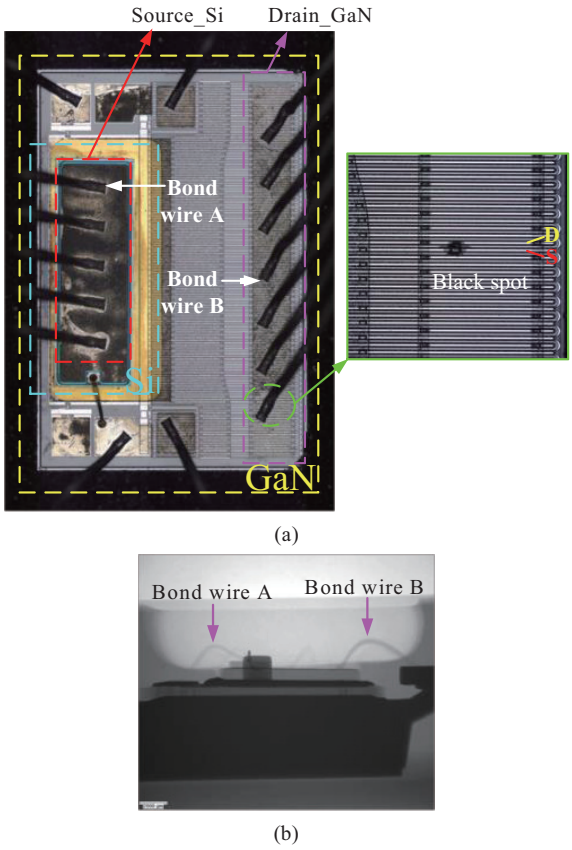

Fig. 16. Microscope and X-Ray image of the C-GaN 2: (a) Microscope. (b) X-Ray.

in TABLE III. In order to have a better understanding of the aging root cause, a detailed failure analysis (FA) has been carried out. Although the devices are initially inspected with non-destructive analysis methods like Scanning Acoustic Microscopy (SAM) and X-Ray, these methods did not reveal useful FA information due to the device. However, these images were used to understand the physical structure of the device. Then, the devices are inspected through destructive analysis in order to find the physical failure mechanism evidence. For destructive analysis, the devices are partially decapsulated with a rectangular shape cavity using laser ablation. This process decreases total decapsulation time dramatically and provides a cleaner decapsulation shape. After laser ablation, devices are decapsulated using H_2SO_4 (sulfuric acid) at 120 °C. After decapsulation, optical inspections are carried out with 5x and 20x microscope lenses.

Fig. 16 shows the die picture of C-GaN 2 after decapsulation. As shown in the zoom-in box at the right side given in Fig.16,

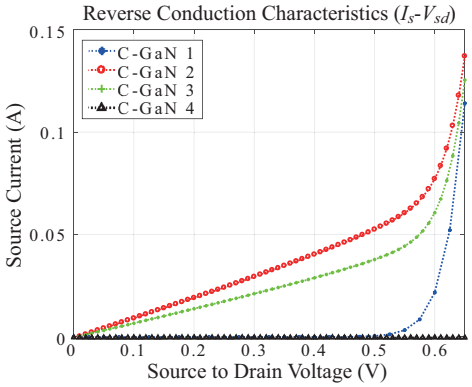

Fig. 17. Reverse conduction characteristics of GaN devices after aging.

Fig. 18. Reverse conduction path.

after removing the bond wires on the drain side of C-GaN, a black spot is detected optically in the die's surface. This black spot forms a short circuit in the GaN contacts, which can lead to the device short-circuit failure.

The reverse conduction characteristics of the C-GaN devices are compared in Fig. 17. As can be seen, C-GaN 2 and C-GaN 3 show a different feature compared to the typical aging results in the literature [7].

Typically, the voltage comprises two parts in the reverse conduction path as plotted in Fig. 18. One is the diode forward voltage drop, and the other one is the path resistance which includes the resistance of depletion mode GaN HEMT and the parasitic resistance. In the healthy devices, the reverse current starts to increase after the source-drain voltage V_{sd} exceeds the body diode voltage drop V_F. However, for C-GaN 2 and C-GaN 3 devices, the current start increasing before V_{sd} exceeds V_F. It suggests a degradation in the Si MOSFET's body diode.

To verify this assumption, the stacked two dies (Si MOSFET on top of the GaN device) are then detached to check the state of each device. The measurement shows that there is a large leakage current between gate to drain and gate to source of the Si MOSFET, and this degradation in the Si MOSFETs leads to different reverse conduction characteristics of the C-GaN devices.

For the C-GaN 4 device, an open circuit failure is observed. To find out the reason, the device is decapsulated and the surface picture is shown in Fig. 19. It is observed that all the bond wires connecting the drain-side of the GaN device and the lead are lifted off. Hence, an open circuit occurs. From the tested devices, the drain-side bond wire connection is found as one of the weak points.

B. E-Mode GaN Device

From the parameter variation shown in Section III, all three devices show a high drain-source leakage current. The E-mode GaN device degradation is mainly caused by the I_{dss} failure, which is also observed in [24]. The degradation of the GaN

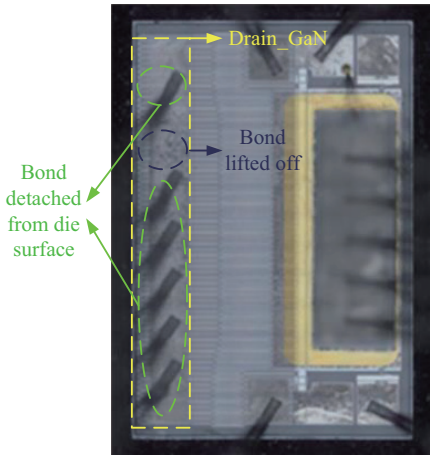

Fig. 19. Microscope image of the C-GaN 4.

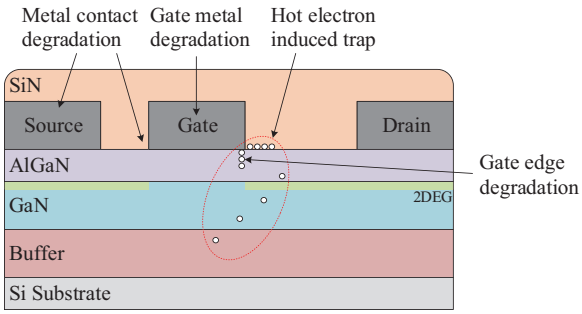

Fig. 20. GaN failure mechanism.

TABLE IV
ELECTRICAL PARAMETERS VARIATION IN DIFFERENT FAILURE MECHANISMS

		$R_{ds,on}$	V_{th}	C_{rss}	V_{bv}
GaN-related failure mechanisms	Gate-edge degradation	✓	✓	✓	✓
	Trap generation due to the electro-thermo-mechanical failure	✓	✓	✓	✓
	Punch-through effect in high drain-source conditions	✓	✓	×	✓
Thermally activated failure mechanisms	Feed metal interconnect degradation	✓	×	×	×
	Ohmic contacts degradation	✓	×	×	×
	Gate metal degradation	✓	✓	×	×
	Delamination of passivation SiN	✓	×	✓	✓

device is caused by several mechanisms and can be mainly divided into three groups, i.e., hot electron induced failure mechanisms, GaN-related failure mechanisms, and thermally activated failure mechanisms as illustrated in Fig. 20 [28].

Since the hot electron generation is not severe in the power cycling test, only the other two mechanism impacts on the device electrical characteristics are listed in TABLE IV. As measured in the curve tracer, the aged device shows an increase in threshold voltage and a decrease in the breakdown voltage V_{bv}. The reason for this change can be the gate degradation due to thermal stress. The gate edge degradation can affect the threshold voltage and reshape the electric field distribution, which can cause the decrease of the breakdown voltage.

V. CONSLUSION

This paper presents a comprehensive analysis of degradation performance in cascode and E-mode *p*-GaN gate devices under cyclic electrical and thermal stresses. The parametric variations show that the on-state resistance in both GaN device types gradually changes, which provides promising results as a degradation precursor. Furthermore, for the *p*-GaN gate device, the threshold voltage increases and transconductance decreases as the device is aged, which offers an alternative degradation precursor. From the analysis of cascode GaN device, the results demonstrate that some of the devices show short circuit characteristic between gate-source and drain-source ports. By decapsulating the devices and detaching the dies, it is found that both of the dies exhibit short circuit characteristic. Besides, the failure analysis shows that the bond wire connecting the drain pad of the GaN die and the drain lead is a weak point in this device. For the *p*-GaN gate device, the anticipated reason is related to gate degradation, which can cause an increase in the gate threshold voltage and reduce the breakdown voltage.

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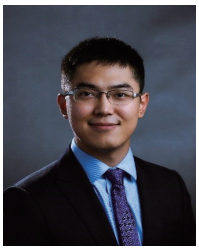

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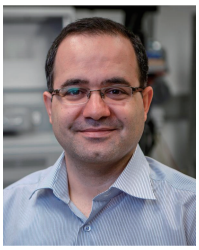

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Highly Compact Isolated Gate Driver With Ultrafast Overcurrent Protection for 10 kV SiC MOSFETs

Daniel Rothmund, Dominik Bortis, and Johann W. Kolar

***Abstract*—Silicon Carbide (SiC) semiconductor technology offers the possibility to manufacture power devices with unprecedented blocking voltages in the range of 10…15 kV and superior switching characteristics, enabling switching frequencies beyond 100 kHz. To drive these 10 kV SiC devices, the power supply and the gate signal of the (high-side) gate driver require an appropriate galvanic isolation featuring a low coupling capacitance and a high du/dt ruggedness. Since at the moment no commercially available gate drivers for these specifications exist, a customized isolated gate driver is developed, which, in order to simplify the use of the high-voltage SiC devices, is intended to be integrated into a future intelligent MV SiC module. For this purpose, a highly compact isolated gate driver with an isolation voltage rating of 20 kV is implemented and tested. The realized isolation transformer of the isolated power supply shows a volume of only 3.1 cm^3 and a coupling capacitance of only 2.6 pF, and has been successfully tested at 20 kV DC. Furthermore, an ultrafast overcurrent protection (OCP) circuit is implemented to protect the expensive SiC modules from destruction due to overcurrents, which e.g. could result from false turn-on of both transistors of a bridge-leg or from short circuits of the load. The OCP circuit reacts within 22 ns to a fault and measurements prove that it can successfully clear both, a hard switching fault (HSF) and even a flashover fault (FOF), where one of the two switches of a bridge-leg configuration is subject to a flashover, in less than 200 ns for a DC-link voltage of 7 kV.**

***Index Terms*—10 kV SiC MOSFET, isolated gate driver, isolation transformer, overcurrent protection, short circuit.**

I. Introduction

MEDIUM-VOLTAGE (MV) SiC devices with blocking voltages of 10…15 kV have gained significant interest in the recent years [1]–[9], since they enable the simplification of MV-connected power electronics by reducing the number of switches and associated isolated gate drivers compared to modular MV converters based on lower voltage devices [10], [11]. Therefore, possible applications for MV SiC MOSFETs and IGBTs are, besides HVDC, e.g. Solid-State Transformers (SSTs) for future data center power supplies [12]–[14], high-power electric vehicle battery charging facilities [15], [16], traction applications [17], [18], naval or marine on-board MV-AC or MV-DC distribution systems [19], [20] or even future all-electric aircrafts [21]. However, these MV SiC devices such as the one shown in Fig. 1 feature extremely fast switching speeds with dv/dt values of up to 100 kV/µs and, in the case of SiC MOSFETs, extremely low soft-switching losses, which allow switching frequencies beyond 100 kHz for DC link voltages in the 5…10 kV range [22]. Consequently, standard isolated gate driver ICs as well as standard isolated gate driver power supplies and optocouplers are not applicable for the power and signal transmission to the high-side switches, since their isolation voltage rating and dv/dt ruggedness are not sufficient. For these reasons, a customized gate driver circuit with a very low coupling capacitance, an isolation voltage in the range of 20 kV for the signal and the power path, and a high dv/dt ruggedness is required to guarantee a reliable operation. Furthermore, in case of a fault, an overcurrent protection (OCP) circuit for the highly expensive SiC devices is desired.

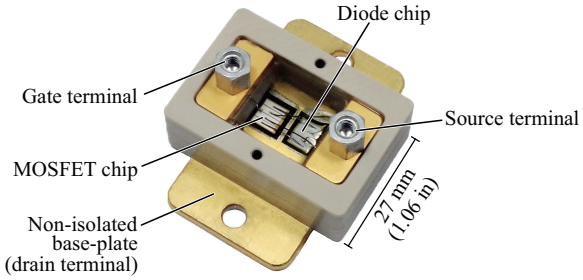

Fig. 1. Basic non-isolated 10 kV SiC module containing a MOSFET chip and an antiparallel SiC JBS diode chip [23], [24].

Concerning the electrical performance, the isolated gate driver should in future be integrated into the SiC module, since this enables a reduction of the gate loop inductance and/or enhances the switching performance of the SiC MOSFET, as it is already reported for 650 V GaN and 1200 V SiC devices [25]–[27]. Moreover, the integration of the isolated gate driver and the OCP into an MV SiC module allows to significantly simplify the design process of MV converters, since the high voltages then only occur at the power terminals of the module, whereas the gate signals and the auxiliary power can be supplied to the module without any additional external isolation measures. Besides the simplification of the MV converter design, this also allows a substantial increase of the MV converter power density, especially by avoiding the large required creepage and clearance distances in air, which can be minimized using a proper insulation material in the isolation transformer and an

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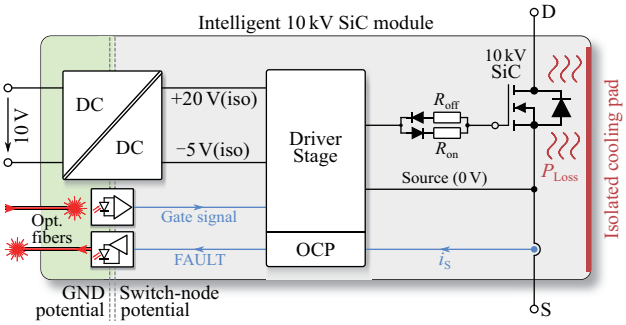

Fig. 2. Concept of a future intelligent 10 kV SiC module which also contains the isolated DC/DC converter for the supply of the (high-side) gate driver stage and a fiber optic receiver for the gate signal. Furthermore, an overcurrent protection (OCP) circuit is integrated, which in case of a fault safely turns off the MOSFET and sends an optically isolated FAULT signal to the supervisory control.

according insulation coordination. Furthermore, in the case of multi-level converters where the auxiliary power is e.g. drawn from the submodule capacitors [28], the integrated isolated power supply can significantly reduce the complexity of the required external auxiliary power supply circuitry.

Fig. 2 shows a schematic drawing of a possible future intelligent 10 kV SiC MOSFET module featuring an integrated isolated DC/DC converter for the generation of the +20 V/−5 V driving voltages, a fiber optic receiver and transmitter for the reception of the gate signal and the transmission of the FAULT signal, and the driver stage with an OCP circuit, which measures the device current and safely turns off the MOSFET in case of a fault. Advantageously, the heat is extracted via an isolated cooling pad, which could be realized with e.g. an aluminum nitride plate featuring a high thermal conductivity while at the same time providing electrical insulation. For the integration of the gate driver, the individual components must be highly compact, which is especially important for the isolated power supply, since the gate driver volume is mainly defined by the volume of the isolation transformer. Consequently, the volume of the isolation transformer V_{trans} has to be minimized, which is one of the main objectives of the following considerations.

In literature, most commonly air or tape-insulated transformers with discrete windings [29]–[34] or PCB windings [35] are used to isolate the power supplies of gate drivers employed in MV SiC applications. In some cases however, these transformers are up to 10 times larger than the 10 kV SiC module shown in Fig. 1. This can be explained by the large creepage distances required in air (40 mm for 10 kV according to the International Standard IEC 60950-1 [36]). Furthermore, these isolation transformers must be placed in safe distance from other converter circuit components in order to not risk creepage currents, partial discharges or even dielectric breakdowns. In [37] a relatively compact current-transformer-based solution with a common AC-bus has been presented and is intended for the supply of several gate drivers at the same time.

Another possibility to realize the galvanically isolated gate driver power supply is to use inductive power transfer (IPT) coils [38]–[41]. However, since the electric breakdown field strength of air is comparably small, a large air gap and large creepage paths are necessary, i.e. the overall IPT system will be large and hence is not suited for an integration in a highly compact module.

A further method to supply electric energy to a floating gate driver circuit is to use an optical fiber [42]. Thereby, a powerful laser (e.g. 3…10 W optical power) feeds an optical fiber, which is connected to the laser receiver on the gate driver side converting the laser power back into electric energy. The advantage of this concept is the theoretically infinite dv/dt immunity, since apart from the remaining intrinsic capacitance of the physical components, the coupling capacitance of the optical fiber is basically zero. Furthermore, no creepage distances to the laser receiver are required, such that compact gate driver circuits could be realized with this concept. However, it has to be mentioned that the laser transmitter is very large (e.g. 220 mm × 197 mm × 143 mm (8.66 in × 7.75 in × 5.63 in) for 3…20 W optical power, cf. [43]) and thus is difficult to accommodate. The low receiver efficiency of only 25% and the high costs are further disadvantages.

Therefore, a highly compact and cost-effective solution for the galvanically isolated power supply of the high-side gate driver circuits for 10…15 kV SiC MOSFETs must be developed, which could be integrated in a future intelligent MV SiC power module.

Furthermore, the gate driver circuit should be equipped with an OCP in order to protect the 10 kV SiC devices (*Wolfspeed CPM3-10000-0350*) from destruction due to overcurrents and/or short circuits. A typical fault scenario is the shoot-through of a bridge-leg configuration, i.e. both switches are erroneously turned on, e.g. due to incorrect or distorted gate signals. For the switch turning on while the complementary switch is already in on-state, this type of fault is called hard switching fault (HSF). In contrast, the switch which is already in the on-state experiences a so-called fault under load (FUL) [44], [45]. However, in MV applications, faults due to isolation and/or flashover failures are especially critical due to their extremely fast transients. These so-called flashover faults (FOF) are much more challenging to handle, and to also protect the MV SiC MOSFETs in this worst-case scenario, an OCP with FOF clearing capabilities is developed.

The most common method for the implementation of an OCP is a desaturation detection circuit, which measures the device on-state voltage and compares it to a certain threshold voltage [42]. However, since during the turn-on transition a large blanking time is required until the device is in full on-state, the fault detection time is relatively high and potentially hazardous for the 10 kV SiC devices due to the high instantaneous power dissipation in the chip during e.g. an FOF. Furthermore, the drain voltage has to be sensed and blocked by several series-connected diodes, which have to be separated from the rest of the gate driver circuit by a certain creepage distance, which increases the gate driver volume [46]. As an alternative, the current could be measured with a shunt in the source path, or, if a Kelvin source contact is available (which is not the case for the 10 kV SiC modules at hand, cf. Fig. 1), the voltage

drop across the parasitic inductance between Kelvin source and power source can be measured and integrated to obtain the device current [47]. Unfortunately, both methods do not offer galvanic isolation, which potentially could lead to undesired CM distortions due to the extremely fast fault transients. Alternatively, the device current could be measured galvanically isolated with a Rogowski coil [48], which is, however, sensitive to external electric and magnetic fields and could therefore lead to false triggering.

In order to avoid the disadvantages of the mentioned OCP methods and to ensure a highly robust and fast protection, an air-gapped current transformer in the source path of the MOSFET is used, which features galvanic isolation, a high bandwidth, and does not require a connection to the drain potential. The measured current is subsequently processed by a high-speed analog circuit, which reacts to a fault within 22 ns and safely turns off the device.

In the following, first the galvanically isolated power supply and the realization of the isolation transformer with minimum volume and coupling capacitance will be discussed (Section II). Subsequently, the ultrafast OCP circuit is described in Section III and it is experimentally proven that it is able to safely clear both, an FOF and a HSF for a DC-link voltage of 7 kV. Finally, conclusions of the main findings are drawn in Section IV.

II. The Isolated Power Supply

The isolated power supply has to provide electric energy to the driver circuit of the power MOSFET, which in the case of the high-side switch is referenced to the switch-node potential, i.e., in the case of 10 kV SiC MOSFETs to a floating rectangular voltage of e.g. 7 kV with a frequency of > 100 kHz, and dv/dt values of up to 100 kV/µs. Therefore, besides providing the isolated +20 V/−5 V driving voltages, the power supply needs to feature a sufficient electrical isolation voltage rating. Furthermore, the common-mode (CM) currents through the parasitic isolation transformer coupling capacitance C_{CM} must be kept sufficiently low in order not to disturb the proper operation of the gate driver and the protection circuits. Commercially available isolated power supplies, e.g. for 3.3 kV and 6.5 kV IGBTs, feature coupling capacitances in the range of 20…25 pF and a size of typically 50 mm × 50 mm × 20 mm [49], [50], whereby MV IGBTs are switching with rather low dv/dt values in the range of 10 kV/µs [51], which is 10 times slower than in the case of 10 kV SiC MOSFETs. Consequently, in a 10 kV SiC MOSFET-based converter, C_{CM} must be reduced by roughly a factor of 10 in order to keep the peak CM current in the same range as in an Si IGBT-based converter. Although there are devices such as [52] featuring an insulation voltage of 12 kV (for one minute) and a coupling capacitance of only 3 pF, the actual allowed operating voltage according to [36] is only 7.2 kV and due to the missing dv/dt and CM frequency ratings, also these devices are unsuitable for MV SiC MOSFET applications. Therefore, a customized isolated power supply featuring appropriate insulation ratings has to be realized. However, with standard isolation transformer designs, a low coupling capacitance can only be realized by large distances between the windings and between the windings and core, whereas on the other hand a significant downsizing is necessary for the integration of the transformer (cf. Fig. 2). To achieve both, a special transformer concept must be developed (cf. Section II-B).

TABLE I
Specification of the Isolated Power Supply

Property	Symbol	Value
Output voltages	U_{DC1} , U_{DC2}	+20 V , − 5 V
Max. output power	P_{max}	2 W
Max. coupling capacitance	$C_{CM,max}$	3 pF
Isolation voltage	U_{iso}	20 kV

The power consumption of the gate driver circuit at hand is 600 mW at most during operation (including the optical fiber transceivers). In order to provide a sufficiently large margin (e.g. if several 10 kV SiC MOSFETs should be operated in parallel), the isolated power supply is rated for a power of P_{max} = 2 W. TABLE I lists the specifications of the power supply as a basis for the design.

A. Isolated Power Supply Topology

Due to the high isolation voltage requirement of 20 kV, a certain isolation distance is required between the transformers' primary and secondary windings. Consequently, a comparably low magnetic coupling factor k and hence a relatively large leakage inductance results, which, if not compensated, leads to a load-dependent voltage drop and hence to a load-dependent output voltage of the gate driver supply. To still obtain a stable secondary-side voltage, a feedback-control would be necessary, which would, however, require an isolated transmission of the measured output voltage signal across the isolation barrier, i.e. additional effort which would further increase the risk of failure of the supply.

To overcome this problem, a topology with a load-independent voltage transfer ratio, namely the series-series compensated resonant converter shown in Fig. 3 is selected. It consists of an H-bridge inverter, a 1 : 1 isolation transformer (i.e. $L_p = L_s$), the resonance capacitors C_{r1} and C_{r2}, and a voltage doubler rectifier generating 20 V DC for the positive gate bias of the 10 kV SiC MOSFET. Thereby, the transformer leakage inductance is compensated by the resonance capacitors and the system is operated at the unity-gain operating point where the output voltage is independent of the load [53]. Furthermore, soft-switching of the primary-side full-bridge (realized with a *MAX13256* IC) can be achieved, enabling a high switching frequency and therefore a more compact design. Furthermore, in this operating point, the transformer currents are sinusoidal and hence beneficial in terms of low high-frequency (HF) losses due to skin-effect and proximity-effect, since no higher current harmonics are present.

According to [53], if only the resistances of the primary and the secondary windings are considered, the highest efficiency (i.e. the lowest rms currents) of the resonant system is achieved when the impedance of the secondary-side is matched to the load impedance. For a maximum output power of P_{max} = 2 W, a given secondary-side inductance L_s and a secondary-side

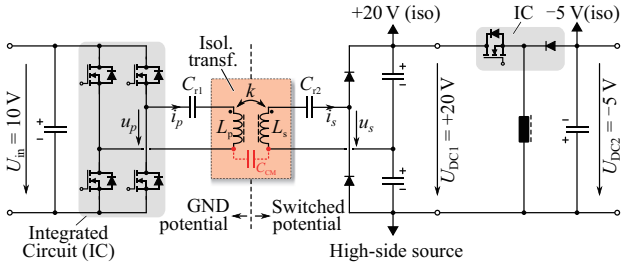

Fig. 3. Schematic diagram of the isolated power supply. The isolation transformer is operated in a series-series compensated configuration whereby $L_p = L_s$ and $C_{r1} = C_{r2}$. The subsequent voltage doubler rectifier generates +20 V DC, from where a buck-boost converter generates −5 V DC, which is used for the supply of the analog and logic ICs as well as for the negative biasing of the gate in the off-state of the 10 kV SiC MOSFET.

voltage of $u_s = U_{DC1}/2 = 10$ V (half the DC output voltage U_{DC1} due to the voltage doubler rectifier, cf. Fig. 3), the optimum operating frequency f_0 in order to fulfill the load matching condition at full load is given as

$$f_0 = \frac{8}{\pi^2} \cdot \frac{u_s^2}{2\pi\sqrt{2}\, L_s k P_{max}}, \tag{1}$$

with k as magnetic coupling factor between the transformer's primary-side and secondary-side. To achieve a load-independent voltage transfer ratio, the resonance capacitors have to be dimensioned as [53]:

$$C_{r1} = C_{r2} = \frac{1}{(2\pi f_0)^2 L_s (1-k)}. \tag{2}$$

In this operating point (which is slightly above the resonance), the phase angle of the input impedance seen by the full-bridge is

$$\varphi(Z_{in}) = \arctan(\sqrt{2}) = 54.7° \tag{3}$$

and hence guarantees ZVS operation of the MOSFETs due to the inductive behavior [53]. Furthermore, due to this particular compensation method, the primary-side rms current is independent of the inductances, the magnetic coupling, and the operating frequency, and can be calculated as

$$i_{p,rms} = \sqrt{\frac{3}{8}} \cdot \pi \cdot \frac{P_{max}}{u_s} = 384\,\text{mA}. \tag{4}$$

The secondary-side current is ideally in phase to the rectangular voltage applied from the rectifier and its rms value can be calculated as

$$i_{s,rms} = \frac{P_{max}}{u_s} \cdot \frac{\pi}{2\sqrt{2}} = 222\ \text{mA}. \tag{5}$$

B. Isolation Transformer

In conventional isolation transformers, the primary and the secondary windings are placed on the same magnetic core and are galvanically isolated from each other by means of insulation material between the primary winding and the core, the secondary winding and the core, and between the primary and secondary windings. In the case of the application at hand, the differential mode voltage applied to both transformer windings is < 50 V and hence, no further isolation between the primary winding and the core (which in this case would be tied to GND potential) would be necessary. However, the secondary winding would have to be isolated from both, the core and the primary winding since it is floating on the switched potential of e.g. 7 kV. Consequently, the winding window and therewith the size of the entire magnetic core has to be chosen sufficiently large, such that the secondary winding can be separated from the core and from the primary winding by approximately 1.6 mm of insulation material thickness to each side, if an (average) electric field strength of 4.5 kV/mm is allowed and the transformer is potted in a suitable insulation material. Since the transformer's power rating is only $P = 2$ W but the isolation distances do not scale with the power but are defined by the isolation voltage, the required winding window would be large compared to the dimensions of a typical 2 W HF transformer without MV isolation and hence, this transformer concept is not suitable for achieving a low volume.

To overcome this limitation and to minimize the volume of the isolation transformer, as many isolation barriers as possible have to be omitted. Therefore, the primary winding and the secondary winding are wound on separate ferrite E-core halves without any isolation distance between the winding and the core. Fig. 4(a) shows a drawing of one of the core halves with its corresponding winding. Thereby, the core consists of several stacked E-cores to achieve the desired form factor. The two core halves with their respective windings are then separated by a certain distance $d = 1.6$ mm to keep the average electric field strength below 4.5 kV/mm in the case of 7 kV CM voltage, similar to the air gap in a conventional transformer [54], [55]. The isolation distance between the two core halves is ensured by mounting them in a 3D-printed enclosure as shown in Fig. 4(b). In operation, the primary winding is on GND potential, whereas the secondary winding floats on the switch-node potential. To also define the potential of the ferrite cores, they are connected to one end of the corresponding winding as shown in Fig. 4(c) and are covered with a thin layer of semiconductive graphite spray (cf. Fig. 4(d)) to tie the surface of the entire core halves to the potential of the respective winding. The surface resistance of the graphite spray (*Kontakt Chemie Graphit 33*) is < 2000 Ω/sq, which is sufficiently low to define the potential of the surface and at the same time is sufficiently high such that no significant eddy current losses are generated by the magnetic field [56]. As an alternative, semiconductive tape could be used to create an equipotential surface.

Consequently, this transformer arrangement can be regar-ded as plate capacitor from an electric field point of view, which allows to estimate the coupling capacitance of the transformer as

$$C_{CM} = \frac{\varepsilon_0 \varepsilon_r A}{d}, \tag{6}$$

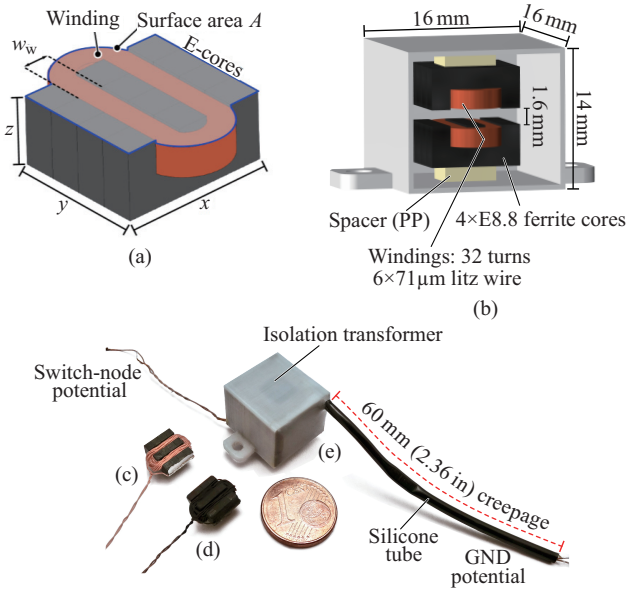

Fig. 4. (a) Ferrite core half (consisting of several stacked E-cores) with its corresponding winding. (b) CAD model of the isolation transformer (outer dimensions 16 mm × 16 mm × 14 mm, i.e., 0.63 in × 0.63 in × 0.55 in) showing the two windings on the ferrite cores, which are separated by a 1.6 mm gap. The 3D-printed housing is then filled up with a special silicone which provides the electrical insulation. (c) Picture of the winding (32 turns of 6 × 71 µm litz wire) on four stacked E8.8 ferrite cores. One end of the winding is electrically connected to the stacked cores with the help of conductive silver paint (silver color). (d) The whole arrangement is then coated with a semiconductive graphite layer (black color) to define an equipotential surface. (e) Picture of the realized silicone-encapsulated isolation transformer. The necessary creepage distance is provided by the silicone tube.

where A is the surface area of the core halves and the windings (cf. Fig. 4(a)) and d is the separation distance between the core halves. Since d is already fixed to d = 1.6 mm, the remaining geometry parameter to minimize the coupling capacitance is the surface area A. With a relative permittivity of ε_r = 4.12 of the selected insulation material (cf. Section II-B1), the surface area must be lower than 132 mm^2 to keep the coupling capacitance below the desired value of $C_{CM,\,max} < 3$ pF, which is roughly 10 times lower than the coupling capacitance of commercially available isolation transformers. To fulfill this condition, four stacked E8.8 ferrite cores (material *N30*) are used (x = 9 mm (0.35 in), y = 8 mm (0.31 in), z = 4.1 mm (0.16 in), cf. Fig. 4(a)), which results in an almost square-shaped form factor of the core surface, a surface area of A = 108 mm^2 (including the winding heads), and a theoretical coupling capacitance of C_{CM} = 2.5 pF.

In order to analyze the electric field in the isolation transformer, a FEM simulation has been implemented and the simulated electric field distribution is shown in Fig. 5. As can be seen, the windings are field-free due to the shielding effect of the graphite coating. Furthermore, a high electric field only occurs between the limbs of the ferrite cores and is slightly lower between the windings (due to the slightly larger distance). To decrease the maximum electric field strength, the edges and corners of the ferrite cores have been rounded off and the maximum value of the electric field (6 kV/mm) is still

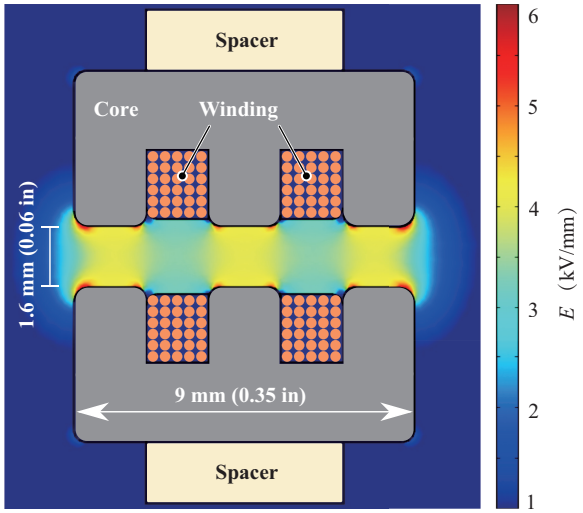

Fig. 5. Simulated electric field strength in the isolation transformer. The maximum occurring electric field strength (6 kV/mm) is still lower than the breakdown field strength of the used insulation material (24 kV/mm) by a factor of four.

a factor of four lower than the breakdown field strength of the used silicone encapsulant and therefore uncritical.

As can be noticed from the dimensions of the cores, the isolation gap is comparably large and hence, a rather low magnetic coupling factor k will result. Thus, the transformer acts similar to a pair of inductive power transfer (IPT) coils. Thereby, larger primary-side and secondary-side inductance values are beneficial for ensuring a higher quality factor [57] and lower magnetization current, and for this reason the number of turns wound on the two core halves should be as high as possible while the thermal limit has to be considered at the same time. Therefore, a maximum current density of J_{max} = 15 A/mm^2 is defined. In order to keep the high-frequency losses due to the skin and proximity effect to a moderate level, litz-wire has to be employed for the primary and secondary windings. For a maximum expected operating frequency of f_{max} = 1 MHz, a skin-depth in copper of δ_{Cu} = 65 µm results. Hence, as a compromise between the copper filling factor and the HF losses, a strand diameter of d_s = 71 µm is selected and with an assumed total copper filling factor of 25% (i.e. 50% litz-internal and a 50% ratio between the winding area and the available core window area), the maximum achievable number of turns is 34. For practical reasons, a 6 × 71 µm litz wire and N = 32 turns is selected, resulting in a DC-resistance of R_{DC} = 620 mΩ.

To check the feasibility of the transformer design, the magnetic flux density in the ferrite core is determined, whereby it is assumed that the operating frequency is in the range of $[f_{min}, f_{max}]$ = [100 kHz, 1 MHz]. Furthermore, due to the series-series compensation of the leakage inductance, the peak value of the sinusoidal voltage applied to the magnetizing inductance of the transformer is approximately equal to the fundamental component of the rectangular voltage applied from the primary-side, i.e.

$$\hat{u}_\mathrm{m} = \frac{4}{\pi} \cdot u_\mathrm{p} \ . \tag{7}$$

Consequently, with the magnetic cross section area A_m of the core, the peak magnetic flux density can be calculated as

$$\hat{B} = \int_0^{\frac{1}{4f}} \frac{\hat{u}_\mathrm{m}}{N \cdot A_\mathrm{m}} \sin(2\pi f t) \cdot \mathrm{d}t = \frac{2u_\mathrm{p}}{\pi^2 N A_\mathrm{m} f} \ , \tag{8}$$

resulting in $\hat{B}$ = 3.2 mT…32 mT for the assumed frequency range, which indicates that the ferrite cores are operated far below the saturation limit and hence the design is feasible from a magnetic perspective.

1) Thermal Model & Selection of the Insulation Material:

For a prediction of the temperature distribution inside the transformer and especially in the insulation material which plays a central role for the transformer at hand, a thermal FEM simulation is conducted. As a basis for the simulation, the different loss components, i.e. winding losses, core losses, and dielectric losses are calculated first.

For an estimation of the worst case winding losses, the AC winding resistance at the highest expected transformer operating frequency (f_max = 1 MHz) is calculated. Considering the skin-effect and the proximity effect, the winding losses can be calculated according to [58] as

$$P_\mathrm{Cu} = R_\mathrm{DC} (F_\mathrm{R} \hat{I}^2 + G_\mathrm{R} \hat{H}^2) \ , \tag{9}$$

where F_R and G_R are the factors describing the skin-effect and the proximity-effect, and $\hat{H}$ depicts the temporal peak value of the magnetic field, which shows a triangular spatial distribution across the winding window width w_w = 1.65 mm (cf. Fig. 4(a)) and a spatial rms value of [59]

$$\hat{H}_\mathrm{srms} = \frac{N\hat{I}}{\sqrt{3}\, w_\mathrm{w}} \ . \tag{10}$$

By combining (9) and (10), the ratio between the effective AC resistance R_AC and the DC resistance R_DC can be derived [58]. For f_max = 1 MHz, this factor is $R_\mathrm{AC}/R_\mathrm{DC}$ = 4.5, i.e., the effective AC resistance is R_AC = 2.8 Ω for each of the two windings. With the calculated primary-side and secondary-side currents (cf. Section II-A), the highest expected winding losses are $P_\mathrm{p,Cu}$ = 415 mW and $P_\mathrm{s,Cu}$ = 138 mW.

Furthermore, a calculation of the core losses with the Steinmetz parameters for *N30* ferrite (k_c = 15.88, α = 1.31, and β = 2.45 [60]) and the determined values for the magnetic flux density leads to 4 mW at f = 100 kHz and 0.3 mW at f = 1 MHz, respectively, i.e. the core losses can be neglected.

Due to the comparably high electric field in the isolation transformer and the high switching frequency of the 10 kV SiC MOSFET bridge, the insulation material between the two core halves is exposed to a high dielectric stress and therefore, dielectric losses might become significant and would have to be considered. According to [61], the dielectric losses generated in a capacitance C_CM by a rectangular voltage with bottom value 0 V, top value U_DC, frequency f_sw and 50% duty cycle can be calculated as

$$P_\mathrm{d} \approx \tan\delta \cdot C_\mathrm{CM} U_\mathrm{DC}^2 \cdot \frac{2f_\mathrm{sw}}{\pi} \ln\left(\frac{2e^\gamma f_\mathrm{c}}{f_\mathrm{sw}}\right), \tag{11}$$

where $\gamma \approx 0.57$ is the Euler-Mascheroni constant, and

$$f_\mathrm{c} = \frac{\ln\left(\frac{0.9}{0.1}\right)}{2\pi t_\mathrm{rise}} \tag{12}$$

is the corner frequency (cf. [61]). Furthermore, t_rise is the 10 %…90 % rise time of the switch-node voltage. Thereby, it is important to note that not only the fundamental frequency component of the switch-node voltage but also the higher order harmonics contribute to the dielectric losses. (11) already includes the effect of the harmonics and as can be seen, the total dielectric losses are proportional to the dissipation factor tan δ, the switching frequency f_sw, and the square of the voltage, or the electric field, respectively. To show that it is important to select a suitable insulation material, the dielectric losses are first calculated for a typical epoxy-based insulation material, e.g. *Damisol 3418* whose dissipation factor is strongly frequency and temperature dependent [61] and is assumed to be tan δ = 1.2% for the following calculations. With a switch-node voltage of 7 kV, a switching frequency of f_sw = 125 kHz and a rise time of t_rise = 100 ns, dielectric losses of P_d = 430 mW occur in the insulation material, which is very high compared to the rated power of the isolation transformer. Furthermore, epoxy resins typically feature a rather low thermal conductivity (0.3 W/(m K) in this case), which means that the extraction of the heat generated by the dielectric losses is impeded and therefore could lead to a thermal runaway.

Fig. 6(a) shows the simulated temperature distribution inside the isolation transformer in the case of epoxy resin as insulation material and a fixed housing temperature of 50 °C. As can be seen, due to the dielectric losses in the insulation material and the low thermal conductivity of the epoxy resin, a hot spot between the two core halves and a temperature rise of 44 K occurs. Since epoxy resins typically show a significant increase of their dielectric dissipation factor tan δ which can reach values of tan δ > 25% at higher temperatures in the region of their glass transition temperature [61]–[63], a thermal runaway is very likely to happen (especially when a higher surface temperature of the isolation transformer is considered, e.g. the baseplate temperature of 100 °C of a SiC module, which also integrates the transformer, cf. Fig. 2) and therefore, epoxy resins are unsuitable for MV MF applications.

In contrast, silicone composites typically feature a very low and stable tan δ up to temperatures beyond 200 °C. However, pure silicone rubber typically shows only a low thermal conductivity, which would potentially lead to an undesired heat accumulation similar to Fig. 6(a). To increase this value, thermally conductive micro or nanoparticles can be added to the pure silicone, which, on the other hand, leads to an

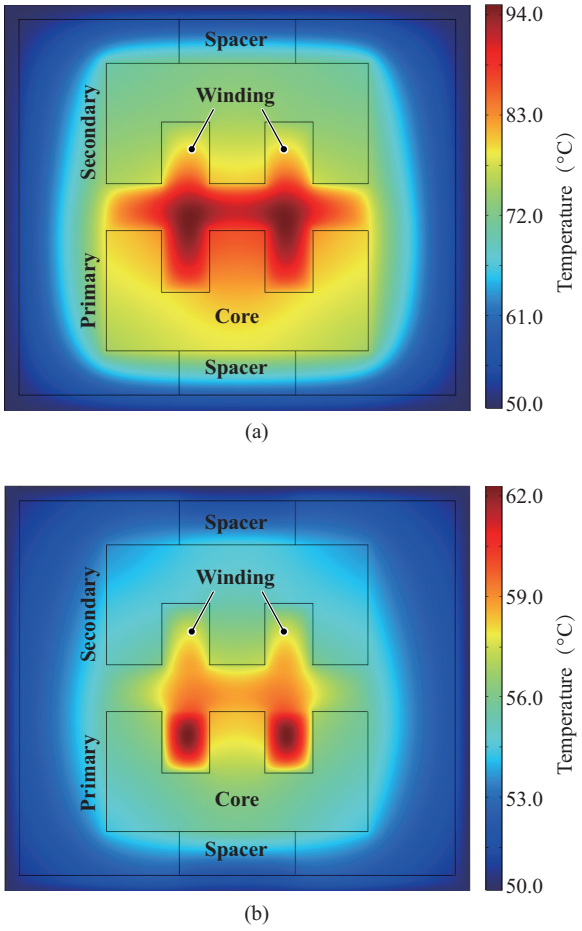

Fig. 6. (a) Thermal FEM simulation of the temperature distribution inside the isolation transformer in the case of epoxy resin as insulation material and a boundary condition of 50 °C at the transformer housing surface. The dielectric losses dominate over the winding and core losses and a temperature increase of 44 K occurs in the insulation material between the core halves. (b) Temperature distribution in the case of silicone (*Dow Corning TC-4605 HLV*) as insulation material. Due to the much lower dissipation factor and the higher thermal conductivity, the temperature increase is only 12 K in this case.

TABLE II
PROPERTIES OF THE UTILIZED SILICONE *DOW CORNING TC 4605 HLV*

Property	Value
Dielectric strength	24 kV/mm
Dielectric constant ε_r	4.12@100 kHz
Dissipation factor tan δ	0.63%@100 kHz
Thermal conductivity	1 W/(m K)
Operating temperature	− 45 . . . 200 °C

increasing dielectric dissipation factor [64]. Therefore, a compromise between a low tan δ and a high thermal conductivity has to be made. The utilized material for the encapsulation of the isolation transformer at hand is the two-component silicone compound *Dow Corning TC-4605 HLV* and the properties of this material are listed in TABLE II. With this insulation material, the dielectric losses are only P_d = 300 mW. Fig. 6(b) shows the associated temperature distribution inside the isolation transformer and as can be seen, the temperature increase in the hot spot, which is now located inside the primary-side winding, is only 12 K due to the lower dielectric losses and the higher thermal conductivity. This shows that the selection of a proper insulation material is crucial for the functionality of a highly compact isolation transformer and consequently, with the selected material, the isolation transformer can be operated inside an intelligent 10 kV SiC module with an assumed baseplate temperature, i.e. transformer surface temperature of 100 °C, which would lead to a hot spot temperature of 112 °C inside the transformer.

For a reliable operation of the isolation transformer, the insulation material must be free of air-cavities or other impurities, which could lead to partial discharges and a degradation of the material over time. Therefore, a vacuum pressure potting (VPP) process is used, i.e. the silicone is devolatilized and the transformer is potted under vacuum (30 mbar) before the pressure is increased again to compress possible air or vacuum cavities. The still liquid silicone compound is then cured at a temperature of 120 °C for several hours. More details on the VPP process and the insulation material are given in [14].

In order to provide a sufficiently large creepage distance between the primary-side and secondary-side litz wires at the outside of the transformer, a silicone tube is covering the primary-side litz wire (on GND potential) and is also potted in the silicone insulation material such that there is no other creepage path than the one along the silicone tube. The finalized isolation transformer is shown in Fig. 4(e).

2) Determination of the Transformer Properties:

Besides the inductances and the magnetic coupling factor k, which are required to determine the optimum operating frequency, also the parasitic coupling capacitance C_{CM} between the primary-side and the secondary-side is measured. For this purpose, a *HP 4294A Precision Impedance Analyzer* is used.

The measured value of the coupling capacitance is C_{CM} = 2.6 pF, which matches very well with the calculated value of 2.5 pF. Considering the small transformer dimensions, this capacitance value is very low and ensures that the parasitic CM currents stay in a reasonable range even in the case of high dv/dt values of up to 100 kV/µs.

The measurement of the primary-side and the secondary-side inductances leads to L_p = 23.7 µH and L_s = 23.4 µH and together with a measured leakage inductance of L_σ = 22 µH, the magnetic coupling factor (referenced to the primary-side) can be calculated as

$$k = \sqrt{1-\frac{L_\sigma}{L_p}} = 0.27. \tag{13}$$

With these values, the optimum operating frequency f_0 = 713 kHz, and the values of the resonance capacitors $C_{r1} = C_{r2}$ = 2.88 nF, can be determined with (1) and (2), respectively.

C. Experimental Verification of the Isolated Power Supply

For the experimental verification of the isolated gate driver power supply, different stress tests have been performed. To test the DC isolation rating of the designed transformer, a

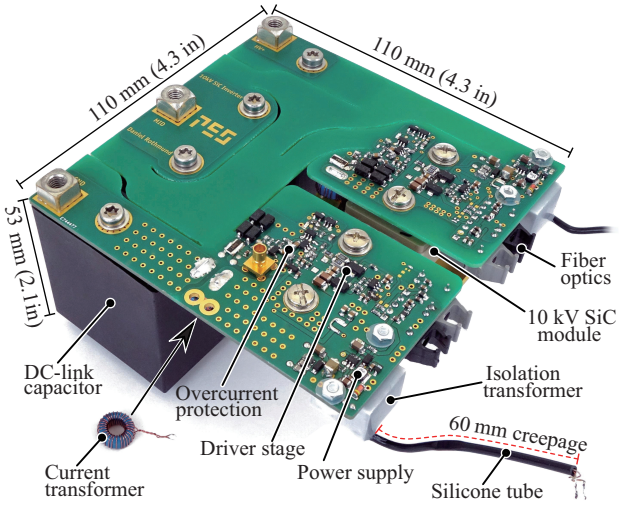

Fig. 7. Picture of the 10 kV SiC-MOSFET half-bridge. Due to the encapsulated isolation transformers, no additional isolation distances are required, enabling a highly compact design of the gate driver circuit and the half-bridge. The 10 kV SiC MOSFETs and the current transformers (cf. Section IV) are mounted below the PCB.

20 kV DC voltage (which is almost three times higher than the maximum operating voltage of 7 kV) has successfully been applied between the transformer's primary and secondary windings for one hour without breakdown, temperature increase or measurable current flow through the isolation. This proves that the isolation concept is properly working and well overdimensioned to guarantee a long lifetime.

Furthermore, to also test the complete gate driver circuit and the isolation transformer under real operating conditions, a 10 kV SiC-MOSFET-based half-bridge inverter has been designed as shown in Fig. 7. It consists of a PCB which incorporates the low-side and the high-side MOSFETs together with their respective gate driver and isolated power supply circuits. As can be seen, the isolation transformers are placed on the bottom side of the PCB and enable the construction of a highly compact half-bridge due to their small dimensions. As already mentioned, the silicone tube provides a 60 mm creepage distance to the primary-side driving circuit of the isolation transformer (not shown), which only consists of a *MAX13256* H-bridge IC, an adjustable clock generator IC, and two ceramic DC buffer capacitors.

To expose the isolation transformer to a very high stress, the half-bridge has been operated with a DC-link voltage of 7 kV and a switching frequency of 125 kHz for one hour. Thereby, an inductor has been used as load to enable ZVS and therewith to minimize the switching losses of the 10 kV SiC MOSFETs [22]. During this test, the CM current of the high-side isolation transformer has been measured. The corresponding circuit diagram and the according voltage and current waveforms during a rising voltage transition are shown in Fig. 8. It can be seen that a dv/dt of 82 kV/µs leads to a peak CM current of 300 mA. To obtain this peak current from the measured voltage slope, a coupling capacitance of 4.1 pF (which is 1.5 pF larger than the measured coupling capacitance of the isolation

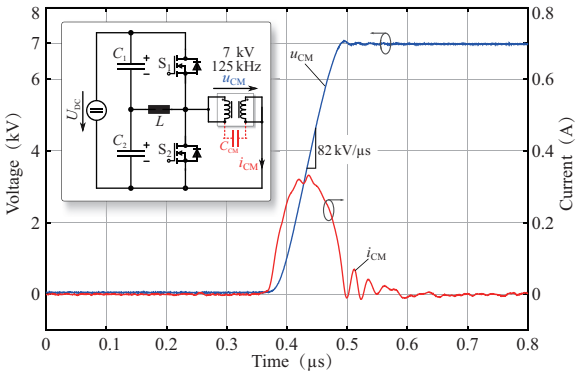

Fig. 8. Measured CM voltage u_{CM} across the isolation transformer together with the measured capacitive current i_{CM}.

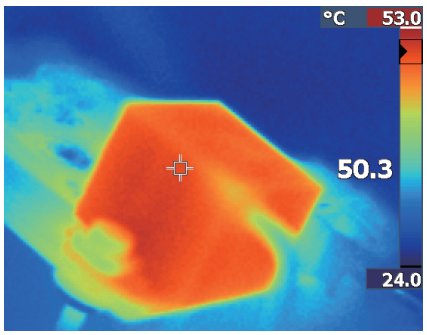

Fig. 9. Thermal image of the isolation transformer under operation with a 2 W load and a CM voltage stress of 7 kV, 125 kHz. The average steady state surface temperature reaches 50 °C under natural convection.

transformer) must be present. The additional capacitance can be explained by parasitic capacitances of the connection of the PCB to the isolation transformer and/or additional cable capacitances.

During the 7 kV, 125 kHz operation of the entire circuit with a load of 2 W, the steady-state surface temperature of the isolation transformer (cf. Fig. 9) reaches 50 °C (at an ambient temperature of 25 °C and for natural convection cooling), and as already shown by the thermal FEM simulation in Fig. 6(b), the hot spot temperature is estimated to be around 62 °C.

III. Ultrafast Overcurrent Protection (OCP)

In MV applications, it is highly recommended to implement an overcurrent and/or short circuit protection for the MV semiconductors due to the high voltages and the corresponding high energies in e.g. the DC-link capacitors, which could lead to serious damage of the hardware in case of a fault. Furthermore, MV SiC devices with blocking voltages of 10…15 kV are still very expensive and are up to now only available as prototype devices.

It is shown in [65] that single 10 kV SiC MOSFETs can survive approximately 8.5 µs under a full short circuit with 6 kV DC-link voltage. However, in [66], a clear relation between the degradation of the MOSFET-chip (i.e. increased $R_{DS,on}$) and the short circuit duration is apparent, since the degradation is an effect of the high temperature of the chip and its metallization

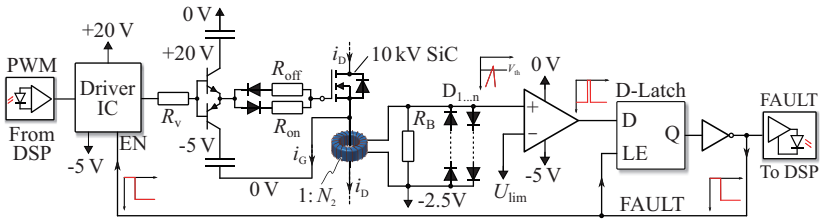

Fig. 10. Circuit diagram of the driver stage and the overcurrent protection. The drain current i_D of the MOSFET is measured via a 1 : N_2 = 1 : 30 air-gapped current transformer and the subsequent burden resistor R_B = 1 Ω. Once the threshold U_{lim} is exceeded, the comparator and consequently also the D-latch changes state and latches the FAULT state. This signal is fed back to the enable input EN of the driver IC (*UCC27531-Q1* from *TI*), leading to a turn-off of the 10 kV SiC MOSFET. The delay of the logic is approximately 22 ns. Furthermore, the FAULT signal is optically transmitted back to the supervisory control.

during a short circuit. Additionally, in the case of 10 kV, 100 A SiC MOSFET modules, a short circuit withstanding time of only 3.5 µs at 6 kV has been observed [67]. Therefore, the goal is to realize an ultrafast overcurrent protection (OCP) with a very short reaction time in order to keep the thermal stress on the 10 kV SiC MOSFET chips as low as possible.

In literature, two major types of faults are described, namely the hard switching fault (HSF), where a MOSFET turns on onto a short circuit, and the fault under load (FUL), where a short circuit occurs while the MOSFET is in on-state. In this case, however, the current and voltage slopes are mainly and significantly limited by the switching speed of the turning on MOSFET, whereas in MV applications, flashovers can occur (due to insulation failures of e.g. the silica gel in MV semiconductor modules or the insulation material e.g. in the transformer employed in a DC/DC converter) and show extremely fast voltage and current transients, which are much more critical to handle for an OCP. Therefore, the standard HSF and FUL tests are the only measure for the quality of an OCP circuit, since they do not test the worst case scenario, namely an arc flashover across one of the MOSFETs in a bridge-leg configuration while the complementary MOSFET is turned on. Therefore, the term flashover fault (FOF) is introduced and an FOF is applied to a 10 kV SiC MOSFET bridge-leg by using a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD* in the high-side position, which internally ignites a low-ohmic plasma (i.e. a solid short circuit) when the applied voltage exceeds its breakdown voltage, while the low-side switch is in on-state and has to clear the fault.

A. Functional Principle of the OCP

For the detection of a fault, the device current is measured by means of an air-gapped current transformer in the source path of the 10 kV SiC MOSFET as shown in Fig. 10. Thereby, the air gap avoids the saturation of the core material due to the DC current component and compared to e.g. a current measurement shunt, the current transformer provides galvanic isolation of the measurement signal and improves the immunity against CM distortions. In the following, the fundamental functionality of the OCP circuit is explained, assuming that the drain current can be measured with a sufficient accuracy with the 1 : 30 current transformer. The details on the design of the current transformer can be found in the Appendix.

In the configuration shown in Fig. 10, the current transformer is placed below the gate and source contacts of the driver stage, which ensures that only the drain current i_D is measured. The secondary-side of the current transformer is connected to a burden resistor R_B = 1 Ω and the entire circuit is powered from the 0 V/ −5 V rails. Since the drain current of the 10 kV SiC device can also be negative, one terminal of the current transformer is connected to a locally generated −2.5 V potential, allowing a voltage swing of ±2.5 V across R_B, which corresponds to a drain current of ±75 A. In case of a fault, where much higher currents can occur, the diodes $D_{1...n}$ start conducting and clamp the voltage across R_B in order to protect the input of the subsequent comparator from overvoltages. The advantage of diode strings compared to a single TVS or zener diode per direction is the steeper characteristic of pn diodes, i.e. the clamping voltage is less current dependent. The type and the number of serial diodes is selected such that a clamping voltage of 2.5 V results.

For the detection of an overcurrent, the voltage at the upper rail of R_B is compared to the threshold voltage U_{lim} = −2.5 V + 1 V = −1.5 V (for an overcurrent threshold of 30 A, R_B = 1 Ω and N_2 = 30) by an ultrafast comparator. Once the threshold is exceeded, the comparator sets its output to HIGH (0 V) and the subsequent D-latch changes state and latches its output state when LE is LOW (−5 V). This FAULT signal (cf. Fig. 10) is connected to the enable input EN of the gate driver IC *UCC27531-Q1* from *TI*), which then initiates a turn-off of the 10 kV SiC MOSFET. The delay caused by the logic ICs and the gate driver IC adds up to T_{react} ≈ 22 ns between the detection of the overcurrent and the reaction of the gate voltage. Since the gate driver IC does not provide a sufficiently high gate current (but undervoltage lockout, which is the reason to use an IC at all), a BJT totem-pole stage is used to provide a sufficiently high gate current. The gate resistors for turn-on and turn-off are R_{on} = 20 Ω and R_{off} = 10 Ω , respectively, according to [22]. Alternatively, a soft turn-off circuit could be implemented, which, in case of a fault, turns off the device with a larger gate resistor as it is done for IGBTs to limit the voltage overshoot. Furthermore, the FAULT signal is also transmitted back to the supervisory control via an optical fiber (30 ns delay) in order to turn-off all devices in the converter system in the case of an overcurrent in one of the 10 kV SiC devices. Accordingly, when a fault is detected, after 22 ns, the inner fault loop initiates the turn-off of the device which detected the overcurrent, and after approximately 100 ns, the gate voltages of all other 10 kV devices react. It should be noted that alternatively a direct

feedback path to the gate could be implemented for a further reduction of the reaction time.

B. Flashover Fault Simulation

Before the OCP is tested in hardware and has to prove that it is able to safely clear a HSF and an FOF at 7 kV DC-link voltage, a simulation is carried out in order to predict the behavior of the circuit under these extreme conditions. Fig. 11(a) shows the simulation model of the bridge-leg in the case of an FOF, where an ideal switch is located in the high-side MOSFET position and the low-side MOSFET is replaced by a simple equivalent circuit consisting of a voltage controlled current source, the nonlinear parasitic MOSFET capacitances, the antiparallel body diode, and the package inductances [20]. The current source is controlled by the internal gate voltage $u_{GS,int}$ across the gate-source capacitance C_{GS} via

$$i_{D,0} = g_m(u_{GS,int} - U_{th}), \tag{14}$$

where U_{th} is the threshold voltage of the MOSFET and g_m is its transconductance. In the simulation, the ideal switch is closed at $t = 0$ while the low-side MOSFET is already turned on, i.e., $u_{Driver} = 20$ V. Furthermore, it is assumed that the overcurrent protection will react 30 ns after the fault and will force the driver output voltage u_{Driver} to −5 V within another 15 ns.

Fig. 11(b) shows the simulated waveforms under these assumptions. Initially, the drain current i_D rises with a very high di/dt, which in turn induces a high positive voltage $u_{LS} \approx 140$ V across the source inductance L_S. The relatively large gate-source capacitance C_{GS} however keeps its voltage $u_{GS,int}$ constant and therefore, the external gate-source voltage u_{GS} closely follows the induced voltage u_{LS} with a 20 V offset, while the effect of the gate inductance L_G can be neglected in this case. Since also the driver voltage u_{Driver} is still clamped to 20 V, the difference of $u_{GS} - u_{Driver} \approx 140$ V peak is applied to the turn-off gate resistor $R_{off} = 10\ \Omega$, forcing a part of the MOSFET channel current through C_{GS} and leading to a negative gate current of $i_G = (u_{GS} - u_{Driver})/R_{off} = -14$ A peak (when the gate inductance L_G is neglected). The reader should note that the gate resistors and the diodes should be well dimensioned to withstand the high peak current. Consequently, C_{GS} is discharged (i.e. $u_{GS,int}$ decreases) and according to (14), the MOSFET channel current $i_{D,0}$ decreases again, as can be seen in the figure. Although the channel current decreases, the series inductances L_S, L_D, and L_σ try to keep the current constant and hence, a part of the drain current i_D commutates to the output capacitance C_{DS}, resulting in a rapid increase of the drain-source voltage u_{DS} and an inductive overshoot. At the same time, the drain current effectively decreases, and the complete process until this point takes place without any action from the gate driver and is therefore referenced as "self turn-off" of the MOSFET. However, at this point, the decreasing drain current leads to a positive gate current due to the negative induced voltage across L_S, such that the MOSFET partly turns on again. Now, the induced voltage is applied to $R_{on} = 20\ \Omega$, which is twice the value of R_{off} and therefore, the increase of the drain current is only small and the oscillation is damped. Furthermore, it is assumed that the OCP detects the overcurrent within 30 ns and switches the driver voltage u_{Driver} to −5 V, thereby actively turning off the remaining drain current. Depending on the application, a higher turn-on gate resistor might be selected to dampen the oscillation even more.

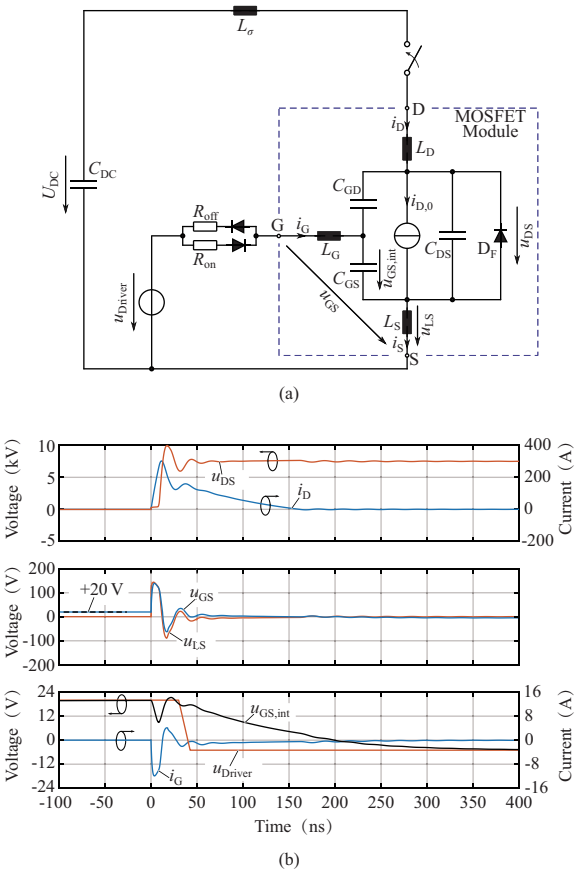

Fig. 11. (a) Schematic diagram of the MOSFET bridge-leg during a flashover fault (FOF), i.e., flashover across the high-side MOSFET during the on-state of the low-side MOSFET. For the simulation, the low-side MOSFET is replaced by a simple equivalent circuit consisting of a gate-source voltage controlled current source and the nonlinear MOSFET capacitances. (b) Simulated waveforms during a 7.6 kV FOF. The fault is cleared successfully and although the gate-source voltage u_{GS}, measured at the module terminals, reaches 140 V, the chip-internal gate-source voltage $u_{GS,int}$ is almost unaffected (voltage drop mostly occurring along the parasitic gate inductance and the gate resistor) and the MOSFET is not endangered.

As can be seen in Fig. 11(b), due to the self turn-off mechanism and the short reaction time, the OCP is able to clear the FOF within 200 ns, whereby a peak drain current of 320 A is reached. Furthermore, it can be noted that the chip-internal gate-source voltage u_{GS} barely exceeds 20 V and hence stays within the absolute maximum ratings, i.e., the MOSFET chip is not endangered.

C. Experimental Results

1) FOF Experiment

Since the results from the FOF simu-lation show that the OCP is able to successfully clear an FOF in theory, this situation is also tested in real hardware. Thereby, as shown in

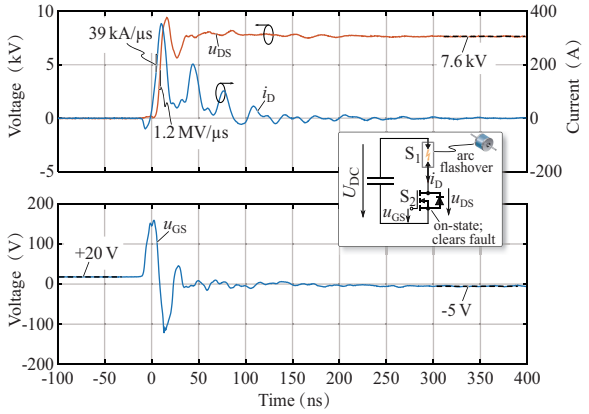

Fig. 12. Measured waveforms in the case of a flashover fault (FOF) for a DC-link voltage of 7.6 kV. S_2 is in the on-state while S_1 fails to short, e.g. due to an isolation breakdown, which is reproduced with a flashover in a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD*. The current rises with a slope of 39 kA/µs and reaches its peak of 350 A. Due to the self turn-off mechanism, the MOSFET turns itself off and the drain-source voltage rises to the DC-link level within 6 ns, i.e. an unprecedented dv/dt of 1.2 MV/µs. After the reaction delay of approximately 22 ns, the gate driver actively brings the gate voltage to −5 V and the fault is cleared within 150 ns.

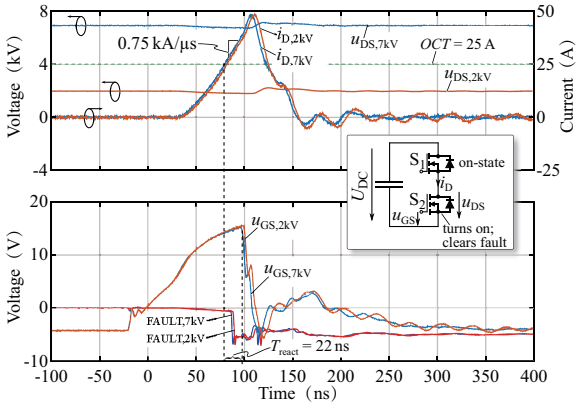

Fig. 13. Measured waveforms for a hard switching fault (HSF) for $U_{DC} = 2$ kV and $U_{DC} = 7$ kV. S_1 is in the on-state when S_2 turns on. 22 ns after drain current reaches the overcurrent threshold (OCT), the gate voltage reacts and S_2 is safely turned off within 150 ns. Almost independently of the DC-link voltage level, the current reaches a maximum of 48 A.

the schematic in Fig. 12, the low-side MOSFET is permanently turned on while the high-side MOSFET is substituted by a gas discharge tube (GDT) of type *Bourns SA2-7200-CLT-STD* and the DC-link voltage is increased until the GDT ignites. Fig. 12 shows the measured drain-source voltage u_{DS}, the gate-source voltage u_{GS}, and the drain current i_D during an FOF test with a 7.2 kV GDT, which ignited at 7.6 kV (due to tolerances). As can be seen, the waveforms are similar to the simulation, i.e., also in real hardware a self turn-off occurs. Thereby, the drain current reaches a value of 350 A and the drain-source voltage rises in 6 ns to the DC-link level with an unprecedented dv/dt of 1.2 MV/µs (which is close to the 100 MHz bandwidth limit of the used voltage probe). The OCP then actively clears the fault within 150 ns and the successful FOF test proves the proper functioning of the OCP under the most extreme conditions. Compared to the simulation, the measured waveforms show more oscillations in the drain current, which can be explained by the fact that the simulation model does not include all parasitics and nonlinear effects in the MOSFET. Furthermore, in the experiment, only the external gate-source voltage can be measured and reaches a value of 150 V peak. However, the simulation shows a very similar external gate-source voltage, which solely occurs due to the inductive voltage drop across the source inductance L_S, whereas the gate-source voltage directly on the MOSFET chip does not exceed 20 V during the FOF, which is therefore also assumed for the real FOF experiment.

If the 10 kV SiC module featured a Kelvin source contact, the MOSFET would not be subject to a self turn-off during an FOF, since the gate loop would be decoupled from the power loop. However, according to [66], the maximum short circuit current (in the case of a usual FUL or HSF) of similar 10 kV SiC MOSFETs from *Wolfspeed* is self-limited by the MOSFET channel to 270 A for a DC-link voltage of 6 kV and therefore, the presented OCP would also work for modules featuring a Kelvin source contact.

2) HSF Experiment

The schematic in Fig. 13 shows the situation for the HSF test, where the high-side MOSFET S_1 is in the on-state when the low-side MOSFET S_2 turns on. The measured waveforms of the drain current i_D, the drain-source voltage u_{DS}, the gate-source voltage u_{GS}, and the FAULT signal are shown for a HSF at 2 kV and 7 kV, respectively. With the increasing gate-source voltage, also the drain current increases and once it reaches the threshold (25 A in this case), after a short delay the internal FAULT signal, which is connected to the enable signal of the driver IC, changes state. The gate driver IC then switches its output to −5 V and the gate-source voltage decreases after the IC's propagation delay has passed. Almost independently of the DC-link voltage, a peak current of 48 A peak is reached and the OCP safely clears the HSF in less than 200 ns. The total reaction time from the point where the current threshold is reached until the gate voltage reacts is $T_{react} = 22$ ns in this case. It should be noted that a successful HSF experiment alone does not mean that the OCP can protect the switch comprehensively. Only in combination with a successful FOF experiment, it can be stated that the OCP is able to protect the device also in worst case fault situations.

IV. Conclusion

In this paper, a highly compact isolated gate driver for 10 kV SiC MOSFETs with ultrafast overcurrent protection is presented. A main challenge for medium-voltage (MV) gate drivers is the galvanic isolation of the gate driver power supply and the isolated low propagation delay signal transmission. In order to obtain a highly compact gate driver circuit, which could be integrated into future MV SiC modules, an encapsulated isolation transformer employed in a resonant converter topology is designed and constructed. Thereby, in contrast to classical transformers with both windings on the same

magnetic core, the primary winding and the secondary winding are wound on separate ferrite core halves, which are separated by a small gap that is filled with a silicone insulation material featuring a low dielectric dissipation factor and a high thermal conductivity to ensure a sufficient heat transport from the windings to the surface of the transformer. The dimensions of the realized transformer are 16 mm × 16 mm × 14 mm and the coupling capacitance is only 2.6 pF. The transformer isolation has been successfully tested for 1 hour with a 20 kV DC voltage and for one hour with a 7 kV, 125 kHz switching-node voltage, which proves the functionality of the designed MV isolation transformer.

Furthermore, in order to protect the 10 kV SiC devices from overcurrents and a possible destruction by short circuits, an ultrafast overcurrent protection (OCP) circuit is implemented. Thereby, the drain current of the device is measured via a gapped toroidal current transformer. The measured signal is subsequently compared to a predefined threshold by an ultrafast comparator whose output signal is latched in case of a fault and fed back to the enable input of the gate driver IC, which then initiates the turn-off of the 10 kV SiC device. The delay between the crossing of the overcurrent threshold and the reaction of the gate voltage is only ≈ 22 ns. Measurements prove that the realized OCP is also able to successfully clear a flashover fault (FOF) and a hard switching fault (HSF) at a DC-link voltage of 7 kV within less than 200 ns. Furthermore, during the FOF experiment, an unprecedented dv/dt of 1.2 MV/µs has been observed.

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Appendix
Design of the Current Transformer

For the measurement of the drain current of the 10 kV SiC MOSFETs, the current transformer has to be designed for a high bandwidth, such that fast overcurrent transients can be measured accurately. Furthermore, the current transformer should not add a significant signal delay to the protection circuit. Consequently, the leakage inductance and capacitance have to be kept small, which can be achieved by choosing a low number of secondary-side turns equidistantly wound on a toroidal ferrite core. As shown in Fig. 10, the secondary winding is connected to a burden resistor $R_B = 1\ \Omega$ where a current-proportional voltage is measured. If a voltage of 1 V across R_B is desired for an overcurrent threshold of $OCT = 30$ A, a turns ratio of $1 : N_2 = 1 : 30$ results, i.e. the number of secondary turns on the current transformer is $N_2 = 30$. To operate the ferrite core material in its linear region, the maximum magnetic AC flux density is set to $B_{max,AC} = 75$ mT and for an assumed rectangular drain current with 50% duty cycle, a minimum converter switching frequency of $f_{min} = 30$ kHz, a bottom value of 0 A, and an amplitude of $i_{d,max} = 30$ A, a core cross section of $A_m = 7.4\ mm^2$ is required. Therefore, a R10 × 6 × 4 ferrite core (N30 material) with a magnetic cross section area of 7.83 mm^2 is selected.

As the drain current of the switches is not a pure AC current but rather a superposition of an AC and a DC current, the current transformer has to be designed appropriately, such that the DC component does not lead to saturation of the magnetic core. Therefore, an air gap is inserted in the ferrite core. For limiting the magnetic DC flux density to $B_{max,DC} = 125$ mT, the required air gap length is

$$\delta = \frac{\mu_0 \cdot i_{D,DC}}{B_{max,DC}} = 150\mu m \tag{15}$$

for a maximum DC current component of $i_{D,DC} = 15$ A.

The air gap, however, causes the magnetizing inductance of the current transformer to drop significantly, which increases the AC magnetizing current. For the current transformer at hand, the peak magnetizing current for $f_{min} = 30$ kHz and 30 A, 50% duty cycle is 7% of the measured current value, which does not influence the detection of a HSF or an FOF due to the usually large resulting fault currents. For the sake of completeness, it should be noted that the current transformer represents a high-pass system (corner frequency $f_c = 17$ kHz) and is not able to measure DC currents, since the DC component only occurs as magnetizing current on the primary-side.

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A 1200 V/200 A Half-Bridge Power Module Based on Si IGBT/SiC MOSFET Hybrid Switch

Lei Li, Puqi Ning, Xuhui Wen, and Dong Zhang

***Abstract*—The hybrid switch (HyS), which is a parallel combination of the silicon (Si) insulated gate bipolar transistors (IGBTs) and the silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs), can realize high switching frequency at a reasonable cost. In this paper, a compact HyS half-bridge power module, rated at 1200 V/200 A, was fabricated in house and fully tested for the first time. An electrothermal model of the HyS was set up in LTspice to determine the optimal gate sequence for the HyS. To minimize the HyS power loss, the turn-on gate signals are applied to the Si IGBTs and the SiC MOSFETs simultaneously while a prior turn-off period exists between the turn-off gate signals of the Si IGBTs and the SiC MOSFETs. By considering the power loss of the HyS and the junction temperature of the SiC MOSFETs, a novel index is proposed to select the optimal prior turn-off period. Based on the HyS power modules, a 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were developed and tested to verify the analysis.**

***Index Terms*—Hybrid switch, insulated gate bipolar transistors (IGBTs), metal-oxide semiconductor field-effect transistors (MOSFETs), silicon carbide (SiC).**

I. Introduction

In the past decades, the Silicon (Si) Insulated Gate Bipolar Transistor (IGBT) has been widely used in many engineering applications such as renewable energy systems, utility power systems and transportation drives [1]. As the growth of the electric cars and the high-speed trains, the highly integrated power converters with more and more high switching frequency are now demanded. However, the long turn-off period induced from the minority carriers recombination namely the tail current severely restricts the switching frequency of the Si IGBT [2].

The Silicon Carbide (SiC) devices are the attractive alternatives because of their potential of high switching frequency [3] and high junction temperature [4]. Among them, the SiC Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is the most promising device to replace the Si IGBT for its high blocking voltage and compatible gate driver design [5]. Unfortunately, the SiC MOSFET is still under development and it is too expensive to be large scale adopted [6].

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The concept of the hybrid switch (HyS) was first proposed in 1993 [7]. With the help of the paralleled MOSFETs, zero-voltage switch (ZVS) of the IGBTs [8] is realized. Thus, the switching loss is reduced and the switching frequency is improved. Compared with the Si counterparts, the SiC MOSFETs have lower on-resistance [9] and lower reverse recovery energy [10]. Thus, better performance of the HyS can be achieved.

The HySs consisting of the paralleled Si IGBTs and the SiC MOSFETs have been investigated before [11]–[19]. It was demonstrated that the HySs can perform lower switching loss compared to the Si IGBTs and lower cost compared to the SiC MOSFETs [11], [12]. However, the reported HySs are commonly based on the discrete semiconductors and the parasitic inductors of the connection severely restrict their performance [13], [14]. A 6.5 kV/40 A HyS power module was developed in [15]. The HyS power module contained only one switch and only the double pulse test was conducted. Possible gate sequences for the HySs were evaluated and the optimal gate sequence was chosen by solely considering the power loss of the HySs [16]–[18]. There is large thermal stress on the SiC MOSFETs within the HySs because the entire load current is conducted through the SiC MOSFETs during the switching transients. A thermal balance control mode and a current-dependent switching strategy was presented in [18] and [19] respectively to keep the reliable operation of the SiC MOSFETs.

Improved from the previous studies, in this paper, a compact HyS half-bridge power module, rated at 1200 V/200 A, was fabricated to suppress the influence of the parasitic inductors and to fully utilize the advantages of the HyS. Si/SiC current ratio is 4:1. An electrothermal model of the HyS was set up in LTspice to determine the suitable gate sequence for the HyS. Considering the power loss of the HyS and the junction temperature of the SiC MOSFETs, a novel index is proposed to select the prior turn-off period between the turn-off gate signals of the Si IGBTs and the SiC MOSFETs. Utilizing the HyS power modules, a 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were developed and tested to verify the analysis.

II. Hybrid Switch Power Module

Fig. 1 depicts the layout of the HyS half-bridge power module. Each HyS consists of one SiC MOSFET (CPM2–1200–0025B, 1200 V/50 A at 100 °C) and two Si IGBTs (IRG8CH97K10F, 1200 V/100 A at 100 °C). Si/SiC current

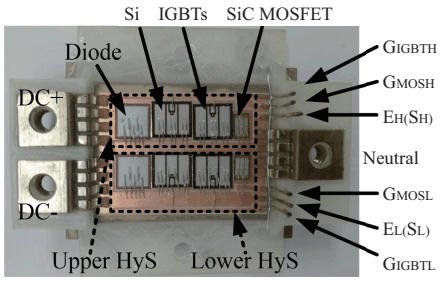

Fig. 1. Layout of the HyS power module.

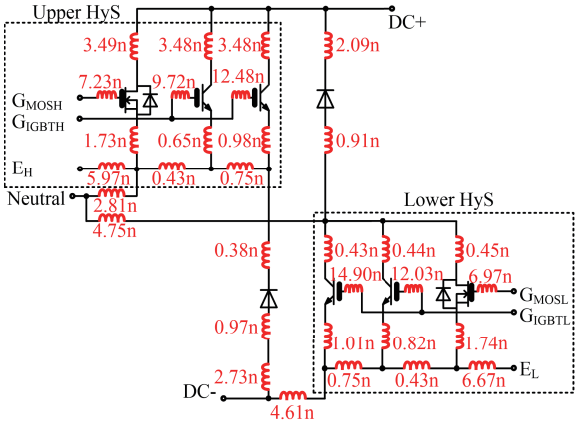

Fig. 2. Parasitic inductance of the HyS power module. (a) Parasitic inductance extracted by Ansys Q3D. (b) Simplified parasitic inductance.

ratio is 4:1. To reduce the cost, a Si PiN Diode (IRD3CH82DB6, 1200 V/200 A at 100 °C) is paralleled to the HyS. The Si IGBTs and the SiC MOSFET are separately controlled. Power terminals (DC+, DC−, and Neutral) and gate terminals (GIGBTH, GMOSH, EH, GIGBTL, GMOSL, and EL) are bonded to Direct-Bond-Copper (DBC) with ultrasonic method to form large contact areas. Si IGBTs collectors, Si Diode cathode and SiC MOSFET drain are soldered DBC. DBC patterns are designed as compact as possible to reduce the commutation path.

TABLE I
HyS Power Module Packaging Materials

Part	Specifications
Baseplate	Aluminum Silicon Carbide (AlSiC), 3 mm thickness
Substrate	Aluminum Nitride (AlN) DBC with Cu/AlN/Cu thickness 0.2 mm/0.4 mm/0.2 mm
Die solder	Au80Sn20, 280 ºC melting point
Power bonding wire	Aluminum, 0.4 mm diameter, 5 parallel wires for SiC MOSFET, 6 parallel wires for Si IGBTs and 6 parallel wires for Si Diode
Gate terminal	1 mm diameter copper pin
Power terminal	0.8 mm thick copper terminal
Encapsulation	Nusil R-2188
Housing	ABS, 1.5 mm thickness, 82 mm × 64 mm × 6 mm

A. Parasitic Inductance of the HyS Power Module

The parasitic inductance of the HyS power module was extracted by Ansys Q3D. The results are concluded in Fig. 2(a). It is difficult to determine the parasitic inductance between the Si IGBTs and the SiC MOSFET according to the results extracted by Ansys Q3D. Thus, the parasitic inductance was simplified utilizing the method in [20], shown in Fig. 2(b). The total inductance between the Si IGBTs and the SiC MOSFET is less than 10 nH, which has little influence on the dynamic current sharing among the devices [13]. As a comparison, the commercial TO−247 packaged devices which were commonly used in the aforementioned studies have more than 15 nH parasitic inductance in power path [21]. With the module design, the parasitic inductance is decreased a lot.

B. Thermal Resistance of the Chips Within the HyS Power Module

The packaging materials of the HyS power module are listed in TABLE I. A thermal resistance test system was built to measure the chip to case thermal resistance of the dies [22]. The linear superposition principle is adopted to evaluate the thermal coupling between the different chips and the junction temperature of the chips can be expressed as a thermal resistance matrix,

$$\begin{bmatrix} T_{j,\mathrm{DiodeH}} \\ T_{j,\mathrm{IGBTH}} \\ T_{j,\mathrm{MOSH}} \\ T_{j,\mathrm{DiodeL}} \\ T_{j,\mathrm{IGBTL}} \\ T_{j,\mathrm{MOSL}} \end{bmatrix} = \begin{bmatrix} T_{j,1} \\ T_{j,2} \\ T_{j,3} \\ T_{j,4} \\ T_{j,5} \\ T_{j,6} \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & R_{13} & R_{14} & R_{15} & R_{16} \\ R_{21} & R_{22} & R_{23} & R_{24} & R_{25} & R_{26} \\ R_{31} & R_{32} & R_{33} & R_{34} & R_{35} & R_{36} \\ R_{41} & R_{42} & R_{43} & R_{44} & R_{45} & R_{46} \\ R_{51} & R_{52} & R_{53} & R_{54} & R_{55} & R_{56} \\ R_{61} & R_{62} & R_{63} & R_{64} & R_{65} & R_{66} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} R_{11} & R_{12} & \cdots & R_{16} \\ R_{21} & R_{22} & \cdots & R_{26} \\ \vdots & \vdots & \ddots & \vdots \\ R_{61} & R_{62} & \cdots & R_{66} \end{bmatrix} = \begin{bmatrix} 0.48 & 0.14 & 0.02 & 0.09 & 0.12 & 0.02 \\ 0.05 & 0.33 & 0.06 & 0.02 & 0.03 & 0.03 \\ 0.02 & 0.18 & 0.95 & 0.02 & 0.09 & 0.15 \\ 0.12 & 0.09 & 0.02 & 0.50 & 0.12 & 0.02 \\ 0.02 & 0.05 & 0.02 & 0.05 & 0.32 & 0.08 \\ 0.02 & 0.12 & 0.15 & 0.02 & 0.21 & 0.93 \end{bmatrix} \tag{2}$$

where $T_{j,i}$ (i = 1–6) are the junction temperatures of the chips, P_i (i = 1–6) are the power losses of the chips, R_{ii} (i = 1–6) are the chip to case thermal resistance of the dies and R_{ik} (i, k = 1–6 and $i \neq k$) describe the junction temperatures rising because of thermal coupling. The two Si IGBTs are treated as one chip to simplify the tests and the analyses. The test results are concluded in (2).

III. Electrothermal Model of the Hybrid Switch

There are four kinds of semiconductors within a HyS, namely Si PiN Diode, Si IGBT, SiC MOSFET and the body diode of the SiC MOSFET, which is also a PiN Diode.

A. Electrothermal Model of the HyS

Fig. 3 demonstrates the circuit representation of the PiN diode model. It is made up of three parts. The first part is based on the finite difference method (FDM) [23] to calculate the excess carrier concentration in the base region under high level injection. I_1 and I_{n+1} are the boundary conditions to solve the ambipolar diffusion equation. The second part is the model to calculate the quasi-neutral base width. The quasi-neutral base region is divided into n elements with the equal length. The third part is a series of voltage sources representing the diode voltage, where E_{jA}, E_{res}, E_{jD}, and E_{SC} is the voltage across the P+/N− junction, the voltage across the base region, the voltage across the N−/N+ junction, and the voltage across the depletion region respectively. The values of the voltage sources are determined by the excess carrier concentration in the base region. In the simulation, the quasi-neutral base region is separated into 10 elements.

Fig. 4 displays the circuit representation of the SiC MOSFET model.The MOSFET channel current consists of I_{mosl}, conducted through the corners of the MOSFET cells, and I_{mosh}, conducted through the main portion of the MOSFET cells [24]. R_d is composed of the N- base region resistor and the drain contact resistor. R_s and R_g is the source contact resistor and the gate contact resistor respectively. The switching characteristics of the SiC MOSFET are described through the gate-source capacitor C_{gs}, gate-drain capacitor C_{gd}, and drain-source capacitor C_{ds}. C_{gs} and C_{ds} are determined by gate-source voltage and drain-source voltage respectively while C_{gd} ane related to both of them. The voltage-controlled capacitors are modeled through a voltage-controlled voltage source, a normal capacitor, and a current-controlled current source [25].

Shown in Fig. 5, the Si IGBT model is the combination of the FDM model and the MOSFET model. The excess carrier concentration in the base region is calculated through the FDM method, and the on-state voltage of the Si IGBT is composed of E_{jA}, E_{res}, and E_{SC}. The switching characteristics of the Si IGBT are described through the gate-emitter capacitor C_{ge}, gate-collector capacitor C_{gc}, and collector-emitter capacitor C_{ce}.

According to the results of the thermal resistance test, the thermal model of the Si IGBT is displayed as Fig. 6 [26]. Junction temperature rise of the Si IGBT is due to the self-heating of the Si IGBT and the thermal coupling between the Si IGBT and the other semiconductors. Thermal model of the Si PiN Diode and the SiC MOSFET can be described using the same circuit.

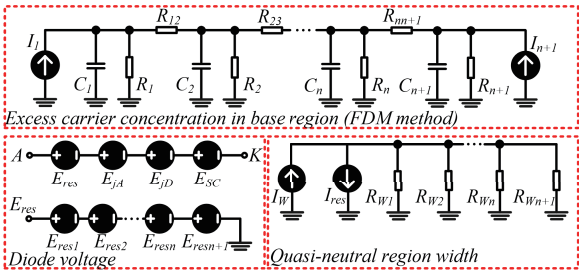

Fig. 3. PiN diode model.

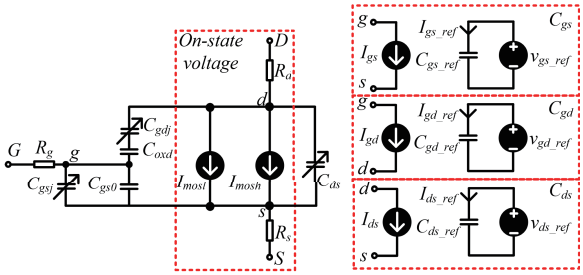

Fig. 4. SiC MOSFET model.

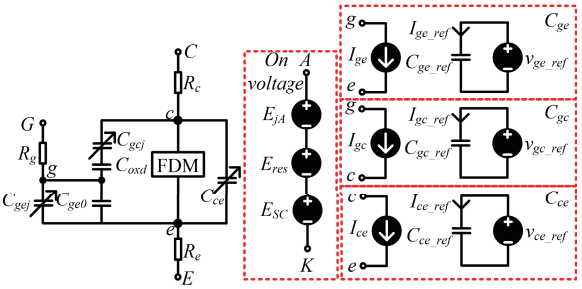

Fig. 5. Si IGBT model.

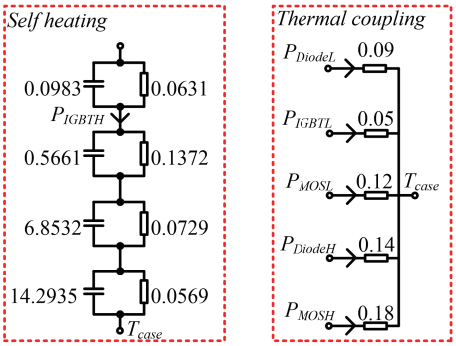

Fig. 6. Thermal model of the Si IGBT.

B. Verification of the Electrothermal Model

The output characteristics of the semiconductors were tested by the static and dynamic testing system from LEMSYS while the switching characteristics were tested utilizing a double pulse test fixture based on the voltage source inverter in Section V [27].

To carry out tests for the separate semiconductors, several

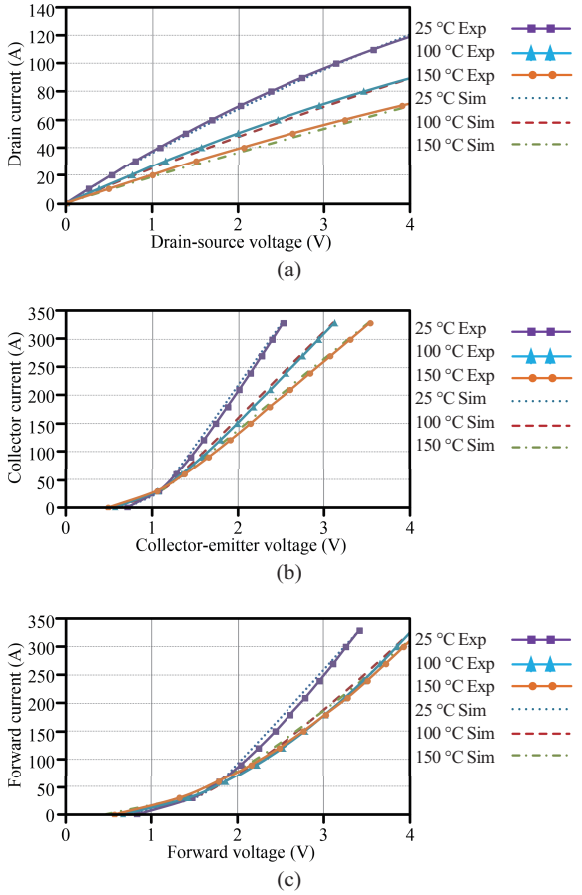

Fig. 7. Comparison of the experiment and simulation output characteristics. (a) SiC MOSFET. (b) Si IGBT. (c) Si Diode.

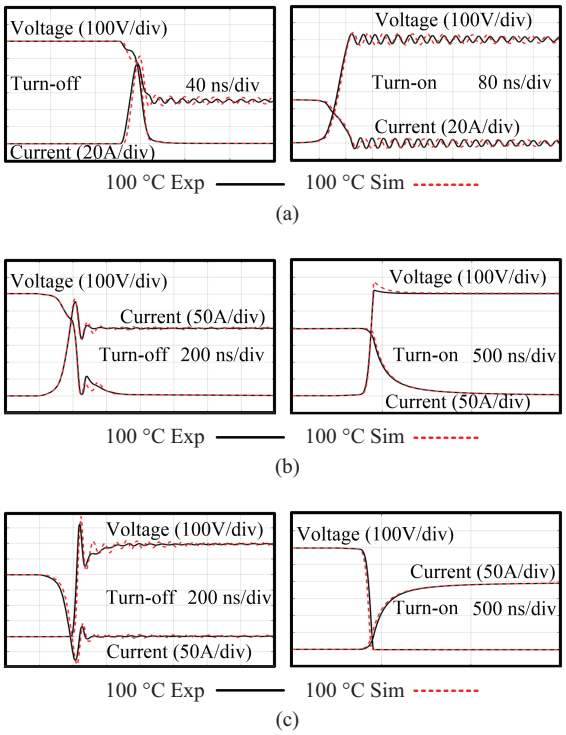

Fig. 8. Comparison of the experiment and simulation switching characteristics. (a) SiC MOSFET. (b) Si IGBT. (c) Si Diode.

HyS power modules were fabricated. All the chips were implemented in the HyS power modules, but only the utilized chips in the corresponding test were connected through the bonding wires. For example, only the Si PiN Diode was connected through the bonding wires to test the output characteristics of the Si PiN Diode. Only the SiC MOSFET and the Si PiN Diode were connected to test the switching characteristics of the SiC MOSFET or the Si PiN Diode. As demonstrated in Fig. 7 and Fig. 8, the output and switching characteristics of the dies predicted by the electrothermal model agree well with the experimental results. Therefore, the electrothermal model can be utilized to determine the gate sequence for the HyS.

IV. Gate Sequence for the Hybrid Switch

As depicted in Fig. 9, all the gate sequences for the HyS can be described using the prior turn-on period t_{on_delay} and the prior turn-off period t_{off_delay}.

Collectors of the Si IGBTs and drain of the SiC MOSFET are connected to the same DBC in the HyS power module (shown in Fig. 1). The power loss of the dies cannot be measured separately. Thus, the proposed HyS power module was simulated in LTSpice to find the optimal gate sequence. The simulation circuit is illustrated in Fig. 10. Buck circuit was utilized to set the load current i_L and the DC-bus voltage v_{dc}. Parasitic inductors were not considered in the simulation. Baseplate temperature was set to be 35 °C. Switching frequency was 50 kHz.

Fig. 11 displays the simulation results with v_{dc} of 400 V and i_L of 130 A. It is obvious that non-zero t_{on_delay} cannot bring any more reduction in the HyS power loss. In fact, the SiC MOSFET turns on prior to the Si IGBTs even the gate signals are applied at the same time because of the larger input capacitance of the Si IGBTs and the time taken to modulate the N-drift region conductivity [28]. Negative t_{on_delay} is not useful for reducing switching loss but introduces more conduction loss. As for positive t_{on_delay}, it eliminates the zero-current turn on of the Si IGBTs and enlarges the switching loss and the conduction loss, shown in Fig. 11(b). t_{on_delay} should remain as 0.

Fig. 12 illustrates the simulation results with v_{dc} of 400 V and i_L of 130 A utilizing different t_{off_delay}. As t_{off_delay} becomes larger, the HyS power loss decreases, but the SiC MOSFET power loss increases. A novel index as in (3) is adopted to determine the suitable t_{off_delay}. It is a characterization of the tradeoff between the HyS power loss reduction, $\Delta loss$ and the SiC MOSFET T_j rise, ΔT_j,

$$\text{Index} = \frac{-\Delta loss}{\Delta t_{off\_delay}} \Big/ \frac{\Delta T_j}{\Delta t_{off\_delay}} = \frac{-\Delta loss}{\Delta T_j} \tag{3}$$

Fig. 13 displays the index curve versus t_{off_delay}. The horizontal red line set the T_j limit as 150 °C and the maximum t_{off_delay} is restricted to be 3.5 us (Point C). Within the permissible t_{off_delay}, the index reaches the peak value at 1 us (Point A).

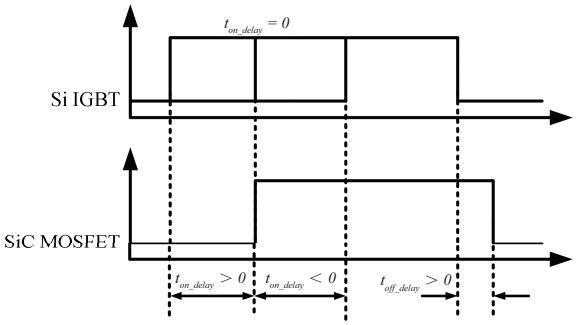

Fig. 9. Gate sequences for the HyS.

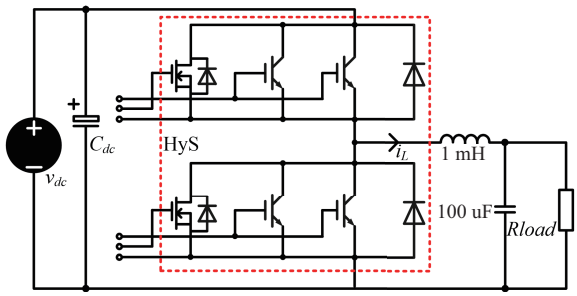

Fig. 10. Schematic of the simulation circuit.

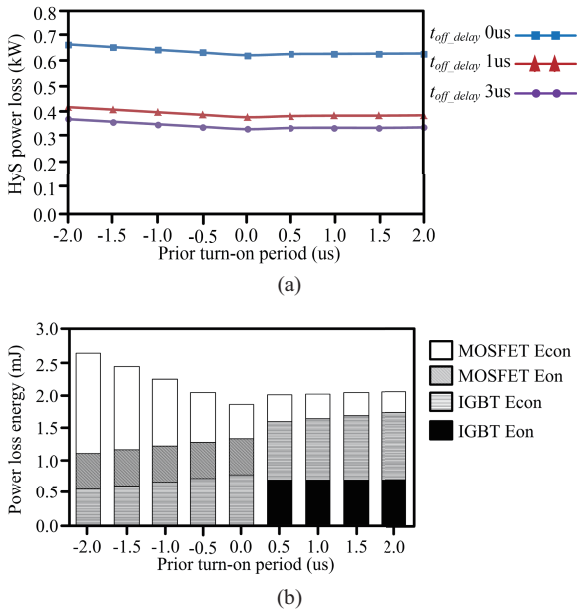

Fig. 11. Simulation results (v_{dc} = 400 V, i_L = 130 A). (a) HyS power loss at different t_{on_delay} and t_{off_delay}. (b) HyS loss energy distribution at different t_{on_delay}. Econ and Eon are conduction loss and turn-on loss respectively.

Between Point A and Point B (3 us), the HyS power loss can be further reduced, but the SiC MOSFET T_j rise is higher. Beyond Point B, the HyS power loss even starts to increase and drive the index to be negative. Therefore, the optimal t_{off_delay} is 1 us. Optimal t_{off_delay} at other operation conditions is concluded in Fig. 14.

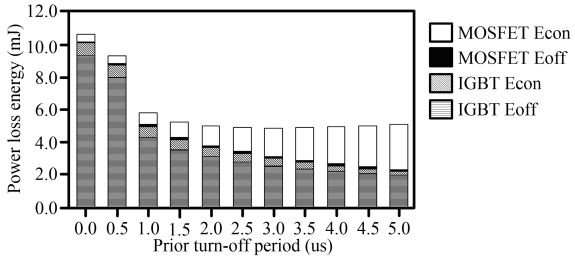

Fig. 12. HyS power loss energy distribution at different t_{off_delay} (v_{dc} = 400 V, i_L = 130 A). Eoff is the turn-off loss.

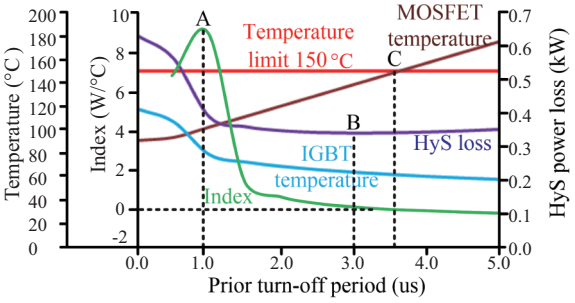

Fig. 13. Index plot to determine the suitable t_{off_delay}.

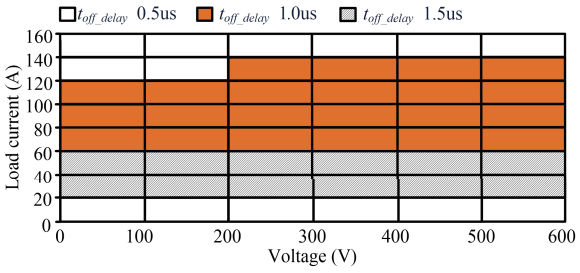

Fig. 14. Optimal prior turn-off period at different operation conditions.

V. Hybrid Switch Based Voltage Source Inverter

Utilizing the HyS power modules, a three-phase air-cooling voltage source inverter was set up to verify the analysis, shown in Fig. 15. The inverter was tested in open-loop mode with SVPWM control. The operation parameters are given in TABLE II.

For each HyS, there were two separate gate driver circuits to control the SiC MOSFET and the Si IGBTs independently. To assure the switching performance, a 2.5 A peak current optocoupler ACPL−332J from Avago followed by a 9 A peak current push-pull circuit IXDN609SI from IXYS were adopted as the gate driver ICs. 2 W DC/DC converters MGJ2D242005SC and MGJ2D241509SC were utilized as the gate driver power supply for the SiC MOSFET and the Si IGBTs respectively. Three 30 Ω chip resistors and three 15 Ω chip resistors, all in 2512 with 2 W rated power, were paralleled to form the gate resistors for the SiC MOSFET and the Si IGBTs respectively. During the turn off transient of SiC MOSFET, a fault turn-on of Si IGBTs may occur due to the fast rising collector-emitter voltage charges Miller

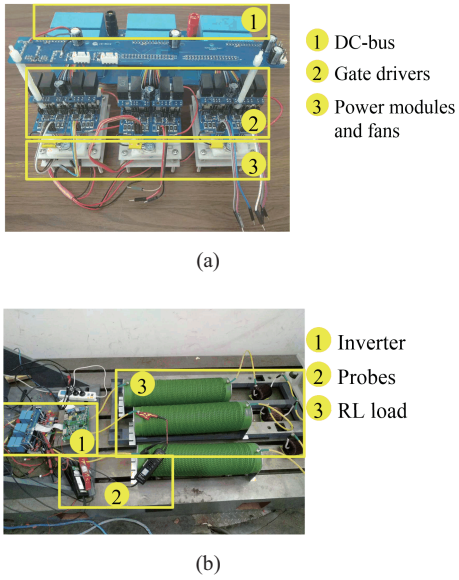

Fig. 15. Three-phase voltage source inverter. (a) Inverter prototype. (b) Test platform.

TABLE II
THREE-PHASE VOLTAGE SOURCE INVERTER OPERATION PARAMETERS

Parameter	Value
Input DC-bus voltage	400 V
Switching frequency	5 to 30 kHz
Modulation ratio	0.43
RL Load	3.0 Ω/0.5 mH
Fundamental phase current amplitude	33 A
Fundamental output frequency	50 Hz
Rated output power	5 kW

capacitors [16]. Thus, the active miller clamp function of ACPL-332J was utilized to depress the miller effect. Besides, the desaturation protection method was utilized by monitoring the on-state drain-source voltage of the SiC MOSFET to avoid shooting through fault.

The gate driver is a four-layer printed circuit board (PCB). In each gate loop, the emitter lines and gate lines are routed at different layers. The DC-DC converters are separately placed at another PCB which connects the gate drive board via the pins. Through such a design, the gate loop is perpendicular to the power loop of the HyS module. The trenches are dug everywhere isolation is needed to ensure the safety. The gate driver board is soldered to the gate pins of the HyS power module to minimize the parasitic inductance within gate loop. Details of the gate driver can be found in [27].

Test procedures are as follows. At first, only the Si IGBTs in the HyS power modules were switched. The SiC MOSFETs were kept in off state. The switching frequency was 5 kHz. Then the gate sequence with the fixed t_{on_delay} of 1 us (Option 2) and −1 us (Option 3) respectively and the fixed t_{off_delay} of 0.5 us was applied. The switching frequency remained

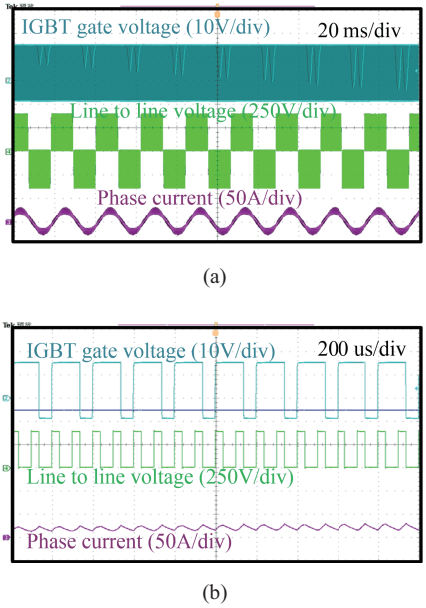

Fig. 16. Experimental waveforms of the three-phase voltage source inverter. Only the Si IGBTs were switched. (a) Gate voltage, line to line voltage and phase current waveforms. (b) Zoom-in waveforms. Switching frequency was 5 kHz. (200 us/div)

as 5 kHz. At last, the gate sequence with non-constant t_{off_delay} (Option 1) was utilized. t_{on_delay} was set to be 0 us. The switching frequency was 5 kHz, 10 kHz, and 30 kHz respectively. The gate sequences were realized through the PWM module of the DSP F28335. Experimental waveforms are demonstrated from Fig. 16 to Fig. 19. The gate voltages were obtained at the lower leg of the middle HyS power module and the positive phase current flowed through the HyS.

Fig. 16 displays the experimental waveforms of the three-phase voltage source inverter. Only the Si IGBTs within the HyS power modules were switched. Gate voltage of the SiC MOSFETs was kept at −5 V to disable the switches. There were almost no disturbances on the gate voltage of the SiC MOSFETs at the switching transients of the Si IGBTs. Switching frequency was 5 kHz. PT1000 thermistor was attached to the baseplate of the middle HyS power module. Baseplate temperature was utilized as an indicator of the HyS power loss. Air flow of the fans is 0.5 m^3/min. As the output power increased from 1 kW to 5 kW, the baseplate temperature rose from 25 °C to 50 °C.

Fig. 17 displays the experimental waveforms of the three-phase voltage source inverter utilizing the gate sequence Option 2 with the fixed t_{on_delay} of 1 us and the fixed t_{off_delay} of 0.5 us. Si IGBTs were turned on prior to the SiC MOSFET. With a positive t_{off_delay}, the Si IGBTs are expected to be turned off prior to the SiC MOSFET. However, a short t_{off_delay} may be not enough. There are two reasons for the increase of the gate voltage of the Si IGBTs (shown in Fig. 17(d)). The first one is the miller effect. Even though an active miller clamp circuit was utilized, the circuit was not supposed to work when the gate voltage of the Si IGBTs was still high. That is, a short

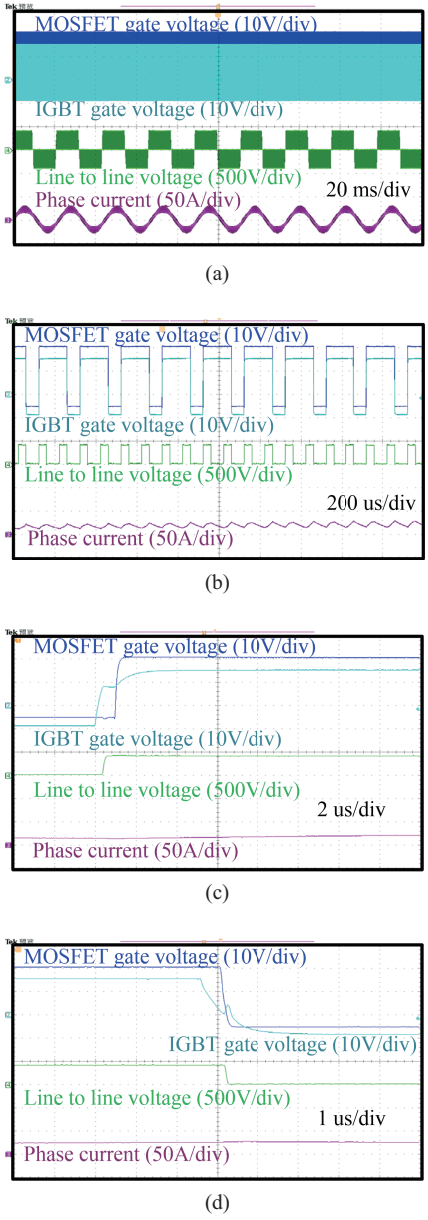

Fig. 17. Experimental waveforms of the three-phase voltage source inverter. Gate sequence Option 2 with the fixed t_{on_delay} of 1 us and the fixed t_{off_delay} of 0.5 us was applied. (a) Gate voltages, line to line voltage and phase current wave-forms. (b) Zoom-in waveforms. Switching frequency was 5 kHz. (200 us/div) (c) Zoom-in waveforms at the turn-on instant. (d) Zoom-in waveforms at the turn-off instant. The Si IGBTs turned on again at the turn-off moment of the SiC MOSFET because t_{off_delay} was small for the load current.

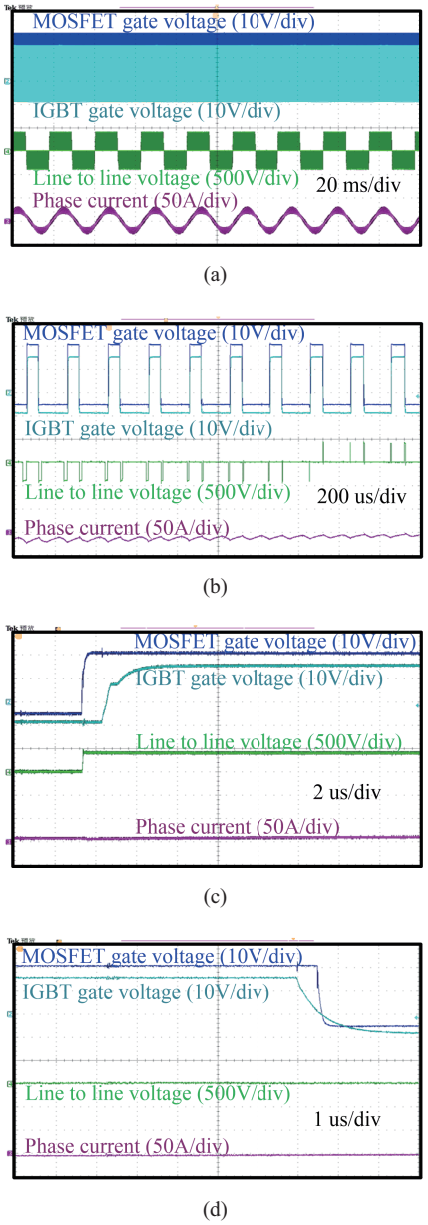

Fig. 18. Experimental waveforms of the three-phase voltage source inverter. Gate sequence Option 3 with the fixed t_{on_delay} of −1 us and the fixed t_{off_delay} of 0.5 us was applied. (a) Gate voltages, line to line voltage and phase current wave-forms. (b) Zoom-in waveforms. Switching frequency was 5 kHz. (200 us/div) (c) Zoom-in waveforms at the turn-on instant. (d) Zoom-in waveforms at the turn-off instant. The Si IGBTs did not turn on again at the turn-off moment of the SiC MOSFET because t_{off_delay} was long enough for the load current (Load current was negative and did not flow through the HyS).

t_{off_delay} may disable the function of miller clamp circuit. The second reason is that the depletion layer expands toward the collector within the N- region of the Si IGBTs, which not only drives the excess carriers away from the N- drift region but also makes an accumulation layer form under the P+ collector. Hereby, both collector current and gate voltage rise. Both phenomena can not be avoided and can become severer at a larger current. A longer t_{off_delay} is helpful for suppressing the effects.

The baseplate temperature rose from 25 °C to 35 °C as the output power increased from 1 kW to 5 kW. Better performance of the HyS compared with the pure Si IGBTs was observed.

As shown in Fig. 18, compared with the gate sequence Option 2, the gate sequence Option 3 reduces the turn-on loss. Thus, a lower baseplate temperature as 30 °C was obtained at the output power of 5 kW.

Fig. 19 displays the experimental waveforms utilizing the gate sequence Option 1. The lowest temperature was observed because it fully utilized the potential of the HyS. As switching frequency increased to 30 kHz, the baseplate temperature was 67 °C at the rated output power. Replacing the fans with the water-cooling plates, the inverter was tested at 30 kW/ 30 kHz,

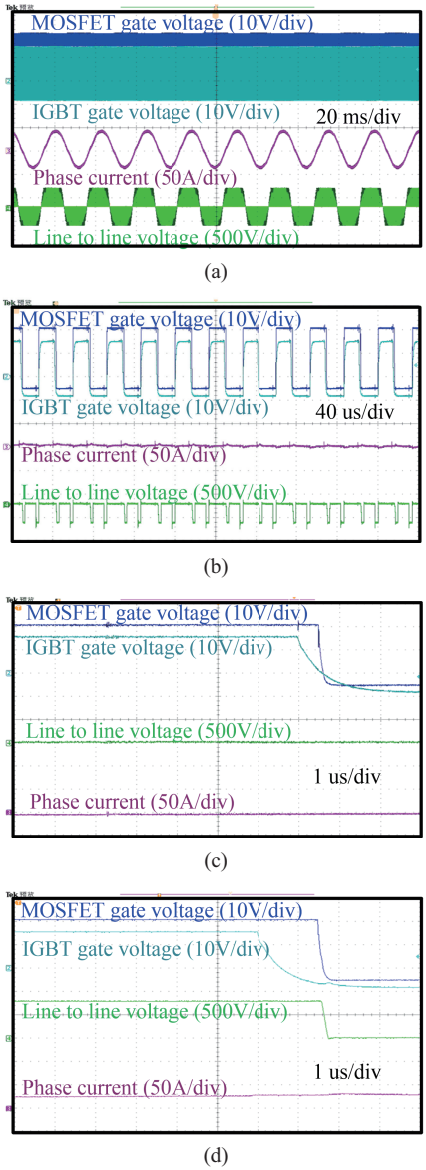

Fig. 19. Experimental waveforms of the three-phase voltage source inverter. Gate sequence Option 1 with the non-constant t_{off_delay} was applied. (a) Gate voltages, line to line voltage and phase current waveforms. (b) Zoom-in waveforms. Switching frequency was 30 kHz (40 us/div). (c) Zoom-in waveforms at the turn-off instant. Small t_{off_delay} (0.5 us) was utilized because of the little load current. (d) Zoom-in waveforms at the turn-off instant. Large t_{off_delay} (1.5 us) was utilized because the load current became larger.

shown in Fig. 20. Inlet cooling temperature was set to be 30 °C.

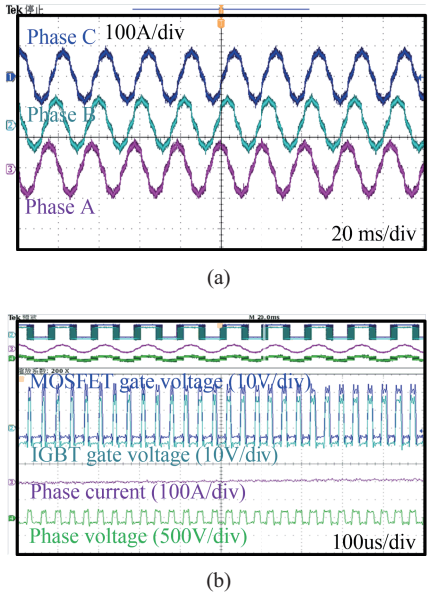

Fig. 20. Experimental waveforms of the voltage source inverter (30 kW/30 kHz). (a)Three phase current. Amplitude of the current was 100 A. (b) Zoom-in waveforms. Switching frequency was 30 kHz. DC bus voltage was 550 V.

VI. Conclusion

A Si IGBT/SiC MOSFET HyS power module was packaged. The Si/SiC current ratio is 4:1. A novel index is proposed to determine the optimal prior turn-off period of the Si IGBTs. Compared with the pure Si IGBTs, the HyS can operate at a higher switching frequency with the reduced power loss. A 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were built for verification. The main features of the paper are as follows.

(1) HyS phase-leg power modules were fabricated and fully tested for the first time.

(2) A method to select the optimal gate sequence for the HyS is presented.

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Impacts of High Frequency, High d*i*/d*t*, d*v*/d*t* Environment on Sensing Quality of GaN Based Converters and Their Mitigation

Bo Liu, Ren Ren, Zheyu Zhang, Ben Guo, Fei (Fred) Wang, and Daniel Costinett

***Abstract*—A systematic study on a gallium nitride (GaN) high-electron-mobility transistor (HEMT) based battery charger, consisting of a Vienna-type rectifier plus a dc-dc converter, reveals a common phenomenon. That is, the high switching frequency, and high d*i*/d*t* and d*v*/d*t* noise inside GaN converters may induce a dc drift or low frequency distortion on sensing signals. The distortion mechanisms for different types of sensing errors are identified and practical minimization techniques are developed. Experimental results on the charger system have validated these mechanisms and corresponding approaches, showing an overall reduction of input current total harmonic distortion (THD) by up to 5 percentage points and improved dc-dc output voltage regulation accuracy. The knowledge helps engineers tackle the troublesome issues related to noise.**

***Index Terms*—Charger, dc bias, gallium nitride (GaN), sensing, three-phase rectifier, wide bandgap.**

I. Introduction

LOW on-resistance and high switching speed have driven the research, commercialization, and application of wide bandgap (WBG) power semiconductor devices, such as SiC and GaN devices, for a more efficient and compact converter design [1]–[3]. However, as WBG devices are applied in practice, more design issues arise, such as the need for optimal power loop layout and device package to reduce parasitics [4], [5], thermal management for low profile devices [6], gate driver noise immunity for fast switching [7]–[9]. And high d*i*/d*t* and d*v*/d*t* are regarded as the main obstacles to electrical performance improvement of WBG converters. High d*i*/d*t* induced ringing and overvoltage in the switching commutation loop introduces high voltage stress, extra loss, and severe radio frequency (RF) emission and electromagnetic interference (EMI). High d*v*/d*t* noise often induces spurious gate voltage, resulting in cross-talk issue in bridge configurations. Besides, the high common mode (CM) voltage transient due to high d*v*/d*t* may cause the false trigger of gate drive ICs. Many works have been done in addressing these d*i*/d*t* and d*v*/d*t* issues through gate driver design [7], [10]–[14] and power stage optimization [4], [5].

Meanwhile, as switching frequency and speed increase in SiC and GaN based converters, some control challenges have been observed recently in applications of high speed and high switching frequency devices, e.g., zero-crossing detection error occurs in peak current control due to EMI distortion in GaN based high frequency buck [15]; several sensing distortions and conditioning circuit arrangements in 500 kHz GaN full bridge converter are reported [16]; and device parasitics can impact on current harmonics in a high frequency three-level GaN rectifier [17], [18]. These previous studies have clearly shown the impacts of high frequency, high d*i*/d*t*, d*v*/d*t* on sensing, conditioning, and control circuits. However, they were more specifically focused on one aspect of these complex issues and did not provide comprehensive relation between high d*v*/d*t*, d*i*/d*t*, high frequency operation environment and sensing and control.

Particularly, signal sensing and processing in the feedback path become the vulnerable link, as signal integrity issues arise due to capacitive coupling from d*v*/d*t* and inductive coupling from d*i*/d*t*. Although these are commonly perceived by engineers and some are well known in information electronics field, few work has been reported in power electronic field to explain some of the phenomena and effects that are specifically associated with high frequency noise and transients. In the work, it is observed experimentally that high frequency noises in GaN based power converters could surprisingly induce nonlinear dc or low frequency shift on the sensing signals through the sensing and conditioning circuitry and lead to deviation from the desired control track as well as voltage/current distortion, if without a proper design.

In this paper, to address the above challenges in WBG based high switching frequency converter design, a systematical study will be conducted in a proposed two-stage charger consisting of three-level/phase Vienna-type power factor correction (PFC) rectifier and three-level LLC dc-dc converter as shown in Fig. 1. Instead of further stressing the high frequency noise itself, the

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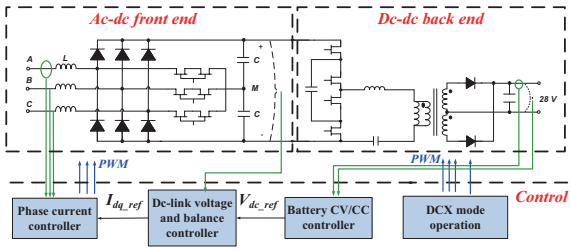


Fig. 1. Schematic of the proposed GaN based two-stage battery charger system including power stage and control structure.

focus will be on illustrating why and how these high frequency distortions produce dc and low frequency sensing error and impact the ac or dc feedback voltage/current control, and the way to mitigate these noises in different situations. Considering that feedback control has no rejection capability for disturbances in the feedback path, understanding and fixing these issues are crucially important.

This paper is organized as follow: Section II presents the overall system topology, the control architecture and sensing arrangement, and the power quality requirement. Section III first introduces several dc and low frequency sensing distortions related to high speed and high frequency WBG converters, and then analyzes the mechanisms of different sensing distortions and proposes the mitigation methods. Of which, one of the major dc bias phenomena and its mechanism and influencing factors presented in subsection A have never been investigated before. Section IV provides experimental results. And Section V concludes this paper.

II. Sensing and Control Architecture in a GaN Based Charger

A. Control Functions and Sensing Arrangement

A proposed two-stage GaN based battery charger is applied as an example to study the sensing issues. As given in Fig. 1, the front end is a 650V enhancement-mode GaN based three-level Vienna-type rectifier operated at 450 kHz switching frequency [17], [18], and the back end is a three-level LLC resonant dc-dc converter which adopts 650 V GaN devices at the primary side and 100 V EPC devices at the secondary side [19]. The charger converts 115 V_{rms} or 235 V_{rms} ac voltage to a maximum 28 V_{dc} output for batteries in aircraft application.

To properly charge the batteries and efficiently operate the charger, LLC converter is operated in dc transformer mode (DCX) with switching frequency fixed at the resonant frequency. Its dc output voltage and current are regulated indirectly by varying the dc-link voltage of the front-end rectifier, where the dc output voltage and current are sensed as the feedback signals for the constant voltage (CV) and constant current (CC) controllers. The output of CC/CV controller is then used as the reference for PFC dc-link voltage controller, which further generates the inner current control reference for phase current regulation.

For the studied system, three current hall sensors are therefore placed at the ac side, and one hall sensor is placed at the dc output side. Meanwhile, the intermediate dc-link voltage as well as dc capacitor voltage is sensed through differential voltage divider pairs, then processed through an instrumentation amplifier, and finally converted to a single-ended signal, whereas the dc output voltage at the low voltage secondary side is sensed through a voltage divider and transmitted via an analog isolated amplifier before it is processed by conditioning circuit on the interface board.

B. Power Quality Requirement

For grid connected inverters or rectifiers, power quality including current harmonic and power factor limits are required by various standards, such as IEC 61000–3–2 [20], IEEE 519–2014 [21], and DO–160E [22]. For dc-dc converters interfacing with local load, such as POL or back end of a battery charger, the accurate regulation of voltage and current is also required [23], [24]. For this aircraft charger, DO–160E standard is followed in which the limit of each order harmonic up to 40th order is specified and the current total harmonic distortion (THD) should be less than 3%, meanwhile the leading power factor should be above 98%.

Although one may expect that good current quality and voltage regulation accuracy can be more easily obtained as a result of higher control bandwidth and lower switching ripple if pushing the converter to high switching frequency, e.g. exploiting WBG devices,it is not always true due to aforementioned challenges in Introduction. Understanding and mitigating the unique dc and low frequency distortions associated with high-speed high-frequency WBG devices are therefore presented in the following section.

III. Sensing Issues and Mitigation Methods

To address these sensing issues in the noisy operation environment, the causes of dc and low frequency bias on sensing signals are firstly understood including two main distortion mechanisms. Mitigation schemes are then discussed for each case.

A. DC Bias from Analog Signal Isolation Amplifier and Mitigation

1) Observed DC Bias on Isolated Voltage Sensing

When isolation is mandatory, voltage or current sensing is often realized by isolation schemes shown in Fig. 2. An analog isolation amplifier (iso-amp) is the key device to achieve the isolation between control and power domains. At the high-power side of an iso-amp, the voltage will be sampled by a resistor divider in a single-ended form or by a divider pair in a differential form. The current will be sampled through a shunt resistor. Then, the isolated sensing signal is processed by downstream conditioning amplifiers and filters before being transmitted to ADC. However, operated in high dv/dt conditions, this scheme is observed to suffer severe distortion, i.e. a nonlinear dc shift, in the GaN based charger system.

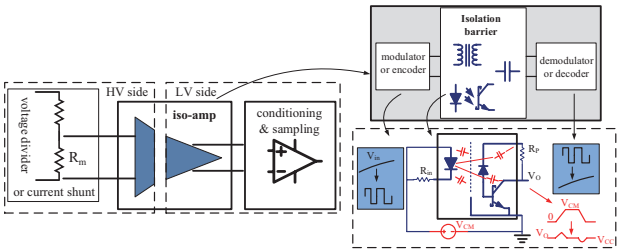


Fig. 2. Iso-amp function block and formation of dc bias through CM noise penetration and demodulation.

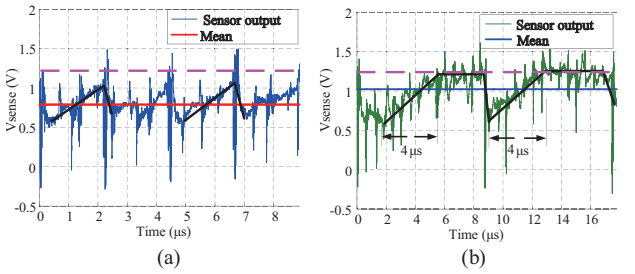


Fig. 3. LLC voltage sensing distortion: (a) 450 kHz PFC. (b) 450/4 kHz PFC. Black line outlines the profile of output signal. Dashed magenta line denotes the desired voltage.

Although LLC resonant converter has much lower EMI emission, the front-end PFC is operated at hard-switching mode with high d*v*/d*t* GaN devices, emitting high amount of noises either conductively or radiationally to its surrounding. Although it is understandable that certain high frequency noise might be coupled onto the sensing signal of LLC output voltage, it is surprising to observe a significant dc bias in the sensed dc voltage. As shown later in Fig. 4, the dc error could be 6 V more.

Because of the sensing voltage shift ΔV_{dc}, the actual voltage regulated by feedback closed loop control is different from the desired value as in (1). This dc error is even larger when the dc-link voltage increases as if a nonlinear voltage-dependent sampling gain exists. For high step-down dc-dc and low output voltage applications, this dc error would be unacceptable.

$$V_{actual} = V_{ref} - \Delta V_{dc} \tag{1}$$

2) Origin of DC Bias

The dc bias from analog signal isolation amplifier in this paper can be understood from the basic structure of an analog iso-amp in Fig. 2, where the analog input is modulated into digital format, e.g. via a sigma-delta ADC at the primary side, and the signal is reconstructed to analog output via a demodulator at the secondary side. An intermediate digital transmitting medium is implemented across the isolation barrier of the iso-amp. As a result, a high CM voltage exists due to the different grounding potential. Taking optical iso-amp as an example, when a rising v_{CM_r} pulse is imposed onto an iso-amp, the internal coupling capacitance of iso-amp induces CM current pulses penetrating the barrier, and a positive differential voltage spike is generated at the output through the pull-up resistor. In addition, the turn-off pulse also induces a negative spike v_{CM_f} at the output. These spikes may falsely toggle the logic level, jeopardize the signal quality of effective signal and finally demodulate analog spikes. Thus, a dc bias can consequently be generated after the downstream filter through the average of these positive and negative analog spikes. This relationship is shown in (2). It should be noticed that the polarity of the spikes could be reversed depending on internal logic of an iso-amp IC.

$$\begin{aligned} \Delta V_{dc\_out} &= \int_0^{T_s} (v_{CM\_r} - v_{CM\_f})\, dt/T_s \\ &= f_s \cdot \int_0^{T_s} (v_{CM\_r} - v_{CM\_f})\, dt \end{aligned} \tag{2}$$

3) Impact Factors of dv/dt Induced DC Bias

a) CM dv/dt in power converter

The magnitude of this CM isolation voltage is determined by the dc-link voltage and CM impedance distribution along the whole CM path including grounding parasitics, transformer inter-winding capacitance of dc-dc converter, isolation capacitance of the iso-amp, etc. The edge slopes of this voltage are related to d*v*/d*t* of device turn-on and turn-off, determined by specific gate driver, gate resistance, switching speed, and dc-link voltage. The turn-off d*v*/d*t* is also strongly impacted by load current level.

b) Asymmetric of dv/dt transient

If the turn-on and turn-off d*v*/d*t* are the same, it seems reasonable that a minimum dc bias might be induced per (1). However, in practice, the two d*v*/d*t* values might be different due to the junction capacitor charging effect, load current, and different gate drive on/off speed control. For GaN based application, this d*v*/d*t* disparity becomes larger. The turn-on transient of 650 V e-mode GaN device is usually less than 10 ns and d*v*/d*t* can be above 100 kV/μs, while its turn-off transient could last for hundreds of ns at ac current zero crossings [25], [18]. Thus, turn-on d*v*/d*t* becomes the primary contributor to the CM transient immunity (CMTI) issue instead of the turn-off d*v*/d*t* at low current level or zero crossing. This is further verified by LLC voltage sensing results in experiment with front-end PFC operating at two different switching frequencies. As shown in Fig. 3, the turn-on d*v*/d*t* induced negative spikes (below the desired voltage sensing level as marked in dashed magenta line) are almost the same in case (a) and (b), whereas no positive peaks show up except for some noises.

c) Transient speed of iso-amp

The above results also highlight another important distortion factor that was not considered previously, i.e. the output signal rise/fall time of an iso-amp IC. Ideally, the output spike due to d*v*/d*t* should only occur during the switching transient. However, it is noticed that at different switching frequencies, the profiles of the output ripples in Fig. 3(a) and (b) have rising ramps which increase linearly from the same negative valley. This is caused by the relatively slow rise time of the iso-amp ACPL-C87B output, roughly 4 μs [26]. For example, in the 450 kHz switching frequency case, the d*v*/d*t* induced spike is reset by the

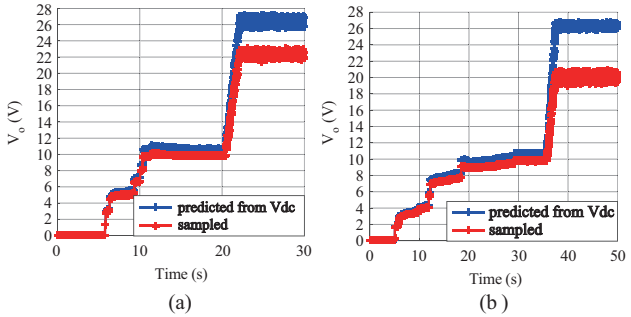


Fig. 4. Recored experimental data of LLC output voltage sampling: (a) 450/4 kHz PFC. (b) 450 kHz PFC.

next switching event before it can reach the steady state level within its 2.2 μs cycle. Whereas in the 112.5 kHz case, the d*v*/d*t* related ripple can jump back to the desired dc voltage in one switching cycle.

d) Switching frequency

Switching frequency will not impact the peak spike of an iso-amp output, but it does impact the dc bias level. This is because: 1) the same noise spike pattern will be averaged over different switching periods, thus the bias is proportional to f_s, as shown in (2); 2) the noise spike of an iso-amp may not reach the correct sensing level if the switching cycle is too short as analyzed above. As a result, high frequency induces more dc sensing drift.

From the experimental results in Fig. 4 recorded by DSP controller, the sampling voltage of LLC output marked in red is compared with the actual voltage marked in blue predicted via the intermediate dc-link voltage and the LLC dc gain (matching the digital meter measurement), at two different frequencies. In the steady-state when the front-end PFC is activated after the soft-start and diode rectification, LLC output voltage sampling begins to suffer high dc shift, and it is clear that this dc shift becomes much higher when PFC is operated at 450 kHz compared to the case at ¼ of 450 kHz.

In sum, the speed of iso-amp, i.e. the rise/fall time, impacts the sensing output distortion induced by CM spikes. More instantaneous distortions and dc bias will be introduced when higher switching frequency, lower speed sensing iso-amp, and higher speed devices are adopted.

4) Mitigation Solutions

The above analysis has shown that the dc bias issue is not just by the switching noise propagation, but it is at the basis of the demodulation of the interference. With high CMTI and fast speed iso-amp, this effect could be suppressed. Unfortunately, the CMTI of the commercial analog iso-amp is relatively low in comparison with GaN device turn-on d*v*/d*t*. TABLE I lists the state-of-the-art commercial iso-amps. As it can be seen, the CMTI of some products is not precisely defined [26], [27]. Detailed information of iso-amp error levels vs. CM voltage or d*v*/d*t* is also unknown, which further increases the difficulty of sensing circuit design. The state-of-the-art commercial voltage sensing iso-amp was from Avago before year 2018, typical with 15 kV/μs CMTI [26] using optocoupler isolation, and current sensing iso-amp has up to 75 kV/μs CMTI [27] using CMOS isolation. Thus, CMOS based iso-amp is a better option currently, since it shows higher CMTI due to RF transmission. To be noted, recently an even higher CMTI voltage sensing iso-amp AMC1311B from Texas Instruments was released in early 2018 [28].

TABLE I
KEY PARAMETERS OF STATE-OF-THE-ART COMMERCIALLY AVAILABLE ANALOG ISOLATION AMPLIFIERS

Amplifier names	Isolation techniques	Bandwidth (kHz)	CMTI (kV/μs)	t_r and t_f (μs)
ACPL-C87B	Optical	100	[a]15 (typ), 10 (min)	2.7 (typ), 4.0 (max)
ACPL-790B/A/0	Optical	200	[a]15 (typ), 10 (min)	1.7 (typ)
Si8920A/B	CMOS	950	[b]75 (typ), 50 (min)	0.42 (typ)
AMC1311B	SiO_2	275	[c]140 (typ), 75 (min)	1.3 (typ)
AMC1311	SiO_2	220	[c]30 (typ), 15 (min)	1.3 (typ)

[a]CMTI failure is defined as the output error of 200 mV deviation from the average output voltage persisting for at least 1 μs, tested at V_{CM} = 1 kV.

[b]CMTI failure is defined as the output error of more than 100 mV persisting for at least 1 μs, tested at V_{CM} = 1.5 kV.

[c]CMTI failure definition is not specified, tested at V_{CM} = 1 kV.

To obtain better voltage sampling quality in high d*v*/d*t* operation, the 75 kV/μs CMTI current sensing iso-amp Si8920B from Silicon Lab is finally selected, considering its tight CMTI definition and higher CM testing voltage, as well as the fastest rise and fall time during the transient. In order to apply this amplifier for voltage sensing, reconfiguration is needed. Since the internal input resistance of this shunt-input iso-amp is much lower than the typical high impedance of the voltage sensing iso-amp, e.g. 37 kΩ only for Si8920B, the resistance of the voltage divider should be properly selected. Higher resistance will lead to the failure of impedance mismatching, while a lower value will introduce additional power loss. The trade-off between the sensing accuracy in terms of voltage divider load dependence and the extra loss introduced by sensing resistors is thus required for a set of given system parameters. For 28 V sampling using Si8920B, as the allowable input voltage is within 0.25 V, the voltage divider ratio is determined as 175. The sensed lower side resistor is chosen as 110 Ω and the upper resistor is 19.1 kΩ, giving a total 40 mW loss at 28 V. Both have 0.1% high accuracy. Impedance mismatch ratio between 110 Ω and 37 kΩ is 0.3%, ensuring enough accuracy for this current sensing iso-amp.

Optionally, common mode filters may be possible to use at the high side of the iso-amp to limit the CM voltage across the iso-amp. This will be similar to the approach for CMTI enhancement of the gate driver [29]. However, the power supply lines should also be in series with the CM filter to avoid

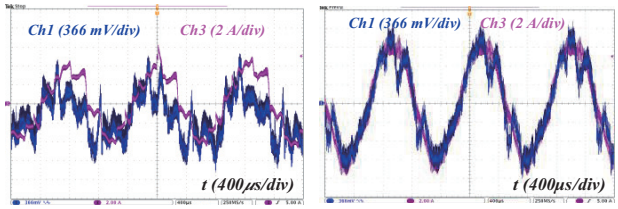


Fig. 5. Experimental waveforms of ac current sampling: (a) 450 kHz PFC. (b) 450/4 kHz PFC. (Ch1: sampled signal, Ch3: current probe result)

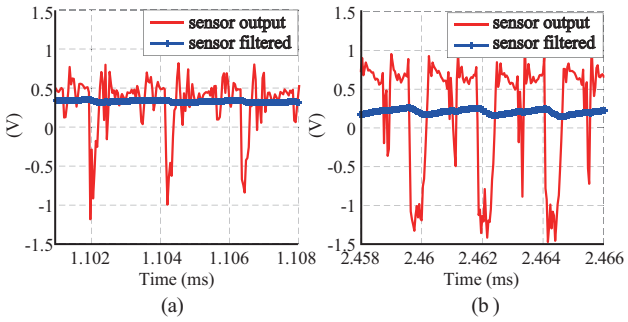


Fig. 6. Experimental waveforms of ac current sensor output with 450 kHz PFC. (a) Higher line current instant. (b) Lower line current instant. (Due to 25 MHz low bandwidth voltage probe used in the test, only the noise envelop is captured where the higher frequency oscillations are not accurate.)

high CM voltage stress across the high side pins of the iso-amp.

B. DC Bias From RF Interference Rectification in Op-amp and Mitigation

For silicon device switching at tens of kHz, a moderate filter implemented in the conditioning circuitry is sufficient to guarantee the integrity of sensed signals. However, when using the similar design principles in GaN based converters, the experimental results reveal that the voltage and current sensing signals along the conditioning circuitry could see a pronounced dc offset or low frequency distortion, which further grows as dc bus voltage or switching frequency increases. An example of ac current sensing at 450 kHz and 112.5 kHz switching frequencies in a GaN based Vienna-type rectifier is provided in Fig. 5, where the sampling signal outputted by digital-to-analog converter (DAC) is much different from the Keysight current probe result. At higher switching frequency, this low frequency or dc shift becomes larger. It should be mentioned the poor quality of the ac current is due to several distortions including the sensing distortion, sampling distortion [30], [31] and the PWM voltage loss during the current zero crossings [18].

1) Identification of Observed Sensing Noise Pattern

To identify the cause of this distortion, the output signal of the hall sensor is checked. High switching transient noises are observed in the sensor output as shown in Fig. 6. Since the onboard sensor is placed close to the main power loop, the noise is found induced by high d*i*/d*t* of switching transients. And noise at turn-on seems more pronounced than that at turn-off, which can be explained from the fact that at turn-off,

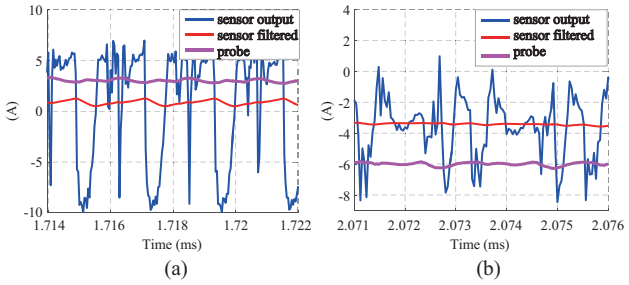


Fig. 7. Comparison between onboard sensor output (blue) and current probe result (magenta) at different current levels with 450 kHz PFC in switching cycle scale. (a) Current instant at the positive line cycle. (b) Current instant at the negative line cycle.

commutation from off-device to on-device is largely determined by load current charging.

The sensor output, ADC sampling, and probe measurement are further compared. From results in Fig. 7, both the sensor output and final ADC sampling have dc shift distortion in switching period scale and low frequency distortion in line period scale. Although the coupled noise and dc shift patterns may be different at different operation points, making the analysis intricate, some key observations are captured: 1) due to the asymmetric nature of the coupled HF noise as mentioned in Section III-A, the mean value of sensor output over a switching period can be shifted from the original level and falsely conveyed to the downstream conditioning amplifier; 2) this dc shift is thus influenced by switching frequency; 3) the fact that an offset also exists between the envelops of the sensor output and probe result, indicates the sensor itself is also affected by the HF noise.

2) Origin of DC Bias and Low Frequency Distortion

Eventually it is found that this dc severe distortion is determined by the amount of high d*i*/d*t* induced noise picked up by signal-ground traces between sensor output and conditioning amplifier input. And the cause of this dc bias is the radio frequency interference (RFI) rectification effect on operational amplifiers (op-amp) [32]–[39], a phenomenon seldom considered in power converter field. According to it, when an op-amp sees high frequency out-of-band noises at its input, its output can induce an instantaneous dc shift due to the nonlinear I-V characteristics of differential transistor pairs at its input stage. And the strength and envelop of the time-domain bias are dependent on the amplitude, frequency and continuity of the input coupled out-of-band noise. Furthermore, noise coupled at the output of an op-amp can also contribute to the input noise via its feedback path. This explains why dc shift at current sensor output was observed, as an internal op-amp exists at the output stage of the current sensor to provide desired quiescent bias [41], [42].

To help understand this rectification effect for power engineers, a brief introduction is provided. RFI rectification was firstly observed in naval research on the susceptivity of transistors to microwave energy [32], [33]. Since then, the effects and mechanisms of RFI distortion on analog and digital ICs have been investigated experimentally and theoretically, in both time domain and frequency domain [32]–[39]. Analog

electronics, in particular, the amplifiers are most susceptive to the EMI noise. Technical notes from industry have attributed the dc bias effect on op-amp to the nonlinear transfer characteristics of its input transistors, e.g., emitter-coupled BJT has exponential I-V curve and source-coupled JFET or CMOS have quadratic I-V curve [34], [35]. Although this theory can confirm the observation that BJT-based amplifiers typically suffer higher RFI distortion than other types, it fails to explain why this effect only occurs at out-of-band frequencies and why the dc offset varies with frequencies. The frequency-dependent nonlinearity and dc bias level was later analytically modeled in [36] for a CMOS op-amp, indicating that the parasitic capacitances C_{gs} of input differential pairs and their total source-to-ground capacitance are the determinants. The mechanism of negative feedback on dc bias was also revealed in [36], [37] for CMOS op-amp. It is noticed that some models are only valid at low level RF input, i.e. two transistors of the input differential pairs are both in saturation region [37], while other models may be feasible for both saturation region and subthreshold region where large signal noise switches the transistor on and off [36].

The susceptivity of an amplifier to RFI EMI can be evaluated by a rejection ratio (EMIRR) [38], from which the corresponding dc bias can be estimated as (3). However, this is only valid at low amplitude EMI/RF [39].

$$\Delta V_{dc} = \frac{1}{10^{\left(\frac{EMIRR_{IN}(dB)}{20}\right)}} \left(\frac{V_{RF\_peak}}{100mV} \right)^2 \tag{3}$$

To further verify the RFI offset issue identified in this work and evaluate EMIRR of the adopted op-amp OPA2227 in cascaded inverting configuration for feedback current conditioning, offline characterization of the OPA2227 is carried out, whose test setup is provided in Fig. 8, using a signal generator to mimic the output of the hall sensor with varying HF noise and injecting the EMI source via a 50 Ω BNC cable.

From results in Fig. 8(b), as RFI amplitude increases, the dc shift becomes larger and occurs earlier. This dc offset also presents nonlinear frequency characteristics. It grows larger as frequency increases from 500 kHz to 2 MHz and then drops back to almost zero around 10 MHz. Testing at even higher frequency is not performed, due to measurement complexities involving reflection effects of input cable, PCB traces and op-amp pins.

3) Mitigation Approaches

A straightforward approach to mitigate the RFI effect is to attenuate EMI noise before the input pins of an op-amp. RC-based CM and DM filters have been built in some commercial amplifiers [35]. However, the filter corner frequency is usually set above tens of MHz to serve general purposes, beyond interested frequency range of the state-of-the-art GaN based power converters. Therefore, a set of external EMI filter should be provided for converter sensing design, as shown in Fig. 9.

For single-ended signals, RC or LC filter can be applied whose bandwidth should be selected between the current control bandwidth frequency and the high switching frequency,

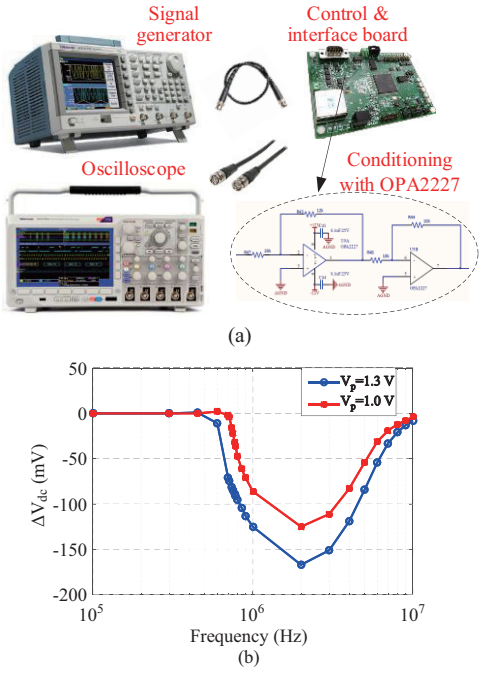


Fig. 8. EMIRR characterization of op-amp OPA2227 in current conditioning circuit. (a) EMIRR measurement setup. (b) Measured RFI induced dc offset on OPA2227 with cascaded inverting configuration.

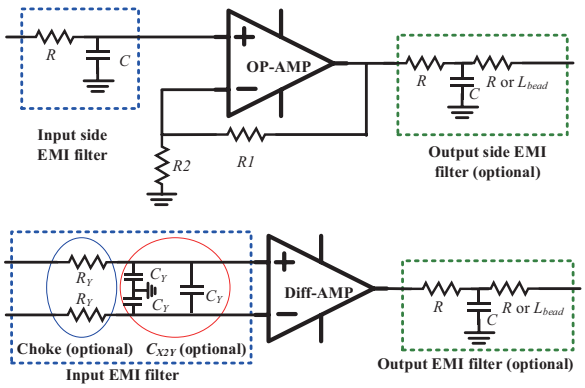


Fig. 9. Recommended filter approaches to mitigate amplifier RFI issue. (Upper for general op-amp and lower for differential amplifier).

e.g. in the middle range, without impacting obvious delay to the feedback control. For differential sensing signals, both CM and DM filters should be adopted following similar design consideration, where the DM filter corner frequency is determined by (4) and the CM filter corner frequency decided by (5) can be slower as it does not affect the feedback control.

$$f_{DM} = \frac{1}{2\pi R_Y (2C_X + C_Y)} \tag{4}$$

$$f_{CM} = \frac{1}{2\pi R_Y C_Y} \tag{5}$$

However, unlike signal processing, power conversion deals with high voltage and current. Particularly, in GaN based converter, high d*i*/d*t*, d*v*/d*t* and high frequency could likely

induce strong noise coupling. Relying purely on filter itself is not effective enough to eliminate RFI noise without sacrificing sensing bandwidth. In fact, as earlier work reported in [16], the pre-filtered voltage sensing circuit can still be distorted once active power control is activated, leading to the design compromise by moving the local sensing circuit of the power board far away and placing onto another board. This prevents further degrees of power function integration, especially for intelligent power module design.

Differently, this paper will show that the direct control of the noise source and associated coupling path is more effective and straightforward. Taking current sensing distortion as an example, if tracing back to the source of the hall sensor noise, it is actually induced by high d*i*/d*t* current circulated in the switching loop and then coupled onto the signal side of the sensor through space magnetic coupling. Given the fixed d*i*/d*t*, smaller power loop means less diffusing magnetic field generation, thus reduces the magnetic coupling. However, less loop inductance can adversely induce higher d*i*/d*t* and d*v*/d*t* [40]. Since power loop layout has been well studied in literature, details are not covered here. Instead, this paper emphasizes the importance of signal loop layout for sensing design. In high power density converter design, surface-mount hall sensor chip is preferred due to its low profile and weight. When it is placed on the power board close to converter terminals, longer traces of control power supply nets and output nets are needed to interface with the control board, thus prone to taking in the high d*i*/d*t* induced voltage noise. Therefore, an effective solution is to layout the sensor circuit and the conditioning circuit with the lowest loop area, in addition to the front-end filters. The basic concept is shown in Fig. 10, where three traces including control ground, control power line, and sensing signal should all be tightly placed on both the power board and the control board.

To implement this scheme, a vertical trace arrangement is proposed to minimize the area of two types of signal loops. In addition, the hall sensor interface loop and power supply loops should be paralleled to the flux orientation and orthogonal to the switching loop, so that the coupling could also be reduced.

Two layout designs are developed for the three-phase ac current sensing. The three-phase sensors are placed next to the switching nodes of the rectifier, and their low side signals have to go across three power traces to the interface connector on the left side where the control interface board is stacked. Compared to the design in Fig. 11(a) with large VCC-GND loop and signal-GND loop on phase B and C, the improved current sensor layout for phase B and C is proposed in Fig. 11(b). The first improvement is that multi-radial power lines are applied for all three sensor chips instead of the central power lines. This decouples possible noises among three-phases and ensures good power quality for each sensor. VCC lines for three sensors directly connect to the main VCC plane, and GND lines also start directly from the GND plane. In addition, all signals are embedded in the mid-layers and overlaid with power lines, to form vertical loops with minimized coupling area. And next to each sensor, reasonable size ground plane is also designed to provide a stable ground potential to each chip.

Finite element analysis (FEA) has been conducted to study

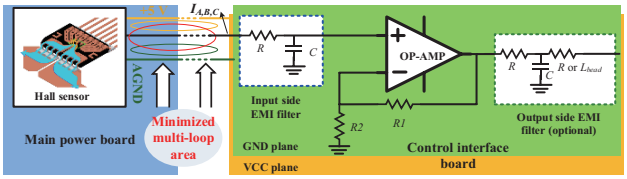
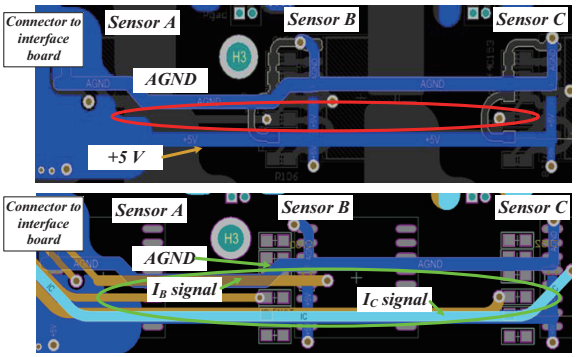
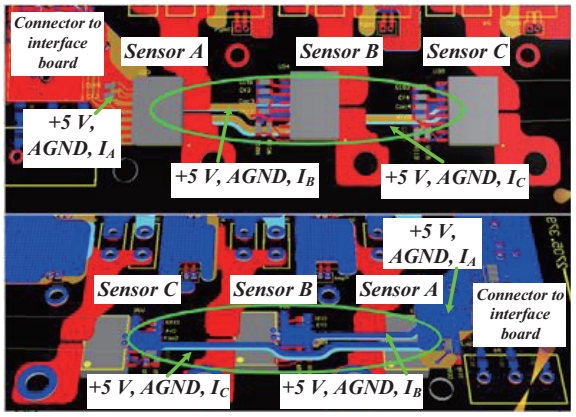


Fig. 10. RFI noise suppression approach through PCB layout for op-amp based sensing circuit. EMI filter can be optional.



(a)



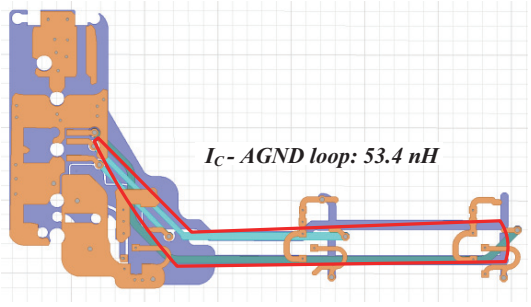
(b)

Fig. 11. Comparison of current sensor layouts on main power board. (a) Large VCC-GND (upper) and signal-GND (lower) loops in the first version design. (b) Small VCC-signal-GND vertical loops with radial power distribution of the improved layout. Top view (upper), bottom view (lower).

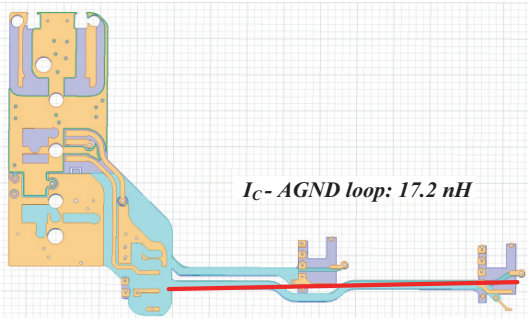
the impact of layout approaches to the loop inductance as shown in Fig. 12. The final measured loop inductance includes the series inductance from the PCB traces formed by the internal trace-self-inductance and external trace-self-inductance, and the negative mutual-partial inductance from the loop which is inversely proportional to the distance between loop segments [43]. As the loop area is shrunk, the negative mutual-partial inductance is maximized and thus effectively cancels or counteracts the external trace-self-inductance that will link/couple with the power switching loop nearby. From Fig. 12, the improved layout has only 17.2 nH loop inductance, reducing 2/3 of that in the original layout.

4) Discussion of Other Noises and Mitigation

Since the magnetic strength is inversely proportional to



(a)



(b)

Fig. 12. Selective FEA results of current sensor layouts on main power board. (a) Large loop in the first version design. (b) Small vertical loops with radial power distribution in the improved design.

the distance, another conservative but effective approach is to move hall sensors far away from the power loop, which is also experimentally verified but at the cost of larger board space.

Apart from d*i*/d*t* inductive coupling noise, other noises also exist for hall sensors. For example, d*v*/d*t* capacitive coupling from high voltage side to signal side of the hall sensor IC could also superpose significant noise onto the low-level sensor output via the isolation capacitance [41], [42]. Recommendations are: 1) placing hall sensors at non-d*v*/d*t* nodes, such as after filter inductors which absorb voltage d*v*/d*t* in the first place [16]; 2) choosing hall sensor chips with internal capacitive shielding can also avoid this type of distortion [42], and is applied in this design; 3) adding proper filter for this HF noise is also suggested [41]. However, that alone may be ineffective, since a dc offset can still be produced if d*v*/d*t* patterns at turn-on and off are not symmetric, following the mechanism disclosed in Section III-A.

C. DC Bias due to RFI Rectification in In-amp and Mitigation

Aside from op-amp, instrumentation amplifier (in-amp) is typically used for high voltage sensing where strong CM signals can be eliminated by the differential structure. However, the typical common mode rejection ratio (CMRR) of in-amps rolls off at 200 Hz, only remaining 20~30 dB at 100 kHz, and the in-amp has only up to 20 kHz bandwidth [35]. If a strong RFI noise is coupled at the input and is not

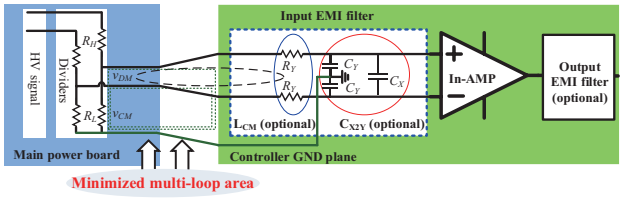


Fig. 13. Combined RFI noise suppression approach through PCB layout and EMI filter for in-amp based sensing circuit.

effectively suppressed, the dc rectification effect happens as well [34], similar to the RFI issue in the above op-amp case. Choosing an in-amp with higher EMI robustness is always the first design choice, however, decent immunity at low voltage signal level can barely cover the high noise strength in power conversion systems.

More practical mitigation in power electronics applications should be again to reduce the noise from its source. The first typical solution is inserting external EMI filter pairs at inputs of the in-amp, with both CM and DM filters implemented by RC filters, chokes, or X2Y capacitors, as shown in Fig. 13.

To be noted, the divider impedance network should also be considered for the input EMI filter design, otherwise improper filter characteristics may affect the control bandwidth of the voltage regulator due to the enlarged phase delay of the filter. Based on the Thevenin theory, the equivalent source impedance from the sensing voltage side is $R_H//R_L$, thus corner frequencies for CM and DM filters are respectively

$$f_{CM} = \frac{1}{2\pi (R_H // R_L + R_Y) C_Y} \tag{6}$$

$$f_{DM} = \frac{1}{2\pi (R_H // R_L + R_Y)(2C_X + C_Y)} \tag{7}$$

Clearly, neglecting the divider impedance $R_H//R_L$ in the filter will lead to selection of higher R_Y and cause underestimated phase delay and much slower voltage controller dynamics than one would expect. Similarly, failure to model it in the control transfer function should also be prohibited. In the case of RC filter, since $R_H//R_L$ is often above tens of kΩ, R_Y and C_X could be removed to simplify the conditioning circuit. If LC filters are used, a second-order RLC circuit analysis would be needed to properly determine the cut-off frequency and damping factors.

Another solution is to minimize the signal coupling loop. Different from the single-ended signal, the differential sensing circuit shown above contains two types of signal trace loops between the sensing divider and the in-amp: the differential-mode signal loop and the common-mode signal-GND loop. When it comes to PCB trace layout for the differential signal, the CM ground loop is often overlooked. In fact, it is as important as the DM loop. Since the high d*i*/d*t* can induce significantly high CM and DM noise voltage on the control interface circuit, the CM noise voltage will also be imposed on the in-amp pins. High stress of such CM noise not only causes clamped 0-volt output of the in-amp (since

its allowable input CM voltage is limited within its power supply voltage and decreases as its DM voltage increases), but also introduces heavier RFI effect as the RFI rectification involves CM and DM noises simultaneously [36], [37]. Reducing both noises and minimizing both types of trace loops is a must. This requires delicate layout on the power board to minimize not only the gap between the differential signal pairs as short as possible but also the gap between signal pairs and the signal ground, where the ground wire can be vertically placed through the multi-layer PCB design. The signal connection from the power board to the control interface board should also be short and compact until the three signal traces safely land onto the controller ground plane. On the interface board, the differential pair should continue to follow the best practice as mentioned to reduce the possible coupling noise.

IV. Experimental Verification

The above sensing issues have been observed and mitigated in the charger design, whose prototype information can be found in [18], [19]. Through this paper, two major mechanisms have been revealed in power electronic field applications. The mitigation performance is now examined in this section.

A. CM dv/dt Impact and Mitigation

Because of the high CM d*v*/d*t* of GaN devices, especially the hard-switching action of the front-end PFC, the LLC dc output voltage sensing signal has suffered from the dc bias noise, as already shown in Fig. 3 and Fig. 4, when the voltage sensing is through a widely adopted voltage sensing iso-amp ACPL-C87 which has been successfully applied in many commercial Si device based converter products for many years. Owing to the significantly high d*v*/d*t* in GaN based converter, the CM d*v*/d*t* noise immunity becomes a new issue as studied in this paper. To reduce the noise, a current sensing iso-amp Si8920B is configured to sample the LLC output voltage, to replace the prior voltage sensing iso-amp ACPL-C87. Thanks to the high CMTI up to 75 kV/µs of Si8920B and its high speed (rise/fall time is 0.42 µs), the dc bias on the desired dc sensing signal is effectively suppressed over the whole operation range of the two-stage charger. In addition, RFI rectification dc bias from its downstream in-amp and op-amp is also eliminated after minimizing all sensing circuit ground loops and the output differential pair loop as well as adding RC based EMI filters. The final voltage sampling result is accurately controlled at the given refenence value 27 V with 650 V dc-link bus voltage, as shown in Fig. 14. Compared to the prior result in Fig. 4, significant improvement on dc bias mitigation has been achieved.

B. RFI Impact and Mitigation

To illustrate this d*i*/d*t* effect and improvement through the new layout approach, sensing waveforms tested under 300 V_{dc} and 450 kHz switching frequency without any control compensation are compared.

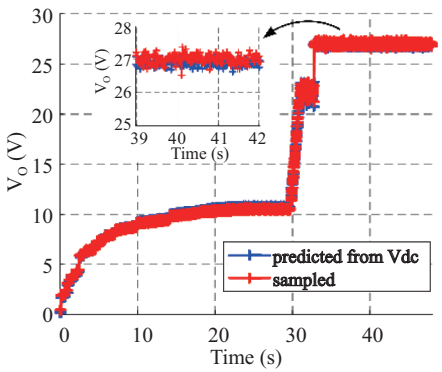


Fig. 14. Eliminated dc sensing shift and accurate dc regulation with the proposed sensing solution.

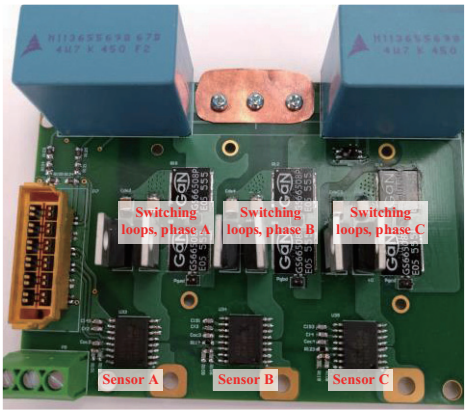
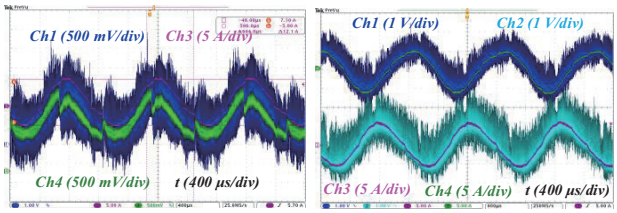


Fig. 15. Photo of ac/dc PFC prototype with revised input current sensor layout (top-overlaid gate driver board is removed).



(a) (b)

Fig. 16. Current sensing waveforms. (a) Current sensing distortion based on the old layout. Ch1: sampled signal via DAC output; Ch3: current probe output; Ch4: conditioning output signal. (b) No sensing distortion based on the improved layout. Ch1 and Ch2: outputs of hall sensors, Ch3 and Ch4: outputs of current probes.

Fig. 15 provides the prototype of the ac-dc PFC stage with the improved layout for the current sensing circuit, highlighting the power switching loops and the hall sensors. Fig. 16(a) gives the output of the conditioning circuit in green, sampling result from DSP in blue, and current probe result in magenta, with the first version layout. Disruptive distortion on the output of current sensor was observed, compared to the result of current probe. After adopting the new layout, all sensor outputs became clean, matching the actual shape of current waveforms obtained from current probes, as given in Fig. 16(b). This lays a solid basis for

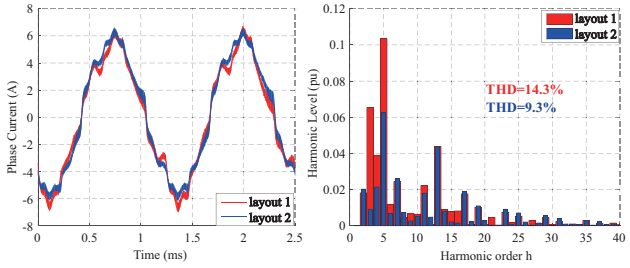


Fig. 17. Reduced current THD with proposed current sensor layout 2 avoiding high d*i*/d*t* noise coupled from power switching loops.

current quality control.

The impact of current sensor distortion on current harmonic distribution is also provided in Fig. 17. Compared to the case with distorted current sensors, tested at 115 V_{rms} input, 600 V_{dc} output, and 450 kHz, the proposed layout improves sensing signal quality and thus reduces phase current THD from 14.3 to 9.3 percentage points, before involving any further compensation [18] or sampling scheme [30], [31].

V. Conclusion

In this paper, different sensing distortions observed when adopting GaN devices in high frequency application are reported and their mechanisms investigated. The corresponding mitigation methods from noise source, propagation path, and noise receptor are studied and experimentally verified. Three types of sensing distortions are found strongly impacted by d*i*/d*t*, d*v*/d*t* and switching frequency, all related to undesired high frequency behaviors of different amplifiers. Mitigation solutions are proven effective in improving the sensing quality and minimizing the influences on feedback control and finally help reduce the ac input current THD by 5 percentage points and eliminate the dc output voltage drift from 6-volts to almost 0-volt in a 28 V_{max} battery charger. It is expected that the discussed noise issues, associated mechanisms, and noise mitigation solutions can be applied to other WBG converters and the results can facilitate converter control design.

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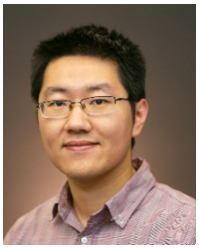

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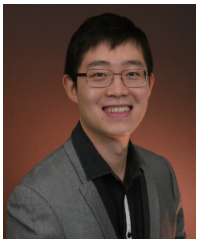

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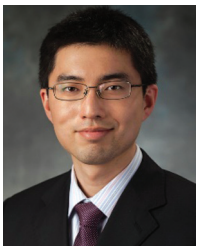

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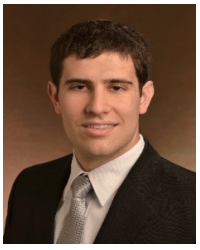

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Amplitude Adaptive Notch Filter With Optimized PI Gains for Mitigation of Voltage Based Power Quality Problems

Sabha Raj Arya, Rakesh Maurya, and Talada Appala Naidu

***Abstract*—In this paper, a three wire DVR has been implemented using control algorithm based on amplitude adaptive notch filter for mitigation of voltage based power quality problems. The compensation of voltage sag, voltage swell, distortions, and imbalance imposed in the supply voltage due to various reasons is carried out using this series connected devices. The amplitude adaptive notch filter (AANF) offers advantages in extracting components like frequency, angle, and sequence components with very simple and fast responding synchronization scheme. It does not require any phase locked loop (PLL) for estimating phase angle or frequency of input signals. The fundamental positive sequence components (FPSCs) embedded in the measured signals is separated using the control algorithm and then utilized in estimation of three phase reference load voltage. The optimization approach for tuning the PI controller's gains is proposed in the developed control algorithm. That is nature inspired whale optimization algorithm (WOA) has been used due to its competitiveness compared to conventional optimization algorithm. The WOA provides the appropriate values of proportional integration (PI) controller's gains within less time as compared to manual tuning of PI controller. The simulation and test performance are discussed to validate the proposed control algorithm in non-ideal AC mains.**

***Index terms*—DVR, fundamental positive sequence components (FPSC), harmonics, imbalance, optimization, sag and swell.**

I. Introduction

DUE to the widespread usage of power electronic devices in the power system, the importance of power quality has increased rapidly [1]. The reliability of the power system at the particular load center depends upon the interconnection of a large number of sources. The idea of custom power devices (CPDs) has been introduced in the distribution system to mitigate power quality issues [2]. Power quality issues related to voltage variations creating appreciable effects on both the generation and different types of loads. A Dynamic Voltage Restorer has been introduced in the distribution system to overcome these voltage related power quality issues [3]. The standard levels for the voltage harmonics need to be maintained have been reported in IEEE Std. [4].

DVR is the series injecting voltage source converter (VSC) based CPD which has been used for compensating the voltage related power quality issues. Mahdianpoor *et al.* in [5] have proposed a multifunctional DVR with a closed-loop controller with Posicast and Proportional plus resonant controllers to improve the transient response of the controller. Authors in [6], have proposed a least error squared based control algorithm for DVR and the DVR with this control is effectively compensating all the sequence components of load voltage with zero steady-state error. Sanchez *et al*. in [7] designed a repetitive control based closed-loop for a 2-level DVR for compensating power quality issues like voltage sags, harmonics, and imbalances in the voltage. Wessels *et al*. in [8] has investigated the application of a DVR connected to a wind turbine DFIG to allow non-interruptible fault ride through of grid voltage faults. A new hybrid DVR system topology is developed experimentally, in which a method of interfacing superconducting magnetic energy storage and BESS has been investigated to support a three-phase load [9].

Nielsen *et al.* in [10] have been tested at medium voltage level DVR with software-based PLL for creating reference load voltage for controlling DVR. Zhan *et al.* in [11], have considered the design issues of three-phase DVR and SPLL under voltage unbalance, voltage harmonics, frequency change, and phase jumps. Enhancement in the PLLs from the standard PLL with advantages like estimation of useful signals those help in the control of power engineering application [12]. Eren *et al.* in [13] have proposed the combination of conventional SRF-PLL and ANF for error due to harmonics and unbalances in the signal. PLLs used for extraction of information embedded in the distorted signals like amplitude, frequency/phase angle, fundamental components have been suffering in the accuracy and computational complexity due to number of pre-filter based control algorithms. Due to these reasons, a new approach of amplitude adaptive filters have been presented to estimate unknown parameters embedded in any disturbed sinusoidal signals without using any PLLs in literature [14]–[17].

Authors in text [14], have introduced two algorithms, direct and indirect adaptive algorithms for estimating the unknown frequency from the distorted sinusoidal signal. Yazdani *et al.* in [15], have been introduced a new 3-phase amplitude adaptive notch filter for online extraction of the fundamental magnitude

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and frequency/phase angle of any given disturbed waveform. This method of synchronization does not require any phase locked loops. Authors in [16], have discussed both the grid connected and the stand alone mode of micro grids with AANF as a tool for grid signal processing and distributed system synchronization. Shitole *et al.* [17], has been developed a three phase AANF based modified current control loop for real time estimation of supply voltage frequency and phase angle to generate the reference current for synchronization of interfacing inverter. It has been observed that AANF has several advantages with respect to control algorithm for DVR such as estimation of magnitude, frequency or phase, fundamental and its quadrature components, and sequential components of a given distorted signal. In this algorithm, PLLs and any transformations like Clark's or Park's are not required. Thus need less computational burden during real time processing. Even though, there are available methods of automatic PI controller tuning, it has been more practice of tuning a PI controller manually (i.e. trial and error) because of the ineffective solution with automatic tuning methods [18]. However, the manual tuning method consumes considerable time and tends to decrease the speed control algorithm implementation. Approach of the optimization techniques has been introduced in the PI controllers design for fast and accurate PI gains estimation [19]. The error of actual and reference signals are modeled as one of the performance indices for defining the cost function. The idea of optimization technique has been adopted in the PI gains estimation for DVR control in [20]. A whale optimization algorithm (WOA) is a Meta heuristic optimization algorithm which uses the natural behavior of the humpback whales [21], [22]. WOA has been used in finding the best feature set with performance comparison with particle swarm optimization and genetic algorithm [21]. An extensive study on WOA has been conducted by applying it in mathematical benchmark functions to analyze its potential for convergence and all other features of the optimization algorithm [22].

In this paper, three-phase AANF based control algorithm has been proposed for estimation of reference load voltage. The optimization technique for PI gains estimation in DVR for compensation of major issues like voltage sag, voltage swell, imbalances, and distortions in the supply voltage has been proposed. Proposed control algorithm has an advantage of online extraction of frequency/phase of disturbed signals. It also produces the fundamental component and its 90° phase shifted component, which helps in computing the sequence components of the given signal. It uses three phase AANF based frequency extraction unit for online frequency extraction. This estimated frequency is further utilized in ANF structures in each phase for separating the fundamental component and its quadrature component of three phases. The sequence components extraction unit is used for the positive sequence components useful for the load voltage reference generation. A Whale Optimization Algorithm (WOA), the optimization approach for tuning the proportional integration (PI) controller's gains is proposed in this control algorithm because of its competitiveness compared to conventional one. The process of PI gains estimation is clearly shown with the help of figures showing the variation with respect to iteration. These estimated gains have been used in the proposed control algorithm for the fast and satisfactory operation of DVR.

II. System Configuration

The detailed system configuration has been presented in Fig. 1, which has mainly two parts namely power and control circuit respectively. The power circuit consists of three-phase ac supply with disturbance creating unit, sensitive/critical load, injection transformer, filter network, bi-directional converter and capacitor. Disturbances in the supply voltage (v_{sabc}) have been created by the disturbance-creating unit as shown in Fig. 1. The disturbance-creating unit consists of different types of loads connected at the same point of common coupling (PCC) with the switches (sw_1 to sw_4) with different times (t_1, t_2… t_4) of switching periods. Switching ON the inductive and capacitive loads at t_1 and t_2 respectively creates sag and swell in the supply voltage. In the same way, switching ON the three-phase unbalanced load and rectifier with RL-load at t_3 and t_4 respectively creates disturbance and unbalances in supply voltage. Resistive-Inductive (RL) load is considered as a sensitive/critical load for which the load voltage (v_{Labc}) at its terminals is to be maintained at the nominal value. Injection transformer (TF_{inj}) with the selected transformation ration (n: 1) has been used for series connection of compensation unit in series with supply and load. Filtering unit is to filterout the generated switching harmonics from the Voltage Source Converter (VSC). VSC used here is the bi-directional converter and provides bidirectional flow of energy.

The energy storage device here is capacitor (C_{DC}) with voltage (V_{DC}) has been maintained at its reference voltage which is measured for the progressive compensation of disturbances created in the supply voltage. The functioning of the power circuit depends on the working of the control circuit that is elaborated in the following subsection.

The control circuit consists of 3-phase AANF based frequency extraction unit, three single units of ANF structures, 3-phase sequence component extraction unit, reference load voltage generation, and gate pulse generator. The gate pulses generated in the control circuit have been used to drive the VSC in the power circuit part of the configuration for working as a bi-directional converter. The detailed explanation of the control algorithm with mathematical analysis and stability analysis has been reported in Section III.

III. AANF Based Control Algorithm

The effective operation of power circuit is completely dependent on performance of control circuit in generating gate pulses for VSC situated in power circuit. The proposed control algorithm is utilizing the AANF for estimating the phase/frequency of the measured signals. Further, the estimated phase/frequency has been taken into account while estimating the fundamental component (FCs) of the input signals. From these

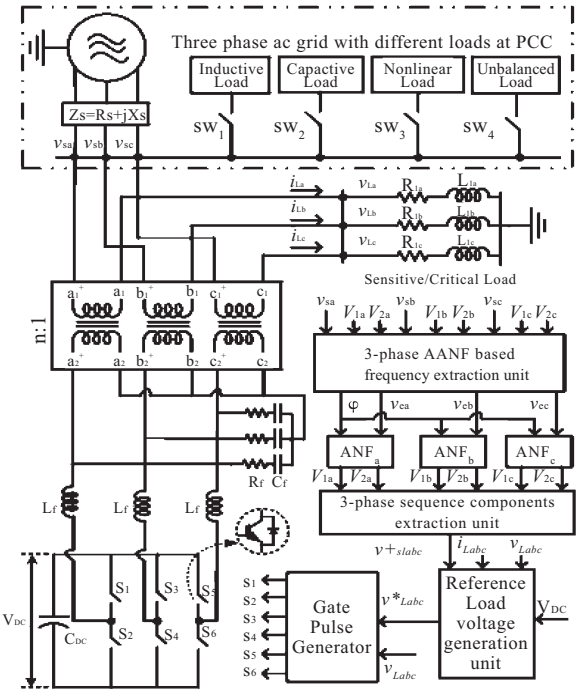


Fig. 1. DVR system with proposed control algorithm.

fundamental components, the positive sequence components (PSCs) have been computed and utilized for the reference load voltage (v^*_{Labc}) generation. The load voltage (v_{Labc}) has been sensed and it has been compared with the reference load voltage (v^*_{Labc}) for producing the PWM pulses to drive the VSC. The details of the control algorithm has been given in the following sub-sections.

A. Basics of Amplitude Adaptive Notch Filter

The adaptive property of AANF has been inspired from the Regalia's algorithms continuous time version. According to this algorithm, considering the estimation of frequency (ω) of a signal *y(t)* where 'θ' is the resulting estimated frequency, it has three states θ, x_1, and x_2, obey the following differential (1) to (3) [14].

$$\dot{x_1} = x_2 \tag{1}$$

$$\dot{x_2} = -2\zeta\theta x_2 - \theta^2 x_1 + ky \tag{2}$$

$$\dot{\theta} = -g\,(ky - 2\zeta\theta x_2)\,x_1 \tag{3}$$

Where, 'ζ', the damping factor, '*g*', the adaption gain, '*k*', the filter gain are the positive constants. The new AANF structure has been provided in [15],[16], which satisfies the (4) to (8). The error, *e(t)* is calculated using (6), 'ε' and 'φ' represent positive constant and frequency respectively. The positive parameters damping factor (ζ), the adaption gain (λ) which represents the speed of convergence and accuracy of the AANF.

$$\ddot{x} + \varphi^2 x = 2\zeta\varphi e(t) \tag{4}$$

$$\dot{\varphi} = -\lambda x \varphi e(t) \tag{5}$$

$$e(t) = x(t) - \dot{x} \tag{6}$$

$$\lambda = \frac{\varepsilon}{(1+A^2)(1+\mu\varphi^2)} \tag{7}$$

$$(\mathrm{O}) = \begin{pmatrix} x \\ \dot{x} \\ \varphi \end{pmatrix} = \begin{pmatrix} \frac{-A_1}{w}\cos(wt+\psi_1) \\ A_1 \sin(wt+\psi_1) \\ w \end{pmatrix} \tag{8}$$

For the fundamental frequency '*w*', the sinusoidal signal, AANF attains a uniform periodic orbit 'O' defined as (8), where 'A_1', 'ψ_1' represent the fundamental component and phase angle respectively. From the (8), fundamental frequency '*w*' is given by 'φ' and it is clear that, $A_1 = \sqrt{\dot{x}^2 + (-\varphi x)^2}$ where $\dot{x} = A_1 \sin(wt+\psi_1)$ and $-\varphi x = A_1 \cos(wt+\psi_1)$ are the fundamental component and its quadrature component respectively.

B. 3-Phase AANF for Extraction of Fundamental Voltage

From the inspiration of the concept of single phase AANF, the 3-phase AANF is formulated for compensation of voltage based power quality problems. The detailed structure of the 3-phase AANF is given in Fig. 2. Let the 3-phase input signal that is to be synchronized is defined as (9) where 'V_N', 'w_n', and 'φ_n' are unknown amplitudes, frequency, and phase angle respectively.

$$v(\mathrm{t}) = \sum_{\substack{N=A,B,C \\ n = a,b,c}} V_N \sin(w_n t + \psi_n) \tag{9}$$

For approximating these unknown parameters of any 3-phase signal in (9), the 3-phase AANF is described as given in the differential (10) to (14) using the (4) to (8) [15],[16], where, n = a, b, c and N = A, B, C. Here, 'φ' represents the frequency and 'ε' is the positive constant. The positive parameters 'ζ', the damping factor, 'λ_n', the adaption gain represents the accuracy and convergence speed of the AANF. Parameter 'v_{en}' is the error voltage which is obtained by subtracting fundamental component (V_{1a}) of the input signal from the input signal (v_n).

$$\ddot{v}_n + \varphi^2 v_n = 2\zeta\varphi v_{en}(t) \tag{10}$$

$$\dot{\varphi} = -\lambda v_n \varphi v_{en}(t) \tag{11}$$

$$v_{en}(t) = v_n(t) - \dot{v}_n \tag{12}$$

$$\lambda_n = \frac{\varepsilon}{(1+V_N^2)(1+\mu\varphi^2)} \tag{13}$$

For the fundamental frequency 'w_1', 3-phase AANF is having the periodic orbit (O) as mentioned in (14), where 'V_N' is the fundamental amplitude of the respective input signal (N = A, B, and C) which is utilized to compute the adaption gain, 'λ_n'. The phase angles of each phase have been represented by 'ψ_n' (n = a, b, c). From the (14), the fundamental frequency of the input signal 'w_1' is identified as 'φ', the fundamental component and its quadrature component are given as $V_N \sin(w_1 t + \psi_n)$ and $V_N \cos(w_1 t + \psi_n)$. These two components have been separated using the separate ANF filters for each phase as shown in Fig. 1.

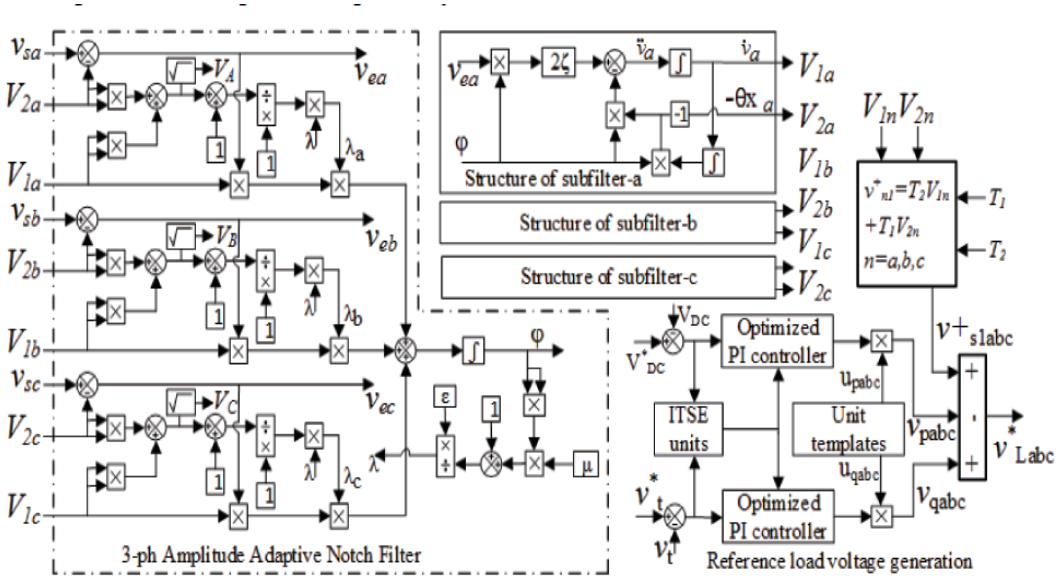


Fig. 2. Structure of AANF based control algorithm for DVR.

The details of ANF filters have been given in Fig. 2 which utilizes the error signal 'v_{en}' and the estimated frequency 'φ' as inputs and produces the fundamental component (V_{1n}), quadrature component (V_{2n}) as outputs given in (15) and (16).

$$(O)=\begin{pmatrix} v_n \\ \dot{v}_n \\ \varphi \end{pmatrix}=\begin{pmatrix} \frac{-V_N}{w_1}cos(w_1t+\psi_n) \\ V_N sin(w_1t+\psi_n) \\ w_1 \end{pmatrix} \tag{14}$$

$$\dot{v}_n = V_N sin(w_1t+\psi_n) = V_{1n} \tag{15}$$

$$-v_n\varphi = V_N cos(w_1t+\psi_n) = V_{2n} \tag{16}$$

Therefore, the amplitude 'V_N' of a particular phase is measured as $V_N=\sqrt{V_{1n}^2+V_{2n}^2}=\sqrt{\dot{v}_n^2+(-\varphi v_n)^2}$ and then utilized in the frequency estimating unit of the AANF structure and sequence component extraction unit.

C. Sequence Components Extraction and Reference Voltage Generation

The 3-phase voltages given in (9) have been separated into their sequence components. The fundamental and its 90° phase sifted component measured using (15) and (16) is then represented by column matrix as shown in (17). The positive Sequence components (PSCs) are computed from the Fundamental Components (FCs) and Transformation Matrices (T_1, T_2) using (18) [15].

$$V_{1n}=\begin{pmatrix} \dot{v}a \\ \dot{v}b \\ \dot{v}c \end{pmatrix} \text{ and } V_{2n}=\begin{pmatrix} -\varphi v_a \\ -\varphi v_b \\ -\varphi v_c \end{pmatrix} \tag{17}$$

$$v_{n1}^{+}=T_2V_{1n}+T_1V_{2n} \tag{18}$$

$$T_1=\frac{1}{2\sqrt{3}}\begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix};\ T_2=\frac{1}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ -1/2 & 1 & -1/2 \\ -1/2 & -1/2 & 1 \end{bmatrix} \tag{19}$$

Finally, the FPSCs of the input voltage extracted are represented as (v_{s1abc}^{+}) and further utilized in generating the reference load voltages (v_{Labc}^{*}).

Now, the reference load voltage (v_{Labc}^{*}) generation has been done by using the FPSCs and Unit templates (u_{pabc} and u_{qabc}) and output signals of DC bus PI controller (V_{DCPI}) and AC bus PI controller (V_{tPI}) respectively.

$$v_{\text{Labc}}^{*}=v_{\text{slabc}}^{+}-v_{pabc}+v_{qabc} \tag{20}$$

$$v_{pabc}=V_{DCPI}\times u_{pabc} \tag{21}$$

$$v_{qabc}=V_{tPI}\times u_{qabc} \tag{22}$$

Where 'u_{pabc}' and 'u_{qabc}' are calculated using the load currents (i_{Labc}) sensed as shown in (23) and (24) [3].

$$u_{pa}=\frac{i_{la}}{i_A};\ u_{pb}=\frac{i_{lb}}{i_A};\ u_{pc}=\frac{i_{lc}}{i_A} \tag{23}$$

$$u_{qa}=\frac{u_{pc}-u_{pb}}{\sqrt{3}};\ u_{qb}=\frac{3u_{pa}+u_{pb}-u_{pc}}{2\sqrt{3}};\ u_{qc}=\frac{-3u_{pa}+u_{pb}-u_{pc}}{2\sqrt{3}} \tag{24}$$

Where $i_A=\sqrt{2/3(i_{la}^2+i_{lb}^2+i_{lc}^2)}$

The sensed load voltage (v_{Labc}) is then compared with the reference load voltage (v_{Labc}^{*}) of each phase to get the load error voltage (v_{Leabc}) for each phase respectively. These error signals have been passed through the high frequency triangular signal for comparison and gate pulses (s_1, s_2), (s_3, s_4), and (s_5, s_6) have been generated for each arm of the VSC respectively.

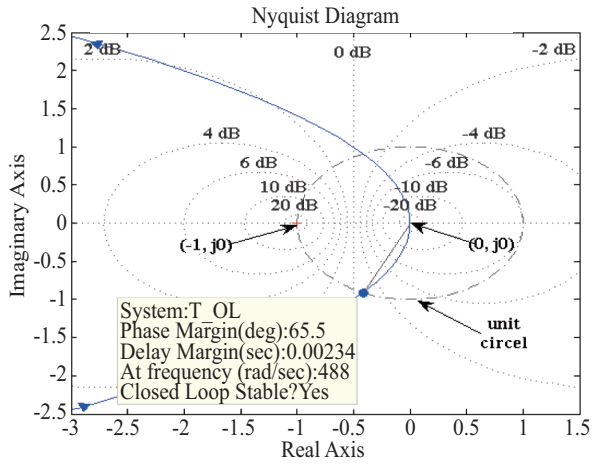


Fig. 3. Nyquist plot for open loop Transfer Function (30).

D. Stability Analysis of Filter

From the (15), it is clear that '$\dot{v}_n$' is the fundamental component of the input signal 'v_s' and it is represented by 'v_f'. Therefore,

$$\dot{v}_n = v_f \tag{25}$$

The Laplace Transform of the (10), (12) and (25) are obtained as (26), (27) and (28) respectively.

$$s^2 V_n(s) + \varphi^2 V_n(s) = 2\zeta\varphi V_e(s) \tag{26}$$

$$V_e(s) = V_s(s) - sV_n(s) \tag{27}$$

$$sV_n(s) = V_f(s) \tag{28}$$

Substituting (28) in (26) and (27) and simplified to obtain the closed-loop transfer function of fundamental signal '$V_f(s)$' to input signal '$V_s(s)$' as in the (29).

$$\frac{V_f(s)}{V_s(s)} = \frac{2\zeta\varphi s}{s^2+2\zeta\varphi s+\varphi^2} = T_{CL} \tag{29}$$

Where $T_{CL} = \dfrac{G(s)}{1+G(s)H(s)}$, $T_{OL} = G(s)H(s)$

$$G(s)H(s) = \frac{2\zeta\varphi s+\varphi^2}{s^2} = \frac{\varphi^2(1+\frac{2\zeta}{\varphi}s)}{s^2} = \frac{k(1+Ts)}{s^2} \tag{30}$$

Hence, the open loop transfer function is derived from the closed loop transfer function as in the (30), Where $k = \varphi^2$ and $T = 2\zeta/\varphi$. The selection of the parameters 'k' and 'T' are based on the selection of 'ζ' and 'φ'. The damping factor, 'ζ' is associated with the damping property of the filter, so it is selected as 0.707 to avoid the dampings in the response. For selected value values of 'ζ' and 'φ', the parameters in the open loop transfer function 'k' and 'T' are found. The stabilty of the filter is examined using the Nyquist stability criteria as shown in Fig. 3. The stability analysis of the filter is observed for the response of the fundamental component '$V_f(s)$' to input signal '$V_s(s)$'. For the selected parameters of the open loop transfer function 'k' and 'T', closed-loop stability can be observed by Nyquist stability analysis from the open loop transfer function (T_{OL}) as given in (30). The AANF parameters, 'ε' and 'μ' are set to 10 000 and 0.000 01 for a satisfactory response, the adaption gain 'λ' is computed accordingly.

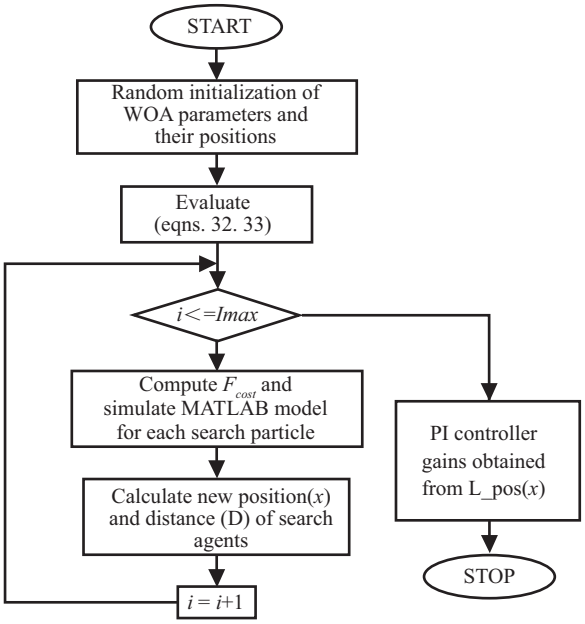


Fig. 4. PI controller gains estimation flow chart using WOA.

E. Estimation of PI Gains Using WOA

A Whale Optimization Algorithm (WOA), the optimization approach for tuning the PI controller's gains is proposed in this control algorithm. PI gains tuning is another task in the control algorithm for most of the power electronics application. Even though, methods of automatic PI controller tuning are available, it has been more practice of tuning PI controller manually (i.e. trial and error) due to occurrence of ineffective solution with automatic tuning methods. The error, *e(t)* of actual and reference signals can be modeled as any one of the performance indices for defining the cost function (f_{cost}). Here, the performance index, Integral of Time Squared Error (ITSE) is considered for cost function. It is expressed as,

$$f_{cost} = \int te^2(t)dt \tag{31}$$

The WOA starts optimization with a randomly selected an initial positions for each and every search agents. For the satisfactory solution, after many tests, the lower (l) and upper (u) bounds are set to '0' and '30'. Number of agents (n), the maximum number of iteration (I_{max}) have been set to 20 and 10. The dimension (d) of the search agent has been set to '4' i.e. Gains of two PI controllers are named as (k_{p1}, k_{i1}) and (k_{p2}, k_{i2}) respectively. Fig. 4. shows the flow chart of WOA for tuning the PI controllers' gains, where 'i' represents the present iteration.

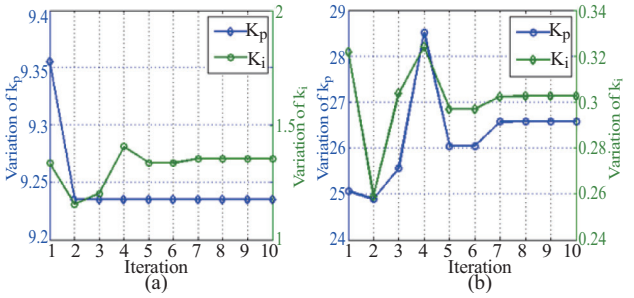


Fig. 5. Variation of PI gains with respect to iterations (a) DC-Link PI and (b) terminal voltage PI.

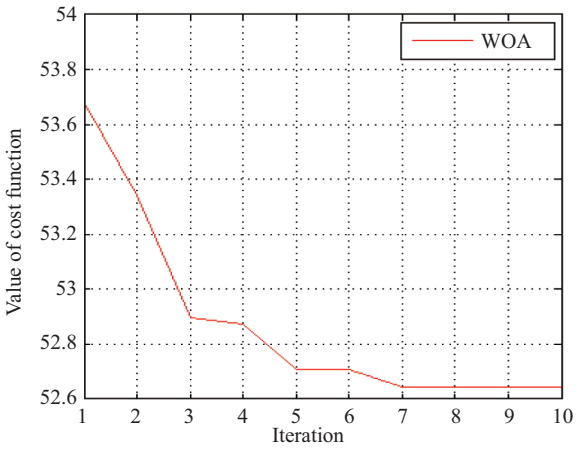


Fig. 6. Convergence curve of cost function with respect to iterations.

Optimal values of PI-controller gains are obtained from the leader position (x). The mathematical description of WOA is as follows.

The position vector (x) and distance (D) of each search agent (leader whale) are updated using (32) and (33). Where, 'p' is the random number in the range (0, 1), b=1, 'l' are constants and "L_pos" represents the position of leader (leading) whale. A, C are the coefficient of vectors measured using (34).

$$\left.\begin{array}{l} D = abs(C \times x\_rand_d - x_{i,d}) \\ x_{i,d} = x\_rand_d - A \times D \end{array}\right\} ...if...abs(A) \geq 1$$
$$\left.\begin{array}{l} D = abs(C \times L\_pos_d - x_{i,d}) \\ x_{i,d} = L\_pos_d - A \times D \end{array}\right\} ...if...abs(A) < 1 \Bigg\} ...if...p < 0.5 \quad (32)$$

$$\left.\begin{array}{l} D = abs(L\_pos_d - x_{i,d}) \\ x_{i,d} = D \times e^{b \times l} \times cos(2\pi l) + L\_pos_d \end{array}\right\} ...if...p \geq 0.5 \quad (33)$$

$$A = (2 \times rand() - 1) \times a_1 ; C = 2 \times rand() \quad (34)$$

Where, $a_1 = \left(1 - \frac{i}{I_{max}}\right) \times 2; a_2 = -\left(1 + \frac{i}{I_{max}}\right);$

$$l = (a_2 - 1) \times rand() + 1; \text{and } p = rand()$$

The variation in the position of variables (k_{p1}, k_{i1}, k_{p2}, and k_{i2}) with respect to iteration can be seen in Fig. 5(a) and (b). During this iterative process, the convergence curve has been depicted in Fig. 6. It is observed that the cost function is stabled at 7th iteration and continuing with the same cost function value i.e. 52.65. From the Fig. 5(a) and (b), at least by 7th iteration the variable (k_{p1}, k_{i1}, k_{p2}, and k_{i2}) are settled to their optimized values 9.23, 1.375, 26.52, and 0.31 respectively. These optimized values of PI controller gains are to be used in the proposed control algorithm for the acceptable performance in the three-phase DVR connected system.

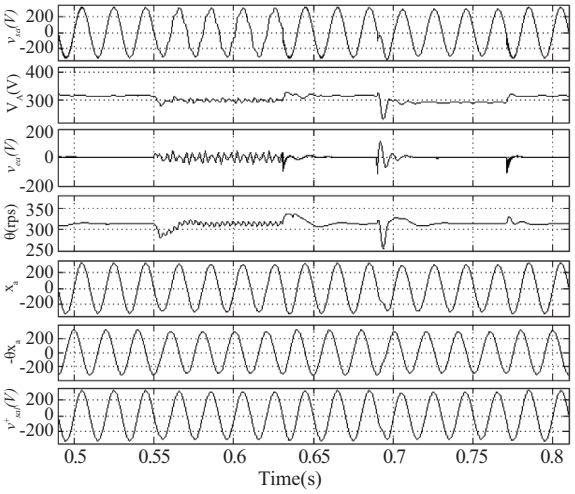


Fig. 7. Internal signals of AANF for extracting FPSCs.

IV. Simulation Results Discussion

The developed AANF based control algorithm is tested with three-phase DVR connected system in compensating the voltage sag/swell, distortions, and unbalance for evaluation. This complete system with AANF based control algorithm is simulated using MATLAB software-based simulator. The solver used in this simulation with a sampling time of 20 µS. It is to be noted that simulation results and performance of AANF based control algorithm have been considered for distortions and unbalance. The performance investigation of DVR with AANF based control algorithm has been carried out under various conditions such as voltage sag/swell, distortions, and unbalance. The system parameters for the simulation work have been given in Appendix A.

A. Performance of AANF Based Control Algorithm

The simulation performance of AANF based control algorithm in extracting the FPSCs and generating the reference load voltage (v^*_{Labc}) with distorted and unbalanced supply voltage (v_{sabc}) is presented in this section. Fig. 7 shows the extraction of FPSCs from the distorted and unbalanced supply voltage of phase 'a' (v_{sa}).The amplitude of phase 'a', V_A, error, v_{ea} of phase 'a', and the estimated frequency, θ are the internal signals of frequency extraction unit of control algorithm shown in this figure. The fundamental component, '$\dot{x}_a$' and its 90° phase shifted component, '$-\theta x_a$' which have been computed from the single-phase structure of AANF presented in this figure. From Fig. 7, it is observed that the variation of frequency during the dynamics can be seen cleary in subplot (4) of Fig. 7 at 0.55 sec and 0.69 sec for distorted and unbalanced

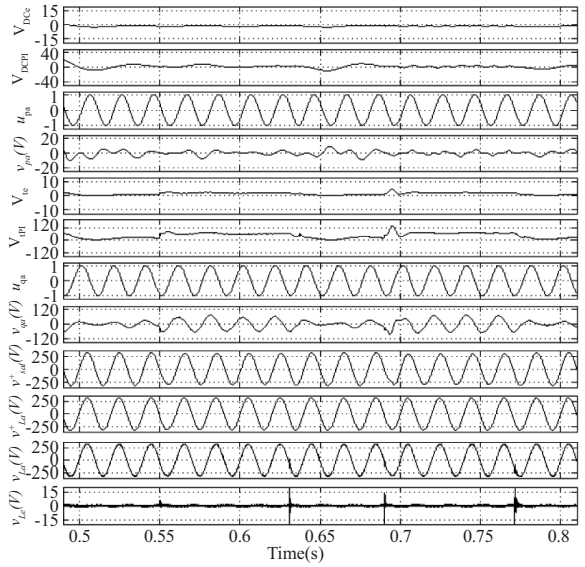


Fig. 8. Internal signals of a proposed control algorithm for generating reference load voltage.

supply. The fundamental and its quadrature components have been used for the Sequence Components (SCs) computation. Computed Fundamental Positive Sequence Component (FPSC) of the supply voltage (v^{+}_{s1a}) has been depicted in subplot (8) of Fig. 7. Fig. 8 shows the internal signals control algorithms in generating the reference load voltage with supply voltage distortions and unbalance. Inputs to the controllers (V_{DCe} and V_{te}), outputs of controller (V_{DCPI}, V_{tPI}), unit templates (u_{pa}, u_{qa}), and signals obtained by multiplying unit templates with PI controller outputs, (v_{pa}, v_{qa}) have been presented in this graph. The FPSC of supply voltage (v^{+}_{s1a}), reference load voltage (v^{*}_{La}) computed by (20), and actual load voltage of phase 'a' (v_{La}) to compare with (v^{*}_{La}) are reported here in Fig. 8. The error load voltage signal (v_{le}) is further passed through high-frequency carrier signal to generate PWM gate pulse signals (s_1, s_2.....s_6) for IGBTs used in the VSC of the power circuit of DVR connected system.

B. Performance of DVR Using AANF Based Control Algorithm

As mentioned in the Section-II, voltage sag, voltage swell, distortions in voltage waveform, and imbalance in the supply voltage have been created by joining the different types of loads at same PCC each for the duration of 4 cycles at 0.25 sec, 0.39 sec, 0.55 sec, and 0.69 sec respectively. Fig. 9(a) represents the overall performance of the DVR system with proposed control algorithm in presence of sag, swell, distortions, and imbalance in the supply voltage. Three-phase supply voltage (v_{sabc}) with all the dynamics, compensated voltages (v_{cabc}), and the load voltage (v_{Labc}) at the load terminal after compensation have been depicted in the subplots (1-5) of Fig. 9(a). It has been observed that the load voltage is free from the disturbances appended to the supply voltage due to effective compensation by DVR. Three-phase load current (i_{Labc}), magnitude of load terminal

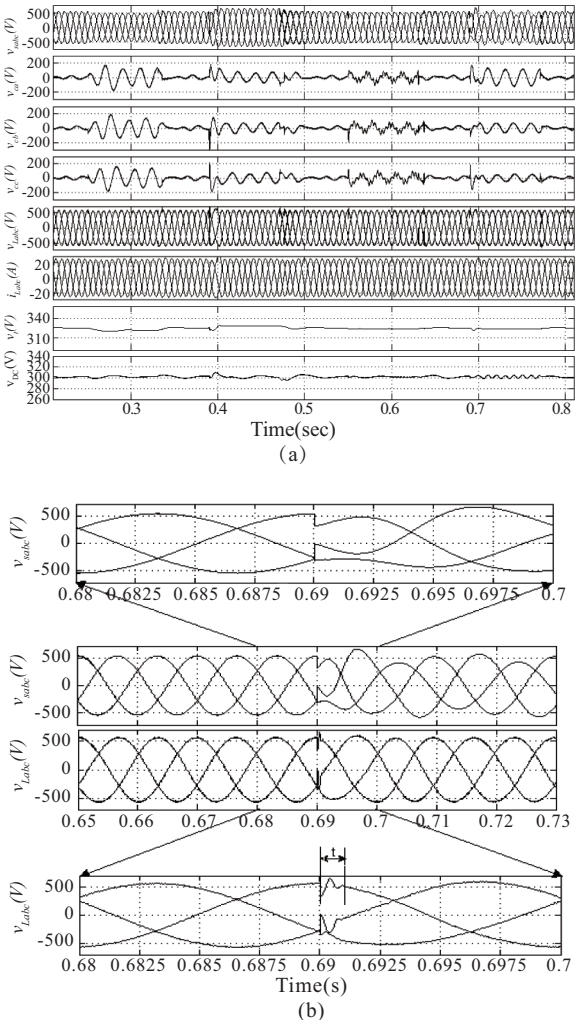


Fig. 9. (a) Performance of DVR in compensation of voltage sag, voltage swell, voltage distortions, and voltage imbalance using AANF based control algorithm. (b) Response time of DVR in compensation of voltage imbalance.

voltage (V_t), and DC-Link voltage (V_{DC}) has been shown in subplots (6-8). PI controllers are effectively maintaining the DC-Link voltage and terminal voltages at their reference levels. The DVR with the proposed AANF based control algorithm is producing the effective solution for the mentioned problems associated with a supply voltage in the distribution system. Fig. 9(b) shows the response time of DVR for compensating an imbalance in the supply voltage by using AANF control algorithm. It is to be noted that the Fig. 9(b) contains the supply voltage and its corresponding load voltage during the unbalances in the supply voltage. The subplot 1 in Fig. 9(b) represents the Zoom-in figure of subplot 2 and subplot 4 represents the Zoom in figure of subplot 3 of the same figure. From the Fig. 9(b), it is clear that the DVR with AANF based control algorithms is able to compensate the unbalances in the supply voltage within the quarter (1/4) cycle.

The steady state performance of the DVR has been described by considering the distortions in the supply voltage depicted in Fig. 10. Fig. 10(a)-(c) represents the distorted supply voltage (v_{sa}), compensated load voltage (v_{La}), and load current (i_{La})

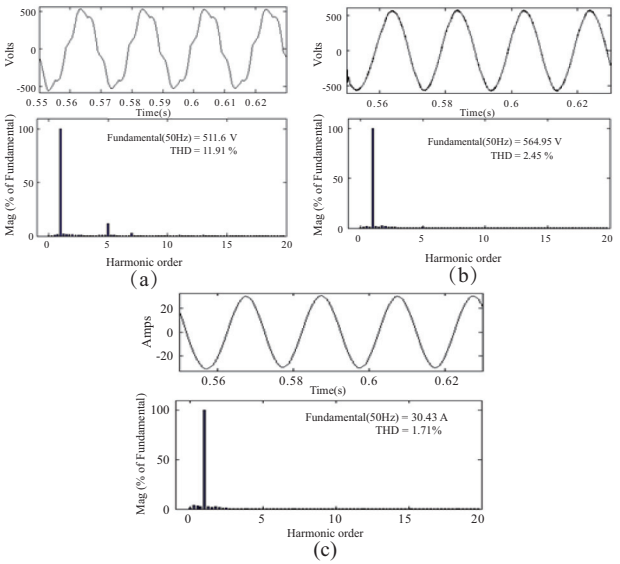


Fig.10. (a) Supply voltage of phase 'a' and its THD (b) Load voltage of phase 'a' and its THD and (c) Load current of phase 'a' and its THD.

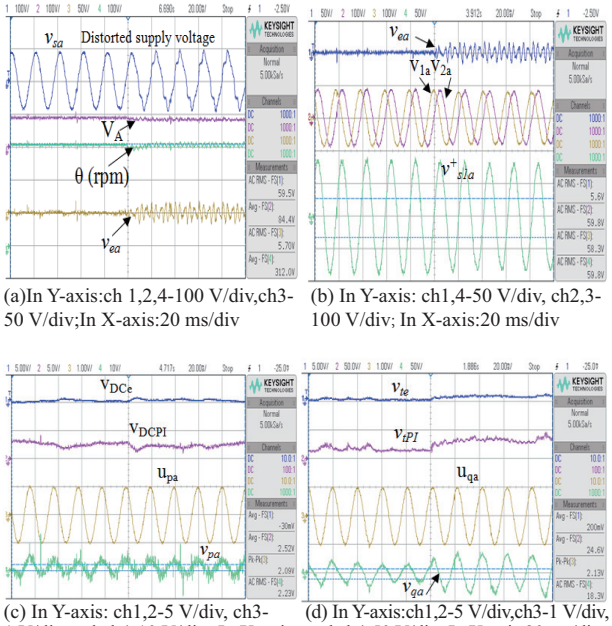
and their respective Total Harmonic Distortions (THDs). The distorted supply voltage shown in Fig. 10(a) contains the harmonics of THD 11.91% with a fundamental voltage of 511 V. After compensation by the DVR the load voltage is free from higher order harmonics with THD of 2.45% and fundamental voltage of 564.95 V as shown in Fig. 10(b). Similarly, the load voltage of THD 1.71% and fundamental current of 30.43 A are presented in Fig. 10(c). It is clearly understood that the levels of THDs obtained in the load voltage and load currents are under the standards of IEEE Std. 519-2014.

V. Test Results Discussion

A prototype DVR with proposed AANF based control algorithm has been built and programmed with field-programmable gate array (FPGA) based processor using OP-5142 real time simulator. The test results have been recorded using DSO-X-2004A, a 4-channel DSO and Fluke 43B, a power quality analyzer. For validation of proposed control algorithm, AANF in three-phase DVR, its internal signals have been observed at 45 µsec sampling time. The dynamic performance has been observed during sag, distortions, and imbalances in the supply voltage. The steady-state results have been recorded during distortions in the source voltage. Throughout the test, the switching frequency of VSC has been maintained at 5 kHz. It is to be noted that the values of internal signals of AANF control algorithm reported in Fig. 11(a)-(e) are in 'phase to ground', whereas the values of signals reported in Fig. 12(a)-(c) to Fig. 14(a)-(c) are in 'phase to phase'. The parameters for the test setup are given in the Appendix B.

A. Performance Evaluation of AANF Based Control Algorithm

The control algorithm proposed in this paper has been

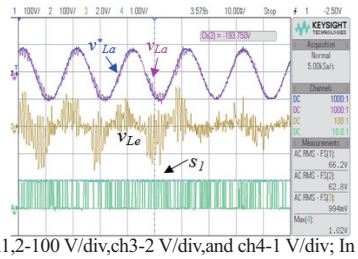


(a)In Y-axis:ch 1,2,4-100 V/div,ch3-50 V/div;In X-axis:20 ms/div

(b) In Y-axis: ch1,4-50 V/div, ch2,3-100 V/div; In X-axis:20 ms/div

(c) In Y-axis: ch1,2-5 V/div, ch3-1 V/div,and ch4-10 V/div; In X-axis: 20 ms/div

(d) In Y-axis:ch1,2-5 V/div,ch3-1 V/div, and ch4-50 V/div; In X-axis:20 ms/div

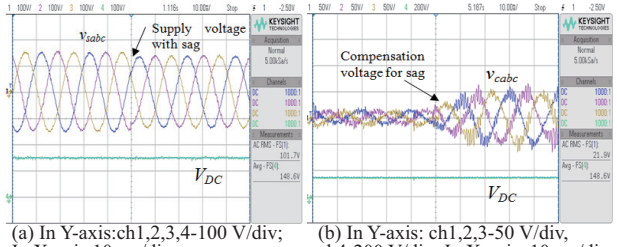


(e) In Y-axis: ch1,2-100 V/div,ch3-2 V/div,and ch4-1 V/div; In X-axis:10 ms/div

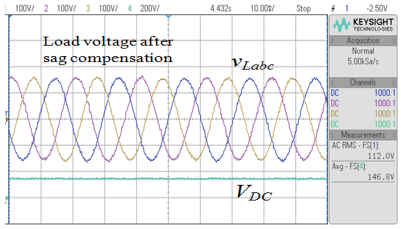
Fig. 11. Internal signals of control algorithm (a)v_{sa}, V_A, v_{ea}, θ, (b) v_{ea}, V_{1a}, V_{2a}, v^+_{sa}, (c) V_{DCe}, V_{DCPI}, u_{pa}, v_{pa}, (d) v_{te}, v_{tPI}, u_{qa},v_{qa} and (e)v^*_{La}, v_{La}, v_{Le}, s_1.

evaluated by observing its performance in extracting the FPSCs of the supply voltage (v^+_{s1abc}) from the distorted supply voltage (v_{sabc}) and generation of reference load voltages (v^*_{Labc}). The internal signals of control algorithm presented in Fig. 11(a)-(e) are of phase 'a' only and those of phase 'b' and 'c' are analogous.

The internal signals of AANF based frequency extraction unit with its input signal (v_{sa}), are amplitude, (V_A), error (v_{ea}), and estimated frequency (θ) have been given in Fig. 11(a). The frequency estimated here is approximately equal to 314 rpm, which corresponds to the nominal frequency of the system. Fig. 11(b) shows the outputs of single ANF unit, fundamental and its 90° phase shifted components ($V_{1a}$and V_{2a}), and its positive sequence component (v^+_{s1a}) along with error (v_{ea}) signal. Thus estimated FPSCs (v^+_{s1abc}) have been used in the generation of reference load voltage. Fig. 11(c), represents the inputs of DC-PI controller (V_{DCe}), output of DC-PI controller (V_{DCPI}), in-phase unit template (u_{pa}), and signal obtained by (21), (v_{pa}). Similarly, Fig. 11(d), represents the input of terminal voltage PI controller (V_{te}), output of terminal voltage PI controller (V_{tPI}), quadrature unit templates (u_{pa} and u_{qa}), and signal obtained by (22), (v_{qa}). These figures depict the acceptable performance

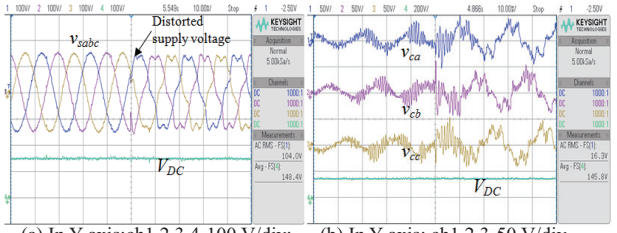


(a) In Y-axis:ch1,2,3,4-100 V/div; In X-axis:10 ms/div (b) In Y-axis: ch1,2,3-50 V/div, ch4-200 V/div; In X-axis: 10 ms/div

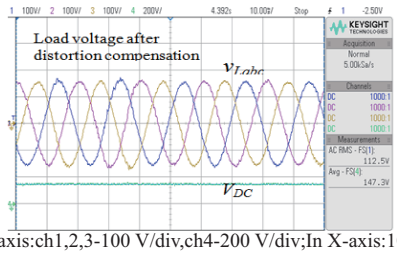


(c) In Y-axis:ch1,2,3-100 V/div,ch4-200 V/div; In X-axis:10 ms/div

Fig. 12. Test results showing sag compensation (a) supply voltage (v_{sabc}) with sag (b) compensated voltage (v_{cabc}) and (c) Load voltage after compensation (v_{Labc}).



(a) In Y-axis:ch1,2,3,4-100 V/div; In X-axis:10 ms/div (b) In Y-axis: ch1,2,3-50 V/div, ch4-200 V/div; In X-axis: 10 ms/div



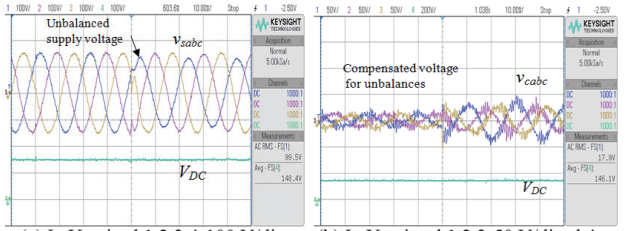
(c) In Y-axis:ch1,2,3-100 V/div,ch4-200 V/div;In X-axis:10 ms/div

Fig. 13. Test results showing distortions compensation (a) supply voltage (v_{sabc}) with distortions (b) compensated voltage (v_{cabc}) and (c) Load voltage after compensation (v_{Labc}).

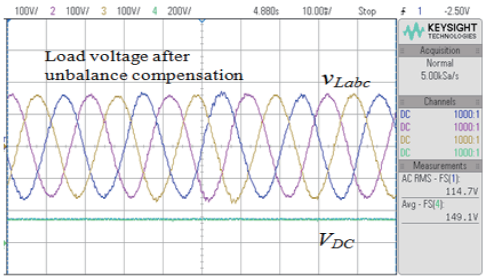
of PI controllers in maintaining values at their respective reference levels. Fig. 11(e), shows the comparison of reference load voltage, (v^*_{La}) and actual load voltage, (v_{La}) of phase 'a', their corresponding error (v_{Le}), and switching pulse (s_1). The generated PWM pulse (s_1, s_2…..s_6) have been given to IGBTs in VSC. This makes the DVR system with AANF based control algorithm to function satisfactorily.

B. Overall Test Performance Evaluation of Three Wire DVR

The performance analysis of DVR with the proposed control algorithm has been analyzed in both dynamic and steady states. Fig.12(a)-(c) to Fig.14(a)-(c)is interpreting the overall



(a) In Y-axis:ch1,2,3,4-100 V/div; In X-axis:10 ms/div (b) In Y-axis: ch1,2,3-50 V/div,ch4-200 V/div; In X-axis: 10 ms/div



(c) In Y-axis:ch1,2,3-100 V/div,ch4-200 V/div;In X-axis:10 ms/div

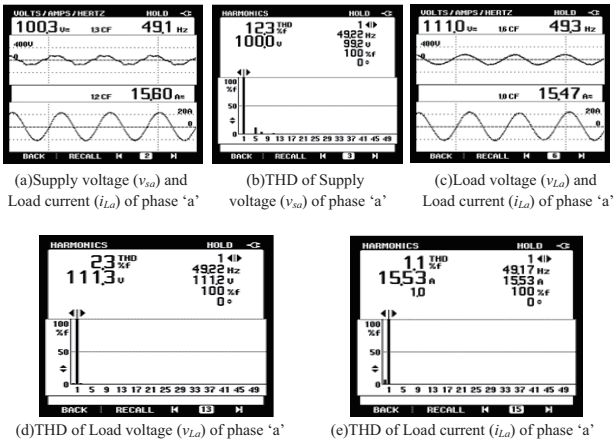
Fig. 14. Test results showing unbalance compensation (a) supply voltage (v_{sabc}) with unbalance (b) compensated voltage (v_{cabc}) and (c) Load voltage after compensation (v_{Labc}).

performance of DVR when the supply voltage is imposed with sag, distortions, and unbalances due to various reasons respectively.

Fig. 12(a)-(c) depicts the three phase supply voltage (v_{sabc}) with sag, compensating voltage (v_{cabc}), and load voltage after compensation (v_{Labc}). The supply voltage with sag is found to be 101 V RMS whereas that of the load voltage after compensation is 112 V RMS with compensated voltage of 21 V RMS. Fig. 13 (a)-(c) shows the distorted three supply voltage (v_{sabc}) with 104 V RMS, compensating voltage (v_{cabc}) of 16 V RMS, and load voltage after compensation (v_{Labc}) is of 112.5 V RMS. Three phase supply voltage (v_{sabc}) with unbalances, compensating voltage (v_{cabc}), and load voltage after compensation (v_{Labc}) are presented in Fig. 14(a)-(c). The supply voltage including unbalance is found to be 99.5 V RMS whereas that of the load voltage after compensation is 114.7 V RMS having a compensated voltage of 17.9 V RMS. It is to be clear that, all the RMS values mentioned in this section are not accurate values of dynamics because DSO screen displaying portion contains both normal state and dynamic state. In all the cases the DC-Link voltage is seen maintaining at its reference value i.e. 150 V.

C. Harmonics Analysis

During the supply voltage distortion, the steady-state performance of the system has been studied for the harmonic analysis of DVR performance. This analysis has been done by measuring the Total Harmonic Distortion (THD) of corresponding waveforms of the Source voltage (v_{sa}), Load voltage (v_{La}), and Load current (i_{La}) of phase 'a' as reported in Fig. 15(a)-(e). The supply voltage with distortions having RMS voltage of 100 V of 12.3 % THD are shown in Fig. 15 (a) and



(a)Supply voltage (v_{sa}) and Load current (i_{La}) of phase 'a'

(b)THD of Supply voltage (v_{sa}) of phase 'a'

(c)Load voltage (v_{La}) and Load current (i_{La}) of phase 'a'

(d)THD of Load voltage (v_{La}) of phase 'a'

(e)THD of Load current (i_{La}) of phase 'a'

Fig.15. Test results showing steady state performance of DVR.

(b). Fig. 15(c) and (d) represents the load voltage of 110 V RMS with 2.3% THD respectively. The load current is also checked for its harmonics, it has been observed that the load current of phase 'a' is shown in Fig. 15(e) is having the RMS value 15 A of current with 1.1% THD. From the steady-state analysis, it is clearly shown that the compensated load voltages and load currents have been found to be in the range of IEEE Std 519-2014.

VI. Conclusions

Three-phase AANF based control algorithm has been developed for DVR. With the proposed control algorithm, DVR has been used for compensating the different types of voltage related issues namely, voltage sag, voltage swell, voltage distortions, and imbalance in the supply voltage. WOA based PI controller gains estimation used in this control algorithm has been providing the approximate PI gains and helping in the speedup of the control process. The simulation study has been done when the supply is imposed with all aforesaid issues. However, the discussion of test results has been presented for three cases voltage sag, distortions, and unbalances in the supply voltage. It has been observed that the DVR with proposed control algorithm producing the satisfactory performance in all the cases. Distortions in supply voltage have been compensated by DVR and the load voltage has seen to be distortion free and within the range of IEEE Std. The PI gains yielded by WOA optimization technique are well utilized in maintaining the DC-Link voltage and terminal voltage at their respective reference levels. The main advantages of proposed three-phase AANF based control algorithm, with WOA optimization technique observed are listed as follows:

- Online estimation of magnitude (A), frequency/phase (θ), fundamental and its 90° phase shifted components, and sequential components of a given distorted signal.
- PLLs and Transformations are not required, so that the computational burden on the control algorithm is reduced.
- PI gains are estimated very accurately within less time as compared to manual tuning.

Observing the above said benefits with proposed AANF control algorithm, DVR is able to compensate all the mentioned power quality indices. The validation of proposed control algorithm has been done by using the simulation and laboratory results of DVR.

Appendix A

System Parameters for Simulation Performance

AC grid- 400 V, 50 Hz; 15 kVA load with 0.85 p.f. (Lagg.); $v_s = 0.7*231 = 162$ V; $i_{Load} = 21.65$ A; $kVA_{T/F} = 3*162*21.65/1000 = 10.52$ kVA ≈ 11 kVA, 200/100 V; $V_{DC} = 300$ V; $C_{DC} = 3300$ µF; $L_f = 1.5$ mH; $R_f = 6\ \Omega$ and $C_f = 10$ µF; Cut of frequency of low pass filter at DC bus = 10 Hz, Cut of frequency of low pass filter at AC bus = 12 Hz, Switching frequency of VSC (f_{sw}) = 12 kHz: Sampling time (t_s) = 20 µsec.

Appendix B

System Parameters for Test Performance

AC grid- 110 V, 50 Hz; 3 kVA load with 0.85 p.f. (Lagg.); (i_L) = 15.74 A; $kVA_{T/F} = 2$ kVA, 100/50 V; $V_{DC} = 150$ V; $C_{DC} = 3300$ µF; $L_f = 1$mH; $R_f = 3\ \Omega$ and $C_f = 20$ µF; Switching frequency of VSC (f_{sw}) = 5 kHz, Sampling time (t_s) = 45 µsec.

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Distortion Minimization for Ultra-Low THD Class-D Power Amplifiers

Mario Mauerer and Johann W. Kolar

***Abstract*—The effects of key sources of total harmonic distortion (THD) in power output signals of digitally controlled switch-mode (Class-D) converters/amplifiers are analyzed. Extensive measurements with a 400 V amplifier prototype, based on gallium nitride (GaN) power transistors, support the investiga-tions. First, the semiconductor loss model and a comprehensive circuit simulation of the converter with its closed-loop feedback system is presented to provide insights on distortion caused by junction temperature variation of the power transistors. Half-bridge interlock time is identified as a significant source of nonlinearity and hence, three simple and effective methods to reduce its deteriorating effect on THD are presented. Another important contribution to linearity arises from the closed-loop feedback controllers, which benefit from small delays and/or, high converter switching frequencies. It is also shown how a Kalman filter, which can be used to significantly reduce converter output noise, deteriorates the THD due to its linear system model. Finally, a method to reduce harmonic distortion and other disturbances caused by a non-ideal DC supply is also demonstrated. By rigorously eliminating distortion sources and applying the presented compensation methods, amplifier output current THD values below −100 dB (0.001%) are achieved and experimentally verified in wide load current ranges.**

***Index Terms*—Dead time, feedback control, feedforward compensation, high power amplifiers, Kalman filter, total harmonic bistortion (THD), wide-bandgap semiconductors.**

I. Introduction

PRECISION switch-mode, i.e., Class-D amplifiers are power electronic converters that provide output voltage or current waveforms with little deviation from (often arbitrarily shaped) reference input signals. Consequently, additional output signal components, such as noise or harmonic distortion, are unfavorable for different industrial, medical and research applications.

In high-energy particle accelerators, such amplifiers provide the currents for the superconducting magnets and beam forming structures. They operate with output powers exceeding 100 kVA, while achieving steady-state current accuracies below 10 ppm (with respect to the full-scale current) [1], [2]. Medical magnetic resonance imaging (MRI) applications require high-bandwidth, high-current and low-noise power converters to drive gradient coil currents, with amplitudes regularly in excess of 500 A. The coil current quality strongly influences the imaging capability [3], [4].

Nanoscale-precision positioning applications, required in integrated circuit manufacturing processes, employ different actuators such as magnetic bearings or linear motors that are supplied with currents of low noise and/or low distortion in order to prevent the generation of undesired forces and thus, disturbing movements of the positioning systems [5]. Due to continuously shrinking semiconductor feature sizes and the desire for an increased manufacturing throughput, the requirements with respect to noise, linearity and power of precision amplifiers that drive such actuators with controlled currents, are increasing equally [6], [7].

Due to stringent requirements on actuator current noise and distortion in high-precision positioning applications, linear or hybrid power amplifiers, together with analog feedback control systems, are often employed [8]–[10]. For nanoscale positioning applications, THD figures below −90 dB are desired. However, for high-power applications, e.g., high-speed positioning systems or MRI, linear or hybrid amplifiers are difficult to employ due to their restricted output power capability, limited scalability and reduced efficiency [11], [12]. These disadvantages can be overcome with switch-mode power converters. Furthermore, a digital control system, as opposed to analog controllers, is deployable on different converters with only minor modifications, which reduces development time and cost. It also significantly improves design flexibility and allows the application of advanced control system and signal processing concepts.

The considered motion systems are characterized by positioning stages with little damping and friction (e.g., due to the usage of air or magnetic bearings) and thus, the noise current easily translates to undesired forces or torques of the actuators [13]–[15]. Noise components of the output currents are of special disadvantage in mechatronic positioning applications that rely on slowly varying or static currents, e.g., in magnetic levitation bearings or vibration isolation systems [16], [17].

Distortion arises due to nonlinear transfer functions in the amplifier signal and power paths, and can manifest itself with spectral components at integer multiples of the output signal's desired fundamental frequency (i.e., harmonics). If the desired output signal contains more than one frequency component, intermodulation distortion occurs [18]. These effects require consideration in continuously moving mechatronic applications like integrated semiconductor lithography or excimer laser annealing of displays, where the actuator current should not contain harmonics, or other unwanted signal components originating from nonlinear effects in the power amplifiers,

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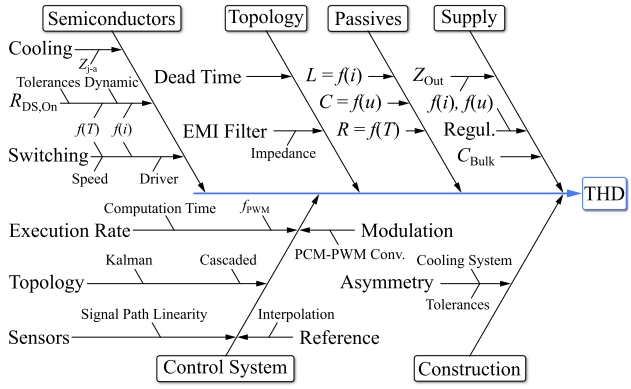

Fig. 1. Nonidealities of system components influencing the total harmonic distortion (THD) of the output quantities of digitally controlled switch-mode power amplifiers. $f(T)$ indicates a dependency of the temperature T. Likewise, i and u represent currents and voltages, respectively. PCM: Pulse-code modulation.

in order to reproduce the demanded forces (and hence, the movements) as exactly and linearly as possible [5], [7], [19].

This work investigates different sources of harmonic distortion and their significance in a digitally controlled, precision switch-mode power amplifier. Fig. 1 lists key system components and nonidealities that contribute to output distortion [7], [20]–[22]. A hardware demonstrator system is used to support the presented insights with measurements. It operates as a single-phase DC/AC inverter and can provide up to 400 V and a controlled output current of up to 25 A (peak) to a resistive-inductive load. Fundamental amplifier output current frequencies for common mechatronic applications range from several hertz up to hundreds of hertz. The results presented in this work are applicable for a wide frequency range, as outlined in the corresponding sections of this work. Four half-bridges, encompassing gallium nitride (GaN) enhancement-mode high-electron-mobility (E-HEMT) power transistors (*GaN Systems, GS66508T*), allow the implementation of two different power stage topologies, which is used in the investigation of dead time related distortion. This work does not consider sources of noise in the discussed amplifier systems, only harmonic distortion. This is possible as the underlying and systematic causes of noise and distortion are fundamentally different and rarely interacting. However, the topic of noise is covered by a second, future publication of the authors in this journal.

Several key contributions arise from this work. The recent availability of fast-switching gallium nitride power semiconductors in low-parasitic packages enables kilowatt-range power amplifiers with unprecedented output distortion figures. This is verified with detailed measurements that reveal THD values below −100 dB. To facilitate the usage of the new power devices in industrial applications, detailed loss models and converter design guidelines, with respect to low-distortion amplifiers, are presented. Furthermore, different methods have been discussed in the past that aim to mitigate distortion caused by half-bridge interlock/dead time. The flexible hardware demonstrator utilized in this work allows a direct comparison of three important distortion reduction techniques. Their specific advantages and implementation details are discussed and verified with comprehensive measurements in order to facilitate future design decisions. Furthermore, modern high-performance signal processors enable extraordinary high-frequency, high-gain feedback controllers. Control system considerations and measurements with different configurations highlight the effect and limits of this important system component. Additionally, the construction and verification of the discussed ultra-low-distortion power amplifiers requires specialized components and design approaches, and sophisticated measurement techniques, which are presented in detail. Hence, this work provides sensitivity analyses of amplifier subsystems with respect to distortion such that amplifier designers can direct their resources and attention to the critical system components.

The amplifier system, including its underlying design decisions, is introduced in Section II. After introducing the semiconductor loss model, Section III investigates to what extent the thermal variation of the power transistor junction temperatures contributes to load current THD. Next, Section IV presents the deteriorating effect of the half-bridge interlock time on load current THD and introduces three methods to effectively reduce this distortion component. Measurements demonstrate the performances. Section V illustrates and experimentally verifies how the THD performance of the closed-loop control system is increased with the converter switching frequency. In this context, the effects of a Kalman filter on load current THD are also discussed. The sensitivity of the power amplifier to its DC supply is investigated theoretically and experimentally in Section VI. All in all, amplifier load current THD figures of −100 dB are achieved in wide load current ranges with the demonstrator system. Finally, Section VII presents a brief conclusion and an outlook on amplifier systems of even lower THD.

II. System Overview

A hardware demonstrator serves as versatile test bed for the investigation of different key influence factors on load current THD. Fig. 2 illustrates its power stage topology, driving a single-phase bridge-tied load, i.e., it is connected between two phases, each comprising two interleaved converter half-bridge legs. This allows the application of the full DC-link voltage to the load and provides a better power supply rejection than a single-ended amplifier configuration [24]. The two interleaved half-bridges in each phase enable the implementation of two operating modes. If both half-bridges conduct an (ideally) identical current, the regular interleaved topology is employed. A second mode of operation, known as dual buck converter, is achieved by introducing a circulating current to the two half-bridges in each phase, with the effect that the dead-time related distortion can be reduced, as shown in [7], [20], [25]and in Section II-B below. The EMI filters at the input and output of the converter ensure compliance with common norms and protect sensitive equipment near the load from high-frequency signal components. By changing the phase shifts between the

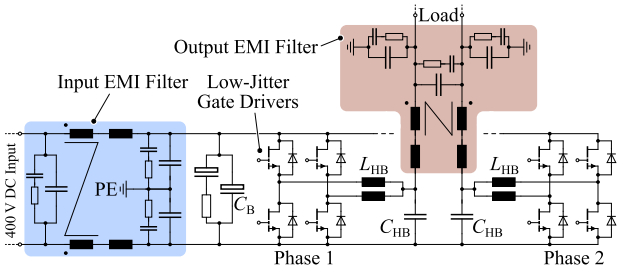

Fig. 2. Hardware demonstrator power circuit topology. Two interleaved half-bridges in two phases drive a bridge-tied load. C_B = 1.8 mF, C_{HB} = 12 µF, L_{HB} = 700 µH. The low-jitter gate drivers are presented in [23].

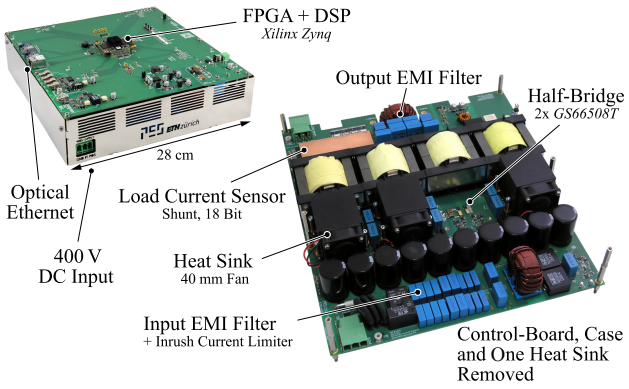

Fig. 3. Hardware demonstrator (with and without enclosure) employing four 650 V GaN (*GaN Systems GS66508T*) half-bridges, high-resolution ADCs and a high-performance digital processor and FPGA. The max. input voltage is 400 V DC. The system is capable of driving a single-phase bridge-tied load with current amplitudes up to 25 A peak.

PWM carriers of the four half-bridges, the high-frequency spectral content (both common-mode and differential-mode components) of the load voltage can be influenced [21]. The demonstrator hardware is depicted in Fig. 3.

A. Power Semiconductors

As the switching behavior of the power transistors influences the amplifier's achievable THD, fast-switching state-of-the-art gallium nitride power transistors (*GaN Systems GS66508T,* 650 V, 30 A, 50 mΩ) are employed to create a power stage that can provide output signals of inherently low distortion [20]. The converter is designed for an input voltage of ≤ 400 V DC and the load current amplitude $\hat{i}_L$ can reach 25 A (e.g., peak value of a sinusoidal signal). The expected output frequencies range from DC up to ≈ 200 Hz, which is a common range in mechatronic motion systems. The converter's switching frequency extends to 200 kHz, which is facilitated by the fast switching speed of the GaN transistors and their lack of a reverse recovery effect, resulting in low hard-switched losses. As the switching transistors are cooled from the top side, no thermal printed circuit board vias are required, which would otherwise disrupt the commutation loop of the half-bridges. This enables low-inductance commutation loops and fast switching actions with little voltage overshoots and ringing [23]. Fig. 4 illustrates the circuit board crosssection of a top-cooled

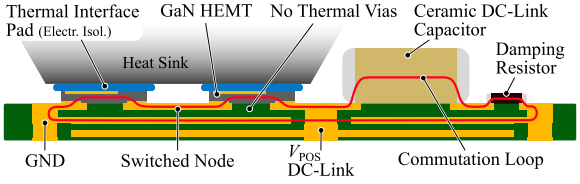

Fig. 4. Simplified circuit board cross-section illustrating the layout of a top-cooled half-bridge. The lack of thermal vias allows for a low-inductance vertical commutation loop. Only the top two copper layers are shown. Geometric proportions are altered for better visualization.

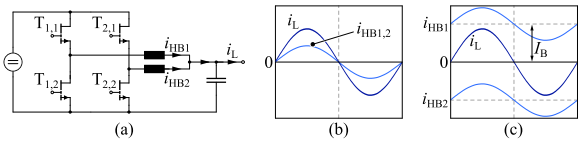

Fig. 5. (a) Interleaved power stage topology of one phase of the prototype system. (b) Regular interleaved operation, where each half-bridge conducts an identical current. (c) Dual buck operation: A circulating bias current renders the half-bridge currents unidirectional. The bias current is introduced by altering the reference currents with the feedback control system according to (1).

half-bridge, featuring one heat sink and a 40 mm fan for forced air cooling (cf. Fig. 3).

Each transistor is driven by an *LM5114* gate driver with separate turn-on/off resistors of 6.7 Ω and 3.3 Ω, respectively. The gate voltage applied to turn the transistors on is 6 V and −3.3 V to ensure reliable turn-off. The gate control signal is isolated using a low-jitter digital isolator (*Si8271*, 40 ps RMS jitter, 30 ns delay), which reduces wideband noise in the switched half-bridge output voltages [23], [26].

Short (i.e., 30 ns) half-bridge interlock/dead times are achieved with the fast-switching GaN transistors. This is the time interval T_D required between the turn-off of a half-bridge transistor and the subsequent turn-on of the complementary device, during which both power transistors are turned off, in order to prevent a destructive half-bridge shoot-through or short-circuit. SiC Schottky diodes (*CREE C3D1P7060Q*) are placed in parallel to the transistors to conduct the current during the dead time interval in order to eliminate the otherwise high voltage drop of the GaN transistors in reverse conduction [27]. As shown in this work, low dead times significantly reduce amplifier output distortion and are thus highly beneficial for the discussed applications.

B. Power Circuit Topology

Fig. 5(a) illustrates the interleaved half-bridge converter legs of a phase of the demonstrator system (which employs two phases in total, cf. Fig. 2). Conventionally, both half-bridge currents $i_{HB1,2}$ are ideally identical, as shown in Fig. 5(b). For this regular operating mode, it is well-established that dead time is a significant cause of distortion in the half-bridge output waveforms, as further explained in Section IV below.

The dual buck (DB) power stage topology, also named opposed current converter or balanced current amplifier, whose operating principle is described in [7], [20], [28], [29], does traditionally not require dead time and is hence not subject to

this cause of distortion. Its key characteristic is the introduction of a circulating bias current to the two interleaved half-bridges, such that each half-bridge exhibits unipolar currents:

$$i_{\mathrm{HB1,2}}(t) = i_{\mathrm{L}}(t)/_2 \pm I_{\mathrm{B}}. \quad (1)$$

The resulting current waveforms are illustrated in Fig. 5(c). This also has the effect that the half-bridge currents are dominated by the (constant) bias current and are thus less modulated by the load current. This renders the variation of the half-bridge voltage switching transitions less pronounced, which further reduces distortion.

As the half-bridge currents are unipolar, the two half-bridge transistors $T_{1,2}$ and $T_{2,1}$ could be replaced with power diodes, which would constitute the conventional dual buck topology [7]. However, this is not done in the demonstrator system in order to improve the efficiency and linearity of the topology, as analyzed in [20]. A dead time is then still required, but, due to the unipolar half-bridge currents, it does not affect the voltage-forming behavior of the half-bridges and hence, does not introduce distortion.

Starting from a conventional, interleaved half-bridge operation, the dual buck behavior is simply obtained by introducing the circulating current between the two half-bridges by means of the control system, i.e., the half-bridge current references of the two half-bridge P-controllers are adapted according to (1). It should be noted that the bias current can be modulated to reduce losses, as shown in [7]. However, this increases distortion and is thus not further considered.

As the dual buck operating mode results in higher transistor RMS currents, the resulting losses must be carefully considered to prevent additional distortion and thermal overload. Therefore, Section III-A introduces the loss model of the GaN E-HEMTs.

C. Feedback Control System

To increase the amplifier's reference tracking and disturbance attenuation performance, a closed-loop feedback con-trol system is used. Its structure is illustrated in Fig. 6. It comprises three cascaded controllers. A type-III (lead-lag) controller regulates the amplifier's precision output current. It provides the load voltage references to the two proportional-integral (PI) phase voltage controllers. The innermost control loop consists of proportional (P) controllers that act on the half-bridge currents. All feedback loops are tuned, using loop shaping, to achieve open-loop phase margins of at least 50° and gain margins of ≈ 6 dB, while the gains of the open-loop transfer functions are maximized to achieve a high disturbance rejection in each loop [30], [31]. This necessitates the careful analysis of the time delays in the controlled plants, caused by the PWM and the calculation of the feedback controllers [31], [32]. These delays reduce the controller phase margins. The gain of the proportional half-bridge current controllers could be selected arbitrarily high if there was no such delay, as their plants exhibit only first-order integrative characteristics.

Fig. 7 illustrates the important time delays. At the start t_{u} of each PWM cycle, the necessary measurements are obtained and the error signals for the feedback controllers are formed. As all controllers are implemented with digital logic in an FPGA, they can therefore provide the newly calculated duty cycles (i.e., the inputs to the controlled system) before the start of the next PWM period, i.e., during the time $T_{\mathrm{D,Ctrl}}$. Due to the triangular carrier, the delay of the PWM is constant: $T_{\mathrm{D,PWM}} = T_{\mathrm{PWM}}/2$ [32].

Consequently, the PWM frequency of the power converter influences the achievable performance of the feedback control system, as, with reduced delays, higher open-loop gains can be achieved for the given required phase margins. Fig. 8 exemplarily shows the difference in control system performance when the controller is tuned for a PWM rate of 100 kHz and 200 kHz. The open-loop gain (which is a measure of the disturbance rejection capability [30]) is ca. 9 dB larger when the converter (and the control system) operate at 200 kHz in-stead of 100 kHz. The indicated gray area is maximized during controller tuning, using a numerical optimization method that performs the loop shaping of the individual feedback loops, with consideration of the aforementioned time delays and the required phase/gain margins.

All controllers are executed synchronously with the converter switching frequency (regular symmetric PWM sampling) [33]. However, they can also be updated twice per PWM cycle (regular asymmetric sampling), with the result-ing implications and limitations discussed in Section II. In order to reduce the quantization noise of the low-resolution PWM, digital delta-sigma noise shapers are employed. They do not affect THD, as they only act on the modulator's quantization noise [34]. As the ratio of the PWM sampling rate (f_{PWM}) to common load current fundamental frequencies f_{F} is high (> 500), distortion caused by the sampling of the PWM modulator is not relevant, as it is in the order of ≈ −110 dB (THD) for the discussed system [33], [34]. However, for mechatronic applications with fundamental frequencies in excess of ≈1 kHz (e.g., magnetic bearings in high-speed motors), the modulation harmonics potentially become considerable. For such applications, the modulation method must be changed (e.g., by means of a hysteretic modulator), or the PWM frequency must be sufficiently increased [33].

Remark: Sensor noise can be reduced by utilizing a Kalman filter that provides the low-noise estimates of the voltages and currents for the feedback system, as also shown in Fig. 6 [35]. Details of the converter noise performance are not scope of this paper. Nonetheless, Section V-A presents implications of the Kalman filter on the amplifier linearity.

All important system voltages and currents are measured using high-resolution, low-noise acquisition systems as indicated in Fig. 6. All analog-to-digital converters (ADCs) feature an amplitude resolution of 16 bits and a maximum sample rate of 1 MHz (*LTC2368-16 and ADS8861*), except for the load current ADC, which is an 18-bit, 5 MHz device (*AD7960*) in order to minimize the intrinsic sensor noise of the load current measurement. All currents are measured using shunt resistors (with isolated ADCs), as this enables a superior

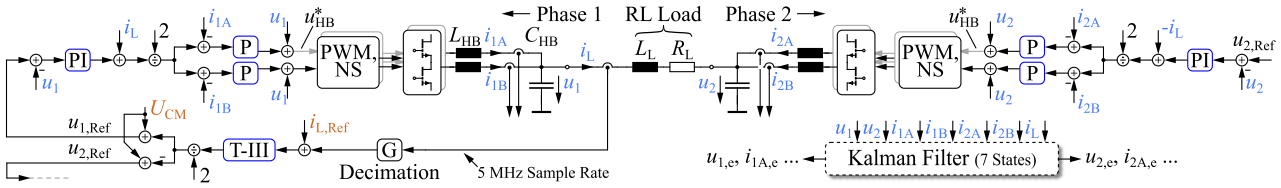

Fig. 6. Cascaded control system structure of the hardware demonstrator. The pulse-width modulators employ digital noise shapers (NS) to reduce quantization noise. The control topology comprises of three cascaded controllers with feedforward compensation. Proportional (P) current controllers are used for the four half-bridge currents, proportional-integral (PI) voltage controllers for the two phase voltages and a type-III (lead-lag) controller for the load current. L_{HB} = 700 µH, gapped ferrite core. C_{HB} = 12 µF, film capacitors.

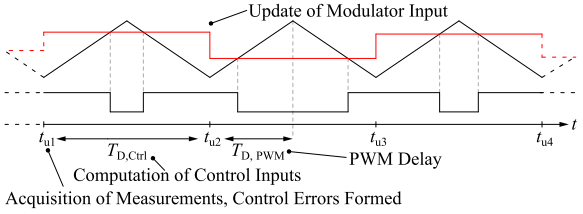

Fig. 7. Time delay model for the forward path of the P-type current controller plants. The total delay is $T_{Fwd} = T_{D,Ctrl} + T_{D,PWM} = 1.5T_{D,PWM}$. The control system performance improves with increased switching frequencies.

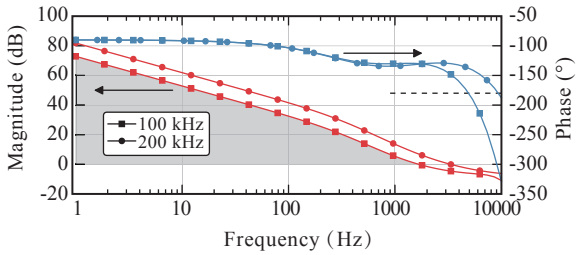

Fig. 8. Open-loop bode plot of the type-III load current controller and its plant (5 Ω + 2.5 mH load configuration) for PWM frequencies of 100 kHz and 200 kHz (which correspond to the control system execution frequencies). The gray area is maximized by controller tuning.

noise and distortion performance as compared to integrated solutions [36]. The DC-link and phase voltages (≤ 400 V) are measured using resistive dividers that are optimized for low noise and distortion [36]. The 5 MHz load current ADC employs oversampling and a 6th-order anti-aliasing Butterworth filter. This sensor is capable of measuring THD down to a level of ≈ −110 dB, which is mainly limited by the operational amplifiers in its gain stage and anti-aliasing filter (*LT1028, AD8620* and *ADA4932*) [36]. This is sufficient for the demonstrated performance, as the THD is limited by other factors, such as half-bridge dead time.

Due to the large number of high-speed and high-resolution ADCs, as well as the need to calculate complex control system tasks, such as a Kalman filter, a high-performance processing system (*Xilinx Zynq Z-7020*) is used to manage converter operation [37]. It features an FPGA as well as two 666 MHz *ARM Cortex-A9* CPUs with double-precision floating-point units. A 1 GiB DDR3 memory is connected to the processing system, which allows the recording of large amounts of internal data, such as ADC samples. A 100 Mbits^{-1} optical Ethernet link (*100BASE-FX*) facilitates the transmission of such data to an external computer for further analysis and processing.

D. Measurement Methods and Definitions

Common loads for the discussed precision amplifiers are often electromagnetic actuators or magnetic bearings that can be described by a series connection of a load inductor L_L and a load resistor R_L. For linear permanent magnet motors, values for R_L are in the range of 1 Ω to 10 Ω , whereas the inductance values L_L range from 100 µH to 100 mH. Consequently, three different resistive-inductive loads are used for all measurements presented in this work: 2 Ω + 10 mH, 5 Ω + 2.5 mH and 10 Ω + 100 µH. The load resistors and inductors need to be highly linear as they otherwise introduce undesired distortion components which prevents an accurate evaluation of the converter THD. Consequently, for the load resistors, thick film, high-power resistors with a low thermal coefficient of resistance are used (*Vishay LPS 600*), that implement the three different load resistance values. The magnetic cores of the load inductors are made from laminated silicon steel (designed for low-frequency power grid applications) in case of the 2.5 mH and 10 mH inductors, whereas the core of the 100 µH inductor is a gapped ferrite. All inductors have a sufficient current and saturation rating of > 25 A RMS. Their respective linearities are demonstrated with measurements in Section V.

As the power amplifier is capable of supplying a current with very low distortion, a sufficiently linear and low-noise sensor is required to accurately obtain a reference current measurement. Consequently, a *LEM IT 65-S* flux-gate current transducer is used as reference current sensor to measure the amplifier load current THD [38]. Three primary winding turns are used to fully utilize the sensor's range. Its burden resistor has a value of 47 Ω and consists of ten paralleled metal film resistors to minimize power dissipation and thus, maintain lin-earity. The burden voltage is measured with a *Rohde&Schwarz UPV* audio analyzer, which is a low-noise, high-precision spectrum analyzer [39]. This setup can measure THD levels of ≈ −108 dB (dominated by odd harmonics and limited by the *LEM* current sensor), which is sufficiently accurate for the presented measurements. All measured THD and SNR figures in this work are directly obtained by this instrument.

In order to measure the amplifier output THD, a sinusoidal digital current reference $i_{L,Ref}$ (cf. Fig. 6) is used with a fundamental frequency f_F of 35 Hz or 210 Hz. The amplifier then also creates a load current with the same fundamental frequency. This selection of f_F ensures that its harmonics do not interfere with

the 50 Hz grid harmonics that are being coupled into the *LEM* current sensor through external stray fields, but are not present in the actual load current (as determined by experimental validations). Furthermore, these frequencies are in the range of common actuator current frequencies used in positioning applications. The THD of the load current is defined as:

$$\mathrm{THD} = 20\log_{10}\frac{\sqrt{i_2^2+i_3^2+\cdots+i_9^2}}{i_1}, \tag{2}$$

where i_1 is the current amplitude of the fundamental component (at frequency f_F) and $i_2 \ldots_9$ are the amplitudes of the first eight integer harmonics of the fundamental (at frequencies $k f_F$, with $k \in [2, 3, \ldots, 9]$).

Two different high-power DC supplies (*HP 6035A* and *Sorensen SGI 600-17*) are used for the measurements, whereas their selection does not affect the measured THD figures (but the achievable load currents, due to their output limits), as verified by measuring the amplifier's output THD with both DC supplies in certain measurements.

III. Distortion Due to Power Transistor Junction Temperature Variation

Commonly used switching transistors in power electronic converters exhibit a nonlinear behavior of the on-state resistance $R_{DS,on}$ as a function of the junction temperature [27], [40]. Naturally, the total transistor losses and hence, T_j and $R_{DS,on}$, are a function of the converter operating point (i.e., its output current and/or voltage), which causes a modulation of the main conduction path resistances and hence, harmonic distortion. Even as modern wide-bandgap semiconductors show a less pronounced temperature-dependent $R_{DS,on}$ than their silicon counterparts [27], this nonlinear effect has to be considered for highly linear amplifiers, which necessitates a detailed power transistor loss model.

A. Transistor Loss Model

The majority of power stage losses are generated by the hard-switching GaN transistors. Consequently, to prevent thermal overload and to optimize the utilized transistors with respect to the active die area, their losses and thermal model is presented.

The evaluation of the transistor switching losses is aggravated by the fact that they depend significantly on the gate drive configuration, and sufficient data is rarely found in data sheets. Loss measurements of the utilized GaN power transistors for soft- and hard-switching transitions are provided in [41], which are used here to derive the transistor losses occurring during a complete PWM cycle as a function of the half-bridge current and the DC-link voltage. The loss model is extended by incorporating additional parasitic capacitances, which cause increased hard-switching losses (e.g., due to the PCB routing or the half-bridge inductors). Dynamic behavior of the transistor on-state conduction resistance $R_{DS;on}$ is not observed and is thus not modeled [42]. The resulting loss energies for each half-bridge transistor during one PWM cycle (i.e., two switching transitions) are illustrated in Fig. 9 for a DC-link voltage of 400 V and under the assumption of a constant half-bridge current during the PWM cycle. Measurements of the overall converter losses corroborate the accuracy of this transistor loss model. The polynomial fit for the high-side transistor switching losses are listed in TABLE I.

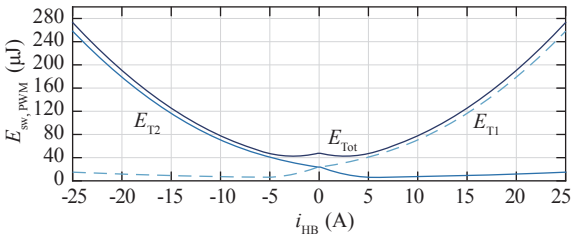

Fig. 9. Measured transistor switching loss energies for a half-bridge consisting of a high-side (T_1) and low-side (T_2) transistor (*GaN Systems GS66508T*) [41]. These energies are dissipated once per PWM cycle. Positive half-bridge currents i_{HB} flow out of the half-bridge (hard switching of T_1) and negative currents flow into the half-bridge switch-node (soft/partially soft switching of T_1). $u_{DC} = 400$ V. Gate driver: *LM5114*. Turn-on/off resistors: 6.7 Ω /3.3 Ω. Turn-on/off voltages: 6 V/ 3.3 V. Numeric fitting data provided in TABLE I.

TABLE I
Polynomial Fitting Coefficients for the Switching Energy E_{T_1} Dissipated During One PWM Cycle (See Fig. 9). Unit: µJ.

$$E_{T1} = c_0 + c_1 i_{HB} + c_2 i_{HB}^2 + c_3 i_{HB}^3 + \cdots + c_6 i_{HB}^6$$

Range of i_{HB}	c_0	c_1	c_2	c_3
0 A to 25 A	24.17	1.943	0.2544	0.001716
−25 A to 0 A	25.43	8.29	1.303	0.09475
	c_4	c_5	c_6	
0 A to 25 A	0	0	0	
−25 A to 0 A	0.003415	5.322e-5	1.985e-7	

To accurately model the transistor conduction losses, with consideration of the temperature-dependent $R_{DS,on}$, a computer simulation is employed. This allows to track the variation of the junction temperature T_j during converter operation with fundamental output frequencies f_F of several tens of hertz, which are common in mechatronic positioning applications. Note that a simple thermal model, consisting only of thermal resistances, is insufficient to correctly model the behavior of T_j during a fundamental period, as the converter is not operated with a constant load current and hence, the thermal capacitances greatly influence the dynamics of T_j. Fig. 10 illustrates the thermal simulation model employed for each transistor. Once per PWM cycle, the individual conduction and switching losses (P_C, P_{Sw}) are evaluated and applied to the equivalent thermal model, which consists of two capacitances and resistances that implement the important thermal dynamics. The capacitance C_j and resistance R_{jc} model the thermal behavior of the transistor chip. Their values are often provided by manufacturers or can be extracted from the transient thermal impedance curve often found in power transistor data sheets. C_{HS} and R_{ca} represent the heat sink and the thermal resistance from transistor case to

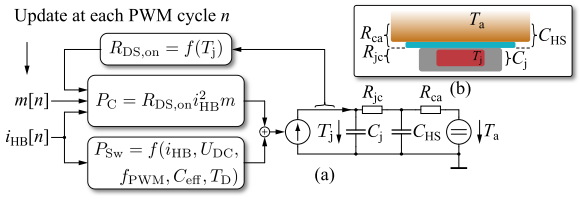

Fig. 10. (a) Thermal model used to simulate the thermal cycling of $R_{DS,on}$ during amplifier operation, including transistor conduction and switching losses. (b) The model uses the thermal junction-case resistance R_{jc}, the thermal junction capacitance C_j, the thermal resistance of the heat transfer pad and the heat sink to ambient, R_{ca}, and the thermal capacitance of the heat pad and heat sink, C_{HS}. The modulation index m is the relative on-time of the high-side half-bridge transistor during one PWM cycle.

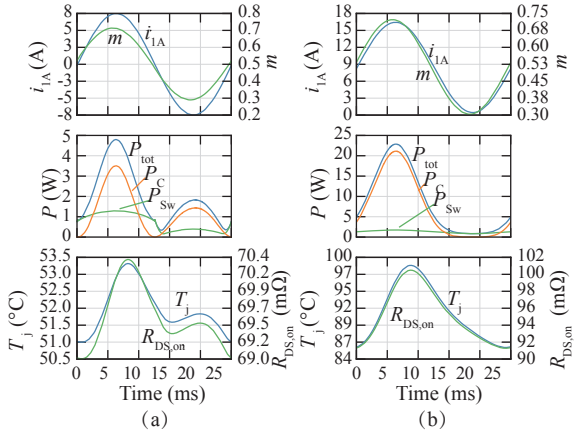

Fig. 11. Simulation results of the thermal behavior of a high-side half-bridge transistor during one fundamental load current period. (a) Regular interleaved mode. (b) Dual buck current control. m: half-bridge modulation index (relative turn-on time of the high-side transistor during a PWM period). Middle plots: transistor losses, $P_{tot} = P_C + P_{Sw}$. $\hat{i}_L = 16$ A, $f_F = 40$ Hz, $I_B = 8$ A, $f_{PWM} = 100$ kHz, $u_{DC} = 200$ V, $L_L = 2.5$ mH, $R_L = 5\,\Omega$, $T_a = 40$ °C, $R_{jc} = 0.5$ K W^{-1}, $C_j = 2.4$ mF, $R_{ca} = 5.5$ K W^{-1}, $C_{HS} = 10$ mF.

ambient. Values are given in Fig. 11. It is assumed that the heat sink fins and base plate are fixed at the ambient temperature T_a. This is justified as the heat sink has a comparably large thermal capacitance due to its mass and hence, its temperature variation is negligible. However, the thermal capacitance C_{HS} models the capacitance of the less massive heat spreader, which connects the transistor case thermally to the base plate of the heat sink. The values of this capacitance/resistance are found using a thermal 3D FEM simulation that incorporates the utilized geometries and required material properties.

The temperature dependence of the $R_{DS,on}$ is usually provided by manufacturer data sheets, which facilitates the evaluation of the transistor conduction losses [27], [40]. Note that, as this model incorporates the important nonlinearities, it is capable of predicting thermal runaway, which can be caused by high transistor losses and the fact that the currents are impressed by the feedback control system. The disadvantage of this approach is that the thermal system requires time to reach its steady-state value, which prolongs simulations. This can be alleviated by initializing the thermal model to the expected temperatures.

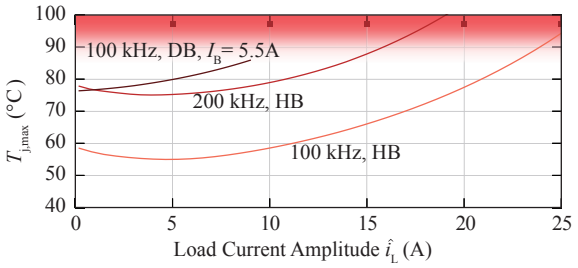

Fig. 12. Calculated peak junction temperatures during converter operation with PWM frequencies of 100 kHz and 200 kHz for the regular interleaved half-bridge (HB) and dual buck (DB) configurations (with a constant bias current of I_B = 5.5 A). This is valid for all considered load configurations and for fundamental load current frequencies below ≈ 40 Hz.

B. Amplifier Operating Range

Using the presented thermal model, incorporated into a complete converter circuit model and also including the cascaded feedback control system, the transistor thermal behavior can be investigated [43]. Fig. 11 exemplarily illustrates simulation waveforms. The load current i_L is sinusoidal with an ampli- tude $\hat{i}_L$ of 16 A and a frequency of 40 Hz. In Fig. 11(a), the converter is operated with the regular, interleaved power stage topology. It can be seen that the junction temperature varies by ≈ 2.3 K. On the other hand, if the converter is operated with the dual buck mode (cf. Fig. 11(b)), which results in higher half-bridge currents as indicated, a variation of T_j of ≈ 12 K ensues, which consequently also leads to a higher variation of the $R_{DS,on}$.

This simulation approach can be used to investigate the converter's highest allowable load current amplitude for a given operating configuration. The load current limit is set such that the peak junction temperature of the power transistors does not exceed ≈ 90 °C, in order to prevent thermal runaway and to provide some safety margin. The operating point illustrated in Fig. 11(b) exceeds this boundary, as the peak junction temperature reaches 98 °C. The allowable load current limits for different operating modes used in this work are illustrated in Fig. 12. Note that the transistor losses are practically independent of the chosen load resistor/inductor values, as they mainly depend on the switched current and not on the half-bridge duty cycles. The same applies for the fundamental frequency f_F of the sinusoidal load current, as the reactive power (due to the half-bridge filter capacitors) is negligible at the considered frequencies. It is evident that the dual buck approach, due to its circulating bias current and thus, the increased transistor losses, can provide less load current before the junction temperatures reach critical values, which is an inherent limitation of this operating mode [7].

The achieved overall peak power conversion efficiencies of the demonstrator system are illustrated in TBALE II. They are obtained using a power analyzer to measure the active power at the converter input and the load (P_L). Note that the auxiliary power required for control and cooling fans is not included. Depending on the fan speed, the converter requires ≈ 10 W to 30 W of auxiliary power. The shown conversion efficiencies demonstrate the advantage of switch-mode power converters as compared to hybrid or linear solutions. Furthermore, the

TABLE II
MEASURED PEAK POWER CONVERSION EFFICIENCIES OF THE DEMONSTRATOR SYSTEM FOR DIFFERENT LOAD CONFIGURATIONS

u_{DC}	f_{PWM}	$R_L + L_L$	$\hat{i}_L$	P_L	η
Regular Interleaved Topology:					
400 V	100 kHz	10 Ω + 100µH	18.5 A[a]	1.7 kW	96.5 %
		5 Ω + 2.5 mH	24.0 A	1.4 kW	94.4 %
		2 Ω + 10 mH	24.0 A	576 W	88.0 %
400 V	200 kHz	10 Ω + 100 µH	16 A	1.3 kW	94.7 %
		5 Ω + 2.5 mH	16 A	640 W	90.4 %
		2 Ω + 10 mH	16 A	256 W	80.3 %
Dual Buck Topology (I_B = 5.5 A):					
400 V	100 kHz	10 Ω + 100 µH	8 A	320 W	85.4 %

[a] Limited by load resistor dissipation capability.

achieved output powers exceed typical values of precision amplifiers currently employed in industry. The loss model also reveals that with an ohmic load of 14 Ω, a DC-link voltage of 400 V and a PWM frequency of 100 kHz, a load power of 4 kW is thermally feasible (sinusoidal load current with $\hat{i}_L$ = 24 A).

As the power transistor losses limit the load current, the next section shows the possibility of optimally extending the achievable output current range by paralleling power transistors.

C. Extending the Load Current Range

It is illustrated how the load current range can be extended by changing the power transistor's active area (e.g., by placing two power transistors in parallel). This reduces the current of each transistor and hence, its losses and junction temperature, as shown above.

As the losses P_T of a single *GS66508T* transistor are known in detail (cf. Fig. 9), the losses of n parallel transistors, operating with a total half-bridge current i_{HB}, can be derived with:

$$P_{T,\,Tot} = nP_T\left(i_{HB}/n\right) \ . \tag{3}$$

This assumes that each transistor has its individual gate driver and cooling system, such that for each transistor, the same losses as presented in the previous section occur. Note that n does not necessarily have to be integer, as long as the gate driver and cooling system is also scaled accordingly.

The resulting total transistor losses are illustrated in Fig. 13 for different n and load current amplitudes $\hat{i}_L$, and a DC-link voltage of 400 V with a PWM frequency of 200 kHz. Note that these are the averaged transistor losses over one load current fundamental period. From this analysis, it can be seen that a single *GS66508T* transistor is the optimal selection for the operation with $\hat{i}_L \approx 20$ A at the indicated DC-link voltage and switching frequency. This extension of load current capability can similarly be achieved by introducing more interleaved half-bridges instead of paralleled transistors [44].

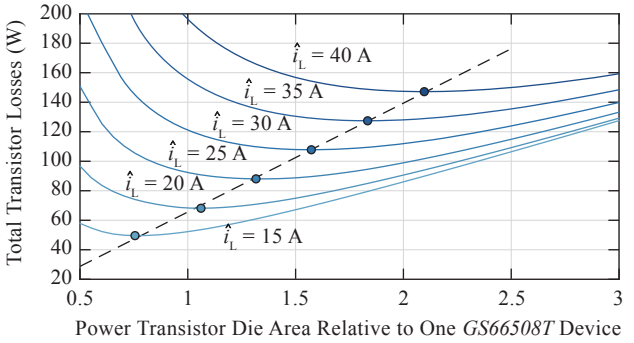

Fig. 13. Transistor losses (conduction and switching) of the demonstrator system, averaged over a fundamental period of the load current, for different load current amplitudes $\hat{i}_L$. The active transistor area is scaled relative to the active area of a single *GaN Systems GS66508T* transistor. f_{PWM} = 200 kHz, u_{DC} = 400 V. Regular interleaved power stage topology.

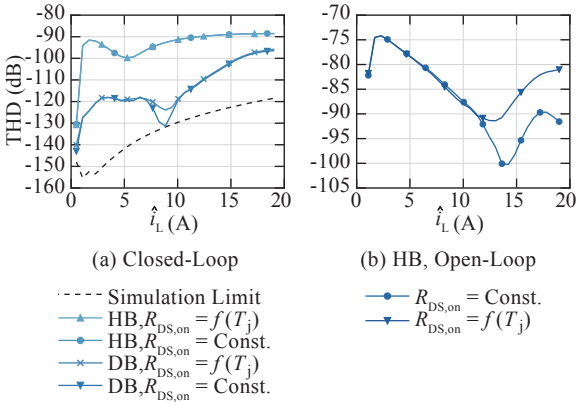

Fig. 14. Simulated THD of regular interleaved (HB) and dual buck (DB) topologies, incorporating thermal $R_{DS,on}$ cycling. (a) Closed-loop feedback control, T_D = 40 ns. (b) Open-loop operation, T_D = 10 ns. The simulation limit is the best achievable THD with an ideal amplifier model, only restricted by the simulation time step.

D. Distortion Analysis

The presented transistor losses and thermal simulation model is used, in conjunction with a circuit simulation of the power amplifier demonstrator that also includes its closed-loop feedback control system, to assess the load current THD, with consideration of the junction temperature variation of each power transistor [43]. This approach allows the direct manipulation of thermal system properties, such that their influences on THD can be methodically investigated. A similar investigation regarding open-loop amplifiers has been performed in [20].

Fig. 14(a) visualizes simulation result with the load current THD of the two considered power stage topologies: Regular interleaved (HB) and dual buck (DB), for different load currents with closed-loop converter operation. Note that the power semiconductor switching action is assumed ideal in order to reduce the model complexity. Consequently, the indicated THD values are not directly comparable to measurements. However, they do reflect the influence of the $R_{DS,on}$-variation on THD.

It shows that the fluctuation of the junction temperature and the resulting change in $R_{DS,on}$ has only a negligible effect on

the distortion of the closed-loop converter system, even at high load currents and with the dual buck topology, which causes a significantly larger variation in $R_{DS,on}$, as shown in Section III-B. The thermal influence on THD manifest only when the closed-loop control system is not utilized, as Fig. 14(b) illustrates. However, in order to visualize the miniscule effects on THD during open-loop operation at all, the dead time is reduced to 10 ns in the simulation.

It can be concluded that the thermal dependency of the $R_{DS,on}$ does not significantly contribute to the output THD of a wide-bandgap, switch-mode power amplifier, even during open-loop operation, as other nonlinearities, most notably dead time, are source of more prominent distortion components.

IV. Distortion Due to Dead Time

It is well-known that half-bridge interlock/dead time is a significant source of distortion in Class-D power amplifiers or DC/AC inverters [21], [22]. Consequently, this section demonstrates the amplifier's THD sensitivity to dead time and presents three methods that can be employed to significantly reduce dead time related distortion.

Fig. 15 briefly illustrates the nonlinear mechanism in half-bridges with dead time. The shape and time instants of the switched half-bridge output voltage transitions in u_{SN} depend on the instantaneous magnitude and polarity of the half-bridge current i_{HB}, which is proportional to the load current and consequently, due to this load current dependent switch-node voltage behavior, indicated with the colored areas, harmonic distortion is introduced.

In the illustrated example, the first switching action undergoes a hard-switched transition whereas the second one is either fully soft or achieves partial soft-switching, which depends on the instantaneous value of i_{HB}, the power tran-sistor parasitic capacitances, the DC-link voltage (due to the nonlinear transistor capacitances), as well as other parasitic circuit capacitances, e.g., the load capacitance [45].

Using the demonstrator system, the effect of dead time on the amplifier output current distortion is experimentally investigated. Fig. 16 illustrates the THD for different dead times as a function of the load current amplitude of the 10 Ω + 100 µH load. As expected, dead time only affects odd harmonics, as the half-bridge output waveform error is a function of the current polarity, which renders it half-wave symmetrical. The amplitudes of the even harmonics are constant and independent of dead time, as the logarithmic fit matches well. The odd-order harmonics, which dominate the THD, depend significantly on dead time, which corroborates the expected high sensitivity to this cause of distortion. In the following, three methods are presented that ameliorate the distortion caused by dead time.

A. Dead Time Minimization

The first approach to increase the amplifier linearity is to simply reduce dead time as much as possible. As Fig. 16 illustrates, 30 ns of dead time result in a THD of ≈ −100 dB

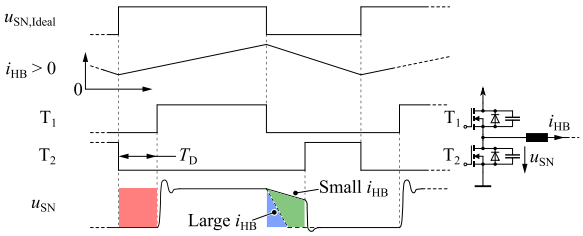

Fig. 15. Time-domain waveforms illustrating the cause of dead time related distortion in a half-bridge configuration. Depending on the magnitude and polarity of the half-bridge current i_{HB}, the switch-node voltage u_{SN} deviates from the ideal shape, as indicated with the colored areas. Note that the low-frequency waveform of i_{HB} is not visible during one PWM cycle as illustrated here, where the behavior during a time interval with $i_{HB} > 0$ is exemplarily chosen.

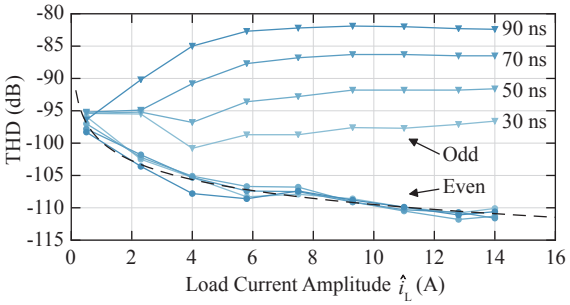

Fig. 16. Measured THD for different dead times as indicated. Load: 10 Ω + 100 µH. Odd harmonics: 3, 5, 7, 9. Even harmonics: 2, 4, 6, 8. The THD considering the even harmonics follows a logarithmic fit (dashed). f_F = 35 Hz, u_{DC} = 400 V, f_{PWM} = 200 kHz.

over a wide load current range. Such low dead times are facilitated by the fast half-bridge switching transitions, which take less than 6 ns at a DC-link voltage of 400 V [23]. As the high-side half-bridge power transistor requires an isolated gate control signal, the propagation delay difference (skew) of the two half-bridge gate control signal paths (and the variation of this timing difference, e.g., due to temperature), which is mostly dominated by the digital signal isolators, imposes a practical lower limit to dead time, as it must be guaranteed that a minimum dead time is always ensured to prevent half-bridge shoot-through. With current digital signal isolators and gate drivers, the lower dead time limit is ≈ 30 ns to 60 ns [46]. Another option to further reduce dead time is given by special gate drivers that couple the two gate voltages and make sure that always only one transistor is conducting, while minimizing dead time at the same time [47]. However, this approach increases circuit complexity and affects the gate loop parasitic inductance, which, due to the fast switch-node transitions of the half-bridges and the low GaN HEMT gate threshold voltages, could lead to parasitic transistor turn-on [23]. Other approaches supervise the conduction state of a transistor and communicate it to the complementary gate driver that can then control the switching state accordingly [48], [49]. This method also requires more circuit elements and a fast communication channel to the isolated gate driver, which also has to be robust against fast common-mode transients.

Therefore, in the following, the second method to reduce

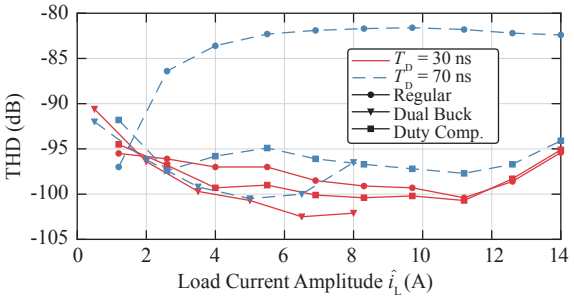

Fig. 17. Measured THD improvement using the dual buck topology and the duty cycle compensation method to reduce dead time related distortion. Load: 10 Ω +100 µH. u_{DC} = 400 V, f_{PWM} = 100 kHz, f_F = 35 Hz. I_B = 5.5 A for the dual buck topology.

dead time related distortion, based on a different power stage topology (the dual buck), as well as its effect on THD, is presented.

B. Dual Buck Topology

As the demonstrator system supports the dual buck topology (see Section II-B), its effect on the load current THD can be investigated. Fig. 17 illustrates the results. By introducing the bias current (I_B = 5.5 A), the THD can be significantly lowered, especially when the dead time is long. With shorter dead times, the linearizing effect of the dual buck topology is less pronounced, as the related distortion is already reduced. Unfavorably, the allowable load current amplitude is severely limited when operating the dual buck topology, which is due to the increased losses in the half-bridge transistors caused by the required bias current (see Section III-B). The inherently high losses of the dual buck topology could be lowered by dynamically adapting I_B during converter operation to the momentarily occurring load current amplitudes, while still maintaining an acceptable distortion performance.

However, to circumvent the significantly higher losses and reduced load current capabilities of the dual buck, a feedforward compensation scheme is presented in the following.

C. Duty Cycle Compensation

Different methods to reduce dead time induced distortion by means of a feedback or feedforward system have been presented [33], [50]–[54]. However, in the presented amplifier system, an advanced dead time compensation method can be employed, due to the availability of all half-bridge current and voltage measurements, and a high-performance digital processor. Its key feature is the continuous calculation of the faulty voltage-time areas introduced by dead time (cf. the colored areas in Fig. 15). The duty cycle of each half-bridge is then corrected such that the desired voltage-time area is applied to the half-bridge inductor, hereby reducing distortion caused by the dead time intervals. To further enhance the performance, the half-bridge current ripple is also calculated and considered. Fig. 18 illustrates the algorithm.

To model the half-bridge switching behavior, especially with

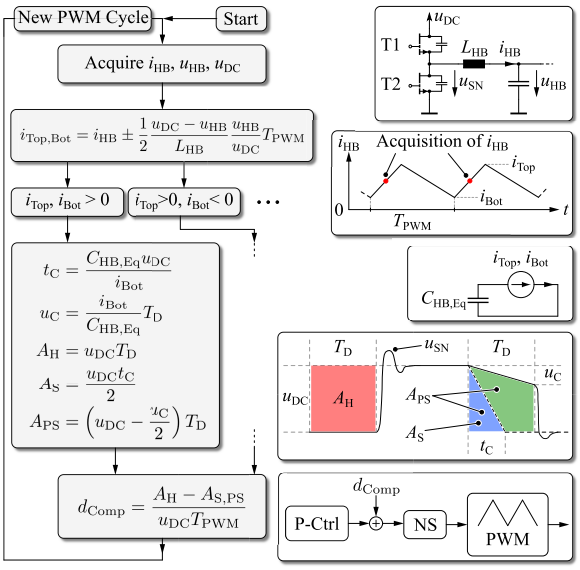

Fig. 18. Dead time compensation algorithm. The voltage-time area deviations caused by dead time are calculated and the reference duty cycle, provided by the half-bridge P-current controller, is corrected with d_{Comp}. Note that the algorithm is shown for $i_{Top,Bot} > 0$. For the other cases, the method works accordingly. The algorithm is not necessarily executed every PWM cycle as the calculation can take more than one cycle. NS: Noise shaper, for high-resolution PWM generation, see [34].

respect to the soft- and/or partially soft-switched transitions, resulting in the voltage-time areas A_S and A_{PS}, the algorithm assumes a (linear) equivalent half-bridge capacitance $C_{HB,Eq}$, comprising the parasitic power transistor capacitances C_{oss}, as well as the parasitic capacitances in the PCB layout and the half-bridge inductor. During the switching transition, it is assumed that $C_{HB,Eq}$ is charged/discharged by a constant current, which, due to the large energy storage provided by L_{HB} compared to the energies stored in $C_{HB,Eq}$, is valid for a wide current range [45]. Consequently, the soft-switched transition times of the switch-node voltage u_{SN} are easily calculated as shown in Fig. 18. The value of $C_{HB,Eq}$ can be tuned during converter operation such that the THD is minimized. Due to the nonlinearity of the power transistor parasitic capacitances, the value for $C_{HB,Eq}$ depends on the DC-link voltage. In the demonstrator system, this value ranges from ≈ 300 pF to 400 pF (200 V to 400 V).

The algorithm is executed regularly and synchronously with the converter switching frequency, at a rate of 50 kHz, which is limited by the capability of the digital signal processor. Its effects on the load current THD are also shown in Fig. 17. If the system operates with T_D = 70 ns, the benefits of the presented method are clearly visible, and it reaches THD levels close to what the dual buck topology can achieve, with the added benefit that the allowable load current is not limited, as the converter losses are not affected by the compensation method.

However, the dual buck topology still achieves a slightly better performance, which is mainly attributable to the fact that a linear equivalent capacitance is used to model the switching behavior, whereas the shape of the half-bridge voltage transitions is determined by the highly nonlinear power transistor ca-

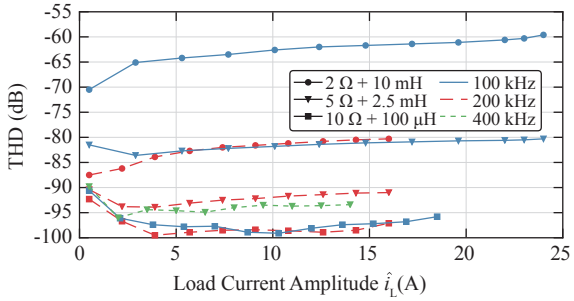

Fig. 19. Measured THD of three different loads for control system execution frequencies of 100 kHz, 200 kHz and 400 kHz. f_F : 35 Hz. u_{DC} = 400 V. PWM frequencies are 100 kHz and 200 kHz, whereas the 400 kHz control system rate is achieved by updating the reference twice per PWM period. Load currents are limited by the power transistor losses and/or the load resistor dissipation capabilities.

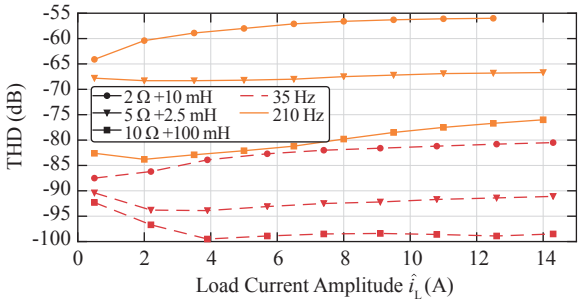

Fig. 20. THD measurements at an increased fundamental load current frequency f_F = 210 Hz. The 35 Hz measurements are the results with the 200 kHz execution rate, as presented in Fig. 19.

pacitances. Additionally, the assumption of a constant current during the half-bridge transition to charge/discharge the capacitances also breaks down at small current amplitudes [45]. Furthermore, the actual dead time can also be slightly different from what the algorithm assumes, due to propagation delay skews between different gate signal paths (see Section IV-A). The algorithm could also be implemented based on a static lookup table, which would obviate the real-time calculation of the correction factors during converter operation.

V. Control System Performance

The feedback control system is a key system component that affects the amplifier linearity considerably, as it suppresses undesired disturbances caused by nonlinear elements such as half-bridge dead time or saturating inductors [30], [31]. The structure of the demonstrator feedback system is described in Section II-C. As outlined, the power converter switching frequency, which is identical to the execution rate of the digital control system, directly affects the disturbance rejection performance of the feedback controllers. This is demonstrated in the following with measurements.

Fig. 19 illustrates measured load current THD figures for the three considered configurations, and different PWM frequencies. As expected, the THD is significantly reduced at higher controller execution rates. This especially applies to the load configurations that utilize the 2.5 mH or 10 mH iron core inductors (cf. Section II), as they are more nonlinear (i.e., they show a more current-dependent inductance variation) than the 100 µH gapped ferrite core inductor. The inductor nonlinearity manifests itself as a disturbance to the control system, which is rejected more effectively with higher control gains, and consequently, higher PWM and controller execution frequencies.

In order to double the control system execution rate, asymmetric regular sampling, where the modulator reference is updated twice per PWM cycle, can also be employed [33]. Note that this reduces the effectiveness of the digital noise shaper significantly and is hence not a preferred operating mode [34]. Nonetheless, Fig. 19 also illustrates the controller performance with asymmetric regular sampling, which results in a control system execution frequency of 400 kHz. However, THD is not significantly improved anymore. This is due to the digital implementation of the controllers in the FPGA fabric as logic circuits based on fixed-point arithmetic to enable high execution rates. Specifically, the type-III load current controller is modeled using an IIR filter which implements this controller's transfer function. As the clock frequency of the FPGA design is set to 200 MHz (again, to achieve short computation times), it prevents the usage of com-plex (i.e., wide bit-widths) multipliers and adders in order to achieve timing closure. Consequently, for high-gain controller implementations, internal signals can saturate and/or overflow, which subsequently renders the controllers unstable. Due to the implementation as an IIR filter, it is also difficult to implement stabilizing structures, such as anti-windup elements, which can further decrease the stability. Consequently, the controller gain has to be reduced in order to render it stable and hence, the control performance cannot increase arbitrarily.

A reduction in control performance is also observed at higher load current fundamental frequencies, as Fig. 20 reveals for f_F = 210 Hz, which is compared to the 35 Hz, 200 kHz measurements from Fig. 19. The deterioration of the THD figures is due to the reduction of open-loop gain at higher frequencies, as illustrated in Fig. 8. This must be considered for amplifier systems that operate with elevated fundamental output frequencies. If necessary, the gains of the feedback controllers must be increased, e.g., by reducing the delay of the pulse-width modulator or the feedback sensors.

The measurements reveal a high sensitivity of the load current distortion to the control system's open-loop gain, which, due to digital implementation limits, cannot be arbitrarily increased. The necessity for linear loads, which otherwise introduce additional undesired distortion, is also demonstrated.

A. Kalman Filter

As introduced in Section II, a Kalman estimator can be used to reduce noise in the acquired signals. This reduces the load current noise significantly due to the inherently high sensor noise sensitivity of closed-loop feedback control systems [31]. Details of the implementation and noise measurements are not scope of this paper. However, in the following, it is shown how

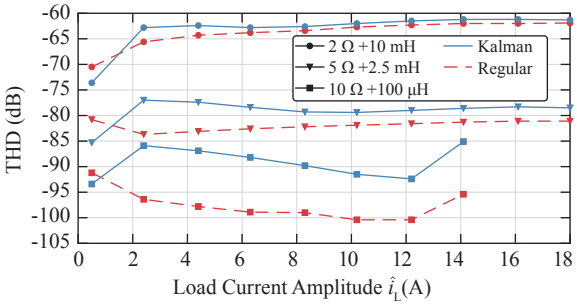

Fig. 21. Measured effect of the Kalman filter on THD. The trade-off between noise filtering and deterioration of THD is a tuning parameter of the Kalman filter. The sudden increase of THD at high load currents with the 10 Ω load is due to the DC supply output current limit. u_{DC} = 400 V, f_{PWM} = 100 kHz, f_F = 35 Hz.

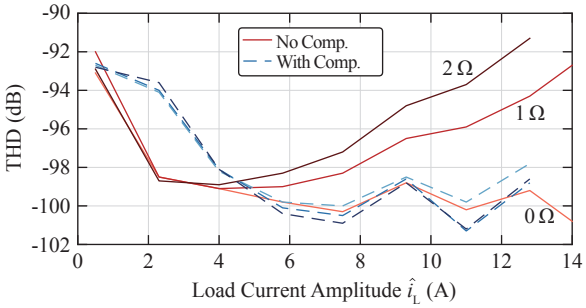

Fig. 22. Measured influence of an (ohmic) series impedance of the DC supply on the THD. Measuring the varying DC-link voltage and compensating the half-bridge duty cycles accordingly improves the THD. u_{DC} = 200 V, f_{PWM} = 200 kHz, f_F = 35 Hz. Load: 10 Ω + 100 µH.

the converter linearity is affected.

The employed Kalman filter utilizes a linear system model of the converter and the load, in order to estimate the true values of its voltages and currents (i.e., without the measurement noise) [35]. The Kalman filter provides a tuning parameter (the Kalman gain) that weights its predictions, which are based on its linear model, against the measurements, in order to produce a new estimate of the system states. If the filter prediction is weighted more, sensor noise is effectively attenuated, since less emphasis is put on the measurements to create the new estimates. On the other hand, by weighting the measurements more than the output from the linear model, the estimates become more noisy. As a linear system model is used to create the filter predictions, nonlinearities, such as current-dependent inductances or thermal coefficients of load resistors, cannot be modeled and hence, the filter predictions do not contain corresponding harmonic distortion components. Consequently, if the Kalman gain is tuned with emphasis on the predictions, harmonics, like noise, are attenuated in the filter estimates, as the linear model allows for neither. This has the adverse effect that the actual harmonics present in the output current are then not supplied to the feedback controllers and thus, the load current THD deteriorates. The Kalman gain can be tuned to influence this trade-off between reduction in load current noise and allowable deterioration of THD [35].

Measurements shown in Fig. 21 illustrate this effect. With the Kalman filter enabled, the THD degrades, while at the same time, the load current noise is significantly reduced (not shown). Due to the high-performance processing system, the Kalman filter can be executed at a rate of 100 kHz, which is thus used as f_{PWM} in this measurement.

The THD could potentially be improved by employing a Kalman system model that incorporates the nonlinearities of the physical system (e.g., current-dependent inductances). However, this requires an accurate model of the nonlinearities and potentially increases the computation time, with the result of decreasing the achievable controller execution rate, which affects THD adversely as shown earlier in this section.

VI. DC Supply Impedance and Compensation

The supply voltage is a potential source of undesired signal components in the power converter output, as it directly affects the switched half-bridge voltages during the turn-on intervals of the high-side transistors. Open-loop Class-D amplifiers in principle have an insufficient power supply rejection and/or limited applicability for precision applications [21], [22]. If the power converter drives a bridge-tied load, as it is the case with the demonstrator system, where the load is connected between two converter phases (see Fig. 6), the load voltage, for the steady-state case and averaged over a switching period, is given as

$$u_L = u_1 - u_2 = u_{DC}\,(d_1 - d_2)\,, \tag{4}$$

whereas $d_{1,2}$ are the half-bridge duty cycles of the two phases (assuming regular interleaved operation). Thus, as u_L is a function of u_{DC}, and $d_1 \neq d_2$ due to the bridge-tied load, the sensitivity to variations in the DC supply is high. Although this sensitivity is significantly reduced by the feedback controllers, if the DC-link voltage variation correlates to the converter output current, harmonic distortion can be introduced. This is, e.g., the case with a single-phase AC load that is characterized by a fluctuating instantaneous power and hence, an accordingly varying amplifier input current. The DC power supply, which usually has a given output series impedance $Z_s \neq 0$ and a limited disturbance rejection, cannot maintain its voltage output and hence, the DC-link voltage varies correspondingly. This variation is usually less than several volts and is finally attenuated by the closed-loop control system, but has to be considered for low-distortion power converters.

In the demonstrator system, the required half-bridge duty cycle d is normally calculated from the P-current controller output, which is the requested half-bridge voltage u^*_{HB} (cf. Fig. 6), by assuming a constant DC-link voltage value: $d = u^*_{HB}/u_{DC,Const}$. However, since the system is capable of measuring u_{DC} during operation, the variation in u_{DC} can be taken into account: $d = u^*_{HB}/u_{DC,\,Meas}(t)$. Such supply feedforward methods are also applied in audio amplifiers [55], at the disadvantage of requiring an additional voltage sensor.

The sensitivity of the load current THD to the DC supply series output resistance is investigated with the measurements shown in Fig. 22, both with and without the mentioned duty

cycle compensation. It is evident that a DC supply series impedance deteriorates the load current THD, especially at high current amplitudes, and despite the usage of closed-loop feedback control. However, when utilizing the feedforward compensation method, the THD is not affected by the varying supply voltage. The feedforward compensation approach is also effective at attenuating other undesired signal components from the DC-link voltage, which are potentially originating from the supply. Note that in Fig. 22, at low currents, the THD seems deteriorated by the usage of the feedforward compensation method. This is an artifact, as the measurement of u_{DC} introduces noise to the duty cycle (through the noise of the DC-link voltage and its measurement), which consequently increases the load current noise. This masks some harmonics with noise and renders the THD measurement inaccurate at low load currents. A low-pass filter could reject some noise from the DC supply voltage measurement and reduce this effect. Nonetheless, a disadvantage of this compensation method is revealed, as it potentially increases the load current noise (whose analysis is the scope of future work).

VII. Conclusion

Important system parameters of high-power switch-mode amplifiers that significantly influence their linearity and hence, total harmonic distortion (THD), are presented, analyzed and directly compared in order to identify critical design aspects. The findings are relevant for precision switch-mode power converters used to provide ultra-low-noise and low-distortion output voltages or currents, which are often required in different nanoscale positioning applications in the semiconductor manufacturing industry.

A 400 V amplifier prototype based on gallium nitride (GaN) power transistors and a cascaded feedback control system that uses low-distortion sensors, is utilized for investigations. Several methods and approaches are demonstrated. Load current THD values of less than −100 dB, or 0.001%, are achieved.

A detailed loss model of the converter system is used to determine the achievable load current amplitudes of the demonstrator system, which are limited by the power dissipation of the GaN transistors. In conjunction with a circuit simulation, it is revealed that the thermal modulation of the power transistor on-state resistances does not significantly contribute to distortion of the amplifier load current.

Dead time, which is inherently required in many switch-mode conversion systems, significantly increases load current distortion as it introduces a modulated voltage error at the switched half-bridge outputs. The detrimental effect of dead time on THD is demonstrated with detailed measurements. Three methods to reduce the influence of dead time on load current THD are exhibited. The first method aims at simply reducing the dead time, which is facilitated by the use of fast-switching GaN power transistors. A dead time of 30 ns is finally achieved and bounded only by propagation delay skews and tolerances in gate drivers and signal isolators. Another option to reduce such distortion is given by the interleaved dual buck power stage topology, which, by using a circulating bias current between two half-bridges, leads to unidirectional half-bridge currents. THD values of −102.5 dB are achieved, at the disadvantage of significantly increased losses and thus, a reduced load current range of the amplifier. Consequently, the third method employs a software algorithm which computes the dead time related error during converter operation and adjusts the half-bridge duty cycles accordingly. This method does not suffer from increased losses and shows a similarly high performance than the dual buck topology.

The importance of the feedback control system is also demonstrated. By increasing the power converter switching frequency, time delay in the control system plants can be reduced and consequently, the achievable open-loop gains of the feedback controllers can be increased, which effectively attenuates distortion components in the converter output signal. This also corroborates the need for low-loss GaN transistors that are capable of operating at elevated switching frequencies, despite high voltage/power levels (200 kHz at 400 V in the demonstrator system). A Kalman filter, which is effective at reducing sensor noise, can also be deployed. However, due to its linear system model, it attenuates distortion components in its estimates and hence, the THD of the controlled current deteriorates. Nonetheless, the Kalman filter provides a method to influence this behavior.

Finally, a method of rejecting disturbance and variation of the DC-link voltage is presented, as there is no ideal DC supply that could provide an ideally stable output voltage for the amplifier. The consequences of different DC supply impedances on the load current THD, and the effectiveness of the compensation method, are exhibited.

A. Outlook

As the amplifier's key system components have been optimized to reduce distortion, the residual converter nonlinearity is mainly caused by external sources such as the DC supply or passive components like nonlinear filter or load inductors, or load resistors. In order to further improve the converter THD, several methods are considered.

First, the control system open-loop gains could be increased by using higher PWM frequencies, as shown in Section V. This, however, raises switching losses and reduces the available load current range of the amplifier (see Section III-B). Furthermore, the digital implementation of high-gain controllers requires great care and capable digital hardware in order to prevent numerical saturation or overflow effects. Approaches based on model predictive control are considered to be computationally too exhaustive, even with modern embedded processors [56].

Another option to increase the converter linearity would be the usage of a highly stable, low-impedance DC supply in order to provide a constant DC-link voltage for the main amplifier. Its control system could also be integrated with the amplifier to make use of feedforward compensation to further improves the supply's tracking performance.

Last, the THD could potentially be further reduced by adding distinct, low-power, high-frequency switch-mode con-version stages that could operate with high open-loop gains and thus

correct the residual errors of the load current/voltage.These auxiliary converter(s) could be, e.g., connected in series or parallel to the load, the DC-link, or the half-bridge filter capacitors [57]–[59]. However, this essentially creates a hybrid switch-mode converter system with an increased system com-plexity and development cost, which obviates the advantages of a single-stage power converter.

As mentioned in Section II, the low-distortion sensor system for the load current has an intrinsic THD limit of ≈ -110 dB, which is primarily caused by the operational amplifiers of its analog front-end. This restriction could be overcome by reducing the filter complexity by, e.g., increasing the ADC sampling rate [36].

In conclusion, this paper demonstrates and measures important influence factors that affect distortion in ultra-high precision switch-mode power converters. Various effective countermeasures, which enable unprecedented distortion levels at high output powers, are presented. This permits the usage of switch-mode power amplifiers in domains previously occupied by inefficient, relatively complex and power-limited linear or hybrid systems.

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Noise Minimization for Ultra-High SNR Class-D Power Amplifiers

Mario Mauerer and Johann W. Kolar

***Abstract*—Important noise sources affecting power output waveforms of digitally controlled switch-mode (Class-D) converters/amplifiers are investigated with a 400 V hardware demonstrator utilizing gallium nitride (GaN) power transistors. First, the influence of the open-loop gains of the cascaded feedback control system on the load current signal-to-noise ratio (SNR), which is a key metric in low-noise, nanometer-precision mechatronic positioning applications, is demonstrated. With a PWM frequency of 200 kHz, the high achievable controller gains enable unprecedented SNR values in excess of 105 dB (DC–10 kHz). Next, it is shown how a real-time Kalman filter, calculated at a rate of 100 kHz and used to attenuate sensor noise, increases the amplifier output SNR by more than 10 dB. Furthermore, digital delta-sigma (noise shaping) modulation improves the SNR by 5 dB, while not affecting distortion.**

***Index Terms*—Delta-sigma modulation, feedback control, Kalman filter, low noise, power amplifier, pulse-width modulation, signal-to-noise ratio (SNR), wide-bandgap semiconductors.**

I. Introduction

POWER amplifiers are universally employed in applications such as high-frequency mobile base stations, consumer audio or magnetic resonance imaging systems, with output power levels covering more than six orders of magnitude. This work investigates low-noise (microampere), high-power (kilowatt) amplifiers indispensable for industrial nanoscale positioning applications, where the amplifiers are embodied as power electronics converters that provide amplified output waveforms which should follow the corresponding reference signals with minimum deviation and should show a very low noise level in wide frequency ranges.

The considered amplifiers generate well-controlled output currents that produce torques and forces in different types of electromagnetic actuators such as magnetic bearings or single-/three-phase permanent magnet motors. Vibration isolation systems, for example, are often used to decouple sensitive positioning stages from ground vibrations caused by nearby equipment or geologic activity [1], [2]. Consequently, their actuators require current signals of extremely low noise in order to prevent the generation of undesired movements. Positioning stages used for lithography scanners or back-end processes in integrated circuit manufacturing often feature magnetic or air bearings, whose key characteristics are low friction and damping [3]–[6]. Consequently, the noise requirements for the driving amplifiers are critical in a frequency range from DC to ≈ 10 kHz, as the mechanical stages typically provide little attenuation in the transfer functions from actuator currents to positioning stage accelerations in this bandwidth. Besides very low-noise, amplifiers in lithography systems also have to provide high output powers and dynamics to enable fast accelerations of the motion stages in order to sustain high production throughput rates and large wafer diameters [7]. Due to integrated semiconductor features that continuously shrink in size and grow in complexity, actuator load current dynamic ranges in excess of 90 dB are expected, with signal-to-noise ratio (SNR) requirements in excess of 100 dB [8], [9].

Traditionally, linear amplifiers, which are commonly based on power operational amplifiers or discrete devices, are preferred for these tasks due to their inherently low noise over wide frequency ranges, combined with low output impedances [10]. Noise and linearity can be further improved with closed-loop feedback systems that can be implemented in the analog or digital domain, whereas the former also features intrinsic low noise due to the absence of (digital) amplitude quantization [11], [12]. However, linear amplifiers collectively suffer from limited efficiencies and limited output power levels. Hybrid amplifiers strive to alleviate these restrictions by combining linear amplifiers with high-power, efficient switch-mode converters [13], [14]. Nonetheless, such topologies increase the complexity of the electrical circuit and, if utilized, the feedback control system, as the fundamentally different characteristics of the linear and switched conversion stages, with respect to their dynamics and input/output impedances, have to be analyzed and stabilized individually, which increases development effort and cost.

Therefore, this work analyzes key influence factors on the output noise of digitally controlled, pulse-width modulated (PWM) switch-mode power amplifiers/converters. The analysis is similar to the one conducted in [15], which focuses on distortion and utilizes the same hardware demonstrator system to provide verification measurements as in this work. Fig. 1 lists important sources of noise in such converters. Due to the intended application in mechatronic positioning systems, the amplifier output current noise is considered, as the generated electromagnetic actuator forces are proportional to current. Nonetheless, the presented insights are universally applicable to amplifiers that provide either a controlled current or a controlled output voltage. Throughout this work, the term noise encompasses all undesired signal components, except for

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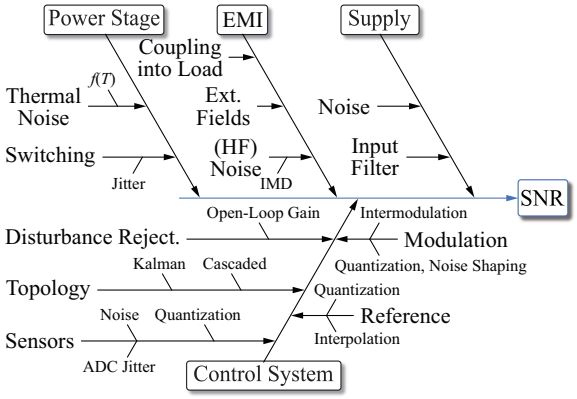

Fig. 1. Nonidealities of system components influencing the signal-to-noise ratio (SNR) of the output quantities of digitally controlled switch-mode power amplifiers.

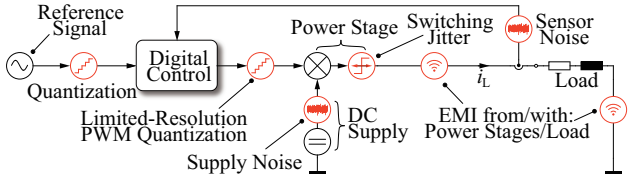

Fig. 2. Amplifier noise sources can be modeled as series-connected voltage/signal sources. Reference signal quantization noise is effectively eliminated with digital signals of sufficient resolution (> 30 bit). Electromagnetic interference (EMI) within the amplifier itself (e.g., from other switching stages or auxiliary DC/DC regulators) is rejected with shielding and proper PCB layout techniques.

harmonics in AC output signals (that are caused by amplifier nonlinearities). Thus, signals with spectral components at 50 Hz, e.g., due to electromagnetic interference (EMI) originating from the power grid, are also accounted to the noise power [16].

Fig. 2 outlines key noise sources in the context of a switch-mode power amplifier, modeled as series-connected voltage or (digital) signal sources. The quantization noise introduced by the limited-resolution PWM [17], as well as the time-domain jitter of the power transistor switching actions [18], are linked to stochastic processes and thus introduce wideband noise of uniform power density [19]. Supply noise, or electromagnetic interference (EMI) from external sources by means of stray fields that couple to the amplifier's circuit, on the other hand, often exhibit spectral components at distinct frequencies. Due to nonlinear elements within the amplifier, such as half-bridges with dead time or saturating inductors, these frequency components can undergo intermodulation distortion, which results in noise signals at lower frequencies [20], [21]. Therefore, it is important to also consider noise sources outside the frequency band of interest (DC to 10 kHz in this work), as their intermodulation products can appear in sensitive frequency ranges. In this work, it is demonstrated to what amount the mentioned noise sources influence the SNR of the load current, which is an important quality measure for low-noise amplifiers. Note that fundamental output load current frequencies of amplifiers in mechatronic motion systems range from DC to ≈ 200 Hz.

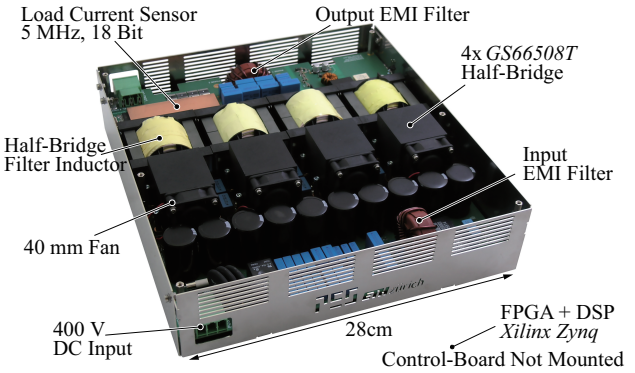

Fig. 3. Hardware demonstrator featuring four *GaN Systems GS66508T* half-bridges (650 V, 30 A) and high-resolution current/voltage ADC systems. The max. DC-link voltage is 400 V. The system is designed for supplying a single-phase inductive-resistive load with a maximum current amplitude of 25 A. The control board is mounted on top (not shown) and features a high-performance FPGA and DSP to implement complex control structures such as Kalman filters.

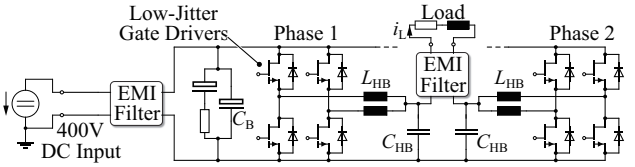

Fig. 4. Power circuit topology of the hardware demonstrator. The bridge-tied, single-phase load is supplied by two interleaved half-bridges, which can implement two power stage topologies, namely the regular interleaving of two half-bridges and the dual-buck topology. EMI filters ensure compliance with corresponding standards and reduce EMI for sensitive nearby equipment of the positioning systems. L_{HB} = 700 µH, C_{HB} = 12 µF.

To conduct this analysis, a hardware demonstrator, illustrated in Fig. 3, is employed. It features four interleaved half-bridges based on 650 V enhancement-mode, high-electron-mobility gallium nitride (GaN) power transistors (*GaN Systems, GS66508T*), which enables the system to deliver up to 25 A (peak) to a bridge-tied, single-phase load. The nominal DC-link voltage is 400 V and the PWM pulse repetition frequency f_{PWM} is $\leqslant$ 200 kHz, limited by transistor switching losses. The converter's power circuit topology is depicted in Fig. 4. Further details of this system are given in [15], which focuses on the output distortion of the amplifier.

To eliminate time-domain jitter from the half-bridge switching transitions, which is a considerable source of wideband noise, low-jitter gate drivers, as presented in [18], are used to drive all power transistors. The output noise of the limited-resolution pulse-width modulators, which are a considerable source of wideband noise, is reduced with digital delta-sigma modulators/noise shapers (NS), which can shift the PWM quantization noise to higher frequencies, as shown in [17] and in Section IV-A below.

The interleaved half-bridges enable the implementation of two distinct power stages, namely the regular interleaved half-bridge arrangement and the dual buck topology, whereas the latter is not subject to distortion related to half-bridge interlock (dead time) intervals, as demonstrated in [15], which also provides details of the demonstrator's closed-loop feedback

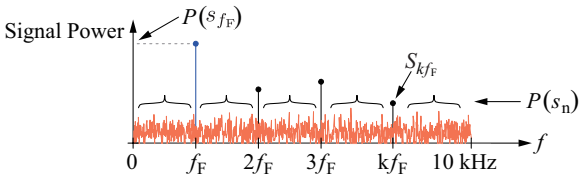

Fig. 5. Noise power considered for the SNR excludes the power of the signal at the fundamental frequency f_F and its harmonics. The frequency band from DC to 10 kHz is critical for mechatronic motion systems.

control system.

To increase the control system's flexibility and to de-couple the cascaded control loops dynamically, each system state, i.e., the four half-bridge currents, the two phase voltages and the load current, are measured. As shown in this work, sensor noise critically affects the control system and hence, low-noise voltage and current sensors are used, featuring 16-bit analog-to-digital converters (ADCs) that operate without anti-aliasing filters (for increased control system bandwidth) and synchronously with the converter's switching actions, in conjunction with optimized signal processing circuits (filters/amplifiers) [22]. The load current sensor employs an 18-bit ADC with an anti-aliasing filter (it samples asynchronously to the converter's switching instants) and a sampling rate of 5 MHz to make use of oversampling, which reduces ADC quantization noise [22]. Further details of the sensor systems are given in [15]. An FPGA is well-suited to acquire and process the high-speed, high-resolution data streams from the individual ADCs, which results in an overall data rate of 112 Mbit s^{-1} when operating with $f_{PWM} = 200$ kHz. However, some control tasks, like a Kalman filter, are implemented with low complexity as a floating-point accurate, procedural program. Consequently, the converter's processing system features a *Xilinx Zynq Z-7020*, which combines an FPGA with two 666 MHz *ARM Cortex-A9* CPUs and high-performance floating-point units [23].

For the calculation of the load current SNR, the noise of the current signal is considered from DC to 10 kHz, as this frequency range is critical for precision positioning applications:

$$SNR = 10 \log_{10} \frac{P(s_{f_F})}{P(s_n)}, \tag{1}$$

where $P(s_{f_F})$ is the power of the desired amplifier output signal component s_{f_F} with fundamental frequency f_F (assuming a sinusoidal signal), and $P(s_n)$ is the power of the noise in a frequency range from DC to 10 kHz, which considers the power of all signal components in this bandwidth, except the power of the fundamental component at s_{f_F} and its integer harmonics s_{kf_F}, with $k \in [1, 2, \ldots]$ [20], as shown with the following equation and Fig. 5:

$$P(s_n) = \int_{DC}^{10\,\text{kHz}} P(s)\,\mathrm{d}f - \sum_{k=1}^{\infty} P(s_{kf_F}). \tag{2}$$

As it will be demonstrated in this work, the noise power of the output signal is independent of the fundamental frequency f_F and, to a large extent, also from the amplitude of s_{f_F}.

The presented demonstrator is capable of providing a low-noise output load current i_L and consequently, an independent reference current sensor with sufficiently low inherent measurement noise is required for the acquisition of verification measurements. For this purpose, a *LEM IT 65-S* current sensor, in conjunction with a high-precision, low-noise spectrum analyzer, is used to acquire the sinusoidal amplifier output current [15], [24], [25]. This setup is capable of measuring SNR values (according to (1)) in excess of ≈ 108 dB. Amplifier output current fundamental frequencies f_F of 35 Hz and 210 Hz are used, which are similar to actuator frequencies in mechatronic positioning systems, and whose harmonics do not interfere with harmonics of the power grid, as described in [15]. The amplifier generates sinusoidal output currents, as this waveform allows the effective analysis of SNR and distortion, and is common in mechatronic motion control systems. The utilized resistive-inductive passive loads comprise high-power thick-film resistors and high-current inductors, whereas three different loads, which recreate the characteristics of different mechatronic actuators (e.g., linear motors with and without iron cores), are employed for the measurements: 2 Ω +10 mH, 5 Ω + 2.5 mH and 10 Ω +100 µH. The 100 µH inductor employs a gapped ferrite core, whereas the two other inductors are significantly larger and their cores are made from laminated silicon steel (designed for low-frequency power grid applications).

Several key contributions arise from this work. First, state-of-the-art, high-performance signal processors enable high-frequency and high-gain feedback controllers that can provide a substantial disturbance attenuation. Measurements directly compare the achievable performance, which is strongly affected by the PWM frequency. Different influence factors, such as load impedance or DC-supply noise, are highlighted, and the limits to the achievable load current SNR are demonstrated. Detailed measurements are performed to isolate the effects of different noise sources by, e.g. utilizing a battery supply. Next, a real-time Kalman filter implementation is presented in detail. Measurements demonstrate its value for precision switch-mode amplifiers, and design trade-offs are outlined. Finally, the influence of noise shaping PWM modulators on a high-gain closed-loop amplifier is demonstrated with measurements. Hence, this work provides comprehensive sensitivity analyses of amplifier subsystems with respect to noise, which facilitates future design decisions.

In the following, Section II investigates the influence of the control system's disturbance rejection capability on the amplifier's load current SNR. Next, Section III presents the effects of a Kalman filter, which reduces residual sensor noise. Section IV analyzes the noise contributions from the PWM and the noise shapers under closed-loop operation, as well as the influence on SNR when utilizing the low-distortion dual buck topology. Section V summarizes the results of this work and provides an outlook.

II. Control System

A closed-loop feedback control system is an essential con-

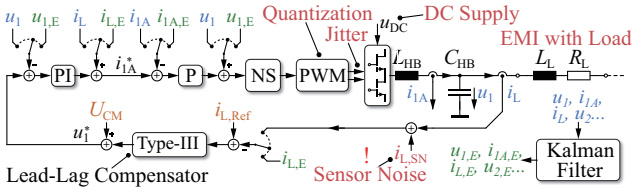

Fig. 6. Simplified diagram of the cascaded control system (second bridge leg (phase) and second half-bridge of the shown bridge leg omitted). Important sources of noise are outlined (sensor noise only shown for i_L, despite all measurements being subject to noise).

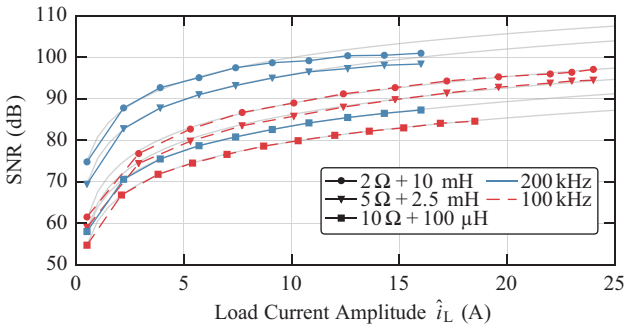

Fig. 7. SNR measured for different loads at different f_{PWM}, which correlates with the achievable disturbance rejection performance of the controllers. Kalman filter disabled (cf. Section III). At high currents and high SNR, noise from the DC supply affects SNR unfavorably. Grey lines are individual least-squares fits for each amplifier configuration with: SNR(dB) = $c_0 \ln(\hat{i}_L) + c_1$. u_{DC} = 400 V, f_F = 35 Hz.

tribution for high-performance output waveforms of any amplifier system, as it is capable of significantly rejecting and/or attenuating disturbances such as noise or harmonic distortion.

Fig. 6 illustrates the simplified block diagram of the demonstrator's decoupled, closed-loop cascaded feedback control system (redundant elements like the second phase and the interleaved half-bridge are omitted for simplicity; see [15] for more details). Dominant sources of noise are illustrated in red. Note that the sensor noise coupling is only shown for the load current measurement i_L, despite all measurements being subject to sensor noise, caused by analog filters or amplifiers, and the subsequent ADC stages [22].

The four half-bridge currents are controlled by individual proportional (P) controllers, which obtain their reference signals from the proportional-integral (PI) phase-voltage controllers. A type-III (lead-lag) compensator controls the load current i_L. All controllers are digital and implemented in the system's FPGA, and are calculated synchronously with the converter's PWM, at the same frequency. They are tuned using loop shaping, with consideration of the delays caused by the calculation times of the control algorithms and the sampling of the PWM, which reduces the phase margins of the control loops. All open-loop gains are maximized, while maintaining phase margins of 50°. More details are given in [15]. A Kalman filter (see Section III below) can be utilized to provide low-noise estimates of the sensor measurements.

Sources of noise that act on the plants of the dynamic system (e.g., the supply noise) appear as disturbances to the control system and are thus effectively attenuated with the open-loop gains of the feedback loops [26]–[28]. Harmonic distortion is also categorized as such a disturbance and the influence of the closed-loop controllers on the amplifier's linearity is discussed in [15]. This disturbance rejection is an important feature of closed-loop feedback control systems. They are thus a key contributor to low-noise and low-distortion power conversion systems. On the other hand, the control system reacts equally sensitive to sensor noise than to its reference input and consequently, it cannot be rejected by feedback control, which constitutes a fundamental disadvantage [26], [28]. This corroborates the necessity for low-noise sensors or advanced control methods, such as a Kalman filter.

Nonetheless, a high disturbance rejection is still desired to attenuate sources of noise, to linearize the amplifier and to improve its reference tracking performance. This demands high open-loop gains of all feedback loops, which are limited by their respective stability margins.

A. Load Current Noise Measurements

As mentioned above and as further discussed in [15], the control performance increases with the PWM frequency of the converter, as delays are reduced. Fig. 7 illustrates this with measurements of the amplifier's load current SNR, obtained at two different PWM switching frequencies. Due to the increased switching losses of the power transistors at higher f_{PWM}, the achievable $\hat{i}_L$ is reduced, as derived in [15]. The power dissipation capability of the 10 Ω load resistor, and the utilized DC power supply, may also limit $\hat{i}_L$ in certain measurement configurations. As expected, the control topology with the higher open-loop gains rejects noisy disturbances better and hence, SNR is improved by up to 10 dB. Naturally, load configurations with higher inductance values show less current noise due to the fact that the power amplifier operates as a voltage source, whose noise components translate to noise currents in accordance with the load impedance.

The gray lines in Fig. 7 are logarithmic least-squares fits of the SNR values of each corresponding amplifier configuration (the formula is given in the figure caption). As given by (1), the SNR exhibits a logarithmic behavior as a function of the load current, if the noise power remains constant. This is behavior of the SNR is experienced with the measurements in Fig. 7, which hence implies that the load current noise is not affected by the magnitude of $\hat{i}_L$. This is expected, as major noise sources, e.g., the PWM or gate drive signal isolation, operate independently of the output current amplitude [18]. Consequently, the achievable SNR is limited by the load current capability of the power amplifier, as the noise power remains, ideally, constant. However, at increased load currents, the SNR measurements can deviate from their predicted values (cf. the 2 Ω + 10 mH load in Fig. 7). This is attributed to the fact that noise originating from the DC laboratory power supply increases at high output powers.

The deteriorating effects of increasing DC supply noise

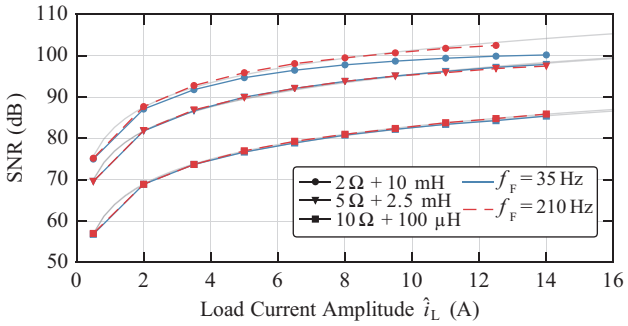

Fig. 8. SNR measured for different loads and fundamental frequencies f_F. With higher power ripple frequencies, the DC supply can provide better voltage regulation and thus, less output noise. Regular cascaded control system (Kalman filter disabled). u_{DC} = 400 V, f_{PWM} = 200 kHz.

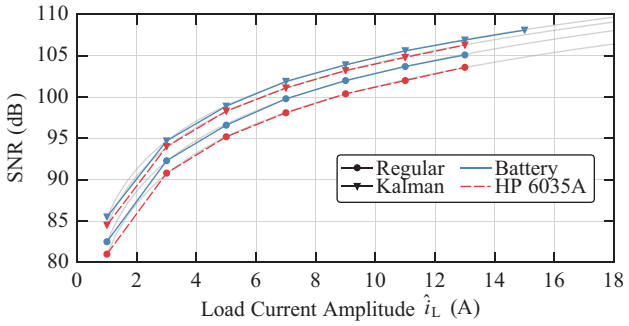

Fig. 9. Load current SNR improves with a battery supply compared to a switch-mode, high-power laboratory supply (*HP 6035A*). Regular cascaded control system executed with 200 kHz, Kalman controller executed with 100 kHz (cf. Section III). f_{PWM} = 200 kHz. u_{DC} = 75 V, f_F = 35 Hz. Load: 2 Ω + 10 mH.

is also visible in the current amplitude sweeps shown in Fig. 8, which shows similar measurements, but performed at two different fundamental load current frequencies f_F. The degrading effect on the SNR is, again, only visible with the 2 Ω +10 mH load and for f_F = 35 Hz, whereas the measurement performed with f_F = 210 Hz follows its expectation well (i.e., it does not derive from its logarithmic fit line). This distinction of load current SNR between the different fundamental frequencies is owed to the fact that the amplifier's DC-link buffer capacitors (C_B=1.8 mF in the demonstrator system) present less impedance for the single-phase load ripple current at higher f_F and consequently, it is shunted from the DC-link supply, whose output current is thus experiencing less variation. This improves its voltage regulation and hence, noise is reduced. The DC-link voltage could be measured and used in conjunction with a feedforward compensation method to mitigate the impacts of the DC-link voltage variations. However, as shown in [15], this approach can potentially introduce further noise and thus, deteriorate the SNR.

Generally, however, the SNR is independent of f_F, which is expected as the disturbance rejection of the feedback controllers is not affected by the frequency of their reference signals. This is not the case for harmonic distortion as shown in [15], as the control system provides less open-loop gain at higher frequencies, which is needed to attenuate the harmonics at integer multiples of f_F.

To further illustrate the influence of the DC supply on the load current noise, Fig. 9 shows measurements where the amplifier output SNR, when operating with a switch-mode laboratory supply, is compared to the performance with a battery supply, comprising six individual, series-connected 12 V lead-acid cells that typically feature a negligible voltage noise. For this measurement, the DC-link voltage is set to ≈ 75 V for both supply types. By eliminating the noise of the switch-mode laboratory supply, the load current SNR improves slightly and does not deteriorate at higher load currents.

These measurements emphasize the requirement for low-noise DC supply voltage sources, despite the usage of high-gain feedback controllers. Amplifier operation with single-phase loads are characterized by a large power pulsation, which aggravates the stability of the DC supply further. In case of a switch-mode supply system, a good rejection of signal components at the supply's switching frequency is also desired, as intermodulation distortion can shift such components into sensitive frequency ranges.

In the following, sensor noise, which is a critical influence factor, is largely eliminated by employing a Kalman filter.

III. Real-Time Kalman Filter

A fundamental impediment of closed-loop feedback systems is their high sensor noise sensitivity, as this noise source is essentially amplified by the (usually) high controller gains [26], [28]. Despite the low-noise voltage and current sensors in the demonstrator system [22], sensor noise can still not be neglected, as it will be shown in this section.

Generally, the Kalman filter presents an approach to provide estimates of unknown or noisy states of a dynamic system (e.g., voltage, current, position, speed etc.), given some knowledge about the dynamic system itself, and usually (noisy) measurements of some (or all) states [29]. Kalman filters, which can manifest in different implementations that are often tailored for specific applications (e.g., with linear or nonlinear dynamic system models), are commonly used in guidance or navigation. Such applications do not require high execution rates of the required calculations due to their limited dynamics. However, as shown in Section II and [15], the controller execution rate is critical for achieving amplifier output waveforms of low noise and distortion. In the discussed application, the Kalman filter is used to attenuate sensor noise and hence, it must be computed with the same rate as the feedback control system (i.e., in *real-time*), in order to provide the updated low-noise estimates of the measurements for each control cycle.

Due to their computational complexity, real-time Kalman filters in power electronic applications usually do not exceed execution rates in excess of 5 kHz to 30 kHz, which is insufficient for precision amplifiers due to the accompanying reduction of achievable control gain and/or bandwidth [30]–[34]. By implementing the Kalman algorithm using con-

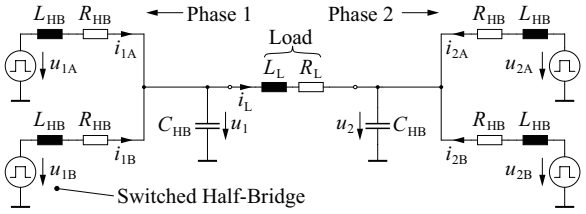

Fig. 10. Linear dynamic system model of the demonstrator system power stage used for the Kalman filter. L_{HB} = 700 µH, R_{HB} = 70 mΩ, C_{HB} = 12 µF.

figurable logic (i.e., with an FPGA), the execution rates can be increased to more than 150 kHz [35], [36]. However, this comes at the cost of a significantly increased implementation complexity and a loss of design flexibility. Consequently, this work presents a real-time Kalman filter implementation, executed as a procedural program that is calculated by a conventional processor. It is part of the demonstrator's feedback control system and it can provide low-noise estimates of the sensor data at a rate of 100 kHz, while featuring seven system states and four inputs in its underlying dynamic model, as presented in the following.

The Kalman algorithm requires a dynamic model of the physical system. In order to reduce the computational complexity, a linear model of the power amplifier system, illustrated in Fig. 10, is utilized. The switched half-bridges are modeled as controlled voltage sources to obtain a linear system. Its description, including the state vector x, the input vector u, and a vector w that models noise, can be given by

$$\dot{x} = Ax + Bu + Gw\,, \tag{3}$$

with the state and input vectors as follows:

$$x = \begin{bmatrix} i_{1A} & i_{1B} & i_{2A} & i_{2B} & i_L & u_1 & u_2 \end{bmatrix}^\top,$$
$$u = \begin{bmatrix} u_{1A} & u_{1B} & u_{2A} & u_{2B} \end{bmatrix}^\top,$$

and the system matrices as:

$$A = \begin{bmatrix} \frac{-R_{HB}}{L_{HB}} & 0 & 0 & 0 & 0 & \frac{-1}{L_{HB}} & 0 \\ 0 & \frac{-R_{HB}}{L_{HB}} & 0 & 0 & 0 & \frac{-1}{L_{HB}} & 0 \\ 0 & 0 & \frac{-R_{HB}}{L_{HB}} & 0 & 0 & 0 & \frac{-1}{L_{HB}} \\ 0 & 0 & 0 & \frac{-R_{HB}}{L_{HB}} & 0 & 0 & \frac{-1}{L_{HB}} \\ 0 & 0 & 0 & 0 & \frac{-R_L}{L_L} & \frac{1}{L_L} & \frac{-1}{L_L} \\ \frac{1}{C_{HB}} & \frac{1}{C_{HB}} & 0 & 0 & \frac{-1}{C_{HB}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{HB}} & \frac{1}{C_{HB}} & \frac{1}{C_{HB}} & 0 & 0 \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{1}{L_{HB}} & 0 & 0 & 0 \\ 0 & \frac{1}{L_{HB}} & 0 & 0 \\ 0 & 0 & \frac{1}{L_{HB}} & 0 \\ 0 & 0 & 0 & \frac{1}{L_{HB}} \\ & O_{3\times4} & & \end{bmatrix},$$

with O being the zero matrix where its indices define the number of its rows and columns. The state vector x includes all capacitor/inductor voltages and currents, and the input vector u contains the four half-bridge output voltages. In the demonstrator system, all seven states are measured by sensors and consequently, the measurement equation, including the measurement noise term v, is given by

$$y_m = Ix + v, \tag{4}$$

with I being the identity matrix. Noise is described by the process noise w, which accounts for sources of noise within the dynamic system, and measurement noise v, generated by the sensors. The noise is assumed to have a Gaussian probability distribution and a white (i.e., uniform) power spectral density. The corresponding noise covariance matrices Q and R are given as $Q = E(ww^\top)$ and $R = E(vv^\top)$, where E is the expected value.

The process noise model is based on the assumption that the four half-bridge voltages are the only sources of noise within the dynamic system (apart from the measurement noise). This is given in the demonstrator hardware, in which the quantization noise of the limited-resolution PWM, or the half-bridge switching jitter, are injecting such process noise into the plant [17]. Other sources of noise within the system, such as EMI with the load (cf. Fig. 2), are neglected due to their comparably small noise powers and often parasitic natures. Consequently, G is modeled such that the process noise only affects the four half-bridge currents:

$$G = \left[\begin{array}{c|c} I_{4\times4} & O_{4\times3} \\ \hline O_{3\times4} & O_{3\times3} \end{array}\right]. \tag{5}$$

The process noise (co)variances are modeled as

$$Q = \left[\begin{array}{cccc|c} \sigma_{HB}^2 & 0 & 0 & 0 & \\ 0 & \sigma_{HB}^2 & 0 & 0 & O_{4\times3} \\ 0 & 0 & \sigma_{HB}^2 & 0 & \\ 0 & 0 & 0 & \sigma_{HB}^2 & \\ \hline \multicolumn{4}{c|}{O_{3\times4}} & O_{3\times3} \end{array}\right], \tag{6}$$

with σ_{HB}^2 being the noise variance of the half-bridge voltages.

Similarly, the measurement noise covariance matrix is

$$R = \mathrm{diag}\left([\sigma_{i_{\mathrm{HB}}}^2 \;\; \sigma_{i_{\mathrm{HB}}}^2 \;\; \sigma_{i_{\mathrm{HB}}}^2 \;\; \sigma_{i_{\mathrm{HB}}}^2 \;\; \sigma_{i_{\mathrm{L}}}^2 \;\; \sigma_{u_{\mathrm{HB}}}^2 \;\; \sigma_{u_{\mathrm{HB}}}^2]\right), \qquad (7)$$

which incorporates the variances of the three different types of sensors (half-bridge currents, load current and phase voltages). The diagonal matrix reflects the independence of the sensor noise sources, as each sensor is a self-contained unit which cannot influence the noise of other sensors. The corresponding sensor noise standard deviations, measured during converter operation with no applied voltages or currents, are given as $\sigma_{i_{\mathrm{HB}}} = 2.0$ mA, $\sigma_{i_{\mathrm{L}}} = 83.0$ µA and $\sigma_{u_{\mathrm{HB}}} = 25.0$ mV. For each measurement, 5×10^6 samples are obtained. As shown in [22], the sensor noise levels remain constant in their operating ranges. The low value for $\sigma_{i_{\mathrm{L}}}$ reflects the effort to create a low-noise measurement for the load current i_{L} (i.e., oversampled, 18-bit ADC with optimized analog processing circuitry) [22].

Using the presented system and noise covariance matrices (i.e., *A, B, G, Q* and *R*), the Kalman filter can be designed. To reduce the required computations during converter operation and thus, to maximize the Kalman filter execution rate, a steady-state implementation of the Kalman estimation method is chosen. It is based on the assumption of constant noise covariance matrices (*Q, R*) and hence, does not require the time-consuming calculation of inverse matrices or matrix factorizations [29]. This assumption holds in the considered power converter, as sensor noise and the system's input noise sources (e.g., PWM or half-bridge switching jitter) maintain a constant and independent noise behavior during operation.

In the presented application, the Kalman filter is implemented in a sampled system and consequently, the discrete-time process noise covariance matrix is determined using Van Loan's method [29], whereas the continuous-time system description can be converted to a sampled model using common discretization methods such as zero-order hold or Tustin's method. The design process is well documented and common engineering tools can be used to effortlessly determine the optimal solution of the Kalman estimation problem [29], [37].

For the case of the considered steady-state Kalman filter, the algorithm, which provides the required low-noise measurement estimates, reduces to the calculation of a dynamic system of the following form, where the filtered measurements at each execution step *n* are given by y_e, and x_n is an internal state that is continuously updated:

$$x_n = A_k x_{n-1} + B_k \begin{bmatrix} u_{n-1} \\ y_{m,n} \end{bmatrix}, \qquad (8)$$

$$y_e = C_k x_n + D_k \begin{bmatrix} u_{n-1} \\ y_{m,n} \end{bmatrix}. \qquad (9)$$

Note that the solution of the Kalman estimation problem is embedded in the matrices A_k, B_k, C_k and D_k [37]. The

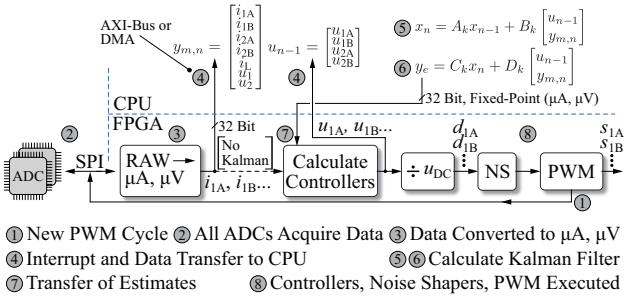

Fig. 11. Data paths for the calculation of the steady-state Kalman filter in the demonstrator system. The entire algorithm can be executed with 100 kHz (two PWM cycles if $f_{\mathrm{PWM}} = 200$ kHz). If the Kalman filter is not used, the measured data is sent directly to the feedback controllers.

vector $y_{m,n}$ contains the measurements at step *n* and u_{n-1} is the system input as applied in the previous step. The two equations contain only multiplications and additions, and no complex matrix operations such as finding an inverse. Thus, the computations can be performed in a comparably short time.

A key parameter of the Kalman filter is the *Kalman gain* [29]. Using the system model as described above, the Kalman filter algorithm calculates predictions for the true states of the dynamic system in each execution step. The Kalman gain is then used to weight these predictions relative to the measurements in order to form a weighted estimate of the system states, which in this case, is also the Kalman filter's output. Consequently, this presents a tuning opportunity. The Kalman gain is determined during the design process as optimal solution of the Kalman estimation problem, and affected by the assumed process noise standard deviation σ_{HB} (see (6)) [29], [37]. By increasing this value, the filter increases the weight on the measurements compared to the predictions from its linear model, as there is a high uncertainty in the dynamic system (i.e., increased process noise). Consequently, the noise content of the estimates increases. On the other hand, by choosing smaller values for σ_{HB}, which leads to a Kalman gain that weights the measurements less, as the filter then trusts its predictions more, noise in the estimates can be reduced. In summary, the behavior of the Kalman filter can be tuned with the noise covariance matrices, which affect the resulting Kalman gain. As shown in [15], the Kalman gain also affects the linearity of the amplifier due to the utilization of a linear system model in conjunction with a slightly nonlinear physical system. For the demonstrator system, values for σ_{HB} are experimentally determined in order to maximize the achievable SNR, while still obtaining stable Kalman filters. Values between 1 and 15 result, depending on the utilized load configuration.

Fig. 11 illustrates the implementation of the Kalman algorithm and the signal paths inside the demonstrator's *Xilinx Zynq Z-7020* processing system. At the beginning of each PWM cycle (if $f_{\mathrm{PWM}} = 100$ kHz, or every second cycle if $f_{\mathrm{PWM}} = 200$ kHz), the sensors measure all seven system states and transmit the data to the FPGA fabric, where the raw ADC measurements are rescaled to 32 bit wide fixed-point data vectors that represent the physical quantity in µA or µV, which is sufficient to cover

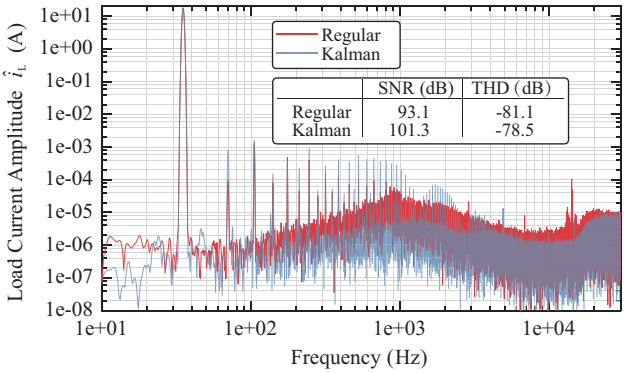

Fig. 12. Spectra of the load current obtained from the amplifier's load current sensor, with and without the use of Kalman estimates for the feedback control system. THD includes the first 9 harmonics and the SNR includes noise from DC to 10 kHz. $f_{PWM} = 100$ kHz, $u_{DC} = 400$ V, $\hat{i}_L = 18$ A, $f_F = 35$ Hz, Load: 5 Ω + 2.5 mH. FFT window: Kaiser, 38th order. Nr. of samples: 20e6. Sampling rate: 5 MHz. Kalman filter executed with 100 kHz.

the dynamic ranges of the measurements, while also providing sufficiently low quantization noise. If the Kalman filter is enabled, an interrupt is raised in the CPU and the measurements, together with the previously requested half-bridge voltages u_{n-1}, are transferred from the FPGA fabric to the cache of one of the *ARM Cortex* CPUs. Due to the small data payload (44 bytes), this transfer requires approximately the same amount of time with register-based CPU bus transfers (*AXI4-Lite*) as with a cache-coherent direct memory access. Next, the transferred data is converted to a floating-point representation and the Kalman filter algorithm is computed, using the processor's floating-point unit, according to (8) and (9). The matrices A_k, B_k, C_k and D_k are stored as floating-point arrays in the processor memory. The updated estimates y_e of the system states are then transferred back to the FPGA fabric (again, as 32-bit fixed-point numbers), where the cascaded controllers are executed using the estimates instead of the measurements. Subsequently, the delta-sigma noise shapers (NS) and pulse-width modulators are updated with the new duty cycles as requested by the control system, and the process, whose execution requires ≈ 8 µs, is complete and repeated with the start of the next PWM cycle.

Fig. 12 shows two frequency spectra of $\hat{i}_L$ to demonstrate the influence of the Kalman filter, as the only difference between the two measurements is the utilization of either the Kalman estimates or directly the measurements for the closed-loop control system. As illustrated, the Kalman filter increases the load current SNR significantly, which is also evident from the lower noise floor in the spectrum. However, as explained in [15], the Kalman filter affects THD unfavorably.

Fig. 13 illustrates the SNR improvement of the Kalman filter for the three analyzed loads, with a controller update rate of f_{PWM} = 100 kHz. As observed in Section II, at very high SNR values, the achievable performance is limited by the noise of the DC supply. Nonetheless, the SNR can be improved in excess of 10 dB by the presented steady-state Kalman filter, which only requires sufficient computational power.

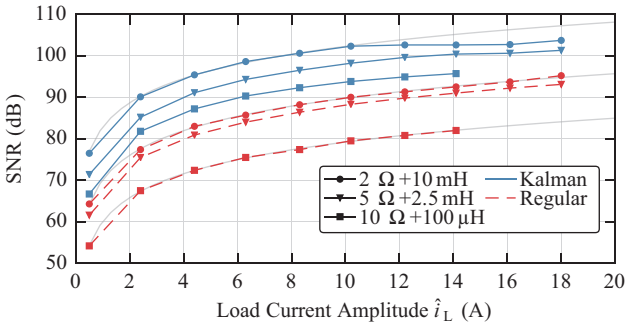

Fig. 13. Measurement of the load current SNR improvement by the Kalman filter. Deviation from fitted line at high SNR is due to DC supply noise at high powers. All controllers and Kalman filter executed with f_{PWM} = 100 kHz. $u_{DC} = 400$ V, $f_F = 35$ Hz.

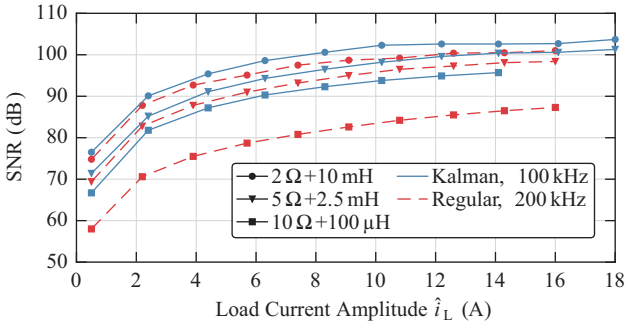

Fig. 14. Load current SNR performance comparison between the control system with the enabled Kalman algorithm, calculated at a rate of 100 kHz, and the regular controllers that use the unmodified measurements, but tuned for an execution rate of 200 kHz. The PWM frequencies correspond to the controller execution rates. This plot combines the data from Fig. 7 and Fig. 13.

However, despite employing a sophisticated processing platform, the Kalman filter execution rate is limited to 100 kHz, which is mainly caused by the time required to perform the floating-point operations for the calculation of (8) and (9). The execution time could be lowered by implementing the algorithm in the FPGA fabric as a digital design. This, however, substantially increases complexity, prolongs development times and reduces design flexibility [29].

A similar noise performance than what is achievable with an enabled Kalman algorithm can also be obtained with the regular control system, but executed with f_{PWM} = 200 kHz. This facilitates controllers with higher open-loop gains, which reduces the influence of noise sources such as the DC supply or the pulse-width modulators. Fig. 14 illustrates this by comparing the relevant measurements. If the Kalman filter would also be executed at a rate of 200 kHz, the SNR would even further improve. The Kalman filter is especially effective at improving the SNR of the 100 µH load, despite the reduced control gains. This load inductor is not subject to significant external noise due to its few winding turns and small size. Thus, sensor noise is a dominant contributor to the amplifier's overall output noise in this configuration and hence, the Kalman filter can effectively reduce this noise source. Higher control gains can only marginally improve the SNR of this load, as sensor noise dominates (cf. Fig. 7).

The two other loads generally achieve a better SNR due to their higher impedances, but sensor noise is not dominating, as these inductors are subjected to noise related to external EMI sources (due to their large size and number of winding turns) and hence, the Kalman filter is not as effective.

In summary, the performance gain achievable with the Kalman algorithm depends on the noise environment of the amplifier. If the load current noise is dominated by sensor noise, the Kalman filter can provide a significant improvement. If other sources of noise, which act as disturbances to the control system dominate, it can be advantageous to refrain from utilizing a Kalman filter and instead select a higher controller execution rate. If the increase of f_{PWM} is not possible due to the resulting increase of converter switching losses, a real-time Kalman filter provides a viable method to eliminate noise in closed-loop converter systems that use digitally acquired measurements. Thus, in order to reduce cost and sensor complexity, more noisy voltage or current sensors could also be utilized, as the measurement noise is effectively filtered by the Kalman estimator.

The implications of the Kalman filter on amplifier linearity are discussed in [15], where it is shown that the Kalman estimator rejects harmonic signal components from the measurements, as the linear system model does not account for nonlinearities that cause distortion (like saturating inductors or the dead time of the bridge legs). A similar effect potentially influences the noise rejection of the amplifier when the Kalman filter is used, as the filter's linear model cannot consider external disturbances, like EMI that couples directly into the load, e.g., into the windings of an actuator. Consequently, such signal components are attenuated by the Kalman estimator and not present in its output. Thus, they do not appear at the inputs of the feedback control system and therefore cannot be rejected. Due to the often parasitic nature of such external noise sources, an application-specific tuning of the Kalman gain is required in order to optimize the overall noise rejection of the amplifier, or an inclusion of such sources, if they can be modeled with sufficient accuracy, in the process noise matrix.

IV. Further Noise Sources

The demonstrator system allows investigating additional sources of amplifier noise. In the following, the benefits of delta-sigma noise shapers on the load current noise of the converter operating under closed-loop conditions is demonstrated. Furthermore, it is revealed that the low-distortion dual buck topology does not have any implications on output SNR.

A. Modulator Quantization Noise

Due to the relatively low-resolution pulse-width modulators often employed in power electronics converters (usually less than 10 bits of amplitude resolution are available for PWM frequencies in excess of 100 kHz). Therefore, significant wide-band quantization noise is added to the PWM output signals, which is consequently also present in the switched

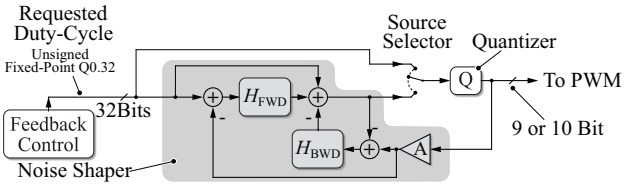

Fig. 15. Noise shaping in the demonstrator system reduces PWM quantization noise from DC to 10 kHz. Further details are given in the Appendix. The noise shaper consists mainly of two FIR filters $H_{FWD\,/\,BWD}$ [17] and can be bypassed to investigate its effect.

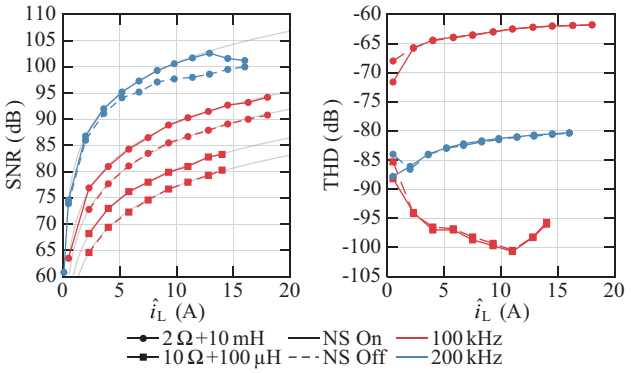

Fig. 16. Experimentally analyzed effects of delta-sigma modulation on SNR with closed-loop converter operation. Regular cascaded control topology (Kalman filter disabled), executed with f_{PWM} = 100 kHz and 200 kHz. At high load currents, the DC supply noise affects SNR. As shown, THD is not affected by the noise shapers. u_{DC} = 400 V, f_F = 35 Hz.

half-bridge waveforms [17]. This naturally reduces the load current SNR. Special quantization techniques (delta-sigma modulation/noise shaping) that are capable of creating low-noise (i.e., high-resolution) signals in a certain bandwidths (e.g., from DC to 10 kHz) are thus highly beneficial for low-noise PWM power amplifiers [38]. The basic functionality of this method is briefly explained in the Appendix. As shown in [17], [18], such noise shaping quantizers are added to the input of each PWM unit, which subsequently is able to provide a low-noise PWM output signal in the desired frequency band. Fig. 15 illustrates the (disengageable) system as used in the demonstrator.

During open-loop operation of the power converter, when no closed-loop feedback system is active, the noise shaper significantly increases the SNR of a pulse-width modulated half-bridge output voltage by up to 30 dB [17]. Fig. 16 illustrates the influence of the noise shapers on SNR during closed-loop converter operation. With bypassed noise shapers, the regular, truncating quantizer creates significant noise and thus, the load current SNR degrades by up to 5 dB. This effect is less pronounced if the higher-gain control system (f_{PWM} = 200 kHz) is utilized, as it is capable of rejecting more quantization noise than the controllers that are executed with 100 kHz. Again, at high load powers, the influence of the DC supply becomes visible as it deteriorates the SNR.

In the same measurement, the load current total harmonic

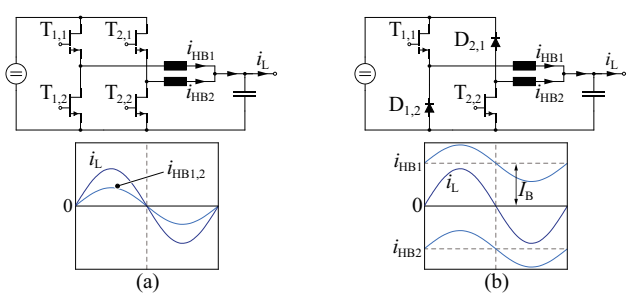

Fig. 17. (a) Regular interleaved half-bridge power stage and the corresponding current waveforms. (b) Dual buck topology, with unidirectional half-bridge currents. In the demonstrator system, the two power diodes are replaced by identical power transistors [15]. This results in the same power transistor arrangement as shown in (a). Further information is provided in [15].

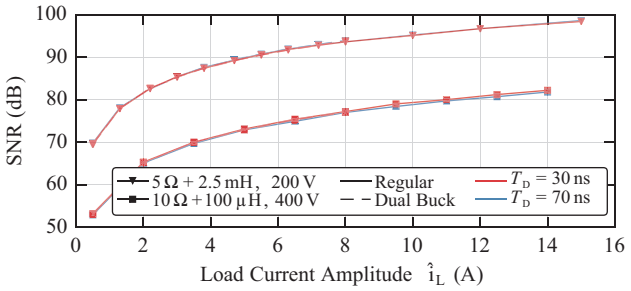

Fig. 18. Experimental analysis of the dependency of load current SNR on half-bridge dead time T_D and power stage topology. 200 V measurements taken with f_{PWM} = 200 kHz, 400 V measurements with f_{PWM} = 100 kHz. f_F = 35 Hz. Kalman filter disabled.

distortion (THD) is also acquired and it is evident that the noise shaping modulator does not affect amplifier linearity. The distortion measurement method is detailed in [15]. This behavior is expected as the noise shaper only affects quantization noise [17].

A noise shaping modulator is a valuable addition to any low-noise PWM conversion system, as it is capable of attenuating a significant noise source. This is especially relevant for power converters without feedback control systems, as shown in [17], [18]. Nonetheless, the noise shaper benefits are still evident in high-performance closed-loop systems. The implementation of the selected noise shaper only requires two comparably small FIR filters (whose orders are usually smaller than 15) that can conveniently be implemented with an FPGA.

B. Low-Distortion Dual Buck Topology

Due to the realization of the demonstrator bridge legs with two interleaved half-bridges, two different power stage topologies can be implemented in order to investigate their influence on converter output distortion [15]. Fig. 17 illustrates the regular interleaved half-bridge and the dual buck topology, together with their corresponding waveforms.

In the regular interleaved topology, both half-bridges of each phase conduct an (ideally) identical current, i.e., half the output (load) current. However, this topology is subject to distortion caused by half-bridge dead time. The dual buck topology introduces a circulating current between the two half-bridges of each phase (cf. Fig. 17(b)), which renders the half-bridge currents unidirectional and hence reduces dead time related distortion significantly. A detailed analysis and comparison of these topologies is presented in [15].

The effect of the two power stage topologies on the load current SNR is investigated with the measurements in Fig. 18. The experimental analysis reveals that the load current SNR is neither affected by the power stage topology, the employed dead time or the DC supply voltage. This is expected as dead time is always constant and introduces no possible source of noise. The dual buck behavior of the power converter is achieved by altering the current references of the four half-bridge current controllers such that the desired circulating current is introduced. This change in power circuit topology does not provide an additional source of noise. Thus, the only significant disadvantage of the dual buck topology are its increased transistor losses (due to the additional circulating current) and hence, a reduced amplifier output current capability [15].

V. Conclusion

In this paper, important system constituents for achieving low-noise, high-power output waveforms of digitally controlled switch-mode power amplifiers are presented, analyzed and directly compared. The results are, e.g., relevant for the applications of such systems in nanometer-scale positioning tasks such as lithography processes in integrated circuits manufacturing that require actuator current signal-to-noise ratios (SNR) in excess of 100 dB (DC–10 kHz), which is demonstrated in this work. A 400 V power converter based on gallium nitride (GaN) power transistors is used for demonstrating different influence factors. Further details of the prototype can be found in [15].

First, noise is effectively attenuated by a feedback control system. It is shown how digital controllers with high open-loop gains are enabled by fast execution rates and consequently, high converter PWM frequencies. The demonstrator system can achieve a pulse repetition rate of 200 kHz which, compared to a control system executed with half this rate, increases load current SNR by ≈ 10 dB to values in excess of 105 dB.

Measurements with the prototype system reveal the importance of a low-noise DC amplifier power supply, as industrial laboratory supplies are not optimized for low-noise voltage outputs and hence, the amplifier load current SNR is limited at high power levels due to noise injected from the DC supply.

Furthermore, the load current SNR can be improved by employing a real-time, steady-state Kalman filter (seven states and four inputs). It effectively attenuates residual sensor noise, to which the feedback control system in principle reacts sensitively. The high processing power provided by the demonstrator's combination of FPGA and procedural CPU (*Xilinx Zynq*) enables a Kalman filter execution rate of 100 kHz, which increases the load current SNR by more than 10 dB, such that it reaches values of more than 108 dB.

Finally, it is shown how the delta-sigma modulating noise shapers, used to mitigate the quantization noise of the low-resolution PWM modulators, improve the load current SNR by up to 5 dB, while not affecting distortion.

As an outlook, several options are feasible to even further increase the amplifier SNR. First, the careful consideration of the DC supply of such switch-mode power amplifiers, with regard to output voltage noise and control stability, could prevent the injection of noise into the amplifier circuit. This is especially important for single-phase amplifier loads, as they are characterized by a pulsating power flow. A power pulsation buffer could be used to relieve the power supply from delivering a pulsating current and/or to stabilize the amplifier's supply voltage [39]. Additionally, an active power supply filter, basically consisting of a non-isolated DC/DC converter that employs low-noise technologies as presented in this work, could be connected between the (noisy) DC power supply and the precision amplifier, to provide a well-stabilized, low-noise supply voltage.

Another method to increase the load current SNR is offered by paralleling the outputs of N precision amplifiers (e.g., by interleaving more half-bridges). The output noise of the different converters is (ideally) uncorrelated and hence, the overall noise power only increases with $\sqrt{N}$, whereas the available power of the intended output signal increases linearly with N, which boosts the achievable SNR [40]. A higher number of interleaved half-bridges could also open the possibility to use only one noise shaper per amplifier phase and operate it at the effective interleaved frequency $N f_{\mathrm{PWM}}$ of the power converter, as opposed to utilizing one noise shaper per half-bridge, operating with f_{PWM}. This increases the modulator's noise rejection capability in the base band, which further reduces PWM quantization noise [17].

In summary, this work presents a fully digital switch-mode power amplifier with unprecedented output noise levels, resulting in load current SNR figures in excess of 100 dB at rated output. The relatively low realization effort of the proposed system encourages the usage of efficient and high-power switch-mode amplifiers in applications that currently rely on complex and low-efficiency linear or hybrid systems.

Appendix

A. Limits of Digital PWM

Digital PWM is widely adopted for the generation of power switch control signals due to the constant modulation frequency and simple structure. In the presented application, it is used to obtain the half-bridge switch control signals. The modulators are commonly based on digital counters, as illustrated in Fig. 19. It is evidant that each counter step represents a possible PWM duty cycle and hence, the duty cycle (and correspondingly, the half-bridge output voltage) can only take values from a discrete set (i.e., it is quantized), with the number of available counter steps representing the respective duty cycle resolution.

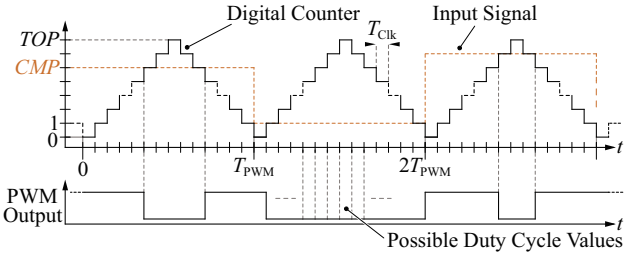

Fig. 19. Digital pulse-width modulation. Each counter step, which, due to its digital nature, is amplitude-quantized, represents a possible duty cycle. Consequently, the duty cycle is also quantized correspondingly, as the half-bridge output voltages can only take values from a discrete set that corresponds to the available duty cycles.

Thus, the achievable SNR of the PWM output signal is limited due to quantization errors that are common to signals of finite amplitude resolution. The SNR of a sinusoidal, amplitude-quantized digital signal (e.g., the modulated half-bridge transistor gate control signal) with a resolution of n bits can be approximated by

$$\mathrm{SNR} \approx 6.02n + 1.76\ \mathrm{dB}\ . \tag{10}$$

The corresponding quantization noise occurs in a frequency range from DC to half the signal's sampling frequency ($f_s/2$) [20].

To obtain low-noise digital signals (e.g., in this case from a PWM modulator), a sufficient number of amplitude levels is mandatory. This requires high digital clock frequencies such that the digital counter covers all required values within the PWM period. For example, to obtain a PWM signal with a pulse repetition rate of $f_{\mathrm{PWM}} = 50$ kHz and a duty cycle resolution of $n = 17$ bits, a clock frequency $f_{\mathrm{Clk}} \approx 13.1$ GHz is necessary. However, the physical implementation of high-resolution counters operating at such high clock rates is unfeasible with state-of-the-art digital logic circuits. Consequently, low-SNR PWM signals cannot be generated at PWM frequencies that are common in power electronics (e.g., ≈ 10 kHz to 1000 kHz) with regular modulation techniques.

B. Delta-Sigma Modulation

Noise shaping delta-sigma modulation comprises different methods that can alter the frequency distribution of quantization noise [38]. In the context of the presented digital power amplifier, the employed noise shaping modulators shift the quantization noise to frequencies above 10 kHz, where it does not affect mechatronic positioning systems. This quantization noise is necessarily generated when low-resolution digital signals are created from high-resolution references, such that regular, low-resolution pulse-width modulators can be employed. Fig. 20 exemplarily illustrates the resulting noise power spectral densities of the signals that are supplied to regular pulse-width modulators. This allows the unaltered replication of the high-resolution reference signals with low-resolution PWM in a certain frequency band.

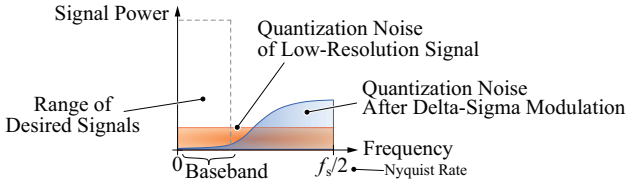

Fig. 20. Illustration of spectral densities of quantization noise of digital, sampled signals (sampling rate f_s), both with and without delta-sigma modulation. Quantization noise can be shifted to higher frequencies to obtain a low-noise baseband.

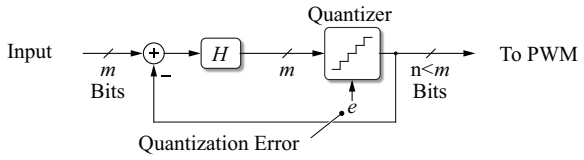

Fig. 21. Simplified noise shaping principle. The transfer function H can be designed to attenuate the quantization noise (caused by the quantization error e), while minimally affecting the desired signal, in this example.

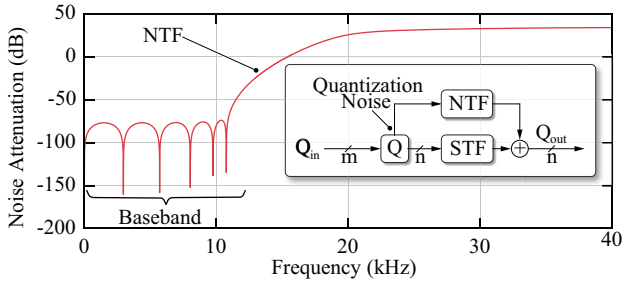

Fig. 22. Amplitude plot of an exemplarily selected noise transfer function (NTF). The high-pass characteristic shifts the quantization noise to higher frequencies. The signal transfer function is usually unity and does not affect the desired signal.

The basic concept behind a noise shaping signal conversion system, that is used to reduce the resolution of digital signals, is illustrated in Fig. 21. The digital reference input signal has a high amplitude resolution of m bits, whereas the low-resolution output (n bits), which, in the discussed application can be used as input for the subsequent pulse-width modulator, is generated by rescaling and truncating the input signal, which maps it to the (smaller) range of the output signal. The transfer function of this exemplarily selected simple arrangement is given as

$$\text{Output} = e \cdot \underbrace{\frac{1}{1+H}}_{\text{NTF}} + \text{Input} \cdot \underbrace{\frac{H}{1+H}}_{\text{STF}}, \tag{11}$$

where the noise transfer function (NTF) determines the effect of the quantization noise e on the output, and the signal transfer function (STF) describes the behavior of the input signal on the output. Noise-shaping delta-sigma modulation structures are generally designed such that STF = 1.

Thus, only the quantization noise is affected by the delta-sigma modulator, whereby the NTF is selected such that the noise is shifted to higher frequencies (high-pass characteristic). Fig. 22 illustrates an NTF that attenuates noise in the baseband from DC to 10 kHz by ≈ 75 dB.

Further details on the specific implementation of the delta-sigma modulators utilized in the demonstrator amplifier's control system are given in [17], [18].

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Control Techniques of the Auxiliary-Resonant Commutated Pole With Special Regards on the Dual-Active Bridge DC-DC Converter

Johannes Voss, Jochen Henn, and Rik W. De Doncker

***Abstract*—In this work, a dual-active bridge dc-dc converter with auxiliary-resonant commutated pole is presented. The paper focuses on the control strategies of the auxiliary-resonant commutated pole to allow soft turn on and soft turn off of the main switches, and thus increasing the efficiency of the converter. These strategies are developed for a high-power IGCT-based dual-active bridge dc-dc converter. Two boosting strategies, constant time magnetization and constant current boosting are presented and tested. Besides its main objective to reduce the switching losses, the ARCP also allows balancing of the dc-link voltages in case of imbalanced loads. Strategies for boost current control and active dc-link balancing are introduced, presented and experimentally verified on a small-scale laboratory setup.**

***Index terms*—DC-DC power converters, field programmable gate arrays, resonant inverters, soft-switching, zero-voltage switching.**

I. Introduction and Motivation

In Fig. 1, the schematic of a dual-active bridge (DAB) dc-dc converter with auxiliary-resonant commutated pole (ARCP) is shown. In case one of the main devices is switched, the ARCP causes a resonance to allow a zero-voltage condition at the main devices which then results in soft switching. This soft-switching behavior can be supported by additional resonant capacitors C_{res}. In case of using ARCP with IGCTs, it has been shown that the switching losses can be reduced to an eighth of the original amount [7]. Further details on the DAB can be found in [1] and [8] and on the ARCP in [2] and [9]. The presented control techniques for the ARCP are developed for a 5 MW DAB. Therefore, some presented hardware components are designed for 5 kV and fiber optical logic signals are used. The techniques are tested on a smallscale model (SS-DAB) rated for powers in the lower kW range to minimize risks.

A. Auxiliary-Resonant Commutated-Pole for Dual-Active Bridge

As described in [1], a two-level three-phase DAB operates in six-step mode where each bridge is switched with a constant duty cycle of 50%. The three phases of the bridge are shifted by 120° generating a six-step voltage waveform at the transformer terminal. The phase shift between the primary and secondary bridges causes a voltage drop across the transformer leakage inductance, resulting in a power flow.

In partial load conditions or unsymmetrical input/output voltages, the DAB converter loses its soft-switching capability because there is not enough reactive current to discharge the snubber capacitors of the turning off device. Hence, the turning off devices are hard switched. The ARCP circuit is a promising technique to overcome this problem, thus extending the soft-switching capability of the DAB. The main principle is to force a resonance just before a commutation process from a bottom switch to a top switch (BtT) or vice versa (TtB) so that the snubber capacitors in parallel to the switched device are fully discharged and charged, respectively [2], [4]. The main switch is then triggered under a zero-voltage condition. Especially thyristor-based turn-off devices (GTOs or IGCTs) have a deeper charge carrier saturation [3] and, therefore, introduce higher switching losses as compared to their competitive devices, e.g. Insulate-Gate Bipolar Transistors (IGBTs). To overcome the drawback of high switching losses and to take advantage of the superior conduction behavior of IGCTs, an ARCP can be applied to the DAB.

B. Control Techniques Supporting Soft-Switching

In Fig. 4, one phase-leg of the three-phase DAB with ARCP (DAB ARCP) is shown. A more detailed description of the basic ARCP principle can be found in [2] and [5]. The auxiliary inductor L_{AUX} needs to be tuned, according to the di/dt characteristics of the device in the converter with the lowest di/dt capability. In case the converter legs consist of IGBTs, no restriction for di/dt exists. However, IGCTs have di/dt limitations (e.g. 800 A/μs) which make a conservative design of L_{AUX} necessary.

Furthermore, Fig. 4 introduces a zero-voltage detection (ZVD). This ZVD is needed to switch on the main devices during the zero-voltage condition and to protect them from short-circuiting the resonant capacitors C_{res} in case they are not completely discharged. Since the resonance phase is in the range of 10-30 μs the ZVD must be very fast to avoid a flip back of the voltages across the resonant capacitors. A controller unit triggers the switch via the ZVD: whenever the ZVD

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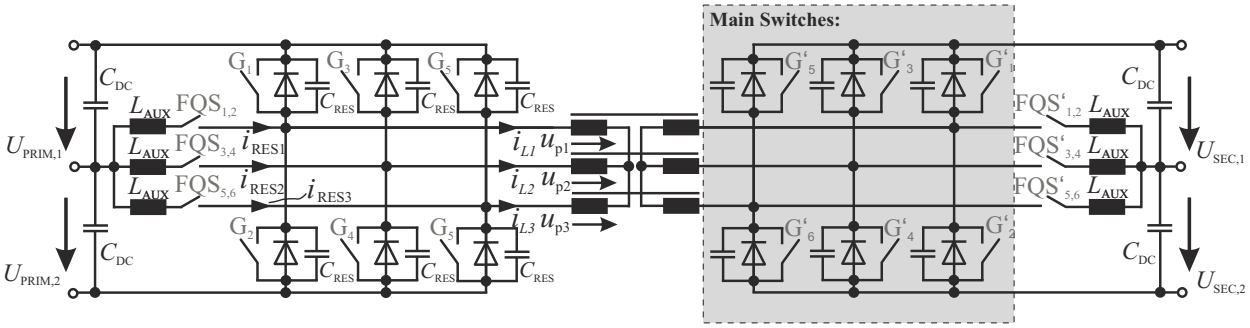


Fig. 1. Dual-active bridge with auxiliary-resonant commutated pole.

TABLE I
SPACE VECTORS (SV) AND THYRISTOR TRIGGERING SIGNALS FQS FOR ONE CONVERTER

Time Sequence	SV	FQS	State
$-T_{discharge} < t < 0$	000000	000000	0
$-T_{trg} < t < 0$	010101	010000	0-1
$0 < t < T_{sw}/6$	100101	000000	1
$T_{sw}/6 - T_{trg} < t < T_{sw}/6$	100101	000100	1-2
$T_{sw}/6 < t < 2T_{sw}/6$	101001	000000	2
$2T_{sw}/6 - T_{trg} < t < 2T_{sw}/6$	101001	100000	2-3
$2T_{sw}/6 < t < 3T_{sw}/6$	011001	000000	3
$3T_{sw}/6 - T_{trg} < t < 3T_{sw}/6$	011001	000001	3-4
$3T_{sw}/6 < t < 4T_{sw}/6$	011010	000000	4
$4T_{sw}/6 - T_{trg} < t < 4T_{sw}/6$	011010	001000	4-5
$4T_{sw}/6 < t < 5T_{sw}/6$	010110	000000	5
$5T_{sw}/6 - T_{trg} < t < 5T_{sw}/6$	010110	010000	5-6
$5T_{sw}/6 < t < 6T_{sw}/6$	100110	000000	6
$6T_{sw}/6 - T_{trg} < t < 6T_{sw}/6$	100110	000010	6-1

detects a turn-on signal and a zero-voltage condition at the main device, it is triggered on (logic AND). In case the controller unit generates a trigger signal without having zero-voltage condition, the ZVD does not trigger the main devices and thus avoiding a snubber dump.

As given in literature [8], [2] and [11], a boost current is an additional current which is needed to overcome losses during switching and to force a current into the anti-parallel diodes.

In this paper, two boosting strategies are introduced: the constant boost time and the constant boost current. By iterative simulation and loss estimation, the minimal boost time can be determined for various but steady operating points of the converter, as it has been shown in [10]. Instead of setting a constant boost time, a constant boost current can be obtained by using additional hardware. Since in dc grids a voltage variation of +/−10% may exist, a constant boost time will lead to different boosting currents, i.e. an increased dc-link voltage causes a linear increasing ARCP peak current. By choosing a constant boost current technique, it is guaranteed to have the same boost current in every operation point of the converter.

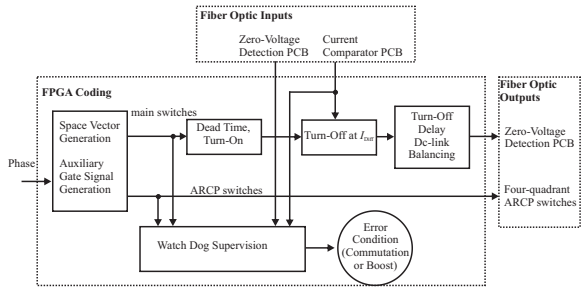


Fig. 2. Structure of the control algorithms in the FPGA.

II. CONTROL OF THE DAB WITH ARCP

In this section the generation of gate signals is explained. The code has been verified in Matlab/Simulink using the Xilinx System Generator. In TABLE I, the switching sequence for the space vectors (SV) controlling the main converter legs and the four-quadrant switches (FQS) for the auxiliary branch are programmed on the FPGA[1]. Since thyristors are line-commutated devices, '0' does not necessarily mean that the device is not conducting current. Whenever the thyristors is triggered it carries current until it decays to zero. During $T_{discharge}$ the resonant capacitor has to be discharged by the zerostate chopper (ZSC). Without using a ZSC, the converter is not able to start from an initial space vector '000' as given in the TABLE I with state 0, since the snubber capacitors of the device would share the dc-link voltage equally and the ZVD will not allow to trigger the main devices. Hard-switching with IGBTs might not be a critical, due to their high over current capability without d*i*/d*t* limitation. In case of IGCTs this is crucial aspect. T_{sw} defines the switching period and T_{trg} marks the magnetization time of the resonant inductor. Whenever a state should be changed, the corresponding FQS is triggered to realize the resonant commutation of a leg (e.g. from state 0 to state 1 only FQS_1 must be triggered). In total, 12 gate signals for the main switches and 12 FQS signals are generated for the primary and secondary side. As shown in Fig. 2 a turn-on delay is embedded to prevent a short circuit on the dc link in any case. The turn-off block given in Fig. 2 is only applied when constant boost

[1] '1' means a switch is triggered on, and '0' a switch is not triggered, e.g. $SV(G_1,G_2,G_3,G_4,G_5,G_6)$ = '000000' means all switches are not triggered.

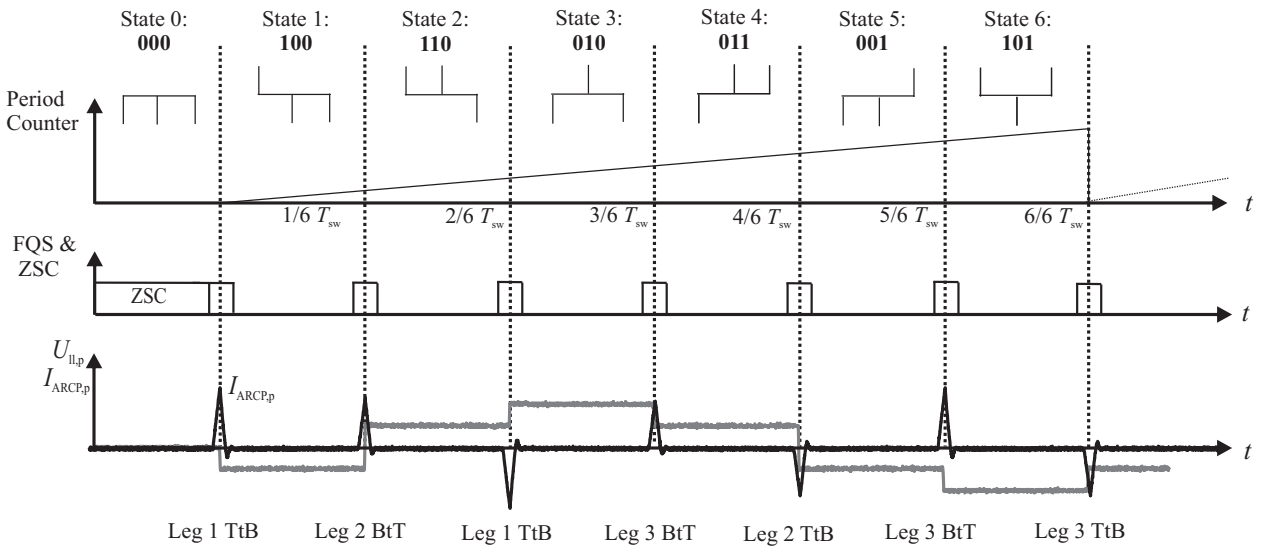


Fig. 3. Space vectors and the resulting phase voltage of the 3PH DAB including the ARCP currents.

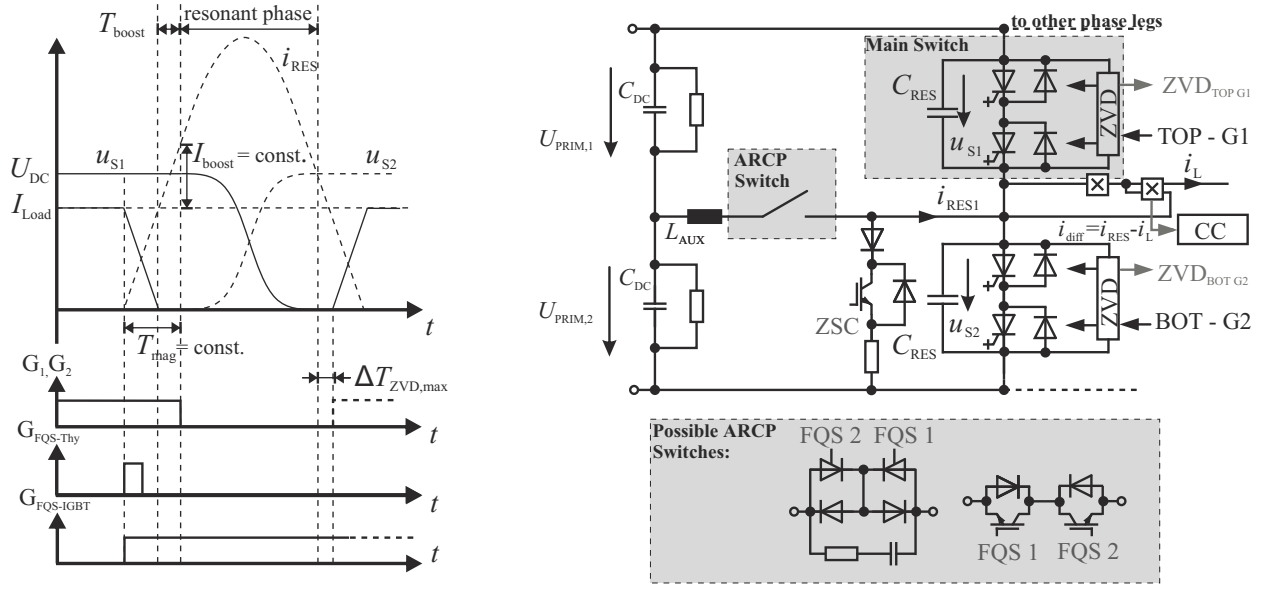


Fig. 4. Boosting strategies for ARCP current: Either constant magnetization time or constant boost current using comparator PCB.

current mode is applied, which will be explained in the next section.

In TABLE I and TABLE II, the basic timings for the main switches and the FQS are given. Various topologies of semiconductor for the four-quadrant switch (FQS) are possible. Since the resonant phase ends at a zero-current crossing line-commutated and forced-commutated devices can be utilized. In case of line-commutated devices, namely thyristors, only a short trigger impulse has to be applied to start the resonant phase. If forced-commutated devices are used (e.g. MOSFETs, IGBTs or IGCTs), the devices are not allowed to turn off during current commutation. A good solution, is adding up twice the magnetization-time (rising, boosting and falling) of the auxiliary inductor plus the time of the resonant phase as defined in [2], in worst case condition. If the device would be turned off before the current decays to zero, the auxiliary inductor would cause an over-voltage condition at the device.

In Fig. 3 the SV given for each converter leg are depicted with the timing constrains for thyristor-based FQS and the ZSC. The resulting six-step voltages of the DAB and the resonant current i_{res} of the ARCP are plotted below.

A. Commutation Control

The boost current is essential for a proper commutation. Whenever the current in the device that is about to be turned off is negative, and thus the anti-parallel diode is conducting, the current needs to be reversed for the commutation. In this operation mode, the current in the auxiliary branch must be higher than the load current to overcome losses during the

TABLE II
SPACE VECTORS (SV) AND IGBT TRIGGERING SIGNALS (FQS) FOR ONE CONVERTER

Time Sequence	SV	FQS	State
$-T_{\text{discharge}} < t < 0$	000000	000000	0
$-T_{\text{trg}} < t < +2 \cdot T_{\text{trg}}$	010101	010000	0-1
$0 < t < T_{\text{sw}}/6$	100101	000000	1
$T_{\text{sw}}/6 - T_{\text{trg}} < t < T_{\text{sw}}/6 + 2T_{\text{trg}}$	100101	000100	1-2
$T_{\text{sw}}/6 < t < 2T_{\text{sw}}/6$	101001	000000	2
$2T_{\text{sw}}/6 - T_{\text{trg}} < t < 2T_{\text{sw}}/6 + 2T_{\text{trg}}$	101001	100000	2-3
$2T_{\text{sw}}/6 < t < 3T_{\text{sw}}/6$	011001	000000	3
$3T_{\text{sw}}/6 - T_{\text{trg}} < t < 3T_{\text{sw}}/6 + 2T_{\text{trg}}$	011001	000001	3-4
$3T_{\text{sw}}/6 < t < 4T_{\text{sw}}/6$	011010	000000	4
$4T_{\text{sw}}/6 - T_{\text{trg}} < t < 4T_{\text{sw}}/6 + 2T_{\text{trg}}$	011010	001000	4-5
$4T_{\text{sw}}/6 < t < 5T_{\text{sw}}/6$	010110	000000	5
$5T_{\text{sw}}/6 - T_{\text{trg}} < t < 5T_{\text{sw}}/6 + 2T_{\text{trg}}$	010110	010000	5-6
$5T_{\text{sw}}/6 < t < 6T_{\text{sw}}/6$	100110	000000	6
$6T_{\text{sw}}/6 - T_{\text{trg}} < t < 6T_{\text{sw}}/6 + 2T_{\text{trg}}$	100110	000010	6-1

commutation and to accomplish the commutation within a reasonable time. Here, two techniques are presented:

1) Fixed Magnetization Time

In terms of control effort, keeping the magnetization time constant is a straight forward approach. The magnetization must greater than the rising time and the minimal required boosting time. The FPGA is set up to trigger the FQS a certain time before the main switches transition. This time can either be kept constant overall operating points or adjusted by the controller according to system voltage and phase current amplitudes. Anyway changing the time according to the operation point of the converter can be challenging during operation.

Fig. 5(a) and (b) depicts the effect of changing system voltages on the resonant currents at a constant boost time.

Except for ease of control, this approach has the following drawbacks: for commutations at negative phase currents, constant magnetization time will increase the device stress during turn-off for the bottom main switches, as it adds the full resonant current to the load current, thus increasing the resulting current in the switch. This unnecessary current causes losses in all devices taking part in these commutations.

However, constant boost time has the natural capability of balancing the dc-link voltages. Whenever one of the two dc-link capacitors connected in series is unbalanced, the auxiliary inductor is magnetized with a higher peak current. As shown in Fig. 5(c), an increased amount of energy is pushed into the corresponding capacitor.

2) Constant Boost Current

The drawbacks of a control based on equations and calculations for optimal boost time [10] can be overcome by dynamically terminating the boost sequence. This can be

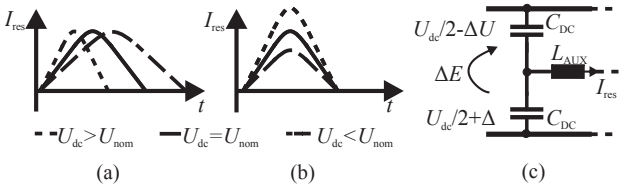


Fig. 5. Impact of dc-link voltage variation on constant boost current strategy (a) or constant boost time strategy (b) and increasing boost current during bottom to top transition for dc-balancing purposes (c).

achieved by monitoring the difference of resonant and load current i_{RES}-i_{L} using an additional sensing. If this difference reaches a certain limit I_{lim}, the FPGA will turn off the according main switch, stopping the inductor magnetization. This way, the influence of load current and voltage amplitude are rejected and the boost current is kept constant. The increased hardware effort is a clear drawback of this approach. Adjusting the turn-off time of the main switches according to the incoming signal is a small extension of the existing FPGA code.

B. DC-Link Balancing Using Variable Boost Currents

The ARCP circuit is connected to the midpoint of the dc-link, thus the DAB converter can be used in bipolar dc systems. For a system with unbalanced loads, the DAB ARCP can provide voltage balancing capabilities. The following subsections will discuss the natural and active dc-link balancing behavior of the ARCP as well as the control approach taken. A hysteresis controller enables active dc-link balancing for variable set and reset boundaries as shown in Fig. 9(c). Both, the upper and lower dc-link voltages are monitored and therefore the DSP is able to determine how to counteract the imbalanced voltages. Fig. 2 depicts the block 'turn off delay' which allows to extend the magnetization time of the auxiliary inductor. To balance the dc-links only the magnetization time for one component is extended. E.g. if the upper dc-link $U_{\text{PRIM,1}}$ is lower compared to the second one $U_{\text{PRIM,2}}$, the boost time of the FQS2, FQS4 and FQS6 is extended. In case, the dc-link of $U_{\text{PRIM,2}}$ is lower, the boost time of FQS1, FQS3 and FQS5 is adjusted. As a result the ARCP currents are asymmetrical and thus the power transferred between the dc-link capacitors is asymmetrical as well. The basic topology behind the ARCP is a push-pull converter. Based on this knowledge, it would be possible to define a transfer function with a disturbance coupling according the load current i_{L}. Here, for simplicity, only a hysteresis controller is embedded. Whenever the voltage differs more than 20% from half the sum of the two measured dc-link voltages - nominal $U_{\text{dc}}/2$ - the hysteresis control is engaged until the difference of the virtual $U_{\text{dc}}/2$ is less than 2%.

III. SIMULATION OF PROPOSED CONTROL TECHNIQUES

The simulations are performed in Matlab Simulink/PLECS and the VHDL code is integrated using the Xilinx System Generator. In Fig. 6, the results of the simulations are shown. At the beginning of the simulation, the zero-state chopper is activated until the resonant capacitors at the bottom switches are

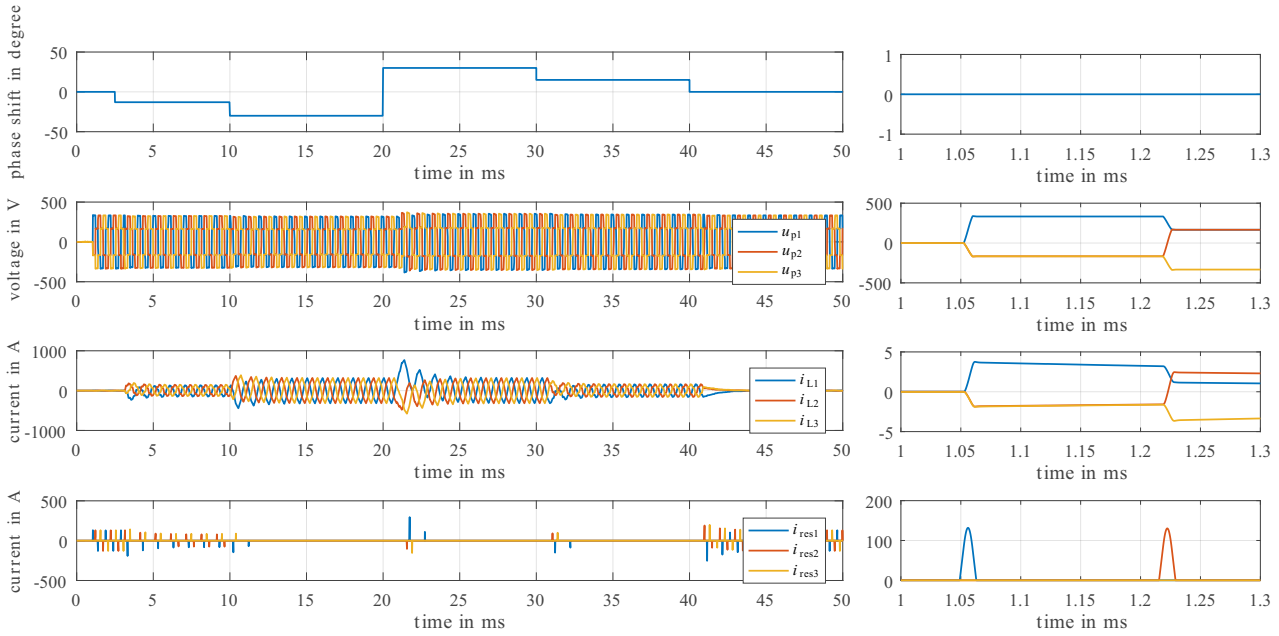


Fig. 6. Performed simulation of the FPGA code using the Xilinx System Generator.

completely discharged, equivalent to state 0.

In the first plot of Fig. 6, the phase shift is given in degree. In the second plot, the phase voltages, phase currents and, finally the ARCP currents are depicted. On the right-hand side, a zoomed in of the start-up procedure is shown. Here, the converter is initiated, using the zero-state of the SVM. The transition of the first interval is supported with the ARCP branch, up to approximately $t = 4$ ms.

The phase shift is increased afterwards. Due to transient effects which results in dc-voltage-offsets, the ARCP is activated only at some switching transitions since the phase current does not reach the specified minimum load current for natural soft switching.

At $t = 10$ ms, the phase-angle is changed to its maximum and the converter is running at nominal load. Now the phase current is beyond the minimum load current for soft switching and the ARCP is left turned off. This operation area is named as natural soft-switching mode since no additional reactive power is needed to allow zero-voltage switching. The nominal power is reversed at $t = 20$ ms. The very fast change of the load causes very high peak currents during the transition.

The current comparator equivalently reacts on this current and ensures soft-switching during this event. This could be avoided using ICC as proposed in [12]. However, using ICC additional timing constrains regarding minimum intermediate steps must be considered.

Afterwards, the power is decreased equally and the con-verter is running in forced soft-switching mode again.

IV. Small-Scale Laboratory Setup

Here, the experimental setup of the small-scale dual-active bridge (SS SAB) is introduced. The utilized hardware is pictured in Fig. 7. The schematic is given in Fig. 8. The dc-link

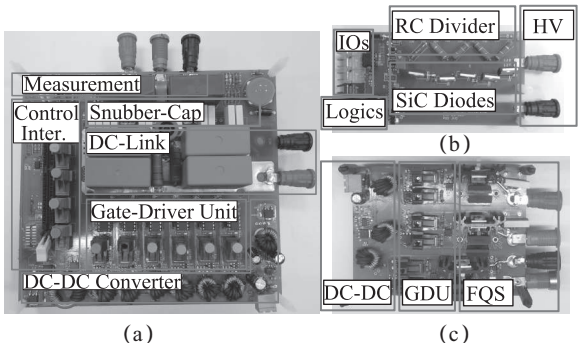


Fig. 7. Pictures of components in the experimental setup.

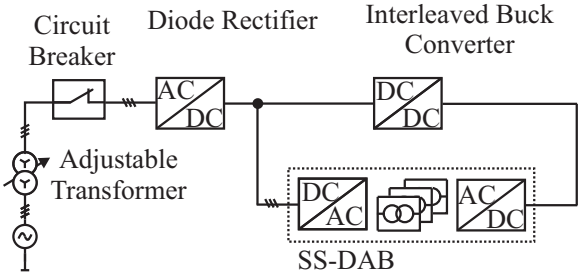
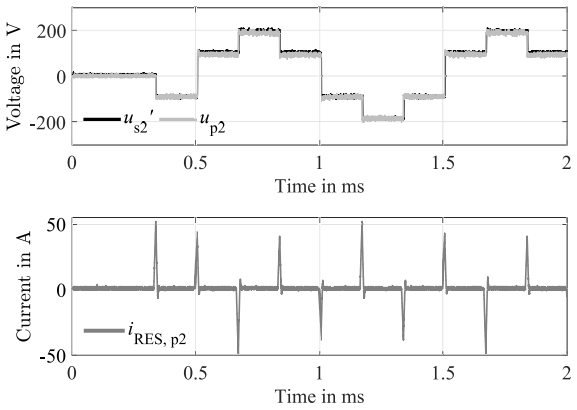


Fig. 8. Simplified schematic of the SS DAB laboratory setup.

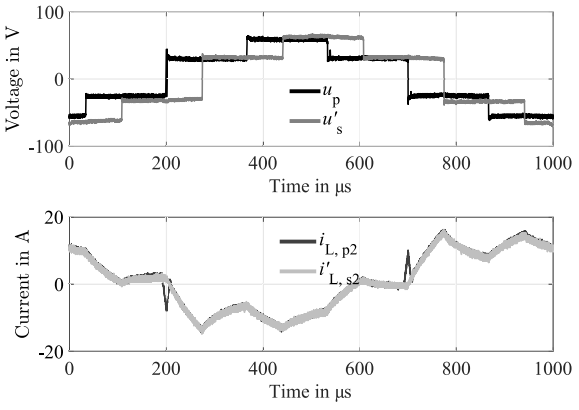
is powered by an adjustable transformer with a diode rectifier to test the strategies under varying voltage conditions.

A. Voltage-Source Converter

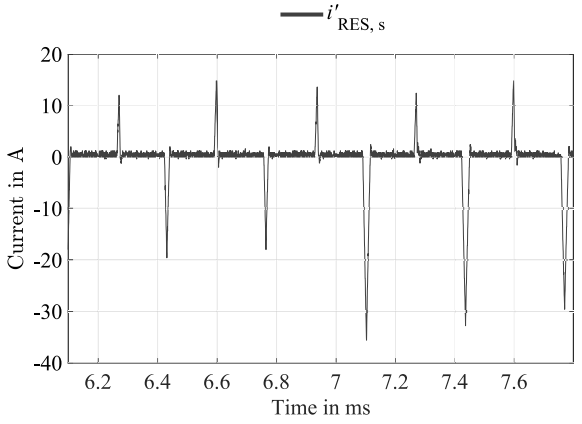
The three-phase input and output converters as well as the buck converter are independent systems incorporating a fiber optic input/output interface (I/O), galvanically isolated GDUs,



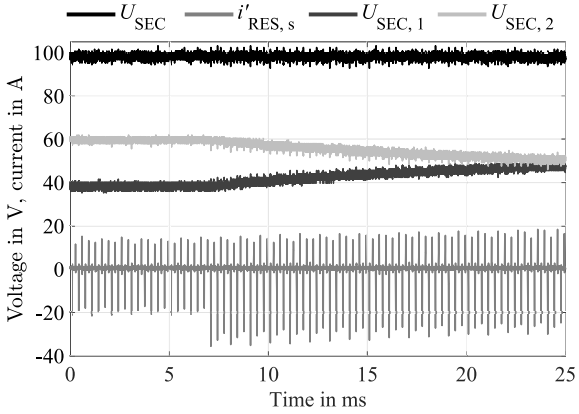
(a) Characteristic voltages of the DAB during start-up procedure for DAB-ARCP operation and primary resonant currents of all phases.



(b) Primary and secondary transformer voltages and phase currents with auxiliary current for primary side at 45° phase shift. Boost currents visible in I_L at t = 200 µs and 700 µs



(c) Engaging active balancing of dc-links with hysteresis controller at t = 7 µs.



(d) Detailed view of I_{ARCP} in Fig. 9(c) around t = 7 µs.

Fig. 9. Experimental results part 1.

an IGBT module and a heat sink. The IGBT modules are mounted under the PCB on a heat sink and not visible in Fig. 7(a). The converter is state-of-the-art topology with additional snubber capacitors mounted at the output side. If the converter is used as an independent system, a TI F28335 DSP can be plugged in and programmed via USB interface.

B. Four-Quadrant Switches for ARCP

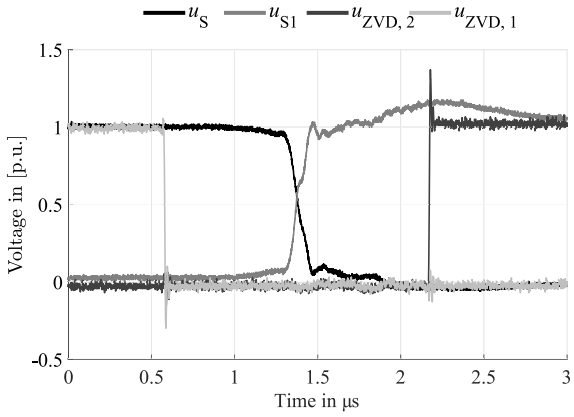
In this work, both types of FQS based on thyristors and on IGBTs are used. Both topologies have advantages and disadvantages. From control perspectives, thyristors are beneficial since they turn off at a zero crossing. However, most common thyristors are not designed for higher switching frequencies, resulting in restrictions for di/dt and dU/dt and during soft-start sequences of the converter. Fig. 7(c) show a version with thyristors.

C. Zero-Voltage Detection and Current Comparator

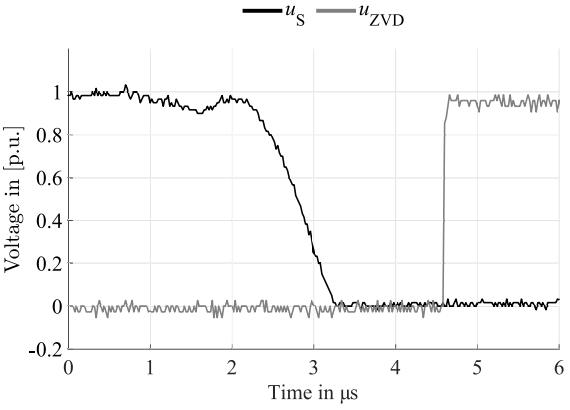
The ZVD is necessary to prevent the main devices from switching while their snubber capacitor is still charged. IGCTs in general are sensitive to high di/dt slopes, as their structure can cause internal hot spots if a high current immediately after a turn on occurs [13]. Since the ZVD is designed for the 5 MW, 5 kV converter zero-voltage is defined as voltage below 20 V. The ZVD is shown in Fig. 7(b).

In case of an early turn-on of the main switch, these additional devices would protect the main switches from shorting the snubbers, which is called a snubber dump. The detection PCB via the main switches in the main converter legs is directly mounted across the snubber capacitors. The basic logic is illustrated in Fig. 11. The PCB receives the gate turn-on signal from the FPGA. This signal is delayed and only passed on to the device once the voltage condition of less than 20 V is reached.

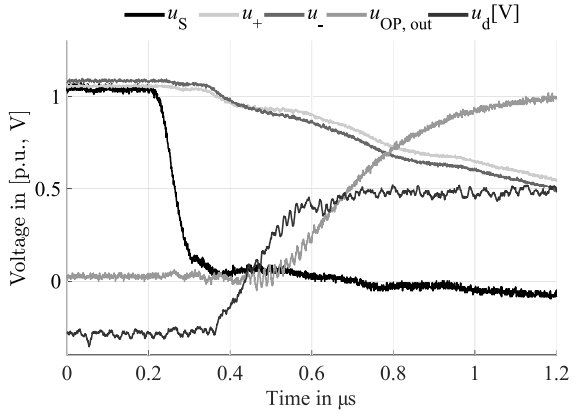
The circuit schematic of the ZVD is shown in Fig. 12. To block against the 5 kV, five SiC high-voltage (HV) diodes, each rated for 1.2 kV, are connected in series, with a typical forward voltage of 0.77 V at low currents, as indicated in Fig. 12. Their capacitance is stated to be 59 pF at 800 V. They are connected in series and terminated to ground with a Zener diode U_Z = 20 V. The voltage across the SiC diodes is balanced with an ohmic divider. Each resistor is rated for 470 kΩ. In order to maintain a predictable behavior, to reject parasitic elements and to provide a stable delay over a wide range of operating points, a constant



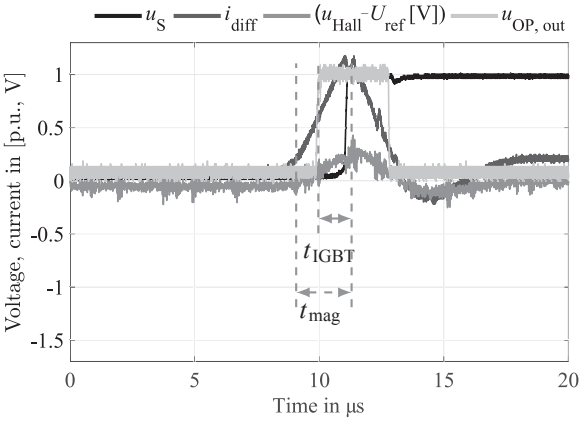
(a) Detailed voltages during a resonant commutation and voltage input of the fiber optic receiver at the main switch GDU generated by the ZVD.



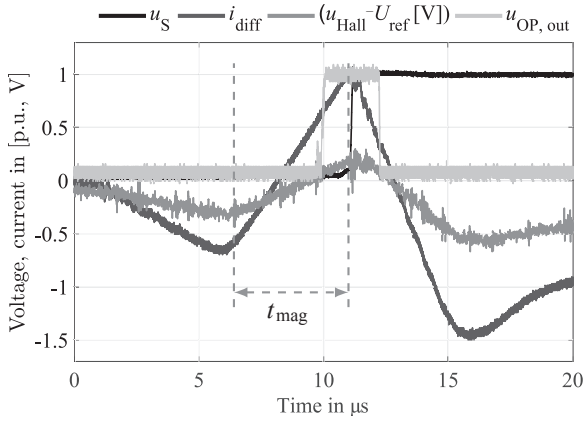
(b) Voltage of main switch and delay of ZVD during a test at 1.2 kV.



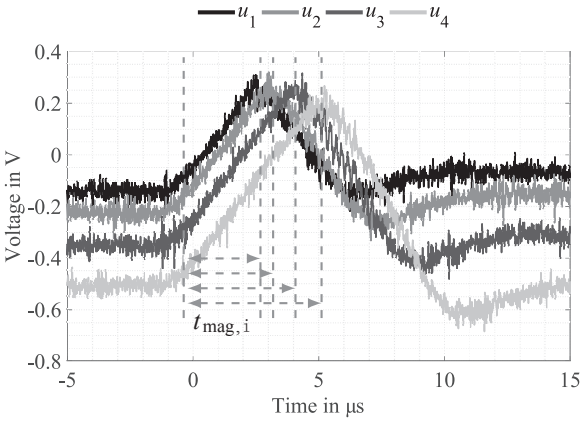
(c) Detailed probe signals of ZVD during test at 80 V.



(d) Constant boost current control at no load current condition.



(e) Constant boost current at negative load current condition.



(f) $U_i = U_{Hall}$–U_{ref} on current comparator at various operating points resulting in different magnetization times and constant current amplitudes.

Fig. 10. Experimental results part 2. measurements in (a) to (e) are in p.u.

current source supports the detection circuit. This current source is constantly feeding approximately 30 mA into the circuit. Depending on the switching state of the main switch, this current will flow through the Zener diode or into the switching path. Thus, the provided energy keeps the voltage across the Zener diode high until the current changes paths into the HV diodes. Compared to a voltage source, no additional capacitors are used and the parasitic capacitance of the Zener diode is not increased. An adjustable voltage divider provides a reference voltage U_+ for the comparator as indicated in Fig. 12. For low voltages across the switch or a short between U_S and ground, the current source will feed current into the switching path

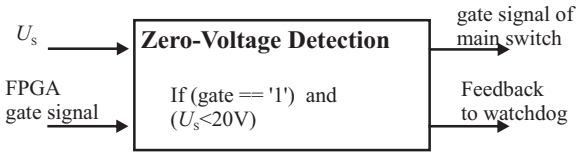


Fig. 11. Logic of zero-voltage detection.

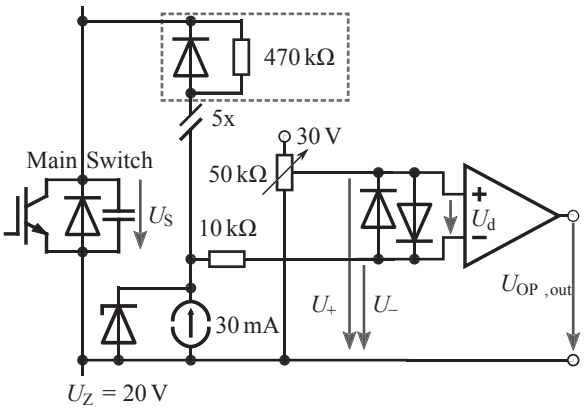


Fig. 12. Schematic of the analogue part on the zero-voltage detection PCB.

and thus pull U_- down and forward bias the protection diode in front of the comparator. Therefore, U_d is positive. Since the operational amplifier acts as a comparator, the output resembles a logical high for $U_d \geq 0$ V. In the opposite case, at a voltage greater than 20 V across the switch, the Zener diode will pull up U_-. By adjusting the reference voltage to be slightly below the Zener voltage, the delay produced by the ZVD can be minimized. Although, a safety margin should be kept in order to provide more stability. The output $U_{OP,out}$ is linked to the gate signal from the FPGA on a logic AND gate to generate the final main switch gate signal.

Another critical feature of a ZVD is its delay chain. In order to turn on the main switch as long as zero-voltage conditions are present, the ZVD should not withhold the gate signal too long. During a resonant commutation, an interval of a few micro seconds exists where the main switch is turned on under zero-voltage conditions. Delays inside the ZVD are caused by the parasitic charging, the lag of the comparator and the logic "AND" IC. The first two can be observed in Fig. 10(c). For this experiment, the reference is set close to the Zener voltage, so the delay between U_{SW} being smaller than 20 V is as short as possible. Here, it is about 100 ns. The time between $U_d > 0$ V and the output of the comparator reaching high is about 0.5µs.

D. Current Comparator

The comparator is needed to compare the current in the auxiliary branch I_{RES} to the load current I_L. Whenever I_{RES} is higher than the I_L, it can be ensured that boost current is flowing into the diode during commutation. The phase to resonant current comparator is logic high whenever the current $I_{DIFF} = I_{RES} - I_L$ is higher than a predefined limit. Since the boost current is only present during a commutation, it takes an unreasonable amount of effort to measure it directly with the DSP. Interrupt times can make it very difficult to measure with the needed speed and/or precision. It is possible to obtain the amplitude of the resonant current by measuring the phase and resonant currents and subtracting them from each other. Typical boost times are well below 15 µs. An implementation of a detection algorithm in software would delay the result for too long and the current would increase far over the desired limits. Since the FPGA is much faster compared to the DSP interrupt sequence, the approach here is to embed the function in an analogous platform.

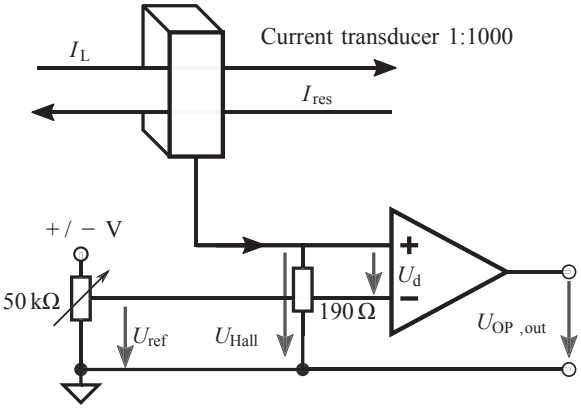


Fig. 13. Schematic of the analogue part on the current comparator PCB.

The basic principle can be described as depicted in Fig. 4 on the right side and Fig. 13 respectively. Hall-based current transducers transform the auxiliary current and the load current in such a way that the fields within the sensor compensate. With a ratio of 1:1000, the current is injected into a high-precision measuring resistors causing a voltage drop equivalent to the boost current. The resistor is connected to an operational amplifier with a high differential voltage capability. This voltage is then compared to a reference created by a variable voltage divider. Whenever the comparator detects a voltage U_{Hall}, representing the boost current $I_{boost} = I_{res} - I_L$, higher than the reference voltage, the main switch is turned off. This initiates the resonant commutation as stated in Fig. 5. The amplitude of the boost current can be adjusted by setting the reference voltage to the desired value. The reference voltage represents the minimum current $|I_{min}|$ which is needed to allow a commutation within a specified time as explained in [8]. As shown in Fig. 2, the dead time must be compensated since the main switch turn-off is delayed compared to a fixed boost time control, effecting the turn on of its complementary switch. Additionally, the delays introduced by this PCB have to be taken into account. Again, a chain of delays caused by the operational amplifier, fiber optic I/O, FPGA computation time and the turn off time of the main switch t_{IGBT} can be observed. For this application, the delay of the main switch is the major contributor to the overall delay. Note that an increased delay causes an extended magnetization time and, therefore, a tremendously increased boost current.

V. Experimental Results

In Fig. 9 and Fig. 10, the experimental results are summarized.

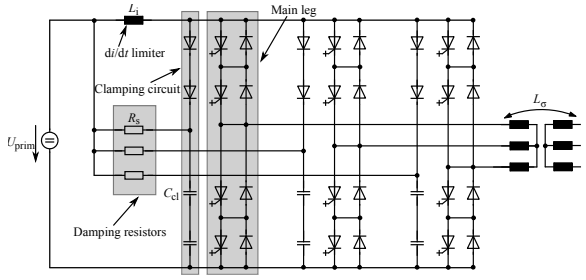


Fig. 14. Conventional snubbers for IGCT-based converters.

TABLE III
COST COMPARISON OF CONVENTIONAL IGCT SNUBBERS CIRCUIT AND ARCP SNUBBERS

	Component	No. of Dev.	Est. Price
Conventional Snubber	d*i*/d*t* limiter	2	12.5 t€
	Clamping diode	12	8.4 t€
	Clamping capacitor	12	4.8 t€
	Damping resistor	6	3.6 t€
ARCP Snubber	Snubber capacitor	48	1.5 t€
	Auxiliary inductor	2	1.6 t€
	Auxiliary switch (IGBT)	12	15.6 t€
	Radiators for IGBTs	12	1.1 t€
	GDUs IGBTs	12	0.96 t€
	ZVD PCB	12	0.5 t€
	ZCD PCB	12	0.8 t€
	Hall-based sensors	12	1.2 t€
	Total amount		−6.0 t€

In Fig. 9(a) and (b), the main operation of the converter is shown. Beginning with the start of the converter, the steady-state voltages and the resonant currents are shown in Fig. 9(a). Whenever a phase-shift is applied, the load current and the resonant current are added up as it can be observed at t = 200 µs and t = 700 µs in Fig. 9(b). In Fig. 10(a), a detailed voltage commutation in a converter leg and the ZVD signals are shown. Fig. 10(b) and (c) show the ZVD. In Fig. 10(b) a high-voltage test has been conducted and the delay of about 1 µs can be achieved over a wide voltage range. To learn more about the total delay, detailed measurements are taken at lower voltages and plotted in Fig. 10(c). Measurements taken during tests of the constant boost current mode are depicted in Fig. 10(d)−(f).

These measurements show the successful application of the introduced control techniques on a small scale test bench and validate the simulations used to design the VHDL structures. Future measurements on the full scale DAB will provide insights on efficiency improvements achieved by these techniques.

Conventional systems using IGCTs need *RCD* snubbers and d*i*/d*t* limiter to fulfill the SOA of the IGCT devices as shown in Fig. 14. In the high-power setup, the applied IGCTs 5SHY35L4510 have d*i*/d*t* limitations of 800 A/µs. The modification from a classical clamping to an ARCP system will affect the number of used components. However, the conventional snubber systems are not needed anymore. In TABLE III a cost comparison between conventional snubber and usage of an ARCP with IGBTs as auxiliary switches is given. The table considers the investment costs of the three-phase high-power DAB converter. For conventional snubbers an investment of 29.3 t€ for the high-power setup is needed. The ARCP circuit requires an investment of 23.3 t€. Embedding the ARCP would result in 6.0 t€ savings, plus the efficiency improvements which will cumulate more savings over time. A big price difference can be seen between the d*i*/d*t* limiter, the auxiliary inductors and the switches. In conventional clamping circuit the d*i*/d*t* limiter must be rated for the total dc-link current in the existing high-power setup it is water-cooled resulting in an expensive design. The auxiliary resonant inductor is only rated for the rms current during the resonant phase.

VI. CONCLUSION AND OUTLOOK

The auxiliary-resonant commutated pole seems to be an interesting technique for reducing the switching losses of a high-power 5 MW dc-dc converter based on IGCTs. The basic control is explained using space vectors and the given timing constrains regarding the ARCP branch are introduced. As a four-quadrant switch either line-commutated or forced-commutated devices can be used. The modulation is verified in a small-scale setup with FPGA/DSP based controller. The two presented boosting strategies, constant magnetization time and constant boost current, are tested in the experimental setup and results are shown. For the ARCP concept a high-speed ZVD is design and explained with a delay of approximately 1.5 µs. To compensate the delay time analog tuning is necessary. Finally, the use of an ARCP to balance the dc-link capacitors is introduced, allowing the DAB converter to operate in bipolar systems with unbalanced loads. The small-scale dual-active bridge proves the proper functionality of the control techniques. The boosting strategies can be applied directly to the 5 MW converter. In the near future the developed control will be implemented in a high-power dc-dc converter and tested to show improvements in IGCT switching behavior and an increase in efficiency.

ACKNOWLEDGMENT

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An Adaptive Sliding Mode Control Scheme for Grid Integration of a PV System

Aurobinda Bag, Bidyadhar Subudhi, and Pravat Kumar Ray

***Abstract*—An Adaptive Sliding Mode Control (ASMC) algorithm is developed in this paper for grid synchronization of a photovoltaic (PV) system. This ASMC algorithm minimizes the difference between the reference inverter current and the actual inverter current of the grid connected PV system (GCPVS) during unbalanced loading, grid voltage distortion and variation in solar irradiance. The maximum output power from the PV panel is obtained using modified incremental conductance (IC) MPPT algorithm. Instantaneous power theory (IPT) is employed to transfer active power and reactive power between the PV system, grid and the non-linear load. The ASMC-IC-IPT control scheme is applied to a grid connected PV system firstly using simulation and then on a prototype experimental setup. The performance of ASMC-IC-IPT scheme is compared with that of sliding mode control (SMC)-IC-IPT scheme. From the obtained results, it is observed that ASMC-IC-IPT control scheme outperforms the SMC-IC-IPT control scheme during transient, steady state and dynamic loading conditions.**

***Index Terms*—Adaptive sliding mode control, grid synchronization, Lyapunov function, total harmonic distortion.**

I. Introduction

In view of the load disturbance and uncertainties in parameters e.g. voltage, current, resistance, inductance of a grid connected PV system, designing an appropriate control algorithm is important. Also a number of non-linear control algorithms have been proposed for a PV system such as Lyapunov based controller [1], two-loop controller, SMC controller [2]. Among the aforesaid non-linear control algorithms, SMC algorithm is popular due to its robustness in face of parametric uncertainties and load variations. However, the SMC algorithm yields chattering in the control signal resulting reduction in control accuracy and high heating losses in the power circuit [3]. Sliding mode observer based adaptive slip ratio control algorithm is proposed in [4] for a hybrid electric vehicle. In [5], the adaptive global fast terminal SMC using fuzzy neural network approaches are proposed for an H-bridge inverter. An adaptive fuzzy SMC [6] is proposed for a two stage single-phase grid connected PV system. An adaptive SMC is also developed for a single-phase grid connected PV system in [7].

The contribution of this paper lies in designing an ASMC-IC-IPT scheme for a three-phase grid connected PV system. The robustness of the ASMC-IC-IPT scheme is investigated over SMC-IC-IPT scheme. The performance of the ASMC-IC-IPT is evaluated in both simulation and an experimental setup with grid voltage distortion, load variation and change in solar irradiance.

The rest of the paper is organised as follows. The modified incremental conductance MPPT algorithm is presented in Section II. In Section III, the proposed adaptive SMC scheme is presented that considers uncertainties due to parameter variation and measurements. Section IV describes the instantaneous power theory to estimate the reference inverter current. In Section V , simulation results and discussion are presented. Section VI presents the experimental results with discussion. Section VII provides the conclusion of the paper.

II. Adaptive Sliding Mode Control Algorithm

The schematic diagram of a GCPVS is shown in Fig. 1. The nonlinear loads I and II are used to verify the performance of ASMC-IC-IPT scheme, as shown in Fig. 1. A modified IC MPPT algorithm is used to extract maximum power from PV panel [8].

A. Modeling of Grid Connected PV System

The dynamic model of the GCPVS can be derived using Fig. 1.

$$\frac{d}{dt}I_{cd} = \frac{1}{L_c}D_d V_{pv} - \frac{R_c}{L_c}I_{cd} + wI_{cq} - \frac{1}{L_c}V_{gd} \tag{1}$$

$$\frac{d}{dt}I_{cq} = \frac{1}{L_c}D_q V_{pv} - \frac{R_c}{L_c}I_{cq} - wI_{cd} - \frac{1}{L_c}V_{gq} \tag{2}$$

$$\frac{d}{dt}V_{pv} = \frac{1}{C_{dc}}I_{pv} - \frac{1}{C_{dc}}(D_d I_{cd} + D_q I_{cq}) \tag{3}$$

where, I_{cd}, I_{cq} are the d-q axis VSI currents, V_{gd}, V_{gq} are *d-q* axis grid voltages, D_d, D_q, are *d-q* axes duty cycle and w, represents the frequency of the grid voltage.

B. Assumptions

In the GCPVS, there may be some unpredictable electromagnetic interference during the operation which causes noise while measuring the parameters such as voltage, current through sensors. Also the parameters such as resistance, inductance of inverter interface may vary due to variation in ambient temperature and skin effect. To represent the actual value of these parameters e.g. voltage, current, resistance and inductance which are used by the controller, the following assumptions are taken.

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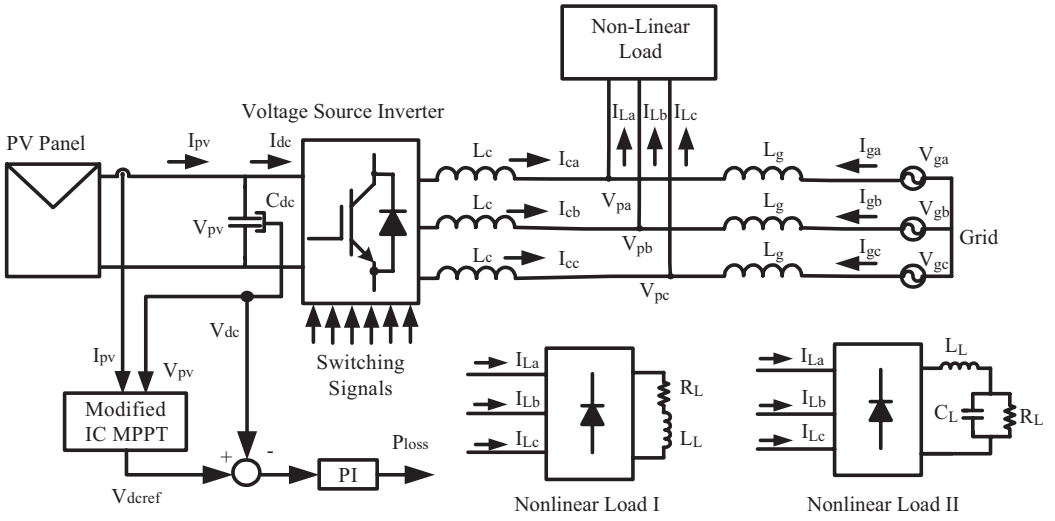


Fig. 1. Schematic Diagram for grid connected PV System.

$$|I_{cd} - I_{cd,\,meas}| \leqslant \Delta I_{cd}, I_{cd} \leqslant I_{cd,\,meas} + \Delta I_{cd} \tag{4}$$

$$|I_{cq} - I_{cq,\,meas}| \leqslant \Delta I_{cq}, I_{cq} \leqslant I_{cq,\,meas} + \Delta I_{cq} \tag{5}$$

$$\left| \frac{V_{gd}}{L_c} - \frac{V_{gd,\,meas}}{L_{c,\,meas}} \right| \leqslant \Delta \frac{V_{gd}}{L_c} \tag{6}$$

$$\left| \frac{V_{gq}}{L_c} - \frac{V_{gq,\,meas}}{L_{c,\,meas}} \right| \leqslant \Delta \frac{V_{gq}}{L_c} \tag{7}$$

$$|K_d e_d - K_d e_{d,est}| \leqslant K_d \Delta e_d \tag{8}$$

$$|K_q e_q - K_q e_{q,est}| \leqslant K_q \Delta e_q \tag{9}$$

$$|K_1 I_{cd} - K_{1,\,est} I_{cd,\,meas}| \leqslant \Delta K_1 I_{cd} \tag{10}$$

$$|K_2 I_{cq} - K_{2,\,est} I_{cq,\,meas}| \leqslant \Delta K_2 I_{cq} \tag{11}$$

where $R_{c,\,meas}$, $L_{c,\,meas}$, $I_{cd,\,meas}$, $I_{cq,\,meas}$, $V_{gd,\,meas}$, $V_{gq,\,meas}$ represent the measured values, $K_{1,est}$, $K_{2,est}$, $e_{d,est}$, $e_{q,est}$ represent the estimated values and ΔI_{cd}, ΔI_{cq}, $\Delta \frac{V_{gd}}{L_c}$, $\Delta \frac{V_{gq}}{L_c}$, Δe_d, Δe_q, $\Delta K_1 I_{cd}$, $\Delta K_2 I_{cq}$ are the uncertainties due to parametric variations and measurements.

C. Design of Adaptive Sliding Mode Control Scheme

It is intended to design an adaptive SMC algorithm such that tracking of the reference inverter current is achieved. It is necessary that the magnitude, phase and frequency of the actual inverter current should be equal to the reference inverter current. We choose sliding surfaces as follows

$$S = \begin{bmatrix} S_d \\ S_q \end{bmatrix} \tag{12}$$

where S_d, S_q denote sliding surfaces for d and q axes. In order to maintain the enhanced transient response and to reduce the steady state error, we introduce the integral forms as follows

$$\begin{bmatrix} S_d \\ S_q \end{bmatrix} = \begin{bmatrix} e_d + K_d \int_{-\infty}^{t} e_d(\tau) d\tau + e_{d0} \\ e_q + K_q \int_{-\infty}^{t} e_q(\tau) d\tau + e_{q0} \end{bmatrix} \tag{13}$$

where K_d, K_q are positive constants, e_{d0}, e_{q0} are initial errors between the reference and the actual d-q components of inverter current. e_d and e_q are defined as follows

$$e_d = I^*_{cd} - I_{cd},\ e_q = I^*_{cq} - I_{cq}$$

So $S_d = 0$ and $S_q = 0$ represent the precise tracking of d-q components of inverter current of GCPVS.

When the system state reaches the sliding manifolds, the structure of the feedback loop is adaptively altered to slide the system state along the sliding surface. The time derivative of (13) yields

$$\begin{aligned} \dot{S}_d &= \frac{d}{dt} S_d = \frac{d}{dt}(I^*_{cd} - I_{cd}) + K_d (I^*_{cd} - I_{cd}) \\ &= -K_{d1} sign(S_d) \\ \dot{S}_q &= \frac{d}{dt} S_q = \frac{d}{dt}(I^*_{cq} - I_{cq}) + K_q (I^*_{cq} - I_{cq}) \\ &= -K_{q1} sign(S_q)\ . \end{aligned} \tag{14}$$

Substituting (1) and (2) into (14), yields

$$\begin{aligned} \frac{d}{dt} S_d &= \frac{d}{dt} I^*_{cd} - \frac{1}{L_c} D_d V_{pv} + \frac{R_c}{L_c} I_{cd} - w I_{cq} \\ &\quad + \frac{1}{L_c} V_{gd} + K_d e_d \\ \frac{d}{dt} S_q &= \frac{d}{dt} I^*_{cq} - \frac{1}{L_c} D_q V_{pv} - \frac{R_c}{L_c} I_{cq} + w I_{cd} \\ &\quad + \frac{1}{L_c} V_{gq} + K_q e_q \end{aligned} \tag{15}$$

(15) can be rewritten as

$$\frac{d}{dt}S = F + DU_{dq} \tag{16}$$

where

$$F = \begin{bmatrix} F_d \\ F_q \end{bmatrix} = \frac{d}{dt}\begin{bmatrix} I_{cd}^* \\ I_{cq}^* \end{bmatrix} + \begin{bmatrix} \frac{R_c}{L_c} & -w \\ w & -\frac{R_c}{L_c} \end{bmatrix}\begin{bmatrix} I_{cd} \\ I_{cq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} & 0 \\ 0 & \frac{1}{L_c} \end{bmatrix}\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} + \begin{bmatrix} K_d & 0 \\ 0 & K_q \end{bmatrix}\begin{bmatrix} e_d \\ e_q \end{bmatrix},$$

$$D = \begin{bmatrix} -\frac{V_{pv}}{L_c} & 0 \\ 0 & -\frac{V_{pv}}{L_c} \end{bmatrix} \text{ and } \mathrm{U}_{dq} = \begin{bmatrix} D_d \\ D_q \end{bmatrix}.$$

The control law can be obtained as follows

$$U_{dq} = -D^{-1}\left\{\begin{bmatrix} F_{d,} \\ F_{q,} \end{bmatrix} + \begin{bmatrix} K_{d1} & 0 \\ 0 & K_{q1} \end{bmatrix}\begin{bmatrix} sign\,(S_d) \\ sign\,(S_q) \end{bmatrix}\right\} \tag{17}$$

The switching action in (17) may yield chattering owing to presence of sign functions. This can be minimized by introducing a boundary layer. This can be obtained by replacing the sign function by a saturation function *sat(S)* with narrow region of the sliding surface through which the discontinuities in the switching control action can be avoided.

$$sat(S) = \frac{S}{|S| + \lambda}$$

where $\lambda << |S|$ is a small positive gain i.e. the width of the boundary layer.

In order to make the SMC algorithm adaptive considering the uncertainties due to parametric variations and measurements as described in Section III-A, the control law can be derived as follows

$$U_{dq} = -D^{-1}\left\{\begin{bmatrix} F_{d,est} \\ F_{q,est} \end{bmatrix} + \begin{bmatrix} K_{d1} & 0 \\ 0 & K_{q1} \end{bmatrix}\begin{bmatrix} sat\,(S_d) \\ sat\,(S_q) \end{bmatrix}\right\} \tag{18}$$

where

$$F_{est} = \begin{bmatrix} F_{d,est} \\ F_{q,est} \end{bmatrix} = \frac{d}{dt}\begin{bmatrix} I_{cd}^* \\ I_{cq}^* \end{bmatrix} + \begin{bmatrix} K_{1,est} & -w \\ w & K_{2,est} \end{bmatrix}\begin{bmatrix} I_{cd} \\ I_{cq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} & 0 \\ 0 & \frac{1}{L_c} \end{bmatrix}\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} + \begin{bmatrix} K_d & 0 \\ 0 & K_q \end{bmatrix}\begin{bmatrix} e_d \\ e_q \end{bmatrix},$$

$$D = \begin{bmatrix} -\frac{V_{pv}}{L_c} & 0 \\ 0 & -\frac{V_{pv}}{L_c} \end{bmatrix} \text{ and } \mathrm{U}_{dq} = \begin{bmatrix} D_d \\ D_q \end{bmatrix}.$$

Accordingly the tunning law for *d*-axis can be derived as follows

$$\dot{K}_{1,\,est} = \frac{I_{cd,\,meas}S}{\alpha} \tag{19}$$

and for *q*-axis (see the Appendix) is as follows

$$\dot{K}_{2,\,est} = \frac{I_{cq,\,meas}S}{\alpha} \tag{20}$$

where $K_1 = \frac{R_c}{L_c}$. The sensitivity of the controlled system to variation of uncertainties and external disturbances still exists in the reaching phase, before sliding mode occurs, which means that the loss of robustness in the transient state. To guarantee the sliding mode at the initial time instant, the initial conditions of the integrators should be chosen as

$$I_{d0} = \frac{-e_{d0}}{K_d} \text{ and } I_{q0} = \frac{-e_{q0}}{K_q} \tag{21}$$

where I_{d0} and I_{q0} are the initial conditions of the integrator defined as

$$I_{d0} = \int_{-\infty}^{0} e_d(\tau)\,d\tau,\; I_{q0} = \int_{-\infty}^{0} e_q(\tau)\,d\tau \tag{22}$$

Hence at $t = 0$

$$S_{d0} = e_{d0} + K_d I_{d0} = 0 \tag{23}$$

$$S_{q0} = e_{q0} + K_q I_{q0} = 0 \tag{24}$$

(23) and (24) imply that the system states are on the sliding surfaces at the initial time instant without the reaching phase, and the complete robustness can be obtained during the entire response. Fig. 2 shows the structure of the proposed ASMC employed with the instantaneous power theory for the GCPVS. The reference active power and reactive power for VSI are calculated using the instantaneous power theory. Then the reference inverter current is calculated using (32) and (33). After implementation of ASMC, the required gate signal is generated using (18), which is applied to the VSI.

III. Reference Current Generation for VSI

We employed IPT and power balance to generate the reference current for VSI. The α, β components of grid voltage, grid current and load current can be calculated using Clarke transformation as follows

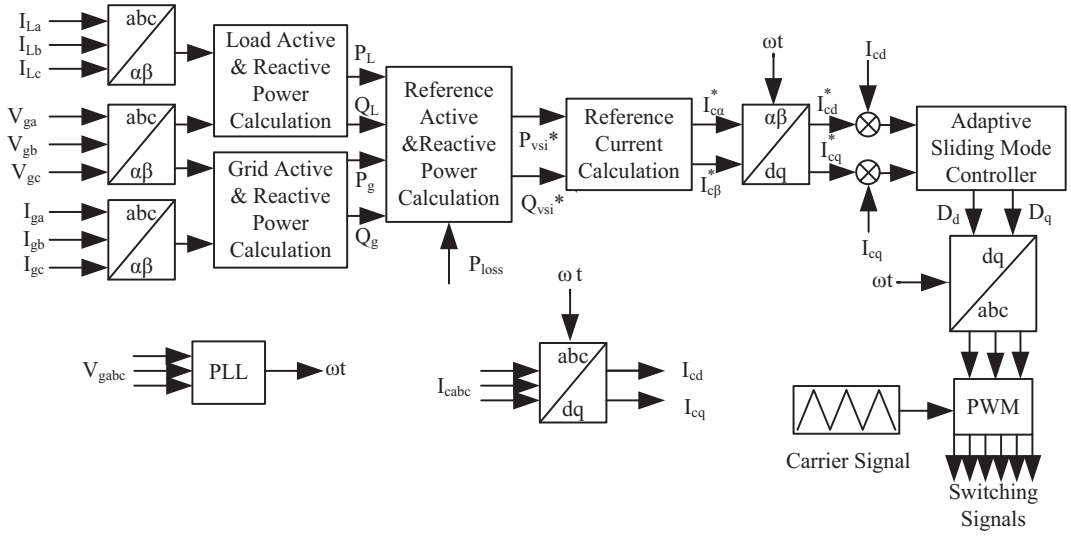


Fig. 2. Structure of adaptive SMC algorithm for a grid connected PV System.

$$\begin{bmatrix} V_{g\alpha} \\ V_{g\beta} \end{bmatrix} = M \begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} \tag{25}$$

$$\begin{bmatrix} I_{L\alpha} \\ I_{L\beta} \end{bmatrix} = M \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{26}$$

$$\begin{bmatrix} I_{g\alpha} \\ I_{g\beta} \end{bmatrix} = M \begin{bmatrix} I_{ga} \\ I_{gb} \\ I_{gc} \end{bmatrix} \tag{27}$$

where, $M = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$

The load active and reactive power is calculated using (28) as follows

$$\begin{bmatrix} P_L \\ Q_L \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix}. \tag{28}$$

The real power and reactive power of the load comprises of an average component (*superscript* $^-$) and an oscillating component (*superscript* $^\sim$). The oscillating component of power can be obtained using a low pass filter (LPF) [9].

$$\begin{aligned} P_L &= \bar{P}_L + \tilde{P}_L \\ Q_L &= \bar{Q}_L + \tilde{Q}_L . \end{aligned} \tag{29}$$

The dc link capacitor voltage of VSI is measured at the time of operation of VSI. A PI-controller is employed to regulate the dc link voltage. The reference dc link voltage is obtained as the output of the modified IC MPPT algorithm. The output from the PI-controller represents as power loss (P_{loss}) which flows to (from) the capacitor C_{dc} to keep the dc link capacitor voltage at a fixed value. The utility active power can be calculated as follows.

$$P_g = V_{g\alpha} I_{g\alpha} + V_{g\beta} I_{g\beta} . \tag{30}$$

If the (P_{loss}) is supplied by the PV panel, then the reference real and reactive power for inverter is calculated as follows

$$P^*_{vsi} = P_L - \bar{P}_g + \bar{P}_{loss} \tag{31}$$

$$Q^*_{vsi} = Q_l .$$

Accordingly the reference d-q component of inverter current can be estimated by following equations.

$$\begin{bmatrix} I^*_{c\alpha} \\ I^*_{c\beta} \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix}^{-1} \begin{bmatrix} P^*_{vsi} \\ Q^*_{vsi} \end{bmatrix} \tag{32}$$

$$\begin{bmatrix} I^*_{cd} \\ I^*_{cq} \end{bmatrix} = \begin{bmatrix} \cos\varphi & \sin\varphi \\ -\sin\varphi & \cos\varphi \end{bmatrix} \begin{bmatrix} I^*_{c\alpha} \\ I^*_{c\beta} \end{bmatrix} . \tag{33}$$

TABLE I
PARAMETERS FOR ASMC SCHEME

Parameter	Value	Parameter	Value
K_d	100	K_q	100
K_{d1}	1000	K_{q1}	1000

IV. SIMULATION RESULTS

The simulation is performed for GCPVS using both non-linear load I and II with ASMC-IC-IPT scheme shown in Fig. 1 in MATLAB/SIMULINK. The performance of ASMC-IC-IPT scheme is compared with that of the SMC-IC-IPT scheme [8] and summarized in Section V-C. The parameters used for the PV system are given in [8]. The control parameters are given in TABLE I.

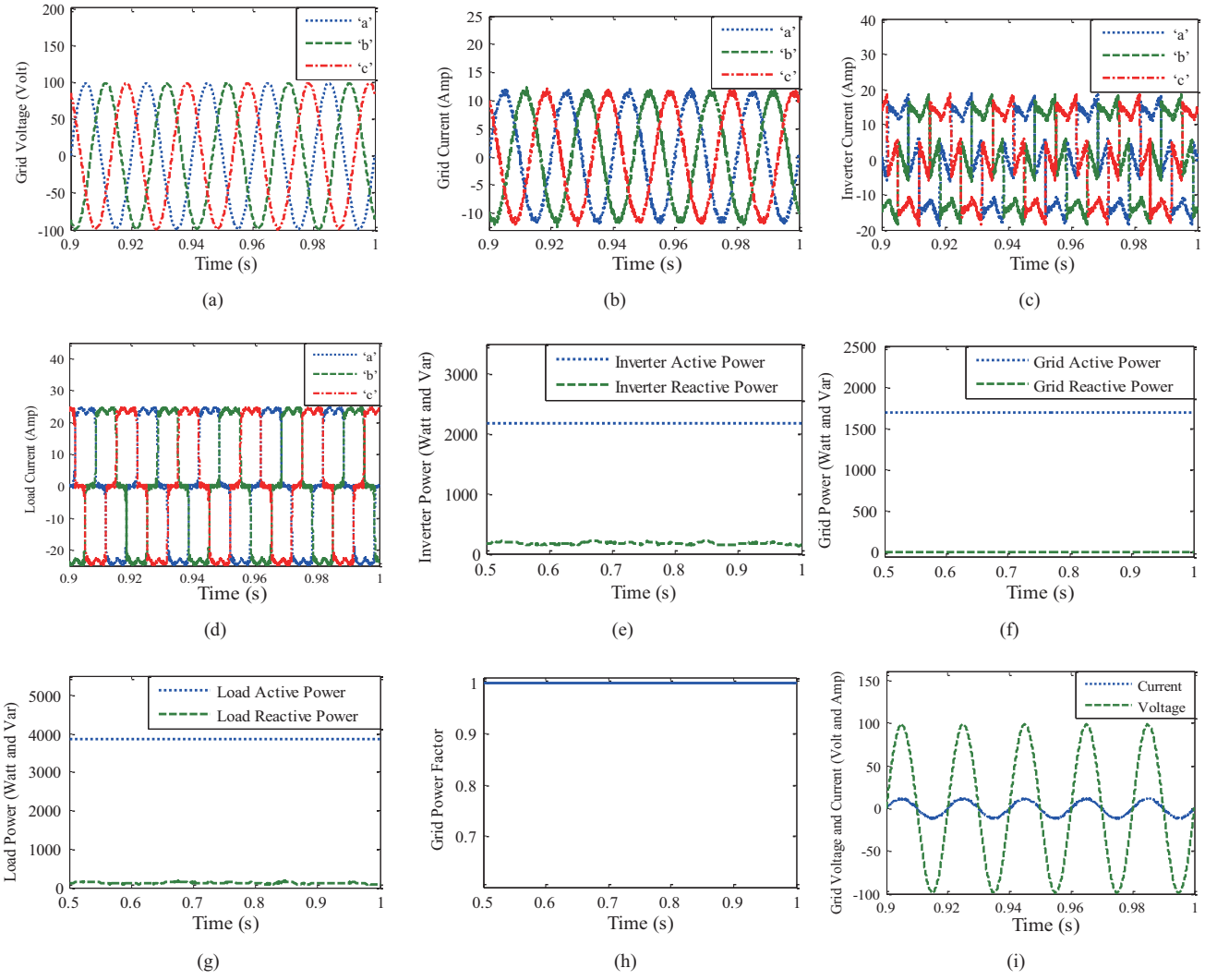


Fig. 3. Steady state performance of ASMC-IC-IPT using non-linear load I and ideal grid (with out grid voltage distortion) condition: (a) Grid voltage. (b) Grid current. (c) Inverter current. (d) Load current. (e) Inverter power. (f) Grid power. (g) Load power. (h) Grid power factor. (i) Grid voltage and current for phase 'a'.

A. Performance of the Proposed ASMC-IC-IPT Using Non-Linear Load I

The simulated performance of the proposed ASMC-IC-IPT scheme using non-linear load I (Fig. 1) is shown in Fig. 3. The three-phase grid voltage V_{ga}, grid current I_{ga}, inverter current I_{ca} and load current I_{La} for ASMC-IC-IPT scheme are shown in Fig. 3(a), (b), (c) and (d). From Fig. 3(b), (c) and (d), it can be observed that, the total load current, 26.6 A is the summation of PV-VSI current, 15.1 A and the grid current, 11.5 A. The total load active power, 3.9 kW, is the addition of PV-VSI output power, 2.2 kW and the grid power, 1.7 kW, which is seen from Fig. 3(e), (f), and (g). The load reactive power, 200 VARs is supplied by PV-VSI system. Therefore, the grid power factor as shown in Fig. 3(h) is unity. The grid voltage and current for phase 'a' are in the same phase, which is seen from Fig. 3(i).

B. Performance of the proposed ASMC-IC-IPT Using Non-Linear Load II

The performance for ASMC-IC-IPT scheme using non-linear load II (Fig. 1) is shown in Fig. 4. The three-phase grid current, grid voltage and current for phase 'a' and grid current THD are shown in Fig. 4(a), (b) and (c) respectively. It is seen from Fig. 4(c) that, the THD of grid current obtained in ASMC-IC-IPT scheme using non-linear load II is 2.82%, which is slightly more than that obtained from Fig. 6(b) using non-linear load I. This may be due to inclusion of capacitor in the nonlinear load II.

C. Performance of the ASMC-IC-IPT Under Grid Distortion

The simulation results for ASMC-IC-IPT scheme under grid voltage distortion are shown in Fig. 5. In Fig. 5(a), (b)

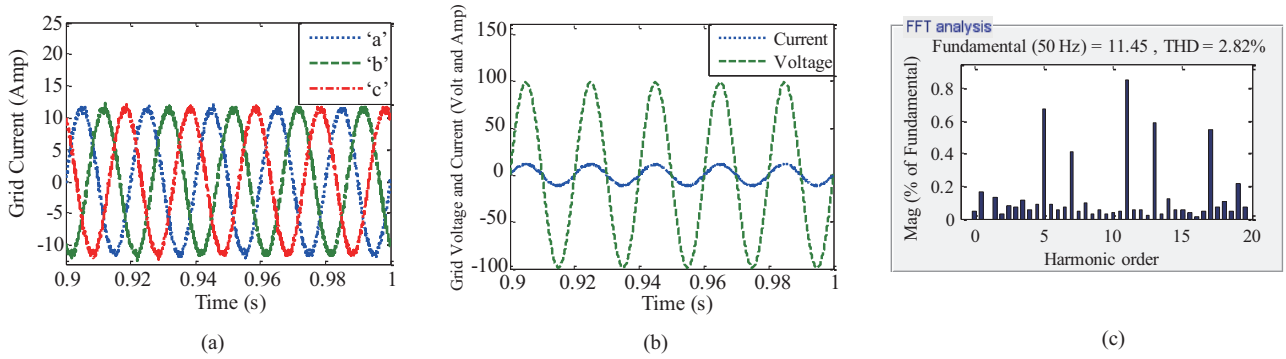


Fig. 4. Steady state performance of ASMC-IC-IPT using non-linear load II and ideal grid (with out grid voltage distortion) condition: (a) Grid current. (b) Grid voltage and current for phase 'a'. (c) Grid current THD.

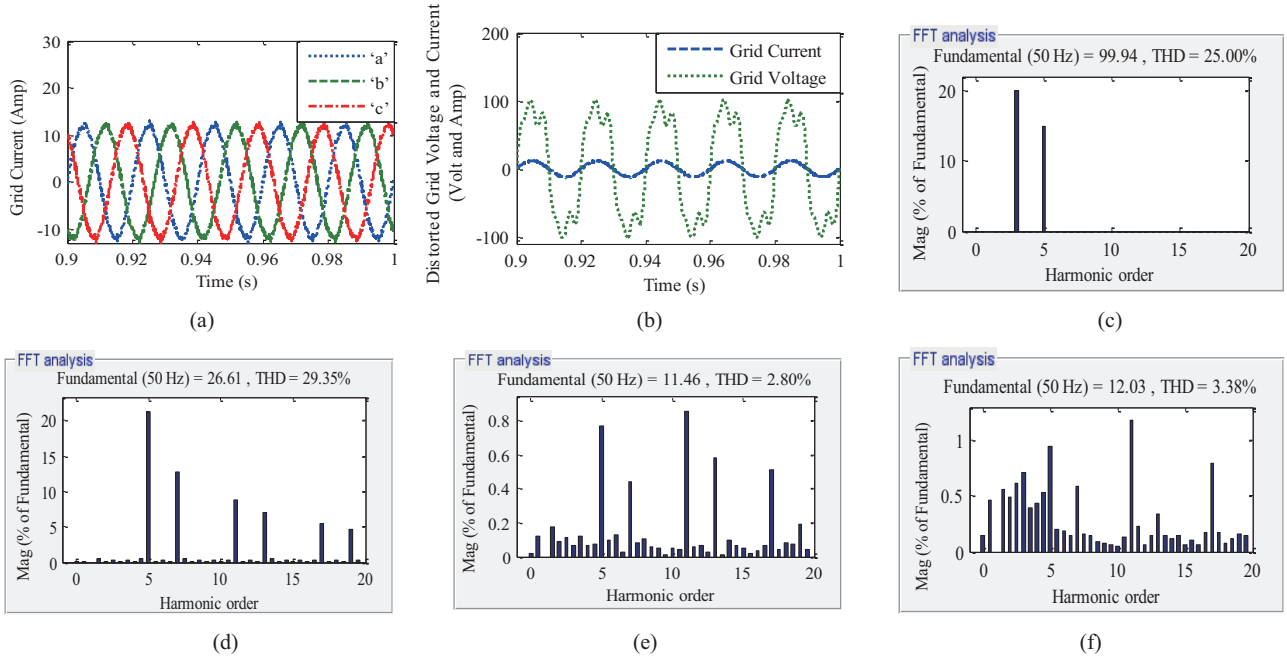


Fig. 5. Steady state performance of ASMC-IC-IPT and SMC-IC-IPT algorithm under grid voltage distortion: (a) Grid current. (b) Grid voltage and current for phase 'a'. (c) Grid voltage THD. (d) Load current THD. (e) Grid current THD using ASMC-IC-IPT. (f) Grid current THD using SMC-IC-IPT.

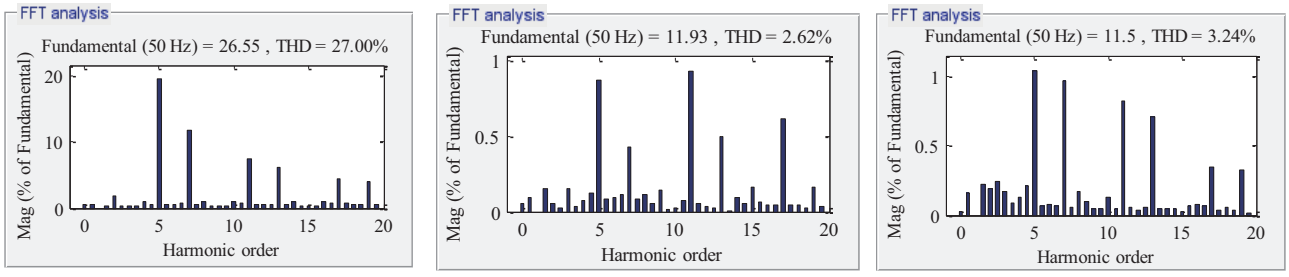
and (c) the 3-phase grid current, grid voltage and current for phase 'a' and the THD of distorted grid voltage is shown. The ASMC-IC-IPT scheme reduces the grid current THD from 29.35% to 2.80% and the SMC-IC-IPT scheme reduces the grid current THD to 3.38%.

D. Comparison Between the ASMC-IC-IPT and SMC-IC-IPT Schemes

The THD of grid current and load current using the proposed ASMC-IC-IPT scheme are 2.62% and 27% and that of SMC-IC-IPT scheme is 3.24%, which can be observed from Fig. 6(a), (b), and (c) respectively. The steady state response of grid current of ASMC-IC-IPT and SMC-IC-IPT scheme under ideal grid (without grid voltage distortion) are shown in Fig. 7(a). From Fig. 7(a) it is observed that, the grid current is made sinusoidal in 0.055 s using ASMC-IC-IPT scheme, but it takes 0.08s in SMC-IC-IPT scheme. The ASMC-IC-IPT scheme shows fast response to that of SMC-IC-IPT scheme under steady state condition. The transient response of grid current of ASMC-IC-IPT and SMC-IC-IPT scheme is compared in Fig. 7(b). The response of grid current is shown during the time, the load current of phase 'a'is disconnected from 0.5s to 0.51s. The grid current is made sinusoidal instantly (just after connected to the load of phase 'a') using ASMC-IC-IPT scheme, but it takes 0.01 s to that of SMC-IC-IPT scheme. So it is observed that in ASMC-IC-IPT scheme, the grid current adaptively made sinusoidal just after connection of the load of phase 'a'.

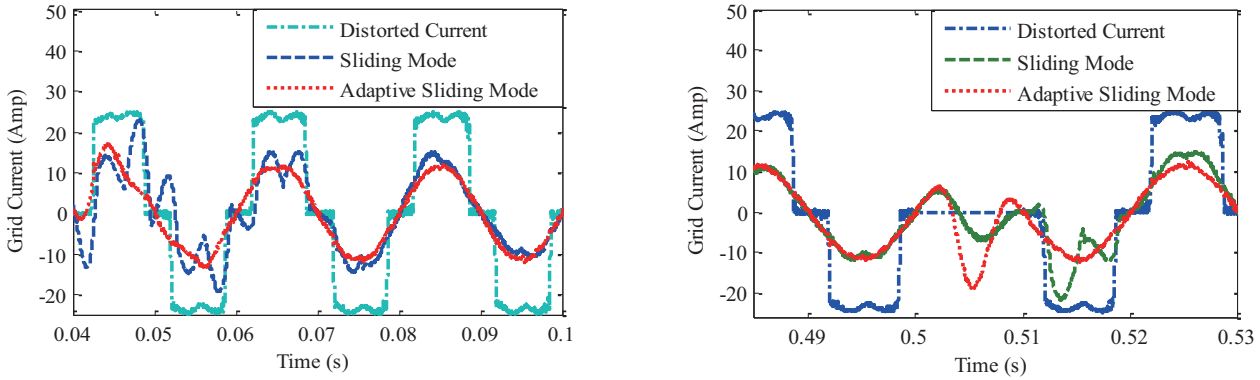
V. Experimental Results

The output power of solar simulator is fixed at 100 W. The dc capacitor voltage is kept at 100 V fixed. The parameters used in the experimental setup are given in [8]. The picture of the experimental setup is shown in [8]. Performance



(a) (b) (c)

Fig. 6. Steady state performance comparison of ASMC-IC-IPT and SMC-IC-IPT: (a) Load current THD. (b) Grid current THD using ASMC-IC-IPT. (c) Grid current THD using SMC-IC-IPT.



(a) (b)

Fig. 7. Comparison of performance between ASMC-IC-IPT and SMC-IC-IPT: (a) Steady state grid current performance. (b) Grid current transient performance during disconnection of load current for phase 'a'.

evaluation of the the modified IC algorithm was done for two cases, e.g. at 700 W/m^2 and 1000 W/m^2. In both the cases 98% MPPT efficiency is achieved.

A. Transient Performance of ASMC-IC-IPT

The dynamic performance of ASMC-IC-IPT scheme using non-linear load I is shown in Fig. 8. Fig. 8(a) shows the grid voltage v_{ga}, grid current i_{ga}, load current i_{La}, inverter current i_{ca} of ASMC-IC-IPT scheme when non-linear load is added to phase 'a'. It can be observed from Fig. 8(a) that, the grid current is sinusoidal even during the addition of non-linear load of phase 'a'. Fig. 8(b) shows the grid voltage v_{ga}, grid current i_{ga}, load current i_{La}, inverter current i_{ca} of ASMC-IC-IPT scheme when there is a change in dc side resistance of non-linear load I. It can be observed from Fig. 8(b) that grid current, inverter current and load current change smoothly with the change in load resistance.

B. Performance comparison of ASMC-IC-IPT and SMC-IC-IPT scheme

The performance of ASMC-IC-IPT scheme is compared with that of the experimentation obtained from the SMC-IC-IPT scheme. From Fig. 9(b), it can be observed that the dc capcitor voltage obtained from the SMC-IC-IPT scheme contains 5 V ripple. But 0.5 V ripples appeared in the case of ASMC-IC-IPT scheme as shown in Fig. 9(a). It can be observed from Fig. 10(a) and (b) that, there is 5% overshoot in grid current i_{ga} using ASMC-IC-IPT scheme and 25% overshoot occurs in grid current i_{ga} using SMC-IC-IPT scheme, when the APF is switched on.

C. Performance of the Control Schemes

SMC-IC-IPT: Time taken for grid current to make sinusoidal (during load disconnection): 0.01s, Time taken for grid current to make sinusoidal (under steady state): 0.09s, Grid current THD (in %) under steady state with ideal grid (simulation): 3.24%, Grid current THD (in %) under steady state with grid voltage distortion (simulation): 3.38. Grid current THD (in %) under steady state with ideal grid (experimental): 3.6%, % of overshoot occured in grid current at the time of switching on the APF (experimental): 5%, Presence of ripple in dc link voltage (experimental) in volt: ±5 V.

ASMC-IC-IPT: Time taken for grid current to make sinusoidal (during load disconnection): 0.003s, Time taken for grid current to make sinusoidal (under steady state): 0.06s, Grid current THD (in %) under steady state with ideal grid (simulation): 2.62%, Grid current THD (in %) under steady state with grid voltage distortion (simulation): 2.80, Grid current THD (in %) under steady state with ideal grid (experimental): 2.9%, % of overshoot occured in grid current at the time of

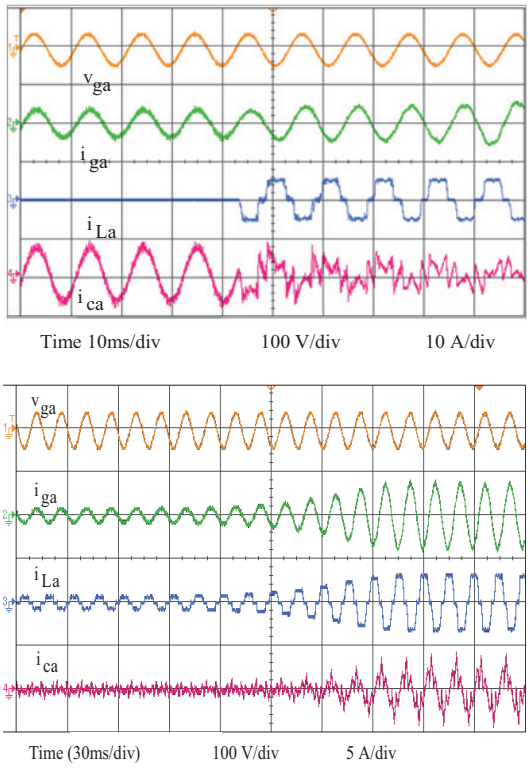


Fig. 8. Transient performance of ASMC-IC-IPT scheme during dynamic loading: (a) Performance during disconnection of load of phase 'a'. (b) Performance during change in dc side resistance of non-linear load I.

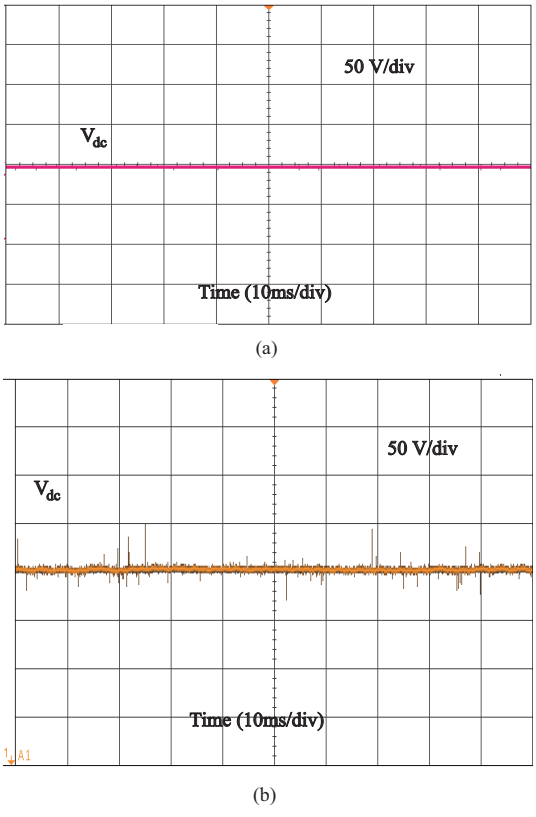


Fig. 9. Comparison of dc link voltage between ASMC-IC-IPT and SMC-IC-IPT scheme: (a) DC link voltage for ASMC-IC-IPT. (b) DC link voltage for SMC-IC-IPT.

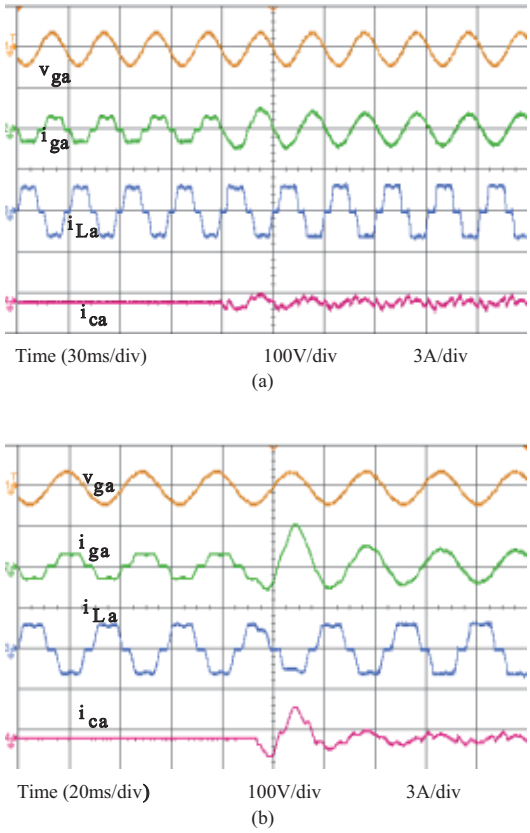


Fig. 10. Comparison of response between ASMC-IC-IPT and SMC-IC-IPT scheme when active power filter is switched on: (a) Grid voltage v_{ga}, grid current i_{ga}, load current i_{La}, inverter current i_{ca} of ASMC-IC-IPT. (b) Grid voltage v_{ga}, grid current i_{ga}, load current i_{La}, inverter current i_{ca}, of SMC-IC-IPT.

switching on the APF (experimental): 5%, Presence of ripple in dc link voltage (experimental) in volt: ±0.5 V.

VI. Conclusions

We proposed a new ASMC-IC-IPT controller for grid synchronization of a PV system, which involves a modified IC MPPT algorithm, to obtain max power from the PV panel during change in solar irradiance. Instantaneous power theory and power balance control theory are used to generate the reference inverter current. The simulation and experimental results of the proposed ASMC-IC-IPT scheme are compared with that of SMC-IC-IPT scheme. From the above results, it is observed that the proposed ASMC-IC-IPT control scheme exhibits robust and fast response even when there is distortion in the grid voltage, change in solar irradiance and dynamic loading conditions. This proposed controller also exhibits superior performance when compared with SMC-IC-IPT controller in terms of reduced overshoot in grid current waveform (25% to 5%) and ripples in dc capacitor voltage (5 V to 0.5 V) using the experimental setup. Further, the proposed controller is efficient to bring down the THD of grid current from 3.24% to 2.62% in simulation (without grid voltage distortion), 3.38% to 2.80% (with grid voltage distortion) and 3.6% to 2.9% (without grid voltage distortion) in the experimental setup. The grid current THD

is kept within the IEEE-519 standard.

Appendix

Considering the uncertainties due to parametric variations and measurements as described in section III-A, the SMC algorithm can be made adaptive by choosing a Lyapunov function as follows

$$V(t)=\frac{1}{2}S^2+\frac{1}{2}\alpha\left(K_1-K_{1,\,\mathrm{est}}\right)^2. \tag{34}$$

Taking time derivative of (34), we have

$$\dot{V}(t)=S*\dot{S}-\alpha\bar{K}_1\dot{K}_{1,\,\mathrm{est}} \tag{35}$$

where, $K_1-\dot{K}_{1,\,\mathrm{est}}=\widetilde{K}_1$

Taking $K_1=\frac{R_c}{L_c}$ and substituting (15) into (35) one can obtain

$$\dot{V}(t)=\mathrm{S}\begin{pmatrix}\frac{d}{dt}I_{cd}^{*}-\frac{1}{L_c}D_dV_{pv}+K_1I_{cd}\\-wI_{cq}+\frac{1}{L_c}V_{gd}+K_de_d\end{pmatrix}-\alpha\bar{K}_1\dot{K}_{1,\,\mathrm{est}} \tag{36}$$

Substituting (17) into (36), we have

$$\begin{aligned}\dot{V}(t)=S\Bigg[&\tfrac{d}{dt}I_{cd}^{*}-\left(\frac{V_{pv}}{L_c}\right)\left\{\left(\frac{L_{c,\,meas}}{V_{pv,\,meas}}\right)\left(\frac{d}{dt}I_{cd}^{*}\right.\right.\\&\left.+K_de_{d,\,meas}+K_{d1,\,\mathrm{est}}\,sign\left(S_d\right)\right)\\&\left.\left.+K_{1,\,\mathrm{est}}\,I_{cd,\,est}-wI_{cq,\,est}+\frac{V_{gd,\,meas}}{L_{cd,\,meas}}\right)\right\}\\&+KI_{cd}-wI_{cq}+\frac{V_{gd}}{L_c}+K_de_d\Bigg]-\alpha\widetilde{K}_1\dot{K}_{1,\,est}\end{aligned} \tag{37}$$

K_{d1} should be chosen that, the condition for SMC algorithm is satisfied, i.e.

$$\frac{1}{2}\frac{d}{dt}S^2\leqslant-\eta\left|S\right|. \tag{38}$$

So taking $\theta=m_{meas}m^{-1}$, K_{d1} can be obtained as follows

$$\begin{aligned}K_{d1}\geqslant(\theta-1)&\begin{pmatrix}K_{d,\,est}e_{d,\,est}\\+I_{cd}^{*}+\frac{V_{gd,meas}}{L_{c,meas}}\\-wI_{cq,\,meas}\\+K_{1,\mathrm{est}}I_{cd,\,meas}\end{pmatrix}\\&+\theta\begin{pmatrix}\eta+K_d\Delta e_d+\Delta\frac{V_{gd}}{L_c}\\-w\,\Delta I_{cq}+\Delta K_1I_{cd}\end{pmatrix}.\end{aligned} \tag{39}$$

The Lyapunov function will be negative definite if the tunning law for d-axis will be as follows

$$\dot{K}_{1,\,\mathrm{est}}=\frac{I_{cd,\,meas}S}{\alpha}. \tag{40}$$

Similarly taking $-\frac{R_c}{L_c}=K_2$ the value of K_{q1} can be obtained as follows

$$\begin{aligned}K_{q2}\geqslant(\theta-1)&\begin{pmatrix}K_{q,\,est}e_{q,\,est}\\+I_{cq}^{*}\\+\frac{V_{gq,\,meas}}{L_{c,\,meas}}\\-wI_{cd,\,meas}\\+K_{2,\,est}I_{cq,\,meas}\end{pmatrix}\\&+\theta\begin{pmatrix}\eta+K_q\Delta e_q+\Delta\frac{V_{gq}}{L_c}\\-w\Delta I_{cd}+\Delta K_2I_{cq}\end{pmatrix}.\end{aligned} \tag{41}$$

The Lyapunov function will be negative definite using the tunning law for q-axis as follows

$$\dot{K}_{2,\,est}=\frac{I_{cq,\,meas}S}{\alpha}. \tag{42}$$

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