Performance Degradation of GaN HEMTs Under Accelerated Power Cycling Tests

Chi Xu, Fei Yang, Enes Ugur, Shi Pu, and Bilal Akin

***Abstract*—In this paper, performance degradations of enhancement mode (E-mode) gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) under accelerated power cycling tests are presented. For this purpose, a DC power cycling setup is designed to accelerate the aging process in a realistic manner. In order to evaluate the aging-related parameter shifts and corresponding precursors, electrical parameters are periodically monitored through a high-end curve tracer. Both the cascode device and *p*-GaN gate GaN devices are evaluated during these tests. In the experimental results, it is observed that the on-state resistance gradually increases in both devices. Meanwhile, the threshold voltage of the *p*-GaN gate GaN device gradually increases over the aging cycles and a remarkable variation in the transfer characteristics is observed. At the end of the tests, failure analyses are conducted on both devices. The cascode GaN devices show both short and open circuit failure modes, and a weak point in the drain-side bond wires is detected. For the *p*-GaN gate GaN device, the electrical parameter shifts indicate a possible gate degradation after the device is aged.**

***Index Terms*—Aging precursor, failure analysis, failure mode, failure model, GaN device, power cycling.**

I. Introduction

GALLIUM nitride (GaN) devices are one of the most promising power devices in high frequency, high efficiency and high power density power conversions [1], [2]. Compared to Si and SiC counterparts, GaN high-electron-mobility transistors (HEMTs) exhibit a better figure of merit. The GaN HEMTs can be categorized into normally-on and normally-off devices [3]. Normally-on GaN device is less desirable in power converters due to its reliability concerns. For normally-off GaN devices, there are several methods to implement, including recessed Schottky gate, *p*-GaN gate, plasma treatment under the gate and cascode structure [4]. Among them, the cascode GaN and *p*-GaN gate GaN are mainly applied in commercially available GaN devices as shown in Fig. 1.

Both these types of GaN devices show different characteristics from the conventional Si devices. For cascode GaN devices, there are two primary heat sources, i.e., the GaN HEMT and Si MOSFET devices. These two devices are purposely overlapped in the stacked-die package to reduce the package related parasitics [5]. However, this makes it more difficult to dissipate the heat compared to the conventional design where each die sits on the base plate. On the other side, for E-mode GaN HEMTs, since there is no wire and die attachment compared to the conventional wire bond process [6]–[12], the common failure regarding package, such as bond-wire cracks, lift-off and die attachment delamination won't be observed. Hence it is quite necessary to study the reliability of these newly developed devices [13].

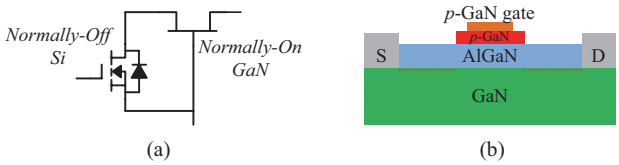


Fig. 1. Structure of GaN device: (a) Cascode GaN. (b) E-mode GaN.

Recent studies mainly focus on exerting stress directly on the device, including the high electric field, high temperature and high drain bias [14]–[18]. These stressors can result in current collapse [19], drain current degradation, threshold voltage shift and gate leakage current increase. To simulate the device's real operation in power converters, the device reliability under the power cycling test (PCT) is also studied. In [20], [21], the results show that the bond wire lift-off at the drain side of Cascode GaN (C-GaN) devices is the main cause of failure. In [22]–[24], both of the forward and reverse conduction operation modes of *p*-GaN gate GaN HEMTs are studied. There is no significant difference in the failure modes of these two operation conditions, and the common failure of the devices under test (DUTs) is solder delamination. In [20], similar results of *p*-GaN gate GaN devices are given, i.e., the solder joint delamination. However, comprehensive analysis of the static electrical parameter shifts throughout the aging process is not adequately addressed in the literature. This paper aims to evaluate the reliability of existing commercially available GaN devices by applying accelerated power cycling tests to mimic aging-related degradation. The investigation regarding the electrical parameters' change throughout the aging process is provided to identify the aging precursors, which can be used to prevent costly shutdowns and realize device condition monitoring.

The paper is organized as follows: in Section II, a power cycling test setup is designed and its operation principle is briefly discussed. With the proposed test setup, power cycling is implemented and the electrical parameter variations throughout the aging process are provided in Section III. In Section IV,

Manuscript received November 12, 2018. This work was supported in part by the Office of Naval Research under award number N00014-15-1-2325 and in part by the Semiconductor Research Corporation (SRC)/Texas Analog Center of Excellence (TxACE) under the Task ID 2712.026.

The authors are with the Department of Electrical and Computer Engineering, University of Texas at Dallas, Richardson, USA (e-mail: Chi.Xu212@utdallas.edu; Fei.Yang1@utdallas.edu; exu150130@utdallas.edu; Shi.Pu@utdallas.edu; Bilal.Akin@utdallas.edu).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00027

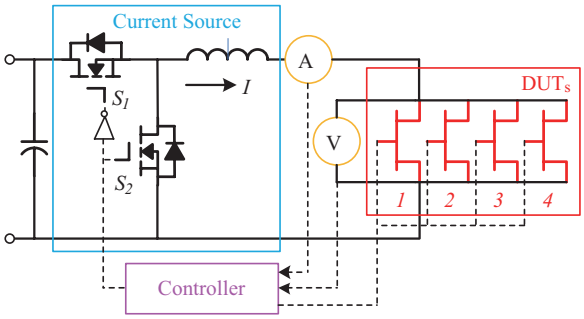


Fig. 2. Schematic overview of the accelerated aging test setup.

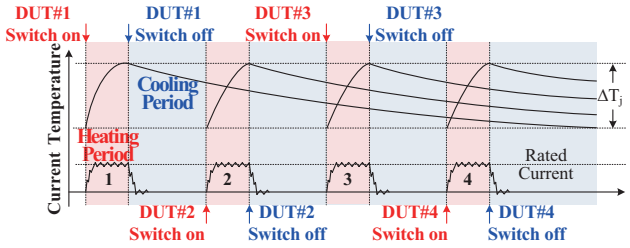


Fig. 3. Switching sequence of the test setup.

physical inspections are provided to investigate the causes of failures and discussions are given regarding parameter variations. Finally, the conclusions are provided in Section V summarizing the experimental results.

II. Accelerated Aging Test Setup

Power cycling test is commonly used to accelerate the aging process, which can trigger various failure mechanisms due to junction temperature swings, sheer stress, thermal expansion coefficient mismatch and enables aging precursors identification for health monitoring and lifetime estimation. In [22], a constant current is injected into the DUT by controlling a MOSFET. A bypass MOSFET is paralleled with the DUT branch for current free-wheeling. However, the current source is not fully used as it heats up the bypass MOSFET during the cooling period. To increase the utilization of the current source, a new power cycling test setup is designed to heat up all the DUTs sequentially.

The circuit diagram of the system is shown in Fig. 2, and it consists of five parts: a current source (CS), a DSP controller, a measurement board, a temperature controlled cold-plate and the DUTs. Among them, the output capacitor-less buck converter is applied as a current source for actively heating up the devices. Specifically, when one of the DUTs is turned on, S_2 is kept in off-state, and the duty cycle of high side switch S_1 is adjusted to regulate the load inductor's current to the rated current value of the DUT. The current value of the inductor is measured through a current sensor for feedback control. As the DUT is heated up by the inductor's current, the junction temperature is estimated through one of the temperature sensitive electrical parameters, i.e., the on-state resistance, which is calculated in real time with the measured drain-to-source voltage and the drain current. When the junction temperature of DUT reaches

TABLE I
Specification of Aging Test Setup

Item	Value
CS MOSFET	40 V/100 A
CS Inductor	40 μH
Maximum Junction Temperature	150 °C
Heat Sink Temperature	25 °C

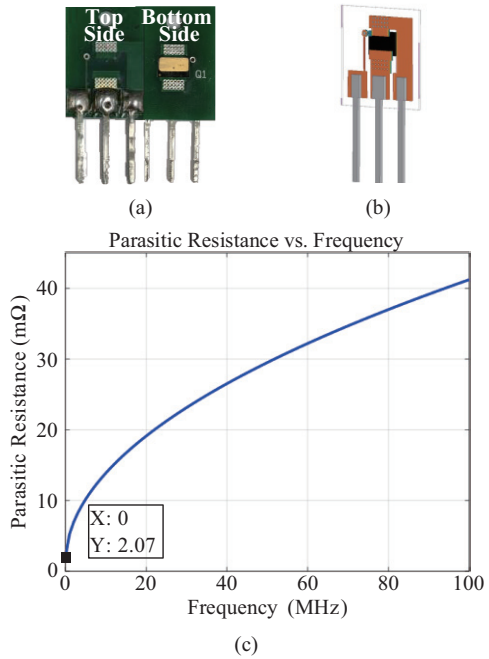


Fig. 4. TO-package adaptor: (a) PCB. (b) Q3D model. (c) Parasitics resistance vs. frequency.

the maximum temperature limit of 150 °C, the current is set to zero immediately. Here, the temperature is kept within SOA to avoid triggering unrealistic aging modes. When the inductor current becomes low, the DUT is turned off for cooling down to the cold plate temperature, i.e., 25 °C. The remaining small current ripple, as shown in Fig. 3, is dissipated by the output capacitance C_{oss} and the body diode of low side switch S_2. While cooling down the previous DUTs, the next DUT is heated up. The switching sequence is given in Fig. 3 and the detailed specifications are listed in TABLE I.

In order to measure the device's parameters on the curve tracer, a dedicated TO-247 PCB adaptor is designed as shown in Fig. 4(a). The adaptor model is imported to Ansys Q3D as shown in Fig. 4(b), and the added resistance of the PCB adaptor is simulated to be 2.07 mΩ at DC as indicated in Fig. 4(c). This value is negligible on the device's parameter measurement. Fig. 5 shows the system hardware and the devices with the adaptor mounted on the cold-plate are given in the zoomed-in box.

III. Parametric Analyses of Thermally Aged GaN Devices

In this study, 650 V cascode [25] and 650 V *p*-Gate gate

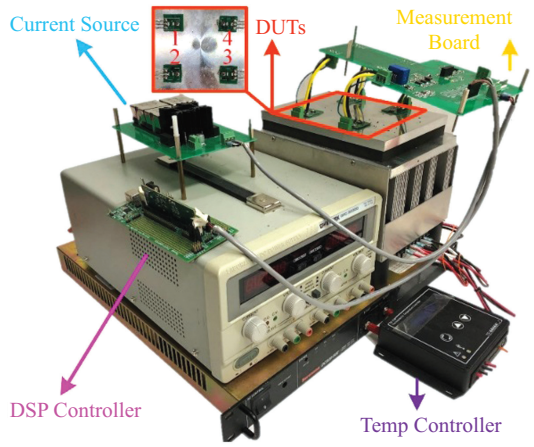


Fig. 5. Accelerated aging test setup hardware.

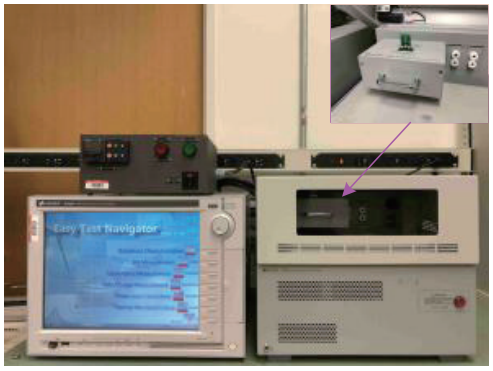


Fig. 6. Photo of the B1506A curve trace.

device [26] are used. The electrical parameters such as the gate-source leakage current I_{gss}, the drain-source leakage current I_{dss}, the threshold voltage V_{th}, the on-state resistance $R_{ds,on}$, the device capacitances (C_{iss}, C_{oss}, C_{rss}), the transfer characteristics (I_d-V_{gs}) and the output characteristics (I_d-V_{ds}), are periodically measured over the aging cycles with the Keysight B1506A curve tracer as shown in Fig. 6. In the following sections, the parameter shifts of each device are presented in detail.

A. Gate-to-Source Leakage Current I_{gss}

I_{gss} is measured by applying 15 V voltage on gate-source to the cascode GaN and 5 V voltage to the *p*-GaN device. The gate leakage current versus the number of power cycles is plotted for the cascode and *p*-GaN device respectively in Fig. 7(a) and (b).

Before the devices are aged, I_{gss} is very low, i.e., a maximum of 50 pA for cascode GaN and 50 μA for the *p*-GaN device. After certain aging process, I_{gss} of C-GaN 2, 3 and E-mode GaN (E-GaN) 2, 3 reach the compliance value of 1 mA. There is no gradual increase of I_{gss} before the device fails. Therefore, it is difficult to rely on the I_{gss} change as an aging precursor to predict the device's remaining useful lifetime. In fact, a high gate leakage current increase in the cascode GaN device suggests a failure in the Si MOSFET.

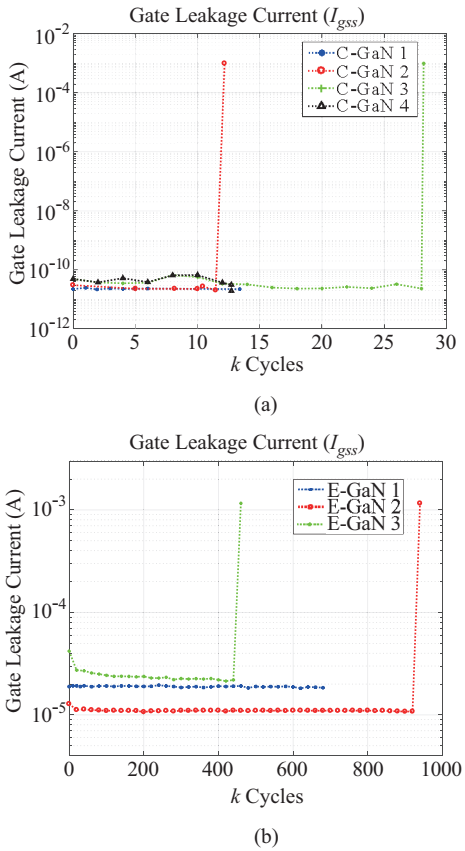


Fig. 7. Gate leakage current change during the aging process: (a) Cascode GaN. (b) E-mode GaN.

B. Drain-to-Source Leakage Current I_{dss}

I_{dss} is defined as the drain leakage current when the rated voltage is applied to the drain-source. As shown in Fig. 8, initially I_{dss} of cascode GaN and *p*-GaN device are also very low, i.e., a maximum of 40 μA for cascode GaN and less than 1 μA for the *p*-GaN device. Similar to the gate leakage current change, the I_{dss} of C-GaN 2, 3 reaches the compliance value of 400 μA and loses the blocking voltage ability. For the cascode device, since two devices are in series, it is necessary to decapsulate the device to find out the root cause of the failure, which is discussed later in the failure analysis.

For the *p*-GaN device, the leakage current of E-GaN 2, 3 reaches the compliance value of 40 μA after certain aging cycles and also loses the blocking ability. Similar to the gate leakage current, the drain leakage current does not gradually increase which makes it non-ideal for aging detections.

C. Threshold Voltage V_{th}

V_{th} is defined as the minimum gate-source voltage that is needed to create a drain current conducting between the drain and source terminals, i.e., 250 μA for cascode GaN and 7 mA for the *p*-GaN device. Fig. 9 gives the threshold voltage versus power cycles. For the new devices, the typical threshold voltage of the cascode GaN is 2.1 V. Before the devices fail, V_{th} doesn't change much for all cascode GaN devices.

On the other side, typical threshold voltage of the new *p*-GaN

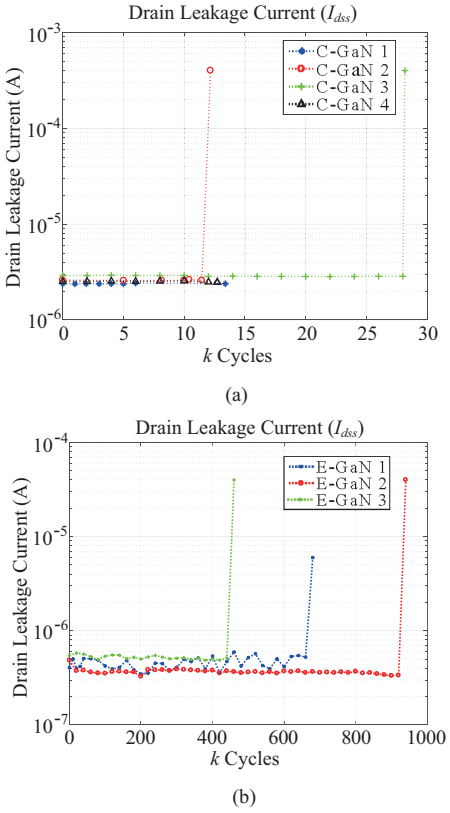


Fig. 8. Drain leakage current change during the aging process: (a) Cascode GaN. (b) E-mode GaN.

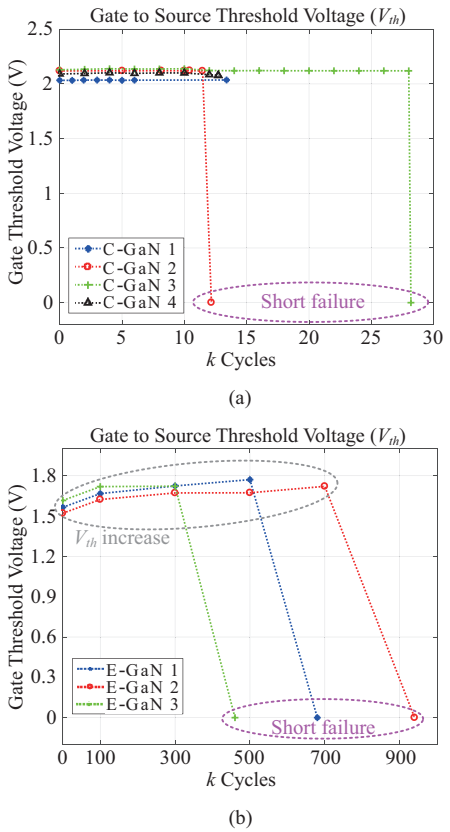


Fig. 9. Threshold voltage change during the aging process: (a) Cascode GaN. (b) E-mode GaN.

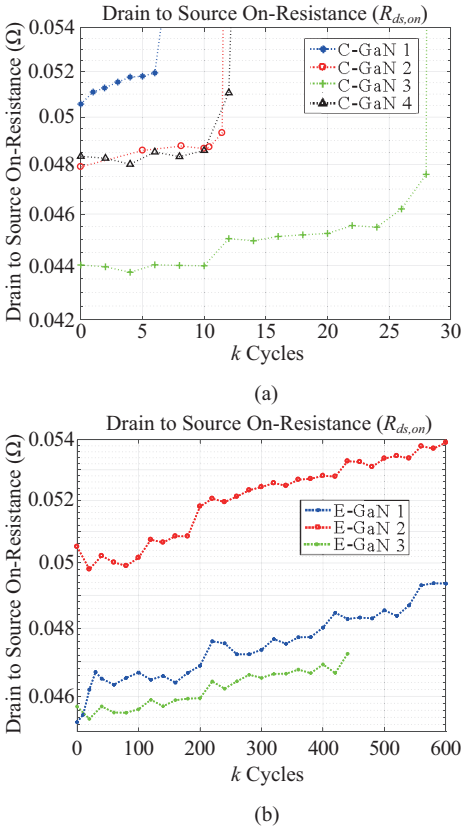


Fig. 10. On-state resistance change with respect to power cycles: (a) Cascode GaN. (b) E-mode GaN.

devices is around 1.5 V. V_{th} increases for all p-GaN devices during the aging process and the maximum increase of V_{th} is by 20%. As can be seen in Fig. 9(b), the incremental increase in V_{th} makes it a good candidate for aging detections. The threshold voltage increase can potentially be caused by the traps under the gate and the AlGaN/GaN interface layer as the device is aged [27]. After the devices lose the blocking capability, a large drain leakage current is observed and the threshold voltage drops significantly.

D. On-State Resistance $R_{ds,on}$

The on-state resistance $R_{ds,on}$ versus power cycles is shown in Fig. 10. It is observed that $R_{ds,on}$ curves for both cascode GaN and p-GaN devices increase gradually. The maximum increase of $R_{ds,on}$ for these two types of devices are about 8% and 10% compared to the initial values.

To find out the cause of the on-resistance variation toward the end of the lifetime, the on-resistance differences between the healthy and aged conditions for C-GaN 3 and E-GaN 2 are displayed in Fig. 11 under different gate-source voltages. As can be seen, the $\Delta R_{ds,on}$ of cascode GaN device does not change too much with the V_{gs}. This implies that the on-resistance change is not caused by the channel resistance degradation. It is suspected that the on-resistance increase is mainly due to the package related degradations. However, for the p-GaN device, the $\Delta R_{ds,on}$ increases significantly as V_{gs} is reduced. Therefore, it is concluded that the channel resistance mainly contributes to this

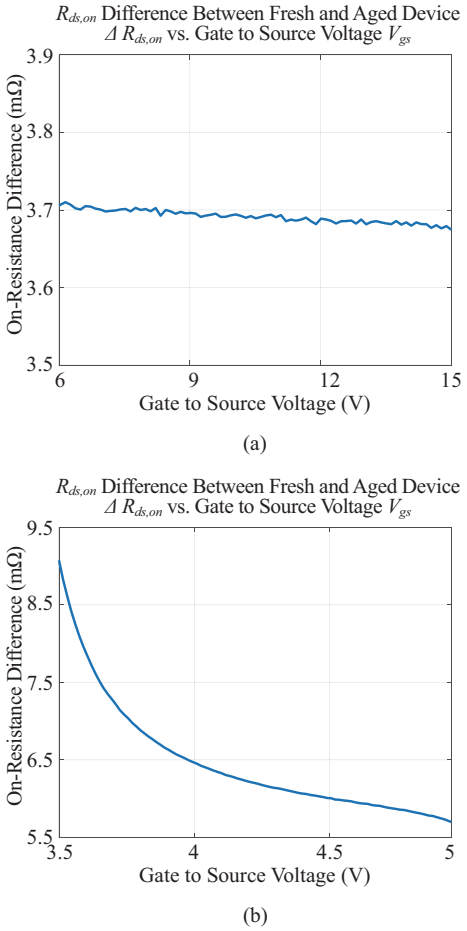


Fig. 11. On-resistance difference between fresh and aged device vs. gate to source voltage: (a) C-GaN 3. (b) E-GaN 2.

on-resistance increase as the *p*-GaN device is aged.

From the experimental results, the on-state resistance is found to be a good candidate for health condition monitoring as it changes gradually, especially for the *p*-GaN device.

E. Device Capacitances: C_{iss}, C_{oss}, C_{rss}

Since all the tested cascode GaN devices exhibit a similar result regarding the capacitance, only the input capacitance C_{iss}, the output capacitance C_{oss} and the reverse transfer capacitance C_{rss} of the C-GaN 3 throughout the power cycles are given in Fig. 12(a). As can be seen, no significant change is observed. Similarly, the *p*-GaN devices show little change on the capacitances except there is only a slight decrease of C_{rss} as shown in Fig. 12(b).

F. Transfer Characteristics I_d-V_{gs}

Fig. 13 and Fig. 14 illustrate the I_d-V_{gs} curve of the C-GaN 3 and E-GaN 2 respectively with respect to the number of power cycles. The transconductance $g_m = \frac{\Delta I_d}{\Delta v_{gs}}$ is derived from the curves.

As can be seen from Fig. 13, there is little change in the transfer characteristics and transconductance of the cascode GaN device. However, for the *p*-GaN device, a shift of transfer curve

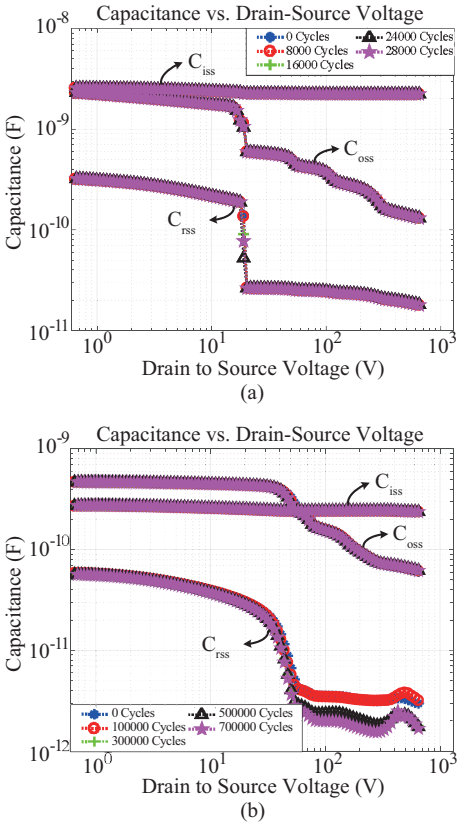


Fig. 12. Device capacitance change during power cycles: (a) Cascode GaN. (b) E-mode GaN.

is observed as the device is aged as shown in Fig. 14(b). It is also found that the transconductance g_m is gradually decreasing during the aging process. For the *p*-GaN devices, the theoretical equation for I_d-V_{ds} in the saturation region is given as:

$$I_d = K(V_{gs} - V_{th})^2 \tag{1}$$

Where K depends on the device dimension and mobility. The variation of K and V_{th} can be derived by fitting the transfer characteristics curve with the equation

$$y = K(x - V_{th})^2 \tag{2}$$

TABLE II summarizes the change of K and V_{th} at different numbers of aging cycles. It can be seen that the threshold voltage increases and K decreases during the aging process. Since the device's dimension does not change so much, the decrease in K suggests that the electron mobility decreases during the power cycle test. The decrease in mobility can potentially be caused by the trapped electrons as the device is aged.

G. Output Characteristics I_d-V_{ds}

The output characteristics are defined as the relation between the drain current and drain-source voltage. Fig. 15 gives the I_d-V_{ds} curves of C-GaN 3 and E-GaN 2 with respect to the power

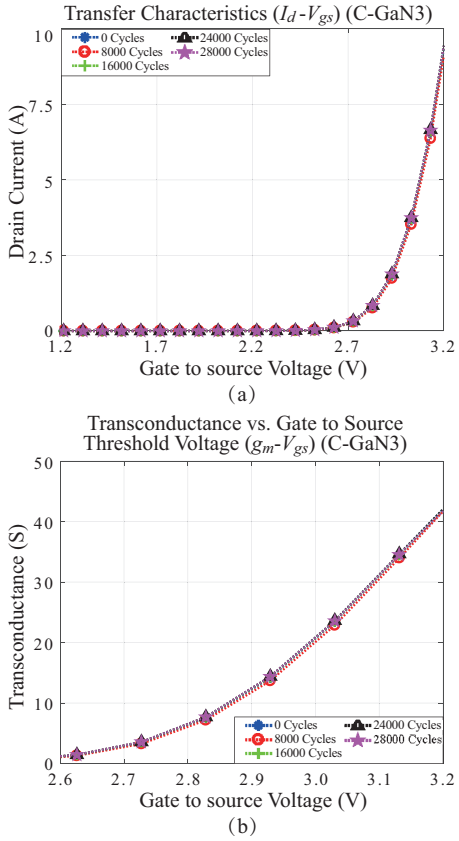


Fig. 13. Transfer characteristics and g_m curves of C-GaN 3 with respect to gate to source voltage: (a) Transfer characteristics. (b) g_m vs. V_{gs}.

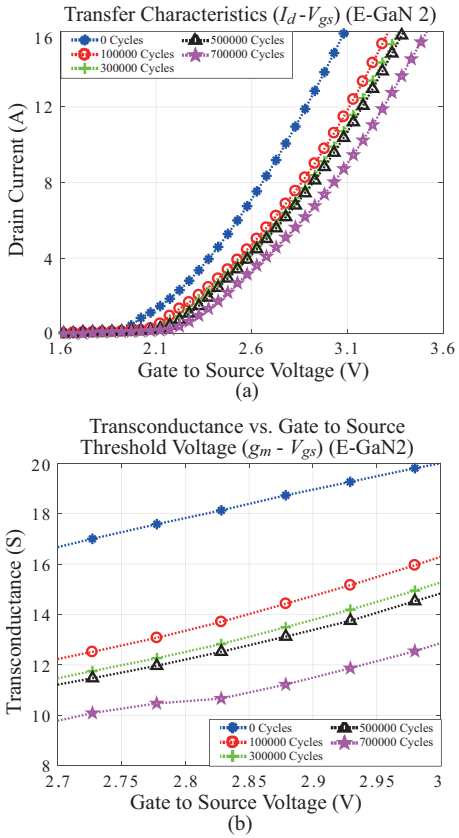


Fig. 14. Transfer characteristics and g_m curves of E-GaN 2 with respect to gate to source voltage: (a) Transfer characteristics. (b) g_m vs. V_{gs}.

TABLE II
I_d-V_{gs} OF E-GAN CURVE FITTING PARAMETERS

Cycles	K	V_{TH}
0	8.164	1.674
10k	6.308	1.737
30k	6.035	1.754
50k	6.005	1.772
70k	5.196	1.799

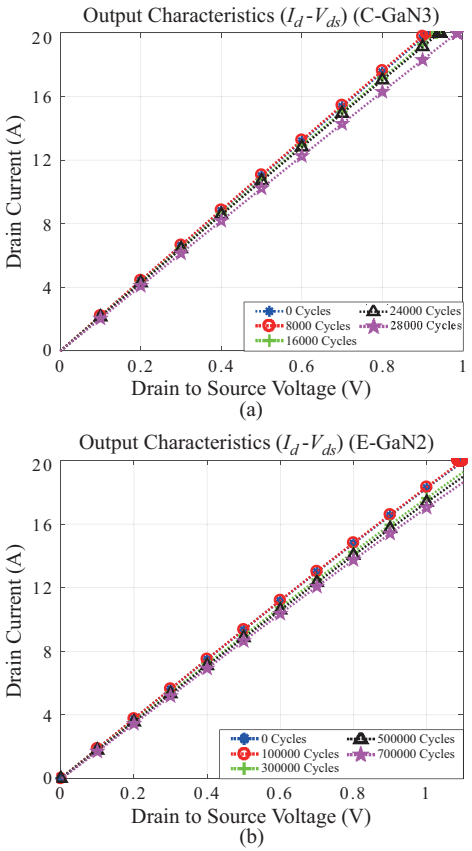


Fig. 15. Output characteristics curve with respect to power cycles: (a) Cascode GaN. (b) E-mode GaN.

cycles. Both types of GaN devices show a noticeable shift as the devices age. Specifically, for the *p*-GaN device, the theoretical equation for I_d-V_{ds} in the triode region is given as:

$$I_d = K[2(V_{gs} - V_{TH})V_{ds} - V_{ds}^2] \tag{3}$$

As summarized previously in TABLE II, the threshold voltage increases and K decreases as the device is aged. Consequently, the I-V curve tends to shift to the right according to (3).

IV. FAILURE ANALYSIS

A. Cascode GaN Devices

The failure modes of the C-GaN devices are summarized

TABLE III
FAILURE MODES OF C-GAN

Device	Failure mode
C-GaN 1	Doubled on-state resistance
C-GaN 2, 3	High gate-source and drain-source leakage current
C-GaN 4	Open circuit

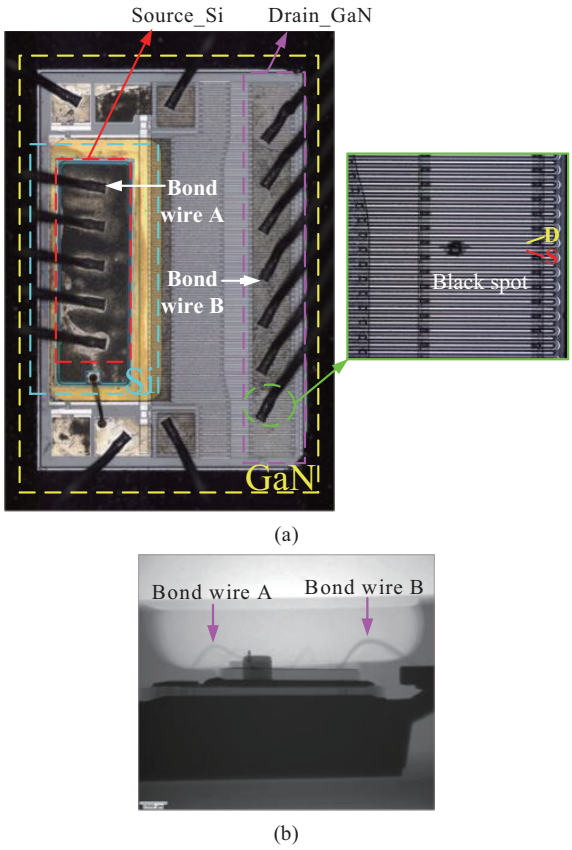


Fig. 16. Microscope and X-Ray image of the C-GaN 2: (a) Microscope. (b) X-Ray.

in TABLE III. In order to have a better understanding of the aging root cause, a detailed failure analysis (FA) has been carried out. Although the devices are initially inspected with non-destructive analysis methods like Scanning Acoustic Microscopy (SAM) and X-Ray, these methods did not reveal useful FA information due to the device. However, these images were used to understand the physical structure of the device. Then, the devices are inspected through destructive analysis in order to find the physical failure mechanism evidence. For destructive analysis, the devices are partially decapsulated with a rectangular shape cavity using laser ablation. This process decreases total decapsulation time dramatically and provides a cleaner decapsulation shape. After laser ablation, devices are decapsulated using H_2SO_4 (sulfuric acid) at 120 °C. After decapsulation, optical inspections are carried out with 5x and 20x microscope lenses.

Fig. 16 shows the die picture of C-GaN 2 after decapsulation. As shown in the zoom-in box at the right side given in Fig.16,

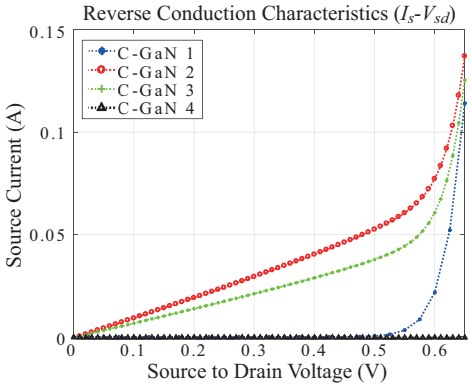


Fig. 17. Reverse conduction characteristics of GaN devices after aging.

Fig. 18. Reverse conduction path.

after removing the bond wires on the drain side of C-GaN, a black spot is detected optically in the die's surface. This black spot forms a short circuit in the GaN contacts, which can lead to the device short-circuit failure.

The reverse conduction characteristics of the C-GaN devices are compared in Fig. 17. As can be seen, C-GaN 2 and C-GaN 3 show a different feature compared to the typical aging results in the literature [7].

Typically, the voltage comprises two parts in the reverse conduction path as plotted in Fig. 18. One is the diode forward voltage drop, and the other one is the path resistance which includes the resistance of depletion mode GaN HEMT and the parasitic resistance. In the healthy devices, the reverse current starts to increase after the source-drain voltage V_{sd} exceeds the body diode voltage drop V_F. However, for C-GaN 2 and C-GaN 3 devices, the current start increasing before V_{sd} exceeds V_F. It suggests a degradation in the Si MOSFET's body diode.

To verify this assumption, the stacked two dies (Si MOSFET on top of the GaN device) are then detached to check the state of each device. The measurement shows that there is a large leakage current between gate to drain and gate to source of the Si MOSFET, and this degradation in the Si MOSFETs leads to different reverse conduction characteristics of the C-GaN devices.

For the C-GaN 4 device, an open circuit failure is observed. To find out the reason, the device is decapsulated and the surface picture is shown in Fig. 19. It is observed that all the bond wires connecting the drain-side of the GaN device and the lead are lifted off. Hence, an open circuit occurs. From the tested devices, the drain-side bond wire connection is found as one of the weak points.

B. E-Mode GaN Device

From the parameter variation shown in Section III, all three devices show a high drain-source leakage current. The E-mode GaN device degradation is mainly caused by the I_{dss} failure, which is also observed in [24]. The degradation of the GaN

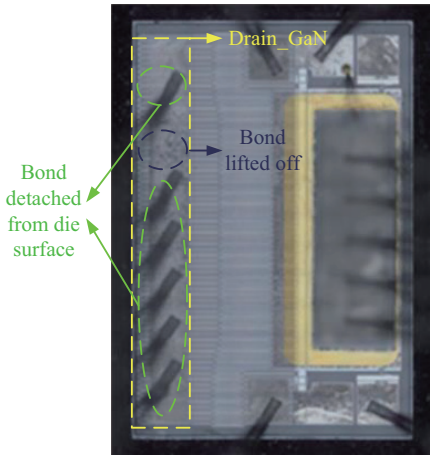


Fig. 19. Microscope image of the C-GaN 4.

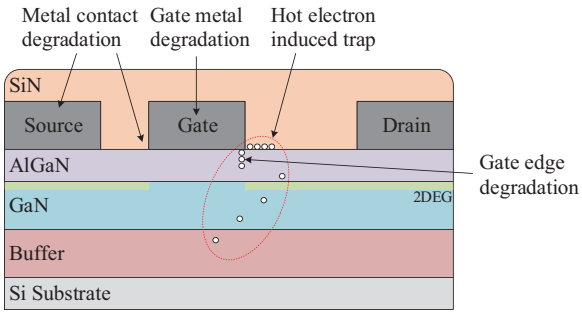


Fig. 20. GaN failure mechanism.

TABLE IV
ELECTRICAL PARAMETERS VARIATION IN DIFFERENT FAILURE MECHANISMS

		$R_{ds,on}$	V_{th}	C_{rss}	V_{bv}
GaN-related failure mechanisms	Gate-edge degradation	✓	✓	✓	✓
	Trap generation due to the electro-thermo-mechanical failure	✓	✓	✓	✓
	Punch-through effect in high drain-source conditions	✓	✓	×	✓
Thermally activated failure mechanisms	Feed metal interconnect degradation	✓	×	×	×
	Ohmic contacts degradation	✓	×	×	×
	Gate metal degradation	✓	✓	×	×
	Delamination of passivation SiN	✓	×	✓	✓

device is caused by several mechanisms and can be mainly divided into three groups, i.e., hot electron induced failure mechanisms, GaN-related failure mechanisms, and thermally activated failure mechanisms as illustrated in Fig. 20 [28].

Since the hot electron generation is not severe in the power cycling test, only the other two mechanism impacts on the device electrical characteristics are listed in TABLE IV. As measured in the curve tracer, the aged device shows an increase in threshold voltage and a decrease in the breakdown voltage V_{bv}. The reason for this change can be the gate degradation due to thermal stress. The gate edge degradation can affect the threshold voltage and reshape the electric field distribution, which can cause the decrease of the breakdown voltage.

V. CONSLUSION

This paper presents a comprehensive analysis of degradation performance in cascode and E-mode *p*-GaN gate devices under cyclic electrical and thermal stresses. The parametric variations show that the on-state resistance in both GaN device types gradually changes, which provides promising results as a degradation precursor. Furthermore, for the *p*-GaN gate device, the threshold voltage increases and transconductance decreases as the device is aged, which offers an alternative degradation precursor. From the analysis of cascode GaN device, the results demonstrate that some of the devices show short circuit characteristic between gate-source and drain-source ports. By decapsulating the devices and detaching the dies, it is found that both of the dies exhibit short circuit characteristic. Besides, the failure analysis shows that the bond wire connecting the drain pad of the GaN die and the drain lead is a weak point in this device. For the *p*-GaN gate device, the anticipated reason is related to gate degradation, which can cause an increase in the gate threshold voltage and reduce the breakdown voltage.

REFERENCES

[1] F. C. Lee, Q. Li, Z. Liu, Y. Yang, C. Fei, and M. Mu, "Application of GaN devices for 1 kW server power supply with integrated magnetics," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 3–12, Dec. 2016.

[2] Y. Cui, W. Zhang, L. M. Tolbert, D. J. Costinett, F. Wang, and B. J. Blalock, "Two phase interleaved ISOP connected high step down ratio phase shift full bridge DC/DC converter with GaN FETs," in *Proc. IEEE Transp. Electrif. Conf. Expo.*, 2015, pp. 1414–1419.

[3] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.

[4] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of GaN HFETs," in *Proc. IEEE Wide Bandgap Power Devices Appl.*, 2014, pp. 24–29.

[5] S. She *et al.*, "Thermal analysis and improvement of cascode GaN device package for totem-pole bridgeless PFC rectifier," *Appl. Therm. Eng.*, vol. 90, pp. 413–423, Nov. 2015.

[6] S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran, and B. Akin, "Aging precursor identification and lifetime estimation for thermally aged discrete package silicon power switches," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 251–260, Jan. 2017.

[7] S. Dusmez and B. Akin, "Comprehensive parametric analyses of thermally aged power MOSFETs for failure precursor identification and lifetime estimation based on gate threshold voltage," in *Proc. IEEE Appl. Power Electron. Conf*, 2016, pp. 2108–2113.

[8] J. R. Celaya, A. Saxena, P. Wysocki, S. Saha, and K. Goebel, "Towards prognostics of power MOSFETs: Accelerated aging and precursors of failure," in *Proc. Annu. Conf. Prognostics Health Manage. Soc.*, 2010, pp. 1–10.

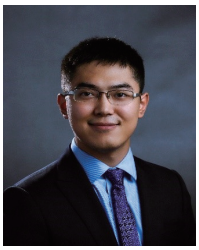
[9] X. Ye, C. Chen, Y. Wang, G. Zhai, and G. J. Vachtsevanos, "Online condition monitoring of power MOSFET gate oxide degradation based on miller platform voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4776–4784, Jun. 2017.

[10] L. Ren, Q. Shen, and C. Gong, "Real-time aging monitoring for power MOSFETs using threshold voltage," in *Proc. IEEE Annual Conf. of the IEEE Ind. Electron. Soc.*, 2016, pp. 441–446.

[11] A. Singh, A. Anurag, and S. Anand, "Evaluation of Vce at inflection point for monitoring bond wire degradation in discrete packaged IGBTs," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2481–2484,

Apr. 2017.
[12] B. Wang, J. Cai, X. Du, and L. Zhou, "Review of power semiconductor device reliability for power converters," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 101–117, Jun. 2017.
[13] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-level reliability of GaN devices," in *Proc. IEEE Int. Reliab. Phys. Symp.*, 2016, pp. 4A31–4A36.
[14] O. Hilt, J. Würfl, and J. Kuzmík, "Gate reliability investigation in normally-off p-type-GaN Cap/AlGaN/GaN HEMTs under forward bias stress," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 385–388, Apr. 2016.
[15] W. Saito, "Reliability of GaN-HEMTs for high-voltage switching applications," in *Proc. IEEE Int. Reliab. Phys. Symp.*, 2011, pp. 417–421.
[16] K. Tanaka *et al.*, "Reliability of hybrid-drain-embedded gate injection transistor," in *Proc. IEEE Int. Reliab. Phys. Symp.*, 2017, pp. 4B2.1-4B2.10.
[17] B. D. Christiansen, R. A. Coutu, E. R. Heller, B. S. Poling, G. D. Via, and N. Carolina, "Reliability testing of AlGaN/GaN HEMTs under multiple stressors," in *Proc. Int. Reliab. Phys. Symp.*, 2011, pp. CD.2.1-CD.2.5.
[18] B. Dong *et al.*, "Trap behaviours characterization of AlGaN/GaN high electron mobility transistors by room-temperature transient capacitance measurement," *AIP Adv.*, vol. 6, no. 9, Sep. 2016.
[19] F. Yang, C. Xu, E. Ugur, S. Pu, and B. Akin, "Design of a fast dynamic on-resistance measurement circuit for GaN power HEMTs," in *Proc. IEEE Transp. Electrif. Conf. Expo.*, 2018, pp. 359–365.
[20] J. Franke, G. Zeng, T. Winkler, and J. Lutz, "Power cycling reliability results of GaN HEMT devices," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2018, pp. 467–470.
[21] C. Xu, E. Ugur, and B. Akin, "Investigation of performance degradation in thermally aged cascode GaN power devices," in *Proc. IEEE Wide Bandgap Power Devices Appl.*, 2017, pp. 55–59.
[22] S. Song, S. Munk-Nielsen, C. Uhrenfeldt, and K. Pedersen, "Power cycling test of a 650 V discrete GaN-on-Si power device with a laminated packaging embedding technology," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2540–2545.
[23] S. Song, S. Munk-Nielsen, and C. Uhrenfeldt, "Failure mechanism analysis of a discrete 650V enhancement mode GaN-on-Si power device with reverse conduction accelerated power cycling test," in *Proc. IEEE Appl. Power Electron. Conf*, 2017, pp. 756–760.
[24] S. Song, S. Munk-Nielsen, and C. Uhrenfeldt, "Failure mechanism analysis of off-state drain-to-source leakage current failure of a commercial 650 V discrete GaN-on-Si HEMT power device by accelerated power cycling test," *Microelectron. Reliab.*, vol. 76–77, pp. 539–543, Sep. 2017.
[25] Transphorm, "TPH3205WSB." [Online]. Available: https://www.transphormusa.com/en/document/650v-aec-q101-cascode-gan-fet-tph3205wsbqa/.
[26] GaN Systems, "GS66508T." [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66508T-DS-Rev-180424.pdf.
[27] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Mechanism of threshold voltage shift in p-GaN gate AlGaN/GaN transistors," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1145–1148, Aug. 2018.
[28] G. Meneghesso *et al.*, "Degradation of AlGaN/GaN HEMT devices: Role of reverse-bias and hot electron stress," *Microelectron. Eng.*, vol. 109, pp. 257–261, Sep. 2013.

Chi Xu received the B.S. degree from Huazhong University of Science and Technology, Wuhan, China, in 2012 and the M.S. degree from Zhejiang University, Hangzhou, China in 2015. He is currently working toward the Ph.D. degree at the University of Texas at Dallas, Richardson, TX, USA. His research interests include high frequency and high power density power conversion, wide bandgap device's reliability and application.

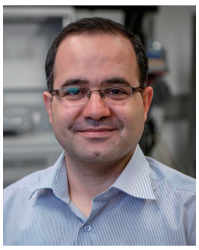


Fei Yang received the B.S. degree from Northwestern Polytechnical University, Xi'an, China, in 2011, and the M.S. degree from the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT), University of Tennessee, Knoxville, TN, USA, in 2017, both in electrical engineering. He is currently working toward the Ph.D. degree at the University of Texas at Dallas, TX, USA.

From 2012 to 2014, he was working as a researcher at the Advanced Power Electronics Lab (APEL), Kettering University, Flint, MI, USA. From 2014 to 2017, he was a Graduate Research Assistant at CURENT, University of Tennessee, Knoxville, TN, USA. From 2015 to 2017, he was working on packaging related projects at the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory, Oak Ridge, TN, USA. Since 2017, he has been a Graduate Research Assistant at the University of Texas at Dallas, TX, USA. His research interests include wide bandgap semiconductor device's reliability and application, power module packaging and integration, and motor drive system design.

Enes Ugur received the B.Sc. degree in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 2008 and the M.Sc. degree from Yildiz Technical University, Istanbul, in 2011. He is currently working toward the Ph.D. degree at the University of Texas at Dallas, Richardson, TX, USA. His research interests include dc-dc converters, electric vehicles, real-time fault diagnosis of wide-bandgap devices, and energy management strategies for renewable energy systems.

Shi Pu received the B.S. degree from the College of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2014 and the M.S. degree from Auburn University, Auburn, AL, USA, in 2016. He is currently working toward the Ph.D. degree at the University of Texas at Dallas, Richardson, TX, USA. His research interests include wide bandgap device's reliability and real-time fault diagnosis.



Bilal Akin received the Ph.D. degree in electrical engineering from the Texas A&M University, College Station, TX, USA, in 2007. He was an R&D Engineer with Toshiba Industrial Division, Houston, TX, USA, from 2005 to 2008. From 2008 to 2012, he worked as an R&D Engineer at C2000 DSP Systems, Texas Instruments Incorporated. Since 2012, he has been with the University of Texas at Dallas as an Assistant Professor. Dr. Akin is the recipient of NSF CAREER '15 award, Jonsson School Faculty Research and Teaching awards, IEEE IAS Transactions 1st Place Prize Paper Award and Top Editors Recognition Award from IEEE TVT Society. He is an Associate Editor of IEEE Transactions on Industry Applications and IEEE Transactions on Vehicular Technology. His research interests include design, control, and diagnosis of electric motors & drives, digital power control and management, and fault diagnosis & condition monitoring of power electronics components.