Performance Degradation of GaN HEMTs Under Accelerated Power Cycling Tests

Chi Xu, Fei Yang, Enes Ugur, Shi Pu, and Bilal Akin

Abstract—In this paper, performance degradations of enhancement mode (E-mode) gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) under accelerated power cycling tests are presented. For this purpose, a DC power cycling setup is designed to accelerate the aging process in a realistic manner. In order to evaluate the aging-related parameter shifts and corresponding precursors, electrical parameters are periodically monitored through a high-end curve tracer. Both the cascode device and p-GaN gate GaN devices are evaluated during these tests. In the experimental results, it is observed that the on-state resistance gradually increases in both devices. Meanwhile, the threshold voltage of the p-GaN gate GaN device gradually increases over the aging cycles and a remarkable variation in the transfer characteristics is observed. At the end of the tests, failure analyses are conducted on both devices. The cascade GaN devices show both short and open circuit failure modes, and a weak point in the drain-side bond wires is detected. For the p-GaN gate GaN device, the electrical parameter shifts indicate a possible gate degradation after the device is aged.

Index Terms—Aging precursor, failure analysis, failure mode, failure model, GaN device, power cycling.

I. INTRODUCTION

GALLIUM nitride (GaN) devices are one of the most promising power devices in high frequency, high efficiency and high power density power conversions [1], [2]. Compared to Si and SiC counterparts, GaN high-electron-mobility transistors (HEMTs) exhibit a better figure of merit. The GaN HEMTs can be categorized into normally-on and normally-off devices [3]. Normally-on GaN device is less desirable in power converters due to its reliability concerns. For normally-off GaN devices, there are several methods to implement, including recessed Schottky gate, p-GaN gate, plasma treatment under the gate and cascode structure [4]. Among them, the cascode GaN and p-GaN gate GaN are mainly applied in commercially available GaN devices as shown in Fig. 1.

Both these types of GaN devices show different characteristics from the conventional Si devices. For cascode GaN devices, there are two primary heat sources, i.e., the GaN HEMT and Si MOSFET devices. These two devices are purposely overlapped in the stacked-die package to reduce the package related parasitics [5]. However, this makes it more difficult to dissipate the heat compared to the conventional design where each die sits on the base plate. On the other side, for E-mode GaN HEMTs, since there is no wire and die attachment compared to the conventional wire bond process [6]–[12], the common failure regarding package, such as bond-wire cracks, lift-off and die attachment delamination won’t be observed. Hence it is quite necessary to study the reliability of these newly developed devices [13].

Recent studies mainly focus on exerting stress directly on the device, including the high electric field, high temperature and high drain bias [14]–[18]. These stressors can result in current collapse [19], drain current degradation, threshold voltage shift and gate leakage current increase. To simulate the device’s real operation in power converters, the device reliability under the power cycling test (PCT) is also studied. In [20], [21], the results show that the bond wire lift-off at the drain side of Cascode GaN (C-GaN) devices is the main cause of failure. In [22]–[24], both of the forward and reverse conduction operation modes of p-GaN gate GaN HEMTs are studied. There is no significant difference in the failure modes of these two operation conditions, and the common failure of the devices under test (DUTs) is solder delamination. In [20], similar results of p-GaN gate GaN devices are given, i.e., the solder joint delamination. However, comprehensive analysis of the static electrical parameter shifts throughout the aging process is not adequately addressed in the literature. This paper aims to evaluate the reliability of existing commercially available GaN devices by applying accelerated power cycling tests to mimic aging-related degradation. The investigation regarding the electrical parameters’ change throughout the aging process is provided to identify the aging precursors, which can be used to prevent costly shutdowns and realize device condition monitoring.

The paper is organized as follows: in Section II, a power cycling test setup is designed and its operation principle is briefly discussed. With the proposed test setup, power cycling is implemented and the electrical parameter variations throughout the aging process are provided in Section III. In Section IV,
physical inspections are provided to investigate the causes of failures and discussions are given regarding parameter variations. Finally, the conclusions are provided in Section V summarizing the experimental results.

II. ACCELERATED AGING TEST SETUP

Power cycling test is commonly used to accelerate the aging process, which can trigger various failure mechanisms due to junction temperature swings, shear stress, thermal expansion coefficient mismatch and enables aging precursors identification for health monitoring and lifetime estimation. In [22], a constant current is injected into the DUT by controlling a MOSFET. A bypass MOSFET is paralleled with the DUT branch for current free-wheeling. However, the current source is not fully used as it heats up the bypass MOSFET during the cooling period. To increase the utilization of the current source, a new power cycling test setup is designed to heat up all the DUTs sequentially.

The circuit diagram of the system is shown in Fig. 2, and it consists of five parts: a current source (CS), a DSP controller, a measurement board, a temperature controlled cold-plate and the DUTs. Among them, the output capacitor-less buck converter is applied as a current source for actively heating up the devices. Specifically, when one of the DUTs is turned on, \( S_2 \) is kept in off-state, and the duty cycle of high side switch \( S_1 \) is adjusted to regulate the load inductor’s current to the rated current value of the DUT. The current value of the inductor is measured through a current sensor for feedback control. As the DUT is heated up by the inductor’s current, the junction temperature is estimated through one of the temperature sensitive electrical parameters, i.e., the on-state resistance, which is calculated in real time with the measured drain-to-source voltage and the drain current. When the junction temperature of DUT reaches the maximum temperature limit of 150 °C, the current is set to zero immediately. Here, the temperature is kept within SOA to avoid triggering unrealistic aging modes. When the inductor current becomes low, the DUT is turned off for cooling down to the cold plate temperature, i.e., 25 °C. The remaining small current ripple, as shown in Fig. 3, is dissipated by the output capacitance \( C_{oss} \) and the body diode of low side switch \( S_2 \). While cooling down the previous DUTs, the next DUT is heated up. The switching sequence is given in Fig. 3 and the detailed specifications are listed in TABLE I.

TABLE I  
SPECIFICATION OF AGING TEST SETUP

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS MOSFET</td>
<td>40 V/100 A</td>
</tr>
<tr>
<td>CS Inductor</td>
<td>40 μH</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>150 °C</td>
</tr>
<tr>
<td>Heat Sink Temperature</td>
<td>25 °C</td>
</tr>
</tbody>
</table>

III. PARAMETRIC ANALYSES OF THERMALLY AGED GaN DEVICES

In this study, 650 V cascode [25] and 650 V p-Gate gate
device [26] are used. The electrical parameters such as the gate-source leakage current $I_{\text{gss}}$, the drain-source leakage current $I_{\text{dss}}$, the threshold voltage $V_{\text{th}}$, the on-state resistance $R_{\text{ds,on}}$, the device capacitances ($C_{\text{iss}}$, $C_{\text{oss}}$, $C_{\text{rss}}$), the transfer characteristics ($I_{\text{d}}$-$V_{\text{gs}}$), and the output characteristics ($I_{\text{d}}$-$V_{\text{ds}}$), are periodically measured over the aging cycles with the Keysight B1506A curve tracer as shown in Fig. 6. In the following sections, the parameter shifts of each device are presented in detail.

**A. Gate-to-Source Leakage Current $I_{\text{gss}}$**

$I_{\text{gss}}$ is measured by applying 15 V voltage on gate-source to the cascode GaN and 5 V voltage to the $p$-GaN device. The gate leakage current versus the number of power cycles is plotted for the cascode and $p$-GaN device respectively in Fig. 7(a) and (b).

Before the devices are aged, $I_{\text{gss}}$ is very low, i.e., a maximum of 50 pA for cascode GaN and 50 μA for the $p$-GaN device. After certain aging process, $I_{\text{gss}}$ of C-GaN 2, 3 and E-mode GaN (E-GaN) 2, 3 reach the compliance value of 1 mA. There is no gradual increase of $I_{\text{gss}}$ before the device fails. Therefore, it is difficult to rely on the $I_{\text{gss}}$ change as an aging precursor to predict the device’s remaining useful lifetime. In fact, a high gate leakage current increase in the cascode GaN device suggests a failure in the Si MOSFET.

**B. Drain-to-Source Leakage Current $I_{\text{dss}}$**

$I_{\text{dss}}$ is defined as the drain leakage current when the rated voltage is applied to the drain-source. As shown in Fig. 8, initially $I_{\text{dss}}$ of cascode GaN and $p$-GaN device are also very low, i.e., a maximum of 40 μA for cascode GaN and less than 1 μA for the $p$-GaN device. Similar to the gate leakage current change, the $I_{\text{dss}}$ of C-GaN 2, 3 reaches the compliance value of 400 μA and loses the blocking voltage ability. For the cascode device, since two devices are in series, it is necessary to decapsulate the device to find out the root cause of the failure, which is discussed later in the failure analysis.

For the $p$-GaN device, the leakage current of E-GaN 2, 3 reaches the compliance value of 40 μA after certain aging cycles and also loses the blocking ability. Similar to the gate leakage current, the drain leakage current does not gradually increase which makes it non-ideal for aging detections.

**C. Threshold Voltage $V_{\text{th}}$**

$V_{\text{th}}$ is defined as the minimum gate-source voltage that is needed to create a drain current conducting between the drain and source terminals, i.e., 250 μA for cascode GaN and 7 mA for the $p$-GaN device. Fig. 9 gives the threshold voltage versus power cycles. For the new devices, the typical threshold voltage of C-GaN 2, 3 reach the compliance value of 40 μA after certain aging cycles and also loses the blocking ability. Similar to the gate leakage current, the drain leakage current does not gradually increase which makes it non-ideal for aging detections.
devices is around 1.5 V. \( V_{th} \) increases for all \( p \)-GaN devices during the aging process and the maximum increase of \( V_{th} \) is by 20\%. As can be seen in Fig. 9(b), the incremental increase in \( V_{th} \) makes it a good candidate for aging detections. The threshold voltage increase can potentially be caused by the traps under the gate and the AlGaN/GaN interface layer as the device is aged [27]. After the devices lose the blocking capability, a large drain leakage current is observed and the threshold voltage drops significantly.

### D. On-State Resistance \( R_{ds,on} \)

The on-state resistance \( R_{ds,on} \) versus power cycles is shown in Fig. 10. It is observed that \( R_{ds,on} \) curves for both cascode GaN and \( p \)-GaN devices increase gradually. The maximum increase of \( R_{ds,on} \) for these two types of devices are about 8\% and 10\% compared to the initial values.

To find out the cause of the on-resistance variation toward the end of the lifetime, the on-resistance differences between the healthy and aged conditions for C-GaN 3 and E-GaN 2 are displayed in Fig. 11 under different gate-source voltages. As can be seen, the \( \Delta R_{ds,on} \) of cascode GaN device does not change too much with the \( V_{gs} \). This implies that the on-resistance change is not caused by the channel resistance degradation. It is suspected that the on-resistance increase is mainly due to the package related degradations. However, for the \( p \)-GaN device, the \( \Delta R_{ds,on} \) increases significantly as \( V_{gs} \) is reduced. Therefore, it is concluded that the channel resistance mainly contributes to this
is observed as the device is aged as shown in Fig. 14(b). It is also found that the transconductance \( g_m \) is gradually decreasing during the aging process. For the \( p \)-GaN devices, the theoretical equation for \( I_d-V_{ds} \) in the saturation region is given as:

\[
I_d = K(V_{gs} - V_{th})^3
\]  

(1)

Where \( K \) depends on the device dimension and mobility. The variation of \( K \) and \( V_{th} \) can be derived by fitting the transfer characteristics curve with the equation

\[
y = K(x - V_{th})^3
\]  

(2)

TABLE II summarizes the change of \( K \) and \( V_{th} \) at different numbers of aging cycles. It can be seen that the threshold voltage increases and \( K \) decreases during the aging process. For the \( p \)-GaN devices, the decrease in mobility can potentially be caused by the trapped electrons as the device is aged.

E. Device Capacitances: \( C_{iss}, C_{oss}, C_{rss} \)

Since all the tested cascode GaN devices exhibit a similar result regarding the capacitance, only the input capacitance \( C_{iss} \), the output capacitance \( C_{oss} \), and the reverse transfer capacitance \( C_{rss} \) of the C-GaN 3 throughout the power cycles are given in Fig. 12(a). As can be seen, no significant change is observed. Similarly, the \( p \)-GaN devices show little change on the capacitances except there is only a slight decrease of \( C_{rss} \) as shown in Fig. 12(b).

F. Transfer Characteristics \( I_d-V_{gs} \)

Fig. 13 and Fig. 14 illustrate the \( I_d-V_{gs} \) curve of the C-GaN 3 and E-GaN 2 respectively with respect to the number of power cycles. The transconductance \( g_m = \frac{dI_d}{dV_{gs}} \) is derived from the curves.

As can be seen from Fig. 13, there is little change in the transfer characteristics and transconductance of the cascode GaN device. However, for the \( p \)-GaN device, a shift of transfer curve

Fig. 11. On-resistance difference between fresh and aged device vs. gate to source voltage: (a) C-GaN 3. (b) E-GaN 2.

on-resistance increase as the \( p \)-GaN device is aged.

From the experimental results, the on-state resistance is found to be a good candidate for health condition monitoring as it changes gradually, especially for the \( p \)-GaN device.

G. Output Characteristics \( I_d-V_{ds} \)

The output characteristics are defined as the relation between the drain current and drain-source voltage. Fig. 15 gives the \( I_d-V_{ds} \) curves of C-GaN 3 and E-GaN 2 with respect to the power

![Graph](image-url)
cycles. Both types of GaN devices show a noticeable shift as the devices age. Specifically, for the \( p \)-GaN device, the theoretical equation for \( I_d-V_{ds} \) in the triode region is given as:

\[
I_d = K [2(V_{gs}-V_{th})V_{ds} - V_{ds}^3]
\]  

(3)

As summarized previously in TABLE II, the threshold voltage increases and \( K \) decreases as the device is aged. Consequently, the \( I-V \) curve tends to shift to the right according to (3).

IV. FAILURE ANALYSIS

A. Cascode GaN Devices

The failure modes of the C-GaN devices are summarized...
in TABLE III. In order to have a better understanding of the aging root cause, a detailed failure analysis (FA) has been carried out. Although the devices are initially inspected with non-destructive analysis methods like Scanning Acoustic Microscopy (SAM) and X-Ray, these methods did not reveal useful FA information due to the device. However, these images were used to understand the physical structure of the device. Then, the devices are inspected through destructive analysis in order to find the physical failure mechanism evidence. For destructive analysis, the devices are partially decapsulated with a rectangular shape cavity using laser ablation. This process decreases total decapsulation time dramatically and provides a cleaner decapsulation shape. After laser ablation, devices are decapsulated using H$_2$SO$_4$ (sulfuric acid) at 120 °C. After decapsulation, optical inspections are carried out with 5x and 20x microscope lenses.

Fig. 16 shows the die picture of C-GaN 2 after decapsulation. As shown in the zoom-in box at the right side given in Fig.16, after removing the bond wires on the drain side of C-GaN, a black spot is detected optically in the die’s surface. This black spot forms a short circuit in the GaN contacts, which can lead to the device short-circuit failure.

The reverse conduction characteristics of the C-GaN devices are compared in Fig. 17. As can be seen, C-GaN 2 and C-GaN 3 show a different feature compared to the typical aging results in the literature [7].

Typically, the voltage comprises two parts in the reverse conduction path as plotted in Fig. 18. One is the diode forward voltage drop, and the other one is the path resistance which includes the resistance of depletion mode GaN HEMT and the parasitic resistance. In the healthy devices, the reverse current starts to increase after the source-drain voltage $V_{sd}$ exceeds the body diode voltage drop $V_F$. However, for C-GaN 2 and C-GaN 3 devices, the current start increasing before $V_{sd}$ exceeds $V_F$. It suggests a degradation in the Si MOSFET’s body diode.

To verify this assumption, the stacked two dies (Si MOSFET on top of the GaN device) are then detached to check the state of each device. The measurement shows that there is a large leakage current between gate to drain and gate to source of the Si MOSFET, and this degradation in the Si MOSFET leads to different reverse conduction characteristics of the C-GaN devices.

For the C-GaN 4 device, an open circuit failure is observed. To find out the reason, the device is decapsulated and the surface picture is shown in Fig. 19. It is observed that all the bond wires connecting the drain-side of the GaN device and the lead are lifted off. Hence, an open circuit occurs. From the tested devices, the drain-side bond wire connection is found as one of the weak points.

### B. E-Mode GaN Device

From the parameter variation shown in Section III, all three devices show a high drain-source leakage current. The E-mode GaN device degradation is mainly caused by the $I_{ds}$ failure, which is also observed in [24]. The degradation of the GaN
device is caused by several mechanisms and can be mainly divided into three groups, i.e., hot electron induced failure mechanisms, GaN-related failure mechanisms, and thermally activated failure mechanisms as illustrated in Fig. 20 [28].

Since the hot electron generation is not severe in the power cycling test, only the other two mechanism impacts on the device electrical characteristics are listed in TABLE IV. As measured in the curve tracer, the aged device shows an increase in threshold voltage and a decrease in the breakdown voltage $V_{bd}$. The reason for this change can be the gate degradation due to thermal stress. The gate edge degradation can affect the threshold voltage and reshape the electric field distribution, which can cause the decrease of the breakdown voltage.

V. CONCLUSION

This paper presents a comprehensive analysis of degradation performance in cascode and E-mode $p$-GaN gate devices under cyclic electrical and thermal stresses. The parametric variations show that the on-state resistance in both GaN device types gradually changes, which provides promising results as a degradation precursor. Furthermore, for the $p$-GaN gate device, the threshold voltage increases and transconductance decreases as the device is aged, which offers an alternative degradation precursor. From the analysis of cascode GaN device, the results demonstrate that some of the devices show short circuit characteristic between gate-source and drain-source ports. By decapsulating the devices and detaching the dies, it is found that both of the dies exhibit short circuit characteristic. Besides, the failure analysis shows that the bond wire connecting the drain pad of the GaN die and the drain lead is a weak point in this device. For the $p$-GaN gate device, the anticipated reason is related to gate degradation, which can cause an increase in the gate threshold voltage and reduce the breakdown voltage.

REFERENCES


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