A 1200 V/200 A Half-Bridge Power Module Based on Si IGBT/SiC MOSFET Hybrid Switch

Lei Li, Puqi Ning, Xuhui Wen, and Dong Zhang

***Abstract*—The hybrid switch (HyS), which is a parallel combination of the silicon (Si) insulated gate bipolar transistors (IGBTs) and the silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs), can realize high switching frequency at a reasonable cost. In this paper, a compact HyS half-bridge power module, rated at 1200 V/200 A, was fabricated in house and fully tested for the first time. An electrothermal model of the HyS was set up in LTspice to determine the optimal gate sequence for the HyS. To minimize the HyS power loss, the turn-on gate signals are applied to the Si IGBTs and the SiC MOSFETs simultaneously while a prior turn-off period exists between the turn-off gate signals of the Si IGBTs and the SiC MOSFETs. By considering the power loss of the HyS and the junction temperature of the SiC MOSFETs, a novel index is proposed to select the optimal prior turn-off period. Based on the HyS power modules, a 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were developed and tested to verify the analysis.**

***Index Terms*—Hybrid switch, insulated gate bipolar transistors (IGBTs), metal-oxide semiconductor field-effect transistors (MOSFETs), silicon carbide (SiC).**

I. Introduction

In the past decades, the Silicon (Si) Insulated Gate Bipolar Transistor (IGBT) has been widely used in many engineering applications such as renewable energy systems, utility power systems and transportation drives [1]. As the growth of the electric cars and the high-speed trains, the highly integrated power converters with more and more high switching frequency are now demanded. However, the long turn-off period induced from the minority carriers recombination namely the tail current severely restricts the switching frequency of the Si IGBT [2].

The Silicon Carbide (SiC) devices are the attractive alternatives because of their potential of high switching frequency [3] and high junction temperature [4]. Among them, the SiC Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is the most promising device to replace the Si IGBT for its high blocking voltage and compatible gate driver design [5]. Unfortunately, the SiC MOSFET is still under development and it is too expensive to be large scale adopted [6].

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The concept of the hybrid switch (HyS) was first proposed in 1993 [7]. With the help of the paralleled MOSFETs, zero-voltage switch (ZVS) of the IGBTs [8] is realized. Thus, the switching loss is reduced and the switching frequency is improved. Compared with the Si counterparts, the SiC MOSFETs have lower on-resistance [9] and lower reverse recovery energy [10]. Thus, better performance of the HyS can be achieved.

The HySs consisting of the paralleled Si IGBTs and the SiC MOSFETs have been investigated before [11]–[19]. It was demonstrated that the HySs can perform lower switching loss compared to the Si IGBTs and lower cost compared to the SiC MOSFETs [11], [12]. However, the reported HySs are commonly based on the discrete semiconductors and the parasitic inductors of the connection severely restrict their performance [13], [14]. A 6.5 kV/40 A HyS power module was developed in [15]. The HyS power module contained only one switch and only the double pulse test was conducted. Possible gate sequences for the HySs were evaluated and the optimal gate sequence was chosen by solely considering the power loss of the HySs [16]–[18]. There is large thermal stress on the SiC MOSFETs within the HySs because the entire load current is conducted through the SiC MOSFETs during the switching transients. A thermal balance control mode and a current-dependent switching strategy was presented in [18] and [19] respectively to keep the reliable operation of the SiC MOSFETs.

Improved from the previous studies, in this paper, a compact HyS half-bridge power module, rated at 1200 V/200 A, was fabricated to suppress the influence of the parasitic inductors and to fully utilize the advantages of the HyS. Si/SiC current ratio is 4:1. An electrothermal model of the HyS was set up in LTspice to determine the suitable gate sequence for the HyS. Considering the power loss of the HyS and the junction temperature of the SiC MOSFETs, a novel index is proposed to select the prior turn-off period between the turn-off gate signals of the Si IGBTs and the SiC MOSFETs. Utilizing the HyS power modules, a 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were developed and tested to verify the analysis.

II. Hybrid Switch Power Module

Fig. 1 depicts the layout of the HyS half-bridge power module. Each HyS consists of one SiC MOSFET (CPM2–1200–0025B, 1200 V/50 A at 100 °C) and two Si IGBTs (IRG8CH97K10F, 1200 V/100 A at 100 °C). Si/SiC current

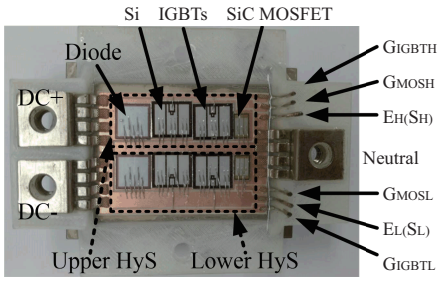

Fig. 1. Layout of the HyS power module.

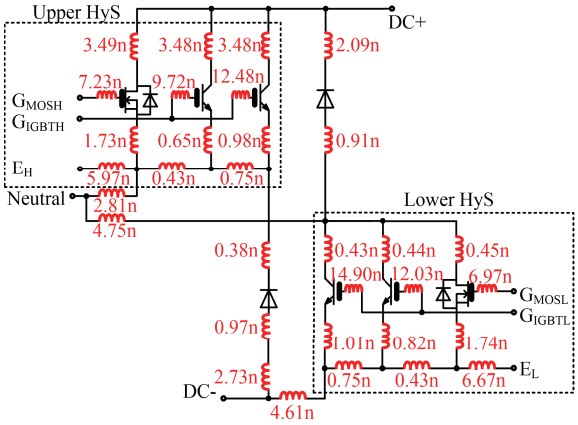

Fig. 2. Parasitic inductance of the HyS power module. (a) Parasitic inductance extracted by Ansys Q3D. (b) Simplified parasitic inductance.

ratio is 4:1. To reduce the cost, a Si PiN Diode (IRD3CH82DB6, 1200 V/200 A at 100 °C) is paralleled to the HyS. The Si IGBTs and the SiC MOSFET are separately controlled. Power terminals (DC+, DC−, and Neutral) and gate terminals (GIGBTH, GMOSH, EH, GIGBTL, GMOSL, and EL) are bonded to Direct-Bond-Copper (DBC) with ultrasonic method to form large contact areas. Si IGBTs collectors, Si Diode cathode and SiC MOSFET drain are soldered DBC. DBC patterns are designed as compact as possible to reduce the commutation path.

TABLE I
HyS Power Module Packaging Materials

Part	Specifications
Baseplate	Aluminum Silicon Carbide (AlSiC), 3 mm thickness
Substrate	Aluminum Nitride (AlN) DBC with Cu/AlN/Cu thickness 0.2 mm/0.4 mm/0.2 mm
Die solder	Au80Sn20, 280 ºC melting point
Power bonding wire	Aluminum, 0.4 mm diameter, 5 parallel wires for SiC MOSFET, 6 parallel wires for Si IGBTs and 6 parallel wires for Si Diode
Gate terminal	1 mm diameter copper pin
Power terminal	0.8 mm thick copper terminal
Encapsulation	Nusil R-2188
Housing	ABS, 1.5 mm thickness, 82 mm × 64 mm × 6 mm

A. Parasitic Inductance of the HyS Power Module

The parasitic inductance of the HyS power module was extracted by Ansys Q3D. The results are concluded in Fig. 2(a). It is difficult to determine the parasitic inductance between the Si IGBTs and the SiC MOSFET according to the results extracted by Ansys Q3D. Thus, the parasitic inductance was simplified utilizing the method in [20], shown in Fig. 2(b). The total inductance between the Si IGBTs and the SiC MOSFET is less than 10 nH, which has little influence on the dynamic current sharing among the devices [13]. As a comparison, the commercial TO−247 packaged devices which were commonly used in the aforementioned studies have more than 15 nH parasitic inductance in power path [21]. With the module design, the parasitic inductance is decreased a lot.

B. Thermal Resistance of the Chips Within the HyS Power Module

The packaging materials of the HyS power module are listed in TABLE I. A thermal resistance test system was built to measure the chip to case thermal resistance of the dies [22]. The linear superposition principle is adopted to evaluate the thermal coupling between the different chips and the junction temperature of the chips can be expressed as a thermal resistance matrix,

$$\begin{bmatrix} T_{j,\mathrm{DiodeH}} \\ T_{j,\mathrm{IGBTH}} \\ T_{j,\mathrm{MOSH}} \\ T_{j,\mathrm{DiodeL}} \\ T_{j,\mathrm{IGBTL}} \\ T_{j,\mathrm{MOSL}} \end{bmatrix} = \begin{bmatrix} T_{j,1} \\ T_{j,2} \\ T_{j,3} \\ T_{j,4} \\ T_{j,5} \\ T_{j,6} \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & R_{13} & R_{14} & R_{15} & R_{16} \\ R_{21} & R_{22} & R_{23} & R_{24} & R_{25} & R_{26} \\ R_{31} & R_{32} & R_{33} & R_{34} & R_{35} & R_{36} \\ R_{41} & R_{42} & R_{43} & R_{44} & R_{45} & R_{46} \\ R_{51} & R_{52} & R_{53} & R_{54} & R_{55} & R_{56} \\ R_{61} & R_{62} & R_{63} & R_{64} & R_{65} & R_{66} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} R_{11} & R_{12} & \cdots & R_{16} \\ R_{21} & R_{22} & \cdots & R_{26} \\ \vdots & \vdots & \ddots & \vdots \\ R_{61} & R_{62} & \cdots & R_{66} \end{bmatrix} = \begin{bmatrix} 0.48 & 0.14 & 0.02 & 0.09 & 0.12 & 0.02 \\ 0.05 & 0.33 & 0.06 & 0.02 & 0.03 & 0.03 \\ 0.02 & 0.18 & 0.95 & 0.02 & 0.09 & 0.15 \\ 0.12 & 0.09 & 0.02 & 0.50 & 0.12 & 0.02 \\ 0.02 & 0.05 & 0.02 & 0.05 & 0.32 & 0.08 \\ 0.02 & 0.12 & 0.15 & 0.02 & 0.21 & 0.93 \end{bmatrix} \tag{2}$$

where $T_{j,i}$ (i = 1–6) are the junction temperatures of the chips, P_i (i = 1–6) are the power losses of the chips, R_{ii} (i = 1–6) are the chip to case thermal resistance of the dies and R_{ik} (i, k = 1–6 and $i \neq k$) describe the junction temperatures rising because of thermal coupling. The two Si IGBTs are treated as one chip to simplify the tests and the analyses. The test results are concluded in (2).

III. Electrothermal Model of the Hybrid Switch

There are four kinds of semiconductors within a HyS, namely Si PiN Diode, Si IGBT, SiC MOSFET and the body diode of the SiC MOSFET, which is also a PiN Diode.

A. Electrothermal Model of the HyS

Fig. 3 demonstrates the circuit representation of the PiN diode model. It is made up of three parts. The first part is based on the finite difference method (FDM) [23] to calculate the excess carrier concentration in the base region under high level injection. I_1 and I_{n+1} are the boundary conditions to solve the ambipolar diffusion equation. The second part is the model to calculate the quasi-neutral base width. The quasi-neutral base region is divided into n elements with the equal length. The third part is a series of voltage sources representing the diode voltage, where E_{jA}, E_{res}, E_{jD}, and E_{SC} is the voltage across the P+/N− junction, the voltage across the base region, the voltage across the N−/N+ junction, and the voltage across the depletion region respectively. The values of the voltage sources are determined by the excess carrier concentration in the base region. In the simulation, the quasi-neutral base region is separated into 10 elements.

Fig. 4 displays the circuit representation of the SiC MOSFET model.The MOSFET channel current consists of I_{mosl}, conducted through the corners of the MOSFET cells, and I_{mosh}, conducted through the main portion of the MOSFET cells [24]. R_d is composed of the N- base region resistor and the drain contact resistor. R_s and R_g is the source contact resistor and the gate contact resistor respectively. The switching characteristics of the SiC MOSFET are described through the gate-source capacitor C_{gs}, gate-drain capacitor C_{gd}, and drain-source capacitor C_{ds}. C_{gs} and C_{ds} are determined by gate-source voltage and drain-source voltage respectively while C_{gd} ane related to both of them. The voltage-controlled capacitors are modeled through a voltage-controlled voltage source, a normal capacitor, and a current-controlled current source [25].

Shown in Fig. 5, the Si IGBT model is the combination of the FDM model and the MOSFET model. The excess carrier concentration in the base region is calculated through the FDM method, and the on-state voltage of the Si IGBT is composed of E_{jA}, E_{res}, and E_{SC}. The switching characteristics of the Si IGBT are described through the gate-emitter capacitor C_{ge}, gate-collector capacitor C_{gc}, and collector-emitter capacitor C_{ce}.

According to the results of the thermal resistance test, the thermal model of the Si IGBT is displayed as Fig. 6 [26]. Junction temperature rise of the Si IGBT is due to the self-heating of the Si IGBT and the thermal coupling between the Si IGBT and the other semiconductors. Thermal model of the Si PiN Diode and the SiC MOSFET can be described using the same circuit.

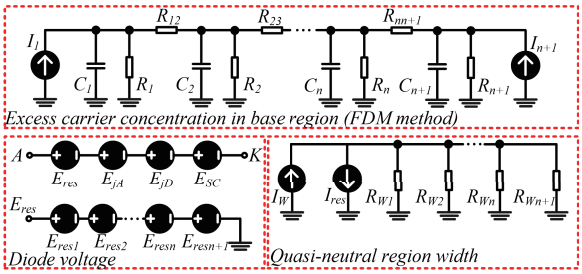

Fig. 3. PiN diode model.

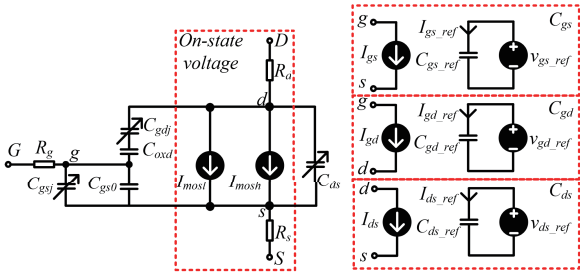

Fig. 4. SiC MOSFET model.

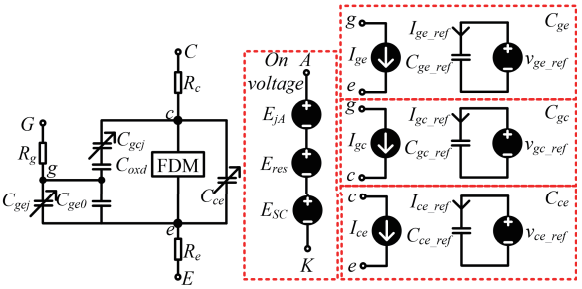

Fig. 5. Si IGBT model.

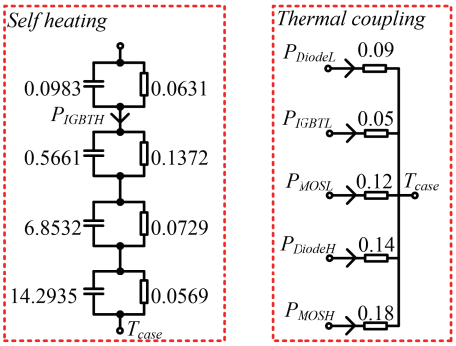

Fig. 6. Thermal model of the Si IGBT.

B. Verification of the Electrothermal Model

The output characteristics of the semiconductors were tested by the static and dynamic testing system from LEMSYS while the switching characteristics were tested utilizing a double pulse test fixture based on the voltage source inverter in Section V [27].

To carry out tests for the separate semiconductors, several

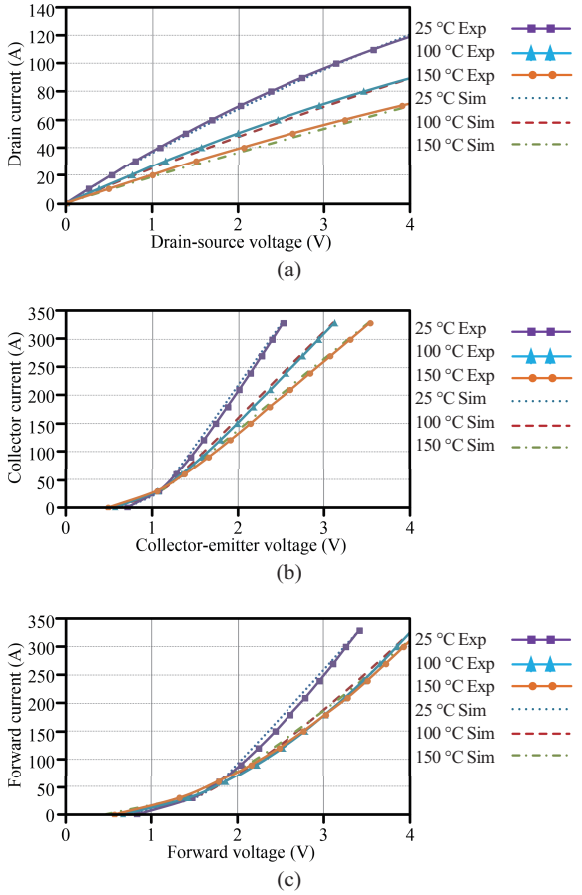

Fig. 7. Comparison of the experiment and simulation output characteristics. (a) SiC MOSFET. (b) Si IGBT. (c) Si Diode.

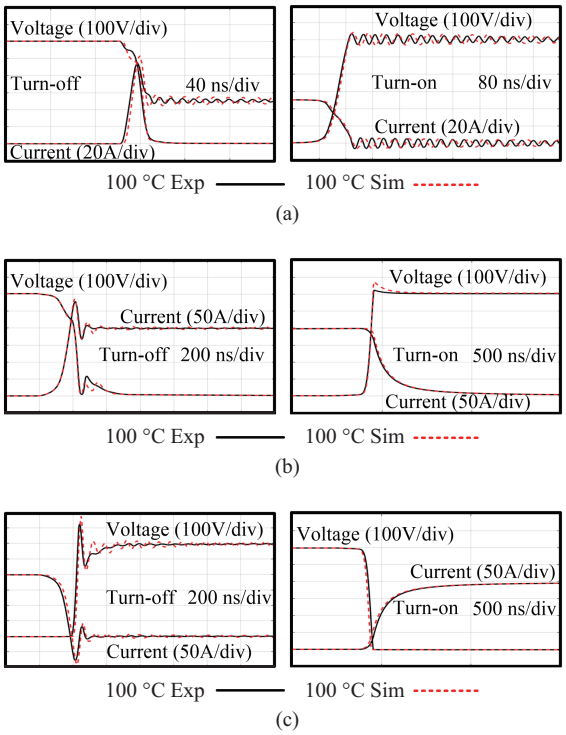

Fig. 8. Comparison of the experiment and simulation switching characteristics. (a) SiC MOSFET. (b) Si IGBT. (c) Si Diode.

HyS power modules were fabricated. All the chips were implemented in the HyS power modules, but only the utilized chips in the corresponding test were connected through the bonding wires. For example, only the Si PiN Diode was connected through the bonding wires to test the output characteristics of the Si PiN Diode. Only the SiC MOSFET and the Si PiN Diode were connected to test the switching characteristics of the SiC MOSFET or the Si PiN Diode. As demonstrated in Fig. 7 and Fig. 8, the output and switching characteristics of the dies predicted by the electrothermal model agree well with the experimental results. Therefore, the electrothermal model can be utilized to determine the gate sequence for the HyS.

IV. Gate Sequence for the Hybrid Switch

As depicted in Fig. 9, all the gate sequences for the HyS can be described using the prior turn-on period t_{on_delay} and the prior turn-off period t_{off_delay}.

Collectors of the Si IGBTs and drain of the SiC MOSFET are connected to the same DBC in the HyS power module (shown in Fig. 1). The power loss of the dies cannot be measured separately. Thus, the proposed HyS power module was simulated in LTSpice to find the optimal gate sequence. The simulation circuit is illustrated in Fig. 10. Buck circuit was utilized to set the load current i_L and the DC-bus voltage v_{dc}. Parasitic inductors were not considered in the simulation. Baseplate temperature was set to be 35 °C. Switching frequency was 50 kHz.

Fig. 11 displays the simulation results with v_{dc} of 400 V and i_L of 130 A. It is obvious that non-zero t_{on_delay} cannot bring any more reduction in the HyS power loss. In fact, the SiC MOSFET turns on prior to the Si IGBTs even the gate signals are applied at the same time because of the larger input capacitance of the Si IGBTs and the time taken to modulate the N-drift region conductivity [28]. Negative t_{on_delay} is not useful for reducing switching loss but introduces more conduction loss. As for positive t_{on_delay}, it eliminates the zero-current turn on of the Si IGBTs and enlarges the switching loss and the conduction loss, shown in Fig. 11(b). t_{on_delay} should remain as 0.

Fig. 12 illustrates the simulation results with v_{dc} of 400 V and i_L of 130 A utilizing different t_{off_delay}. As t_{off_delay} becomes larger, the HyS power loss decreases, but the SiC MOSFET power loss increases. A novel index as in (3) is adopted to determine the suitable t_{off_delay}. It is a characterization of the tradeoff between the HyS power loss reduction, $\Delta loss$ and the SiC MOSFET T_j rise, ΔT_j,

$$\text{Index} = \frac{-\Delta loss}{\Delta t_{off\_delay}} \Big/ \frac{\Delta T_j}{\Delta t_{off\_delay}} = \frac{-\Delta loss}{\Delta T_j} \tag{3}$$

Fig. 13 displays the index curve versus t_{off_delay}. The horizontal red line set the T_j limit as 150 °C and the maximum t_{off_delay} is restricted to be 3.5 us (Point C). Within the permissible t_{off_delay}, the index reaches the peak value at 1 us (Point A).

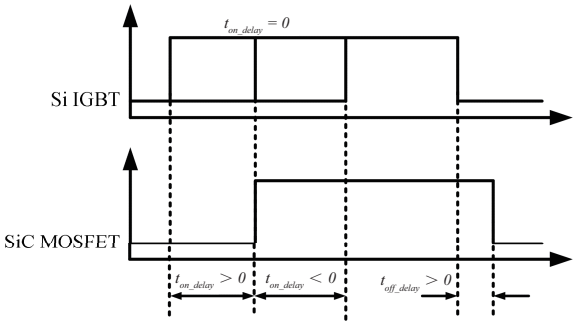

Fig. 9. Gate sequences for the HyS.

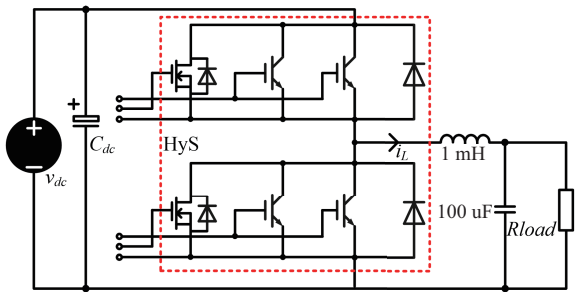

Fig. 10. Schematic of the simulation circuit.

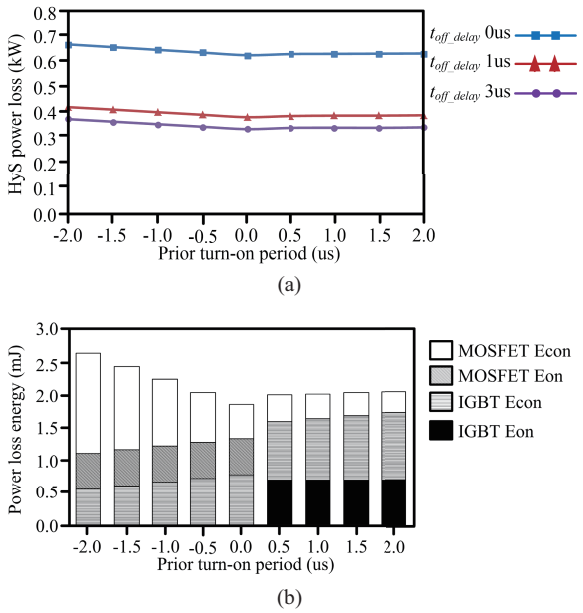

Fig. 11. Simulation results (v_{dc} = 400 V, i_L = 130 A). (a) HyS power loss at different t_{on_delay} and t_{off_delay}. (b) HyS loss energy distribution at different t_{on_delay}. Econ and Eon are conduction loss and turn-on loss respectively.

Between Point A and Point B (3 us), the HyS power loss can be further reduced, but the SiC MOSFET T_j rise is higher. Beyond Point B, the HyS power loss even starts to increase and drive the index to be negative. Therefore, the optimal t_{off_delay} is 1 us. Optimal t_{off_delay} at other operation conditions is concluded in Fig. 14.

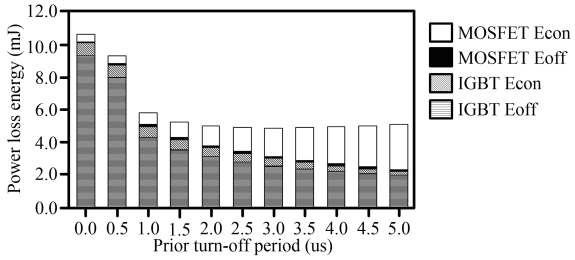

Fig. 12. HyS power loss energy distribution at different t_{off_delay} (v_{dc} = 400 V, i_L = 130 A). Eoff is the turn-off loss.

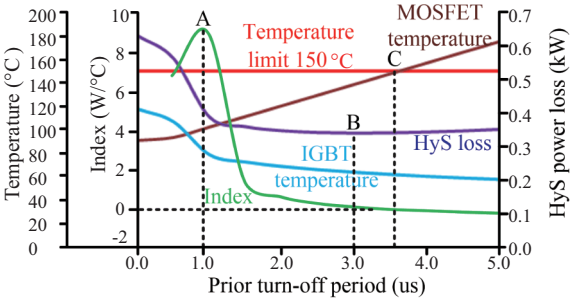

Fig. 13. Index plot to determine the suitable t_{off_delay}.

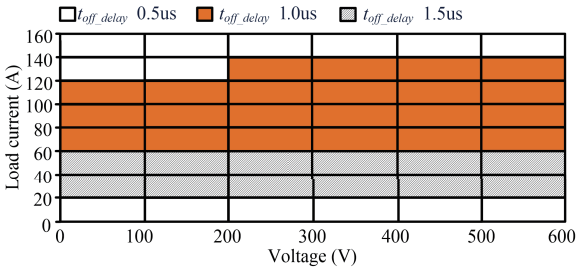

Fig. 14. Optimal prior turn-off period at different operation conditions.

V. Hybrid Switch Based Voltage Source Inverter

Utilizing the HyS power modules, a three-phase air-cooling voltage source inverter was set up to verify the analysis, shown in Fig. 15. The inverter was tested in open-loop mode with SVPWM control. The operation parameters are given in TABLE II.

For each HyS, there were two separate gate driver circuits to control the SiC MOSFET and the Si IGBTs independently. To assure the switching performance, a 2.5 A peak current optocoupler ACPL−332J from Avago followed by a 9 A peak current push-pull circuit IXDN609SI from IXYS were adopted as the gate driver ICs. 2 W DC/DC converters MGJ2D242005SC and MGJ2D241509SC were utilized as the gate driver power supply for the SiC MOSFET and the Si IGBTs respectively. Three 30 Ω chip resistors and three 15 Ω chip resistors, all in 2512 with 2 W rated power, were paralleled to form the gate resistors for the SiC MOSFET and the Si IGBTs respectively. During the turn off transient of SiC MOSFET, a fault turn-on of Si IGBTs may occur due to the fast rising collector-emitter voltage charges Miller

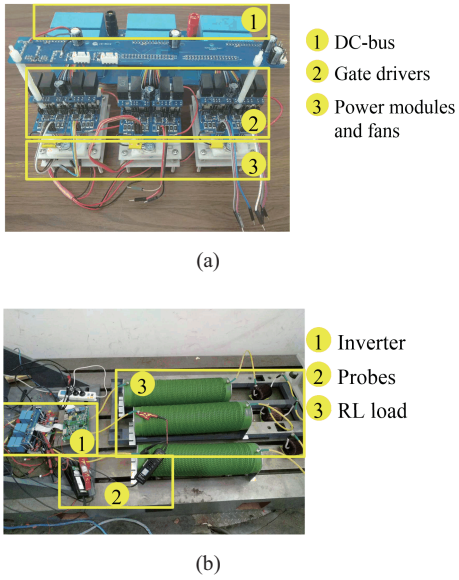

Fig. 15. Three-phase voltage source inverter. (a) Inverter prototype. (b) Test platform.

TABLE II
THREE-PHASE VOLTAGE SOURCE INVERTER OPERATION PARAMETERS

Parameter	Value
Input DC-bus voltage	400 V
Switching frequency	5 to 30 kHz
Modulation ratio	0.43
RL Load	3.0 Ω/0.5 mH
Fundamental phase current amplitude	33 A
Fundamental output frequency	50 Hz
Rated output power	5 kW

capacitors [16]. Thus, the active miller clamp function of ACPL-332J was utilized to depress the miller effect. Besides, the desaturation protection method was utilized by monitoring the on-state drain-source voltage of the SiC MOSFET to avoid shooting through fault.

The gate driver is a four-layer printed circuit board (PCB). In each gate loop, the emitter lines and gate lines are routed at different layers. The DC-DC converters are separately placed at another PCB which connects the gate drive board via the pins. Through such a design, the gate loop is perpendicular to the power loop of the HyS module. The trenches are dug everywhere isolation is needed to ensure the safety. The gate driver board is soldered to the gate pins of the HyS power module to minimize the parasitic inductance within gate loop. Details of the gate driver can be found in [27].

Test procedures are as follows. At first, only the Si IGBTs in the HyS power modules were switched. The SiC MOSFETs were kept in off state. The switching frequency was 5 kHz. Then the gate sequence with the fixed t_{on_delay} of 1 us (Option 2) and −1 us (Option 3) respectively and the fixed t_{off_delay} of 0.5 us was applied. The switching frequency remained

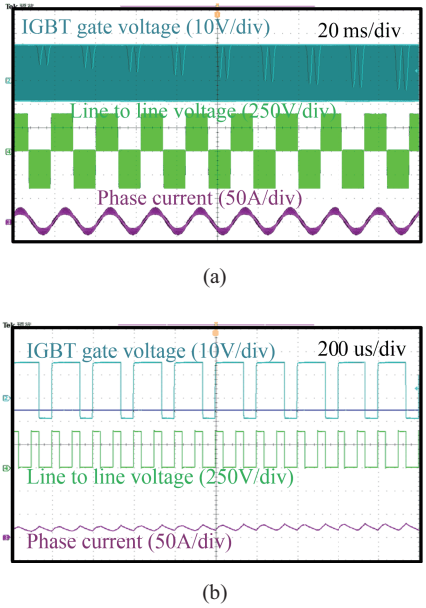

Fig. 16. Experimental waveforms of the three-phase voltage source inverter. Only the Si IGBTs were switched. (a) Gate voltage, line to line voltage and phase current waveforms. (b) Zoom-in waveforms. Switching frequency was 5 kHz. (200 us/div)

as 5 kHz. At last, the gate sequence with non-constant t_{off_delay} (Option 1) was utilized. t_{on_delay} was set to be 0 us. The switching frequency was 5 kHz, 10 kHz, and 30 kHz respectively. The gate sequences were realized through the PWM module of the DSP F28335. Experimental waveforms are demonstrated from Fig. 16 to Fig. 19. The gate voltages were obtained at the lower leg of the middle HyS power module and the positive phase current flowed through the HyS.

Fig. 16 displays the experimental waveforms of the three-phase voltage source inverter. Only the Si IGBTs within the HyS power modules were switched. Gate voltage of the SiC MOSFETs was kept at −5 V to disable the switches. There were almost no disturbances on the gate voltage of the SiC MOSFETs at the switching transients of the Si IGBTs. Switching frequency was 5 kHz. PT1000 thermistor was attached to the baseplate of the middle HyS power module. Baseplate temperature was utilized as an indicator of the HyS power loss. Air flow of the fans is 0.5 m^3/min. As the output power increased from 1 kW to 5 kW, the baseplate temperature rose from 25 °C to 50 °C.

Fig. 17 displays the experimental waveforms of the three-phase voltage source inverter utilizing the gate sequence Option 2 with the fixed t_{on_delay} of 1 us and the fixed t_{off_delay} of 0.5 us. Si IGBTs were turned on prior to the SiC MOSFET. With a positive t_{off_delay}, the Si IGBTs are expected to be turned off prior to the SiC MOSFET. However, a short t_{off_delay} may be not enough. There are two reasons for the increase of the gate voltage of the Si IGBTs (shown in Fig. 17(d)). The first one is the miller effect. Even though an active miller clamp circuit was utilized, the circuit was not supposed to work when the gate voltage of the Si IGBTs was still high. That is, a short

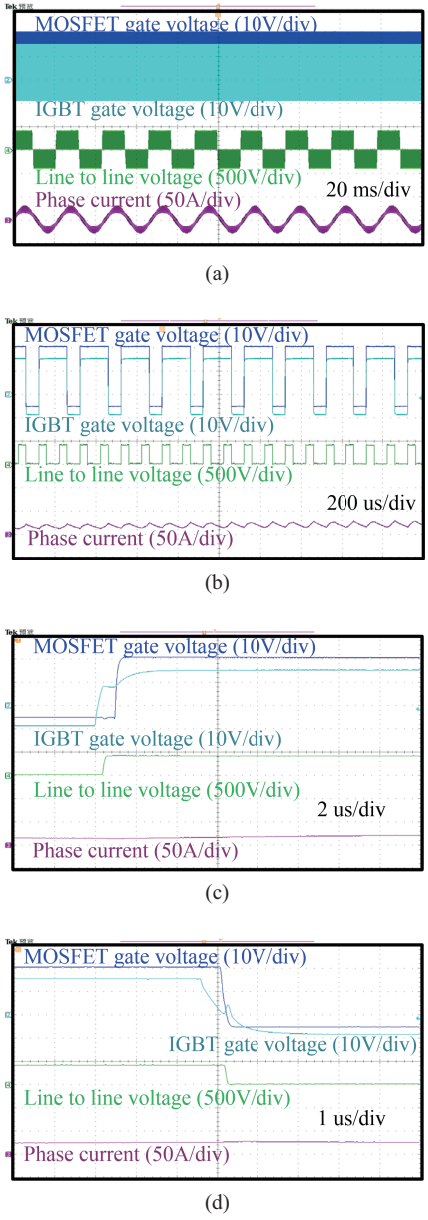

Fig. 17. Experimental waveforms of the three-phase voltage source inverter. Gate sequence Option 2 with the fixed t_{on_delay} of 1 us and the fixed t_{off_delay} of 0.5 us was applied. (a) Gate voltages, line to line voltage and phase current wave-forms. (b) Zoom-in waveforms. Switching frequency was 5 kHz. (200 us/div) (c) Zoom-in waveforms at the turn-on instant. (d) Zoom-in waveforms at the turn-off instant. The Si IGBTs turned on again at the turn-off moment of the SiC MOSFET because t_{off_delay} was small for the load current.

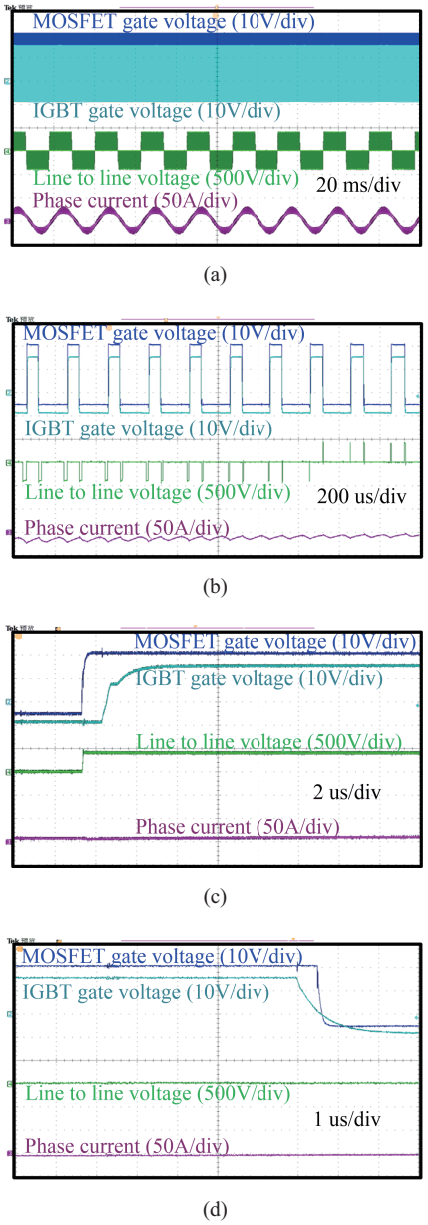

Fig. 18. Experimental waveforms of the three-phase voltage source inverter. Gate sequence Option 3 with the fixed t_{on_delay} of −1 us and the fixed t_{off_delay} of 0.5 us was applied. (a) Gate voltages, line to line voltage and phase current wave-forms. (b) Zoom-in waveforms. Switching frequency was 5 kHz. (200 us/div) (c) Zoom-in waveforms at the turn-on instant. (d) Zoom-in waveforms at the turn-off instant. The Si IGBTs did not turn on again at the turn-off moment of the SiC MOSFET because t_{off_delay} was long enough for the load current (Load current was negative and did not flow through the HyS).

t_{off_delay} may disable the function of miller clamp circuit. The second reason is that the depletion layer expands toward the collector within the N- region of the Si IGBTs, which not only drives the excess carriers away from the N- drift region but also makes an accumulation layer form under the P+ collector. Hereby, both collector current and gate voltage rise. Both phenomena can not be avoided and can become severer at a larger current. A longer t_{off_delay} is helpful for suppressing the effects.

The baseplate temperature rose from 25 °C to 35 °C as the output power increased from 1 kW to 5 kW. Better performance of the HyS compared with the pure Si IGBTs was observed.

As shown in Fig. 18, compared with the gate sequence Option 2, the gate sequence Option 3 reduces the turn-on loss. Thus, a lower baseplate temperature as 30 °C was obtained at the output power of 5 kW.

Fig. 19 displays the experimental waveforms utilizing the gate sequence Option 1. The lowest temperature was observed because it fully utilized the potential of the HyS. As switching frequency increased to 30 kHz, the baseplate temperature was 67 °C at the rated output power. Replacing the fans with the water-cooling plates, the inverter was tested at 30 kW/ 30 kHz,

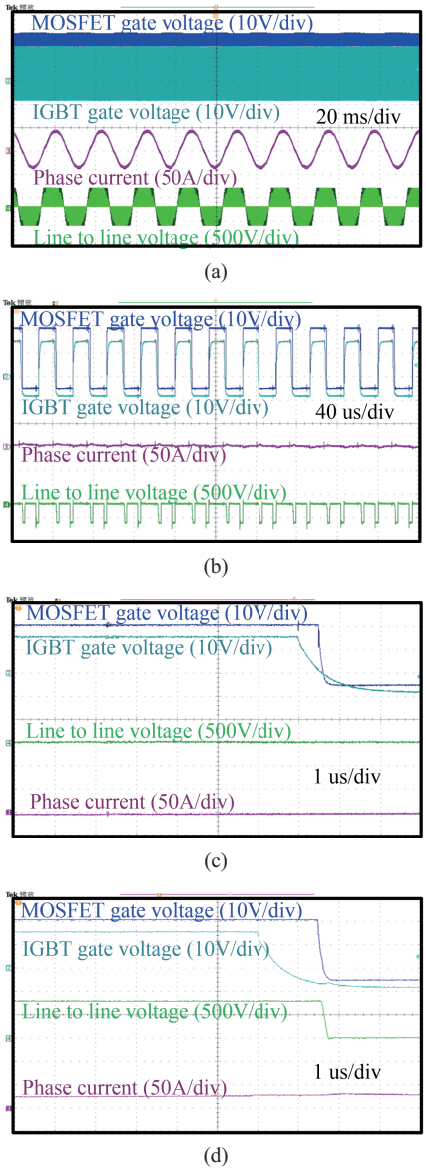

Fig. 19. Experimental waveforms of the three-phase voltage source inverter. Gate sequence Option 1 with the non-constant t_{off_delay} was applied. (a) Gate voltages, line to line voltage and phase current waveforms. (b) Zoom-in waveforms. Switching frequency was 30 kHz (40 us/div). (c) Zoom-in waveforms at the turn-off instant. Small t_{off_delay} (0.5 us) was utilized because of the little load current. (d) Zoom-in waveforms at the turn-off instant. Large t_{off_delay} (1.5 us) was utilized because the load current became larger.

shown in Fig. 20. Inlet cooling temperature was set to be 30 °C.

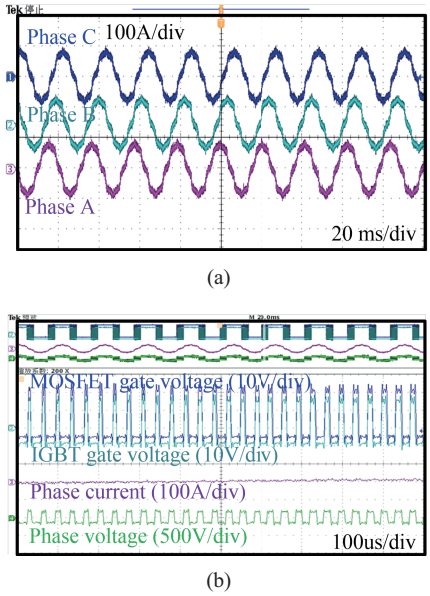

Fig. 20. Experimental waveforms of the voltage source inverter (30 kW/30 kHz). (a)Three phase current. Amplitude of the current was 100 A. (b) Zoom-in waveforms. Switching frequency was 30 kHz. DC bus voltage was 550 V.

VI. Conclusion

A Si IGBT/SiC MOSFET HyS power module was packaged. The Si/SiC current ratio is 4:1. A novel index is proposed to determine the optimal prior turn-off period of the Si IGBTs. Compared with the pure Si IGBTs, the HyS can operate at a higher switching frequency with the reduced power loss. A 5 kW air-cooling voltage source inverter and a 30 kW water-cooling voltage source inverter were built for verification. The main features of the paper are as follows.

(1) HyS phase-leg power modules were fabricated and fully tested for the first time.

(2) A method to select the optimal gate sequence for the HyS is presented.

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