Control Techniques of the Auxiliary-Resonant Commutated Pole With Special Regards on the Dual-Active Bridge DC-DC Converter

Johannes Voss, Jochen Henn, and Rik W. De Doncker

***Abstract*—In this work, a dual-active bridge dc-dc converter with auxiliary-resonant commutated pole is presented. The paper focuses on the control strategies of the auxiliary-resonant commutated pole to allow soft turn on and soft turn off of the main switches, and thus increasing the efficiency of the converter. These strategies are developed for a high-power IGCT-based dual-active bridge dc-dc converter. Two boosting strategies, constant time magnetization and constant current boosting are presented and tested. Besides its main objective to reduce the switching losses, the ARCP also allows balancing of the dc-link voltages in case of imbalanced loads. Strategies for boost current control and active dc-link balancing are introduced, presented and experimentally verified on a small-scale laboratory setup.**

***Index terms*—DC-DC power converters, field programmable gate arrays, resonant inverters, soft-switching, zero-voltage switching.**

I. Introduction and Motivation

In Fig. 1, the schematic of a dual-active bridge (DAB) dc-dc converter with auxiliary-resonant commutated pole (ARCP) is shown. In case one of the main devices is switched, the ARCP causes a resonance to allow a zero-voltage condition at the main devices which then results in soft switching. This soft-switching behavior can be supported by additional resonant capacitors C_{res}. In case of using ARCP with IGCTs, it has been shown that the switching losses can be reduced to an eighth of the original amount [7]. Further details on the DAB can be found in [1] and [8] and on the ARCP in [2] and [9]. The presented control techniques for the ARCP are developed for a 5 MW DAB. Therefore, some presented hardware components are designed for 5 kV and fiber optical logic signals are used. The techniques are tested on a smallscale model (SS-DAB) rated for powers in the lower kW range to minimize risks.

A. Auxiliary-Resonant Commutated-Pole for Dual-Active Bridge

As described in [1], a two-level three-phase DAB operates in six-step mode where each bridge is switched with a constant duty cycle of 50%. The three phases of the bridge are shifted by 120° generating a six-step voltage waveform at the transformer terminal. The phase shift between the primary and secondary bridges causes a voltage drop across the transformer leakage inductance, resulting in a power flow.

In partial load conditions or unsymmetrical input/output voltages, the DAB converter loses its soft-switching capability because there is not enough reactive current to discharge the snubber capacitors of the turning off device. Hence, the turning off devices are hard switched. The ARCP circuit is a promising technique to overcome this problem, thus extending the soft-switching capability of the DAB. The main principle is to force a resonance just before a commutation process from a bottom switch to a top switch (BtT) or vice versa (TtB) so that the snubber capacitors in parallel to the switched device are fully discharged and charged, respectively [2], [4]. The main switch is then triggered under a zero-voltage condition. Especially thyristor-based turn-off devices (GTOs or IGCTs) have a deeper charge carrier saturation [3] and, therefore, introduce higher switching losses as compared to their competitive devices, e.g. Insulate-Gate Bipolar Transistors (IGBTs). To overcome the drawback of high switching losses and to take advantage of the superior conduction behavior of IGCTs, an ARCP can be applied to the DAB.

B. Control Techniques Supporting Soft-Switching

In Fig. 4, one phase-leg of the three-phase DAB with ARCP (DAB ARCP) is shown. A more detailed description of the basic ARCP principle can be found in [2] and [5]. The auxiliary inductor L_{AUX} needs to be tuned, according to the di/dt characteristics of the device in the converter with the lowest di/dt capability. In case the converter legs consist of IGBTs, no restriction for di/dt exists. However, IGCTs have di/dt limitations (e.g. 800 A/μs) which make a conservative design of L_{AUX} necessary.

Furthermore, Fig. 4 introduces a zero-voltage detection (ZVD). This ZVD is needed to switch on the main devices during the zero-voltage condition and to protect them from short-circuiting the resonant capacitors C_{res} in case they are not completely discharged. Since the resonance phase is in the range of 10-30 μs the ZVD must be very fast to avoid a flip back of the voltages across the resonant capacitors. A controller unit triggers the switch via the ZVD: whenever the ZVD

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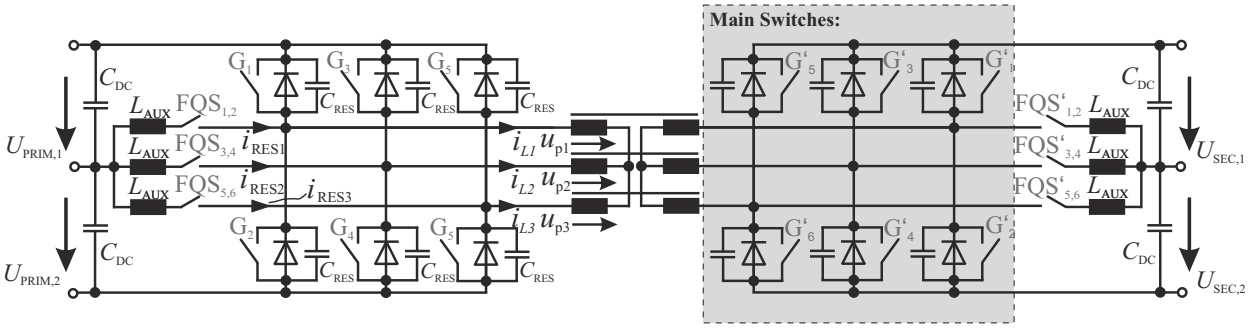


Fig. 1. Dual-active bridge with auxiliary-resonant commutated pole.

TABLE I
SPACE VECTORS (SV) AND THYRISTOR TRIGGERING SIGNALS FQS FOR ONE CONVERTER

Time Sequence	SV	FQS	State
$-T_{discharge} < t < 0$	000000	000000	0
$-T_{trg} < t < 0$	010101	010000	0-1
$0 < t < T_{sw}/6$	100101	000000	1
$T_{sw}/6 - T_{trg} < t < T_{sw}/6$	100101	000100	1-2
$T_{sw}/6 < t < 2T_{sw}/6$	101001	000000	2
$2T_{sw}/6 - T_{trg} < t < 2T_{sw}/6$	101001	100000	2-3
$2T_{sw}/6 < t < 3T_{sw}/6$	011001	000000	3
$3T_{sw}/6 - T_{trg} < t < 3T_{sw}/6$	011001	000001	3-4
$3T_{sw}/6 < t < 4T_{sw}/6$	011010	000000	4
$4T_{sw}/6 - T_{trg} < t < 4T_{sw}/6$	011010	001000	4-5
$4T_{sw}/6 < t < 5T_{sw}/6$	010110	000000	5
$5T_{sw}/6 - T_{trg} < t < 5T_{sw}/6$	010110	010000	5-6
$5T_{sw}/6 < t < 6T_{sw}/6$	100110	000000	6
$6T_{sw}/6 - T_{trg} < t < 6T_{sw}/6$	100110	000010	6-1

detects a turn-on signal and a zero-voltage condition at the main device, it is triggered on (logic AND). In case the controller unit generates a trigger signal without having zero-voltage condition, the ZVD does not trigger the main devices and thus avoiding a snubber dump.

As given in literature [8], [2] and [11], a boost current is an additional current which is needed to overcome losses during switching and to force a current into the anti-parallel diodes.

In this paper, two boosting strategies are introduced: the constant boost time and the constant boost current. By iterative simulation and loss estimation, the minimal boost time can be determined for various but steady operating points of the converter, as it has been shown in [10]. Instead of setting a constant boost time, a constant boost current can be obtained by using additional hardware. Since in dc grids a voltage variation of +/−10% may exist, a constant boost time will lead to different boosting currents, i.e. an increased dc-link voltage causes a linear increasing ARCP peak current. By choosing a constant boost current technique, it is guaranteed to have the same boost current in every operation point of the converter.

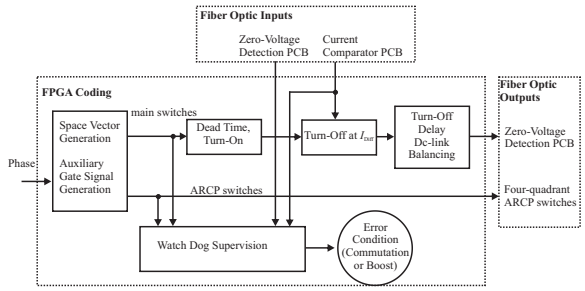


Fig. 2. Structure of the control algorithms in the FPGA.

II. CONTROL OF THE DAB WITH ARCP

In this section the generation of gate signals is explained. The code has been verified in Matlab/Simulink using the Xilinx System Generator. In TABLE I, the switching sequence for the space vectors (SV) controlling the main converter legs and the four-quadrant switches (FQS) for the auxiliary branch are programmed on the FPGA[1]. Since thyristors are line-commutated devices, '0' does not necessarily mean that the device is not conducting current. Whenever the thyristors is triggered it carries current until it decays to zero. During $T_{discharge}$ the resonant capacitor has to be discharged by the zerostate chopper (ZSC). Without using a ZSC, the converter is not able to start from an initial space vector '000' as given in the TABLE I with state 0, since the snubber capacitors of the device would share the dc-link voltage equally and the ZVD will not allow to trigger the main devices. Hard-switching with IGBTs might not be a critical, due to their high over current capability without d*i*/d*t* limitation. In case of IGCTs this is crucial aspect. T_{sw} defines the switching period and T_{trg} marks the magnetization time of the resonant inductor. Whenever a state should be changed, the corresponding FQS is triggered to realize the resonant commutation of a leg (e.g. from state 0 to state 1 only FQS_1 must be triggered). In total, 12 gate signals for the main switches and 12 FQS signals are generated for the primary and secondary side. As shown in Fig. 2 a turn-on delay is embedded to prevent a short circuit on the dc link in any case. The turn-off block given in Fig. 2 is only applied when constant boost

[1] '1' means a switch is triggered on, and '0' a switch is not triggered, e.g. $SV(G_1,G_2,G_3,G_4,G_5,G_6)$ = '000000' means all switches are not triggered.

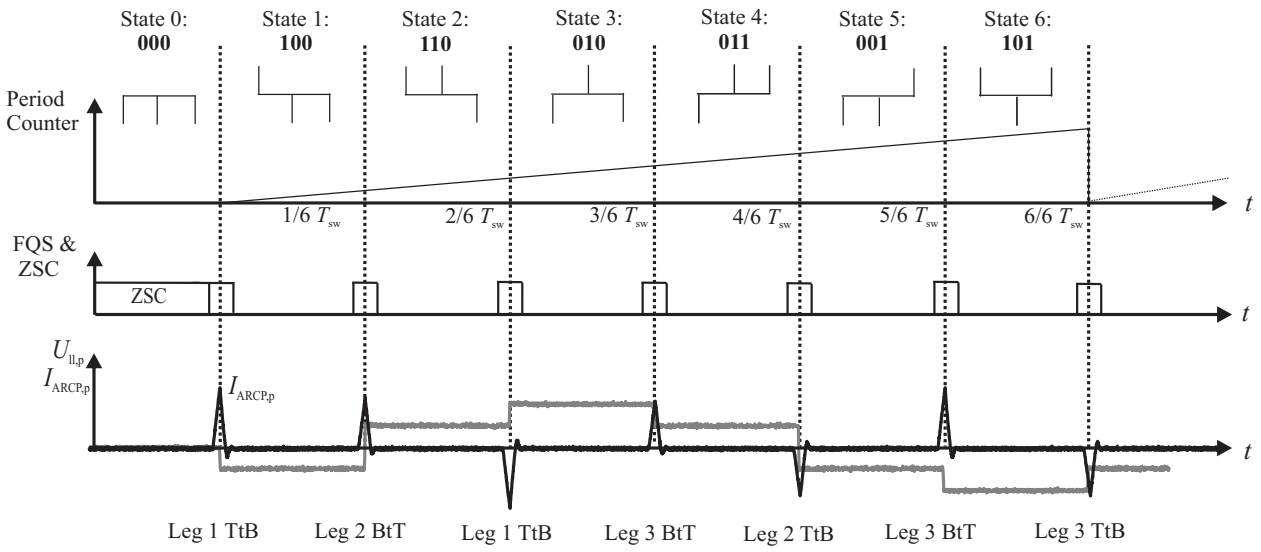


Fig. 3. Space vectors and the resulting phase voltage of the 3PH DAB including the ARCP currents.

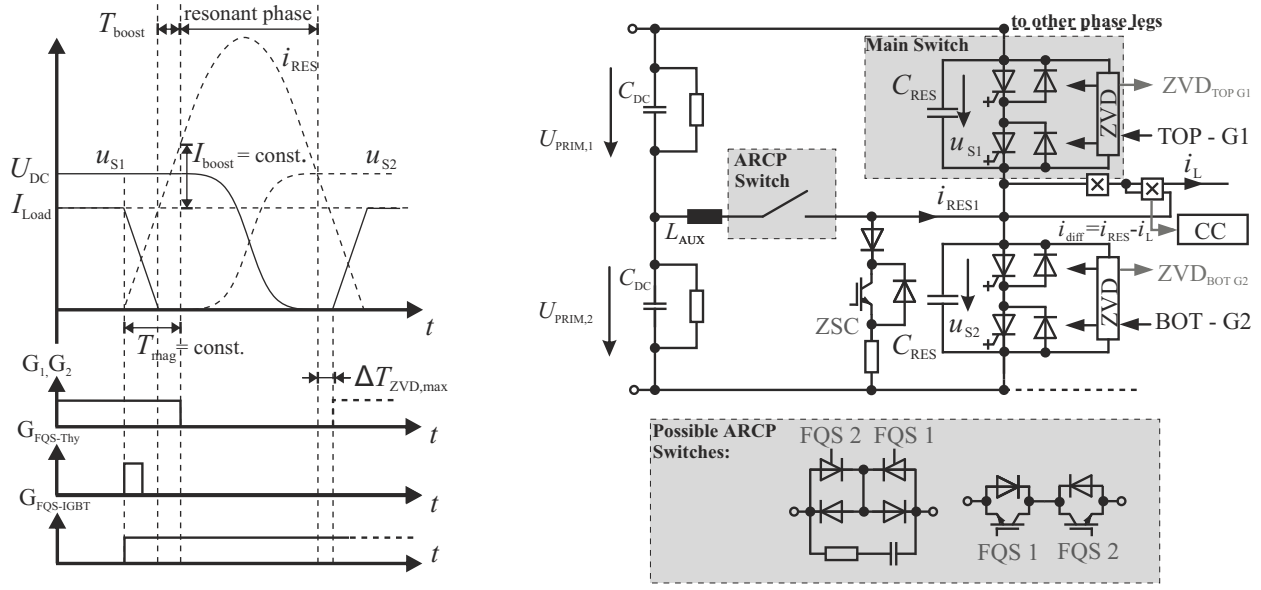


Fig. 4. Boosting strategies for ARCP current: Either constant magnetization time or constant boost current using comparator PCB.

current mode is applied, which will be explained in the next section.

In TABLE I and TABLE II, the basic timings for the main switches and the FQS are given. Various topologies of semiconductor for the four-quadrant switch (FQS) are possible. Since the resonant phase ends at a zero-current crossing line-commutated and forced-commutated devices can be utilized. In case of line-commutated devices, namely thyristors, only a short trigger impulse has to be applied to start the resonant phase. If forced-commutated devices are used (e.g. MOSFETs, IGBTs or IGCTs), the devices are not allowed to turn off during current commutation. A good solution, is adding up twice the magnetization-time (rising, boosting and falling) of the auxiliary inductor plus the time of the resonant phase as defined in [2], in worst case condition. If the device would be turned off before the current decays to zero, the auxiliary inductor would cause an over-voltage condition at the device.

In Fig. 3 the SV given for each converter leg are depicted with the timing constrains for thyristor-based FQS and the ZSC. The resulting six-step voltages of the DAB and the resonant current i_{res} of the ARCP are plotted below.

A. Commutation Control

The boost current is essential for a proper commutation. Whenever the current in the device that is about to be turned off is negative, and thus the anti-parallel diode is conducting, the current needs to be reversed for the commutation. In this operation mode, the current in the auxiliary branch must be higher than the load current to overcome losses during the

TABLE II
SPACE VECTORS (SV) AND IGBT TRIGGERING SIGNALS (FQS) FOR ONE CONVERTER

Time Sequence	SV	FQS	State
$-T_{\text{discharge}} < t < 0$	000000	000000	0
$-T_{\text{trg}} < t < +2 \cdot T_{\text{trg}}$	010101	010000	0-1
$0 < t < T_{\text{sw}}/6$	100101	000000	1
$T_{\text{sw}}/6 - T_{\text{trg}} < t < T_{\text{sw}}/6 + 2T_{\text{trg}}$	100101	000100	1-2
$T_{\text{sw}}/6 < t < 2T_{\text{sw}}/6$	101001	000000	2
$2T_{\text{sw}}/6 - T_{\text{trg}} < t < 2T_{\text{sw}}/6 + 2T_{\text{trg}}$	101001	100000	2-3
$2T_{\text{sw}}/6 < t < 3T_{\text{sw}}/6$	011001	000000	3
$3T_{\text{sw}}/6 - T_{\text{trg}} < t < 3T_{\text{sw}}/6 + 2T_{\text{trg}}$	011001	000001	3-4
$3T_{\text{sw}}/6 < t < 4T_{\text{sw}}/6$	011010	000000	4
$4T_{\text{sw}}/6 - T_{\text{trg}} < t < 4T_{\text{sw}}/6 + 2T_{\text{trg}}$	011010	001000	4-5
$4T_{\text{sw}}/6 < t < 5T_{\text{sw}}/6$	010110	000000	5
$5T_{\text{sw}}/6 - T_{\text{trg}} < t < 5T_{\text{sw}}/6 + 2T_{\text{trg}}$	010110	010000	5-6
$5T_{\text{sw}}/6 < t < 6T_{\text{sw}}/6$	100110	000000	6
$6T_{\text{sw}}/6 - T_{\text{trg}} < t < 6T_{\text{sw}}/6 + 2T_{\text{trg}}$	100110	000010	6-1

commutation and to accomplish the commutation within a reasonable time. Here, two techniques are presented:

1) Fixed Magnetization Time

In terms of control effort, keeping the magnetization time constant is a straight forward approach. The magnetization must greater than the rising time and the minimal required boosting time. The FPGA is set up to trigger the FQS a certain time before the main switches transition. This time can either be kept constant overall operating points or adjusted by the controller according to system voltage and phase current amplitudes. Anyway changing the time according to the operation point of the converter can be challenging during operation.

Fig. 5(a) and (b) depicts the effect of changing system voltages on the resonant currents at a constant boost time.

Except for ease of control, this approach has the following drawbacks: for commutations at negative phase currents, constant magnetization time will increase the device stress during turn-off for the bottom main switches, as it adds the full resonant current to the load current, thus increasing the resulting current in the switch. This unnecessary current causes losses in all devices taking part in these commutations.

However, constant boost time has the natural capability of balancing the dc-link voltages. Whenever one of the two dc-link capacitors connected in series is unbalanced, the auxiliary inductor is magnetized with a higher peak current. As shown in Fig. 5(c), an increased amount of energy is pushed into the corresponding capacitor.

2) Constant Boost Current

The drawbacks of a control based on equations and calculations for optimal boost time [10] can be overcome by dynamically terminating the boost sequence. This can be

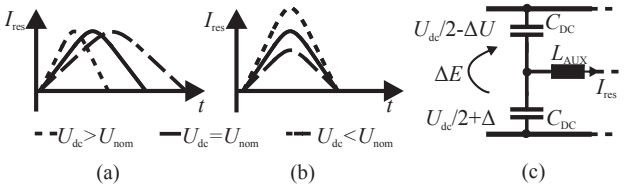


Fig. 5. Impact of dc-link voltage variation on constant boost current strategy (a) or constant boost time strategy (b) and increasing boost current during bottom to top transition for dc-balancing purposes (c).

achieved by monitoring the difference of resonant and load current i_{RES}-i_{L} using an additional sensing. If this difference reaches a certain limit I_{lim}, the FPGA will turn off the according main switch, stopping the inductor magnetization. This way, the influence of load current and voltage amplitude are rejected and the boost current is kept constant. The increased hardware effort is a clear drawback of this approach. Adjusting the turn-off time of the main switches according to the incoming signal is a small extension of the existing FPGA code.

B. DC-Link Balancing Using Variable Boost Currents

The ARCP circuit is connected to the midpoint of the dc-link, thus the DAB converter can be used in bipolar dc systems. For a system with unbalanced loads, the DAB ARCP can provide voltage balancing capabilities. The following subsections will discuss the natural and active dc-link balancing behavior of the ARCP as well as the control approach taken. A hysteresis controller enables active dc-link balancing for variable set and reset boundaries as shown in Fig. 9(c). Both, the upper and lower dc-link voltages are monitored and therefore the DSP is able to determine how to counteract the imbalanced voltages. Fig. 2 depicts the block 'turn off delay' which allows to extend the magnetization time of the auxiliary inductor. To balance the dc-links only the magnetization time for one component is extended. E.g. if the upper dc-link $U_{\text{PRIM,1}}$ is lower compared to the second one $U_{\text{PRIM,2}}$, the boost time of the FQS2, FQS4 and FQS6 is extended. In case, the dc-link of $U_{\text{PRIM,2}}$ is lower, the boost time of FQS1, FQS3 and FQS5 is adjusted. As a result the ARCP currents are asymmetrical and thus the power transferred between the dc-link capacitors is asymmetrical as well. The basic topology behind the ARCP is a push-pull converter. Based on this knowledge, it would be possible to define a transfer function with a disturbance coupling according the load current i_{L}. Here, for simplicity, only a hysteresis controller is embedded. Whenever the voltage differs more than 20% from half the sum of the two measured dc-link voltages - nominal $U_{\text{dc}}/2$ - the hysteresis control is engaged until the difference of the virtual $U_{\text{dc}}/2$ is less than 2%.

III. SIMULATION OF PROPOSED CONTROL TECHNIQUES

The simulations are performed in Matlab Simulink/PLECS and the VHDL code is integrated using the Xilinx System Generator. In Fig. 6, the results of the simulations are shown. At the beginning of the simulation, the zero-state chopper is activated until the resonant capacitors at the bottom switches are

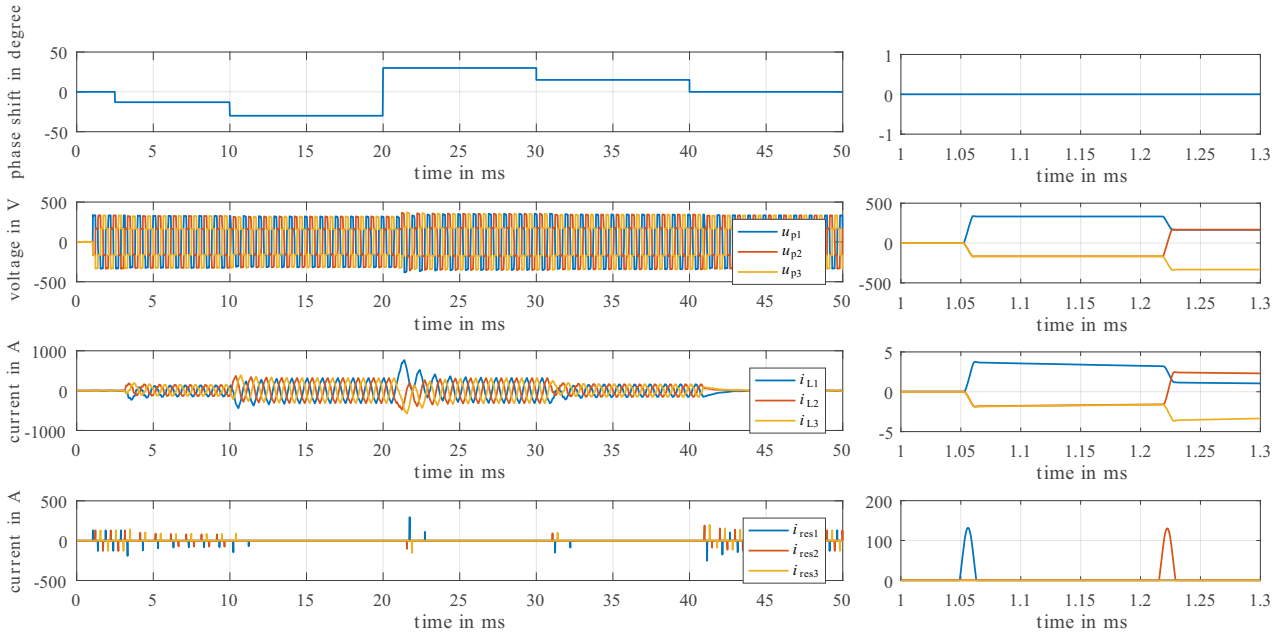


Fig. 6. Performed simulation of the FPGA code using the Xilinx System Generator.

completely discharged, equivalent to state 0.

In the first plot of Fig. 6, the phase shift is given in degree. In the second plot, the phase voltages, phase currents and, finally the ARCP currents are depicted. On the right-hand side, a zoomed in of the start-up procedure is shown. Here, the converter is initiated, using the zero-state of the SVM. The transition of the first interval is supported with the ARCP branch, up to approximately $t = 4$ ms.

The phase shift is increased afterwards. Due to transient effects which results in dc-voltage-offsets, the ARCP is activated only at some switching transitions since the phase current does not reach the specified minimum load current for natural soft switching.

At $t = 10$ ms, the phase-angle is changed to its maximum and the converter is running at nominal load. Now the phase current is beyond the minimum load current for soft switching and the ARCP is left turned off. This operation area is named as natural soft-switching mode since no additional reactive power is needed to allow zero-voltage switching. The nominal power is reversed at $t = 20$ ms. The very fast change of the load causes very high peak currents during the transition.

The current comparator equivalently reacts on this current and ensures soft-switching during this event. This could be avoided using ICC as proposed in [12]. However, using ICC additional timing constrains regarding minimum intermediate steps must be considered.

Afterwards, the power is decreased equally and the con-verter is running in forced soft-switching mode again.

IV. Small-Scale Laboratory Setup

Here, the experimental setup of the small-scale dual-active bridge (SS SAB) is introduced. The utilized hardware is pictured in Fig. 7. The schematic is given in Fig. 8. The dc-link

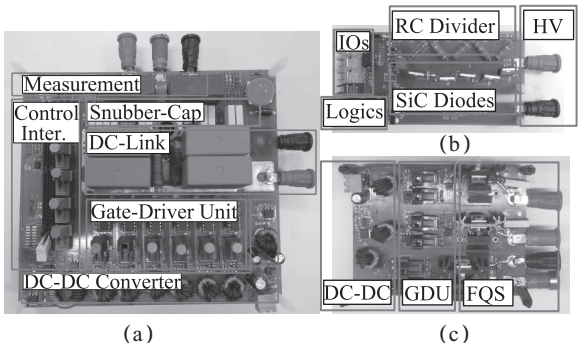


Fig. 7. Pictures of components in the experimental setup.

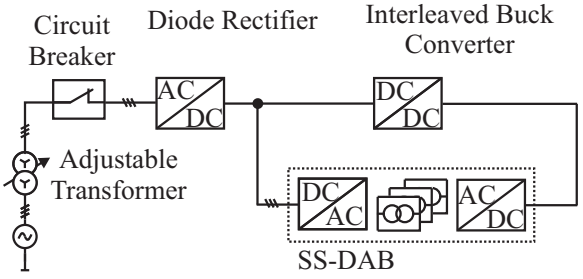
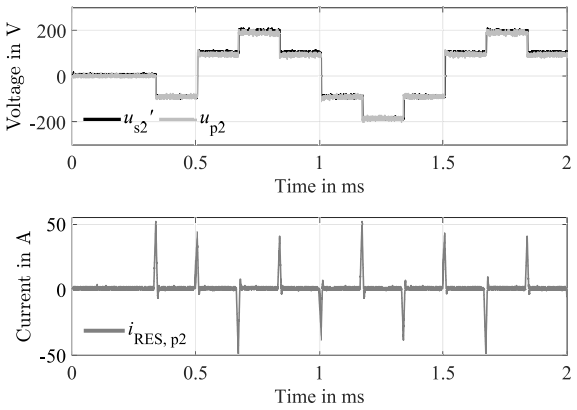


Fig. 8. Simplified schematic of the SS DAB laboratory setup.

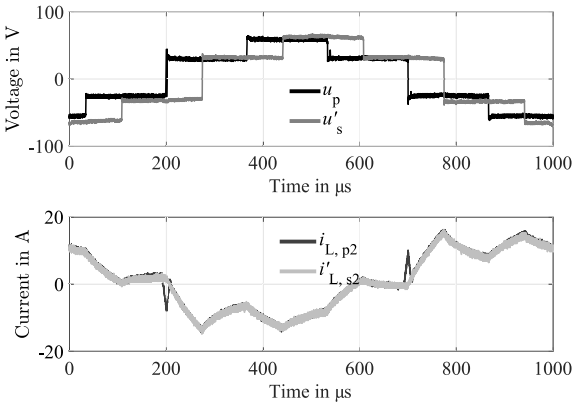
is powered by an adjustable transformer with a diode rectifier to test the strategies under varying voltage conditions.

A. Voltage-Source Converter

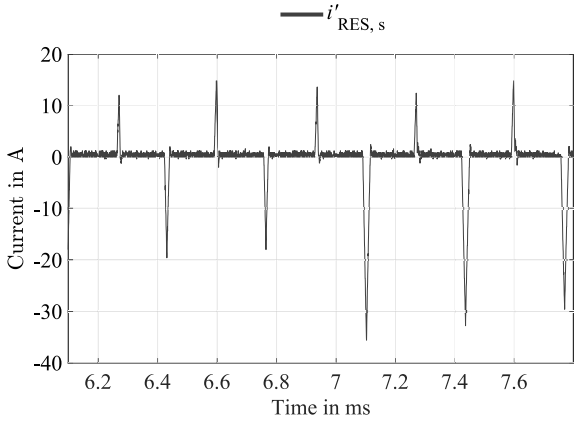
The three-phase input and output converters as well as the buck converter are independent systems incorporating a fiber optic input/output interface (I/O), galvanically isolated GDUs,



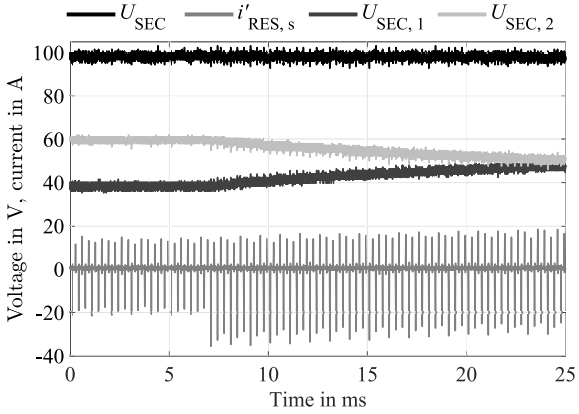
(a) Characteristic voltages of the DAB during start-up procedure for DAB-ARCP operation and primary resonant currents of all phases.



(b) Primary and secondary transformer voltages and phase currents with auxiliary current for primary side at 45° phase shift. Boost currents visible in I_L at t = 200 µs and 700 µs



(c) Engaging active balancing of dc-links with hysteresis controller at t = 7 µs.



(d) Detailed view of I_{ARCP} in Fig. 9(c) around t = 7 µs.

Fig. 9. Experimental results part 1.

an IGBT module and a heat sink. The IGBT modules are mounted under the PCB on a heat sink and not visible in Fig. 7(a). The converter is state-of-the-art topology with additional snubber capacitors mounted at the output side. If the converter is used as an independent system, a TI F28335 DSP can be plugged in and programmed via USB interface.

B. Four-Quadrant Switches for ARCP

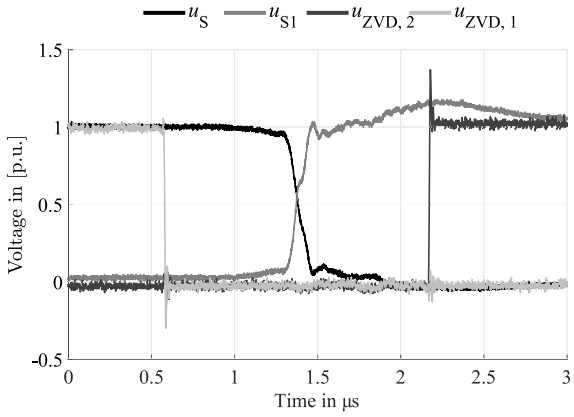
In this work, both types of FQS based on thyristors and on IGBTs are used. Both topologies have advantages and disadvantages. From control perspectives, thyristors are beneficial since they turn off at a zero crossing. However, most common thyristors are not designed for higher switching frequencies, resulting in restrictions for di/dt and dU/dt and during soft-start sequences of the converter. Fig. 7(c) show a version with thyristors.

C. Zero-Voltage Detection and Current Comparator

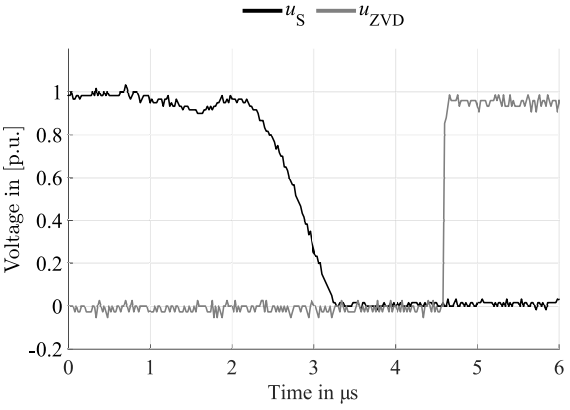
The ZVD is necessary to prevent the main devices from switching while their snubber capacitor is still charged. IGCTs in general are sensitive to high di/dt slopes, as their structure can cause internal hot spots if a high current immediately after a turn on occurs [13]. Since the ZVD is designed for the 5 MW, 5 kV converter zero-voltage is defined as voltage below 20 V. The ZVD is shown in Fig. 7(b).

In case of an early turn-on of the main switch, these additional devices would protect the main switches from shorting the snubbers, which is called a snubber dump. The detection PCB via the main switches in the main converter legs is directly mounted across the snubber capacitors. The basic logic is illustrated in Fig. 11. The PCB receives the gate turn-on signal from the FPGA. This signal is delayed and only passed on to the device once the voltage condition of less than 20 V is reached.

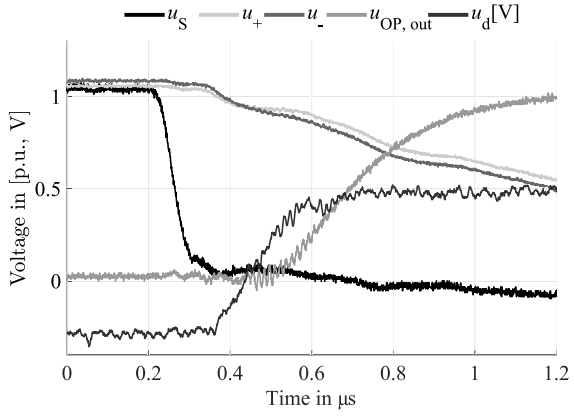
The circuit schematic of the ZVD is shown in Fig. 12. To block against the 5 kV, five SiC high-voltage (HV) diodes, each rated for 1.2 kV, are connected in series, with a typical forward voltage of 0.77 V at low currents, as indicated in Fig. 12. Their capacitance is stated to be 59 pF at 800 V. They are connected in series and terminated to ground with a Zener diode U_Z = 20 V. The voltage across the SiC diodes is balanced with an ohmic divider. Each resistor is rated for 470 kΩ. In order to maintain a predictable behavior, to reject parasitic elements and to provide a stable delay over a wide range of operating points, a constant



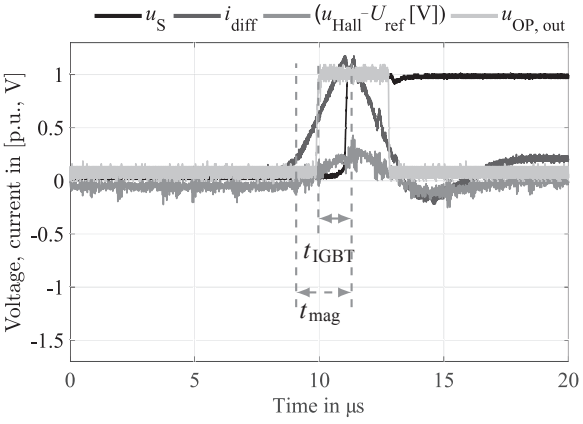
(a) Detailed voltages during a resonant commutation and voltage input of the fiber optic receiver at the main switch GDU generated by the ZVD.



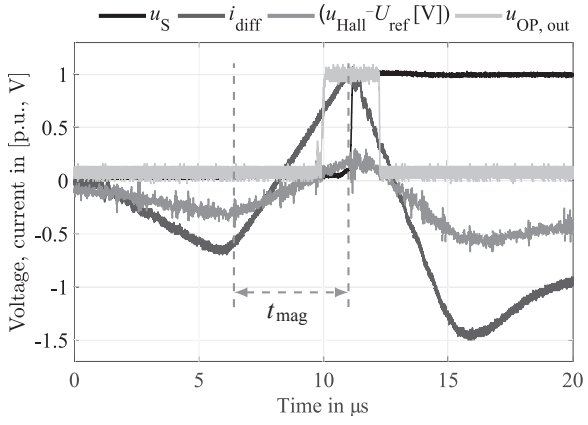
(b) Voltage of main switch and delay of ZVD during a test at 1.2 kV.



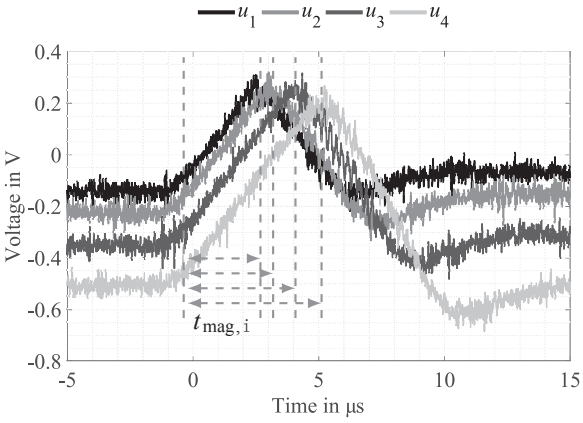
(c) Detailed probe signals of ZVD during test at 80 V.



(d) Constant boost current control at no load current condition.



(e) Constant boost current at negative load current condition.



(f) $U_i = U_{Hall}$–U_{ref} on current comparator at various operating points resulting in different magnetization times and constant current amplitudes.

Fig. 10. Experimental results part 2. measurements in (a) to (e) are in p.u.

current source supports the detection circuit. This current source is constantly feeding approximately 30 mA into the circuit. Depending on the switching state of the main switch, this current will flow through the Zener diode or into the switching path. Thus, the provided energy keeps the voltage across the Zener diode high until the current changes paths into the HV diodes. Compared to a voltage source, no additional capacitors are used and the parasitic capacitance of the Zener diode is not increased. An adjustable voltage divider provides a reference voltage U_+ for the comparator as indicated in Fig. 12. For low voltages across the switch or a short between U_S and ground, the current source will feed current into the switching path

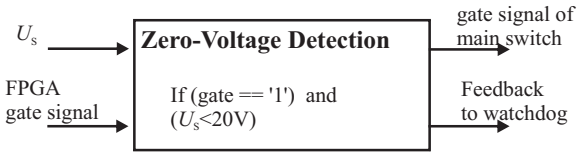


Fig. 11. Logic of zero-voltage detection.

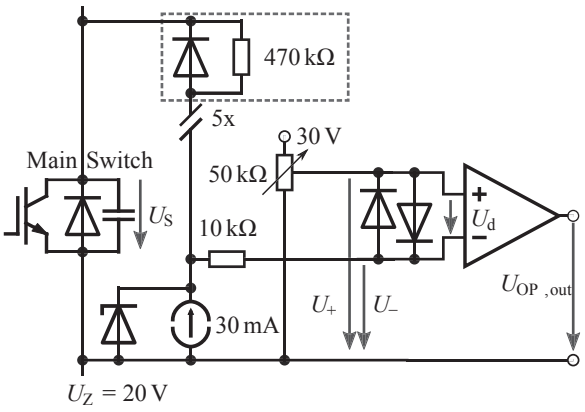


Fig. 12. Schematic of the analogue part on the zero-voltage detection PCB.

and thus pull U_- down and forward bias the protection diode in front of the comparator. Therefore, U_d is positive. Since the operational amplifier acts as a comparator, the output resembles a logical high for $U_d \geq 0$ V. In the opposite case, at a voltage greater than 20 V across the switch, the Zener diode will pull up U_-. By adjusting the reference voltage to be slightly below the Zener voltage, the delay produced by the ZVD can be minimized. Although, a safety margin should be kept in order to provide more stability. The output $U_{OP,out}$ is linked to the gate signal from the FPGA on a logic AND gate to generate the final main switch gate signal.

Another critical feature of a ZVD is its delay chain. In order to turn on the main switch as long as zero-voltage conditions are present, the ZVD should not withhold the gate signal too long. During a resonant commutation, an interval of a few micro seconds exists where the main switch is turned on under zero-voltage conditions. Delays inside the ZVD are caused by the parasitic charging, the lag of the comparator and the logic "AND" IC. The first two can be observed in Fig. 10(c). For this experiment, the reference is set close to the Zener voltage, so the delay between U_{SW} being smaller than 20 V is as short as possible. Here, it is about 100 ns. The time between $U_d > 0$ V and the output of the comparator reaching high is about 0.5µs.

D. Current Comparator

The comparator is needed to compare the current in the auxiliary branch I_{RES} to the load current I_L. Whenever I_{RES} is higher than the I_L, it can be ensured that boost current is flowing into the diode during commutation. The phase to resonant current comparator is logic high whenever the current $I_{DIFF} = I_{RES} - I_L$ is higher than a predefined limit. Since the boost current is only present during a commutation, it takes an unreasonable amount of effort to measure it directly with the DSP. Interrupt times can make it very difficult to measure with the needed speed and/or precision. It is possible to obtain the amplitude of the resonant current by measuring the phase and resonant currents and subtracting them from each other. Typical boost times are well below 15 µs. An implementation of a detection algorithm in software would delay the result for too long and the current would increase far over the desired limits. Since the FPGA is much faster compared to the DSP interrupt sequence, the approach here is to embed the function in an analogous platform.

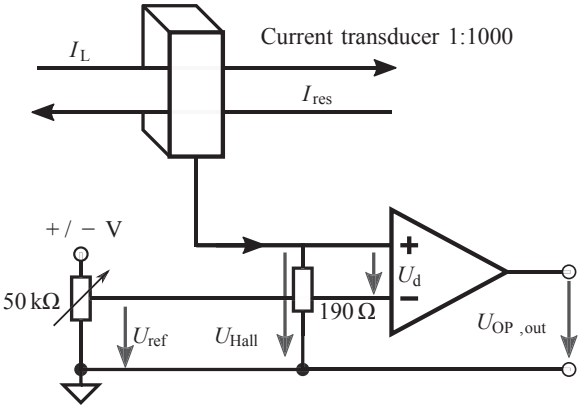


Fig. 13. Schematic of the analogue part on the current comparator PCB.

The basic principle can be described as depicted in Fig. 4 on the right side and Fig. 13 respectively. Hall-based current transducers transform the auxiliary current and the load current in such a way that the fields within the sensor compensate. With a ratio of 1:1000, the current is injected into a high-precision measuring resistors causing a voltage drop equivalent to the boost current. The resistor is connected to an operational amplifier with a high differential voltage capability. This voltage is then compared to a reference created by a variable voltage divider. Whenever the comparator detects a voltage U_{Hall}, representing the boost current $I_{boost} = I_{res} - I_L$, higher than the reference voltage, the main switch is turned off. This initiates the resonant commutation as stated in Fig. 5. The amplitude of the boost current can be adjusted by setting the reference voltage to the desired value. The reference voltage represents the minimum current $|I_{min}|$ which is needed to allow a commutation within a specified time as explained in [8]. As shown in Fig. 2, the dead time must be compensated since the main switch turn-off is delayed compared to a fixed boost time control, effecting the turn on of its complementary switch. Additionally, the delays introduced by this PCB have to be taken into account. Again, a chain of delays caused by the operational amplifier, fiber optic I/O, FPGA computation time and the turn off time of the main switch t_{IGBT} can be observed. For this application, the delay of the main switch is the major contributor to the overall delay. Note that an increased delay causes an extended magnetization time and, therefore, a tremendously increased boost current.

V. Experimental Results

In Fig. 9 and Fig. 10, the experimental results are summarized.

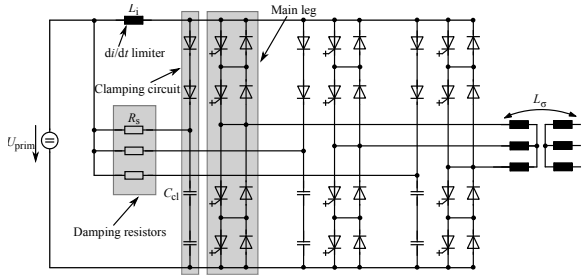


Fig. 14. Conventional snubbers for IGCT-based converters.

TABLE III
COST COMPARISON OF CONVENTIONAL IGCT SNUBBERS CIRCUIT AND ARCP SNUBBERS

	Component	No. of Dev.	Est. Price
Conventional Snubber	d*i*/d*t* limiter	2	12.5 t€
	Clamping diode	12	8.4 t€
	Clamping capacitor	12	4.8 t€
	Damping resistor	6	3.6 t€
ARCP Snubber	Snubber capacitor	48	1.5 t€
	Auxiliary inductor	2	1.6 t€
	Auxiliary switch (IGBT)	12	15.6 t€
	Radiators for IGBTs	12	1.1 t€
	GDUs IGBTs	12	0.96 t€
	ZVD PCB	12	0.5 t€
	ZCD PCB	12	0.8 t€
	Hall-based sensors	12	1.2 t€
	Total amount		−6.0 t€

In Fig. 9(a) and (b), the main operation of the converter is shown. Beginning with the start of the converter, the steady-state voltages and the resonant currents are shown in Fig. 9(a). Whenever a phase-shift is applied, the load current and the resonant current are added up as it can be observed at t = 200 µs and t = 700 µs in Fig. 9(b). In Fig. 10(a), a detailed voltage commutation in a converter leg and the ZVD signals are shown. Fig. 10(b) and (c) show the ZVD. In Fig. 10(b) a high-voltage test has been conducted and the delay of about 1 µs can be achieved over a wide voltage range. To learn more about the total delay, detailed measurements are taken at lower voltages and plotted in Fig. 10(c). Measurements taken during tests of the constant boost current mode are depicted in Fig. 10(d)−(f).

These measurements show the successful application of the introduced control techniques on a small scale test bench and validate the simulations used to design the VHDL structures. Future measurements on the full scale DAB will provide insights on efficiency improvements achieved by these techniques.

Conventional systems using IGCTs need *RCD* snubbers and d*i*/d*t* limiter to fulfill the SOA of the IGCT devices as shown in Fig. 14. In the high-power setup, the applied IGCTs 5SHY35L4510 have d*i*/d*t* limitations of 800 A/µs. The modification from a classical clamping to an ARCP system will affect the number of used components. However, the conventional snubber systems are not needed anymore. In TABLE III a cost comparison between conventional snubber and usage of an ARCP with IGBTs as auxiliary switches is given. The table considers the investment costs of the three-phase high-power DAB converter. For conventional snubbers an investment of 29.3 t€ for the high-power setup is needed. The ARCP circuit requires an investment of 23.3 t€. Embedding the ARCP would result in 6.0 t€ savings, plus the efficiency improvements which will cumulate more savings over time. A big price difference can be seen between the d*i*/d*t* limiter, the auxiliary inductors and the switches. In conventional clamping circuit the d*i*/d*t* limiter must be rated for the total dc-link current in the existing high-power setup it is water-cooled resulting in an expensive design. The auxiliary resonant inductor is only rated for the rms current during the resonant phase.

VI. CONCLUSION AND OUTLOOK

The auxiliary-resonant commutated pole seems to be an interesting technique for reducing the switching losses of a high-power 5 MW dc-dc converter based on IGCTs. The basic control is explained using space vectors and the given timing constrains regarding the ARCP branch are introduced. As a four-quadrant switch either line-commutated or forced-commutated devices can be used. The modulation is verified in a small-scale setup with FPGA/DSP based controller. The two presented boosting strategies, constant magnetization time and constant boost current, are tested in the experimental setup and results are shown. For the ARCP concept a high-speed ZVD is design and explained with a delay of approximately 1.5 µs. To compensate the delay time analog tuning is necessary. Finally, the use of an ARCP to balance the dc-link capacitors is introduced, allowing the DAB converter to operate in bipolar systems with unbalanced loads. The small-scale dual-active bridge proves the proper functionality of the control techniques. The boosting strategies can be applied directly to the 5 MW converter. In the near future the developed control will be implemented in a high-power dc-dc converter and tested to show improvements in IGCT switching behavior and an increase in efficiency.

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