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Application Range Analysis and Implementation of the Logic-Processed CPS-PWM Scheme Based MMC Capacitor Voltage Balancing Strategy

Kun Wang, Leyuan Zhou, Yan Deng, Yi Lu, Chaoliang Wang, and Feng Xu

Abstract—Fundamental frequency sorting algorithm (FFSA) is outstanding for the MMC capacitor voltage balance due to the reduced computational burden and elimination of arm current detection. However, with the traditional carrier-phase-shifted pulse width modulation (CPS-PWM) scheme, FFSA will be ineffective when the carrier frequency is higher than 250 Hz, where the line frequency is 50 Hz. Thus, previous works proposed a logicprocessed CPS-PWM scheme to overcome this disadvantage. This paper furtherly introduces the application ranges and implementation of this logic-processed CPS-PWM scheme based capacitor voltage balancing method in detail. With a detailed mathematical analysis, the factors that influence the balancing strategy's convergence speed are obtained, i.e., modulation index and power factor angle. It is found that in the applications where the modulation index is usually higher than 0.75, the influence of the modulation index is negligible. However, when the power factor angle is closed to $\pm \pi/2$, the convergence speed is almost zero. Therefore, by comparing with the traditional CPS-PWM scheme based FFSA balancing method, the application ranges of power factor angle are revealed to guarantee a high convergence speed. Meanwhile, the balancing strategy's application scope is specified. Moreover, a three-tier control architecture is demonstrated, where the logic process of driving signals and capacitor voltage sorting process are both executed in the middle-tier FPGA controller. This centralized scheme guarantees the synchronization of switching actions. And the logic process is easy and cost-effective in FPGA. Simulation and experimental results are presented to validate the theoretical analysis.

Index Terms—Balancing strategy, convergence speed, FFSA, logic-processed CPS-PWM, modular multilevel converter.

I. INTRODUCTION

MODULAR multilevel converter (MMC) has attracted great attention due to its modularity, high efficiency and scalability [1]–[3]. With these advantages, MMC is promising in medium- and high-voltage applications. Researches on modulation schemes, voltage balancing strategies and circulating current suppression strategies have been widely carried out [4]–[7]. Capacitor voltage balancing of sub-modules (SMs) is vital for the stable operation and performance of MMC.

Different kinds of voltage balancing methods have been presented in the literature. Among them, the open-loop balancing method requires no measurement of the capacitor voltages, which simplifies the design of the control system and reduces the cost [8]. However, its dynamic performance is poor. Sorting and selecting method is one of the most commonly used methods, which sorts the capacitor voltages at first and then inserts proper SMs according to the sorting result and the arm current direction [9]. Although this method is easy to implement. the high frequency sorting process leads to heavy computational burden and excessive switching actions. A reduced switchingfrequency voltage balancing strategy was proposed in [10] to reduce the switching actions of SMs. But the sorting frequency of this method is still high. Fundamental frequency sorting algorithm (FFSA) based balancing strategy is proposed in [11], which avoids the excessive switching actions and effectively reduces the sorting frequency to fundamental frequency. So, a large amount of computing resources is saved. Further studies on FFSA have been carried out in [12]-[14] under different modulation schemes, such as carrier-phase-shifted pulse width modulation (CPS-PWM), nearest level (NL) modulation and phase disposition PWM (PD-PWM). And it is found in [14] that, with CPS-PWM scheme, FFSA based balancing strategy will no longer feasible when the carrier frequency is higher than 250 Hz, where the line frequency is 50 Hz. This is caused by the little difference in the charging ability among different driving signals. Therefore, an improved balancing strategy is proposed in [14]-[15] based on the logic-processed CPS-PWM scheme. In the improved balancing strategy, driving signals with proper phase angle difference are processed by logic AND/OR process to synthesize new driving signals with obviously charging ability difference. Subsequently, the FFSA can balance the capacitor voltage under high-frequency CPS-PWM. However, the convergence speed and application ranges of the proposed balancing strategy is not analyzed in detail.

In this paper, the convergence speed of logic-processed CPS-PWM scheme based MMC capacitor voltage balancing strategy is analyzed in detail. It is found that the convergence

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Fig. 1. Structure of a typical three-phase grid-connected MMC.

speed is influenced by the modulation index and power factor angle. While, as revealed in this paper, in the applications where the modulation index is usually higher than 0.75, the influence of modulation index is negligible. However, when the power factor angle is closed to $\pm \pi/2$, the balancing strategy becomes infeasible because the convergence speed is too slow to balance the capacitor voltage. By comparing with the traditional CPS-PWM scheme based FFSA balancing method, the application ranges of power factor angle are revealed. Consequently, the proposed balancing method's application scope is specified. It is especially suitable for the high voltage direct current (HVDC) transmission, but not suitable for applications such as static synchronous compensator (STATCOM), which mainly generate or absorb reactive power. Moreover, a three-tier control architecture is also presented, where the logic-processed CPS-PWM is centralized in the middle-tier FPGA controllers for each phase. Thus, the synchronization of switching actions is guaranteed, and the logic process can be accomplished easily and cost-efficiently.

This paper is organized as follows. The principles of logicprocessed CPS-PWM scheme based capacitor voltage balancing strategy are presented in Section II. In Section III, the convergence speed is analyzed in detail, and the application ranges of power factor angle are revealed subsequently. The three-tier control architecture is demonstrated in Section IV. Simulation and experimental results verify the theoretical analysis in Section V. Finally, Section VI draws the conclusion.

II. LOGIC-PROCESSED CPS-PWM SCHEME BASED VOLTAGE BALANCING STRATEGY WITH FFSA

A. Structure of MMC

A typical structure of three-phase grid-connected MMC is illustrated in Fig. 1, where each phase leg is comprised of two arms. In each arm, N SMs and one inductor are connected in series. The SM consists of two IGBT switches and one capacitor. When S_1 is on, the SM is inserted. And it is bypassed when S_2 is on. Thus, the output voltage of SM varies between V_c and zero, where V_c is the capacitor voltage. The output voltage



Fig. 2. Principle of fundamental frequency sorting algorithm.

can be synthesized by properly inserting a certain number of SMs in upper and lower arms.

B. Traditional CPS-PWM Scheme Based Balancing Strategy With FFSA

The basic principle of FFSA is firstly introduced in [11]. In this algorithm, the capacitor voltage variations of SMs in the previous fundamental period are calculated and sorted in ascending order at the fundamental frequency. In Fig. 2, ΔV_{ch} , ΔV_{ci} , ΔV_{ci} represent the voltage variations of SM_h, SM_i and SM_{j} , and ΔV_{cseq} stores the sorting result. The voltage variations sorting result reflects the charging ability of each SM's driving signal assigned to them in the previous fundamental period. Subsequently, the driving signals sequence, namely D_{seq} , is obtained in ascending order regarding to their charging ability. Meanwhile, the capacitor voltages are sorted in descending order, obtaining the voltage sequence labeled as v_{csea} . Symbols v_{ck} , v_{cl} , and v_{cm} represent the capacitor voltage of SM_k, SM_l and SM_m , respectively. And N_{seq} stores the corresponding number of the SMs. So far, the relationship between driving signals and SMs can be rebuilt with the balancing strategy going like this: in the following fundamental period, driving signal which has the lowest charging ability will be assigned to SM with the highest capacitor voltage, e.g., D_h is assigned to SM-N_k, while driving signal which has the highest charging ability will be assigned to SM with the lowest capacitor voltage, e.g., D_i is assigned to SM- N_m . Thus, the capacitor voltage can be well balanced.

However, in this scenario, the charging ability of driving signals is related to the CPS-PWM carrier frequency. As illustrated in Fig. 3, *N* carriers are compared with the modulation signal v_{aref} to generate driving signals for the lower arm of phase *A*. Taking S_x as an example, which is generated by the x^{th} carrier, the Fourier expression of S_x can be derived as:

$$S_{lxCPS} = \frac{1}{2} + \frac{m_{\nu}}{2} \cos(\omega t + \theta_{\nu}) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} A_{mn} \cos[m(\omega_{c} t + \theta_{cx}) + n(\omega t + \theta_{\nu})]$$
(1)

where m_v is the modulation index, ω is the angular frequency of modulation signal, ω_c is the angular frequency of carrier, θ_v is the phase angle of the modulation signal, θ_{cx} is the initial phase angle of x^{th} carrier and A_{mn} is the amplitude of harmonic



Fig. 3. Illustration of CPS-PWM and logic processing of driving signals.

component, in which m is the carrier harmonic index and n is the carrier sideband harmonic index (m = 1, 2, 3, ... and $n = 0, \pm 1, \pm 2, \ldots$). So the voltage variation caused by the x^{th} carrier during one fundamental period can be calculated as:

$$\Delta V_{clxCPS} = \frac{1}{C} \int_0^T S_{lxCPS} \times i_{lA} dt = \Delta V_1 + \Delta V_2 + \Delta V_3$$
⁽²⁾

where i_{l_A} is the lower arm current of phase A and ΔV_1 , ΔV_2 and ΔV_3 represent the voltage variations caused by carrier harmonics and their sidebands that overlap the DC component, the fundamental component and the secondary harmonic, respectively. As presented in [14], if the line frequency is 50 Hz, when the carrier frequency is higher than 250 Hz, the charging abilities of each driving signal are all near to zero, which leads to the failure of balancing strategy based on traditional CPS-PWM scheme with FFSA.

C. Logic-Processed CPS-PWM Scheme Based Balancing Strategy With FFSA

In order to synthesize driving signals with obviously different charging ability when the carrier frequency is higher than 250 Hz, the logic-processed CPS-PWM scheme is proposed. As depicted in Fig. 3, carrier x and carrier y are selected in pairs as an example. Driving signal Sor is the logic OR process result of S_x and S_{yy} and S_{and} is the result of logic AND process of S_x and S_{ν} . As proved in the next section, the logic-processed driving signals, S_{or} and S_{and} possess obviously different charging ability with each other. So the logic-processed CPS-PWM scheme based balancing strategy with FFSA can be executed as follows.

Firstly, the sorting process of capacitor voltages is operated at fundamental frequency with the corresponding SM's number sequence stored in N_{seq} , as illustrated in Fig. 4. The voltage differences of each SM-pair can be obtained simultaneously, where the SMs are combined in pairs by the following rules: SM with the highest capacitor voltage is combined with the SM with lowest capacitor voltage, and the second highest SM is combined with the second lowest SM, and so on. In this paper, 2% of the rated capacitor voltage is set as the threshold to determine whether the SMs are in balance state or not. If the voltage difference overreaches this threshold, it means that the corresponding SM-pair is in unbalance state. As shown in



Fig. 4. Logic process and assignment of the driving signals.

Fig. 4, assume there are N_d pairs of SMs in unbalance state, i.e., voltage differences of the highest N_d SMs and the lowest N_d SMs ($\Delta V_1 \sim \Delta V_{Nd}$) exceed the threshold. Accordingly, N_d pairs of driving signals with proper phase angle difference are selected in S(i) and S(N-i+1), where $i = 1, 2, ..., N_d$. And the rest driving signals are stored in $S(N_d+1)$ to $S(N-N_d+1)$, which are directly assigned to the SMs in balance state. $P_{I}(i)$ and $P_{I}(i)$ represent the logic process of driving signal pairs as defined in (3) and (4), where *min* {} means selection of the driving signal with lower charging ability, and *max*{} means selection of the driving signal with higher charging ability. And then, $P_{I}(i)$ is assigned to SM- $N_{seq}(i)$, while $P_{U}(i)$ is assigned to SM- $N_{seq}(N-i+1)$. Consequently, the capacitor voltages can converge back to the balance state.

$$P_{L}(i) = \min\left\{\frac{S(i)||S(N-i+1)}{S_{or}}, \frac{S(i) \&\&S(N-i+1)}{S_{out}}\right\} (3)$$

$$P_{U}(i) = \max\left\{\frac{S(i)||S(N-i+1)}{S_{or}}, \frac{S(i) \&\&S(N-i+1)}{S_{out}}\right\} (4)$$

 S_{and}

III. CONVERGENCE SPEED AND APPLICATION RANGE **ANALYSIS**

 S_{ar}

It is clear that the charging ability difference between driving signals is the key to balance the capacitor voltages. The voltage balancing strategy may be deactivated when the charging ability difference is not so obvious. Thus, the convergence speed is analyzed in this section and the application range is revealed.

A. Convergence Speed Analysis

Similar to the traditional CPS-PWM scheme, the Fourier expression of S_{or} and S_{and} can be obtained and the voltage variations caused by them in one fundamental period can be derived as follows:

$$\Delta V_{or} \approx -\frac{I_{sm}}{\omega C} \frac{m_{v}}{2} \cos \theta \Big(m_{v} \sin \varphi_{xy} - \varphi_{xy} - \frac{\theta_{xy}}{2} + \frac{\theta_{xy} \varphi_{xy}}{\pi} \Big) - \frac{I_{sm}}{\omega C} \frac{\varepsilon_{c2\omega}}{2} \cos \left(2\theta_{v} - \theta_{c2\omega} \right) \times \Big(m_{v} \sin \varphi_{xy} + \frac{\theta_{xy} - \pi}{\pi} \sin 2\varphi_{xy} + \frac{m_{v}}{3} \sin 3\varphi_{xy} \Big)$$
(5)

$$\Delta V_{and} \approx \frac{I_{sm}}{\omega C} \frac{m_{v}}{2} \cos \theta \Big(m_{v} \sin \varphi_{xy} - \varphi_{xy} - \frac{\theta_{xy}}{2} + \frac{\theta_{xy}\varphi_{xy}}{\pi} \Big) \\ + \frac{I_{sm}}{\omega C} \frac{\varepsilon_{c2\omega}}{2} \cos(2\theta_{v} - \theta_{c2\omega}) \tag{6}$$
$$\times \Big(m_{v} \sin \varphi_{xy} + \frac{\theta_{xy} - \pi}{\pi} \sin 2\varphi_{xy} + \frac{m_{v}}{3} \sin 3\varphi_{xy} \Big)$$

where I_{sm} is the amplitude of output phase current, θ is the power factor angle, θ_{xy} is the phase angle difference of carrier x and y, and φ_{xy} is calculated as follows:

$$\varphi_{xy} = \begin{cases} 0, & 0 \leq \theta_{xy} \leq (1 - m_{v}) \pi \\ \arccos \frac{1 - \theta_{xy} / \pi}{m_{v}}, & (1 - m_{v}) \pi < \theta_{xy} < (1 + m_{v}) \pi \end{cases}$$
(7)
$$\pi, & (1 + m_{v}) \pi \leq \theta_{xy} < 2\pi \end{cases}$$

It should be noticed that the voltage variations caused by the carrier sideband harmonic are neglected in (6) since they are very small when the carrier frequency is high. Moreover, because the driving signals are logic processed in pairs and assigned to the SM-pairs simultaneously, the convergence speed of capacitor voltage can be evaluated by the difference of variations caused by S_{or} and S_{and} as shown in (8).

$$\Delta V = \left| \Delta V_{or} - \Delta V_{and} \right| = \begin{cases} 2\Delta V_{or}, & \theta \in \left[-\frac{\pi}{2}, \frac{\pi}{2} \right] \\ \\ 2\Delta V_{and}, & \theta \in \left[-\pi, -\frac{\pi}{2} \right] || \left[\frac{\pi}{2}, \pi \right] \end{cases}$$
(8)

Furtherly, since the second part of (5) and (6) is also small enough to be neglected, only the first part of the voltage variations is considered for simplification. Thus, ΔV can be simplified as follows:

$$\Delta V = 2 \left| \Delta V_{or_{\perp}} \right| = 2 \left| \Delta V_{and_{\perp}} \right|$$
$$= \frac{I_{sm} \left| \cos \theta \right|}{\omega C} m_{v} \left(\varphi_{xy} + \frac{\theta_{xy}}{2} - m_{v} \sin \varphi_{xy} - \frac{\theta_{xy} \varphi_{xy}}{\pi} \right)^{(9)}$$

It can be observed that the convergence speed is determined by active current component $I_{sm}|\cos \theta|$, modulation index m_v and carrier phase angle difference θ_{xy} . By the partial differential operation of θ_{xy} and φ_{xy} , the following equation can be obtained as:

$$\begin{cases} \frac{\partial \Delta V}{\partial \theta_{xy}} = \frac{I_{xm} |\cos \theta|}{\omega C} m_{\nu} \left(\frac{1}{2} - \frac{\varphi_{xy}}{\pi} \right) \\ \frac{\partial \Delta V}{\partial \theta_{xy}} = \frac{I_{xm} |\cos \theta|}{\omega C} m_{\nu} \left(1 - m_{\nu} \cos \varphi_{xy} - \frac{\theta_{xy}}{\pi} \right) \end{cases}$$
(10)

Assuming (10) to be zero, it can be derived that ΔV achieves its maximum value when $\theta_{xy} = \pi$ and $\varphi_{xy} = \pi/2$. Consequently, the maximum convergence speed ΔV_{max} can be calculated as:

$$\Delta V_{\max} = \frac{I_{sm} |\cos \theta|}{\omega C} m_{\nu} \left(\frac{\pi}{2} - m_{\nu}\right)$$
(11)



Fig. 5. Influence of power factor angle θ and modulation index m_v on the normalized convergence speed ΔV_{\max}^* .

Normalized by $I_{sm}/\omega C$, the relationship of ΔV_{\max}^* , m_v and θ is illustrated in Fig. 5. It can be observed that the balancing strategy has the highest convergence speed when θ equals to 0 or $\pm \pi$. While it reaches the lowest speed when θ equals to $\pm \pi/2$. And it can be seen from Fig. 5(b) that when m_v is higher than 0.75, m_v has little influence on the convergence speed. Thus, only the application range of power factor angle θ needs to be analyzed in the next subsection.

B. Application Range Analysis

It is presented in [14] that the balancing strategy's convergence speed will be degraded when there is reactive power transferred. However, the acceptable application range of power factor angle is not clearly specified. It is reasonable to take the convergence speed of traditional CPS-PWM based balancing strategy as the reference to analyze the application ranges of the proposed strategy. As demonstrated above, the traditional CPS-PWM based balancing strategy's convergence speed slows down with the increase of carrier frequency and eventually becomes infeasible when the carrier frequency is higher than 250 Hz. But it can still offer considerable speed when the carrier frequency is 150 Hz [14]. Therefore, the convergence speed of traditional CPS-PWM based balancing strategy with 150Hz carrier frequency is taken as the lowest acceptance of convergence speed for the proposed balancing strategy.

Based on the expansion of (2), the maximum and minimum



Fig. 6. Convergence speed $V_{d150Hzmax}^*$ versus the power factor angle θ and the modulation index m_{v} .

capacitor voltage variations generated by the driving signals with 150 Hz carrier frequency are calculated as (12).

$$\Delta V_{clx150Hzmax} \approx -\frac{I_{sm}}{\omega C} \frac{\pi}{2} \times A_{1(-2)} \cos(\theta_{cx1} - 3\theta_{\nu} + \theta)$$

$$\Delta V_{clx150Hzmin} \approx -\frac{I_{sm}}{\omega C} \frac{\pi}{2} \times A_{1(-2)} \cos(\theta_{cx2} - 3\theta_{\nu} + \theta)$$
(12)

where θ_{cx1} is the phase angle of carrier x_1 , $x_1 = mod$ (round $(1 + N(\theta_{c1} - 3\theta_v + \theta)/2\pi), N)$, θ_{cx2} is the phase angle of carrier $x_2, x_2 = mod$ (round $(1 + N(\theta_{c1} - 3\theta_v + \theta - \pi)/2\pi), N)$. And $A_{1(-2)}$ is the harmonic amplitude, which can be calculated as:

$$A_{1(-2)} = \frac{1}{\pi^{2}} \int_{-\pi}^{\pi} e^{j(\frac{\pi}{2}m_{v}\cos\theta + 2\theta)} d\theta$$
(13)

Thus, the maximum convergence speed with 150 Hz carrier frequency can be represented by $\Delta V_{cl150 Hz max}$ as follows:

$$\Delta V_{cl150Hzmax} = \Delta V_{clx150Hzmax} - \Delta V_{clx150Hzmin}$$

= $\frac{I_{sm}}{\omega C} \frac{\pi}{2} \times A_{1(-2)} [\cos(\theta_{cx2} - 3\theta_{v} + \theta) - (14) - \cos(\theta_{cx1} - 3\theta_{v} + \theta)]$

Normalized by $I_{sm}/\omega C$, the relationship of $\Delta V_{cl150lfzmax}^*$, m_v and θ is illustrated in Fig. 6, where $\theta_{cl} = 0$, $\theta_v = 0$, and N = 20. Fig. 6 shows that, for the traditional CPS-PWM based balancing strategy, the convergence speed is mainly determined by m_v . Compared to the logic-based CPS-PWM based strategy, when the modulation index m_v is higher than 0.75, its normalized convergence speed is always above 0.3. Therefore, $\Delta V_{max}^* = 0.3$ is taken as the lowest acceptable convergence speed of the proposed balancing strategy.

It can be calculated from (11) or read from Fig. 5(b) that the logicprocessed CPS-PWM scheme based voltage balancing strategy reaches a normalized convergence speed of 0.3 when $\theta \approx \pm \pi/3$ and $\pm 2\pi/3$. Hence the conclusion can be drawn that the application range of power factor angle is $\theta \in [-\pi/3, \pi/3] ||[-\pi, -2\pi/3]||[2\pi/3, \pi]]$. Fig. 7 illustrates the application ranges. Thus, it can be inferred that the proposed strategy is especially suitable for the HVDC



Fig. 7. Application ranges of power factor angle for logic-processed CPS-PWM scheme based balancing strategy.



Fig. 8. The three-tier control architecture for logic-processed CPS-PWM based balancing strategy.

transmission, which mainly deals with active power and has a modulation index higher than 0.75.

IV. IMPLEMENTATION OF THE LOGIC-PROCESSED CPS-PWM Based Balancing Strategy

In the logic-processed CPS-PWM scheme, the manipulation of driving signals should be achieved without affecting the synchronization of switching actions among SMs. Otherwise, distorted voltage levels and defected arm currents will be induced [16]. As demonstrated in Fig. 8, a three-tier control system architecture is proposed. The control system is divided into three parts: the main controller, phase controllers and submodule controllers. The main controller is one DSP controller, which is responsible for the high-level controls, such as active and reactive power control.

The phase controller utilizes FPGA as the control unit, which carries out the logic-processed CPS-PWM scheme based capacitor voltage balancing strategy. Since the generation and manipulation of driving signals are centralized in the middle-tier controller, the synchronization of switching actions is naturally guaranteed. Moreover, the logic process of driving signals is easy and cost-effective in FPGAs. The SM controllers only receive control signals from the phase controllers and report the capacitor voltage to the phase controllers.

TABLE I PARAMETERS OF SIMULATION AND PROTOTYPE

Parameters	Simulation	Prototype
DC Bus Voltage (V_{dc})	19 kV	800 V
Apparent Power (S)	2 MVA	6 kVA
Line to Line Voltage (V ₁₋₁ , rms)	10 kV	400 V
Output Frequency (f)	50 Hz	50 Hz
Carrier Frequency (f_c)	$450~\mathrm{Hz}/150~\mathrm{Hz}$	450 Hz
Number of SMs in each arm (N)	20	8
Arm Inductance (L)	40 mH	40 mH
SM Capacitance (C)	3 mF	3 mF
Rated Capacitor Voltage (V_c)	950 V	100 V

V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the theoretical analysis, a 21-level threephase grid-connected inverter is built in MATLAB Simulink and a 9-level three-phase grid connected prototype is established. The parameters of simulation and prototype are shown in Table I. And the carrier frequency (switching frequency) is set as 450 Hz for both simulation and experiment.

A. Simulation Results

Dual-loop control is adopted in the simulation, where the outer loop controls the active and reactive power and the inner loop controls the active and reactive current. The carrier phase angle difference for the logic processed driving signals is selected according to [14], so new driving signals with proper charging ability can be synthesized.

Simulation results with different power factor angles are presented in Fig. 9(a)–(c). The output voltage, output current, enable flag and execution flag of balancing strategy, and the lower arm capacitor voltages of phase A are presented successively. In order to verify the effectiveness of the balancing strategy, the capacitor voltages should be diverse at the initial state. Therefore, the balancing strategy is disabled at first, and the logic processed driving signals are intentionally assigned to specific SMs to charge and discharge the capacitors. This process is not illustrated in Fig. 9. After a preset timespan, the SMs are in unbalance state and they are re-assigned with their original driving signals. At the meantime, the balancing strategy is still disabled. As observed in Fig. 9(a)-(c), with the original high frequency driving signals, the capacitor voltages keep unchanged. This is because there is little difference in the charging ability of original driving signals, which verifies the theoretical analysis.

The balancing strategy is enabled at 0.3 s. And it can be seen from Fig. 9(a)–(c) that the capacitor voltages convergence speeds are different with different power factor angles. Fig. 9(d) is the simulation result of the traditional CPS-PWM scheme based balancing strategy with 150 Hz carrier frequency, and its power factor angle is $\pi/3$.



Fig. 9. Simulation results. (a) power factor angle $\theta = 0$ with 450 Hz logic processed CPS-PWM, (b) $\theta = \pi/6$ with 450 Hz logic processed CPS-PWM, (c) $\theta = \pi/3$ with 450 Hz logic processed CPS-PWM, (d) $\theta = \pi/3$ with 150 Hz traditional CPS-PWM.

TABLE II Comparison of Simulation Results

Balancing Strategy	Logic Pro	Traditional CPS-PWM		
Carrier Frequency (f_c)		450 Hz		150 Hz
Power Factor Angle (θ)	0	$\pi/6$	π/3	$\pi/3$
Voltage Variation (ΔV)	220.3 V	219.8 V	212.8 V	223.5 V
Convergence Time (Δt)	0.1 s	0.12 s	0.2 s	0.14 s
Voltage Ripple (ΔV_{ripple})	34.2 V	36.6 V	43.1 V	42.2 V

Key performance characters of the simulation results are concluded in Table II. When the power factor angle θ changes from 0 to $\pi/6$, i.e., active power is still the major power component, the convergence speed difference is small. However, when reactive power becomes the major power component (power factor angle θ changes to $\pi/3$), the convergence time is two times longer than that with $\theta = 0$. It indicates that the convergence speed drops quickly with the increase of reactive power. Compared with the traditional CPS-PWM scheme based balancing strategy (seven fundamental periods), the convergence speed of logic processed CPS-PWM scheme based balancing strategy is much slower when power factor angle reaches $\pi/3$ (ten fundamental periods). This result verifies the proposed application ranges of power factor angle in Section III.

B. Experimental Results

Similarly, the logic-processed voltage balancing strategy is disabled at first, and the driving signal synthesized by logic *OR* process of the 1st and the 5th carriers is assigned to SM_1 , and the driving signal synthesized by logic *AND* process is assigned to SM_8 . Besides, the rest SMs' driving signals remain unchanged. Consequently, the capacitor voltages of SM_1 and SM_8 diverge from their rated value.

Three cases are studied in this section, i.e., the power factor angle equals to 0, $\pi/6$ and $\pi/3$. The experimental results are presented in Fig. 10(a), (b), (c). The output voltage, output current, capacitor voltages of SM1, SM5 and SM8 in the lower arm of phase A, execution flag and enable flag of the balancing strategy are depicted in sequence in each figure. It should be noticed that, in order to keep a high convergence speed and avoid the possible voltage oscillations, the selection of carrier phase angle difference for logic processing is divided into three regions according to the voltage divergence degree as introduced in [14]. Therefore, the convergence time is indicated by the execution flag of the outermost region *flag* 1 and the innermost region *flag* 3. The key experimental results are concluded in Table III. It is consistent with the analysis and simulation that the convergence time increases with the increase of reactive power component. And when the power factor angle θ reaches $\pi/3$, the convergence speed drops a lot compared to the condition when $\theta = 0$ (from five fundamental periods to fifteen fundamental periods).



Fig. 10. Experimental results for 450 Hz logic-processed CPS-PWM based balancing strategy, (a) power factor angle $\theta = 0$, (b) $\theta = \pi/6$, (c) $\theta = \pi/3$.

TABLE III Comparison of Experimental Results

Balancing Strategy	Logic Processed Scheme With FFSA			
Carrier Frequency (f_c)		450 Hz		
Power Factor Angle (θ)	0	π/6	$\pi/3$	
Voltage Variation (ΔV)	33 V	35 V	34 V	
Convergence Time (Δt)	0.1 s	0.14 s	0.3 s	
Voltage Ripple (ΔV_{ripple})	8.7 V	9.4 V	9.5 V	

VI. CONCLUSION

The convergence speed and application ranges of the logicprocessed CPS-PWM scheme based balancing strategy is analyzed in this paper. It is revealed through mathematical analysis that the convergence speed is mainly determined by the power factor of MMC. And by comparing with the normal CPS-PWM scheme based balancing strategy, the application ranges of power factor angle for the proposed balancing strategy is derived, i.e., $[-\pi/3, \pi/3] \parallel [-\pi, -2\pi/3] \parallel [2\pi/3, \pi]$. It indicates that this strategy is especially suitable for MMC-HVDC transmissions, which mainly deals with active power. Besides, with the proposed three-tier control system, CPS-PWM and logic process are centralized in the phase-controllers (FPGA). Therefore, the synchronization of switching actions is guaranteed naturally. The theoretical analysis is validated by both simulation and experimental results.

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