Online Junction Temperature Estimation Method for SiC Modules With Built-in NTC Sensor

Ping Liu, Changle Chen, Xing Zhang, and Shoudao Huang

***Abstract*—Silicon carbide (SiC) devices characterized by high efficiency, high power density and wide bandgap, have great potential in many advanced applications, such as electric automotive, aviation and military. Thermal management, condition monitoring and life estimation of SiC modules are essential to achieve high reliability. These control techniques require realtime monitoring or estimation of the module's junction temperature. This paper proposed a thermal model based on an integrated negative thermal coefficient (NTC) thermistor in SiC modules. The Finite Element Methods simulation results showed that the parameters of the thermal model are invariant under different heat dissipation conditions and ambient temperatures. The combination of the proposed thermal model with the reading of NTC sensor realized the online estimation of the junction temperature. The accuracy of the thermal model and the independence of thermal impedance were verified by simulation and experimental results.**

***Index Terms*—Boundary conditions, junction temperature, silicon carbide (SiC), thermal model.**

I. Introduction

SILICON carbide (SiC) power semiconductor devices, with great potential in future power electronic conversion systems, have been widely used in high-reliability applications, such as automotive, aerospace and military. The SiC modules have the features of higher power densities, more compact package and higher efficiency. These features make it crucial to find a precise method of measuring or estimating junction temperature of SiC devices during the operation. In addition, the precise real-time junction temperature plays an important role in the thermal management control, condition monitoring and lifetime estimation. It will facilitate the reliability and stability analysis of the SiC devices.

In the literature, many studies have been conducted on chip/power module thermal analysis. There are several advanced simulation tools used, such as Finite Element Method (FEM), Finite Difference Method (FDM) and Finite Volume Method (FVM) [1]–[3]. All of them can provide precise and detailed thermal information of the power devices during steady-state and transient operation. However, massive computation time are needed due to the complex three-dimensional structure of the power modules and multi-physics environments. Thus, they are not suitable for the long-time load profile analysis of the power modules and online temperature estimation.

Among other solutions, RC-lumped thermal network (RC-TN) and thermo-sensitive electrical parameters (TSEPs) are widely used with fast response [4]–[7]. The RC-TN-based method relies on a one-dimensional RC network with multiple time constants. Fixed thermal impedance values are used, which will change under some special conditions, such as nonlinear characterization, fatigue of thermal interface materials and abnormal cooling conditions. This high dependence on the multi-order thermal model reduces the accuracy of the RC-TN-based method. In addition, the TSEPs-based method has the following limitations: 1) complexity caused by additional circuit; 2) issues on measurement accuracy and robustness to noise; 3) impact of invasive methods on the normal operation. Hence, it is still a challenging task to rapidly and accurately estimate the temperature of the power semiconductor under real-time applications.

In fact, many existing power modules are equipped with a temperature sensor, which usually is a negative thermal coefficient thermistor (NTC). For the module under test in this work, the NTC was located on the same ceramic substrate as the SiC MOSFET and diode chips (see Fig. 1). It could be used to predigest the thermal model of the power module, making it easier to estimate the chip junction temperature under less impact of the thermal grease fatigue and cooling condition changes. Usually, the integrated NTC is only aimed at protecting and monitoring when the junction temperature reaches a threshold value, as well as ensuring turn-off procedures. Few thermal models estimating the junction temperature through the integrated NTC have been proposed in [8]–[10]. However, the fly in the ointment is the response or accuracy when tracking the dynamic junction temperature variation in real-time applications. In [9], an experimental method was put forward to extract the thermal network parameters, ignoring the thermal impedance of the diode. Also, the influence of the heat dissipation effect and ambient temperature on the thermal model was not considered.

In this paper, a thermal model was obtained by FEM simulation, aiming to estimate the junction temperature for the power devices in SiC power module [11], [12]. Based on this method, estimation of the junction temperature can be realized by the NTC sensor reading and the thermal network between the chips and NTC. Due to the use of NTC, analyzing the thermal

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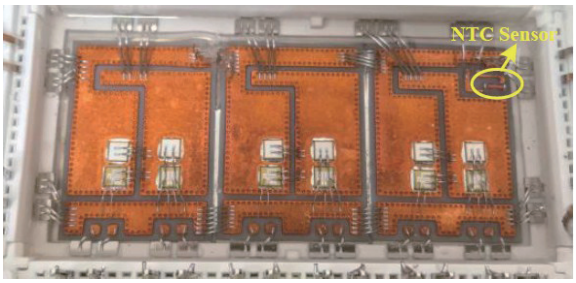
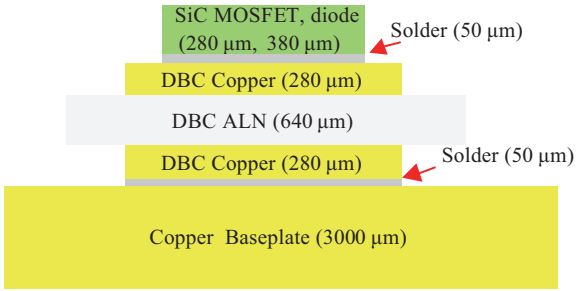
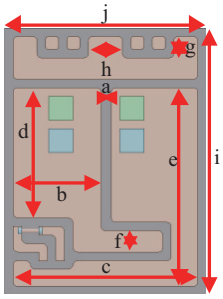


Fig. 1. Module under test (CREE 1200 V/20 A, SiC MOSFET module: CCS020M12CM2).



(a)



Dimension	Size(mm)
a	1.2
b	10.3
c	21.6
d	19.24
e	23.24
f	2.5
g	2.5
h	4.0
i	31.24
j	23.6

(b)

Fig. 2. Thickness and length dimension of each layer of the SiC MOSFET module.

resistance of the low physical layers becomes unnecessary. In addition, experimental results showed the thermal resistance remained unchanged under different heatsink or ambient temperature conditions. It proved the proposed model to be much applicable to the circuit simulator for long-time load profile analysis or the condition monitoring of the power modules.

II. Modeling of Thermal Impedance Network

The test SiC module CREE CCS020M12CM2 in the paper is shown in Fig. 1. In detail, the selected SiC MOSFET module consists of 3 half-bridge parallel converters, including 6 MOSFET and 6 diode chips, which are all installed on the Direct Copper Bonded (DCB). The three-dimensional finite element simulation model and structural parameters of this module are presented in Fig. 2. The finite element simulation model of the SiC MOSFET module is provided in Fig. 3.

When the SiC MOSFET module is operated under low-frequency and high-power or standstill conditions, a maximum DC current will flow through a single diode continuously. This may result in a rapid growth in the junction temperature of the

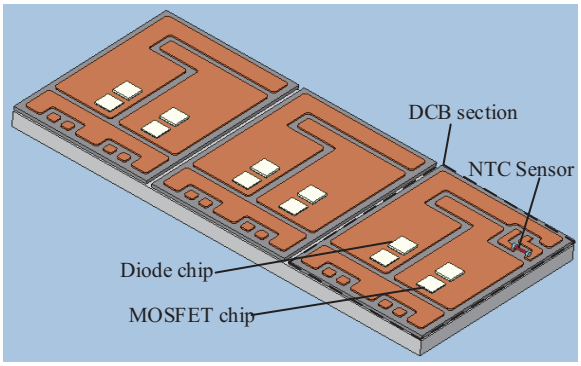


Fig. 3. Schematic of the 1200 V/20 A SiC MOSFET module modeled FEM analysis.

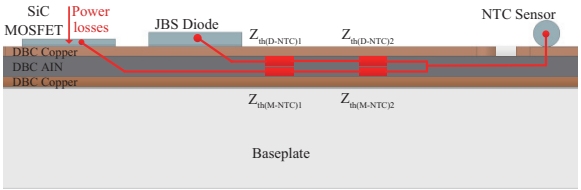


Fig. 4. Thermal model of the SiC MOSFET module with integrated NTC sensor.

diode. Therefore, establishing thermal models for both MOSFET and diode becomes essential. Fig. 4 shows the thermal model of the SiC MOSFET module established by NTC, where $Z_{th(M\text{-}NTC)}$ and $Z_{th(D\text{-}NTC)}$ represent the thermal resistance from the MOSFET and the diode respectively to NTC. The relationship between the transient thermal impedance $Z_{th(j\text{-}N)}(t)$ and the step power loss at the chip is defined as:

$$Z_{th(j-N)}(t) = \frac{T_j(t) - T_{NTC}(t)}{P(t)} \tag{1}$$

After obtaining the power loss P(t) of the SiC MOSFET module and the NTC temperature T_{NTC}, junction temperatures with any power dissipations can be expressed by (2), which is the form in s-domain. The power losses used in the thermal model are calculated based on the SiC module datasheet. The power loss for the power semiconductor devices is composed of two parts: conduction loss and switching loss, which has been well investigated [13].

$$\begin{aligned} T_{MOSFET}(s) &= (Z_{th(M-NTC)1}(s) + Z_{th(M-NTC)2}(s))*P_{MOSFET}(s) + T_{NTC}(s) \\ T_{Diode}(s) &= (Z_{th(D-NTC)1}(s) + Z_{th(D-NTC)2}(s))*P_{Diode}(s) + T_{NTC}(s) \end{aligned} \tag{2}$$

To get the junction temperatures, thermal impedance between the chip and NTC is in need. A second-order Foster thermal network is shown in Fig. 5, the dynamic response of which can well reflect the heat flow from the MOSFET or diode to the NTC sensor by the curve fitting method. Therefore, the thermal impedance elements in (2) are represented by this circuit impedance. The transfer function of the thermal network is obtained as:

$$Z_{th(j-N)}(s) = \frac{R_{th(j-N)1}}{1 + s\tau_{th(j-N)1}} + \frac{R_{th(j-N)2}}{1 + s\tau_{th(j-N)2}} \tag{3}$$

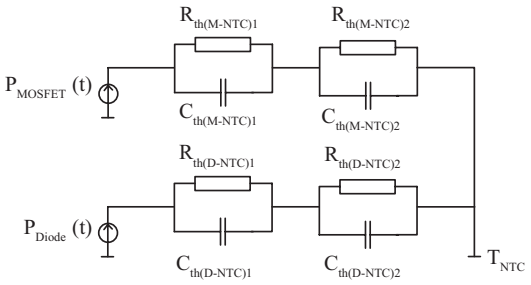


Fig. 5. Proposed Foster thermal model.

TABLE I
BOUNDARY CONDITIONS IN FEM SIMULATION

Power dissipation	40 W per chip
Ambient temperature	25~100 °C
Coefficient of convection with air	10~10000 W/(m^2•K)
Elements	18167

where the time constant $\tau_{th(j-N)}$ equals to $R_{th(j-N)} * C_{th(j-N)}$.

Generally, the fourth-order thermal model of the power module in the datasheet is provided by the power module manufacturer. In practical applications, the thermal model is converted into a difference equation in advance and then applied to achieve programming. The calculation of the thermal model in the datasheet requires 80 instruction cycles. The calculation of the proposed thermal model requires 40 instruction cycles. In terms of programming implementation, the proposed thermal model exhibits a higher response speed.

According to the zero-hold transform method, (3) is transformed into the z-domain transfer function (4), in which T_s is the sampling period. Thus, the z-domain form of (2) is obtained. Then, with the obtained parameters $R_{th(j-N)}$ and $\tau_{th(j-N)}$ in (3), junction temperature of the chip can be estimated by the processor.

$$Z_{th(j-N)}(z) = \frac{b_{th(j-N)1} z^{-1}}{1+z^{-1} a_{th(j-N)1}} R_{th(j-N)1} + \frac{b_{th(j-N)2} z^{-1}}{1+z^{-1} a_{th(j-N)1}} R_{th(j-N)2}$$
$$b_{th(j-N)} = \frac{T_s}{\tau_{th(j-N)}},\ a_{th(j-N)} = b_{th(j-N)} - 1 \quad (4)$$

The step response of the thermal network is expressed by an exponential term as given in (5).

$$Z_{th(j-N)}(t) = \sum_{m=1}^{2} R_{th(j-N)m}\left(1 - \exp\left(-\frac{t}{\tau_{th(j-N)m}}\right)\right) \quad (5)$$

To obtain the proposed thermal network parameters, parameters $R_{th(j-N)}$ and $\tau_{th(j-N)}$ in (5) under different boundary conditions should be derived by the curve fitting of the step response. The ANSYS Workbench was selected to conduct the transient thermal analysis and to obtain the step responses. The boundary conditions of the FEM simulation are listed in Table I.

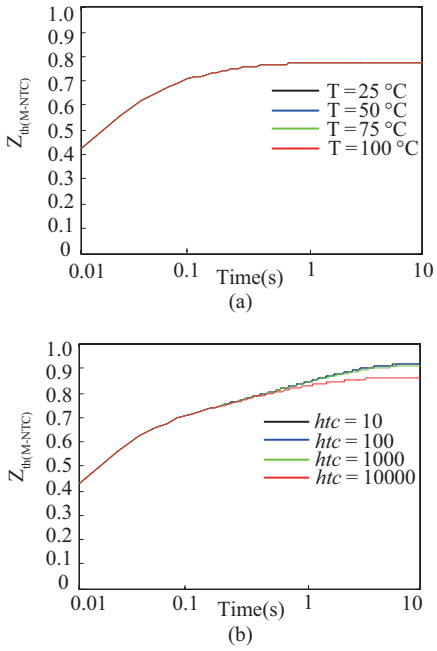


Fig. 6. (a) Thermal resistance $Z_{th(M-NTC)}$ under different ambient temperatures when *htc* is 10000 W/m^2•K. (b) Thermal resistance $Z_{th(M-NTC)}$ under different values of *htc* when ambient temperature is 25 °C.

To explore the impact of heatsink boundary condition on SiC MOSFET modules, a coefficient *htc* was introduced to represent the capability of the cooling system [14]. It can be defined as:

$$htc = \frac{q}{\Delta T}\left[W/m^2 \cdot K\right] \quad (6)$$

where q is the amount of heat transferred between two different materials and ΔT is the temperature difference. The equation indicates that, the higher the *htc*, the better the capability of the heat conduction between different layers with the same heat.

For SiC modules with a certain cooling system (constant *htc* coefficient), the heat is mainly localized beneath the chips. It not only leads to a smaller heat spreading, but also reduces the effective heat dissipation area and increases thermal resistance. This enlarges the temperature difference between the junction and the heatsink. According to the heat transfer textbook, the coefficient *htc* in this paper ranged from 10 W/m^2•K to 10000 W/m^2•K, representing common cooling method like forced convection-air and forced convection-water used in SiC modules [15]. On the other hand, the ambient temperature was set from 25 °C to 100 °C to study the effect on thermal resistance in FEM simulation. As the results shown in Fig. 6 and Fig. 7, little change was found in the thermal resistance $Z_{th(M-NTC)}$ and $Z_{th(D-NTC)}$ under different ambient temperatures, or under different *htc*. This phenomenon may originate from the stalling location of the NTC sensor, which was away from heatsinks and on the same layer with the heat sources.

The thermal model is provided in the datasheet, which shows the necessity to establish a thermal impedance network

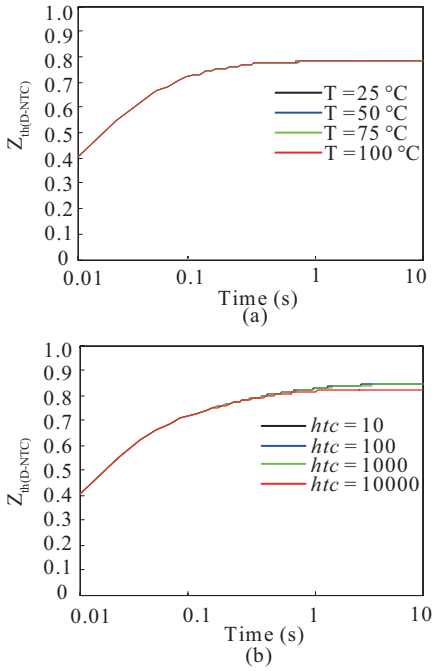


Fig. 7. (a) Thermal resistance $Z_{th(D-NTC)}$ under different ambient temperatures when *htc* is 10000 W/m^2•K. (b) Thermal resistance $Z_{th(D-NTC)}$ under different values of *htc* when ambient temperature is 25 °C.

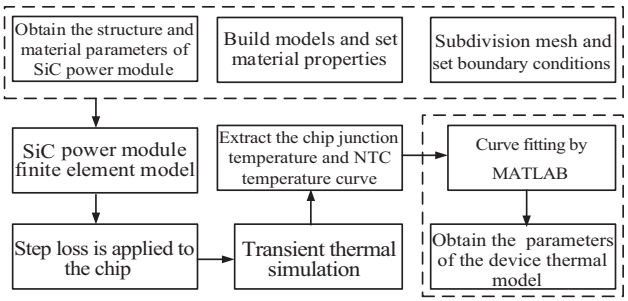


Fig. 8. Flowchart of thermal impedance extraction for SiC module.

from the chip to the heatsink. During the long-term operation of the power module, aging of the solder layer under the substrate plate and thermal grease are inevitable. In this case, the previously determined thermal resistance network model will be greatly offset, resulting in errors in junction temperature prediction. However, as described above, the heat dissipation conditions and ambient temperature of the heatsink have little impact on the heat model proposed in this paper. Therefore, from the perspective of long-term operation, the proposed model is more adaptable and accurate than that described in the datasheet.

Based on the above discussed cases and results, transient thermal impedance $Z_{th(j-N)}(t)$ was obtained from Fig. 8. The three-dimensional finite element model of the SiC module was established by using ANSYS finite element software. Then, a step power loss was loaded on the chip, and the temperature curves of the chips and the NTC sensor were detected. The junction temperature curves of the chips and NTC with ambient temperature T = 25 ˚C and *htc* = 10 W/m^2•K are shown in

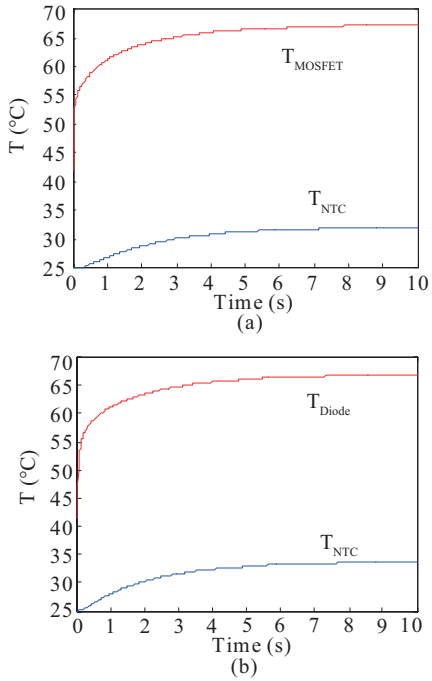


Fig. 9. (a) Thermal responses of the MOSFET chip and NTC. (b) Thermal responses of the diode and NTC.

TABLE II
THERMAL IMPEDANCE OF MOSFET-TO-NTC AND DIODE-TO-NTC

	MOSFET ($Z_{th(M-NTC)}$)		Diode ($Z_{th(D-NTC)}$)	
R_{th} [K/W]	0.7085	0.1682	0.6659	0.1642
C_{th} [J/K]	0.0141	2.9727	0.01502	1.2
τ_i [s]	0.01	0.5	0.01	0.2

Fig. 9. Finally, the parameters of the thermal impedance in (5) were acquired by means of the curve fitting method. Thermal impedance parameters under different coefficient *htc* and ambient temperatures were described as constants, listed in Table II. With all the impedance parameters obtained, junction temperatures were then estimated by the z-domain form of (2) in the microcontrollers.

III. SIMULATION AND EXPERIMENTAL VERIFICATION

To verify the accuracy of the presented thermal model, simulations were performed through MATLAB/Simulink and FEM. On basis of Fig. 5 and (2), a thermal model was built, in which MATLAB/Simulink was used to estimate the junction temperature of the chips in the SiC power module. The estimation results were indicated by the comparison between the FEM simulation and the experimental results.

Fig. 10 shows the simulated junction temperature under different load conditions. Parameters in MATLAB/Simulink simulation are listed in Table III. The experimental results using the proposed model were found to be in line with those of the FEM simulation.

The effectiveness of the presented method was verified by an experiment, in which an opened SiC module was mounted

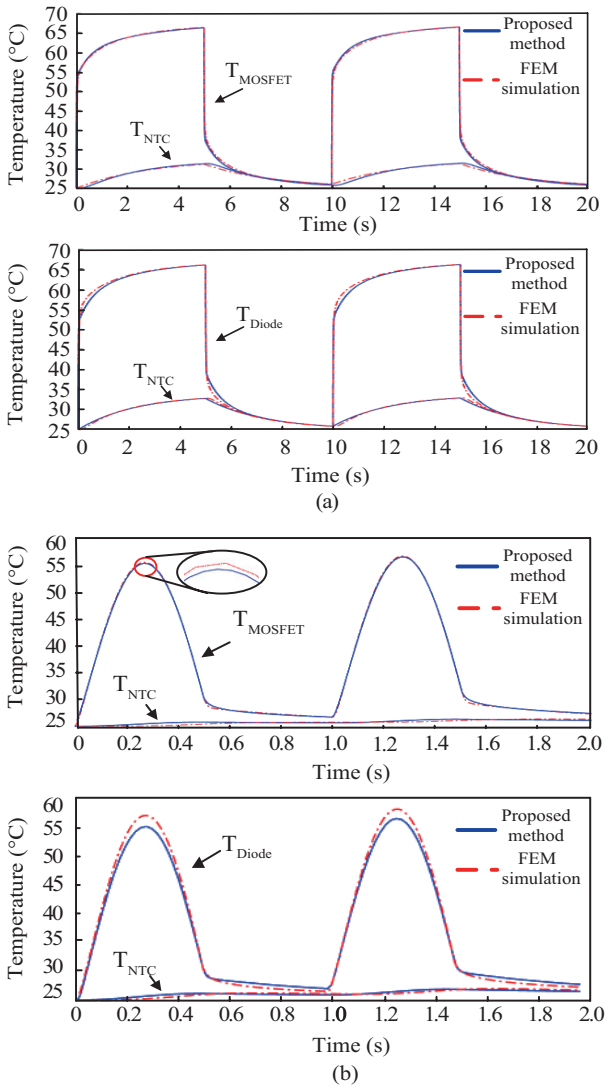


Fig. 10. Estimated junction temperatures of SiC MOSFET and diode under different load conditions: (a) Square wave load. (b) AC load.

TABLE III
SIMULATION PARAMETERS IN MATLAB/SIMULINK

	Square waveform load	AC load
Peak power	40 W	
Period	10 s	1 s
Duration	5 s	0.5 s
Ambient temperature	25 °C	

on a heatsink. An isolated optical fiber temperature sensor OTG-F-10 from Opsens was selected to directly measure the junction temperature of the power devices, as shown in Fig. 11(a). The test conditions for the inspected SiC MOSFET module were a square wave load with a peak current of 5 A and a heatsink temperature of 25 °C. The test period was set as 20 seconds with a duty cycle of 50%.

Fig. 11(b) shows the estimated temperature and measured

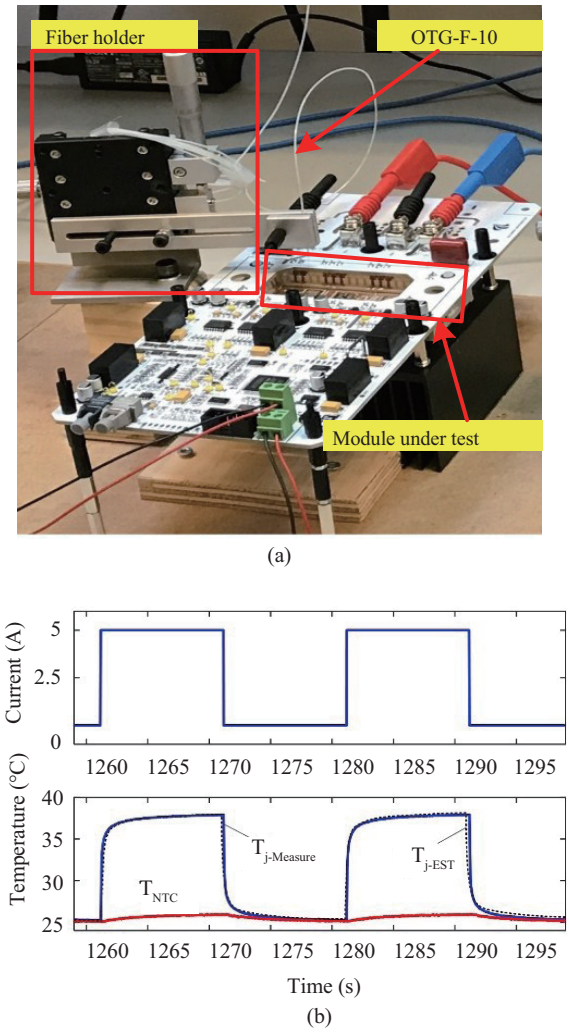


Fig. 11. Experimental set-up and results: (a) Photo of the set-up which shows SiC module with optical fibers for temperature measurement. (b) Experimental results during power cycling test: (upper) load current, (lower) measured $T_{j\text{-}Measure}$ of SiC MOSFET, and estimated $T_{j\text{-}EST}$ using proposed thermal model and T_{NTC}.

temperature during the power cycling test. It was found that the estimation junction temperature ($T_{j\text{-}EST}$) obtained by the proposed thermal model was consistent with the measured result ($T_{j\text{-}Measure}$).

IV. CONCLUSIONS

In this paper, a new junction temperature estimation method based on integrated NTC sensor for SiC modules was presented. A second-order Foster thermal network was established to represent the heat transfer between the chips and the integrated NTC. The comparison between the simulation and the experimental results demonstrates the following advantages of the proposed method: 1) compared with the conventional RC-TN-based solution, it has faster response and improved accuracy in junction temperature estimation with second-order RC lumped thermal network; 2) it is non-invasive with

simple implementation and gets little impact from the ambient temperature or heatsink condition changes; 3) it is able to realize quick, accurate and robust measurement of the power modules' online temperature; 4) it is much appropriate to be used in circuit simulators for long-time load profile analysis or the condition monitoring of power modules.

References

[1] D. Cottet, U. Drofenik, and J. Meyer, "A systematic design approach to thermal-electrical power electronics integration," in *2008 2nd Electron. System-Integration Technol. Conf.*, Greenwich, pp. 219–224.

[2] T. Kojima, Y. Yamada, Y. Nishibe, and K. Torii, "Novel RC compact thermal model of HV inverter module for electro-thermal coupling simulation," in *2007 Power Convers. Conf. - Nagoya*, Nagoya, pp. 1025–1029.

[3] S. Carubelli and Z. Khatir, "Experimental validation of a thermal modelling method dictated to multichip power modules in operating conditions," *Microelectron. J.*, vol. 34, pp. 1143–1151, Jun. 2003.

[4] *Thermal design and temperature ratings of IGBT modules*, App. Note 5SYA 2093–00, ABB, pp. 5–6.

[5] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters-A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[6] H. Kuhn and A. Mertens, "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters," in *2009 13th Eur. Conf. Power Electron. Appl.*, Barcelona, pp. 1–10.

[7] J. A. Butron Ccoa, B. Strauss, G. Mitic, and A. Lindemann, "Investigation of temperature sensitive electrical parameters for power semiconductors (IGBT) in real-time applications," in *PCIM Eur. 2014 Int. Exhibition Conf. Power Electron., Intell. Motion, Renewable Energy, Energy Manag.*, Nuremberg, Germany, pp. 1–9.

[8] M. Schulz and M. Xin, "Correlating NTC-reading and chip-temperature in power electronic modules," in *Proc. PCIM Eur. 2015 Int. Exhibition Conf. Power Electron., Intelli. Motion, Renewable Energy, Energy Manag.*, Nuremberg, Germany, pp. 1–5.

[9] Y. Zhou *et al.*, "Dynamic junction temperature estimation via built-in negative thermal coefficient (NTC) thermistor in high power IGBT modules," *in 2017 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Tampa, FL, pp. 772–775.

[10] G. Lo Calzo, A. Lidozzi, L. Solero, F. Crescimbini, and V. Cardi, "Thermal regulation as control reference in electric drives," in *2012 15th Int. Power Electron. Motion Control Conf. (EPE/PEMC)*, Novi Sad, pp. DS2c.18–1–DS2c.18–7.

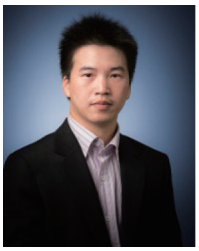
[11] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A 3-D-lumped thermal network model for long-term load profiles analysis in high-power IGBT modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1050–1063, Sept. 2016.

[12] A. J. Morgan, Y. Xu, D. C. Hopkins, I. Husain, and W. Yu, "Decomposition and electro-physical model creation of the CREE 1200V, 50A 3-Ph SiC module," in *2016 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, pp. 2141–2146.

[13] K. Ma, A. S. Bahman, S. Beczkowski, and F. Blaabjerg, "Complete loss and thermal model of power semiconductors including device rating information," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2556–2569, May 2015.

[14] A. S. Bahman, Ke. Ma, and F. Blaabjerg, "General 3D lumped thermal model with various boundary conditions for high power IGBT modules," in *2016 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, pp. 261–268.

[15] J. H. Lienhard IV and J. H. Lienhard V, *A Heat Transfer Textbook*, 4th ed. Englewood Cliffs, NJ, USA: Prentice-Hall Inc., 2013.



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