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Application Range Analysis and Implementation of the Logic-Processed CPS-PWM Scheme Based MMC Capacitor Voltage Balancing Strategy

Kun Wang, Leyuan Zhou, Yan Deng, Yi Lu, Chaoliang Wang, and Feng Xu

***Abstract*—Fundamental frequency sorting algorithm (FFSA) is outstanding for the MMC capacitor voltage balance due to the reduced computational burden and elimination of arm current detection. However, with the traditional carrier-phase-shifted pulse width modulation (CPS-PWM) scheme, FFSA will be ineffective when the carrier frequency is higher than 250 Hz, where the line frequency is 50 Hz. Thus, previous works proposed a logic-processed CPS-PWM scheme to overcome this disadvantage. This paper furtherly introduces the application ranges and implementation of this logic-processed CPS-PWM scheme based capacitor voltage balancing method in detail. With a detailed mathematical analysis, the factors that influence the balancing strategy's convergence speed are obtained, i.e., modulation index and power factor angle. It is found that in the applications where the modulation index is usually higher than 0.75, the influence of the modulation index is negligible. However, when the power factor angle is closed to $\pm\pi/2$, the convergence speed is almost zero. Therefore, by comparing with the traditional CPS-PWM scheme based FFSA balancing method, the application ranges of power factor angle are revealed to guarantee a high convergence speed. Meanwhile, the balancing strategy's application scope is specified. Moreover, a three-tier control architecture is demonstrated, where the logic process of driving signals and capacitor voltage sorting process are both executed in the middle-tier FPGA controller. This centralized scheme guarantees the synchronization of switching actions. And the logic process is easy and cost-effective in FPGA. Simulation and experimental results are presented to validate the theoretical analysis.**

***Index Terms*—Balancing strategy, convergence speed, FFSA, logic-processed CPS-PWM, modular multilevel converter.**

I. Introduction

MODULAR multilevel converter (MMC) has attracted great attention due to its modularity, high efficiency and scalability [1]–[3]. With these advantages, MMC is promising in medium- and high-voltage applications. Researches on modulation schemes, voltage balancing strategies and circulating current suppression strategies have been widely carried out [4]–[7]. Capacitor voltage balancing of sub-modules (SMs) is vital for the stable operation and performance of MMC.

Different kinds of voltage balancing methods have been presented in the literature. Among them, the open-loop balancing method requires no measurement of the capacitor voltages, which simplifies the design of the control system and reduces the cost [8]. However, its dynamic performance is poor. Sorting and selecting method is one of the most commonly used methods, which sorts the capacitor voltages at first and then inserts proper SMs according to the sorting result and the arm current direction [9]. Although this method is easy to implement, the high frequency sorting process leads to heavy computational burden and excessive switching actions. A reduced switching-frequency voltage balancing strategy was proposed in [10] to reduce the switching actions of SMs. But the sorting frequency of this method is still high. Fundamental frequency sorting algorithm (FFSA) based balancing strategy is proposed in [11], which avoids the excessive switching actions and effectively reduces the sorting frequency to fundamental frequency. So, a large amount of computing resources is saved. Further studies on FFSA have been carried out in [12]–[14] under different modulation schemes, such as carrier-phase-shifted pulse width modulation (CPS-PWM), nearest level (NL) modulation and phase disposition PWM (PD-PWM). And it is found in [14] that, with CPS-PWM scheme, FFSA based balancing strategy will no longer feasible when the carrier frequency is higher than 250 Hz, where the line frequency is 50 Hz. This is caused by the little difference in the charging ability among different driving signals. Therefore, an improved balancing strategy is proposed in [14]–[15] based on the logic-processed CPS-PWM scheme. In the improved balancing strategy, driving signals with proper phase angle difference are processed by logic *AND/OR* process to synthesize new driving signals with obviously charging ability difference. Subsequently, the FFSA can balance the capacitor voltage under high-frequency CPS-PWM. However, the convergence speed and application ranges of the proposed balancing strategy is not analyzed in detail.

In this paper, the convergence speed of logic-processed CPS-PWM scheme based MMC capacitor voltage balancing strategy is analyzed in detail. It is found that the convergence

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K. Wang, L. Zhou, and Y. Deng are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: wkun@zju.edu.cn; zlyuan@zju.edu.cn; dengyan@zju.edu.cn).

Y. Lu, C. Wang, and F. Xu are with the State Grid Zhejiang Electric Power Research Institute, Hangzhou 310014, China (e-mail: lu_yi51@zj.sgcc.com.cn; chaoliangwang@126.com; xuf_1988@163.com).

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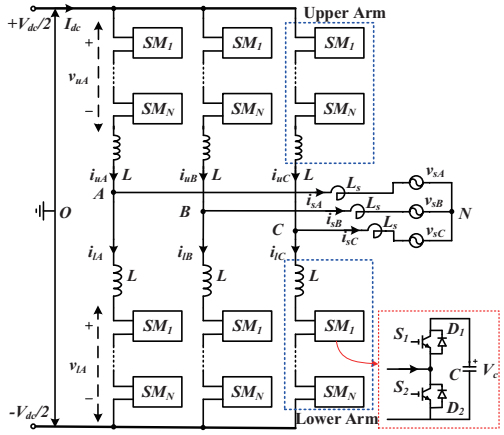

Fig. 1. Structure of a typical three-phase grid-connected MMC.

speed is influenced by the modulation index and power factor angle. While, as revealed in this paper, in the applications where the modulation index is usually higher than 0.75, the influence of modulation index is negligible. However, when the power factor angle is closed to ±π/2, the balancing strategy becomes infeasible because the convergence speed is too slow to balance the capacitor voltage. By comparing with the traditional CPS-PWM scheme based FFSA balancing method, the application ranges of power factor angle are revealed. Consequently, the proposed balancing method's application scope is specified. It is especially suitable for the high voltage direct current (HVDC) transmission, but not suitable for applications such as static synchronous compensator (STATCOM), which mainly generate or absorb reactive power. Moreover, a three-tier control architecture is also presented, where the logic-processed CPS-PWM is centralized in the middle-tier FPGA controllers for each phase. Thus, the synchronization of switching actions is guaranteed, and the logic process can be accomplished easily and cost-efficiently.

This paper is organized as follows. The principles of logic-processed CPS-PWM scheme based capacitor voltage balancing strategy are presented in Section II. In Section III, the convergence speed is analyzed in detail, and the application ranges of power factor angle are revealed subsequently. The three-tier control architecture is demonstrated in Section IV. Simulation and experimental results verify the theoretical analysis in Section V. Finally, Section VI draws the conclusion.

II. Logic-Processed CPS-PWM Scheme Based Voltage Balancing Strategy With FFSA

A. Structure of MMC

A typical structure of three-phase grid-connected MMC is illustrated in Fig. 1, where each phase leg is comprised of two arms. In each arm, N SMs and one inductor are connected in series. The SM consists of two IGBT switches and one capacitor. When S_1 is on, the SM is inserted. And it is bypassed when S_2 is on. Thus, the output voltage of SM varies between V_c and zero, where V_c is the capacitor voltage. The output voltage

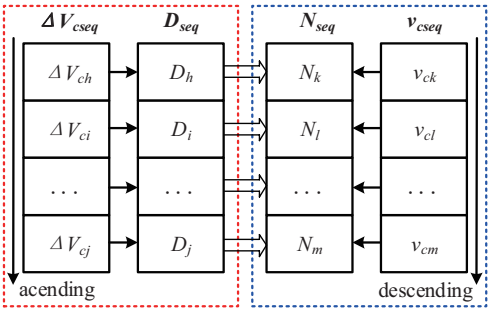

Fig. 2. Principle of fundamental frequency sorting algorithm.

can be synthesized by properly inserting a certain number of SMs in upper and lower arms.

B. Traditional CPS-PWM Scheme Based Balancing Strategy With FFSA

The basic principle of FFSA is firstly introduced in [11]. In this algorithm, the capacitor voltage variations of SMs in the previous fundamental period are calculated and sorted in ascending order at the fundamental frequency. In Fig. 2, ΔV_{ch}, ΔV_{ci}, ΔV_{cj} represent the voltage variations of SM_h, SM_i and SM_j, and ΔV_{cseq} stores the sorting result. The voltage variations sorting result reflects the charging ability of each SM's driving signal assigned to them in the previous fundamental period. Subsequently, the driving signals sequence, namely D_{seq}, is obtained in ascending order regarding to their charging ability. Meanwhile, the capacitor voltages are sorted in descending order, obtaining the voltage sequence labeled as v_{cseq}. Symbols v_{ck}, v_{cl}, and v_{cm} represent the capacitor voltage of SM_k, SM_l and SM_m, respectively. And N_{seq} stores the corresponding number of the SMs. So far, the relationship between driving signals and SMs can be rebuilt with the balancing strategy going like this: in the following fundamental period, driving signal which has the lowest charging ability will be assigned to SM with the highest capacitor voltage, e.g., D_h is assigned to SM-N_k, while driving signal which has the highest charging ability will be assigned to SM with the lowest capacitor voltage, e.g., D_j is assigned to SM-N_m. Thus, the capacitor voltage can be well balanced.

However, in this scenario, the charging ability of driving signals is related to the CPS-PWM carrier frequency. As illustrated in Fig. 3, N carriers are compared with the modulation signal v_{aref} to generate driving signals for the lower arm of phase A. Taking S_x as an example, which is generated by the x^{th} carrier, the Fourier expression of S_x can be derived as:

$$S_{lxCPS} = \frac{1}{2} + \frac{m_v}{2}\cos(\omega t + \theta_v) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} A_{mn}\cos\left[m(\omega_c t + \theta_{cx}) + n(\omega t + \theta_v)\right] \quad (1)$$

where m_v is the modulation index, ω is the angular frequency of modulation signal, ω_c is the angular frequency of carrier, θ_v is the phase angle of the modulation signal, θ_{cx} is the initial phase angle of x^{th} carrier and A_{mn} is the amplitude of harmonic

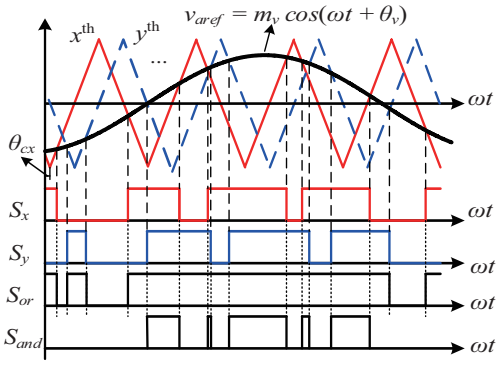

Fig. 3. Illustration of CPS-PWM and logic processing of driving signals.

component, in which m is the carrier harmonic index and n is the carrier sideband harmonic index (m = 1, 2, 3,… and n = 0, ±1, ±2, …). So the voltage variation caused by the x^{th} carrier during one fundamental period can be calculated as:

$$\Delta V_{clxCPS} = \frac{1}{C}\int_0^T S_{lxCPS} \times i_{lA} dt = \Delta V_1 + \Delta V_2 + \Delta V_3 \quad (2)$$

where i_{lA} is the lower arm current of phase A and ΔV_1, ΔV_2 and ΔV_3 represent the voltage variations caused by carrier harmonics and their sidebands that overlap the DC component, the fundamental component and the secondary harmonic, respectively. As presented in [14], if the line frequency is 50 Hz, when the carrier frequency is higher than 250 Hz, the charging abilities of each driving signal are all near to zero, which leads to the failure of balancing strategy based on traditional CPS-PWM scheme with FFSA.

C. Logic-Processed CPS-PWM Scheme Based Balancing Strategy With FFSA

In order to synthesize driving signals with obviously different charging ability when the carrier frequency is higher than 250 Hz, the logic-processed CPS-PWM scheme is proposed. As depicted in Fig. 3, carrier x and carrier y are selected in pairs as an example. Driving signal S_{or} is the logic *OR* process result of S_x and S_y, and S_{and} is the result of logic *AND* process of S_x and S_y. As proved in the next section, the logic-processed driving signals, S_{or} and S_{and} possess obviously different charging ability with each other. So the logic-processed CPS-PWM scheme based balancing strategy with FFSA can be executed as follows.

Firstly, the sorting process of capacitor voltages is operated at fundamental frequency with the corresponding SM's number sequence stored in N_{seq}, as illustrated in Fig. 4. The voltage differences of each SM-pair can be obtained simultaneously, where the SMs are combined in pairs by the following rules: SM with the highest capacitor voltage is combined with the SM with lowest capacitor voltage, and the second highest SM is combined with the second lowest SM, and so on. In this paper, 2% of the rated capacitor voltage is set as the threshold to determine whether the SMs are in balance state or not. If the voltage difference overreaches this threshold, it means that the corresponding SM-pair is in unbalance state. As shown in

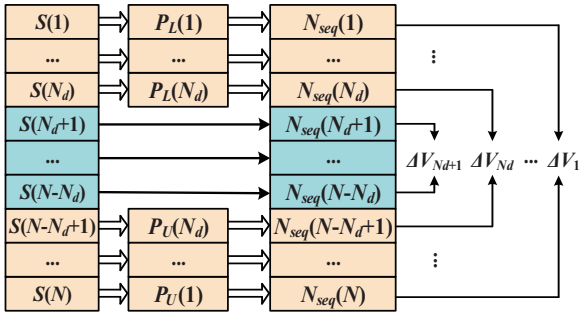

Fig. 4. Logic process and assignment of the driving signals.

Fig. 4, assume there are N_d pairs of SMs in unbalance state, i.e., voltage differences of the highest N_d SMs and the lowest N_d SMs ($\Delta V_1 \sim \Delta V_{Nd}$) exceed the threshold. Accordingly, N_d pairs of driving signals with proper phase angle difference are selected in $S(i)$ and S(N−i+1), where i = 1, 2, …, N_d. And the rest driving signals are stored in $S(N_d+1)$ to $S(N-N_d+1)$, which are directly assigned to the SMs in balance state. $P_L(i)$ and $P_U(i)$ represent the logic process of driving signal pairs as defined in (3) and (4), where *min*{} means selection of the driving signal with lower charging ability, and *max*{} means selection of the driving signal with higher charging ability. And then, $P_L(i)$ is assigned to SM-$N_{seq}(i)$, while $P_U(i)$ is assigned to SM-N_{seq}(N−i + 1). Consequently, the capacitor voltages can converge back to the balance state.

$$P_L(i) = \min\left\{\frac{S(i)\|\, S(N-i+1)}{S_{or}}, \frac{S(i)\,\&\&\, S(N-i+1)}{S_{and}}\right\} \quad (3)$$

$$P_U(i) = \max\left\{\frac{S(i)\|\, S(N-i+1)}{S_{or}}, \frac{S(i)\,\&\&\, S(N-i+1)}{S_{and}}\right\} \quad (4)$$

III. Convergence Speed and Application Range Analysis

It is clear that the charging ability difference between driving signals is the key to balance the capacitor voltages. The voltage balancing strategy may be deactivated when the charging ability difference is not so obvious. Thus, the convergence speed is analyzed in this section and the application range is revealed.

A. Convergence Speed Analysis

Similar to the traditional CPS-PWM scheme, the Fourier expression of S_{or} and S_{and} can be obtained and the voltage variations caused by them in one fundamental period can be derived as follows:

$$\begin{aligned}\Delta V_{or} \approx & -\frac{I_{sm}}{\omega C}\frac{m_v}{2}\cos\theta\left(m_v \sin\varphi_{xy} - \varphi_{xy} - \frac{\theta_{xy}}{2} + \frac{\theta_{xy}\varphi_{xy}}{\pi}\right) \\ & -\frac{I_{sm}}{\omega C}\frac{\varepsilon_{c2\omega}}{2}\cos(2\theta_v - \theta_{c2\omega}) \\ & \times\left(m_v \sin\varphi_{xy} + \frac{\theta_{xy}-\pi}{\pi}\sin 2\varphi_{xy} + \frac{m_v}{3}\sin 3\varphi_{xy}\right)\end{aligned} \quad (5)$$

$$\begin{aligned}\Delta V_{and} \approx & \frac{I_{sm}}{\omega C}\frac{m_v}{2}\cos\theta\left(m_v\sin\varphi_{xy}-\varphi_{xy}-\frac{\theta_{xy}}{2}+\frac{\theta_{xy}\varphi_{xy}}{\pi}\right)\\ & +\frac{I_{sm}}{\omega C}\frac{\varepsilon_{c2\omega}}{2}\cos(2\theta_v-\theta_{c2\omega})\\ & \times\left(m_v\sin\varphi_{xy}+\frac{\theta_{xy}-\pi}{\pi}\sin 2\varphi_{xy}+\frac{m_v}{3}\sin 3\varphi_{xy}\right)\end{aligned} \tag{6}$$

where I_{sm} is the amplitude of output phase current, θ is the power factor angle, θ_{xy} is the phase angle difference of carrier x and y, and φ_{xy} is calculated as follows:

$$\varphi_{xy}=\begin{cases}0, & 0\leqslant\theta_{xy}\leqslant(1-m_v)\pi\\ \arccos\dfrac{1-\theta_{xy}/\pi}{m_v}, & (1-m_v)\pi<\theta_{xy}<(1+m_v)\pi\\ \pi, & (1+m_v)\pi\leqslant\theta_{xy}<2\pi\end{cases} \tag{7}$$

It should be noticed that the voltage variations caused by the carrier sideband harmonic are neglected in (6) since they are very small when the carrier frequency is high. Moreover, because the driving signals are logic processed in pairs and assigned to the SM-pairs simultaneously, the convergence speed of capacitor voltage can be evaluated by the difference of variations caused by S_{or} and S_{and} as shown in (8).

$$\Delta V=\left|\Delta V_{or}-\Delta V_{and}\right|=\begin{cases}2\Delta V_{or}, & \theta\in\left[-\dfrac{\pi}{2},\dfrac{\pi}{2}\right]\\ 2\Delta V_{and}, & \theta\in\left[-\pi,-\dfrac{\pi}{2}\right]\left\|\left[\dfrac{\pi}{2},\pi\right]\right.\end{cases} \tag{8}$$

Furtherly, since the second part of (5) and (6) is also small enough to be neglected, only the first part of the voltage variations is considered for simplification. Thus, ΔV can be simplified as follows:

$$\begin{aligned}\Delta V &= 2\left|\Delta V_{or\_1}\right|=2\left|\Delta V_{and\_1}\right|\\ &=\frac{I_{sm}\left|\cos\theta\right|}{\omega C}m_v\left(\varphi_{xy}+\frac{\theta_{xy}}{2}-m_v\sin\varphi_{xy}-\frac{\theta_{xy}\varphi_{xy}}{\pi}\right)\end{aligned} \tag{9}$$

It can be observed that the convergence speed is determined by active current component $I_{sm}|\cos\theta|$, modulation index m_v and carrier phase angle difference θ_{xy}. By the partial differential operation of θ_{xy} and φ_{xy}, the following equation can be obtained as:

$$\begin{cases}\dfrac{\partial\Delta V}{\partial\theta_{xy}}=\dfrac{I_{sm}|\cos\theta|}{\omega C}m_v\left(\dfrac{1}{2}-\dfrac{\varphi_{xy}}{\pi}\right)\\ \dfrac{\partial\Delta V}{\partial\theta_{xy}}=\dfrac{I_{sm}|\cos\theta|}{\omega C}m_v\left(1-m_v\cos\varphi_{xy}-\dfrac{\theta_{xy}}{\pi}\right)\end{cases} \tag{10}$$

Assuming (10) to be zero, it can be derived that ΔV achieves its maximum value when $\theta_{xy}=\pi$ and $\varphi_{xy}=\pi/2$. Consequently, the maximum convergence speed $\Delta V_{\max}$ can be calculated as:

$$\Delta V_{\max}=\frac{I_{sm}|\cos\theta|}{\omega C}m_v\left(\frac{\pi}{2}-m_v\right) \tag{11}$$

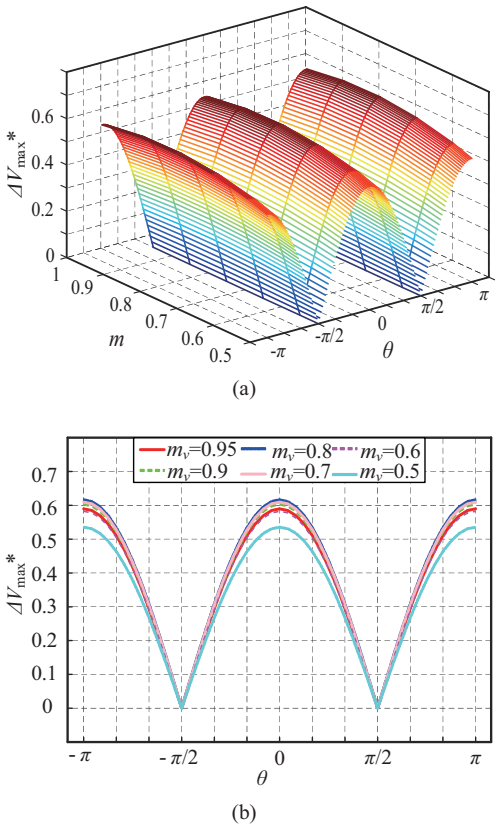

Fig. 5. Influence of power factor angle θ and modulation index m_v on the normalized convergence speed $\Delta V_{\max}^{*}$.

Normalized by $I_{sm}/\omega C$, the relationship of $\Delta V_{\max}^{*}$, m_v and θ is illustrated in Fig. 5. It can be observed that the balancing strategy has the highest convergence speed when θ equals to 0 or $\pm\pi$. While it reaches the lowest speed when θ equals to $\pm\pi/2$. And it can be seen from Fig. 5(b) that when m_v is higher than 0.75, m_v has little influence on the convergence speed. Thus, only the application range of power factor angle θ needs to be analyzed in the next subsection.

B. Application Range Analysis

It is presented in [14] that the balancing strategy's convergence speed will be degraded when there is reactive power transferred. However, the acceptable application range of power factor angle is not clearly specified. It is reasonable to take the convergence speed of traditional CPS-PWM based balancing strategy as the reference to analyze the application ranges of the proposed strategy. As demonstrated above, the traditional CPS-PWM based balancing strategy's convergence speed slows down with the increase of carrier frequency and eventually becomes infeasible when the carrier frequency is higher than 250 Hz. But it can still offer considerable speed when the carrier frequency is 150 Hz [14]. Therefore, the convergence speed of traditional CPS-PWM based balancing strategy with 150Hz carrier frequency is taken as the lowest acceptance of convergence speed for the proposed balancing strategy.

Based on the expansion of (2), the maximum and minimum

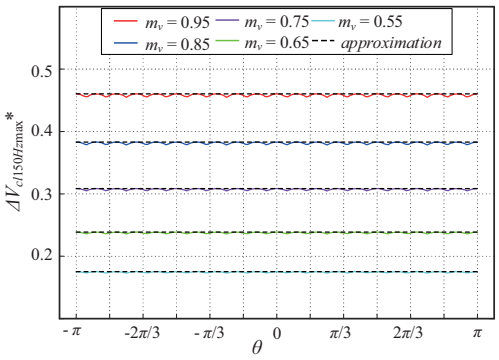

Fig. 6. Convergence speed $V_{cl150Hzmax}^*$ versus the power factor angle θ and the modulation index m_v.

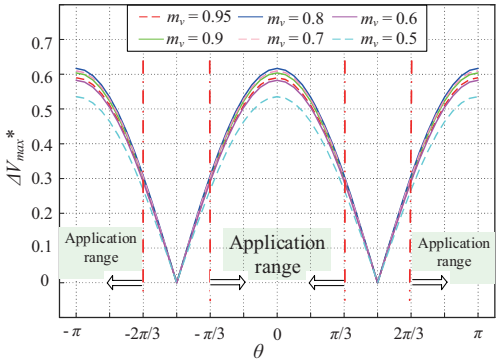

Fig. 7. Application ranges of power factor angle for logic-processed CPS-PWM scheme based balancing strategy.

capacitor voltage variations generated by the driving signals with 150 Hz carrier frequency are calculated as (12).

$$\begin{cases} \Delta V_{clx150Hzmax} \approx -\dfrac{I_{sm}}{\omega C}\dfrac{\pi}{2} \times A_{1(-2)} \cos(\theta_{cx1} - 3\theta_v + \theta) \\ \Delta V_{clx150Hzmin} \approx -\dfrac{I_{sm}}{\omega C}\dfrac{\pi}{2} \times A_{1(-2)} \cos(\theta_{cx2} - 3\theta_v + \theta) \end{cases} \tag{12}$$

where θ_{cx1} is the phase angle of carrier x_1, $x_1 = mod\ (round\ (1 + N\ (\theta_{c1} - 3\theta_v + \theta\ )/2\pi), N)$, θ_{cx2} is the phase angle of carrier x_2, $x_2 = mod\ (round\ (1 + N(\theta_{c1} - 3\theta_v + \theta - \pi)/2\pi), N)$. And $A_{1(-2)}$ is the harmonic amplitude, which can be calculated as:

$$A_{1(-2)} = \frac{1}{\pi}\int_{-\pi}^{\pi} e^{j(\frac{\pi}{2} - m_v \cos\theta + 2\theta)}\, d\theta \tag{13}$$

Thus, the maximum convergence speed with 150 Hz carrier frequency can be represented by $\Delta V_{cl150\,Hz\,max}$ as follows:

$$\begin{aligned} \Delta V_{cl150Hzmax} &= \Delta V_{clx150Hzmax} - \Delta V_{clx150Hzmin} \\ &= \frac{I_{sm}}{\omega C}\frac{\pi}{2} \times A_{1(-2)}\left[\cos(\theta_{cx2} - 3\theta_v + \theta)\right. \\ &\quad \left. - \cos(\theta_{cx1} - 3\theta_v + \theta)\right] \end{aligned} \tag{14}$$

Normalized by $I_{sm}/\omega C$, the relationship of $\Delta V_{cl150Hzmax}^*$, m_v and θ is illustrated in Fig. 6, where $\theta_{c1} = 0$, $\theta_v = 0$, and $N = 20$. Fig. 6 shows that, for the traditional CPS-PWM based balancing strategy, the convergence speed is mainly determined by m_v. Compared to the logic-based CPS-PWM based strategy, when the modulation index m_v is higher than 0.75, its normalized convergence speed is always above 0.3. Therefore, $\Delta V_{max}^* = 0.3$ is taken as the lowest acceptable convergence speed of the proposed balancing strategy.

It can be calculated from (11) or read from Fig. 5(b) that the logic-processed CPS-PWM scheme based voltage balancing strategy reaches a normalized convergence speed of 0.3 when $\theta \approx \pm\pi/3$ and $\pm 2\pi/3$. Hence the conclusion can be drawn that the application range of power factor angle is $\theta \in [-\pi/3, \pi/3] \| [-\pi, -2\pi/3] \| [2\pi/3, \pi]$. Fig. 7 illustrates the application ranges. Thus, it can be inferred that the proposed strategy is especially suitable for the HVDC transmission, which mainly deals with active power and has a modulation index higher than 0.75.

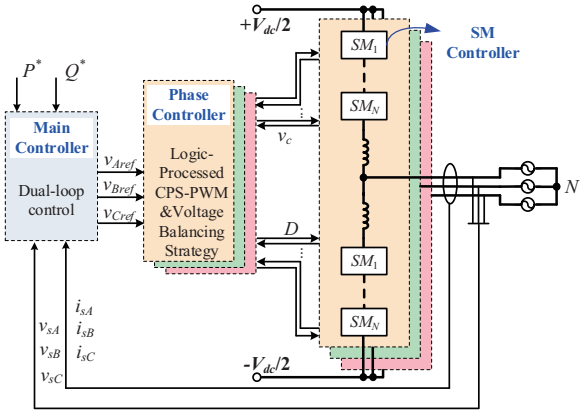

Fig. 8. The three-tier control architecture for logic-processed CPS-PWM based balancing strategy.

IV. Implementation of the Logic-Processed CPS-PWM Based Balancing Strategy

In the logic-processed CPS-PWM scheme, the manipulation of driving signals should be achieved without affecting the synchronization of switching actions among SMs. Otherwise, distorted voltage levels and defected arm currents will be induced [16]. As demonstrated in Fig. 8, a three-tier control system architecture is proposed. The control system is divided into three parts: the main controller, phase controllers and sub-module controllers. The main controller is one DSP controller, which is responsible for the high-level controls, such as active and reactive power control.

The phase controller utilizes FPGA as the control unit, which carries out the logic-processed CPS-PWM scheme based capacitor voltage balancing strategy. Since the generation and manipulation of driving signals are centralized in the middle-tier controller, the synchronization of switching actions is naturally guaranteed. Moreover, the logic process of driving signals is easy and cost-effective in FPGAs. The SM controllers only receive control signals from the phase controllers and report the capacitor voltage to the phase controllers.

TABLE I
PARAMETERS OF SIMULATION AND PROTOTYPE

Parameters	Simulation	Prototype
DC Bus Voltage (V_{dc})	19 kV	800 V
Apparent Power (S)	2 MVA	6 kVA
Line to Line Voltage ($V_{l\text{-}l}$, rms)	10 kV	400 V
Output Frequency (f)	50 Hz	50 Hz
Carrier Frequency (f_c)	450 Hz/150 Hz	450 Hz
Number of SMs in each arm (N)	20	8
Arm Inductance (L)	40 mH	40 mH
SM Capacitance (C)	3 mF	3 mF
Rated Capacitor Voltage (V_c)	950 V	100 V

V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the theoretical analysis, a 21-level three-phase grid-connected inverter is built in MATLAB Simulink and a 9-level three-phase grid connected prototype is established. The parameters of simulation and prototype are shown in Table I. And the carrier frequency (switching frequency) is set as 450 Hz for both simulation and experiment.

A. Simulation Results

Dual-loop control is adopted in the simulation, where the outer loop controls the active and reactive power and the inner loop controls the active and reactive current. The carrier phase angle difference for the logic processed driving signals is selected according to [14], so new driving signals with proper charging ability can be synthesized.

Simulation results with different power factor angles are presented in Fig. 9(a)–(c). The output voltage, output current, enable flag and execution flag of balancing strategy, and the lower arm capacitor voltages of phase A are presented successively. In order to verify the effectiveness of the balancing strategy, the capacitor voltages should be diverse at the initial state. Therefore, the balancing strategy is disabled at first, and the logic processed driving signals are intentionally assigned to specific SMs to charge and discharge the capacitors. This process is not illustrated in Fig. 9. After a preset timespan, the SMs are in unbalance state and they are re-assigned with their original driving signals. At the meantime, the balancing strategy is still disabled. As observed in Fig. 9(a)–(c), with the original high frequency driving signals, the capacitor voltages keep unchanged. This is because there is little difference in the charging ability of original driving signals, which verifies the theoretical analysis.

The balancing strategy is enabled at 0.3 s. And it can be seen from Fig. 9(a)–(c) that the capacitor voltages convergence speeds are different with different power factor angles. Fig. 9(d) is the simulation result of the traditional CPS-PWM scheme based balancing strategy with 150 Hz carrier frequency, and its power factor angle is π/3.

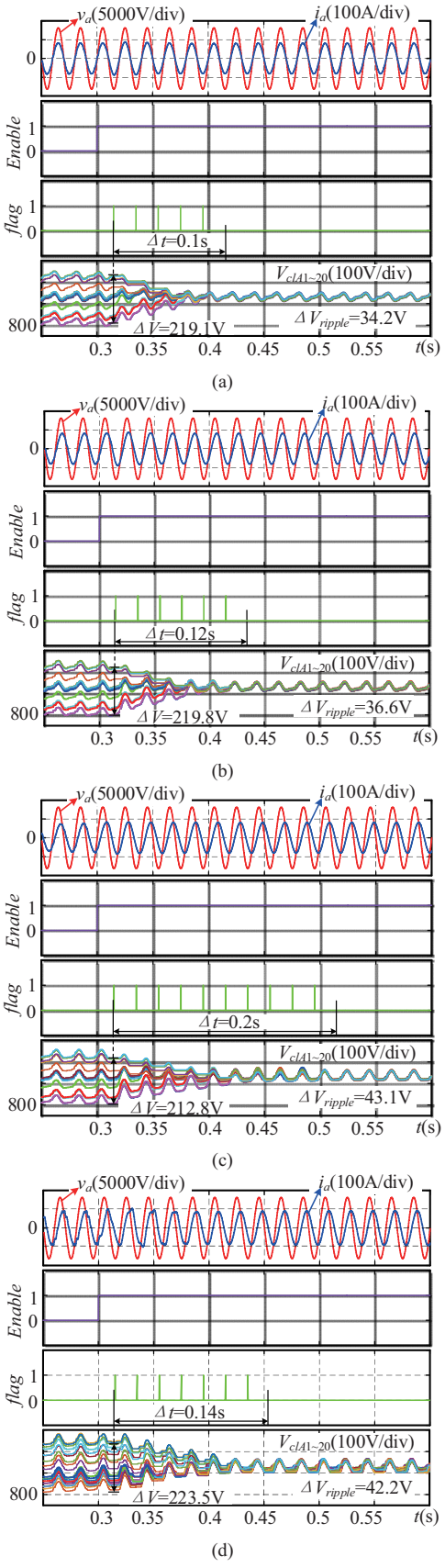

Fig. 9. Simulation results. (a) power factor angle θ = 0 with 450 Hz logic processed CPS-PWM, (b) θ = π/6 with 450 Hz logic processed CPS-PWM, (c) θ = π/3 with 450 Hz logic processed CPS-PWM, (d) θ = π/3 with 150 Hz traditional CPS-PWM.

TABLE II
COMPARISON OF SIMULATION RESULTS

Balancing Strategy	Logic Processed CPS-PWM			Traditional CPS-PWM
Carrier Frequency (f_c)	450 Hz			150 Hz
Power Factor Angle (θ)	0	$\pi/6$	$\pi/3$	$\pi/3$
Voltage Variation (ΔV)	220.3 V	219.8 V	212.8 V	223.5 V
Convergence Time (Δt)	0.1 s	0.12 s	0.2 s	0.14 s
Voltage Ripple (ΔV_{ripple})	34.2 V	36.6 V	43.1 V	42.2 V

Key performance characters of the simulation results are concluded in Table II. When the power factor angle θ changes from 0 to $\pi/6$, i.e., active power is still the major power component, the convergence speed difference is small. However, when reactive power becomes the major power component (power factor angle θ changes to $\pi/3$), the convergence time is two times longer than that with $\theta = 0$. It indicates that the convergence speed drops quickly with the increase of reactive power. Compared with the traditional CPS-PWM scheme based balancing strategy (seven fundamental periods), the convergence speed of logic processed CPS-PWM scheme based balancing strategy is much slower when power factor angle reaches $\pi/3$ (ten fundamental periods). This result verifies the proposed application ranges of power factor angle in Section III.

B. Experimental Results

Similarly, the logic-processed voltage balancing strategy is disabled at first, and the driving signal synthesized by logic *OR* process of the 1st and the 5th carriers is assigned to SM_1, and the driving signal synthesized by logic *AND* process is assigned to SM_8. Besides, the rest SMs' driving signals remain unchanged. Consequently, the capacitor voltages of SM_1 and SM_8 diverge from their rated value.

Three cases are studied in this section, i.e., the power factor angle equals to 0, $\pi/6$ and $\pi/3$. The experimental results are presented in Fig. 10(a), (b), (c). The output voltage, output current, capacitor voltages of SM_1, SM_5 and SM_8 in the lower arm of phase A, execution flag and enable flag of the balancing strategy are depicted in sequence in each figure. It should be noticed that, in order to keep a high convergence speed and avoid the possible voltage oscillations, the selection of carrier phase angle difference for logic processing is divided into three regions according to the voltage divergence degree as introduced in [14]. Therefore, the convergence time is indicated by the execution flag of the outermost region *flag* 1 and the innermost region *flag* 3. The key experimental results are concluded in Table III. It is consistent with the analysis and simulation that the convergence time increases with the increase of reactive power component. And when the power factor angle θ reaches $\pi/3$, the convergence speed drops a lot compared to the condition when $\theta = 0$ (from five fundamental periods to fifteen fundamental periods).

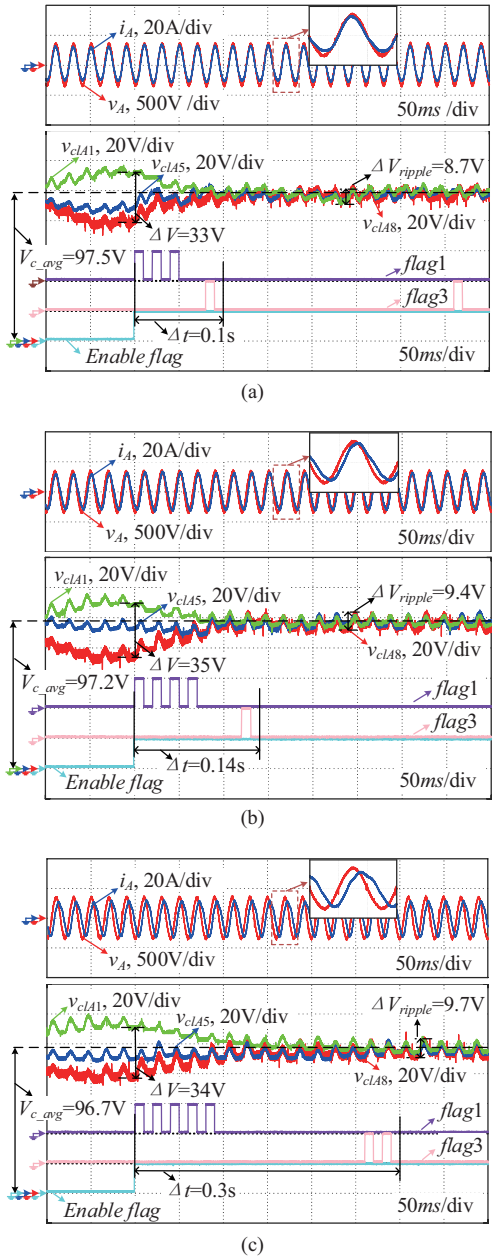

Fig. 10. Experimental results for 450 Hz logic-processed CPS-PWM based balancing strategy, (a) power factor angle $\theta = 0$, (b) $\theta = \pi/6$, (c) $\theta = \pi/3$.

TABLE III
COMPARISON OF EXPERIMENTAL RESULTS

Balancing Strategy	Logic Processed Scheme With FFSA		
Carrier Frequency (f_c)	450 Hz		
Power Factor Angle (θ)	0	$\pi/6$	$\pi/3$
Voltage Variation (ΔV)	33 V	35 V	34 V
Convergence Time (Δt)	0.1 s	0.14 s	0.3 s
Voltage Ripple (ΔV_{ripple})	8.7 V	9.4 V	9.5 V

VI. Conclusion

The convergence speed and application ranges of the logic-processed CPS-PWM scheme based balancing strategy is analyzed in this paper. It is revealed through mathematical analysis that the convergence speed is mainly determined by the power factor of MMC. And by comparing with the normal CPS-PWM scheme based balancing strategy, the application ranges of power factor angle for the proposed balancing strategy is derived, i.e., $[-\pi/3, \pi/3] \parallel [-\pi, -2\pi/3] \parallel [2\pi/3, \pi]$. It indicates that this strategy is especially suitable for MMC-HVDC transmissions, which mainly deals with active power. Besides, with the proposed three-tier control system, CPS-PWM and logic process are centralized in the phase-controllers (FPGA). Therefore, the synchronization of switching actions is guaranteed naturally. The theoretical analysis is validated by both simulation and experimental results.

References

[1] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 4–17, Jan. 2015.

[2] A. Nami, J. Liang, F. Dijkhuizen and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 18–36, Jan. 2015.

[3] H. Alyami and Y. Mohamed, "Review and development of MMC employed in VSC-HVDC systems," in *Proc. IEEE CCECE*, DOI: 10.1109/CCECE.2017.7946676, pp. 1–6, 2017.

[4] M. Hagiwara, R. Maeda and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," *IEEE Trans. Power Electron*., vol. 26, no. 6, pp. 1649–1658, Jun. 2011.

[5] R. Lizana, M. A. Perez, D. Arancibia, J. R. Espinoza and J. Rodriguez, "Decoupled current model and control of modular multilevel converters," *IEEE Trans. Ind. Electron*., vol. 62, no. 9, pp. 5382–5392, Sept. 2015.

[6] R. Zeng, L. Xu, L. Yao and S. J. Finney, "Analysis and control of modular multilevel converters under asymmetric arm impedance conditions," *IEEE Trans. Ind. Electron*., vol.63, no.1, pp.71–81, Jan. 2016.

[7] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron*., vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[8] S. Fan, K. Zhang, J. Xiong and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 358–371, Jan. 2015.

[9] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech. Conf*., vol. 3, pp. 6, Jun. 2003, doi: 10.1109/PTC.2003.1304403.

[10] Q. Tu, Z. Xu and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del*., vol. 26, no. 3, pp. 2009–2017, July 2011.

[11] H. Peng, Y. Wang, Z. Lv, Y. Deng, X. He and R. Zhao, "Capacitor voltage balancing based on fundamental frequency sorting algorithm for modular multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo*., Sept. 2014, pp. 1639–1644, doi: 10.1109/ECCE.2014.6953614.

[12] H. Peng, R. Xie, K. Wang, Y. Deng, X. He and R. Zhao, "A capacitor voltage balancing method with fundamental sorting frequency for modular multilevel converters under staircase modulation," *IEEE Trans. Power Electron*. vol. 31, no. 11, pp. 7809–7822, Nov. 2016.

[13] G. Chen, H. Peng, R. Zeng, Y. Hu and K. Ni, "A fundamental frequency sorting algorithm for capacitor voltage balance of modular multilevel converter with low frequency carrier-phase-shift modulation," *IEEE J. Emerging Sel. Topics Power Electron*., vol. 6, no. 3, pp. 1595–1604, Sept. 2018.

[14] K. Wang, Y. Deng, H. Peng, G. Chen, G. Li, and X. He, "An improved CPS-PWM scheme based voltage balancing strategy for MMC with fundamental frequency sorting algorithm," *IEEE Trans. Ind. Electron*., vol. 66, no. 3, pp. 2387–2397, Mar. 2019.

[15] L. Zhou, K. Wang, Y. Deng, Y. Lu, C. Wang and F. Xu, "Convergence speed analysis of capacitor voltage balancing strategy for MMC with logic processed CPS-PWM scheme," in *Proc. 2018 IEEE Int. Power Electron. Appl. Conf. Expo. (PEAC)*, Nov. 2018, pp. 1–6, doi: 10.1109/PEAC.2018.8590429.

[16] S. Huang, R. Teodorescu and L. Mathe, "Analysis of communication based distributed control of MMC for HVDC," in *2013 15th Eur. Conf. Power Electron. Appl. (EPE)*, Lille, 2013, pp. 1–10.doi: 10.1109/EPE.2013.6634711.

Kun Wang received the B.E.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2013. He is currently working toward the Ph.D. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China. His current research interests include modular multilevel converters, dc-dc converters and grid-connected photovoltaic systems.

Leyuan Zhou received B.Eng from Nanjing University of Science and Technology, China, in 2015. He is currently working towards his M.S. degree in Power Electronics and Motor Drives. His current research interests include modular multilevel converters (MMC) and the inter-connection of multi-end in the distribution network.

Yan Deng received the B.E.E. degree from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1994, and the Ph.D. degree in power electronics and electric drives from the College of Electrical Engineering, Zhejiang University, in 2000.

Since 2000, he has been a faculty member at Zhejiang University, teaching and conducting research on power electronics. He is currently a professor with Zhejiang University. His research interests are topologies and control for switch-mode power conversion.

Yi Lu received his B.S. degree in Electrical Engineering from North China Electric Power University, Baoding, China, in 2001. He received his M.S. and Ph.D. degrees in Intelligence Engineering and Electrical Engineering from the University of Liverpool, Liverpool, U.K., in 2002 and 2007, respectively. In 2008, he joined the State Grid Zhejiang Electric Power Research Institute, Hangzhou, China. He is a senior engineer, and his research interests include HVDC and FACTS.

Chaoliang Wang received his B.S. and M.S. degrees in Electrical Engineering from North China Electric Power University, Beijing, China, in 2011 and 2014, respectively. Since 2014, he has been an engineer at State Grid Zhejiang Electric Power Research Institute, Hang Zhou, China. His current research interests include HVDC and FACTS.

Feng Xu was born in Zhejiang, China, in February 1988. He received the B.S. and Ph.D. degrees in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2010 and 2015 respectively. Currently, he works in State Grid Zhejiang Electric Power Research Institute. His research focus is on high power electronics technology, LCC-HVDC transmission system, VSC-HVDC transmission system, and DC grid.

Two-Type Single-Stage Isolated Modular Multilevel Cascaded Converter (I-M^{2}C^2) Topologies

Chuang Liu, Lianxin Wen, Dongfeng Yang, Hong Ying, Chao Liu, and Haoran Zhang

***Abstract*—This paper introduces two types of single-stage high-frequency isolated converters named isolated modular multilevel converter (I-M^{2}C) and isolated modular cascaded converter (I-MC^2), which are both based on the high-frequency-link concept. The two converters can totally reduce the individual DC-link capacitors at the high-voltage (HV) side and simplify the voltage balancing control. The fundamental principle and applied modulation strategy scheme of I-M^{2}C and I-MC^2 are given in details. The operation mode of I-M^{2}C is analysed as an example. Experimental results are given respectively to illustrate the efficient operating characteristics of the two new types of converters.**

***Index Terms*—High-frequency-link (HFL), hybrid AC and DC power conversion, isolated modular multilevel cascaded converter (I-M^{2}C^2), solid-state transformer.**

I. Introduction

CURRENTLY, with the burgeoning development of power semiconductor technology, solid-state transformer (SST) [1]–[7] has been conceived as a replacement for the conventional line-frequency transformer providing galvanic isolation by means of medium/high-frequency transformers. SST is a key equipment in the future solid-state substation (SSS) [8] with hybrid AC and DC power conversion function, which is easy for the flexible grid integration of renewable energy systems [9], [10]. Modular architecture can bring advantages to the power and voltage scalability and maintenance, as well as the fault-tolerance strategy implementation, and the SST modular systems are generally based on the input-series output-parallel (ISOP) configuration of converter cells, which could be classified into two broad categories: the cascade H-bridge (CHB) converter [11]–[15] and the MMC [7]–[16] based structures as shown in Fig. 1.

From the high-voltage AC side to the common low-voltage DC side, the two structures both have two-stage power conversion. Because of the galvanic isolation for the individual DC side of the cascaded converter and MMC, high-value bulky capacitors are needed to buffer the double-line-frequency (DLF) power oscillation that leads to the space volume problem [17], [18], which may restrict its development in real world application.

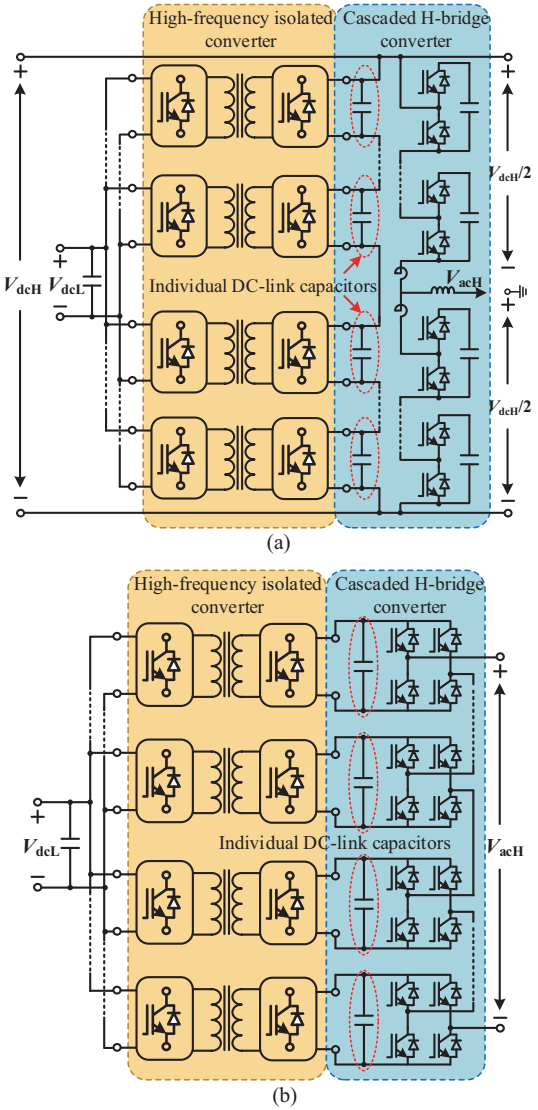

Fig. 1. Typical SST topology between medium-AC and low-DC sides. (a) Single-phase MMC based SST topology. (b) Single-phase CHB based SST topology.

In order to face the future demand of hybrid DC and AC application in SSS application, except for the basic requirements of modular realization, multilevel waveform, high availability, failure management, investment and life cycle cost on the

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C. Liu, L. Wen, D. Yang, C. Liu, and H. Zhang are with Northeast Electric Power University, Jilin 132012, China (e-mail: victorliuchuang@163.com; 423867026@qq.com; ydfnedu@126.com; 774416591@qq.com; 648827329@qq.com).

H. Ying is with Zhejiang Huayun Clean Energy CO. LTD, Hangzhou 310002, China (e-mail: Ying_Hong@zj.sgcc.com.cn).

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modular multilevel cascaded converter (MMCC) [19], the expected main technical and economic aspects of the MMCC's development are:

- Multiport AC and DC system:
  Three basic voltage-level ports of high-voltage AC (HVAC), high-voltage DC (HVDC), and low-voltage DC (LVDC);
- High-frequency galvanic isolation:
  The high isolation voltage between HVAC/DC and LVDC sides with modularity high-frequency transformers;
- Expected requirement of fewer capacitors:
  It will overcome the space problem of individual DC-link capacitors in the CHB and MMC based isolated multilevel converters;
- Simplicity of the control system:
  The entire control system will be without complex multi-loop assisted control, such as voltage balancing.

In consideration of the problems mentioned above, the main contribution of this paper is it first introduces the high-frequency-link (HFL) concept into the MMC and CHB topologies, and proposes two new converters named I-M^{2}C and I-MC^2. The new two-type converters inherit the main merits of the traditional MMC and CHB such as the modular structure, multi-port and multilevel waveform. Thanks to the single-stage power conversion, the bulky DC-link capacitors at the high-voltage side can be eliminated, which avoids the complicated capacitor voltage balancing control. Moreover, compared with the conventional high-frequency link matrix inverter, bidirectional switches at the HV side and bidirectional switches commutation control strategy are avoided because of the positive sub-modules port voltages based on the hybrid AC and DC voltage conversion.

The rest of this paper is organized as followings. In Section II, topologies of the two-type converters are described. Operation principles of I-M^{2}C and I-MC^2 are described in Section III. Experimental results are given in Section IV, the results verify the feasibility of the two novel converter topologies.

II. Concept of Single-Stage Isolated Modular Multilevel Cascaded Converter (I-M^{2}C^2)

Considering that the circuit topologies of the conventional MMC and CHB based SST are derived from the chopper and full-bridge cells, the sub-module configurations of I-M^{2}C and I-MC^2 are proposed in Fig. 2. Fig. 2(a) shows the isolated chopper cells (I-CC) which form the isolated modular multilevel converter (I-M^{2}C); and the isolated modular cascaded converter (I-MC^2) is shown in Fig. 2(b), which is comprised of isolated bridge cells (I-BC). Moreover, the I-BC can be regarded as two I-CCs connecting in parallel at the front-stage and in reverse at the back-stage. Thanks to the high-frequency-link concept of direct single-stage power conversion, port voltage of ab (ac/bc) is clamped to the LVDC voltage and impulses are transferred to the common LVDC side. Thus DC-link capacitors at the HV side can be eliminated in the proposed structures.

According to the two modular cells mentioned above, two types of single-stage isolated modular multilevel cascaded

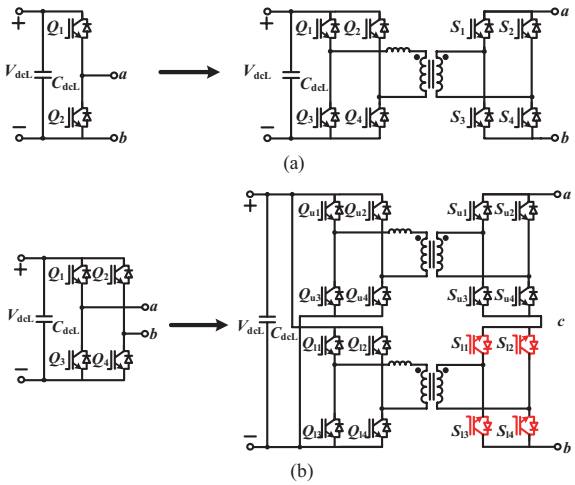


Fig. 2. Deducing of I-M^{2}C^2 sub-module cell. (a) Isolated chopper cell (I-CC) deduced from traditional chopper circuit. (b) Isolated bridge cell (I-BC) deduced from traditional bridge circuit.

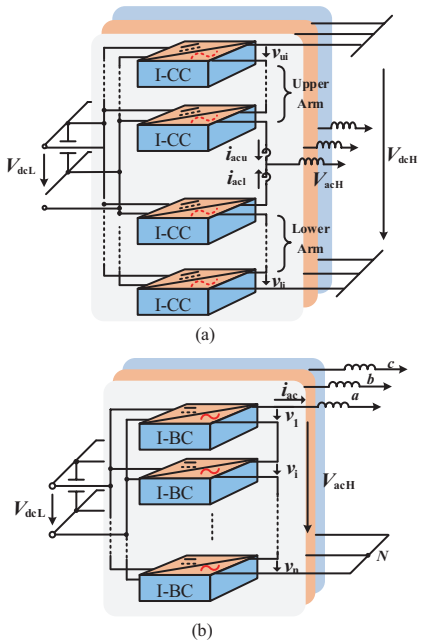


Fig. 3. Topology configuration of I-M^{2}C^2. (a) Isolated modular multilevel converter (I-M^{2}C) based on isolated chopper cell (I-CC). (b) Isolated modular cascaded converter (I-MC^2) based on isolated bridge cell (I-BC).

converter topologies can be constructed respectively, as shown in Fig. 3. The I-CC modules constitute the isolated modular multilevel converter (I-M^{2}C) in the form of MMC while the isolated modular cascaded converter (I-MC^2) is structured by the I-BC modules in the form of input-series output-parallel (ISOP).

Compared to the MMC and CHB structures, the proposed two-type structures have no need for the intermediary DC-link capacitors at the high-voltage side and the power pulsations are buffered by the common capacitors at the LVDC side. Thus a double-line frequency power decoupling circuit can be applied to the primary side to reduce the capacitors effectively [20]. For a three-phase system based on the I-M^{2}C^2 structure, volume of the LVDC capacitors can be very small because of the balance

of the three-phase instantaneous power fluctuation. Therefore, the reduced capacitance of DC-link capacitors [21] at the HV side can be calculated by

$$C = \frac{P_{dc}}{\omega V_{dc} \Delta V_{dc}} \tag{1}$$

where P_{dc} is the average value of the input power from the DC side, ω is the angular frequency, V_{dc} is the DC bus voltage, and ΔV_{dc} is the allowed peak-to-peak voltage variation.

A. Isolated Modular Multilevel Converter (I-M²C)

An I-M²C leg consisting of n I-CCs based on the ISOP connection in upper and lower arms, has three basic voltage ports: HVDC V_{dcH}, HVAC v_{ac}, and LVDC V_{dcL}, as shown in Fig. 3(a). Compared to the sub cell in MMC, the sub structure in I-M²C is high-frequency isolated, which consists of dual active H-bridges, high-frequency link (HFL) transformer and capacitors at the low-voltage side. Regardless of the direction of current $i_{acu/l}$, terminal voltage v_{ui} or v_{li} of each cell can be switched to either 0 V or V_{dcL}/k (k is the HFL transformer turn(conversion) ratio) to reflect the desired average value. Thus the total terminal performance at the high-voltage side in I-M²C is almost the same as that in the conventional MMC. Regardless of the voltage drop of the leakage and arm inductors, (2) shows the relationship between V_{dcL}, v_{ui} or v_{li} of each cell and the total terminal voltage v_{su} or v_{sl} of each arm.

$$\begin{cases} v_{su} = \sum_{i=1}^{n} v_{ui} = \sum_{i=1}^{n} d_{ui} \times \frac{u_{dcL}}{k_{ui}} = d_u \times \frac{n \cdot u_{dcL}}{k} \\ v_{sl} = \sum_{i=1}^{n} v_{li} = \sum_{i=1}^{n} d_{li} \times \frac{u_{dcL}}{k_{li}} = d_l \times \frac{n \cdot u_{dcL}}{k} \end{cases} \tag{2}$$

where d_{ui} and d_{li} ($i = 1, \ldots, n$) are the equivalent modulation ratios of each module, k_{ui} and k_{li} ($i = 1, \ldots, n$) are the transformer ratios of each module; generally speaking, it can be assumed that $d_u = d_{ui}$, $d_l = d_{li}$, $k = k_{ui} = k_{li}$ ($i = 1, \ldots, n$).

Then the HVDC V_{dcH} and HVAC V_{ac} can be given as in (3).

$$\begin{cases} V_{dcH} = v_{su} + v_{sl} = \frac{n \cdot u_{dcL}}{k} \times (d_u + d_l) \\ v_{ac} = -v_{su} + \frac{V_{dcH}}{2} = v_{sl} - \frac{V_{dcH}}{2} \end{cases} \tag{3}$$

To get pure HVDC V_{dcH} and HVAC V_{ac}, d_u and d_l should satisfy the following conditions:

$$\begin{cases} d_u = D + d_a = 0.5 + d_{am} \sin(\omega t + \theta) \\ d_l = D - d_a = 0.5 - d_{am} \sin(\omega t + \theta) \end{cases} (0 \leqslant d_{u,l} \leqslant 1) \tag{4}$$

where the DC modulation index D can be set at 0.5 which is the same as MMC, and the maximum amplitude of AC modulation index d_a is 0.5 to ensure the total value of $d_{u,l}$ which should be between 0 and 1, so that d_a could satisfy the sub-module (SM) operating conditions.

Based on (4), we can get:

$$\begin{cases} V_{dcH} = \left(\frac{n \cdot u_{dcL}}{k} \right) \times (2D) = \frac{n \cdot u_{dcL}}{k} \\ v_{ac} = -\left(\frac{1}{2} + d_a \right) \times (n \cdot u_{dcL}/k) + \frac{V_{dcH}}{2} = -\frac{n \cdot u_{dcL}}{k} d_a \end{cases} \tag{5}$$

where $0 \leq d_{am} \leq 0.5$ and Fig. 2 shows the representative HVDC (v_{dcH}) and HVAC (v_{acH}) output voltage waveforms with arm voltages v_u and v_l.

The high frequency transformers have to withstand a full HV dc voltage as the conventional MMC structure. Thus, application scenarios of the proposed structure are similar to the conventional MMC structure, especially for the Medium Voltage Grids. Meanwhile, because all cells' secondary side voltages are based on the same V_{dcL}, present manufacturing process can ensure that voltage errors of the cells in the same arm are in a reasonable range, which is in no need for the cell voltage balancing control. Although voltage errors between the two arms can cause the arm voltage imbalance which may lead to circulation current between i_{acu} and i_{acl}, balance of the arm voltage can be realized by an additional auxiliary control, which is simpler than the conventional MMC structure. Above all, this new type of I-M²C has the basic triple ports of HVAC, HVDC and LVDC. It is especially suitable for the hybrid DC and AC application in power generation and transmission, such as solid-state transformer (SST), energy router.

B. Isolated Modular Cascaded Converter (I-MC²)

The single-phase cluster of I-MC² consists of n I-BCs based on the ISOP connection. The terminal voltage v_i of I-BC can be regarded as the sum of two sub-module's port voltages v_{ui} (v_{li}). Regardless of the polarity of current i_{ac}, terminal voltage v_{ui} (v_{li}) of the upper (lower) sub-module can be switched to either 0 V or V_{dcL}/k ($-V_{dcL}/k$) to have the desired average value.

Regardless of the voltage drop of the leakage inductors, (6) shows the relationship between V_{dcL}, v_{ui} or v_{li} of each sub-module.

$$\begin{cases} v_{ui} = d_{ui} \times \frac{u_{dcL}}{k_{ui}} \\ v_{li} = -d_{li} \times \frac{u_{dcL}}{k_{li}} \end{cases} \tag{6}$$

And the HVAC V_{acH} can be given as in (7)

$$\begin{aligned} V_{acH} &= \sum_{i=1}^{n} v_i = \sum_{i=1}^{n} (v_{ui} + v_{li}) \\ &= n\left(2\frac{u_{dcL}}{k} d_a \right) \end{aligned} \tag{7}$$

where v_i denotes the voltage of the terminal (ab) in Fig. 2(b). Modulation index $d_{u,l}$ and transformer ratio k are exactly the

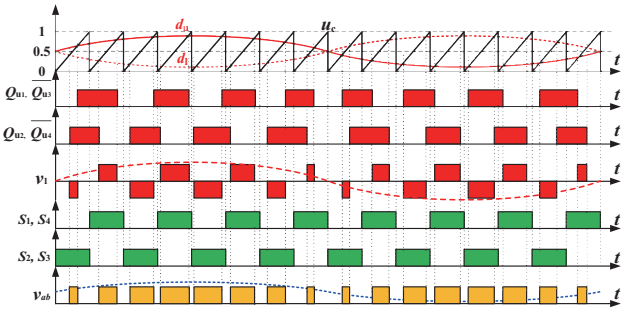


Fig. 4. Driven signal modulation strategy for I-CC.

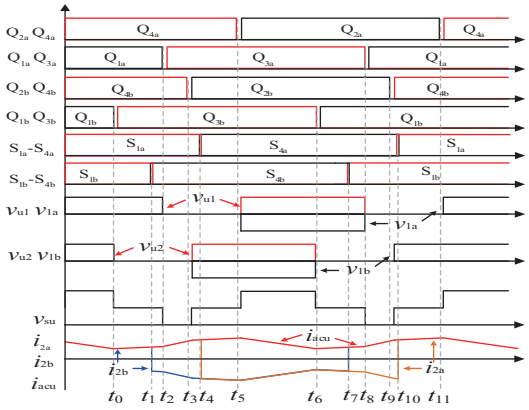


Fig. 5. Theoretical waveforms of the upper arm in I-M^{2}C.

same as mentioned above in I-M^{2}C.

In theory, because of the inconsistency of the sub-modules' characteristic parameters, especially the transformer parameters, the DC modulation index D of the upper and lower sub-modules can not be eliminated completely, thus leading to the output voltage deviation with a certain amount of DC component. Nonetheless, modular manufacturing or simple DC-component suppression control can avoid this dilemma without increasing the complexity of the system. I-MC^2 has the characteristic of high power density thanks to single-stage power conversion and less capacitor volume. Thus the advantages of I-MC^2 are more prominent in some applications where volumes are restricted, e.g., traction equipment and integration of renewable energy system.

III. Operation Principles of I-M^{2}C^2

A. Isolated Modular Multilevel Converter (I-M^{2}C)

In order to realize the natural commutation and avoid other problems in the process of commutation, such as voltage distortion, modulation strategy for a single I-CC module of I-M^{2}C is given by referring to the existing isolated phase-shifted full-bridge (PSFB) modulation strategy and the cycloconverter modulation strategy, as shown in Fig. 4.

As shown in Fig. 4, driven signals of the primary side in an I-CC are based on the equivalent hybrid modulation variable d_u and d_l in (4), compared to the carrier u_c. The switching frequency f_s is half of the sawtooth carrier frequency f_c. And in the upper arm of the secondary side, driven signals of S_{4i} are the same as driven signals of S_{1i}; driven signals of S_{2i} and S_{3i} are symmetric with the signals of S_{1i} ($i = a, b$). Driven signals of the lower arm are the same as the corresponding signals of the upper arm. The driven signals are designed to maintain the "on" state at the entire odd or even carrier cycles, to ensure the switching process of the secondary side, IGBTs always happen when the primary side IGBTs work on the circulation process. To avoid the voltage spike occurrence during HV side H-bridge inverter commutation, "commutation overlap" is also employed to enable natural commutation between unidirectional switches.

Because the sub-module (SM) terminal voltages v_{ui} or v_{li} ($i = 1, \ldots, n$) are always positive, based on the arm current i_{acu} or i_{acl} direction as shown in Fig. 3(a), there are two operation modes for the SMs: 1) buck mode: instantaneous power flow from the common LVDC side to the high-voltage side, and 2) boost mode: instantaneous power flow from the high-voltage side to the common LVDC side, which are the same as the conventional bidirectional phase-shift full-bridge (PSFB) PWM DC-DC converter except that the duty ratio is varying. When the proposed structure works in buck mode, all the active switches at the primary side are Zero Voltage Switching (ZVS), as the conventional PSFB converter. To simplify the analysis of boost mode, this paper assumes that body capacitance of the switches are negligible and the current commutation process is so little that it can be viewed as instantaneous fulfilled.

The theoretical waveforms and commutation step diagrams of the 2-module I-M^{2}C with phase-shift control during a switching cycle are shown in Figs. 5 and 6, where $Q_{1a,\ 1b} - Q_{4a,\ 4b}$ and $S_{1a,\ 1b} - S_{4a,\ 4b}$ are the driven signals of the corresponding switches $S_{u1a,\ u1b} - S_{u4a,\ u4b}$ in Fig. 6; v_{1a} and v_{1b} are the primary pulse-width voltages of the HFT_1 and HFT_2; v_{u1} and v_{u2} are the output voltages of the SM_{u1} and SM_{u2}; i_{1a} and i_{1b} are the primary currents of the HFT_1 and HFT_2; i_{2a} and i_{2b} are the secondary currents of the HFT_1 and HFT_2; i_{acu} is the inductor current of the upper arm.

One complete switching cycle of SM_{u1} and SM_{u2} can be divided into twelve steps in this operation mode. The former six steps are explained in details as follows.

Mode 0: [before t_0, Fig. 6(a)] At the secondary side, S_{1a}, S_{4a}, S_{1b} and S_{4b} are conducting, $i_{2a} = i_{2b} = i_{acu}$. At the primary side, Q_{1a}, Q_{4a}, Q_{1b} and Q_{4b} are all ON, $i_{1a,\ 2b}$ only flows through the antiparallel diodes of $Q_{1a,\ 1b}$ and $Q_{4a,\ 4b}$. Power is transferred from the stored energy of the inductor and source at the HV side to the common DC side. The absolute value $|i_{acu}|$ of the arm-inductor current decreases over time.

Mode 1: [t_0–t_1, Fig. 6(b)] At t_0, Q_{1b} is turned off, and Q_{3b} is turned on. Current i_1 is commutated from the antiparallel diode of Q_{1b} to Q_{3b}. Q_{1b} can have ZCS. Operation stage of the SM_{u2} has not changed.

Mode 2: [t_1–t_2, Fig. 6(c)] At t_1, S_{1b} and S_{4b} are turned off, S_{2b}

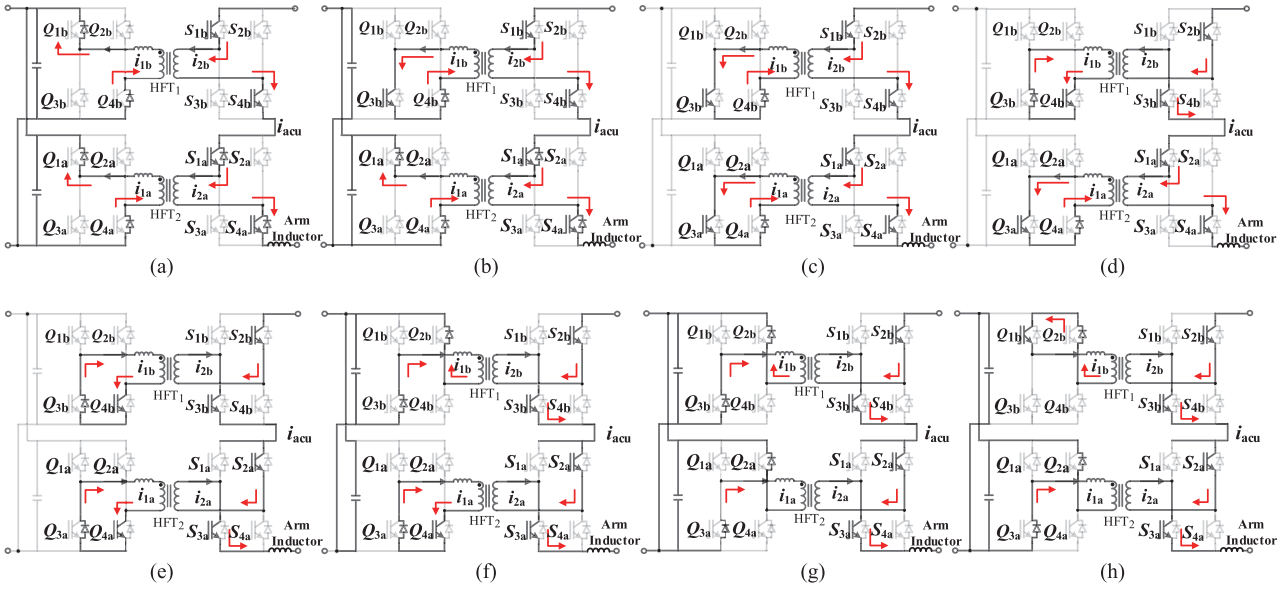


Fig. 6. Operation modes of the upper arm in I-M^{2}C.

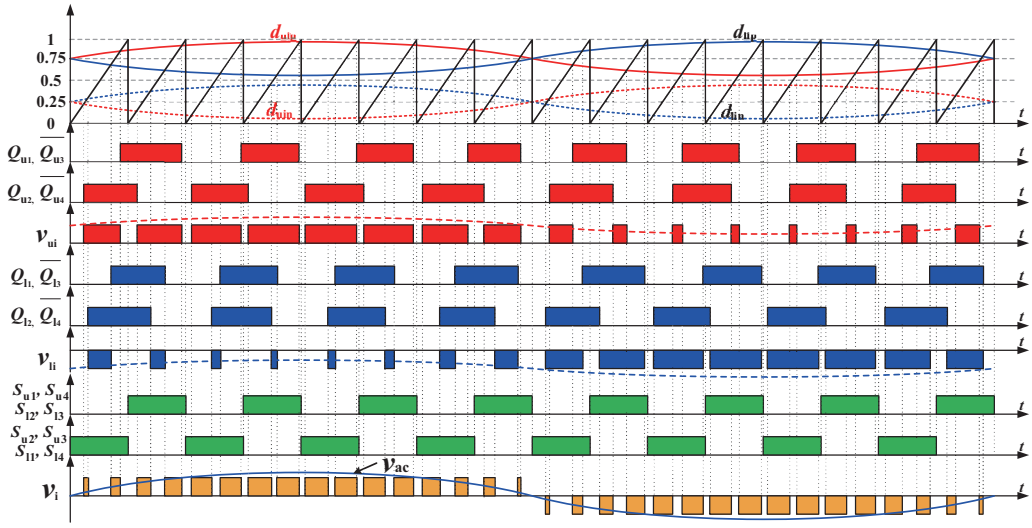


Fig. 7. Driven signal modulation strategy for I-BC.

and S_{3b} are turned on. In practice, an overlap of dead band must be guaranteed for the current i_2 commutation from S_1 and S_4 to S_2 and S_3 at the secondary side. Current i_{1b} is commutated from the antiparallel diode of Q_{4b} and Q_{3b} to the antiparallel diode of Q_{3b} and Q_{4b}. After the current i_2 commutation, $|i_{acu}|$ continues increasing.

Mode 3: [t_2–t_3, Fig. 6(d)] At t_2, Q_{1a} is turned off, and Q_{3a} is turned on. Current i_{1a} is commutated from the antiparallel diode of Q_{1a} to Q_{3a}. Q_{1a} can have ZCS. Operation stage of the SM_{u1} has not changed.

Mode 4: [t_3–t_4, Fig. 6(e)] At t_3, Q_{4b} is turned off, and Q_{2b} is turned on. Current i_{1b} is commutated from Q_{4b} to the antiparallel diode of Q_{2b}. Operation stage of the SM_{u2} has not changed.

Mode 5: [t_4–t_5, Fig. 6(f)] At t_4, S_{1a} and S_{4a} are turned off, S_{2a} and S_{3a} are turned on. Current i_{1a} is commutated from the antiparallel diode of Q_{4a} and Q_{3a} to the antiparallel diode of Q_{3a} and Q_{4a}. Operation stage of the SM_{u1} has not changed.

Mode 6: [t_5–t_6, Fig. 6(g)] At t_5, Q_{4a} is turned off, and Q_{2a} is turned on. Current i_{1a} is commutated from Q_{4a} to the antiparallel diode of Q_{2a}. Step 6 is symmetrical with Step 0. The latter six steps begin, and the working condition is symmetric with the former steps. It is unnecessary to go into details here.

B. Isolated Modular Cascaded Converter (I-MC^2)

The driven signal modulation strategy of I-BC is similar to that of I-CC. And the modulation strategy of a single I-BC module is given as shown in Fig. 7. The switching driven signals of I-MC^2 are based on the equivalent hybrid modulation variable d_{uip}, d_{uin}, d_{lip}, d_{lin} in (8) compared to the same carrier u_c. The equivalent modulation ratio d_{ui} and d_{li} are the same as that mentioned above and should satisfy the condition as well.

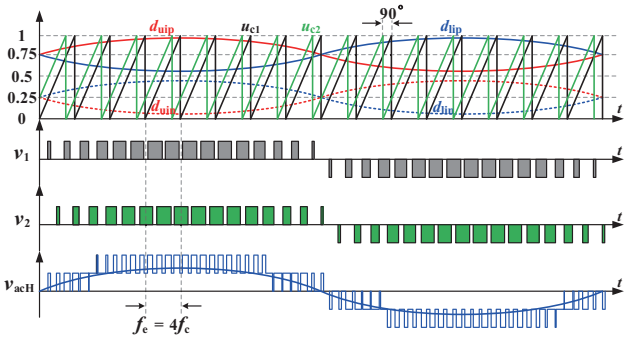
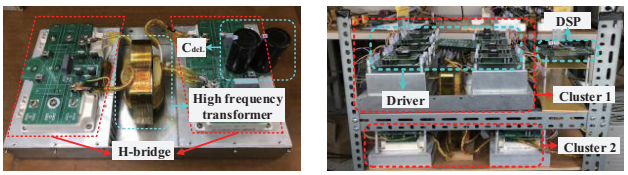


Fig. 8. Modulation strategy for 2-module I-MC^2 with 90° phase-shift.



(a) (b)

Fig. 9. A scaled-down laboratory single-phase system. (a) I-CC module. (b) Single-phase system.

$$\begin{cases} d_{uip} = 0.5 + d_{ui} = 0.5 + 0.5 \times [0.5 + d_{am} \times \sin(\omega t)] \\ d_{uin} = 0.5 - d_{ui} = 0.5 - 0.5 \times [0.5 + d_{am} \times \sin(\omega t)] \\ d_{lip} = 0.5 + d_{li} = 0.5 + 0.5 \times [0.5 - d_{am} \times \sin(\omega t)] \\ d_{lin} = 0.5 - d_{li} = 0.5 - 0.5 \times [0.5 - d_{am} \times \sin(\omega t)] \end{cases} \quad (8)$$

For the multilevel cascaded structure, the phase-shift switching scheme can increase the equivalent switching frequency, leading to significantly less output voltage ripple. Therefore the carrier of n multi-module cascaded I-MC^2 can be shifted by $T_c/2n$ to generate multilevel voltage. For example, Fig. 8 shows the modulation strategy for the 2-module I-MC^2 with 90° phase-shift control. And the carrier phase-shift switching scheme is also applied in the multi-module I-M^{2}C system.

The operation mode of I-BC on the condition of $i_{ac} > 0$ can be divided into fourteen steps. However, since the operation principle of I-BC is analogous to that of I-CC, the working mode of I-BC resembles that of I-CC as well. Therefore it is redundant to discuss the operation mode of I-BC in particular here.

IV. Experimental Results of Single-Phase I-M^{2}C^2

A scaled-down laboratory single-phase system is constructed to verify the proposed I-M^{2}C^2 topologies as shown in Fig. 9. The LVDC common side is supported by the DC voltage source, the HVDC side is connected to the resistors, and the HVAC side is connected to the inductive and resistive load.

To construct the HVAC current loop, a split capacitor at the HVDC side is adopted in I-M^{2}C. Since some experimental parameters of the I-M^{2}C and I-MC^2 are the same, parameters of the experimental system are shown together in Table I.

A. Experiment results of I-M^{2}C

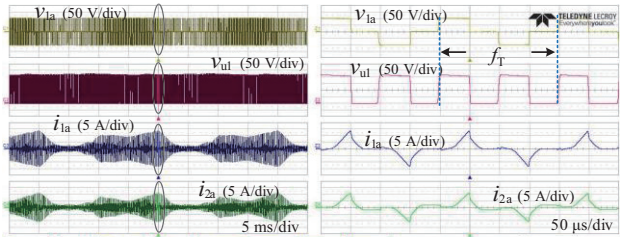
Firstly, Figs. 10, 11, 12, and 13 show the experimental steady-state waveforms when DC load R_{dc} = 160 Ω and AC load Z_{ac} = 160 + j48.4 Ω. Fig. 10 (a) shows the primary side voltage v_{1a}, primary side current i_{1a}, secondary current i_{2a} and output voltage v_{u1} experimental waveforms of the SM$_{u1}$. Fig. 10(b) shows the detailed waveforms in Fig. 10(a). It can be known that the frequency of SM output voltage is 2 times of the primary voltage.

Fig. 11(a) shows the output voltage of SM$_{u1}$ and SM$_{u2}$ and the voltage and current of the upper arm. Fig. 11(b) shows the detailed waveforms in Fig. 11(a). It shows that the output voltage frequency of the whole upper arm is twice of that of the single SM by the PS modulation strategy.

Fig. 12(a) and (b) show the overall and detailed experimental waveforms of the upper arm and lower arm. And the voltage and current waveforms show that the operation state of the proposed converter can be changed freely between buck mode and boost mode. Additionally, it can be seen that the transformer frequency f_T is the same as f_s and the equivalent inductor current

TABLE I
Circuit Parameters of Single-Phase I-M^{2}C^2

Parameter	Symbol	Value
LVDC voltage	V_{dcL}	200 V
Cascade SM number of each cluster	n	2
HVAC output filer	L_f, C_f	L_f = 0.5 mH, C_f = 2 μF
LVDC capacitor	C_{dcL}	C_{dcL} = 4 mF
Sawtooth carrier frequency	f_c	10 kHz
HFT turn ratio	k	17:17.5
HFT leakage inductor	L_k	4 μH
I-M^{2}C		
RMS HVAC voltage	v_{ac}	112 Vrms
HVDC voltage	V_{dcH}	400 V
Arm inductor	L_m	L_m = 0.5 mH
Equivalent switching frequency	f_s	20 kHz
Split DC capacitor at HVDC side	C_{dcH}	C_{dcH} = 1 mF
I-MC^2		
RMS HVAC voltage	v_{ac}	216 Vrms
Equivalent switching frequency	f_s	40 kHz



(a) (b)

Fig. 10. SM$_{u1}$ experimental waveforms. (a) Overall waveforms. (b) Detailed waveforms.

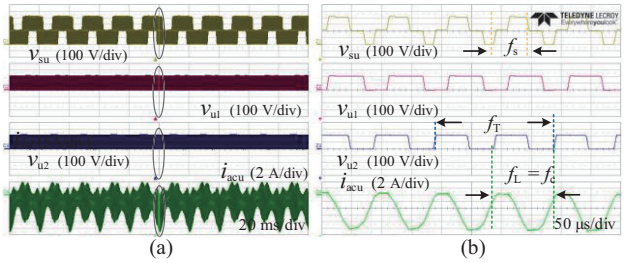


Fig. 11. Upper arm experimental waveforms. (a) Overall waveforms. (b) Detailed waveforms.

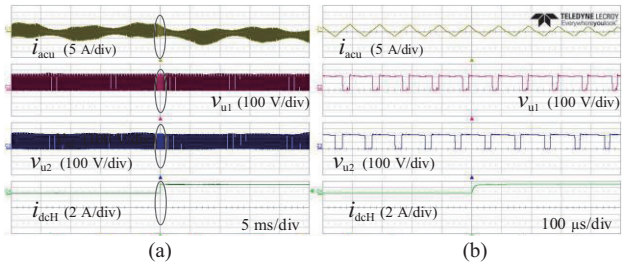


Fig. 12. Output voltage and current of upper and lower arm. (a) Overall waveforms. (b) Detailed waveforms.

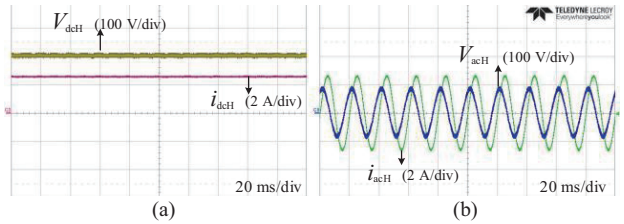


Fig. 13. Output voltage and current of I-MMC. (a) HVDC side waveforms. (b) HVAC side waveforms.

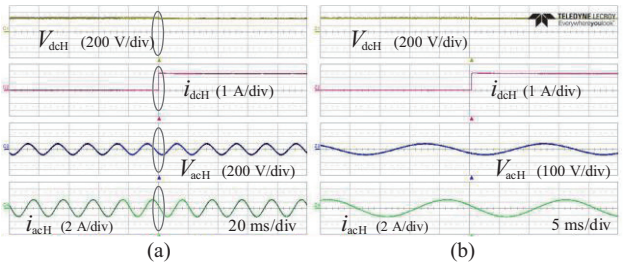


Fig. 14. Output voltage and current waveforms. (a) Overall waveforms. (b) Detailed waveforms.

ripple frequency f_L is same as the sawtooth carrier frequency f_c.

Fig. 13(a) shows the output voltage and current of the HVDC side and Fig. 13(b) shows the output waveforms of the HVAC side. At this time, the LVDC side voltage and current are 200 V and 6.88A. It shows that the proposed converter has high-quality output voltage, current and power.

Secondly, Fig. 14 shows the experimental transition waveforms under different DC load step conditions when the HVDC side load is changed from ∞ Ω to 160 Ω, keeping the HVAC load Z_{ac} = 160 + j48.4 Ω. Fig. 14(a) and (b) show the output voltage and current waveforms when the HVDC load is changed. From Fig. 14, it can be validated that power can flow across the LVDC side, HVDC side and HVAC side, freely.

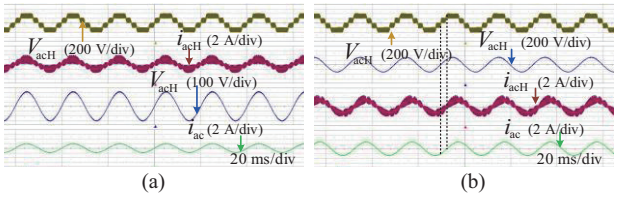


Fig. 15. HVAC side output voltage and current waveforms. (a) Pure active load. (b) Active plus reactive load.

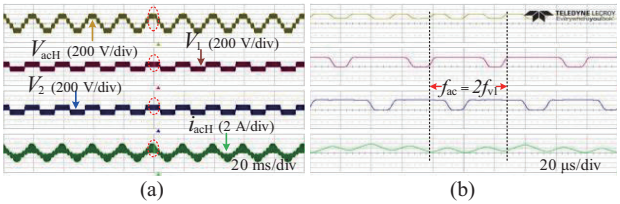


Fig. 16. Output voltage and current of HVAC and individual modules. (a) Overall waveforms. (b) Detailed waveforms.

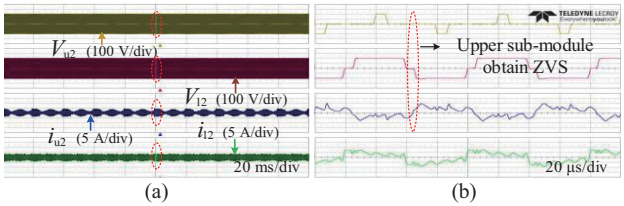


Fig. 17. Voltage and current at the secondary side of HFTs in an I-BC. (a) Overall waveforms. (b) Detailed waveforms.

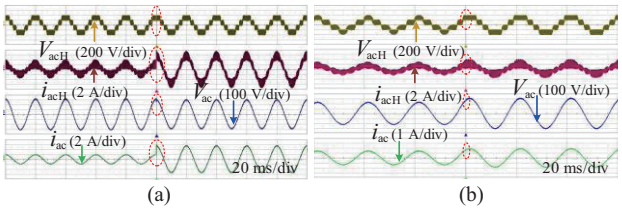


Fig. 18. Output voltage and current waveforms. (a) Load step down. (b) Changing AC duty cycle.

B. Experiment results of I-MC²

Figs. 15, 16 and 17 show the steady-state experimental waveforms when the AC duty cycle d_{am} = 0.8 and the delivered active-power conversion is about 1kW. Fig. 15(a) gives the HVAC side output voltage V_{ac} and current i_{ac} waveforms at R_{ac} = 160 Ω while Fig. 15(b) is at Z_{ac} = 160 + j145.2 Ω.

Fig. 16(a) and (b) shows the HVAC side output terminal voltage (V_i) of the two individual cascaded modules and the total output voltage (V_{acH}) and current (i_{acH}) waveforms. Fig. 17(a) and (b) show the secondary side voltage and current (V_{u2}, V_{l2}, i_{u2}, i_{l2}) waveforms of the high-frequency transformers in a single module. Notice that the upper sub-module and the lower sub-module are working in different modes and current i_{u2} in the upper sub-module changes to decline when V_{u2} = 0, so the switches that make i_{u2} change can obtain ZVS.

As shown in Fig. 18(a), when the HVAC side load steps down from 160 Ω to 54 Ω, the output current (i_{acH}, i_{ac}) achieves a new steady state while the output voltage (V_{acH}, V_{ac}) is unaffected

during the load transients. Fig. 18(b) shows the experimental waveforms when the AC duty cycle d_{am} is changed from 0.2 to 0.8, the output voltage and current (V_{acH}, V_{ac}, i_{acH}, i_{ac}) achieve a new steady state immediately as well.

All the above experimental results have demonstrated the feasibility and availability of the proposed two types of topologies. In the end, I-M^{2}C^2 can have a potentially important value for the hybrid DC and AC application in future power generation and transmission.

V. Conclusion

This paper has introduced the topologies of two categories of isolated modular multilevel cascaded converter (I-M^{2}C^2) and the relevant characteristics. Based on the high-frequency-link concept, the numerous individual DC-link capacitors at the high-voltage side are eliminated to increase power density and simplify control system. Thanks to the invariably positive voltage of the sub-modules' (SMs') port, there is no need for the bidirectional switches for active bridges, thus improving the system performance. A scaled-down laboratory single-phase system has verified the feasibility and availability of the new two types of I-M^{2}C^2 topologies.

References

[1] J. E. Huber and J. W. Kolar, "Solid-state transformers: On the origins and evolution of key concepts," *IEEE Ind. Electron. Mag*., vol. 10, no. 3, pp. 19–28, Sept. 2016.

[2] Jih-Sheng Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in *Conf. Rec. 2005 Ind. Appl. Conf, Fortieth IAS Annu. Meeting*, 2005, pp. 1893–1899.

[3] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 317–326, Jan. 2019.

[4] L. F. Costa, G. De Carne, G. Buticchi, and M. Liserre, "The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electron. Mag*., vol. 4, no. 2, pp. 56–57, Jun. 2017.

[5] J. E. Huber and J. W. Kolar, "Solid-state transformer: On the origins and evolution of key concepts," *IEEE Ind. Electron. Mag*., vol. 10, no. 3, pp. 19–28, Sept. 2016.

[6] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag*., vol. 10, no. 3, pp. 29–42, Sept. 2016.

[7] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z. X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Ind. Electron. Mag*., vol. 10, no. 2, pp. 46–58, Jun. 2016.

[8] K. Mainali et al., "A transformerless intelligent power substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electron. Mag*., vol. 2, no. 3, pp. 31–43, Sept. 2015.

[9] I. Syed and V. Khadkikar, "Replacing the grid interface transformer in wind energy conversion system with solid-state transformer," *IEEE Trans. Power Syst*., vol. 32, no. 3, pp. 2152–2160, May 2017.

[10] R. Gao, X. She, I. Husain, and A. Q. Huang, "Solid-state transformer interfaced permanent magnet wind turbine distributed generation system with power management functions," *IEEE Trans. Ind. Appl*., vol. 53, no. 4, pp. 3849–3861, July–Aug. 2017.

[11] C. Liu et al., "Cascade dual-boost/buck active-front-end converter for intelligent universal transformer," *IEEE Trans. Ind. Electron*., vol. 59, no. 12, pp. 4671–4680, Dec. 2012.

[12] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 1, no. 3, pp. 186–198, Sept. 2013.

[13] L. Wang, D. L. Zhang, Y. Wang, B. Wu, and H. S. Athab, "Power and voltage balance control of a novel three-phase solid-state transformer using multilevel cascaded H-bridge inverters for microgrid applications," *IEEE Trans. Power Electron*., vol. 31, no. 4, pp. 3289–3301, Apr. 2016.

[14] D. Wang, J. Tian, C. Mao, J. Lu, Y. Duan, J. Qiu, and H. Cai, "A 10-kV/400-V 500-kVA electronic power transformer," *IEEE Trans. Ind. Electron*., vol. 63, no. 11, pp. 6653–6663, Nov. 2016.

[15] J. E. Huber and J. W. Kolar, "Optimum number of cascaded cells for high-power medium-voltage AC-DC converters," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 5, no. 1, pp. 213–232, Mar. 2017.

[16] F. Briz, M. Lopez, A. Rodriguez, and M. Arias, "Modular power electronic transformers: modular multilevel converter versus cascaded H-bridge solutions", *IEEE Ind. Electron. Mag*., vol. 10, no. 4, pp. 6–19, Dec. 2016.

[17] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl*., vol. 50, no. 5, pp. 3569–3578, Sept.–Oct. 2014.

[18] C. Ren, X. Han, L. Wang, Y. Yang, W. Qin, and P. Wang, "High-performance three-phase PWM converter with a reduced DC-link capacitor under unbalanced AC voltage conditions," *IEEE Trans. Ind. Electron*., vol. 65, no. 2, pp. 1041–1050, Feb. 2018.

[19] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron*., vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[20] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl*., vol. 36, no. 5, pp. 1419–1429, Sept.–Oct. 2000.

[21] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron*., vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

Chuang Liu received the M.S. degree from Northeast Electric Power University, Jilin, China, in 2009, and the Ph.D. degree from Harbin Institute of Technology, Harbin, China, in 2013, both in Electrical Engineering. From 2010 to 2012, he was with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Ph.D. Student, supported by the Chinese Scholarship Council.

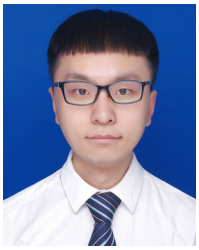
In 2013, he became an Associate Professor in the school of Electrical Engineering, Northeast Electric Power University, where, since 2016, he has been a Professor. His research interests include power-electronics-based ac and dc transformers for future hybrid ac-dc power grids, flexible operation and control of power grid based on ac-ac transformation, and power-electronics-based power system stability analysis and control.

Lianxin Wen was born in Fujian, China, in 1993. He received the B.S. degree from Northeast Electric Power University, Jilin, China, in 2016. He is currently working toward the M.S. degree in Electrical Engineering at Northeast Electric Power University, Jilin, China. His current research interests include renewable energy and distributed generation systems, high frequency isolated dc-ac inverters, and micro grid.

Dongfeng Yang received the M.S. degree from Northeast Electric Power University, Jilin, China, in 2005, and the Ph.D. degree from Harbin Institute of Technology, Harbin, China, in 2016. In 2016, he became an Associate Professor in the school of Electrical Engineering, Northeast Electric Power University. His current research interests include operation analysis of electric power system.

Hong Ying was born in Zhejiang, China, in 1972. He is a senior engineer in Zhejiang Huayun Clean Energy CO. LTD, Hangzhou, China. His current research interests include renewable energy and distributed generation systems.

Chao Liu was born in Heilongjiang, China, in 1994. He received the B.S. degree from Northeast Electric Power University, Jilin, China, in 2016. He is currently working toward the M.S. degree in Electrical Engineering at Northeast Electric Power University, Jilin, China. His current research interests include renewable energy and distributed generation systems, high frequency isolated dc-ac inverters, and micro grid.



Haoran Zhang was born in Heilongjiang, China, in 1995. He received the B.S. degree from Shandong Jianzhu University, Jinan, China, in 2017. He is currently working toward the M.S. degree in Electrical Engineering at Northeast Electric Power University, Jilin, China. His current research interests include renewable energy and distributed generation systems, high frequency isolated dc-ac inverters, and micro grid.

A Network-Based Approach for Modeling Resonant Capacitive Wireless Power Transfer Systems

Eli Abramov, Ilya Zeltser, and Mor Mordechai Peretz

***Abstract*—In this paper, a network-based approach to model capacitive wireless power transfer systems is introduced. The modeling methodology provides insights into the electrical cross-coupling relationships between input and output parameters of the capacitive power transfer (CPT) systems, including the effect of distance and alignment of the coupling plates. It is revealed that, regardless of the circuit complexity or matching network order, the model core can be reduced to a basic gyrator relationship with added coefficients when required, thus obtaining a compact, closed-form relationship between the input and output terminals. The model has been validated through rigorous simulations and experiments; all found to be in excellent agreement with the theoretical predictions under changes of the air-gap, and medium capacitance. To this end, an experimental CPT prototype that operates in the MHz range has been designed and implemented while the transmitter and receiver have been realized by four 170 mm × 170 mm copper plates. In addition, to provide better insight into the capacitive interface under different structures and distances and alignments, the capacitive coupler has been methodically examined through Finite Elements Analysis (FEA) tools Maxwell (Ansys). The results of the FEA have been utilized in the simulation platform to enhance the accuracy of the simulations, accounting for the variable capacitance under variations.**

***Index Terms*—Behavioral modeling, capacitive power transfer, capacitive coupling, gyrator, matching networks, two-port network.**

I. Introduction

OVER the last few years, capacitive power transfer (CPT) is a rapidly growing technology in the field of wireless power transfer (WPT) [1]–[7]. One of the more attractive advantages of capacitive-based WPT is the avoidance of undesired Eddy currents and electromagnetic interfaces (EMI) that comes with magnetic based WPT methods [8]–[10]. In addition to efficiency improvements, CPT systems are potentially with lower volume and construction complexity [1]–[7]. However, the power transfer capability and efficiency still depend on the distance and alignment between the transmitting and receiving sides, which is an inherent feature of near-field WPT systems [11], [12].

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E. Abramov and M. M. Peretz are with the Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 8410501, Israel (e-mail: eliab@post.bgu.ac.il; morp@bgu.ac.il).

I. Zeltser is with Power Electronics Department, Rafael Advanced Defense Systems Ltd, P. O. Box 2250, Haifa 31021, Israel (e-mail: ilyaz@rafael.co.il).

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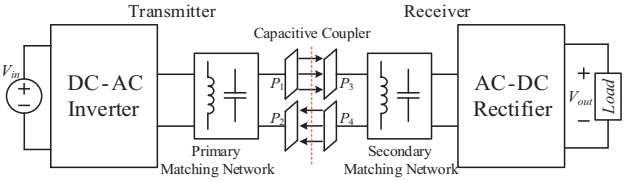

Fig. 1. Simplified diagram of capacitive WPT system.

Several explorations and remedies for extended range power transfer are covered in the literature [13]–[16], for general and capacitive power transfer. An important step in the development of both uniform and specific solutions for extended range WPT systems is a generalized description of the energy transfer mechanism. This requires description of the transfer medium, circuit behavior and their interaction. In particular, in case that active compensation is added, a description of the system's dynamic response is essential. On the topic of the magnetic field based WPT, there can be found several through circuit and system analyses, however, a generic behavioral model and modeling methodology for CPT has not been addressed to-date.

A simplified block diagram of a descriptive CPT system is shown in Fig. 1. In a similar way to magnetic field approaches, reactive networks on both the primary and secondary sides are used for impedance matching between the source and load characteristics [14]–[16]. To achieve degrees of freedom in terms of design, performance and overall input-output relationships in any WPT system, high-order matching networks are used [3], [16], [17]. Analysis of such high-order networks can be quite complex and tedious. As a result, the intricate interaction between the system parameters and characteristics may be overlooked or even missed. Several approaches have been employed to decipher the operation of high-order resonant structures such as analytical multivariable matrices manipulations, geometrical representations [18], [19], and averaging [20], [21]. Circuit derivation of CPT by superpositioning theorem [3], [5], [7], [22], provides clear closed-form expressions to the power delivery and other important relationships. However, since some approximations are involved, accurate overall description not always obtained, in particular for a description of the dynamic characteristics. Numerical simulations are also a strong tool to evaluate and characterize different resonant circuits, this approach, however, losses generality and may be time-consuming for cases that a time domain cycle-by-cycle simulation is carried out [23]–[25]. It would be extremely beneficial if a simple and unified generic

averaging behavioral modeling methodology for capacitive-based WPT systems is utilized.

The objective of this study is therefore to introduce a network-based approach to describe the behavior of capacitive WPT system, under variations of the source and the load circuits, coupling interface and matching networks. The modeling methodology results in a unified model for CPT that provides an insight to the cross-coupling relationship between the input and output parameters and enables to account for changes in distance and alignment of the coupling plates.

The rest of the paper is organized as follows: Following a brief survey of WPT matching structures, Section II details two-port network-based analysis. Section III delineates a case study of a network-based approach to analyze a CPT system. Model validation through various simulations including continuous capacitive medium variations is provided in Section IV. Experimental results of a capacitive WPT prototype are delineated in Section V. Section VI concludes the paper.

II. Review of Two-Port Representation of Matching Networks

A. Matching Network Configurations

Fig. 2 shows several popular matching networks that are mostly used in capacitive WPT systems [1]–[7]. A well-known and simple option is depicted in Fig. 2(a) in which a series inductance is connected to the coupling capacitance of the wireless medium forming a resonator [2]. By this, operation in the vicinity of the resonant frequency results in efficient power transfer to the load. However, a significant drawback of this configuration is that any change either in the capacitive medium or the load parameters, even the slightest, results in different operating point and a significant deterioration of the system ability to transfer power. This is somewhat alleviated by the configuration in Fig. 2(b), in which both the primary and secondary sides of the coupling element include series-parallel resonators (Double-Sided *LC*). Here, the operating frequency is near the matching network's resonance, and therefore the system is less sensitive variations in the coupling capacitance (due to distance or misalignment variations). At the cost of slightly higher component count, the power transfer capabilities are higher than series compensation, but still depends on the coupling for efficiency and delivered power [5], [7].The structure in Fig. 2(c) is a combination of the *LC* matching network with an additional series inductor on both sides of the system (Double-Sided *LCL*). By proper design of the inductors (L_P, L_{P1}, L_S, L_{S1}), this setup allows several degrees of freedom to adjust the power transfer of the system. However, as in the case of *LC* matching network, the power transfer capabilities of *LCL* structure is inversely proportional to the coupling capacitance [2], [4]. A more complex matching network is shown in Fig. 2(d). It consists of a larger number of reactive elements on both primary and secondary (Double-Sided *LCLC*). There, the coupling capacitance in this case does not directly influence the resonance of the matching networks, it is, however, still limits the amount of power transfer of the system, i.e., the lower the coupling capacitance is, proportionally lower the maximum power the system is able to transfer [3].

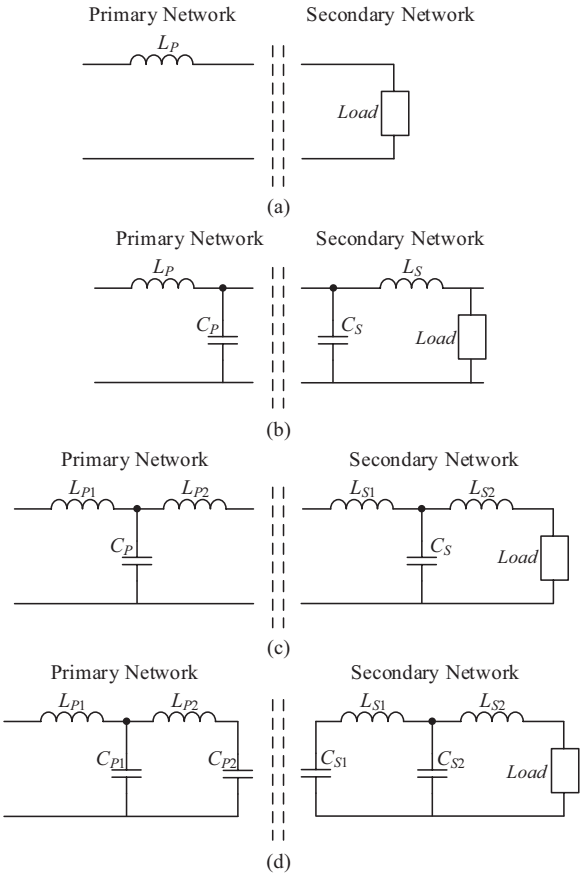

Fig. 2. Matching networks for capacitive WPT systems: (a) series *L*, (b) double-sided *LC*, (c) double-sided *LCL*, (d) double-sided *LCLC*.

B. Equivalent Representations of Matching Networks

Matching L-type structures such as a series inductor combined with a parallel capacitor (series-parallel *LC*, primary in Fig. 2(b)) and a parallel capacitor combined with a series inductor (parallel-series *LC*, secondary in Fig. 2(b)) can be described by a two-port network with gyrator characteristics [26]. A gyrator is a passive, lossless, linear two-port transformation network in which the output and input currents depend on the input and output voltages, respectively, with respect to its trans-conductance gain *G*. In circuit theory, gyrators are often used to reflect inductance using capacitance, impedance into admittance, and vice versa [27]–[30]. The input-output relationship of an ideal gyrator as a two-port network can be expressed as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & -G \\ G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{1}$$

In the context of the above discussion, voltage and current relationships of a series-parallel *LC* matching structure (Fig. 3(a)) can be derived as follows

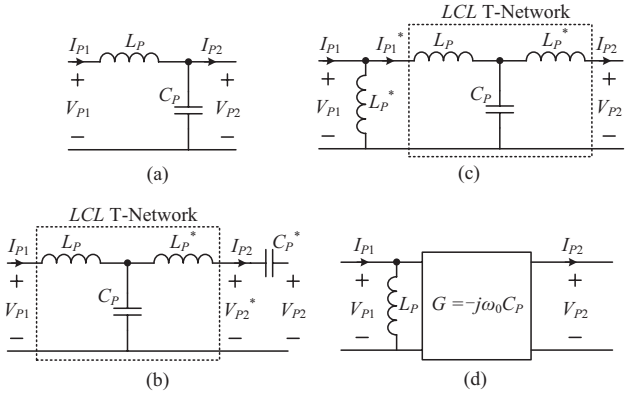

Fig. 3. Equivalent representations of series-parallel *LC* matching network. (a) L-type series-parallel resonant *LC* circuit. (b) Series resonator connected to the L-type circuit for T-type network arrangement. (c) Modified T-type series-parallel *LC* resonant circuit. (d) Two-port network with gyrator characteristics.

$$\begin{cases} V_{P1} = j\omega L_P I_{P1} + V_{P2} \\ V_{P2} = \dfrac{1}{j\omega C_P}(I_{P1} - I_{P2}) \end{cases} \Rightarrow \begin{cases} I_{P1} = \dfrac{(V_{P1} - V_{P2})}{j\omega L_P} \\ V_{P1} = j\omega L_P I_{P1} + \dfrac{1}{j\omega C_P}(I_{P1} - I_{P2}) \end{cases}. \tag{2}$$

Assuming operation at the resonant frequency, the currents I_{P1} and I_{P2} are given by

$$\begin{cases} I_{P1} = -j\omega_0 C_P (V_{P1} - V_{P2}) \\ I_{P2} = -j\omega_0 C_P V_{P1} \end{cases}; \quad \omega_0 L_P = \frac{1}{\omega_0 C_P}, \tag{3}$$

where ω_0 is the resonant angular frequency.

Employing few configurational modifications to the L-type network of Fig. 3(a), an equivalent representation can be obtained. As can be seen in Fig. 3(b), by addition of a series resonator (whereas $L_P^* = L_P$ and $C_P^* = C_P$) the network is transformed into a T-type one (L_P-C_P-L_P^*) with an output series capacitance C_P^*. The resultant voltage and current relationships have two-port gyrator characteristics as follows

$$\begin{aligned} V_{P1} &= j\omega_0 L_P I_{P1} + \frac{1}{j\omega_0 C_P}(I_{P1} - I_{P2}) = \frac{1}{-j\omega_0 C_P} I_{P2} \\ V_{P2}^* &= -j\omega_0 L_P I_{P2} + \frac{1}{j\omega_0 C_P}(I_{P1} - I_{P2}) = \frac{1}{j\omega_0 C_P} I_{P1} \end{aligned}, \tag{4}$$

and in a matrix representation, (4) can be written as

$$\begin{bmatrix} I_{P1} \\ I_{P2} \end{bmatrix} = \begin{bmatrix} 0 & \underbrace{j\omega_0 C_P}_{-G} \\ \underbrace{-j\omega_0 C_P}_{G} & 0 \end{bmatrix} \begin{bmatrix} V_{P1} \\ V_{P2}^* \end{bmatrix}, \tag{5}$$

where the trans-conductance gain is $G = -j\omega_0 C_P$. It should be noted that assuming operation in resonance, the addition of the series branch is an effectively short circuit and does not change the behavior of the circuit.

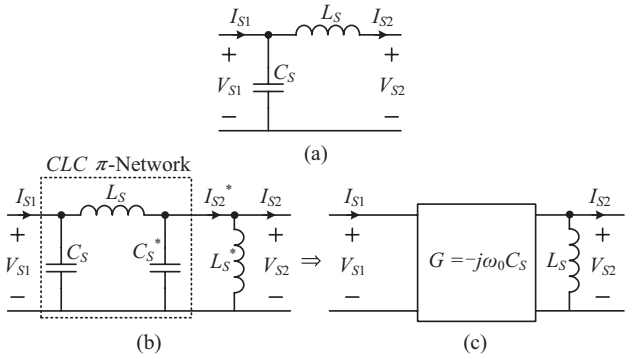

Fig. 4. Equivalent representations of parallel-series *LC* matching network. (a) L-type parallel-series resonant *LC* circuit. (b) Parallel resonator connected to the L-type circuit for π-type network arrangement. (c) Two-port network with gyrator characteristics.

Following the above observations, the series output capacitance C_P^* can be reflected to an input parallel inductance L_P^*, as shown in Fig. 3(c). Finally, the original L-type network can be represented as a gyrator element (Fig. 3(d)) with parallel input inductance L_p.

In analogy to the above practice for the series-parallel *LC* matching network, the parallel-series *LC* structure in Fig. 4(a) can also be defined by gyration ratio. This is facilitated by addition of a parallel resonator (whereas $L_P^* = L_P$ and $C_P^* = C_P$) as shown in Fig. 4(b). Similarly, to the case of the series branch, the parallel resonator is an effectively open circuit when operating at resonance and does not change the original characteristics of the circuit. The L-network is transformed into a π-type one (C_S-L_S-C_S^*) with parallel output inductor L_S^*. The parallel-series *LC* structure can be described as a gyrator element with parallel output inductor L_S as shown in Fig. 4(c).

III. Modeling and Analysis of Capacitive Wireless Power Transfer System

Following the derivations made in Section II, a capacitively-coupled power transfer system with double-sided *LC* matching networks is analyzed. The schematic diagram of the full system is shown in Fig. 5. This loosely-coupled configuration has been selected for the case study demonstration since it can be employed in a variety of medium power level CPT applications [1], [5], [7]. As can be seen in Fig. 5, the matching networks are a series-parallel *LC* circuit at the primary and a parallel-series *LC* at the secondary. The capacitive medium is modeled by a π-network, such that C_M is the equivalent mutual capacitance and C_{M1} and C_{M2} are the self-capacitances of the coupling plates [4], [5], [7], [31], [32]. The system is driven by a full-bridge inverter on the primary side, and the load is fed via a diode rectifier that is connected to the secondary's network. Due to the structural constraints of the coupling plates, as a general practice, it is assumed that the coupling capacitance C_M is significantly lower than the total parallel capacitance. Consequently, the driving frequency is near the matching networks' resonant frequency(i.e., $f_0 = 1/(2\pi\sqrt{L_p C_p}) = 1/(2\pi\sqrt{L_s C_s})$. Since high-$Q$ operation is naturally facilitated because of the high

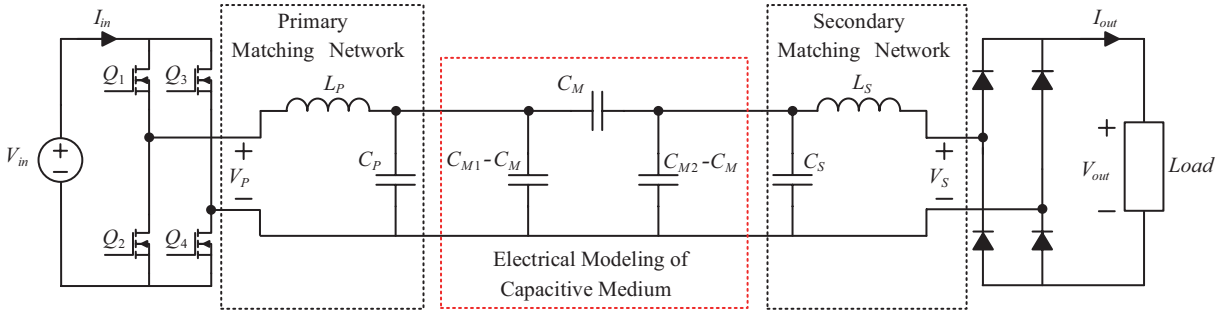

Fig. 5. Schematic diagram of a double-sided *LC* capacitive WPT system.

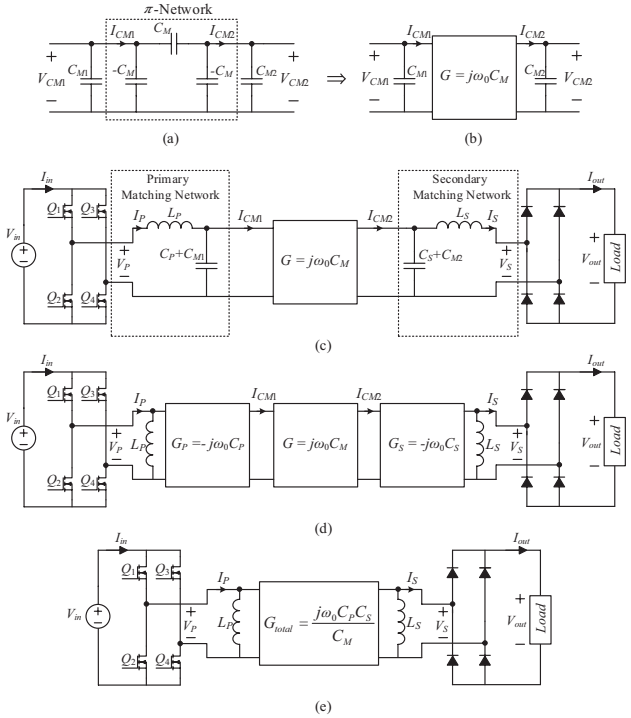

Fig. 6. Equivalent two-port network models of the analyzed double-sided *LC* capacitive WPT system. (a) Electrical equivalent model of four-plate capacitive medium. (b) Representation of the capacitive medium with a two-port network. (c) Representation of double-sided *LC* capacitive WPT system with a gyrator as the capacitive medium. (d) Equivalent circuit of double-sided *LC* capacitive WPT system with three series gyrators. (e) Equivalent simplified circuit of double-sided *LC* capacitive WPT system with a single gyrator.

output impedance of the primary's network, the currents as well as voltages of the reactive elements are virtually sinusoidal.

For the derivations of the model, the circuit of Fig. 5 is simplified by separating the parallel capacitances of the medium from the model self-capacitances, as shown in Fig. 6(a). This forms a π-network constructed by the mutual capacitance C_M, which can be analyzed similarly to the *CLC* π-matching network from Section II. This yields a gyrator element to represent the coupling behavior, as depicted in Fig. 6(b). In the context of the overall system, Fig. 5 is simplified as delineated in Fig. 6(c) (where $C_P >> C_{M1}$ and $C_S >> C_{M2}$). Assigning the network dualities that have been established earlier, the entire system is represented by three gyrators connected in series, as shown in Fig. 6(d). This is further reduced to a single gyrator,

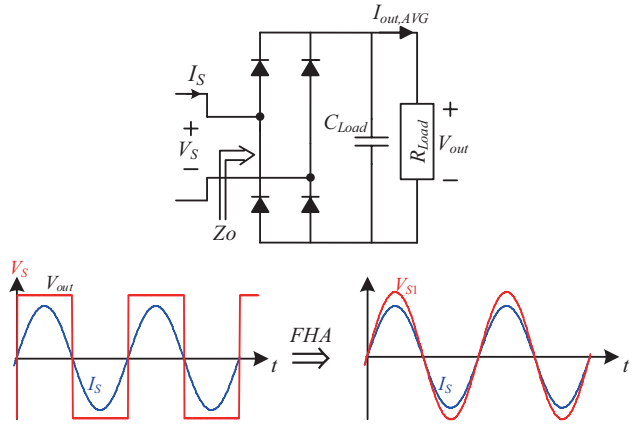

Fig. 7. Secondary side waveforms employing fundamental harmonic approximation.

as illustrated in Fig. 6(e), with total trans-conductance gain that can be expressed as

$$G_{total} = \frac{j\omega_0 C_P C_S}{C_M}. \tag{6}$$

The simplified circuit of the double-sided *LC* capacitive WTP system in Fig. 6(e) can now be analyzed as a two-port network with gyrator characteristics, such that the current-voltage relationships are expressed as follows:

$$\begin{aligned} &\text{(a) } I_P = \frac{V_P}{j\omega_0 L_P} - \frac{j\omega_0 C_P C_S}{C_M} V_S = -j\left(\frac{V_P}{\omega_0 L_P} + \frac{\omega_0 C_P C_S}{C_M} V_S\right) \\ &\text{(b) } I_S = -\frac{V_S}{j\omega_0 L_S} + \frac{j\omega_0 C_P C_S}{C_M} V_P = j\left(\frac{V_S}{\omega_0 L_S} + \frac{\omega_0 C_P C_S}{C_M} V_P\right) \end{aligned}, \tag{7}$$

where I_P, V_P, I_S, V_S are phasors. Assuming that the phase shift due the diode rectifier is negligible and that the load is a battery or capacitive filter with a long time constant, the current I_S and the voltage V_S are in phase. Hence, employing the fundamental harmonic approximation [33], the secondary's square wave voltage, V_S, can be represented by its fundamental component as depicted in Fig. 7. Therefore, the output of the system can be analyzed in a straightforward manner as follows

$$\begin{cases} I_S = \dfrac{\pi}{2} I_{out,AVG} \\ V_S = \dfrac{\pi}{4} V_{out} \end{cases} \Rightarrow Z_O = \frac{V_S}{I_S} = \frac{8}{\pi^2} R_{Load}, \tag{8}$$

substituting (8) into (7)-(b), and after some manipulations yields

$$\begin{aligned} \frac{V_S}{Z_O} &= j\frac{V_S}{\omega_0 L_S} + j\frac{\omega_0 C_P C_S}{C_M} V_P \\ \Rightarrow V_S &\left(\frac{1}{Z_O} + \frac{1}{j\omega_0 L_S} \right) = j\frac{\omega_0 C_P C_S}{C_M} V_P \end{aligned}, \quad (9)$$

from (9), primary-to-secondary voltage ratio can be expressed as follows:

$$\begin{aligned} \frac{V_P}{V_S} &= -\frac{C_M}{C_P}\left(1 + j\frac{\omega_0 L_S}{Z_O}\right) \\ \Rightarrow \angle(V_P, V_S) &= 180° - \text{arctg}\,(Q_S) = 90° \end{aligned}, \quad (10)$$

this can be further simplified by defining the secondary's quality factor, Q_S, as

$$Q_S = \frac{\sqrt{L_S/C_S}}{Z_O} = \frac{\omega_0 L_S}{Z_O} \Rightarrow \frac{V_P}{V_S} = -\frac{C_M}{C_P}(1 + jQ_S). \quad (11)$$

By substituting (11) into (7) and rearranging the equations, the current I_P can be rewritten as

$$\begin{aligned} I_P &= -\frac{C_M}{C_S}\left(\frac{1}{Z_O} + j\frac{C_P C_S - C_M^2}{\omega_0 L_S C_M^2} \right) V_S \\ &= -C_M \omega_0 \left(Q_S + j\left(\frac{1}{k_C} - 1 \right) \right) V_S, \end{aligned} \quad (12)$$

where k_C is the capacitive coupling coefficient and is defined as $k_C = (C_M/\sqrt{C_P C_S})$.

Following the same procedure, the current I_s can be also rewritten as

$$I_S = -\frac{C_P}{C_M}\frac{1}{Z_O + j\omega_0 L_S} V_P = -\frac{C_P}{C_M Z_O}\frac{1}{1 + jQ_S} V_P, \quad (13)$$

typically, the coupling coefficient k_C is relatively small ($k_C << 1$), and assuming $Q_S >> 1$ the system's current-voltage relationships can be simplified to generic expression as follows:

$$\begin{cases} |I_P| = \dfrac{C_M \omega_0}{k_C^2} |V_S| = \underbrace{\dfrac{\omega_0 C_P C_S}{C_M}}_{G_{total}} |V_S| \\ |I_S| = \dfrac{C_P}{C_M Z_O Q_S} |V_P| = \underbrace{\dfrac{\omega_0 C_P C_S}{C_M}}_{G_{total}} |V_P| \end{cases}, \quad (14)$$

it can be well noticed that the double-sided *LC* CPT system has the characteristics of a pure gyrator, which is in perfect agreement with the analysis given in [1].

The implication of this analysis is that the double-sided *LC* capacitive WPT system can be modeled as a voltage dependent current source, I_{out}, which represents the rectified current of I_s as illustrated in Fig. 8. Following the above analysis, the average value of the output current $I_{out,\,AVG}$ is found as a function of the trans-conductance gain and the input voltage V_{in} as follows:

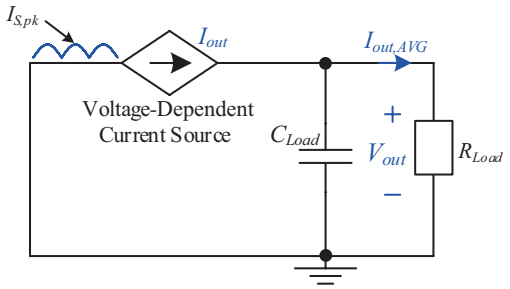

Fig. 8. Behavioral model of the double-sided *LC* capacitive WPT system for the output side.

$$\begin{aligned} V_P &= \frac{4}{\pi} V_{in} \\ \Rightarrow I_{out,\,AVG} &= \frac{8}{\pi^2}\frac{\omega_0 C_P C_S}{C_M} V_{in} \end{aligned}, \quad (15)$$

thus, the average output power $P_{out,AVG}$ can be expressed as

$$P_{out,\,AVG} = \left(\frac{8}{\pi^2}\frac{\omega_0 C_P C_S}{C_M} V_{in} \right)^2 \cdot R_{Load}. \quad (16)$$

From (15), it can be observed that for the double-sided *LC* CPT system the output current (as well as the output power) is inversely proportional to the mutual coupling capacitance C_M.

IV. Model Validation

A. Simulation Results

To verify the behavioral model, a simulation test-bench for the analyzed capacitive WPT system has been constructed in PSIM (PowerSim, Inc.). The input voltage is 30 V and the medium mutual capacitance $C_M = 4.5$ pF, at resonant frequency $f_0 \approx 1.55$ MHz for a load resistance of $R_{Load} = 15\ \Omega$ and output capacitor $C_{Load} = 200$ µF. First set of simulations has been carried out for symmetrical matching parameters: $L_P = L_S = 67$ µH, $C_P = C_S = 156$ pF. The simulation results of the currents and voltages of the primary and secondary sides are shown in Fig. 9(a) and (b), respectively, whereas the dashed lines show the behavioral model predictions. The obtained peak values of the currents are in good agreement with the theoretical predictions in (14), which further implies that the average output current, $I_{out,AVG}$, is as expected from (15).

The second set of simulations has been carried out for asymmetrical matching parameters: $L_P = 67$ µH, $C_P = 156$ pF for the primary side, and $L_S = 90$ µH, $C_S = 116$ pF for the secondary side. Fig. 10 depicts simulation waveforms of the currents and

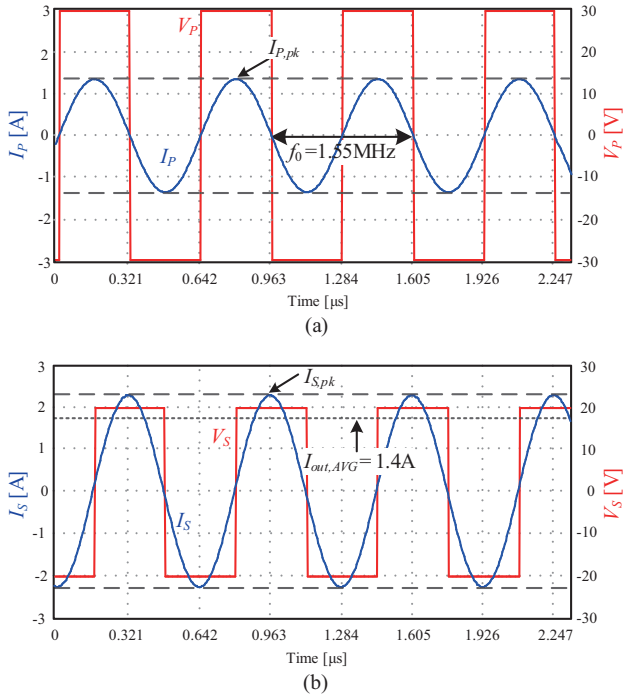

Fig. 9. Simulated waveforms of the currents and voltages for symmetrical matching parameters (dashed lines are the behavioral model predictions): (a) primary, (b) secondary.

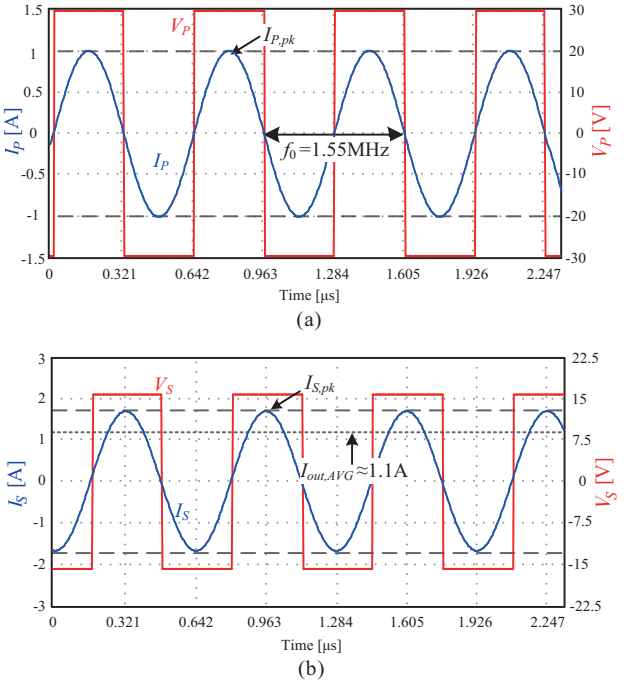

Fig. 10. Currents and voltages simulation results for asymmetrical matching parameters (dashed lines are the behavioral model predictions): (a) primary, (b) secondary.

TABLE I
SIMULATION TEST-BENCHES VALUES AND PARAMETERS

Parameter	Fig. 9	Fig. 10
Input voltage V_{in}	30 V	30 V
Load resistance	15 Ω	15 Ω
Output capacitor	200 μF	200 μF
C_M	4.5 pF	4.5 pF
Inductors L_P and L_S	67 μH	67 μH, 90 μH
Capacitors C_P and C_S	156 pF	156 pF, 116 pF
Resonant frequency f_0	1.55 MHz	1.55 MHz
$I_{out,AVG}$	1.4 A	1.1 A

voltages of the primary and secondary. As can be seen, the obtained results match the model predictions. It can also be noticed that the resulting output current is lower than that in the symmetrical case shown in Fig. 9. This is due to the lower trans-conductance gain in the case with a lower value of C_S. Table I summarizes the operating conditions and parameters for Figs. 9 and 10.

In addition, the calculated results for the average output current of the asymmetrical case are plotted against the results obtained from the simulation. These are depicted in Fig. 11, where Fig. 11(a) shows the current as a function of the input voltage, and Fig. 11(b) shows the current as a function of the coupling capacitances. A very good agreement is obtained throughout these simulations. As can be seen in Fig. 11(b), as predicted by the model in (15), the output current is inversely proportional to the mutual coupling capacitance C_M. Therefore, the output power will follow a similar trend.

In order to evaluate and predict the performance of a double-sided *LC* system for medium variations (distance/misalignment), a simulation test-bench with variable capacitors has been constructed as shown in Fig. 12. There, for convenience, the capacitive medium is illustrated by variable capacitor symbols. The methodology to model a continuous-time, variable inductance as described previously in [34], [35] has been employed and adapted to describe varying capacitance in this study (detailed implementation of continuous-time, variable, capacitor is beyond the scope of this paper and are provided subsequent publication).

Simulations have been carried out under nominal operating conditions and matching networks that are identical to those of the asymmetrical case study, whereas the initial coupling capacitance is 5 pF. Fig. 13(a) shows the result of the average value of I_{out} for a 2 pF variation of the mutual capacitance, such that the final coupling capacitance is C_M= 7 pF. The solid red line shows the simulation result, whereas the dashed blue markers show the behavioral model outcome. It can be observed that the results of the cycle-by-cycle simulation and behavioral model are in very good agreement. It can be further noticed that when C_M increases, the output current decreases as expected from the theoretical analysis. Fig. 13(b) shows the output current for a medium step-down variation of 2 pF, such that the final coupling capacitance is C_M= 3 pF. The output current settles on approximately 1.7 A for both the model and cycle-by-cycle simulation, which suits well the theoretical predictions as shown in detail in Fig. 11(b).

B. Capacitive Coupler Design

To facilitate reliable estimation of the capacitive coupler

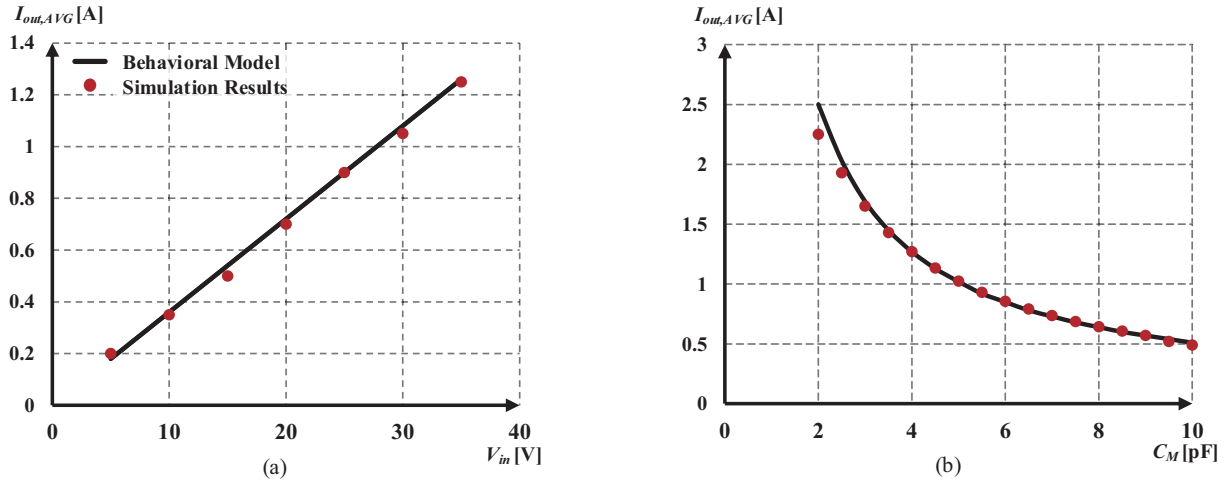

Fig. 11. Behavioral model and simulated average output current, $I_{out,AVG}$, curves an asymmetrical setup. (a) As a function of the input voltage V_{in}. (b) As a function of the mutual coupling capacitance C_M.

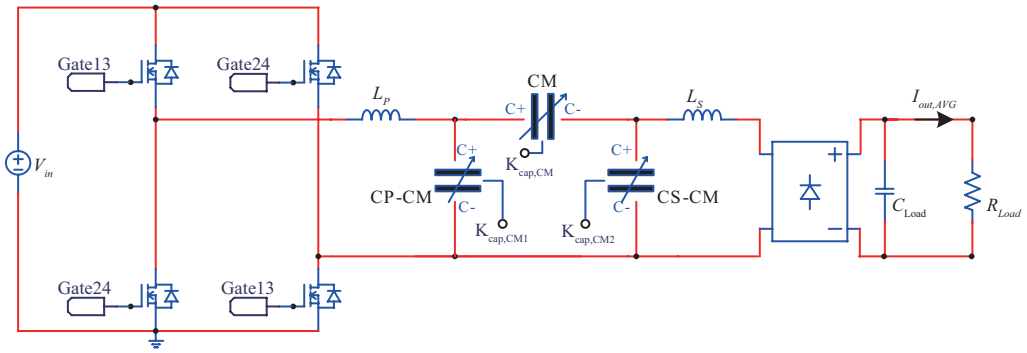

Fig. 12. Schematic simulation test-bench of the WPT system with variable capacitor symbol illustrations for the capacitive medium.

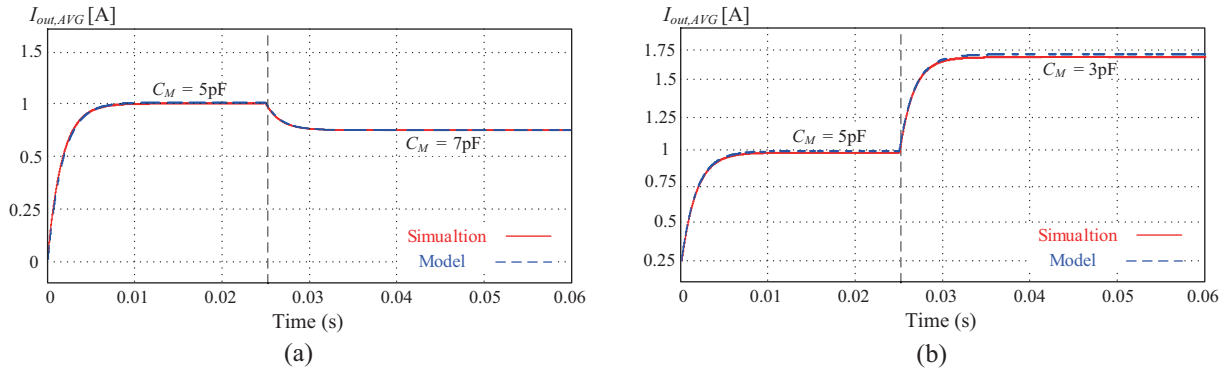

Fig. 13. Average output current for capacitive medium variations with initial mutual capacitance C_M = 5 pF. (a) Step-up of 2 pF. (b) Step-down of 2 pF.

for the experimental measurements, estimation of the plates capacitances has been carried out by Maxwell (Ansys) Finite Element Analysis (FEA) tool (Fig. 14(a)). Rigorous simulation procedure over various air-gaps has been carried out to determine the mutual capacitance, C_M, for the symmetrical copper-based capacitive coupler, whereas each plate is 170 mm × 170 mm. The results for the mutual coupling capacitance, C_M, and for the coupling coefficient, k_C, are shown in Fig. 14(b) and (c), respectively. It can be observed that the coupling coefficient is $<<1$ over the entire range, while C_M decreases by nearly four times at an air-gap of 70 mm.

It should be noted that typically, FEA are generated by defining the geometry of the element and by setting the boundary conditions, in the context of the capacitive coupler these are four symmetrical copper plates and voltage excitations to the plates. The mutual capacitances of the coupling plates have been calculated based on the equations in [4], [5] and the coupling coefficient, k_C, has been calculated by $C_M/\sqrt{C_P C_S}$.

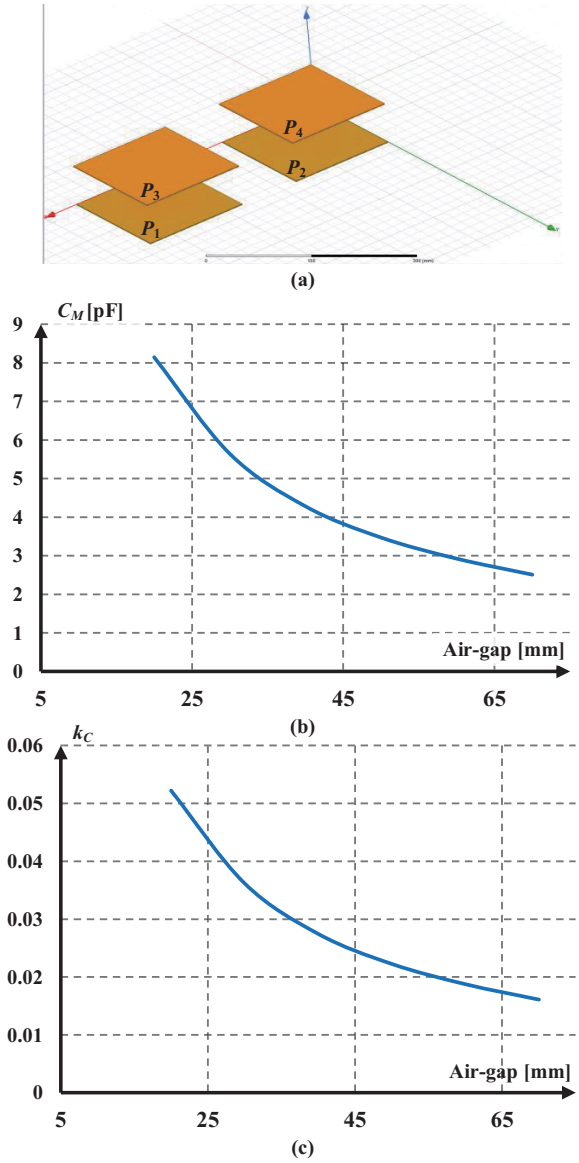

Fig. 14. Maxwell (Ansys software) simulation test-bench for the capacitive coupler design.

V. Experimental Verification

Based on the above analysis and simulations an experimental double-sided *LC* capacitive WPT prototype (Fig. 15), has been designed and examined. Since the coupling plates have been designed symmetrically, the matching networks have been also designed to be symmetrical, with $L_P = L_S \approx 67$ µH and $C_P = C_S = 156$ pF. The gate drive signals of the full-bridge inverter were generated with a Cyclone IV FPGA [36] at an operating frequency slightly above the resonance $f_0 \approx 1.558$ MHz guaranteeing soft-switching operation. The full-bridge inverter has been implemented with GaN modules operable at several MHz [37]. To reduce the limitations due to magnetic and skin-effect losses in the MHz range [38], [39], the matching inductors L_p and L_s have been constructed with AWG 48 litz

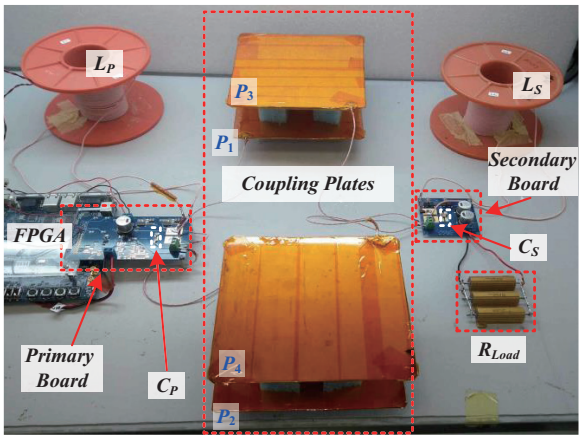

Fig. 15. Experimental setup of a capacitive WPT prototype.

TABLE II
Experimental Prototype Values and Parameters

Parameter	Value/Type
Input voltage V_{in}	30 V
$I_{out,AVG}$	up to 1.6 A
Load resistance R_{Load}	~15 Ω
Coupling plates	170 mm × 170 mm
C_M /air-gaps	2.5 pF-8 pF / 20 mm-70 mm
Full-bridge transistors	LMG5200, 80 V, 15 mΩ, Dual
Rectifier diodes	5 A/200 V, VSSC520S -M3
Inductors L_P and L_S	~67 µH
Capacitors C_P and C_S	156 pF, AVX MLLC 5 kV
Output capacitor C_{Load}	200 µF, EEV- FK2A101M
Resonant frequency f_0	~1.558 MHz

wire wrapped on an air-core. High-voltage multilayer SMD ceramic capacitors have been used in parallel to form the desired matching capacitors C_P and C_S. The overall operating conditions and parameters of the experimental prototype are summarized in Table II.

Fig. 16 shows experimental waveforms of the system for an air-gap of 30 mm (corresponds to $C_M \approx 4.5$ pF approximately), whereas the input voltage $V_{in} = 30$ V and the load resistance $R_{Load} \approx 15$ Ω. Fig. 16(a) shows the primary waveforms, as can be seen V_P toggles between −30 V to 30 V and the peak value of the sinusoidal current I_P is ~1.22 A. The current at the secondary, I_s, is shown in Fig. 16(b), taking into consideration that some losses are introduced throughout the experiments, the obtained peak value (1.8 A) as well as the resulting average value (~1.1 A) are in the vicinity of the simulation results shown in Section IV, and the system efficiency is 75%. Fig. 17 shows experimental waveforms for an air-gap of 60 mm which corresponds to C_M of 3 pF approximately, again, the measured output voltage and current are well predicted by both the behavioral model and simulations.

To further verify the strength of the behavioral model, the average output current has been measured for various input voltages, for a constant air-gap of 30 mm, the results are summarized in Fig. 18(a). The experimental measurements tightly follow the results obtained by the simulations as well as the model predictions. It can be noticed that the output current

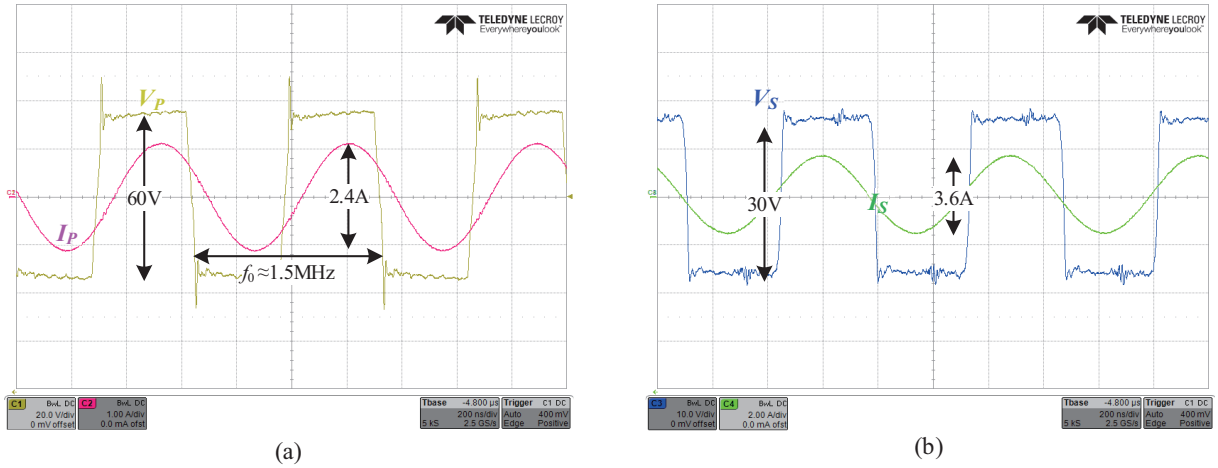

Fig. 16. Experimental waveforms with operating conditions: V_{in} = 30 V, R_{Load} = 15 Ω, coupling capacitance C_M ≈ 4.5 pF. (a) Primary side V_p: 20 V/div, I_P: 1 A/div, (b) Secondary side V_S: 10 V/div, I_S: 2 A/div, Time scale: 200 ns/div.

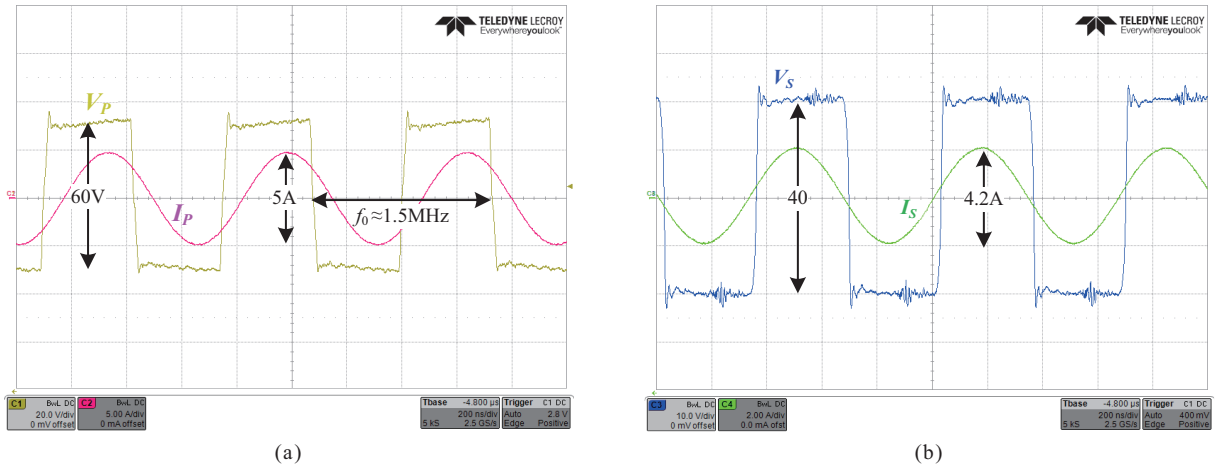

Fig. 17. Experimental waveforms with conditions: V_{in} = 30 V, R_{Load} = 15 Ω, coupling capacitance C_M ≈ 3 pF, (a)Primary side V_P: 20 V/div, I_P: 5 A/div, (b) Secondary side V_S: 10 V/div, I_S: 2 A/div. Time scale: 200 ns/div.

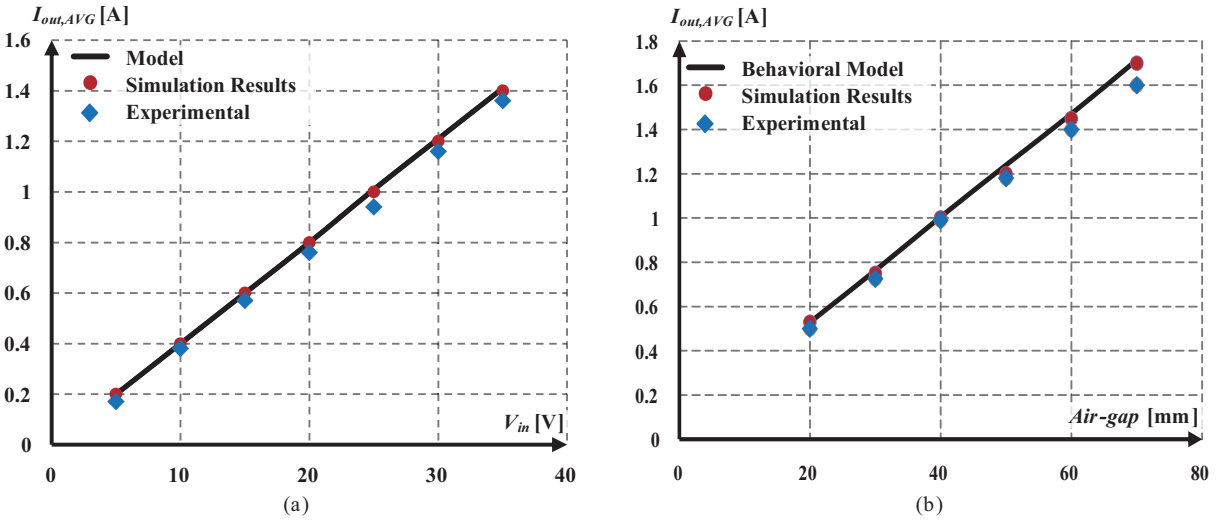

Fig. 18. Average output current, I_{outAVG}, curves: (a) as a function of the input voltage V_{in}, for 30 mm air-gap; (b) as a function of the air-gaps (coupling capacitance C_M), for V_{in} = 30 V.

(as well as the output power) increases with the input voltage, as predicted from the gyrator current-voltage relationships obtained in Section III. Fig. 18(b) depicts the output current comparison between the experimental, simulated and behavioral model for various air-gaps between 20 mm and 70 mm, thus demonstrating variations in distance/misalignment (while V_{in} = 30 V). This way, the inversely proportional behavior between the capacitive coupling and the output current is well validated by the experimental measurements.

VI. Conclusions

A two-port network-based modeling approach for capacitive WPT systems has been presented. Based on the modeling approach, the behavior of resonant-operating capacitive WPT system (or in the vicinity of resonant operation) can be analyzed and described for different system variations such as capacitive coupling interface, resonant frequency and matching networks components. The modeling method provides an insight to the effects of the parameters on the system behavior, the cross-coupling relationships between transmitting and receiving sides, and sourcing features based on the operation mode and settings. The simplicity and generality of the gyrator model as an energy transfer element offers an efficient closed-form alternative to complex analytical approaches or tedious numerical simulations. An experimental CPT prototype operating in the MHz range has been constructed. The prototype has been evaluated for various air-gaps up to 70 mm and 45 W output power delivery. The experimental case-study confirmed the theoretical predictions of the model with an excellent agreement between the analytical derivations, simulations, and experimental results.

Acknowledgment

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References

[1] E. Abramov and M. M. Peretz, "Modeling and analysis of capacitive wireless power transfer systems: a network approach", in *Proc. IEEE Int. Power Electron. Appli. Conf. Expo. (PEAC)*, Nov. 2018, pp. 1−6.

[2] M. P. Theodoridis, "Effective capacitive power transfer," *IEEE Trans. Power Electron*., vol. 27, no. 12, pp. 4906–4913, Dec. 2012.

[3] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A double-sided LCLC compensated capacitive power transfer system for electric vehicle charging," *IEEE Trans. Power Electron*., vol. 30, no. 11, pp. 6011–6014, Jun. 2015.

[4] H. Zhang, F. Lu, H. Hofmann, W. Liu, and C. C. Mi, "A four-plate compact capacitive coupler design and LCL-compensated topology for capacitive power transfer in electric vehicle charging application," *IEEE Trans. Power Electron*., vol. 31, no. 12, pp. 8541–8551, Dec. 2016.

[5] F. Lu, H. Zhang, H. Hofmann, C. Mi, "A loosely coupled capacitive power transfer system with LC compensation circuit topology," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, pp. 1–5, 2016.

[6] F. Lu, H. Zhang, C. Mi, "A two-plate capacitive wireless power transfer system for electric vehicle charging applications," *IEEE Trans. Power Electron*, vol. 33, no. 2, pp. 946–969, Aug. 2017.

[7] F. Lu, H. Zhang, H. Hofmann, and C. Mi, "A double-sided LC compensation circuit for loosely-coupled capacitive power transfer," *IEEE Trans. Power Electron*., vol. 33, no. 2, pp. 1633–1643, Feb. 2017.

[8] T. Imura and Y. Hori, "Maximizing air gap and efficiency of magnetic resonant coupling for wireless power transfer using equivalent circuit and Neumann formula," *IEEE Trans. Ind. Electron*., vol. 58, no. 10, pp. 4746– 4752, Oct. 2011.

[9] J. Sallan, J. L. Villa, A. Llombart, and J. F. Sanz, "Optimal design of ICPT systems applied to electric vehicle battery charge," *IEEE Trans. Ind. Electron*., vol. 56, no. 6, pp. 2140–2149, Jun. 2009.

[10] S. Jaegue *et al*., "Design and implementation of shaped magnetic resonance-based wireless power transfer system for roadway-powered moving electric vehicles," *IEEE Trans. Ind. Electron*., vol. 61, no. 3, pp. 1179–1192, Mar. 2014.

[11] K. Wu, D. Choudhury, and H. Matsumoto, "Wireless power transmission, technology, and applications" in *Proc. IEEE*, Vol. 101, no.6, pp. 1271–1275, June 2013.

[12] L. Collins, "Cut the cord," *IET Journals & Magazines*., vol. 5, no. 6, pp. 42–46, Jan.–Dec. 2007.

[13] F. Lu, H. Zhang, H. Hofmann, C. Mi, "An inductive and capacitive integrated coupler and its LCL compensation circuit design for wireless power transfer," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4903–4913, Oct. 2017.

[14] Y. Lim, H. Tang, S. Lim, J. Park, "An adaptive impedance-matching network based on a novel capacitor matrix for wireless power transfer," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4403−4413, August 2014.

[15] T.C. Beh, M. Kato, T. Imura, S. Oh and Y. Hori, "Automated impedance matching system for robust wireless power transfer via magnetic resonance coupling," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3689−3698, September 2013.

[16] W. Zhang and C. Mi, "Compensation topologies for high power wireless power transfer systems," *IEEE Trans. Veh. Technol.*, vol. 65, no.6, pp. 4768−4778, July 2015.

[17] A. Kumar, S. Sinha, A. Sepahvand, K. K. Afridi, "Improved design optimization for high-efficiency matching networks," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 37−50, Jan. 2018.

[18] A. Witulski and R. W. Erickson, "Extension of state-space averaging to resonant switches and beyond," *IEEE Trans. Power Electron*., vol. 5, no. 1, pp. 98–109, Jan. 1990.

[19] H. Hao, G. A. Covic, and J. T. Boys, "An approximate dynamic model of LCL-T-based inductive power transfer power supplies," *IEEE Trans. Power Electron*., vol. 29, no. 10, pp. 5554–5567, Oct. 2014.

[20] V. Vorperian, R. Tymerski, and F. C. Lee, "Equivalent circuit models for resonant and PWM switches," *IEEE Trans. Power Electron*., vol. 4, no. 2, pp. 205–214, Apr. 1989.

[21] D. Maksimovic and S. Cuk, "A unified analysis of PWM converters in discontinuous modes," *IEEE Trans. Power Electron*., vol. 6, no. 3, pp. 476–490, Jul. 1991.

[22] J. Lu, A. Kumar, K. K. Afridi, "A step-superposition based analysis approach to modeling resonant converters," *IEEE Trans. Power Electron*., vol. 33, no. 8, pp. 7148−7165, Aug. 2018.

[23] C. J. Anderson and J. A. Lyle, "Technique for evaluating system performance using Q in numerical simulation exhibiting inter symbol interference," *Electron. Lett*., vol. 30, pp. 71–72, 1994.

[24] L. Chen, S. Liu, Y. Zhou, and T. Cui, "An optimizable circuit structure for high-efficiency wireless power transfer," *IEEE Trans. Ind. Electron*., vol. 60, no. 1, pp. 339–349, Jan. 2013.

[25] B. Wang, W. Yerazunis, and K. H. Teo, "Wireless power transfer: Metamaterials and array of coupled resonators," in *Proc. IEEE*, vol. 101, no. 6, pp. 1359–1368, Jun. 2013.

[26] Y. H. Sohn, B. H. Choi, G. H. Cho, and C. T. Rim, "Gyrator-based analysis of resonant circuits in inductive power transfer systems," *IEEE Trans. Power Electron,* vol. 31, no. 10, pp. 6824-6843, Oct. 2016.

[27] A. Cid-Pastor, L.Martinez-Salamero, C. Alonso, R. Leyva, and S. Singer, "Paralleling DC–DC switching converters by means of power gyrators," *IEEE Trans. Power Electron*., vol. 22, no. 6, pp. 2444–2453, Nov. 2007.

[28] D. C. Hamill, "Lumped equivalent circuits of magnetic components: The gyrator–capacitor approach," *IEEE Trans. Power Electron*., vol. 8, no. 2, pp. 97–103, Apr. 1993.

[29] S. Singer, "Loss-free gyrator realization," *IEEE Trans. Circuits and Syst*, vol. 35, no. 1, pp. 26−34, Jan. 1988.

[30] S. Singer, "Gyrators application in power processing circuits," *IEEE Trans. Ind. Electron*., vol. IE-34, no. 3, pp. 313–318, Aug. 1987.

[31] C. Liu, A.P. Hu, and M. Budhia, "A generalized coupling model for capacitive power transfer systems," in *Proc. 36th Annu. Conf. IEEE Ind.*

Electron. Society, Glendale, AZ, pp.274–279, Nov. 2010.

[32] L. Huang, A. P. Hu, A. K. Swain, and Y. Su, "Accurate steady-state modeling of capacitive-coupling interface of capacitive power transfer systems with cross-coupling," *Wireless Power Transfer*, vol. 3, no. 1, pp. 53–62, 2016.

[33] R.L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174−182, Apr. 1988.

[34] S. Cheon, Y. H. Kim, S. Y. Kang, M. L. Lee, J. M. Lee, and T. Zyung, "Circuit-model-based analysis of a wireless energy-transfer system via coupled magnetic resonances," *IEEE Trans. Ind. Electron*., vol. 58, no. 7, pp. 2906–2914, Jul. 2011.

[35] S. Ben-Yaakov and M.M. Peretz, "Simulation bits: A SPICE behavioral model of non-linear inductors," *IEEE Power Electron. Soc. Newslett*., vol. 15, no. 4, pp. 9–10, 4th Quarter 2003.

[36] *DE2 Development and Education Board User Manual*, Altera Corporation, 2006.

[37] Texas Instrument: 'LMG5200 80-V, 10-A GaN Half-Bridge Power Stage' [Online]. Available: http://www.ti.com/lit/ds/symlink/lmg5200.pdf, accessed March 2017.

[38] J. Craninckx and M. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, np. 5, pp. 736–744, May 1997.

[39] M. Bartoli, N. Noferi, A. Reatti, and M. Kazimierczuk, "Modeling litzwire winding losses in high-frequency power inductors," in *Proc. IEEE Power Electroni. Specialists Conf*., Jun. 23–27, 1996, pp. 1690–1696.

Eli Abramov received the B.Sc. degree in Electrical and Electronics Engineering from the Samy Shamoon College of Engineering, Beer-Sheva, Israel, in 2013, and the M.Sc degree in electrical and computer engineering from Ben-Gurion University, Israel in 2016. He is currently working toward the Ph.D. degree in electrical and computer engineering at the Center for Power Electronics and Mixed-Signal IC, at Ben-Gurion University of the Negev, Israel.

His research interests include power and analog IC, mixed-signal integration for power management systems, power systems on-chip, modeling and control of wireless power transfer systems.

Ilya Zeltser received the B.Sc., M.Sc. and Ph. D. degrees in Electrical and Computer Engineering at the Ben-Gurion University of the Negev, Beer Sheva, Israel, in the years 1995, 1998 and 2010 respectively.

He was a co-founder of Green Power Technologies Ltd., Israel, where he served as VP R&D during the years 2000−2006. Since 2010, his research activities are being conducted at Rafael Advanced Defense systems Ltd., Israel, where he also held several managerial positions. He currently serves as a Divisional System Engineer.

His current research interests include dc-dc converters, chargers, pulsed power modulators, modeling, renewable energy and wireless power transfer systems.

Mor Mordechai Peretz was born in Beer-Sheva, Israel, in 1979. He received the B.Tech. degree in Electrical Engineering from the Negev Academic College of Engineering, Beer-Sheva, in 2003, and the M.Sc. and Ph.D. degrees in electrical and computer engineering from Ben-Gurion University, Negev, Israel, in 2005 and 2010, respectively.

From 2010 to 2012, he was a Postdoctoral Fellow at the Laboratory for Power Management and Integrated SMPS, University of Toronto, Canada. In 2012, he joined the Department of Electrical and Computer Engineering, Ben-Gurion University, where he is currently the director of the Center for Power Electronics and Mixed-Signal IC. Prof. Peretz serves as an associate editor of the *IEEE Transactions on Power Electronics* and the *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

His research interests include digital and smart control methods for efficient energy processing, SMPS miniaturization, mixed-signal IC design of SMPS, modeling and computer aided design, applications of nonlinear magnetics and renewable energy systems.

Single-Stage Isolated Electrolytic Capacitor-Less EV Onboard Charger With Power Decoupling

Ali Tausif, Hoyoung Jung, and Sewan Choi

***Abstract*—In this paper, a new single-stage single-phase isolated AC-DC converter derived from a differential boost AC-DC converter is proposed. This converter eliminates the need to use the bulky electrolytic capacitor from the system and at the same time provides DC charging by employing the AC Power Decoupling waveform control method, effectively addressing the power density and reliability related issues commonly associated with the bulky electrolytic capacitor. As half of the switches of this converter act as synchronous rectifier during half grid cycle they are inherently ZVS Turned On while the remaining switches achieve ZVS Turn On as they act as synchronous rectifier during other half grid cycle. However, all diodes at the secondary side achieve ZCS Turn Off during the entire line cycle. A conventional controller is implemented for output voltage regulation and PFC control whereas a power decoupling controller is added to compensate second harmonic ripple power. Besides, an interleaving technique is applied to provide high-frequency links for transformers' connection while at the same time increasing the power range and effectively reducing the size of the input filter. Finally, the operating principle of the converter is validated through simulation, and the experimental results are provided.**

***Index Terms*—Current-fed isolated AC-DC, differential converter, electrolytic capacitor-less, onboard battery charger, power decoupling, single-stage system.**

I. Introduction

THE onboard battery chargers (OBCs) are crucial power electronic components in plug-in hybrid electric vehicles (PHEV) and battery electric vehicles (BEV) as they receive power from the grid, convert it to suitable DC voltage, and charges vehicle's battery. Introduction to wideband gap devices such as SiC and GaN in the automotive sector has already revolutionized the electric vehicles power electronics as these devices can operate at high switching frequency with minimal switching and conduction losses which have greatly enhanced the efficiency and power density requirement of the system [1]–[3]. Since OBCs are installed inside vehicles, therefore it is mandatory to develop a charger that should be compact, highly efficient and reliable. According to DOE technical targets 2022, OBC should have an efficiency above 94% and a power density higher than 0.943 kW/L [4]. Much research is going on in developing new topologies that are reliable and can address the issues of the existing topologies cost-effectively.

A conventional approach for EV OBC is a two-stage structure which consists of a front end AC-DC boost PFC converter followed by an isolated DC-DC converter for output regulation [5]. The main advantage of this OBC is its simple structure and control implementation whereas the downside of this is its low efficiency because of its hard switched front end AC-DC converter and due to the existence of diode bridge at grid side it experiences high conduction loss. Besides, a large electrolytic capacitor is used as the DC link capacitor to smooth out the DC voltage which reduces the power density and lifetime of the converter.

Another variation of this topology is to use interleaved boost PFC as an AC-DC converter and full-bridge phase shift converter as a DC-DC converter [6]. The significant improvement is the reduction of switch current rating as the current is divided into half due to interleaving.

It must be noted that in the two-stage topologies explained above, the conduction loss due to slow diode bridge is very significant. To minimize this loss, a bridgeless AC-DC converter is employed as a front end PFC stage followed by DC-DC full-bridge converter [7]. This converter significantly minimizes the conduction losses associated with the diode bridge. However, this bridgeless AC-DC converter is hard switched in nature which limits the increase in switching frequency. Moreover, the capacitance requirement for DC link capacitor is usually high as 2nd harmonic ripple associated with the single-phase system needs to be absorbed to get smooth DC current. So, a bulky electrolytic capacitor is a must which affects the lifetime and power density of the converter.

A reasonable method is also proposed in [7] which solves this constraint of using electrolytic capacitor by replacing it with a film capacitor and allowing 2nd harmonic voltage swing in the DC link capacitor voltage. However, due to this voltage swing, the voltage rating of the switches is increased. Moreover, switching loss associated with AC-DC bridgeless converter still poses restriction in using high frequency and affects efficiency.

Currently, single-stage EV chargers are quite attractive and hot topic for the research. The advantages of single-stage topologies are low components count, high efficiency and compactness.

One single-stage topology is proposed in [8]. It is a three

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All authors are with the Department of Electrical and Information Engineering, Seoul National University of Science and Technology, 418, Mirae hall 232 Gongneung-ro, Nowon-gu 01811, the Republic of Korea (ROK) (e-mail: ali.tausif@seoultech.ac.kr).

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level isolated AC-DC converter. In this topology, a bulky electrolytic capacitor is employed as a DC link capacitor which compromises the volume of the circuit. Moreover, the low-frequency component exists in the transformer winding voltage that increases the size of the transformer. This issue is resolved in [9] in which electrolytic capacitor is replaced by film capacitor; however, it still experiences high conduction loss due to slow diode bridge and also it charges the battery with the sinusoidal current which has a detrimental effect of battery's lifetime due to the heating issue.

Two similar but bridgeless and electrolytic capacitor-less topologies are proposed in [10], [11]. These topologies address most of the issues related to single-stage topologies such as a low-frequency component in transformer voltage, high conduction loss in diode bridge and unreliability due to the short life span of electrolytic capacitors. However, the topology in [11] is superior to [10] concerning its simple structure, bi-directional ability and wide range soft switching capability. The disadvantage with these topologies is the undesirable 2nd harmonic ripple in the battery current which heats the battery and eventually affects its lifetime.

To resolve 2nd harmonic ripple problem associated with single-phase systems many power decoupling techniques have been reviewed and reported in [12], [13]. These techniques have been classified into 2 major categories: 1) independent power decoupling, 2) dependent power decoupling.

In independent power decoupling, the power decoupling cells operate independently from the main converter. Therefore, it requires additional switches to carry out power decoupling which results in increased gate driver losses and circuit complexity. Few well-known topologies for independent power decoupling are proposed in [14]–[18].

On the other hand, the dependent power decoupling method is a convenient way for 2nd harmonic ripple mitigation, as basic decoupling cell shares power semiconductor devices with the original converter partially or even fully. Some of the power decoupling methods in which semiconductor devices are partially shared between power decoupling cell and original converter are proposed in [19]–[21]. Decoupling methods which fully shares the switches with the main converter are also categorised as AC power decoupling methods. In AC power decoupling method, 2nd ripple power is diverted from the DC link and is stored in decoupling capacitors [23]–[25].

One of the suitable AC power decoupling control methods is proposed for the non-isolated AC-DC converter in [26], [27] and is applied to the non-isolated AC-DC differential boost converter [28]. In this approach, power decoupling is successfully achieved by using autonomous closed loop controller. Hence, this concept is extended to obtain a new isolated AC-DC converter which is suitable for EV onboard battery chargers.

The proposed converter has the following features: 1) electrolytic capacitor-less system, 2) high-frequency isolation, 3) AC Power Decoupling and 4) interleaving technique: suitable for high power applications.

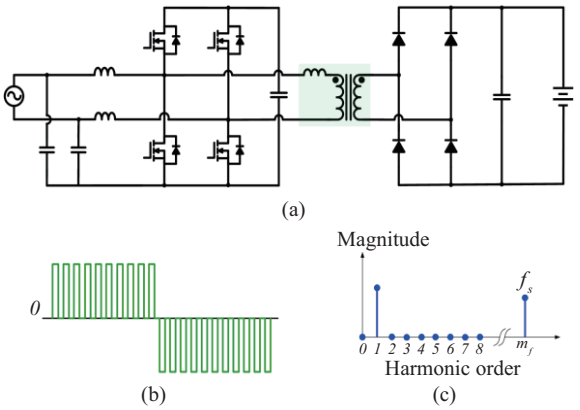


Fig. 1. Single-stage differential boost-type isolated AC-DC converter. (a) Topology. (b) Transformer winding voltage. (c) FFT of transformer winding voltage.

II. Proposed Converter

A. Topology Development

A single stage isolated AC-DC converter based on a differential converter [26] can be constructed as shown in Fig. 1(a). A power decoupling method [23] for a differential converter can be applied to the single stage isolated AC-DC converter. However, the fundamental frequency component appears in the transformer winding voltage as shown in Fig. 1(b) and (c). This fundamental frequency component results in low frequency component in the magnetizing current. Therefore it increases the volume requirement of the transformer making the converter impractical.

In order to have high frequency isolation, the proposed converter, as shown in Fig. 2, is derived by interleaving each leg of the differential converter [26] and connecting each interleaved leg to the transformer windings of two isolated AC-DC converters [29]. Therefore, the two phase interleaved legs have a 180° phase shift in switching frequency. Since there are two of such high frequency links, two transformers are fully utilized and the power is shared between the two converters.

B. Voltage Conversion Ratio

As illustrated in Fig. 3, the proposed converter is composed of two boost converters in which duty d_1 is given to converter 1, and duty d_2 is given to converter 2. Therefore, the voltage conversion ratio of each boost converter is as shown below (1) and (2).

$$\frac{v_{c1}}{1-d_1} = v_{cc} \tag{1}$$

$$\frac{v_{c2}}{1-d_2} = v_{cc} \tag{2}$$

$$v_g = v_{c1} - v_{c2} \tag{3}$$

Substituting (1) and (2) in (3) yields,

$$v_g = (d_2 - d_1)\, v_{cc} = (d_2 - d_1)\, n \cdot v_{bat} \tag{4}$$

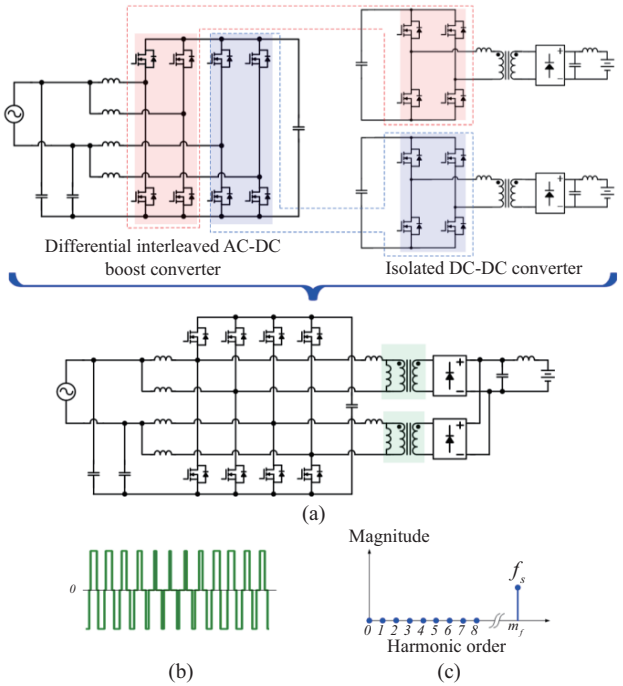


Fig. 2. Proposed single-stage interleaved isolated AC-DC converter. (a) Concept of developing the topology. (b) Transformer winding voltage. (c) FFT of transformer winding voltage.

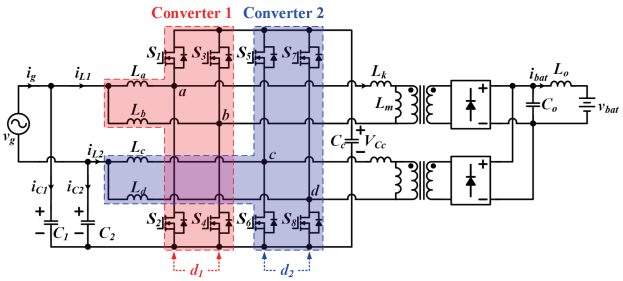


Fig. 3. The structure of the proposed converter.

So, voltage conversion ratio of this topology is,

$$M = \frac{v_{bat}}{v_g} = \frac{1}{n\,(d_2 - d_1)} \tag{5}$$

C. Topology Description

The proposed converter is shown in Fig. 3. It consists of 8 switches at primary side namely S_1~S_8. At input side there are two capacitors C_1 and C_2 followed by input inductors L_a, L_b, L_c and L_d. Two transformers T_1 and T_2 are connected between interleaved legs formed by *leg a, leg b, leg c*, and *leg d* respectively. The secondary side consists of two full bridge diode rectifiers which are connected in parallel and serve as the output terminal. C_c is the clamping capacitor and voltage across C_c is equal to the battery voltage reflected to the primary side, i.e., if leakage inductance of the transformer is assumed to be negligible, then $V_{Cc} = n \cdot v_{bat}$.

According to differential converter [26] concept voltage across C_1 and C_2 is given as:

$$v_{c1} = \frac{nv_{bat}}{2} + \frac{V_g}{2}\sin\omega t \tag{6}$$

$$v_{c2} = \frac{nv_{bat}}{2} - \frac{V_g}{2}\sin\omega t \tag{7}$$

It can be seen that grid voltage and current is given as:

$$v_g = v_{c1} - v_{c2} = V_g \sin\omega t \tag{8}$$

$$i_g = I_g \sin(\omega t + \delta) \tag{9}$$

In the proposed topology C_1 and C_2 are connected directly to the grid. Therefore, leading current will flow through C_1 and C_2 which is given by,

$$i_{lead} = C_{eq}\frac{dv_g}{dt} \tag{10}$$

where $C_{eq} = C_1 \parallel C_2$ and $C_1, C_2 = C$.

$$i_{lead} = \frac{\omega C V_g}{2}\cos\omega t \tag{11}$$

Note that this leading current depends upon the value of C_1 and C_2 and it introduces a slight phase shift (δ) in the grid current deteriorating the power factor. Hence, there will be some reactive power flow into the circuit. However, this current can be minimized by adding reactive power compensation in the controller of the proposed converter.

The instantaneous power flowing across C_1 and C_2 is given as:

$$p_c = v_{c1}C_1\frac{dv_{c1}}{dt} + v_{c2}C_2\frac{dv_{c2}}{dt} \tag{12}$$

$$p_c = \frac{\omega C V_g}{4}\sin 2\omega t \tag{13}$$

Equation (13) is equivalent to reactive power due to leading current.

D. Principle of Power Decoupling

In single phase, AC-DC systems power pulsation at double the line frequency occurs and it is unavoidable in the case of using film capacitors. This 2nd harmonic ripple power appears at the output in the form of pulsating battery current.

Assuming PF = 1, power at the grid side can be calculated as:

$$p_{in} = v_g \cdot i_g \tag{14}$$

$$p_{in} = \frac{V_g I_g}{2} - \frac{V_g I_g \cos 2\omega t}{2} \tag{15}$$

Since, output power is equal to the input power, assuming the converter to be lossless.

$$p_{out} = \frac{V_g I_g}{2} - \frac{V_g I_g \cos 2\omega t}{2} \tag{16}$$

From (16), the instantaneous output power comprises of average power and undesirable ripple power. In the proposed

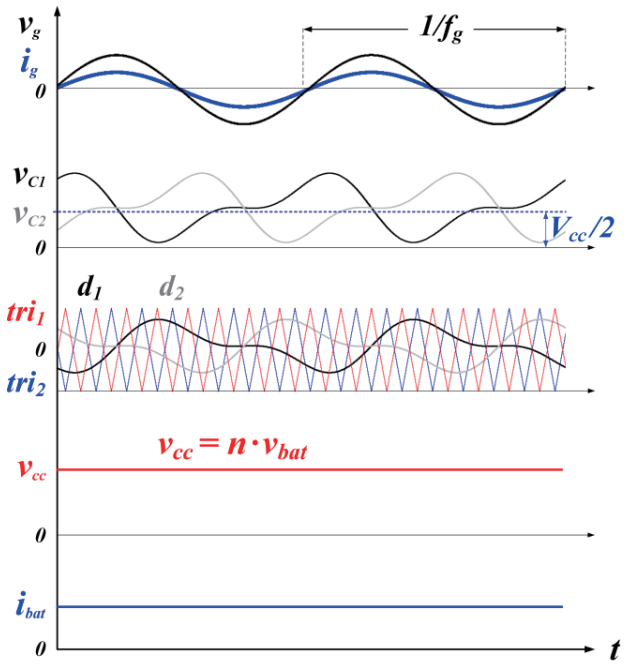


Fig. 4. Key waveform of operating principle for grid frequency.

converter this ripple power is decoupled from the output and is stored in the input capacitors C_1 and C_2 as 2nd harmonic voltage component illustrated in Fig. 4. This is accomplished by shaping the voltage across C_1 and C_2 as:

$$v_{c1} = \frac{nv_{bat}}{2} + \frac{V_g}{2}\sin\omega t + V_c \sin(2\omega t + \phi) \tag{17}$$

$$v_{c2} = \frac{nv_{bat}}{2} - \frac{V_g}{2}\sin\omega t + V_c \sin(2\omega t + \phi) \tag{18}$$

During power decoupling operation, the ripple power component in (16) is diverted from output to C_1 and C_2, so the instantaneous power across C_1 and C_2 can be obtained by substituting (17) and (18) in (12),

$$p_c = \frac{V_g^2}{4}\omega C \sin 2\omega t + 2nv_{bat}V_c\omega C\cos(2\omega t + \phi) + 4\omega C V_c^2 \sin(4\omega t + 2\phi) \tag{19}$$

Note that (19) contains 2nd and 4th harmonic component, this 4th harmonic ripple component is usually small and it can be neglected, so 2nd harmonic component in (19) equates to ripple power component in (16) given as,

$$\frac{V_g^2}{4}\omega C \sin 2\omega t + 2nv_{bat}V_c\omega C\cos(2\omega t + \phi) = \frac{V_g I_g \cos 2\omega t}{2} \tag{20}$$

Solving (20) for V_c and ϕ, we get

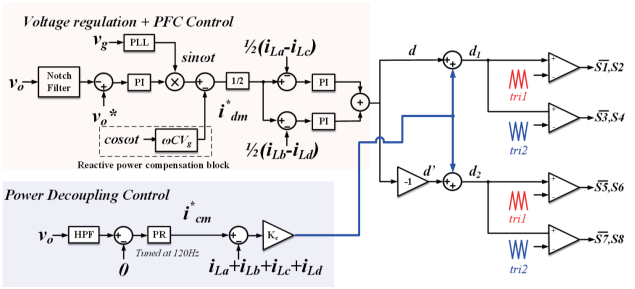


Fig. 5. Block diagram of the proposed controller.

$$V_c = \frac{V_g\sqrt{V_g^2\omega^2C^2 + 4I_g^2}}{8nv_{bat}C\omega} \tag{21}$$

$$\phi = \pi - \tan^{-1}\frac{V_g\omega C}{2I_g} \tag{22}$$

Substituting V_c and ϕ in (17) and (18) yields,

$$v_{c1} = \frac{nv_{bat}}{2} + \frac{V_g}{2}\sin\omega t - \frac{P_O}{2nv_{bat}}\cos 2\omega t + \frac{V_g^2}{8nv_{bat}}\cos 2\omega t \tag{23}$$

$$v_{c2} = \frac{nv_{bat}}{2} - \frac{V_g}{2}\sin\omega t - \frac{P_O}{2nv_{bat}}\cos 2\omega t + \frac{V_g^2}{8nv_{bat}}\cos 2\omega t \tag{24}$$

It can be seen that for a fixed grid voltage, V_c and ϕ are load dependent parameters and in the proposed converter, V_c and ϕ are adjusted by closed-loop controller.

III. Control Method

The controller for the proposed topology is divided into two parts: the differential mode controller and the common mode controller. The differential mode controller is responsible for PFC control and output voltage regulation. In this controller, the difference of sensed inductor currents is compared with the reference to generate an error which is compensated by the inner current loop PI controller. Due to interleaving and nonlinear duty, the inductor current imbalance problem may occur, but it can be resolved by dividing the reference into half and using two separate controllers for each interleaving legs as shown in Fig. 5. Apart from this, a reactive power due to leading current is compensated by adding a feed forward term in the reference of the differential current. The value of this compensating signal is fixed for a particular grid voltage and is independent of load as can be seen from (11).

The reference for differential mode current is given as:

$$i_{dm}^* = \frac{(i_{La} + i_{Lb}) - (i_{Lc} + i_{Ld})}{2} = i_g^* - i_{lead}^* \tag{25}$$

In addition to this, Common Mode Power Decoupling Con-

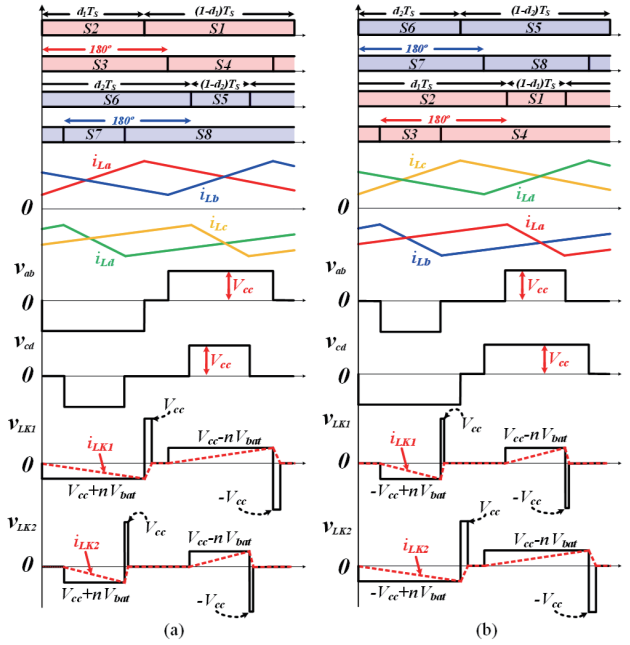


Fig. 6. Key waveforms of the converter for switching period, (a) when $v_g > 0$, (b) when $v_g < 0$.

trol is applied in which 2nd harmonic ripple is extracted from output and is subtracted from 0 reference to generate an error. This error is minimized by using the PR controller tuned at 120 Hz and the 2nd harmonic compensated signal is generated.

The reference for common mode current is given as:

$$\begin{aligned} \overset{*}{i}_{cm} &= i_{La} + i_{Lb} + i_{Lc} + i_{Ld} = 2C\frac{d}{dt}(v_{cm}) \\ &= 2C\frac{d}{dt}\left(\frac{v_{c1} + v_{c2}}{2}\right) \\ &= 4\omega C V_c \cos(2\omega t + \phi) \end{aligned} \tag{26}$$

The compensated signal is the reference signal and it is compared with the sum of all sensed inductor currents. The resulted signal is then fed to the proportional controller with gain K_c which is added to the differential mode controller duties d and d' to obtain final duties d_1 and d_2.

IV. Operating Principles

The primary side of the converter can be thought of as two interleaved converters are illustrated in Fig. 2. One converter in composed of S_1, S_2, S_3 and S_4 is operated with duty d_1 while the other converter is composed of S_5, S_6, S_7 and S_8 is operated with duty d_2. During positive half cycle converter 1 acts as an interleaved boost converter whereas converter 2 acts as an interleaved buck converter. Similarly, during negative half cycle converter 2 acts as interleaved buck converter and converter 1 acts as interleaved boost. The key waveforms of the converter are shown in Fig. 6.

A. Modes by Mode Operation

During the positive half cycle of the grid, the proposed converter undergoes five distinct modes of operation based on its switching status. During Mode 1 switches S_2, S_3, S_6 and S_8 are ON, and switches S_1, S_4, S_5 and S_7 are turned OFF. Inductor L_a charges and L_b discharges. However, both L_c and L_d discharge as these inductors are associated with converter 2 which acts as the buck converter during this mode. In this mode $v_{ab} = -V_{Cc}$ and the power is transferred to the battery through transformer T_1. The current through the transformer increases with the slope given as:

$$\frac{di_{Lk1}}{dt} = \frac{-V_{Cc} + nV_{bat}}{L_k} \tag{27}$$

Mode 2 starts when S_7 is turned ON and S_6 is turned OFF, as shown in Fig. 7. The status of the switches of converters is given as S_2, S_3, S_6 and S_7 are ON while all other switches are OFF. Since S_7 is turned ON the inductor L_d begins to charge in this mode. During this mode the slopes of other inductor currents remain same, however $v_{cd} = -V_{Cc}$, therefore power is transferred through the transformer T_2 as well. The slope of i_{Lk2} is given as:

$$\frac{di_{Lk2}}{dt} = \frac{-V_{Cc} + nV_{bat}}{L_{k2}} \tag{28}$$

As shown in Fig. 7, during Mode 3, S_1, S_3, S_6 and S_8 are ON while others are OFF. Inductor L_a and L_b discharge through the clamping capacitor C_c while L_c and L_d discharge through decoupling capacitor C_2. During this mode, v_{ab}, $v_{cd} = 0$, therefore no power is transferred in this mode.

Mode 4 begins when S_4 is turned ON and S_3 is turned OFF. During this mode L_b begins to charge while all the other inductors are still discharging as in the previous mode. However, during this mode, $v_{ab} = V_{Cc}$, therefore power is being transferred to the load only through the transformer T_1 and its current increases with the slope given as:

$$\frac{di_{Lk1}}{dt} = \frac{V_{Cc} - nV_{bat}}{L_{k1}} \tag{29}$$

Similarly, during Mode 5, S_5 is turned ON, and S_6 is turned OFF. During this mode, L_c begins to discharge as a negative voltage equal to $-v_{c2}$ is applied across it. In this mode, $v_{ab} = V_{Cc}$, therefore the commutation occurs through both the transformers T_1 and T_2 and power is being transferred to the load. The slopes of current through leakage inductances of transformers T_2 is given as:

$$\frac{di_{Lk2}}{dt} = \frac{V_{Cc} - nV_{bat}}{L_{k2}} \tag{30}$$

Operation during the negative half cycle is similar to the positive half cycle. The only difference is that during negative half cycle converter 1 acts as interleaved buck while converter 2 acts as an interleaved boost converter. Operating waveform of the converter for switching period and $v_g < 0$ is presented in Fig. 6(b).

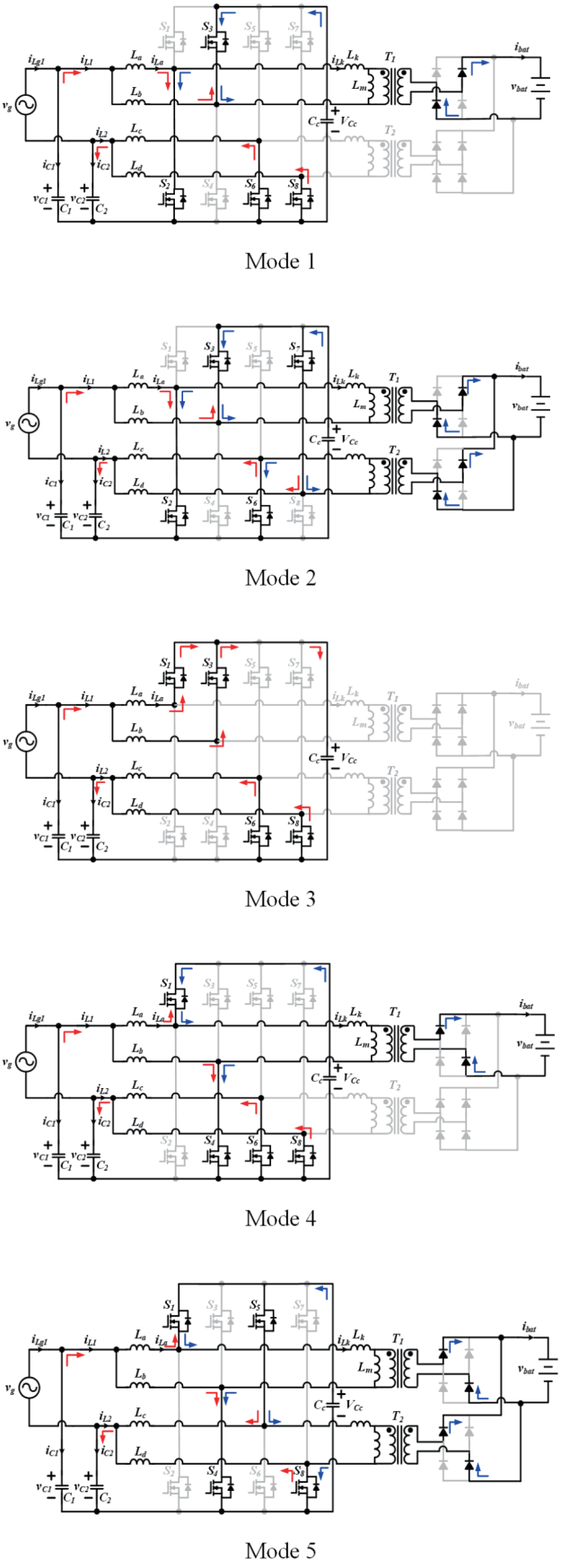


Fig. 7. Modes by mode operation $v_g > 0$.

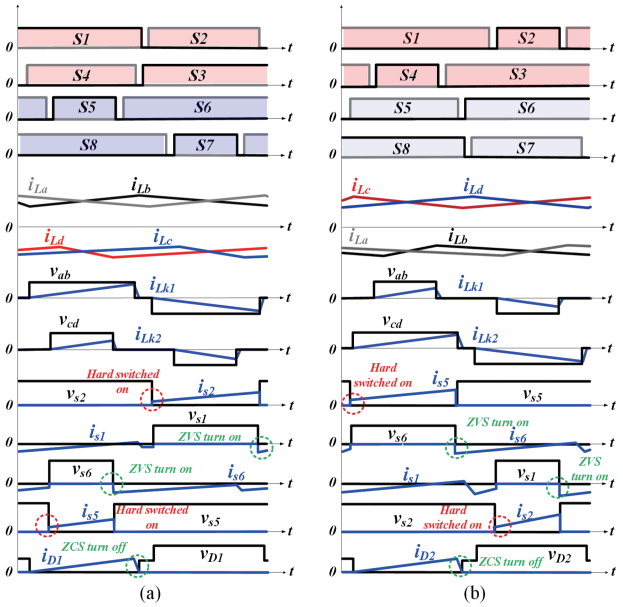


Fig. 8. Switching characteristics, (a) when $v_g > 0$, (b) when $v_g < 0$.

B. Switching Characteristics

As already explained in the previous section, during the positive half cycle, the operation of converter 1 is similar to the interleaved boost converter and that of converter 2 is similar to the interleaved buck converter. Therefore, the switches S_1 and S_3 associated with converter 1 act as synchronous rectifiers and are always turned on with ZVS condition. Whereas switches S_2 and S_4 are hard switched as illustrated in Fig. 8(a). Similarly, switches S_6 and S_8 act as synchronous rectifiers of the interleaved buck converter, i.e., converter 2 and they always achieve ZVS Turn ON, while S_5 and S_7 are hard turned ON.

The operation of converter 1 during the negative half cycle is similar to that of the positive half cycle with the only difference that converter 1 acts as the interleaved buck converter and converter 2 acts as the interleaved boost converter. Therefore switches S_2, S_4, S_5 and S_7 turn ON with ZVS condition and remaining switches are hard turned ON. The waveform of this phenomenon is presented in Fig. 8(b).

Note that all diodes at the secondary side turn OFF with ZCS, the currents flowing through the diodes are the leakage inductor currents i_{Lk1} and i_{Lk2} reflected to the secondary side. Since, L_{k1} and L_{k2} are always naturally clamped to V_{Cc}, hence all secondary diodes turn OFF with slopes given as $\frac{V_{Cc}}{L_k}$.

V. Simulation and Experimental Results

The simulation of the proposed converter is performed in PSIM and circuit components are selected based on 6.6 kW design. Table I shows the circuit parameters.

The universal input range of 90~250 V_{rms} is considered for the design. For typical onboard battery chargers, the output voltage range is from 250~450 V. Input inductor are selected based on input current THD_{ig} which is kept around 5% for the

TABLE I
CIRCUIT PARAMETERS

Output power	P_o	6.6 kW
Switching frequency	f_s	200 kHz
Grid voltage	V_g	220 V_{rms}
Output voltage	V_o	450 V
Input inductors	L_a, L_b, L_c, L_d	60 µH
Decoupling capacitors	C_1, C_2	100 µF
Clamping capacitor	C_c	40 µF
Output capacitor	C_o	20 µF
Turns ratio	N	2
Magnetizing inductance	L_m	5 mH
Leakage inductance	L_k	5 µH

worst case scenario. So, after considering the aforementioned specifications, L_a, L_b, L_c and L_d = 60 µH is selected.

At Input side, decoupling capacitors C_1 and C_2 are chosen based on the fact that the maximum swing of voltage on C_1 and C_2 should be confined within the range 0 to V_{Cc}. This constraint exists because the proposed converter is derived from the boost type differential converter which works on the principle that,

$$0 < v_{c1}, v_{c2} < V_{Cc} \tag{31}$$

As shown in the equations (17) and (18), the peak voltage of v_{c1} and v_{c2} may not only depends upon the peak of grid voltage but also on the peak of 2nd harmonic voltage that is stored in the decoupling capacitors C_1 and C_2.

It is to note that this 2nd harmonic voltage depends upon load parameters, i.e., output power and voltage, as can be seen in (21). Hence, C_1 and C_2 are selected considering the aforementioned constraints. Capacitance requirement at different turn ratio over wide battery voltage range can be determined by satisfying (31) using (23) or (24). The resulted graph is shown in Fig. 9. For the worst case battery voltage of 250 V and turns ratio n = 2, C_1, C_2 lies in the range of 80~100 µF. So, 100 µF is selected.

Simulation waveform is shown in Fig. 10(a), it can be seen that a high power factor of 0.99 and input current THD_{ig} of 5.2% is achieved. DC battery current is obtained at the output which means that 2nd harmonic component is successfully eliminated from the output current and is stored in the form of 2nd harmonic voltage component in the decoupling capacitors C_1 and C_2 as shown in Fig. 10(a).

The simulation waveform also shows that half of the switches of the proposed converter achieves ZVS Turn On during positive half cycle while other half of the switches achieve ZVS Turn On during negative half cycle. The extended waveform of the switches during $v_g < 0$ is depicted in Fig. 10(b) which also shows that half of the switches are ZVS Turn on and half of the switches are Hard Turn On. So, during positive half cycle S_1, S_2, S_6 and S_8 can achieve ZVS Turn On while S_2, S_4, S_5 and S_6 are Hard Turn Off. On the other hand, during negative half cycle

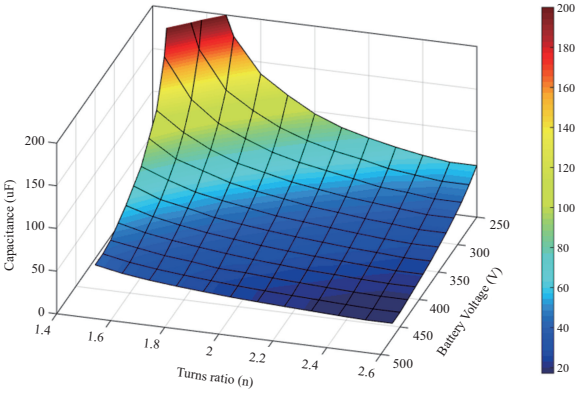


Fig. 9. Capacitance requirement for different turns ratio over wide output voltage range.

S_2, S_4, S_5 and S_6 can achieve ZVS Turn ON while S_1, S_2, S_6 and S_8 are Hard Turn Off. Note that all diodes at the secondary side achieve ZCS Turn Off due to clamping of L_k with C_c during the non-commutation mode of the transformer.

Two transformers of equal L_k and L_m are used for the simulation. For simulation, L_k = 5 µH and L_m = 5 mH is chosen and turn ratio n is selected as 2. The simulation waveform of the transformer winding voltage for the grid frequency is shown in Fig. 10(c) and its FFT in Fig. 10(d).

A 6.6 kW experimental prototype is shown in Fig. 11. 1200 V Silicon Carbide switches are used at primary side of the converter and 650 V SiC Schottky diodes are used for secondary side diodes. Two transformers are designed specifically for 200 kHz to keep the size as compact as possible. The practical values of L_m = 4.7 mH and L_k = 6.7 µH for transformer 1 and L_m = 4.5 mH and L_k = 6.3 µH for transformer 2 are obtained with optimized design.

Fig. 12(a) shows the grid voltage and grid current obtained at around 2.2 kW power. It can be seen that a very high power factor of 0.99 with very low *THD* is achieved. After applying power decoupling control, pure DC voltage is obtained at the output and the 2nd harmonic power pulsation is store in the form of 2nd harmonic voltage component in the input capacitors C_1 and C_2. The experimental waveform is illustrated in Fig. 12(b).

L_a and L_b are interleaved inductors with 180° phase shift in switching frequency, similarly L_c and L_d are also interleaved. This phenomenon is experimentally illustrated in Fig. 12(c).

In this topology, high frequency transformers are utilized. The extended experimental waveform of transformer winding voltage and leakage current is presented in Fig. 12(d). It can be seen that the volt-sec of transformer winding voltage is balanced, therefore magnetizing current will not have any offset or low frequency component.

As already explained earlier, half of the switches achieve ZVS Turn ON during one half cycle and the other half of the switches achieve ZVS Turn ON during the other half cycle. The experimental waveform of this phenomenon for one leg switches is shown in Fig. 13.

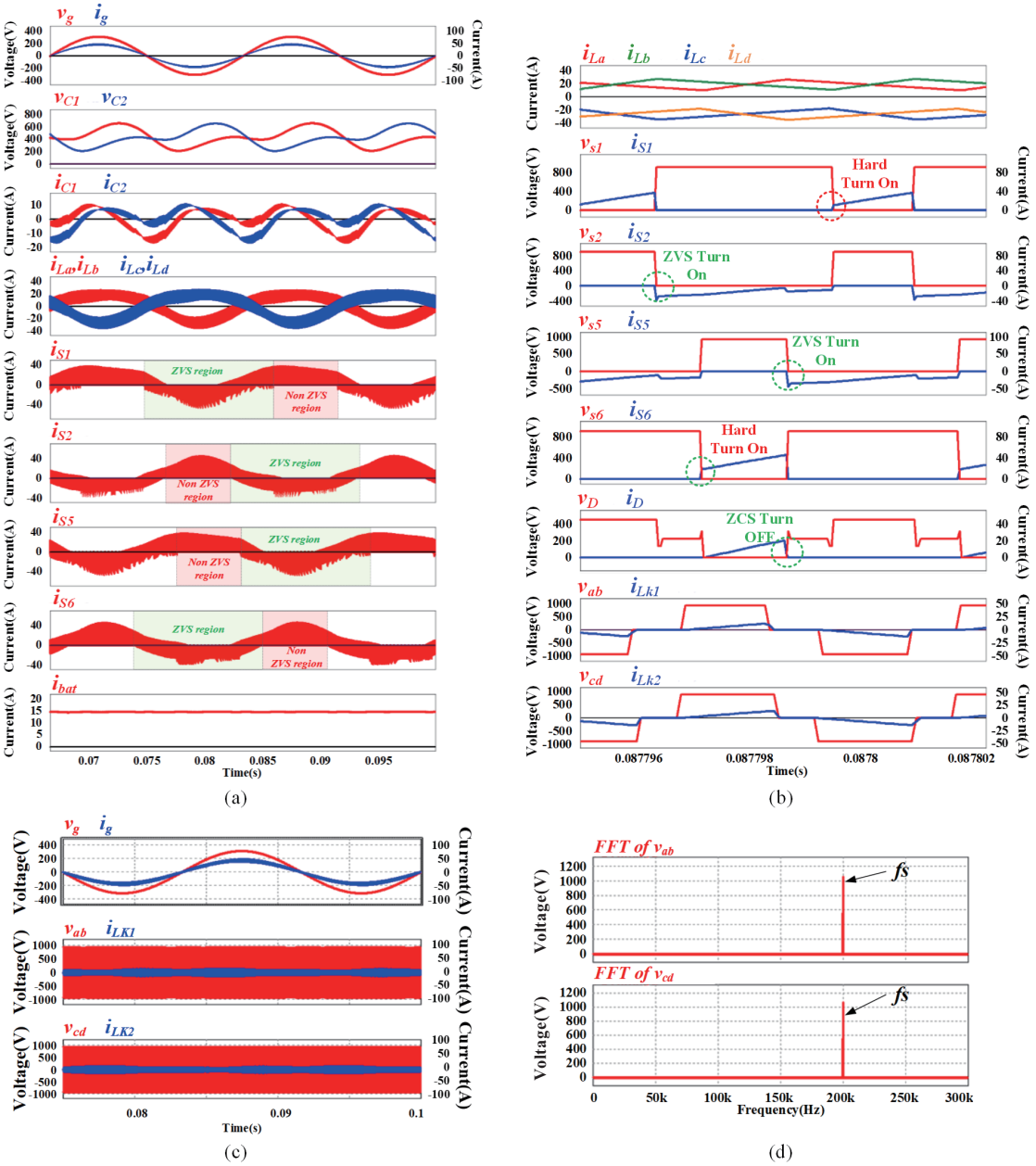


Fig. 10. Simulation waveforms. (a) Key waveforms of converter over line cycle. (b) Switch voltage and current over switching period. (c) Transformer winding voltage and current. (d) FFT of transformer voltage.

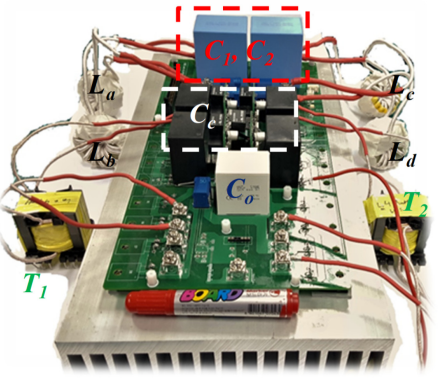


Fig. 11. Experimental prototype of proposed converter.

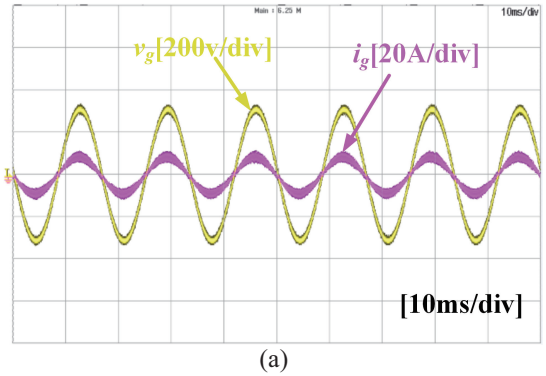
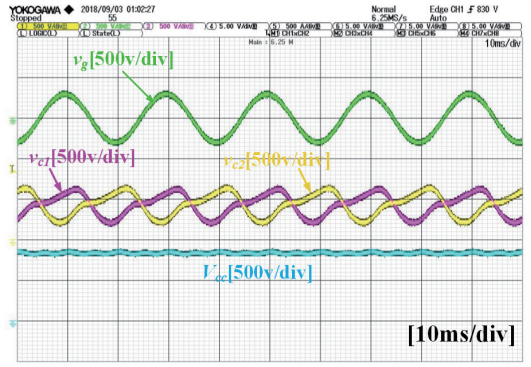
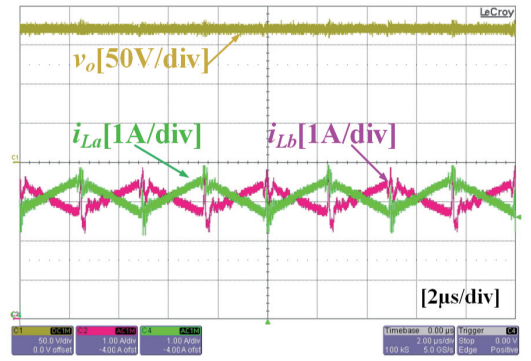


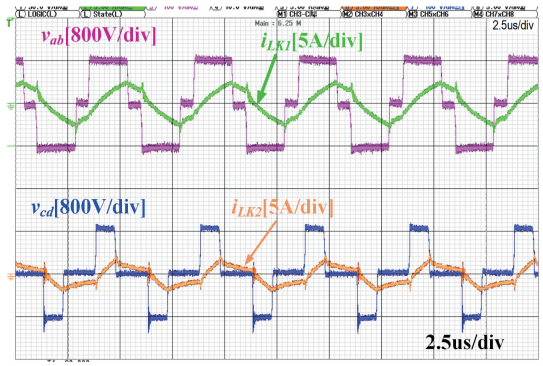
Fig. 12. Experimental waveforms. (a) Grid voltage v_g and grid current i_g.



(b)



(c)



(d)

Fig. 12. (*Continued*..) Experimental waveforms. (b) Grid voltage v_g, decoupling capacitors voltage v_{c1}, v_{c2} and clamping capacitor voltage v_{Cc}. (c) Interleaved inductor current i_{La}, i_{Lb} with output voltage v_o. (d) Transformer winding voltage and current.

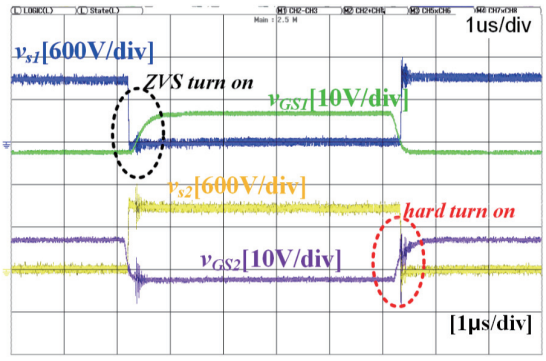


Fig. 13. Experimental waveforms of v_{gs} and v_{ds} of switch S_1 and S_2.

VI. Conclusion

In this paper, a single-stage isolated AC-DC converter has been proposed for EV battery charger. The main features of the proposed converter include high-frequency isolation, and the AC-DC power conversion is done by a single-stage. AC power decoupling is successfully applied to obtain DC charging and the requirement to use bulky electrolytic capacitor is eliminated. Hence film capacitors with small capacitance can be used to enhance reliability and power density of the converter. One good feature of the proposed controller is that it does not require an on-line calculation based on complicated formulas to calculate reference voltage for shaping decoupling capacitor voltage. On the other hand, the switches are turned on with hard switched/ZVS in CCM which means half of the switches of this converter achieve ZVS Turn On during half line cycle and the other half of the switches are Hard Turn On. Moreover, all secondary diodes are turned Off with ZCS. Finally, a 6.6 kW prototype has been built and tested to verify the operating principles of the proposed onboard battery charger.

References

[1] X. Zhang, D. Dome, and R. Rupp, "Efficiency improvement with silicon carbide based power modules", *Power Electron. Europe*, Issue 6, p. 27, Sept. 2009.

[2] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Appl*., vol. 47, no. 2, pp. 912-921, Mar.-Apr. 2011.

[3] A. Stippich, C.H. van der Broeck, A. Sewergin, A. H. Wienhausen, M. Neubert, P. Schulting, S. Taraborrelli, H. van Hoek, and R. W. De Doncker, "Key components of modular propulsion systems for next generation electric vehicles," *CPSS Trans. Power Electron. Appl*. vol. 2, no. 4, Dec. 2017.

[4] Department of Energy. EV everywhere: A grand challenge in plug-in, electric vehicles (initial framing document) (Aug. 2012) [Online]. Available: https://www.energy.gov/articles/ev-everywhere-wants-hear-all-you

[5] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[6] S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An automotive onboard 3.3-kW battery charger for PHEV application," *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3466–3474, Oct. 2012.

[7] B. Whitaker *et al*., "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[8] S. Dusmez, X. Li, and B. Akin, "A fully integrated three-level isolated single-stage PFC converter," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2050–2062, Apr. 2015.

[9] B. Kim, M. Kim, and S. Choi, "A reduced component count single-stage electrolytic capacitor-less battery charger with sinusoidal charging," in *2017 IEEE 3rd Int, Future Energy Electron. Conf. ECCE Asia* (*IFEEC 2017 - ECCE Asia*), Kaohsiung, 2017, pp. 242-246.

[10] B. Kim, M. Kim, and S. Choi, "Single-stage electrolytic capacitor-less AC-DC converter with high frequency isolation for EV charger," in *2016 IEEE 8th Int. Power Electron. Motion Control Conf.* (*IPEMC-ECCE Asia*), Hefei, 2016, pp. 234–238.

[11] H. Belkamel, K. Hyungjin, K. Beywongwoo, Y. Shin, and S. Choi, "Bi-directional single-stage interleaved totem-pole AC-DC converter with high frequency isolation for on-board EV charger," in *2018 IEEE Energy Conv. Congr. Expo.* (*ECCE*), Portland, OR, 2018, pp. 6721-6724.

[12] Y. Sun, Y. Liu, M. Su, W. Xiong and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power*

Electron., vol. 31, no. 7, pp. 4778–4794, July 2016.
[13] K. A. Kim, Y. C. Liu, M. C. Chen, and H. J. Chiu, "Opening the box: survey of high power density inverter techniques from the little box challenge," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, June 2017.
[14] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron*., vol. 27, no. 11, pp. 4690–4698, Nov., 2012.
[15] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl*., vol. 36, no. 4, pp. 1419–1429, Sep./Oct, 2000.
[16] L. Palma, "An active power filter for low frequency ripple current reduction in fuel cell applications," in *Proc. IEEE SPEEDAM,* Pisa, 2010. pp. 1308–1313.
[17] S. K. Mazumder, R. K. Burra, and K. Acharya, "A ripple-mitigating and energy-efficient fuel cell power-conditioning system," *IEEE Trans. Power Electron*., vol. 22, no. 4, pp. 1437–1452, July 2007.
[18] H. Han, Y. Liu, Y. Sun, M. Su, and W. Xiong, "Single-phase current source converter with power decoupling capability using a series-connected active buffer," *IET Power Electron*., vol. 8, no. 5, pp. 700–707, May 2015.
[19] R. Chen, Y. Liu, and F. Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron*., vol. 30, no. 10, pp. 5499–5507, Oct. 2015.
[20] S. Fan, Y. Xue, and K. Zhang, "Novel active power decoupling method for single-phase photovoltaic or energy storage applications," in *Proc. IEEE ECCE,* Raleigh, 2012, pp. 2439-2446.
[21] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Proc. IEEE APEC,* Fort Worth, TX, 2014. vol. 3, pp. 89–95.
[22] H. Zhao, H. Lin, C. Min, and K. Zhang, "A Modified single-phase H-bridge PWM rectifier with power decoupling," in *Proc. IEEE IECON,* Montreal, QC, 2012. pp. 80–85.
[23] I. Serban, "Power decoupling method for single-phase h-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron*., vol. PP, no. 99, pp. 1, Feb. 2015.
[24] G. R. Zhu, S. C. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron*., vol. 28, no. 2, pp. 779–792, Feb. 2013.
[25] S. Li, G. Zhu, S. C. Tan, and S. Y. Hui, "Direct AC/DC rectifier with mitigated low-frequency ripple through waveform control," in *Proc. IEEE ECCE,* Pittsburgh, PA, 2014. pp. 2691–2697.
[26] W. Yao, Y. Tang, X. Zhang, X. Wang, P. C. Loh and F. Blaabjerg, "Power decoupling method for single phase differential buck converter," in *2015 9th Int. Conf. Power Electron. ECCE Asia (ICPE-ECCE Asia)*, Seoul, 2015, pp. 2395–2402.
[27] W. Yao, X. Zhang, X. Wang, Y. Tang, P. C. Loh, and F. Blaabjerg, "Power decoupling with autonomous reference generation for single-phase differential inverters," in *2015 17th European Conf. Power Electron. Appl. (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1–10.
[28] J. Almazan, N. Vazquez, C. Hernandez, J. Alvarez, and J. Arau, "A comparison between the buck, boost and buck-boost inverters," in *7th IEEE Int. Power Electron. Congr. Tech. Proc. CIEP 2000* (Cat. No.00TH8529), Acapulco, Mexico, 2000, pp. 341–346.
[29] A. Tausif and S. Choi, "Single-stage Differential Current-fed Isolated AC-DC Converter for Electrolytic Capacitor-less OBC with DC Charging," in *2018 IEEE Int. Power Electron. Appl. Conf. Expo.* (*PEAC*), Shenzhen, China, 2018, pp. 1–5.

Ali Tausif was born in Pakistan, in 1991. He received his B.S. degree in Electrical Engineering from College of Electrical and Mechanical Engineering (CEME), National University of Science and Technology (NUST), Islamabad, Pakistan, in 2014. In 2016, he joined Power Electronics and Fuel Cell Power Conditioning Lab, SeoulTech as Graduate Research Student. He received his Master's degree from the Department of Electric and Information Engineering, Seoul National University of Science and Technology (Seoul Tech), in 2019. His research interests includes DC-DC converters and AC-DC converters for Electric Vehicles applications and Renewable Energy Systems.

Hoyoung Jung was born in Korea, in 1992. He received the B.S. degrees in the Electrical and Information Engineering from Seoul National University of Science and Technology (Seoul Tech), Seoul, South Korea, in 2018, where he is currently working toward the M.S. degree in electrical and information engineering, Seoul Tech. His research interests include AC-DC converter and grid-connected inverter for electric vehicles and renewable energy systems.

Sewan Choi received the B.S. degree in Electronic Engineering from Inha University, Incheon, Korea, in 1985 and the M.S. and Ph.D. degrees in Electrical Engineering from Texas A&M University, College Station, TX, in 1992 and 1995, respectively. From 1985 to 1990, he was with Daewoo Heavy Industries as a Research Engineer. From 1996 to 1997, he was a Principal Research Engineer at Samsung Electro-Mechanics Co., Korea. In 1997, he joined the Department of Electrical and Information Engineering, Seoul National University of Science and Technology (Seoul Tech), Seoul, Korea, where he is currently a Professor. His research interests include power conversion technologies for renewable energy systems and energy storage systems and DC-DC converters and battery chargers for electric vehicles. He is an associate editor of the *IEEE Transactions on Power Electronics*. He is an IEEE Fellow.

Transient Stability Analysis of Grid-Tied Converters Considering PLL's Nonlinearity

Xiuqiang He, Hua Geng, and Shaokang Ma

***Abstract*—Transient instability events of grid-tied converters probably occur while riding through grid faults. During low-voltage ride through (LVRT) period, seeing from the converter terminal towards the grid, the Thévenin equivalent grid impedance becomes pretty significant, accordingly making the converter terminal voltage highly sensitive to the output current. Under such circumstances, it is challenging for the converter to resynchronize with the grid via a phase-locked loop (PLL). This paper develops a reduced-order nonlinear model to elaborate on the dynamic synchronization characteristic of the converters. By considering the impact of grid impedance and analysing spatial vector tracking relation, resynchronization principle of the converters during LVRT is revealed. Besides, the impacts of circuit parameters and controller parameters, including residual grid voltage, grid impedance, current references, and PLL parameters, on the transient stability of the converters are investigated. The results are verified by simulation and experimental results.**

***Index Terms*—Grid fault, low voltage ride through, phase-locked loop, power converter, synchronization, transient stability.**

I. Introduction

GRID-TIED power converters are playing increasingly important roles in power systems, along with the rapid development of renewable power generation in recent years. Three-phase voltage source converters (VSCs), as one of the most crucial components of renewable energy generation units, often offer quite different performance from the conventional synchronous generator units, such as outstanding rapidity and controllability, but limited fault ride through capability [1], [2]. Grid codes for renewable power generation, in which various facets of the operating characteristics of grid-tied renewable energy generation units are standardized, have been formulated by independent system operators in order to ensure the power system security and stability [2]–[4]. One of the grid codes, namely low-voltage ride through (LVRT) requirement, requires renewable energy generation units to remain connected to the grid and also output a specific reactive current to support the residual grid voltage during LVRT period [2]–[4].

When a grid fault occurs, the Thévenin equivalent grid impedance generally becomes considerable [5], resulting in weak connection between VSCs and the power grid [5]–[7]. Consequently, the VSC terminal voltage is easily affected by the VSC output current. Conversely, the output current is also influenced by the terminal voltage since the current phase-angle is guided by the phase-locked loop (PLL) which is with the terminal voltage as the input. It has been reported that loss of synchronism (LOS) of the grid-tied VSCs probably happens during LVRT because of the dynamic interaction between the PLL and the terminal voltage [5]–[22]. Note that the LVRT requirements of the grid codes can no longer be satisfied once the LOS occurs.

During severe grid faults, i.e., under large disturbances, on one hand, initial states of the VSC systems will probably be random. On the other hand, state trajectories of the VSC systems often exhibit a large change magnitude. Therefore the nonlinearity in system components, especially PLL's nonlinearity, cannot be neglected in the stability assessment. In this regard, previous relevant small-signal stability studies of the VSCs [8]–[11] can not effectively address the transient stability issues.

The transient instability issues associated with the LOS have not drawn much attention. [12] and [13] made investigations on the presence of equilibrium points of the grid-tied VSCs during grid voltage sags, but dynamic synchronization characteristics were not taken into account. [14] and [15] also claimed that the transient stability of VSCs can be considered as the presence of post-fault equilibrium points. However, we found in [5]–[7] that there is an instability possibility for a grid-tied VSC due to improper initial states and poor dynamic performance in addition to the absence of equilibrium points.

To elaborate the instability issue in dynamic processes, [16]–[18] applied the concept of equal area criterion (EAC) to analyse the transient stability of VSCs during LVRT. Nevertheless, the results were conservative since the proportional unit of PLL was ignored in the EAC method. Lately, the research group of X. Wang made innovative studies on the synchronization of grid-tied VSCs using the concept of phase portrait [19]–[22], which have created a new perspective for the transient stability studies of grid-tied VSCs. Besides, it should be noted that Lyapunov's direct method was also employed to assess the transient stability of grid-tied VSCs in [23]–[26]. Although transient stability can be judged through Lyapunov's direct method, the impacts of circuit parameters and controller parameters on the transient stability margin can only be investigated in a case-by-case way through the method, rather

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The authors are with the Department of Automation, Tsinghua University, Beijing, 100084, China (e-mail: he-xq16@mails.tsinghua.edu.cn; genghua@tsinghua.edu.cn; msk15@mails.tsinghua.edu.cn).

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than evaluated systematically.

According to the literature review, although the dynamic synchronization process of VSCs has been investigated in [14]–[22], resynchronization principle of the VSCs during LVRT considering the impact of grid impedance on the PLL detecting ability has not been completely clarified. Furthermore, the effects of circuit parameters and controller parameters on the transient stability have not been extensively investigated. As an expanded version of our conference paper [27], this paper is devoted to filling this gap. Specifically, a reduced-order nonlinear model is derived and validated in Section II. A comprehensive stability analysis is performed in Section III, where the resynchronization principle is analysed through the spatial vector tracking relation from the PLL point of view. Also, the impacts of circuit parameters and controller parameters on the transient stability margin is quantitatively investigated. Sections IV and V show the simulation and experimental results, respectively, and Section VI concludes this paper.

II. System Modeling

A grid-tied VSC system is shown in Fig. 1. PLL is utilized to detect the phase-angle and frequency of the VSC terminal voltage $\boldsymbol{u}_{abc}$, and the estimated phase-angle θ_{pll} is then used as the angle reference for the current control module. Fig. 1(b) depicts the dynamic interaction between the PLL and the VSC terminal voltage. The output of the PLL guides the phase-angle of the output current which makes the grid impedance produce a voltage drop $\Delta\boldsymbol{U}$. The grid impedance voltage drop $\Delta\boldsymbol{U}$ makes the terminal voltage $\boldsymbol{U}$ no longer stiff and highly sensitive to the output current once the grid impedance becomes considerable rather than ignorable.

When a grid fault occurs, a Thévenin equivalent circuit can be built from the fault point of view [5]. [5] indicated that the Thévenin equivalent grid impedance would become considerable if the grid fault is severe. In other words, severe faults would lead to weak connection between the VSC and the infinite-bus grid in the Thévenin equivalent circuit, even though the pre-fault grid is not weak [5].

Prior to modeling the VSC system for the transient stability analysis, several assumptions are made as follows [5]–[7], [12], [13], [16]–[22]:

1) The DC-link voltage of the VSC is considered to be constant, due to the fact that the configured chopper circuit [not shown in Fig. 1(a)] can maintain the DC-link voltage during LVRT.
2) The VSC with the current-controlled vector control can be regarded as a controlled current source, considering that the current loop bandwidth with appropriate current controller parameters is much higher than the PLL bandwidth.
3) Transmission line electromagnetic transient behaviors are neglected because of the fast dynamics.
4) The power grid is represented by an infinite bus with lumped impedance, and grid frequency dynamics are also neglected. Particular attention of this study is focused on the PLL dynamics.

A commonly used synchronous reference frame PLL (SRF-PLL) is depicted in Fig. 2(a), where ω_0 denotes the nominal frequency. Fig. 2(b) and (c) show the relationship between the PLL d-q reference frame and the infinite-bus X-Y synchronous reference frame. In the steady state, direction of the terminal voltage vector $\boldsymbol{U}$ coincides with PLL's d-axis, whereas they have different directions during dynamic processes. The included angle between the two reference frames in Fig. 2(b) [or (c)] is denoted δ and it can be accordingly obtained that

$$d\delta/dt = \omega_{pll} - \omega_g \triangleq \Delta\omega \tag{1}$$

where ω_{pll} represents the PLL frequency and ω_g represents the grid frequency, and the difference between the two is defined as $\Delta\omega$. Furthermore, according to Fig. 2(a), PLL dynamics can be described as follows,

$$d\Delta\omega/dt = d(\omega_{pll} - \omega_g)/dt = d\omega_{pll}/dt = k_p\, du_q/dt + k_i u_q \tag{2}$$

where k_p and k_i are the PLL parameters and u_q is the q-axis

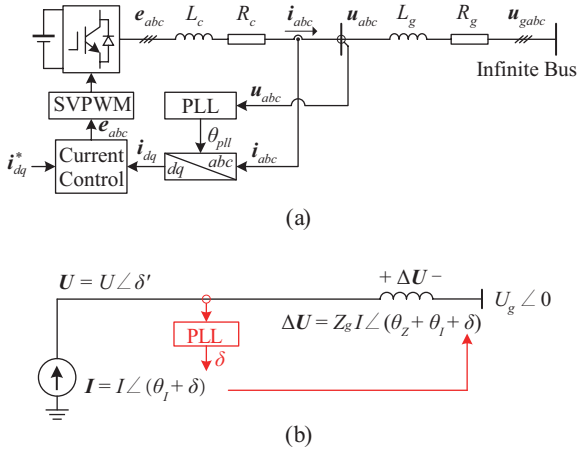

Fig. 1. Grid-tied VSC system. (a) PLL-based current control. (b) Illustration of the dynamic interaction between the PLL and the terminal voltage, where $\boldsymbol{U}$ and $\boldsymbol{I}$ are the phasors of $\boldsymbol{u}_{abc}$ and $\boldsymbol{i}_{abc}$.

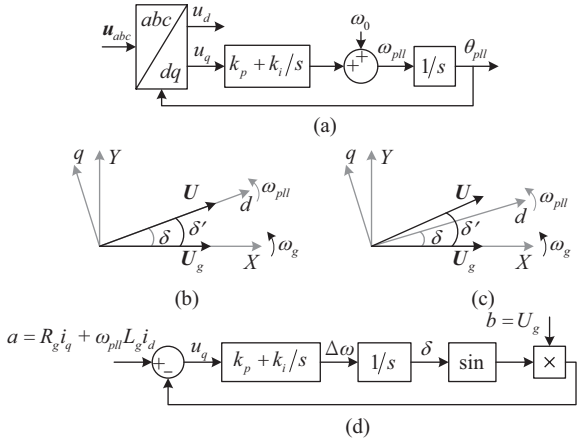

Fig. 2. (a) SRF-PLL diagram. (b) Steady-state relationship between the terminal voltage $\boldsymbol{U}$ and the two reference frames. (c) Dynamic relationship between the terminal voltage $\boldsymbol{U}$ and the two reference frames. (d) Reduced-order nonlinear system model.

voltage of the terminal voltage $\boldsymbol{u}_{abc}$.

As shown in Fig. 2(b) or (c), transforming the grid voltage $\boldsymbol{U}_g$ from the *X*-*Y* reference frame into the PLL *d*-*q* reference frame gives rise to the *d*-axis and *q*-axis voltages of $\boldsymbol{U}_g$ as follows,

$$\begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} = \begin{bmatrix} \cos\delta & \sin\delta \\ -\sin\delta & \cos\delta \end{bmatrix} \begin{bmatrix} U_g \\ 0 \end{bmatrix}. \tag{3}$$

While neglecting the electromagnetic transient behaviors of the transmission lines, the mathematical relation between the VSC terminal voltage $\boldsymbol{u}_{dq}$ and output current $\boldsymbol{i}_{dq}$ can be expressed as follows,

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} + R_g \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega_{pll} L_g \begin{bmatrix} -i_q \\ i_d \end{bmatrix} \tag{4}$$

where $\boldsymbol{u}_{dq}$ and $\boldsymbol{i}_{dq}$ are the counterparts of $\boldsymbol{u}_{abc}$ and $\boldsymbol{i}_{abc}$ transformed into the PLL *d*-*q* reference frame, respectively. Besides, R_g and L_g represent the resistive and inductive components of the lumped grid impedance. It is noted that the grid impedance is from the Thévenin equivalent circuit, therefore it would change with a transmission line ground fault [5], [28].

From (3) and (4), it can be further derived that

$$u_q = R_g i_q + \omega_{pll} L_g i_d - U_g \sin\delta \triangleq a - b\sin\delta. \tag{5}$$

From (5), it can be found that a is an offset term in u_q, which is introduced by the grid impedance voltage drop. Detailed expressions of a and b are as follows,

$$\begin{cases} a = R_g i_q + \omega_{pll} L_g i_d = Z_g I \sin(\theta_Z + \theta_I) \\ b = U_g \end{cases} \tag{6}$$

where Z_g denotes the grid impedance magnitude; I denotes the current amplitude; θ_I and θ_Z (impedance angle) are expressed as follows,

$$\boldsymbol{I} = I\angle(\theta_I + \delta),\ \theta_I = \arctan(i_q/i_d) \tag{7}$$

$$\boldsymbol{Z}_g = Z_g\angle\theta_Z,\ \theta_Z = \arctan(\omega_{pll} L_g/R_g). \tag{8}$$

The differential equations (1) and (2) combining the algebraic equation (5) constitute the reduced-order nonlinear system model, as shown in Fig. 2(d). In addition, value of the currents i_d and i_q in the model should be stated, in order to analyse the transient stability based on the model. Since the VSC system is regarded as a controlled current source, it can be considered that the output current $\boldsymbol{i}_{dq}$ is directly specified by the current references. Taking into account the unity power factor control, the pre-fault current references can be denoted as

$$\begin{aligned} i_{d\_\text{normal}} &= i_{d0} \\ i_{q\_\text{normal}} &= 0 \end{aligned} \tag{9}$$

where i_{d0} denotes the pre-fault steady-state active current, and

TABLE I
VSC Model Parameters

Parameter	Per-unit value	Parameter	Per-unit value
L_g	0.08	Residual grid voltage	0.05 or 0.10
R_g	0.30	k_p (PLL)	100
L_c	0.15	k_i (PLL)	1000
R_c	0.005	k_p (current controller)	2
i_{d_normal}	1.0	k_i (current controller)	10
i_{q_normal}	0.0	Simulation step size	5×10^{-6} s
i_{d_fault}	0.0	i_{q_fault}	−1.0

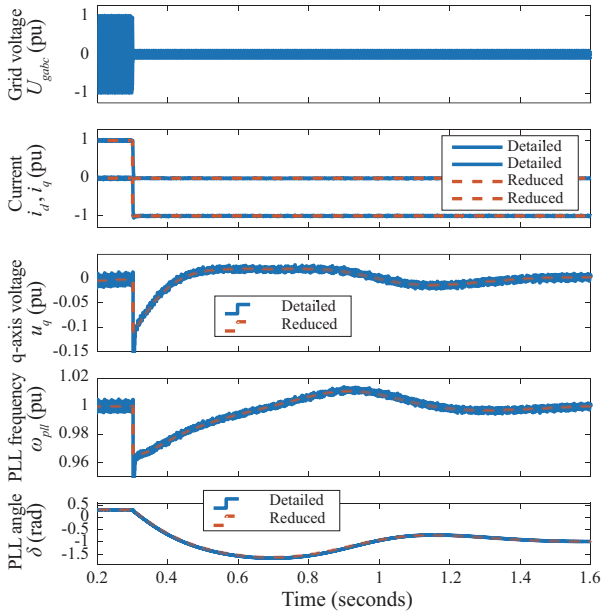

Fig. 3. Validation of the reduced-order model by comparison with the detailed model, where the grid voltage dips to 0.10 p.u.

the VSC outputs zero reactive current under normal operating conditions. The output current during LVRT conditions is directly determined by the grid codes. For example, i_q* is set to –1.0 p.u. if the PCC (point of common coupling) voltage dips larger than 50% [3] and i_d^* is often set to zero considering the output current capability, i.e.,

$$\begin{aligned} i_{d\_\text{fault}} &= 0 \\ i_{q\_\text{fault}} &= -1\,\text{p.u.} \end{aligned} \tag{10}$$

To demonstrate the adequacy of the developed reduced-order nonlinear model, the model is validated by comparing its time-domain responses with those of the detailed electromagnetic transient (EMT) model. Parameters of the detailed model are summarized in Table I.

Figs. 3 and 4 give the simulation results. In Fig. 3, the grid voltage dips from the nominal condition to 0.10 p.u. at 0.3 s, and the VSC output current quickly changes in the meantime according to the reference. Specifically, the reactive current instantaneously changes from 0 to –1 p.u., and the active current changes from i_{d0} to 0. Fig. 3 shows that the PLL is able to quickly resynchronize with the grid after the grid voltage sag.

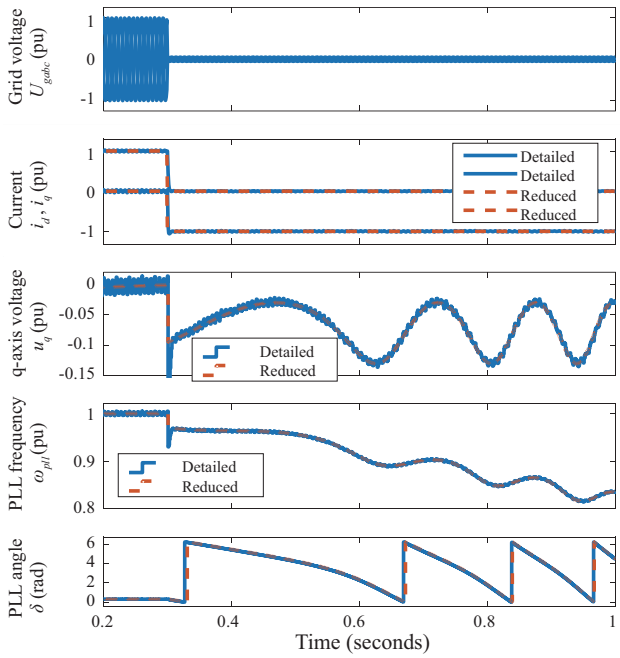

Fig. 4. Validation of the reduced-order model by comparison with the detailed model, where the grid voltage dips to 0.05 p.u., making the VSC system become unstable.

In Fig. 4, a more severe grid voltage sag than that in Fig. 3 occurs, i.e., only 0.05 p.u. residual grid voltage. Simulation results in Fig. 4 indicate that the PLL is not able to resynchronize with the grid after the grid voltage sag. Hence, the VSC system becomes unstable.

From Figs. 3 and 4, it can also be observed that the time-domain responses of the reduced-order model and those of the detailed EMT model are highly consistent, therefore verifying the adequacy of the reduced-order model. Based on the reduced-order model, the transient stability analysis can be easily performed.

III. Transient Stability Analysis

The reduced-order model is comprised of (1), (2), and (5). (1) and (2) describe the PLL dynamic nonlinear characteristic, whereas the zero-crossing point of (5), i.e., $u_q = 0$, determines the steady-state equilibrium point of the system. The transient stability of the system will be analysed from two points of views, which are the equilibrium point analysis and the dynamic characteristic analysis.

A. Steady-State Equilibrium Point Analysis

According to (5), the steady-state equilibrium point of the VSC system satisfies the condition that

$$u_q = a - b\sin\delta = 0. \tag{11}$$

Several examples of the equilibrium point are depicted in Fig. 5, where there are two types of zero-crossing points. The small-signal stability analysis is performed to distinguish between the unstable equilibrium points (UEPs) and the stable

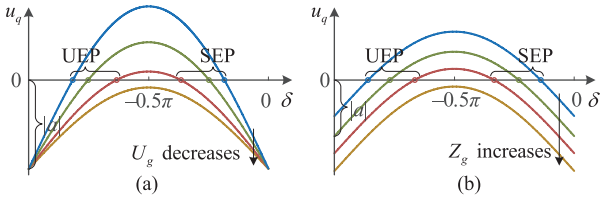

Fig. 5. Illustration of equilibrium points. (a) Grid voltage U_g decreases. (b) Grid impedance magnitude Z_g increases.

equilibrium points (SEPs). The small-signal state variables $\tilde{\delta}$ and $\Delta\tilde{\omega}$ can be denoted as follows,

$$\begin{cases} \delta = \delta_0 + \tilde{\delta} \\ \Delta\omega = 0 + \Delta\tilde{\omega}. \end{cases} \tag{12}$$

Based on the nonlinear model consisting of (1), (2), and (5), and the equilibrium point in (12), the small-signal model can be derived, as shown in (13).

$$\begin{bmatrix} \dot{\tilde{\delta}} \\ \Delta\dot{\tilde{\omega}} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\dfrac{k_i U_g \cos\delta_0}{1 - k_p L_g i_d} & -\dfrac{k_p U_g \cos\delta_0 - k_i L_g i_d}{1 - k_p L_g i_d} \end{bmatrix} \begin{bmatrix} \tilde{\delta} \\ \Delta\tilde{\omega} \end{bmatrix} \tag{13}$$

Considering that $1 - k_p L_g i_d > 0$ almost always holds true, to meet the small-signal stability criterion, the following conditions should be satisfied,

$$\cos\delta_0 > 0 \tag{14}$$

$$k_p U_g \cos\delta_0 > k_i L_g i_d. \tag{15}$$

(15) can further give rise to

$$\cos\delta_0 > k_i L_g i_d / (k_p U_g) \approx 0 \tag{16}$$

which is approximately equivalent to (14). Thus, (14) indicates the zone where SEPs are located, as shown in Fig. 5.

From Fig. 5(a), it can be observed that the curve amplitude b decreases along with the decrease of the grid voltage U_g (because $b = U_g$). In Fig. 5(b), the absolute value of the offset term $|a|$ increases along with the increase of the grid impedance magnitude Z_g.

If $|a|$ is larger than b, caused by a quite severe grid sag or a considerable post-fault grid impedance, there will be no equilibrium point. Then, it will be impossible to maintain the stability of the system whether PLL [29] or frequency-locked loop (FLL) [30], [31] is adopted. The critical equilibrium point corresponds to $|a| = b$.

From Fig. 5, it can also be found that the smaller the absolute offset term $|a|$, and the larger the residual grid voltage amplitude b, the higher the stability margin. Besides, (6) indicates that four variables associated with the output current and the grid impedance have impacts on the offset term. Specifically, both a large current amplitude I and a large grid impedance magnitude

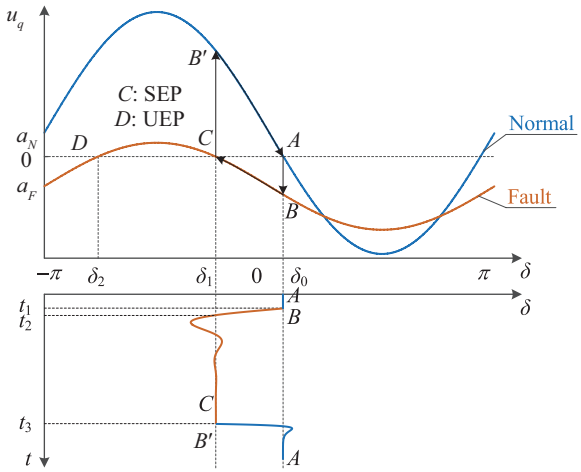

Fig. 6. Illustration of the dynamic synchronization processes of a VSC subjected to a grid voltage sag at t_1 and grid voltage recovery at t_3. Note that a_N and a_F denote the offset terms corresponding to the normal and fault operating conditions, respectively.

Z_g are able to facilitate a large offset term, which accordingly shrinks the stability margin.

When it comes to the relation between the offset term and θ_I or θ_Z, (6) manifests that the relation is not linear. In particular, the offset term equals zero only if $\theta_I + \theta_Z = 0$. In general, $\theta_I = -0.5\pi$ when $i_d = 0$ is set during LVRT. In this regard, the offset term equals zero only if $\theta_Z = 0.5\pi$. Nonetheless, θ_Z is random in actual grid fault scenarios, which is determined by actual fault points and short-circuit resistance.

B. Resynchronization Principle Analysis

Without taking into account the impact of the grid impedance on the PLL, grid synchronization principle as well as dynamic performance of PLLs have been extensively investigated in previous studies [29]. However, it is not enough to guarantee the transient stability of the VSC systems, especially for ones connected to the high-impedance weak grid. Here, from the perspective of spatial vector tracking relation, a resynchronization principle analysis of the VSCs during LVRT is conducted to clarify the stability principle associated with PLL's nonlinearity by considering the impact of the grid impedance.

In Fig. 2(d), the grid impedance introduces the offset term a into the input of the PLL. There is no doubt that the offset term makes the PLL no longer ideal since the input signal u_q is no longer a standard unbiased sinusoidal function related to δ. Therefore, it has effects on the synchronization performance of the PLL.

Fig. 6 illustrates an example of the dynamic synchronization process of a VSC subjected to a grid voltage sag and also a grid voltage recovery. When the grid voltage sag occurs at t_1, the operating curve switches from the blue curve (Normal condition) to the orange curve (Fault condition), and the operating point steps from A to B. There are two steady-state equilibrium points, i.e., C and D, after the grid voltage sag. Note that point C is stable whereas D is unstable. Then, the

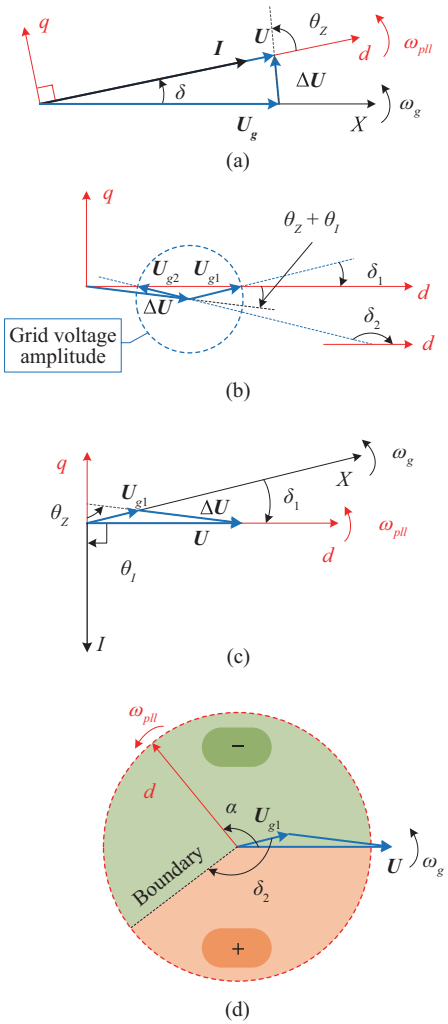

Fig. 7. (a) Spatial vector relation in the pre-fault steady state. (b) There are two steady-state equilibrium points after the grid voltage sag, i.e., $\boldsymbol{U}_{g1}$ (stable) and $\boldsymbol{U}_{g2}$ (unstable), where $\delta_1 + \delta_2 = -\pi$. (c) Spatial vector relation corresponding to the post-fault stable steady-state equilibrium point. (d) Dynamic synchronization process illustration.

operating point moves towards C because B is not a steady-state point, accompanied by a decelerating process of the PLL. The operating point crosses C at t_2, thereafter the PLL frequency begins to increase due to u_q becomes positive. Finally, the operating point reaches the equilibrium point C due to the damping effects. It is supposed that δ would not exceed the UEP D in the accelerating process, otherwise the operating point will fall into the adjacent inversely regulating areas. When the grid fault is cleared at t_3, similar dynamic synchronization process is performed.

Considering the impact of the grid impedance, resynchronization principle of the VSC is elaborated using spatial vector tracking relation. Fig. 7(a) shows the pre-fault steady-state spatial vector relation, where $\omega_g = \omega_{pll}$. Fig. 7(b) shows that there are two steady-state equilibrium points after the grid voltage sag. The grid impedance voltage drop $\Delta\boldsymbol{U}$ is uniquely identified with respect to the d-q reference frame, provided that both grid voltage impedance $\boldsymbol{Z}_g$ and VSC output current

I are determined. The dashed circle denotes the grid voltage amplitude U_g, resulting in two intersections with the *d*-axis, hence corresponding to two grid voltage vectors, $\boldsymbol{U}_{g1}$ and $\boldsymbol{U}_{g2}$. It has been known that only the equilibrium point corresponding to $\boldsymbol{U}_{g1}$ is stable.

Fig. 7(c) illustrates the post-fault steady-state vector relation, where $\omega_g = \omega_{pll}$. As shown in Fig. 7(d), the goal of the PLL is to track the determined voltage vector $\boldsymbol{U}$, i.e., the post-fault steady-state terminal voltage vector, during the dynamic synchronization process. If the *d*-axis of the PLL reference frame surpasses the target vector $\boldsymbol{U}$ and the lead angle α is within the boundary, the PLL will decelerate. On the flip side, if the *d*-axis lags behind the target vector $\boldsymbol{U}$ and the lag angle is within the boundary, the PLL will accelerate.

It should be noted that the accelerating and decelerating areas are mismatched because of the offset term *a* in the PLL input signal u_q. Owing to the mismatched accelerating and decelerating areas, the lead angle α might become so large that it traverses the boundary and then falls into the adjacent inversely regulating areas. As a result, an additional round of tracking path is caused, which, unfortunately, leads to the accelerating and decelerating areas being further mismatched. Therefore, the tracking capability of the PLL is further deteriorated, and loss of synchronism (LOS) potentially occurs.

To sum up, the coordinate transformation (3) incorporates sinusoidal functions, hence introducing both periodicity and nonlinearity. The periodicity leads to the accelerating and decelerating areas being adjacent to each other. The nonlinearity causes the PLL dynamic performance inconsistency at different operating points. Given that the developed nonlinear model is second-order, it is feasible to elaborate the dynamic performance by using the concept of inertia and damping.

C. Damping Characteristic Analysis

Transform the developed nonlinear model into a typical form of motion equation as follows,

$$\begin{aligned} J_{eq}\, d\omega_{pll}/dt &= u_q - D_{eq}(\omega_{pll} - \omega_g) \\ d\delta/dt &= \Delta\omega \end{aligned} \tag{17}$$

where the equivalent inertia and damping coefficients are

$$\begin{aligned} J_{eq} &= (1 - k_p L_g i_d)/k_i \\ D_{eq} &= k_p U_g \cos\delta/k_i,\ k_i \neq 0. \end{aligned} \tag{18}$$

Actually, since $k_p L_g i_d << 1$, (18) can be further simplified as

$$\begin{aligned} J_{eq} &\approx 1/k_i \\ D_{eq} &= k_p U_g \cos\delta/k_i,\ k_i \neq 0. \end{aligned} \tag{19}$$

As shown in Fig. 6, the damping term plays an important role in weakening and gradually suppressing the oscillation during the dynamic synchronization process. If k_p equals zero, then D_{eq} will become zero, and it can be accordingly believed that the damping effect actually originates from the proportional unit of the PLL. It should be noted that [16]–[18] employed the concept of equal area criterion to analyse the stability of grid-tied VSCs based on (17). Since the damping term was neglected, the results were relatively conservative.

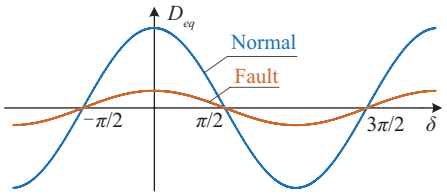

Fig. 8. Change of D_{eq} with δ, where $D_{eq} > 0$ corresponds to positive damping zones whereas $D_{eq} < 0$ corresponds to negative zones.

According to (19), it can be found that a small k_p, a large k_i, and a small U_g are able to make the damping effect weak, therefore deteriorate the stability. Especially, the sign of the damping coefficient is directly decided by the PLL angle δ. Fig. 8 shows the relation between D_{eq} and δ. Once the operating point enters negative damping zones, loss of synchronism (LOS) is very likely to occur. In addition, (19) seemly reveals that the grid impedance has no effect on the damping coefficient. However, it should be noted that grid impedance is able to produce impacts on the PLL angle δ, accordingly have impacts on the damping characteristics.

D. Inertia Characteristic Analysis

From (19), it can be found that the equivalent inertia coefficient J_{eq} is directly related to the integral coefficient k_i of the PLL. Specifically, J_{eq} is inversely proportional to k_i. Therefore, a large k_i is able to lead to a small J_{eq}, which, as a result, might cause potential oscillations with large amplitude. In other words, a large k_i is harmful to the stability of grid-tied VSC during LVRT.

IV. Simulation Results

Simulations are conducted to verify the above results regarding the impacts of circuit parameters and controller parameters on the transient stability of VSCs. Simulations are performed based on a VSC switching-cycle average model with parameters given in Table I. On this basis, bandwidth of the PLL and the current loop can be calculated.

A. Different Grid Voltage Sags

Simulating three degrees of grid voltage sags, i.e., 85%, 90%, and 95%, the simulation results are shown in Fig. 9. It can be found that the VSC cannot resynchronize with the grid when the 95% grid voltage sag occurs. Actually, it is because that there is no equilibrium point after the grid voltage sag.

Besides, when the grid voltage dips 85% and 90%, it can be confirmed that there are indeed equilibrium points, and the system are stable in these two cases. It can also be found that a large residual grid voltage can not only help the present of post-fault equilibrium points, but also facilitate the damping effect for a fast convergence.

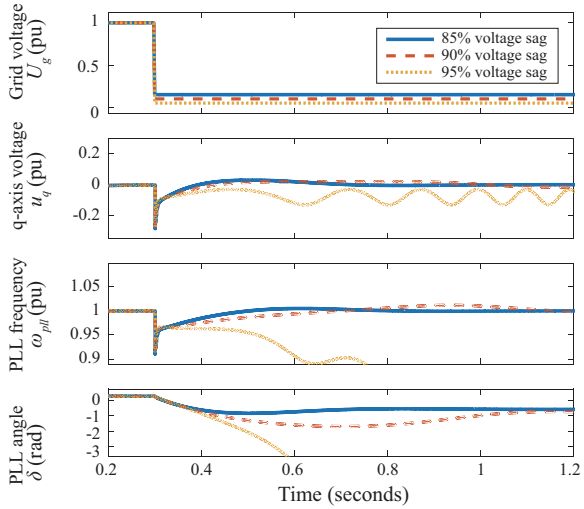

Fig. 9. Simulation results of 85%, 90%, and 95% grid voltage sags.

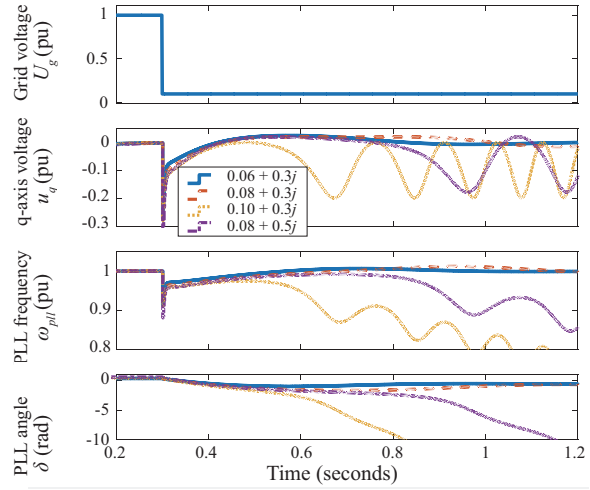

Fig. 10. Simulation results with different post-fault grid impedances, including $\boldsymbol{Z}_g = 0.06 + 0.30j$, $0.08 + 0.30j$, $0.10 + 0.30j$, and $0.08 + 0.50j$.

To sum up, a large residual grid voltage after grid faults contributes to the enhancement of the transient stability.

B. Different Grid Impedance

Simulating four groups of grid impedance, i.e., $\boldsymbol{Z}_g = 0.06 + 0.30j$, $0.08 + 0.30j$, $0.10 + 0.30j$, and $0.08 + 0.50j$ after the same 90% grid voltage sag with the same current reference $i_{d\_\text{fault}} + ji_{q\_\text{fault}} = 0.0 - 1.0j$, the simulation results are shown in Fig. 10. With the increase of the resistive component, it can be observed that the equilibrium point probably becomes absent, thus the system tends to become unstable after the fault.

Besides, Fig. 10 shows that the increase of the inductive component is also able to deteriorate the stability. Although the inductive component of the grid impedance has no effect on the existence of equilibrium points, it is able to affect the initial system state. Specifically, a larger inductive component of the grid impedance makes the initial system state move away from the post-fault equilibrium point, hence leading to a larger accelerating area, as shown in Fig. 6.

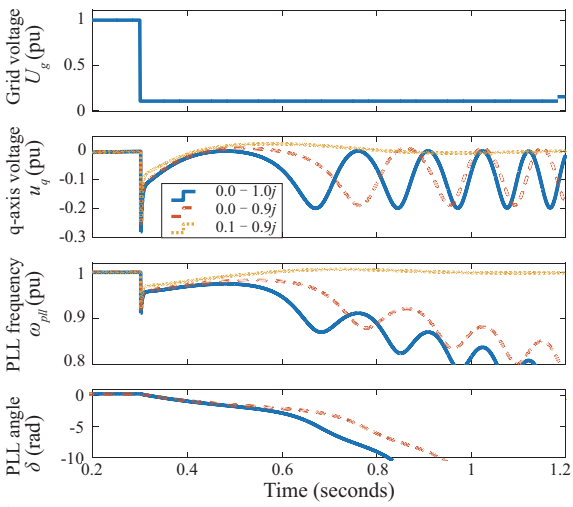

Fig. 11. Simulation results with different current references, including $0.0 - 1.0j$, $0.0 - 0.9j$, and $0.10 - 0.9j$.

To sum up, the transient stability margin is reduced with the increase of grid impedance, either in the resistive or the inductive component. In other words, the weak connection between VSCs and the power grid is indeed harmful to the transient stability of VSCs.

C. Different Current References

Simulating three groups of current reference, i.e., $i_{d\_\text{fault}} + ji_{q\_\text{fault}} = 0.0 - 1.0j$, $0.0 - 0.9j$, and $0.10 - 0.9j$ after the same 90% grid voltage sag with the same post-fault grid impedance $0.1 + 0.3j$, the simulation results are shown in Fig. 11. For the first group of current reference, there exists a critical equilibrium point. The system becomes unstable because of overshoot. For the second group, although the stable equilibrium point is recreated by reducing the reactive current and thereby reducing the offset term in the q-axis voltage u_q, the system still becomes unstable due to the small stability margin. Furthermore, an additional active current is generated in the third group, which further reduces the offset term in u_q, and the system accordingly becomes stable.

To sum up, a small reactive current as well as a nonzero active current is conducive to improving the stability margin. It is because they can help to decrease the offset term in the q-axis voltage.

D. Different PLL Parameters

Figs. 12 and 13 show the impacts of PLL parameters on the transient stability. In Fig. 12, the system with $k_p = 80$ becomes unstable after the grid voltage sag, since a small proportional coefficient gives rise to a small damping coefficient [see (19)], therefore a poor damping effect. The stability is improved with the increase of the PLL proportional coefficient.

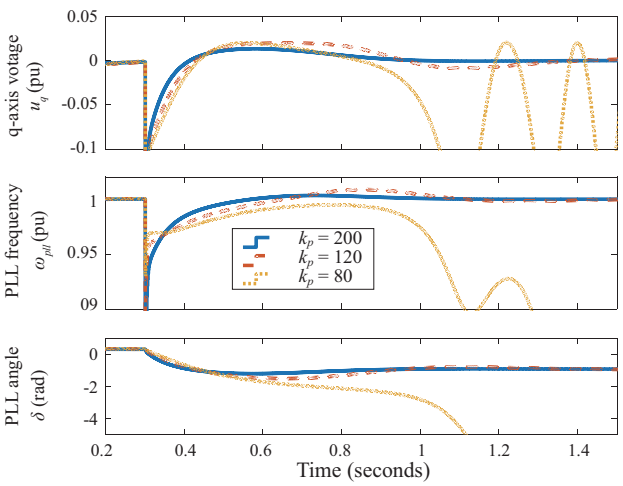

Fig. 12. Simulation results with different PLL proportional coefficients, including k_p = 200, 120, and 80, but the same integral coefficient k_i = 1000.

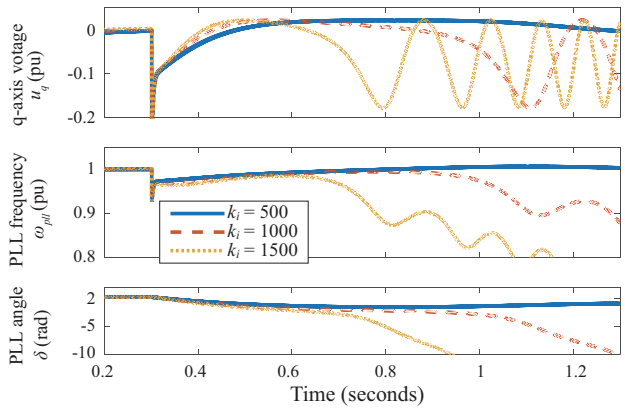

Fig. 13. Simulation results with different PLL integral proportional coefficients, including k_i = 500, 1000, and 1500, but the same proportional coefficient k_p = 80.

Fig. 13 shows that the stability is enhanced with the decrease of the PLL integral coefficient. Actually, it is because that a small integral coefficient yields a large damping coefficient. To sum up, the above results completely coincide with the findings from (19), i.e., both a large k_p and a small k_i during grid voltage sags, are able to make the damping effect strong and therefore improve the transient stability.

It should be noted that the above results are only valid under the condition of ignorable current control dynamics. Once the PLL bandwidth overlaps with the current control bandwidth, both PLL dynamics and current control dynamics should be taken into account while analysing the transient stability.

V. Experimental Results

The stability analysis has also been verified in an actual three-phase 1.0 kW PWM converter system with a DSP digital control platform. The setup of the experimental system is shown in Fig. 14 with parameters given in Table II. Note that both the resistive and inductive components of the grid impedance are large enough to mimic quite weak connection between the VSC and the grid.

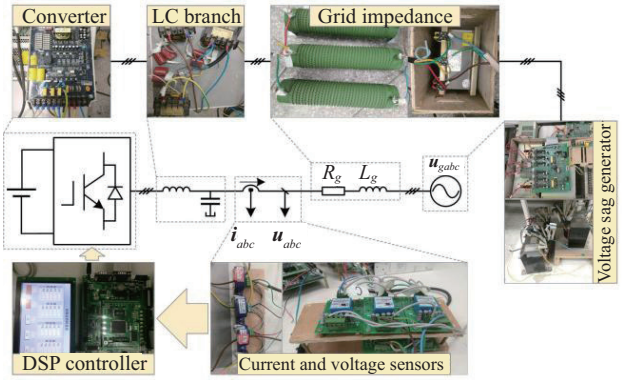

Fig. 14. Experimental setup.

TABLE II
Experimental System Parameters

Capability	1 kW	
Nominal line-to-line voltage	170 V	
Grid resistance	3.5 Ω	0.121 p.u.
Grid inductance	20 mH	0.217 p.u.

From the viewpoint of enhancing the transient stability of grid-tied VSCs, regulating the current references and PLL parameters is a very easy way. For this purpose, two experimental cases are set to further verify: 1) the impact of current references and 2) the impact of PLL parameters on the transient stability of grid-tied VSCs.

A. Impact of Current References

The main attention of this case is focused on the active current reference, considering that there is almost no strict requirement on the active current output in most of the current LVRT codes. In Fig. 15(a), (b), and (c), the active current references are 0.0, 1.0, and 1.6 A, respectively, with the same reactive current reference of –5.1 A during the grid voltage sag from 170 V to 14.2 V. As shown in Fig. 15(a) or (b), the system is unstable with the active current of 0.0 A or 1.0 A, because there is no equilibrium point. Note that k_i is set to zero here, therefore the PLL frequencies undergo continuous oscillations instead of gradual deviations. In Fig. 15(c), the system is stable when the equilibrium point is recreated by a larger active current than that in Fig. 15(a) and (b).

B. Impact of PLL Parameters

The main attention of this case is focused on the PLL integral coefficient as an example. In Fig. 16(a), (b), and (c), the PLL integral coefficients are 2000, 1500, and 1000, respectively, with the same PLL proportional coefficient of 25 during the grid voltage sag. From Fig. 16, it is noticed that the stability is enhanced with the decrease of the PLL integral coefficient, due to the increase of the damping effect. The experimental results accordingly further verify the stability analysis.

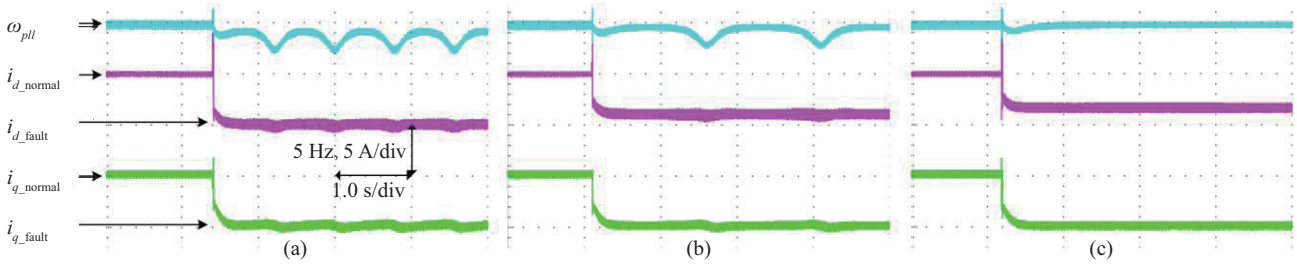

Fig. 15. Experimental results with different active current references during a grid fault. (a) $i_{d\_fault} = 0.0$ A. (b) $i_{d\_fault} = 1.0$ A. (c) $i_{d\_fault} = 1.6$ A.

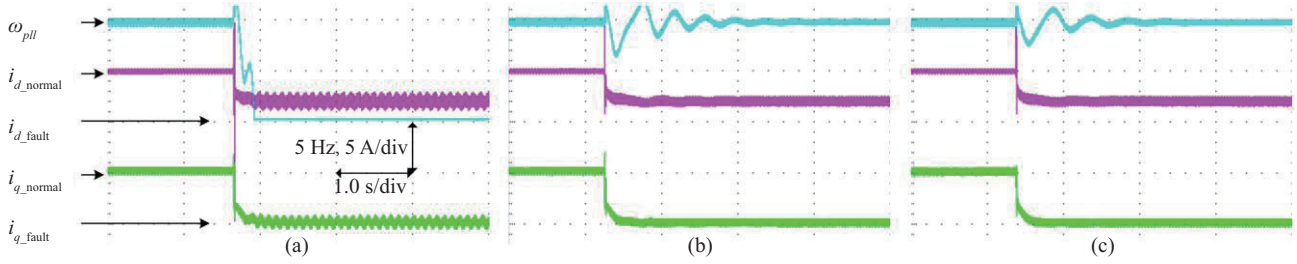

Fig. 16. Experimental results with different PLL integral coefficients during a grid fault. (a) $k_i = 2000$. (b) $k_i = 1500$. (c) $k_i = 1000$.

VI. Conclusions

Loss of synchronism of the grid-tied VSCs probably occurs during severe grid voltage sags. This paper develops a reduced-order nonlinear model to describe the dynamic synchronization process of VSCs. Based on the model, it is clarified that the post-fault grid impedance voltage drop has a significant effect on the transient stability, since it introduces an offset term in the *q*-axis voltage (i.e., PLL input signal). By determining the target terminal voltage vector, the resynchronization principle is analysed from the PLL point of view, according to spatial vector tracking relation. Moreover, from the perspective of equilibrium points and dynamic characteristics, the impacts of grid parameters, current references, and PLL parameters on the transient stability are analysed and verified. The results of this study could be conducive to guiding the designs of current references and PLL parameters for efficiently addressing grid faults.

References

[1] G. Qi, "Improved control strategy of interlinking converters with synchronous generator characteristic in islanded hybrid AC/DC microgrid," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 149–158, Jun. 2017.

[2] H. Geng, C. Liu, and G. Yang, "LVRT capability of DFIG-based WECS under asymmetrical grid fault condition," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2495–2509, 2013.

[3] Grid code-high and extra high voltage, E. ON Netz GmbH, 2006. Tech. Rep., [EB/OL].

[4] M. N. I. Sarkar, L. G. Meegahapola, and M. Datta, "Reactive power management in renewable rich power grids: A review of grid-codes, renewable generators, support devices, control strategies and optimization algorithms," *IEEE Access*, vol. 6, pp. 41458–41489, 2018.

[5] S. Ma, H. Geng, L. Liu, G. Yang, and B. C. Pal, "Grid-synchronization stability improvement of large scale wind farm during severe grid fault," *IEEE Trans. Power Syst.*, vol. 33, no. 1, pp. 216–226, 2018.

[6] H. Geng, L. Liu, and R. Li, "Synchronization and reactive current support of PMSG based wind farm during severe grid fault," *IEEE Trans. Sustain. Energy*, vol. 9, no. 4, pp. 1596–1604, Oct. 2018.

[7] S. Ma, H. Geng, G. Yang, and B. Liu, "Experimental validation of adaptive current injecting method for grid-synchronization improvement of grid-tied REGS during short-circuit fault," in *Proc. IPEC-Niigata*, 2018.

[8] J. Hu, B. Wang, W. Wang, H. Tang, Y. Chi, and Q. Hu, "Small signal dynamics of DFIG-based wind turbines during riding through symmetrical faults in weak AC grid," *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 720–730, 2017.

[9] B. Wen, D. Dong, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 26–38, 2016.

[10] M. Davari, Y. A.-R. I. Mohamed, "Robust vector control of a very weak grid-connected voltage-source converter considering the phase-locked loop dynamics," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 977–994, 2017.

[11] X. He, H. Geng, and G. Yang, "Equivalent modelling of wind farm for small-signal stability analysis in weak power system," *Journal of Engineering*, vol. 2017, no. 13, pp. 1399–1393, 2017.

[12] Ö. Göksu, R. Teodorescu, C. L. Bak, F. Iov, and P. C. Kjær, "Instability of wind turbine converters during current injection to low voltage grid faults and PLL frequency based stability solution," *IEEE Trans. Power Syst.*, vol. 29, no. 4, pp. 1683–1691, 2014.

[13] D. Dong, B. Wen, D. Boroyevich, and P. Mattavelli, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 310–321, 2015.

[14] H. Yuan, H. Xin, K. Wang, Z. Wang, L. Xu, and H. Xie, "Instability mechanism analysis of inverters connected to weak grid during severe voltage sag on remote grid side," *Automation of Electric Power Systems*, vol. 42, no. 22, pp. 38–43, 2018.

[15] H. Yuan, H. Xin, L. Huang, Z. Wang, and D. Wu, "Stability analysis and enhancement of type-4 wind turbines connected to very weak grids under severe voltage sags," *IEEE Trans. Energy Convers.*, in press.

[16] Q. Hu, J. Hu, H. Yuan, and H. Tang, "Synchronizing stability of DFIG-based wind turbines attached to weak AC grid," in *Proc. ICEMS*, 2014, pp. 2618–2624.

[17] C. Zhang, X. Cai and Z. Li, "Transient stability analysis of wind turbines with full-scale voltage source converter," *CSEE J. Power Energy Syst*., vol. 37, no. 14, pp. 4018–4026, Jul. 2017.
[18] G. Han, C. Zhang, and X. Cai, "Mechanism of frequency instability of full-scale wind turbines caused by grid short circuit fault and its control method," *Trans. China Electrotechnical Society*, vol. 33, no. 10, pp. 2167–2175, May 2018.
[19] H. Wu and X. Wang, "Design-oriented transient stability analysis of grid-connected converters with power synchronization control," *IEEE Trans. Ind. Electron*., in press.
[20] H. Wu and X. Wang, "Transient angle stability analysis of grid-connected converters with the first-order active power loop," in *Proc. 2018 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018.
[21] H. Wu and X. Wang, "Transient stability impact of the phase-locked loop on grid-connected voltage source converters," in *Proc. 2018 Int. Power Electron. Conf. (IPEC-Niigata 2018 -ECCE Asia)*, May 2018.
[22] H. Wu and X. Wang, "An adaptive phase-locked loop for the transient stability enhancement of grid-connected voltage source converters," in *Proc. 2018 IEEE Energy Convers. Congr. Expo. (ECCE)*, Sept. 2018.
[23] M. Kabalan, P. Singh, and D. Niebur, "Nonlinear Lyapunov stability analysis of seven models of a DC/AC droop controlled inverter connected to an infinite bus," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 772–781, Jan. 2019.
[24] Z. Shuai, C. Shen, X. Liu, Z. Li, Z. J. Shen, "Transient angle stability of virtual synchronous generators using Lyapunov's direct method," *IEEE Trans. Smart Grid*, in press.
[25] B. Shakerighadi, E. Ebrahimzadeh, F. Blaabjerg, and C. Leth Bak, "Large-signal stability modeling for the grid-connected VSC based on the Lyapunov method," *Energies*, vol. 11, no. 10, pp. 2533, Sept. 2018.
[26] M. Kabalan, P. Singh, and D. Niebur, "Large signal Lyapunov-based stability studies in microgrids: A review," *IEEE Trans. Smart Grid*, vol. 8, no. 5, pp. 2287–2295, Sept. 2017.
[27] X. He, H. Geng, and G. Yang, "Synchronization stability analysis of grid-tied power converters under severe grid voltage sags," in *Proc. IEEE PEAC*, 2018.
[28] M. G. Taul, X. Wang, P. Davari, and F. Blaabjerg, "Grid synchronization of wind turbines during severe symmetrical faults with phase jumps," in *Proc. 2018 IEEE Energy Convers. Congr. Expo. (ECCE)*, Sept. 2018.
[29] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron*., vol. 32, no. 3, pp. 1894–1907, Mar. 2017.
[30] X. He, H. Geng, G. Yang, "A generalized design framework of notch filter based frequency-locked loop for three-phase grid voltage," *IEEE Trans. Ind. Electron*., vol. 65, no. 9, pp. 7072–7084, 2018.
[31] X. He, H. Geng, and G. Yang, "Reinvestigation of single-phase FLLs," *IEEE Access*, vol. 7, pp. 13178–13188, 2019.

Xiuqiang He received the B.S. degree in automatic control from the Department of Automation, Tsinghua University, Beijing, China, in 2016. He is currently working toward the Ph.D. degree in control science and engineering at the Department of Automation, Tsinghua University.

His current research interests include grid-synchronization stability as well as transient stability of power electronic converters, and dynamic equivalent modeling of large-scale distributed generation systems.

Mr. He was a recipient of the Chinese National Scholarship, and the IEEE International Power Electronics and Application Conference and Exposition (PEAC) Excellent Paper Award in 2018.

Hua Geng received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2003, and the Ph.D. degree in control theory and application from Tsinghua University, Beijing, China, in 2008.

From 2008 to 2010, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He joined the Department of Automation, Tsinghua University, in June 2010, where he is currently an Associate Professor. His current research interests include advanced control of power electronics and renewable energy conversion systems.

Dr. Geng serves as an editor of *IEEE Transactions on Energy Conversion*, an associate editor of *IEEE Transactions on Industry Applications* and an associate editor of *Chinese Journal of Electrical Engineering*.

Shaokang Ma received the B.S. degree from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 2012, and the M.S. degree in 2015 from the Department of Automation, Tsinghua University, Beijing, China, where he has been working toward the Ph.D. degree since 2015.

His current research interests include distribution generation systems, renewable energy conversion systems, and digital control systems.

All-Silicon 99.35% Efficient Three-Phase Seven-Level Hybrid Neutral Point Clamped/ Flying Capacitor Inverter

Jon Azurza Anderson, Eli J. Hanak, Lukas Schrittwieser, Mattia Guacci, Johann W. Kolar, and Gerald Deboy

***Abstract*—With the increasing use of photovoltaic systems, a large demand for efficient, power-dense and lightweight grid-interface inverters is arising. Accordingly, new concepts like multi-level converters, which are able to reduce the converter losses while still keeping a low construction volume, have to be investigated. The hybrid seven-level topology analyzed in this paper comprises an active neutral point clamped stage, followed by a flying capacitor stage. Compared to a pure flying capacitor converter, the combination of these two stages allows to save more than half of the capacitor volume, while still having the same requirement for the output filter stage, and hence, the same output filter volume. Moreover, the topology employs low-voltage devices and ensures low conduction and switching losses, resulting in a higher efficiency. The principle of operation of the system is briefly reviewed, and based on a detailed component modeling, an efficiency vs. power density optimization is carried out, for which switching loss measurements of state-of-the-art 200 V semiconductors are performed. From the optimization, a high-efficiency design is selected and the practical hardware realization is discussed. The simulation and optimization results are then verified by realizing an all-silicon 99.35% efficient three-phase seven-level system, featuring a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3), a gravimetric power density of 3.2 kW/kg, and fulfilling CISPR Class A EMI requirements. Finally, it is shown that an all-silicon realization with next generation silicon switches can achieve 99.5% efficiency with the same hardware, and 99.6% with commercial state-of-the-art GaN switches.**

***Index Terms*—Flying capacitor converter, hybrid active neutral point converter, multi-level, PV inverter, ultra-high efficiency.**

I. Introduction

As photovoltaic (PV) energy generation provides a continuously increasing share to the net electricity supply [1], [2], there is a clear demand for power electronics with high efficiency, high power density, low weight and low costs [3]–[6]. For PV systems with high capacity factors, which are in operation for many hours a day, a high energy conversion efficiency is of major importance [7]. With the goal of exploring the efficiency limits, this paper presents an ultra-efficient multi-level three-phase inverter solution designed for a typical PV installation, as conceptually shown in Fig. 1, targeting a peak efficiency of 99.5% for a nominal power of 10 kW.

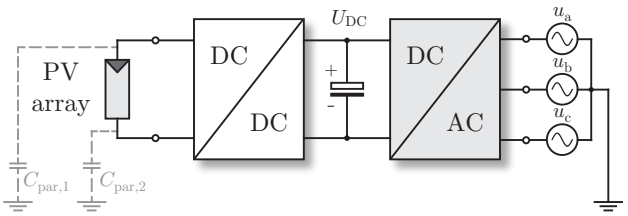

Fig. 1. System overview for transformerless transfer of PV power into the low-voltage three-phase grid (400 V_{rms}, line-to-line). The PV array is typically followed by a DC/DC converter for maximum power point (MPP) tracking and a three-phase PWM inverter (highlighted), which is the focus of this paper.

When aiming for ultra-efficient converters, the trade-off with respect to losses and volume between active (power semiconductors) and passive (magnetic and capacitive) components has to be evaluated in detail. As three-phase converters are typically hard-switched, an optimum between conduction and switching losses that favors large die areas and low switching frequencies exists [8]. However, low switching frequencies lead to bulky magnetic components. This contradiction can be solved by the use of multi-level topologies like the flying capacitor converter (FCC), illustrated in Fig. 2(a) for the case of seven levels. Multi-level converters reduce the inductance requirement of the AC-side inductors for a given current ripple amplitude quadratically with respect to the number of levels, due to the multi-level output voltage characteristic and the increase of the effective switching frequency, leading to smaller and more efficient magnetic components [9], [10]. Additionally, multi-level converters take advantage of low-voltage power MOSFETs, featuring a higher hard-switching figure of merit (FOM) compared to high-voltage power semiconductors [11]. To achieve a multi-level output voltage characteristic with an FCC, capacitors carrying an integer multiple of the lowest cell voltage are alternatingly connected to the output during operation. However, the capacitance requirement of the flying capacitors (FCs), driven by the need to constrain the switching frequency voltage ripple across them, is directly proportional to the load current (and hence, output power) and inversely proportional to the switching frequency [9]. Accordingly, ultra-high power densities can be achieved at the expense of an efficiency reduction by using high switching frequencies (in the hundreds of

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J. Azurza Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, and J. W. Kolar are with the Power Electronic Systems Laboratory (PES), ETH Zurich, Switzerland (e-mail: azurza@lem.ee.ethz.ch).

G. Deboy is with Infineon Technologies Austria AG, Villach, Austria.

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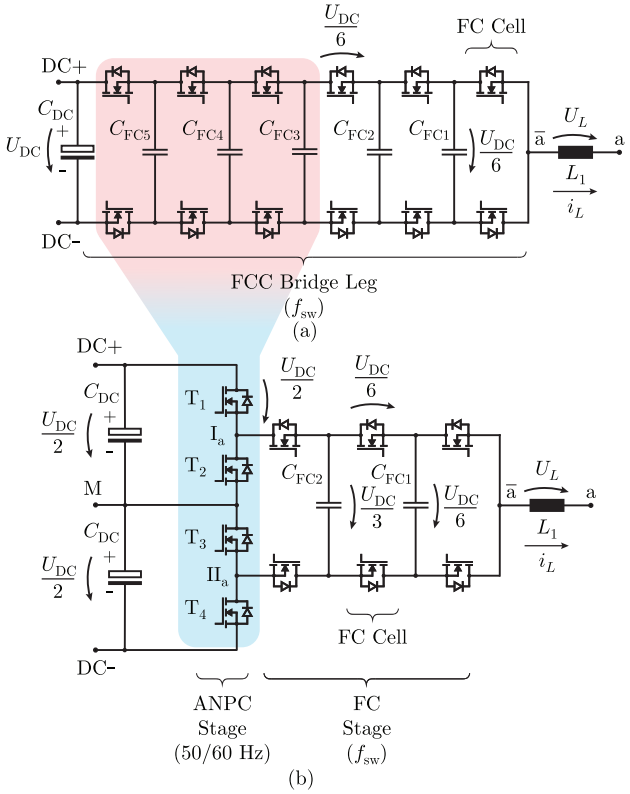

Fig. 2. Circuit schematic of a 7L-FCC bridge-leg, which is purely composed of low-voltage semiconductors operated at switching frequency (a) and the 7L-HANPC bridge-leg structure, i.e., a hybrid approach composed of an ANPC stage with semiconductors switching at 50/60 Hz, and an FC stage, with semiconductors operating at switching frequency (b). Both arrangements are shown for phase a of the three-phase (phases a, b, c) inverter topology.

TABLE I
INVERTER SPECIFICATIONS

P_{nominal}	10 kW
$P_{\text{rated, max}}$	12.5 kW
$U_{\text{dc, nominal}}$	720 V
U_{ac}	400 V_{rms}
f_{mains}	50 Hz
EMI Filter Requirement	Class A

kHz range), that favor the utilization of ceramic capacitors with high energy density [12], [13]. However, as already mentioned, ultra-efficient hard-switching converters designed for high power ratings are typically operated at low switching frequencies (low tens of kHz) [14], [15]. These low switching frequencies lead to higher capacitance requirements of the FCs, giving a clear incentive to research alternatives to the FCC approach, which should still offer multi-level voltage characteristics but with a smaller capacitance demand. A topology that allows reducing by more than half the number of capacitors is presented in [16], [17], where a hybrid approach between the active neutral point clamped (ANPC) converter and the FCC is proposed (cf., Fig. 2(b)), hereafter referred to as the Hybrid Active Neutral Point Clamped (HANPC) converter. This topology, besides reducing the number of capacitors, enables a further volume saving, as only the capacitors with the lowest voltages remain. This is advantageous, since the higher the voltage rating of the capacitors, the lower the capacitance density, and hence, more capacitors have to be arranged in parallel and/or series, as can be seen, e.g., for the case of a thirteen-level FCC in [18]. These characteristics of the HANPC converter outperform the FCC in terms of achieving higher power densities for ultra-efficient converters, in particular for three-phase inverters in the 10 kW range targeting 99.5% efficiency, as shown in a comprehensive multi-level topology evaluation done in [9].

Therefore, this paper focuses on the optimization and hardware realization of an all-silicon ultra-efficient passively-cooled 12.5 kW three-phase seven-level HANPC (7L-HANPC) inverter, and finally experimentally verifies a peak efficiency of 99.35% and a power density of 3.4 kW/dm^3 (55.9 W/in^3) [20]. Firstly, the principle of operation of the HANPC converter is explained in detail in Section II. In Section III a design optimization is presented for the specifications given in Table I. The hardware design and the measurement results are presented in Section IV, and finally, the paper is concluded in Section V. Additionally, a detailed comparison of the accuracy of electric and calorimetric efficiency measurement methods is made in the Appendix.

II. Principle of Operation of the HANPC Converter

As the HANPC topology so far has only been employed in medium-voltage high-power applications [17], [21], a brief review of the principle of operation is provided in the following. Each bridge-leg of the HANPC inverter, illustrated in Fig. 2(b) for seven levels, consists of two cascaded stages: the ANPC stage connected to the DC input voltage and the FC stage finally generating the AC output voltage. The ANPC stage switches ($T_{1...4}$) connect the points I and II for positive output voltages $u_i > 0$ to the positive DC-link voltage rail (DC+) and the DC-link midpoint M respectively, and to M and the negative DC-link voltage rail (DC–) for $u_i < 0$, as shown in Fig. 3. This results in grid frequency operated ANPC stage switches that have to be rated to withstand $U_{DC}/2$. Following, there is a FC stage (for the case of a 7L-HANPC it is a four-level FC stage, as shown in Fig. 2(b)), whose semiconductors are operated at switching frequency using phase shifted PWM, and have to be rated for $U_{DC}/6$.

The fundamental difference between the HANPC converter and the FCC structure is that by actively clamping the FC stage to either the high-side or the low-side of the DC-link, the same number of levels can be obtained with a HANPC converter compared to a FCC. For the HANPC converter, the number of levels is given by

$$N_{\text{lev,HANPC}} = 2 \cdot N_{\text{FCcell}} + 1, \tag{1}$$

where N_{FCcell} is the number of FC cells, whereas for the FCC bridge-leg the number of levels is

$$N_{\text{lev,FCC}} = N_{\text{FCcell}} + 1. \tag{2}$$

From (1) and (2) it can be seen that the HANPC converter needs half the FC cells compared to the FCC to generate the same number of levels. For the case shown in Fig. 2, both the FCC and HANPC converter produce a seven-level voltage

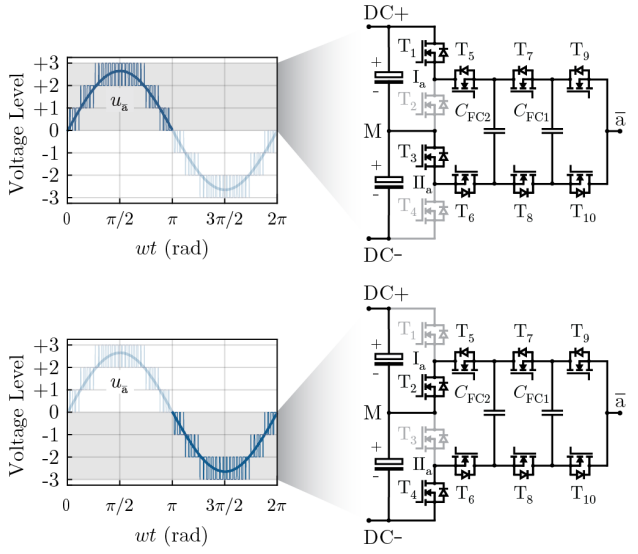

Fig. 3. Conduction states of the ANPC stage for positive and negative output voltages, shown for a bridge-leg of the 7L-HANPC. The ANPC stage switches ($T_{1..4}$) are connecting the subsequent FC stage ($T_{5..10}$) to the upper or lower half of the DC-link depending on the sign of the output voltage, while the FC stage is continuously switching at switching frequency. It has to be noted that Level 0 can be created with the FC stage clamped to either the high- or low-side of the DC-link.

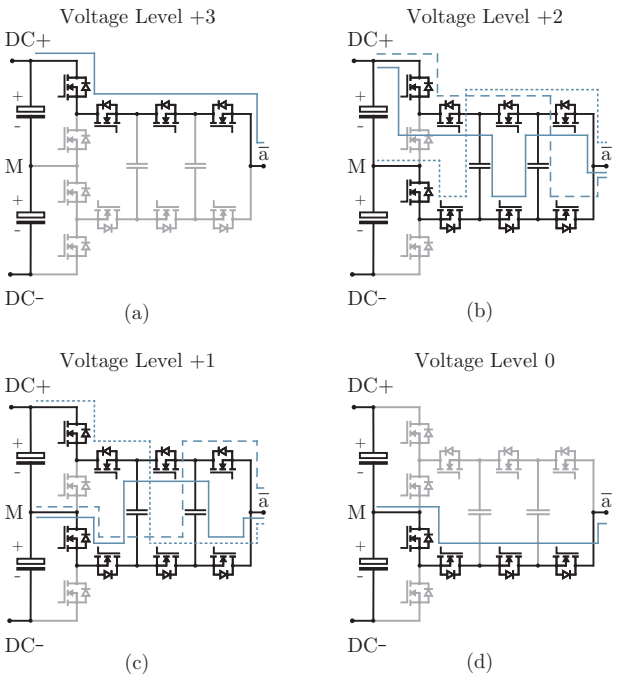

Fig. 4. Conduction states of a 7L-HANPC bridge-leg for the positive output voltage levels (a-c) and zero output voltage (d). For output voltage levels +3 and 0, the FCs are shorted by the high- and low-side FC stage switches respectively, and for levels +2 and +1, and there are three redundant switching states [19]. By ensuring equal conduction times of the three switching states, done by phase-shifted PWM, the flying capacitors are naturally balanced, as shown in Fig. 5.

output, but for the FCC the number of cells is $N_{\mathrm{FCcell}} = 6$, and for the HANPC converter only $N_{\mathrm{FCcell}} = 3$ is implemented. This is further illustrated in Fig. 3, where it can be seen that the +3...0 output voltage levels are created by connecting the FC stage to the upper half of the DC-link (cf., Fig. 4), whereas the output voltage levels 0...−3 are created by connecting the FC stage to the lower DC-link half. Hence, the ANPC stage acts as a selector switch, where the 0 output voltage level can be created in both ANPC stage configurations.

The effective switching frequency applied to the AC-side inductor and/or filter stage, which affects the filter design, losses and volume, is $f_{\mathrm{sw,eff}} = N_{\mathrm{FCcell}} \cdot f_{\mathrm{sw}}$, with f_{sw} being the switching frequency of the individual stages. The difference in N_{FCcell} between both topologies, however, has a minor effect on the effective switching frequency as will be made visible by the following qualitative analysis: if it is assumed that there is a certain loss budget allocation for the power semiconductors of the converter, and that for optimizing semiconductor losses the die areas of the switches are chosen such that the conduction losses and hard-switching losses are similar [8], [22], then the FCC can be designed to have approximately equal conduction losses and switching losses. To adapt the design to the HANPC converter, following Fig. 2, if the conduction losses of half the FC cells of the FCC stage are chosen to be the same as the conduction losses of the ANPC stage switches (which are switching at line frequency and hence have negligible switching losses), then the available budget for the switching losses of the FC stage of the HANPC converter is equal to that of the six cells of the FCC. Therefore, the last three HANPC FC cells can switch at twice the switching frequency of their pure FCC counterpart switches, hence imposing the same effective switching frequency on the filter stage. Following the same argumentation, the dimensioning of the capacitance of the FCs, which depends on the maximum conduction time,

$$t_{\mathrm{FC,max}} = \frac{1}{N_{\mathrm{FCcell}} f_{\mathrm{sw}}}, \tag{3}$$

shown in Fig. 5, remains similar for the FCC and the HANPC converter [9], [12], [23], since the product of $N_{\mathrm{FC,cell}}$ and f_{sw} remains similar. Hence, the dimensioning of the flying capacitors follows

$$C_{\mathrm{FC,min}} = \frac{t_{\mathrm{FC,max}} I_{\mathrm{ac,pk}}}{\Delta U_{\mathrm{FC,max}}}, \tag{4}$$

where $I_{\mathrm{ac,pk}}$ is the peak AC current, and $\Delta U_{\mathrm{FC,max}}$ the maximum allowed peak-to-peak FC voltage ripple. This is illustrated in detail in Fig. 5, where the two-cell and three-cell FC stages are shown for the duty cycle at which $t_{\mathrm{FC,max}}$ respectively occurs. For the case of a two-cell FC stage, $t_{\mathrm{FC,max}}$ occurs for a duty cycle of 0.5, while in the case of a three-cell FC stage, $t_{\mathrm{FC,max}}$ occurs at 0.66 or a duty cycle of 0.33. Hence, to have a conservative approach on the FC dimensioning (cf., (4)), it is considered that the peak output current $I_{\mathrm{ac,pk}}$ occurs for the duty cycles that result in $t_{\mathrm{FC,max}}$. By phase shifting the carriers by $2\pi/N_{\mathrm{FCcell}}$, natural balancing of the FCs occurs regardless of the number of levels, as shown in Fig. 5 for C_{FC1}. Therefore, no measurement of the FC voltage is required to operate this converter. Further analysis of the modulation and switching states of the HANPC converter can be found in [17], [19], [21], a variant of the 7L-HANPC is presented and discussed in [24], and the natural balancing of FC

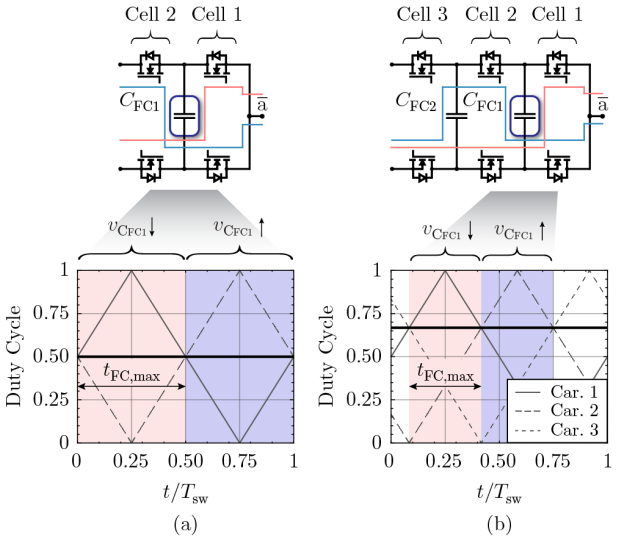

Fig. 5. Conduction states that charge (blue) and discharge (red) C_{FC1} for a two-cell (a) and a three-cell (b) FC stage. Additionally, the duty cycle that leads to the longest FC conduction time $t_{FC,max}$ is shown, where it is seen that $t_{FC,max}$ is inversely proportional to the number of levels. Due to phase-shifted PWM, the FC charge and discharge times remain equal for a whole switching period T_{sw}.

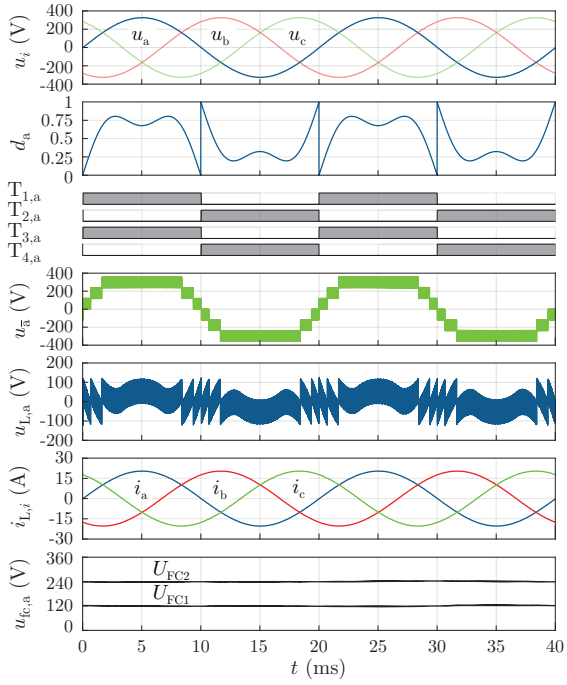

Fig. 6. Main waveforms of the 7L-HANPC inverter (cf., Fig. 2(b) and Fig. 7) operating with a DC-voltage of 720 V and an output power of 10 kW: mains phase voltages, duty cycle for phase a (d_a), gate signals for the ANPC stage switches of phase a, multi-level voltage output of node ā (cf., Fig. 2(b)) referenced to the DC midpoint and filter inductor (L) voltage waveform of phase a, grid phase currents, and FC voltages of phase a. Note that a third harmonic component is superimposed in the modulation to reduce the low-frequency component of the DC-link midpoint current, as seen for d_a, with an amplitude of one-fourth of the phase output voltage.

voltages by phase-shifted PWM is covered in [25]–[28].

The main waveforms of the 7L-HANPC inverter are shown in Fig. 6 for an output EMI filter structure with the star-point of the

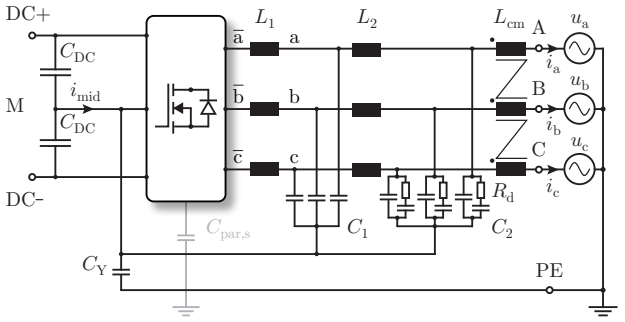

Fig. 7. EMI filter structure of the final prototype, with two *L-C* filter stages, simultaneously attenuating differential-mode (DM) and common-mode (CM) components of the output voltages of the inverter bridge-legs (with reference to the DC voltage midpoint) and a CM choke placed before the grid connection terminals.

filter capacitors connected to the DC-link midpoint as illustrated in Fig. 7. The seven output voltage levels together with the voltage applied to L_1 are shown for phase a, as well as the grid phase currents and the FC voltages, which are naturally balanced using phase shifted PWM. Finally, it has to be mentioned that, as for all NPC converters, a certain difference of the voltages of the upper and lower DC-link half arises due to the midpoint current i_{mid} (cf., Fig. 7) which has a dominant third harmonic component [19], [32]–[34]. However, this voltage difference can be reduced by either superimposing a third harmonic (zero sequence) to the modulation in such a way that the amplitude of the low-frequency part of i_{mid} is minimized, or by increasing the capacitance of the DC-link capacitors.

III. Design Optimization

To evaluate the most suitable component selection for the final hardware demonstrator, a comprehensive optimization of the 7L-HANPC inverter is performed, following the flowchart presented in Fig. 9. The optimization routine is conducted according to the converter dimensioning guidelines presented in [9], where for the FC stage, four different types of switches are considered, switching in a frequency range between 10 kHz and 40 kHz:

- two commercial 200 V silicon *OptiMOS 3* devices (*Infineon*),
- a virtual prototype of a next generation 200 V silicon device (*Infineon*), for which data has been provided by the manufacturer, and,
- the GaN power semiconductors of type *EPC2047 (EPC)*.

For the ANPC stage, however, both 600 V *CoolMOS CFD7* switches (*Infineon*) and a series-connection of the same low-voltage switches as used in the FC stage are considered [35]. This series-connection of the low-voltage switches shown in Fig. 10 would lead to the advantage of having the same semiconductors in the whole system. Its circuit schematic is similar to an FCC, but operated in a two-level configuration by adding balancing resistors (R_b) that ensure equal voltage balancing during steady-state, and capacitors (C_f) of low capacitance that ensure equal voltage balancing during the switching transients.

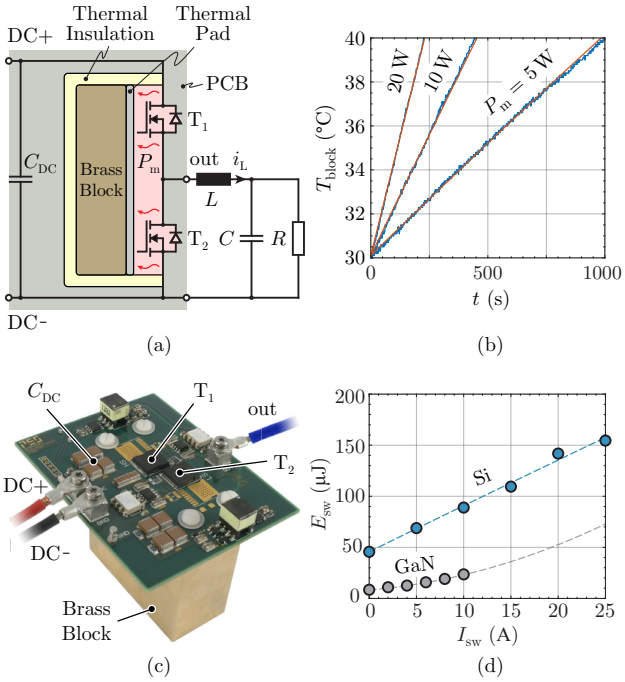

Fig. 8. Switching loss measurements of the lowest-$R_{ds,on}$-in-class low-voltage (200 V) Silicon (Si) (11.1 mΩ *IPT111N20NFD* from *Infineon*) and Gallium Nitride (GaN) (10 mΩ *EPC2047* from *EPC*) power semiconductors. The switching loss measurements are taken with a calorimetric setup based on [29]–[31], where the switching losses are determined by fitting the measured temperature rise curve from 30 °C to 40 °C to a calibrated *R-C* thermal model (a); mapping of the power losses to the temperature rise curve for the case of the Si switches (b); switching loss measurement setup for the Si switches (c), and measured hard-switching loss data at a DC-link voltage of 120 V (addition of the soft- and hard-switched transition losses of a half-bridge that occur during one switching period) for both devices (markers) together with a second order fit (dashed line) (d).

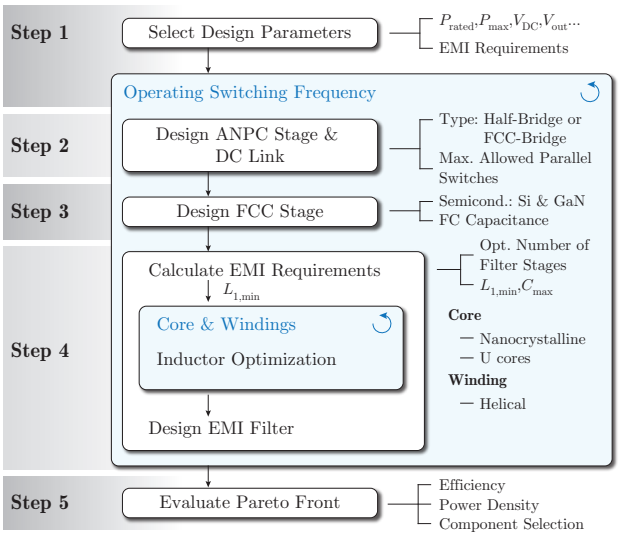

Fig. 9. 7L-HANPC converter optimization flowchart used to determine the Pareto front lines shown in Fig. 10.

Since the semiconductors, and in particular the FC stage switches, are the largest power loss contributors of the converter

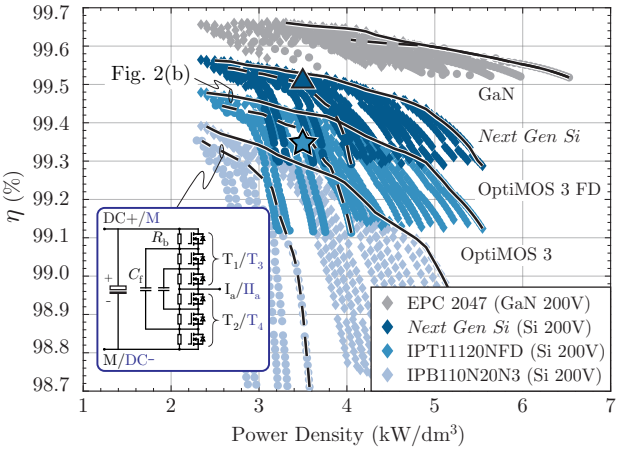

Fig. 10. Pareto optimization results for the different considered semiconductor devices and realizations of the ANPC stages. Results for the ANPC stage with 31 mΩ 600 V *CoolMOS CFD7* (*Infineon*) are shown with rhombi and continuous black Pareto lines, and the results for the series-connection of the same low-voltage MOSFETs of the ANPC stage [35] are shown with circles and dashed black Pareto lines. The efficiency is calculated at the operating point of 10 kW of the three-phase system, where the hardware prototype presented in this paper is represented by a star (four parallel devices for each switch of the ANPC stage), and the achievable performance with *next generation* 200 V silicon switches (estimation resulting from an extrapolation of recent FOM improvement) is shown by a triangle.

(cf., Fig. 11(a)), it is essential to have accurate switching loss data in order to obtain reasonable and realistic results in the converter optimization. For this reason, switching loss measurements were performed for the 11.1 mΩ 200 V Si switches of *Infineon* and the 10 mΩ 200 V GaN switches from *EPC*, which are presented in Fig. 8.

To comply with the International Special Committee on Radio Interference (CISPR) 11 Class A standard [36] on the AC-side, a *n*-stage *L-C* EMI filter structure is considered in the optimization routine ($n \in \{1,2,3\}$), which simultaneously attenuates DM and CM noise [37] as the filter stages are referenced to the DC midpoint (cf., Fig. 7). The filter design space is restricted by two factors: firstly, it should comply with the Class A EMI limits by a minimum attenuation margin of 10 dBµV, and secondly, the resonance frequency of the filter should be lower than one fourth of the effective switching frequency of the converter, to avoid unwanted excitation of the filter circuit [9]. For the filter inductor L_1, modeled and optimized according to [34], nanocrystalline cores with helical windings are used in order to reduce the losses [14], whereas for the further stage inductors (L_2, cf., Fig. 7) commercially available inductors are considered. Since low losses can be achieved with the *L-C* structure (cf., Fig. 11), a separation of the filter into dedicated DM and CM stages, which would increase the component count, is not considered.

Given the efficiency barriers obtained for different semiconductor technologies (indicated with the Pareto curves in Fig. 10), for the final design the all-silicon approach shown with a star is chosen, since the calculated efficiency difference between the commercially available silicon devices and GaN devices is only 0.25% for the same power density; with the introduction of next generation silicon devices, this difference

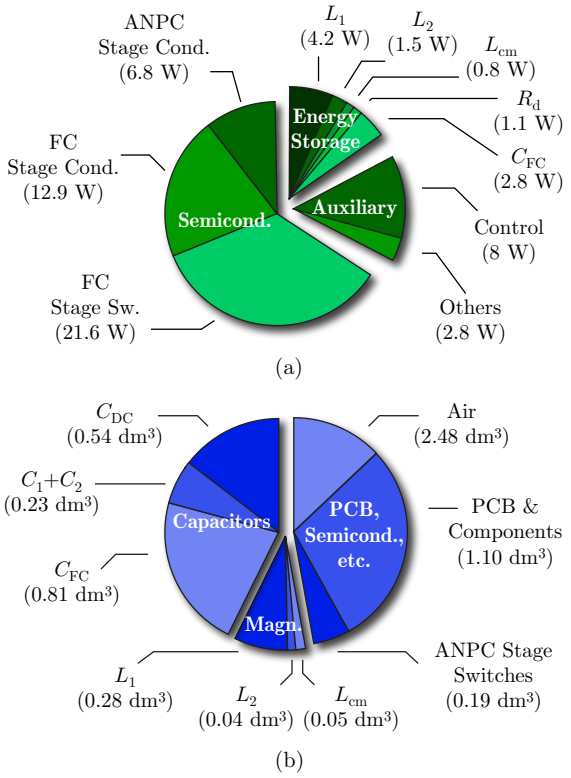

Fig. 11. Loss (a) and volume (b) distribution of the realized hardware (cf., Fig. 13), where the loss breakdown is shown for operation at 10 kW.

TABLE II
MAIN COMPONENTS OF THE FINAL DESIGN
THE EMI FILTER COMPONENT VALUES ARE GIVEN PER PHASE

Component	Value	Part Number
ANPC Stage Switches	31.0 mΩ	4 paralleled Infineon CoolMOS CFD7 600 V IPW60R031CFD7
FC Stage Switches	11.1 mΩ	2 paralleled Infineon OptiMOS 3 FD 200 V IPT111N20NFD
Gate Driver		10 A Infineon 1EDI60N12AF
L_1	113.3 µH	22 turns, Core: F3CC0008 2 mm × 5 mm wire
C_1	2.2 µF	Epcos TDK B32923H3225
L_2	15 µH	Wuerth Elek. 7443641500
C_2	13.2 µF	Epcos TDK B32924D3335
L_{cm}	400 µH (at 100 kHz)	4 turns, 2.5 mm wire Vacuumschmelze 2 x T60006-L2030-W358
C_{DC}	240 µF	Epcos TDK B32776G4406
C_{FC}	120 µF	Epcos TDK B32776G4406
C_Y	40 nF	Epcos TDK B32022A3103
R_d	1.65 Ω	pulse withstanding, through hole

is expected to be reduced to 0.15%. Regarding the ANPC stage configuration, the optimization results shown in Fig. 10 suggest that using 600 V switches for the ANPC stage (solid line Pareto front) offers superior performance both in terms of efficiency and power density compared to the series-connected 200 V device variant (dashed line Pareto front). This is due to the lower $R_{ds,on}$ of the 600 V switches compared to the 200 V switches and the need to passively balance the voltage of the 200 V switches by means of balancing resistors R_b, shown in Fig. 10. Since low switching frequencies yield designs with a high efficiency but a large volume, and high switching frequencies yield compact but more lossy designs (cf., Fig. 10), the design that is finally chosen for the hardware demonstrator reserves place for up to six parallel-connected 31 mΩ *CoolMOS CFD7* devices for the ANPC stage, and two parallel 11.1 mΩ *IPT111N20NFD* devices switching at 16 kHz, resulting in an effective switching frequency of 48 kHz for the filter stage. It has to be noted that for the case of the 600 V switches, the more switches connected in parallel, the lower the losses (negligible switching losses at grid frequency), however, at the price of increased cost and volume. It is for this reason that, in this optimization, a limit of six paralleled switches is considered for the ANPC switches for both ANPC stage configurations. The loss distribution of the selected design for the realized hardware demonstrator is shown in Fig. 11(a) for a power of 10 kW, where it can be observed that the semiconductors account for 66% of the total converter losses, out of which 84% are caused by the FC switches. The resulting contribution of the magnetic components to the loss and volume distributions is in the range of 10...15%, since with the relatively high output effective frequency and the multi-level output voltage waveform, only a small voltage-time area is applied to the inductors.

The final filter structure comprises two *L-C* filter stages, whose star point is connected to the midpoint of the DC-link to provide a return path for the CM current, as shown in Fig. 7. To further mitigate the effects of the unavoidable parasitic capacitance from the switching stage $C_{par,s}$ to ground, an additional CM-choke is placed before the grid connection terminals and a Y-rated capacitor C_Y is connected between earth (PE) and the DC-link midpoint. Finally, *R-C* damping is provided in the second filter stage with damping resistors R_d similar to [15], in order to avoid larger damping losses that would arise due to the switching voltage ripple if damping would be installed in the first stage. A list of the main power components used in the hardware prototype and their part numbers can be found in Table II.

The volume distribution of the hardware is given in Fig. 11(b), where it can be seen that the capacitors are the main volume contributors. The FC capacitance is dimensioned by the minimum capacitance requirement that is obtained by imposing a maximum switching frequency ripple of the FC voltage (see (4)), limited here to $\Delta U_{FC,max}$ = 5 V. Given the low switching frequency and high output current, the capacitance requirement is large, i.e., 107 µF for capacitors which operate at nominal voltages of 120 V and 240 V. Hence, film capacitors are chosen instead of ceramic capacitors, to avoid the need of having to

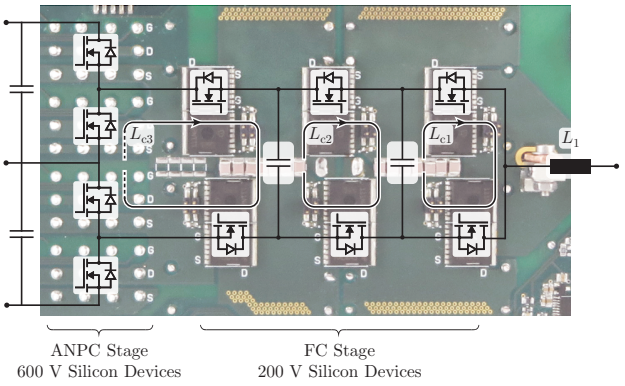

Fig. 12. Realization of the hardware layout of a three-phase 7L-HANPC inverter bridge-leg, where the FCs (film-type) are placed underneath the PCB, and ceramic capacitors are placed on top to improve the switching behavior of the MOSFETs. The commutation loop introduced by the connection of the FC stage to the HANPC stage L_{c3} is the most critical.

parallel-connect ≈ 200 capacitors per FC, which would also lead to approximately a × 15 price increase of the capacitors. However, for converters with a lower power rating (and lower load currents) and higher switching frequencies, ceramic capacitors are more suitable, since a higher volumetric energy density can be achieved [12], [18], [28], [38].

IV. Hardware Implementation and Measurement Results

To validate the presented calculations and the suitability of the 7L-HANPC topology for ultra-high efficiency applications, the hardware implementation of the 7L-HANPC and the main measurement results will be presented in the following.

A. Hardware Implementation

The first step to build the 7L-HANPC inverter is to design an optimal bridge-leg layout, especially because switching losses cause a significant part of the overall losses and depend to a large extent on layout parasitics [39]. The implemented layout and its schematic arrangement are shown in Fig. 12, where particular care has to be taken for the FC stage layout. Since there are three FC cells per bridge-leg, there are three switching frequency commutation loops that require attention in the layout, namely L_{c1}, L_{c2} and L_{c3}, out of which L_{c3} is the most critical for two reasons: firstly, the commutation path of L_{c3} always closes through either the upper side or the lower side DC-link capacitor, for which layout symmetry has to be maximized such that L_{c3} is equal for both cases, as seen in Fig. 12; secondly, given that the high-side and low-side (partial) DC-link voltages are not always equal in value due to the nature of the topology, care has to be taken if commutation capacitors are placed between the ANPC stage and FC stage switches. Since two capacitors of unequal voltage, i.e., the respective DC-link capacitor and the commutation capacitor, which has previously been connected to the opposite half DC-link capacitor, would be connected in parallel, current spikes and ringing would occur when commutating the ANPC stage switches. Note that although space

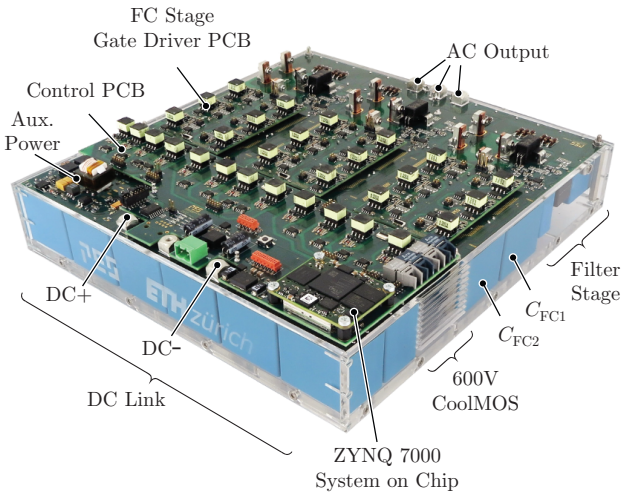

Fig. 13. Hardware prototype of the 12.5 kW three-phase 7L-HANPC inverter, measuring 256 mm × 269 mm × 53 mm (10.1 in × 10.6 in × 2.1 in). The final volumetric power density is 3.4 kW/dm^3 (55.9 W/in^3), and the gravimetric power density is 3.2 kW/kg (1.5 kW/lb).

is provided to place ceramic capacitors between the ANPC and FC stages, this has not finally been done in the current setup (cf., Fig. 12). However, L_{c1} and L_{c2} can easily be optimized by placing ceramic (commutation) capacitors in parallel to the (film-type) FCs to reduce the size of the commutation loop (cf., Fig. 12), keeping the maximum overvoltage of the FC stage switches to 30 V. All the gate drivers are placed on separate PCBs, which on the one hand has the advantage of keeping the power PCB free from the gate driver circuitry for an optimized layout, but on the other hand has the disadvantage of increasing the gate loop inductance. This inductance is minimized by using low-profile board-to-board connectors (*Samtec TMM* and *CLT* types) that result in a distance between the PCBs of only 2.77 mm (0.11 in). Each switch has its own isolated power supply, for which dedicated transformers are used to obtain isolated gate voltages of 15 V and −5 V.

The 12.5 kW hardware demonstrator shown in Fig. 13, features a volumetric power density of 3.4 kW/dm^3 (55.9 W/in^3) and a gravimetric power density of 3.2 kW/kg. It has to be noted that, for the presented measurements, four power MOSFETs were connected in parallel for implementing each switch of the ANPC stage, however, space was provided in the layout to accommodate a total of six parallel switches.

Given the high efficiency nature of the converter, there is no need for active cooling, and hence, neither fans nor heat sinks are required, thus minimizing the implementation effort and increasing the overall reliability of the system. This is particularly true for the converter at hand, where the semiconductor losses are distributed among many switches: the estimated losses of a single ANPC stage switch, housed in a TO-247 three-lead package, are of 0.14 W on average, whereas the losses for an individual SMD FC stage switch are 0.96 W. Experimental measurements yield that at thermal steady-state during operation at 10 kW and an ambient temperature of 40 °C, the 600 V switches housed in a though-hole TO-247 package have a case temperature of 64.8 °C, and that the 200 V switches housed in

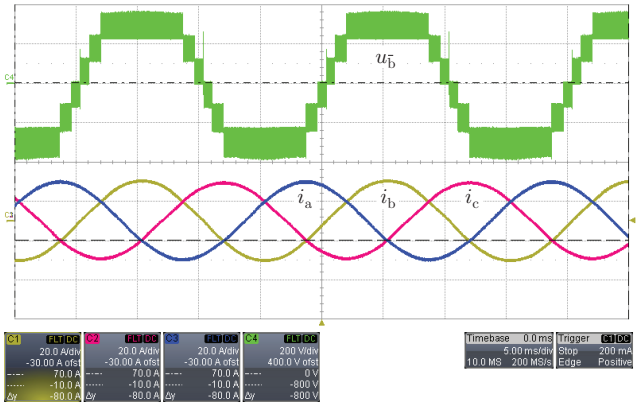

Fig. 14. Measurements of the seven-level output voltage of a bridge-leg of the 7L-HANPC inverter shown in Fig. 13 (200 V/div, referenced to the DC-link midpoint, 5 ms/div) and the currents of the three phase mains (20 A/div) during operation at 10 kW. The experimental waveforms are in accordance with the simulation results shown in Fig. 6.

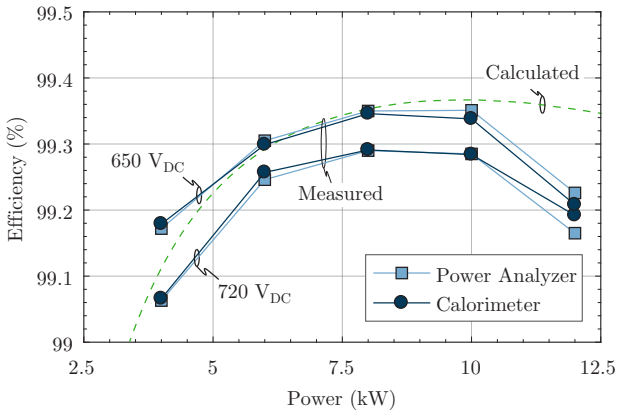

Fig. 15. Measured efficiency of the hardware demonstrator (cf., Fig. 13) reaching peak values of 99.35% for U_{DC} = 650 V and 99.30% for U_{DC} = 720 V, and calculated efficiency characteristic for V_{DC} = 720 V. All efficiency measurements are taken at a controlled ambient temperature of 40 °C.

a HSOF SMD package have a case temperature of 69.3 °C, resulting in a case-to-ambient thermal resistance of 175 °C/W and 36 °C/W, and junction temperature of 64.9 °C and 69.7 °C respectively.

B. Experimental Waveforms

The main measured waveforms taken with a resistive load (i.e., operating the system in inverter mode) are presented in Fig. 14 for 10 kW operation, where the unfiltered seven-level phase voltage measured at the output node $\bar{b}$ with respect to the DC-link midpoint and the three phase currents are shown. The voltage spikes that can be seen during the voltage zero crossings are due to the unequal switching times of the ANPC stage and FC stage switches, and last only for some few tens of nanoseconds not affecting the overall system performance. The DC-link voltage midpoint is controlled by superimposing a third harmonic to the sinusoidal modulation of one fourth of the output voltage amplitude (cf., Fig. 6), achieving a low maximum instantaneous voltage deviation between the upper half and the lower half of the DC-link of 8.9 V during nominal operation. The FC voltages are naturally balanced by phase shifted PWM [25] at their nominal voltages, i.e., at average values of U_{FC2} = 240.5 V and U_{FC1} = 120.9 V.

C. Efficiency Measurements

The efficiency of the three-phase 7L-HANPC inverter is measured both calorimetrically, with the calorimeter presented in [3], and electrically, with a *Yokogawa WT3000* precision power analyzer. The efficiency measurement results of both methods are reported in Fig. 15, together with the calculated efficiency at V_{DC} = 720 V. A peak efficiency of 99.35% is achieved for U_{DC} = 650 V, and 99.30% for U_{DC} = 720 V, where all the converter losses are considered, including those of the EMI filter stage and the auxiliary power. The fitted European weighted efficiency is 99.10%, whereas the California Energy Commission (CEC) weighted efficiency is 99.20% [40]. Since electrical power measurements with precision power analyzers have a large efficiency error band ($\Delta\eta$ = ±0.38% at 10 kW, leading to the uncertainty of the efficiency measurement to be between η = 98.92…99.68%, cf., Appendix), also calorimetric measurements were performed in order to accurately determine the overall efficiency. The calorimetric approach measures the power losses with a relative error smaller than 1% for the whole range where measurements were taken [3], leading to an efficiency accuracy of $\Delta\eta$ = ±0.0065%. The efficiency measurement points presented in Fig. 15 are taken with the converter at thermal steady-state inside the inner chamber of the calorimeter, which is controlled to have an ambient temperature of 40 °C, resulting in 2 to 3 hours of continuous operation for each efficiency measurement point. However, it has to be noted that the electric and the calorimetric loss measurements match very well, as also shown in [15], from which it can be concluded that the actual accuracy of the power analyzer is substantially higher than specified in the datasheet. An in-depth comparison of the electric and calorimetric measurement methods is provided in the Appendix.

D. Conducted EMI Measurements

The results of the conducted EMI emission measurement are presented in Fig. 16, for the frequency range between 10 kHz and 30 MHz. Two different scans are shown, the first one with the peak and average detector for a measurement time of 50 ms for frequencies < 150 kHz, and 10 ms measurement time for frequencies ≥ 150 kHz, and a second one, with the quasi-peak and average detector for a measurement time of 1 s. It has to be noted, that for the effective switching frequency (48 kHz) resulting from the converter optimization described in Section III, the filter dimensioning is limited by the need of sufficiently separating the filter resonance frequency and the effective switching frequency, in order to not excite any filter resonance, and not by the EMI filtering requirements. This can be seen in Fig. 16, since for the first harmonic above 150 kHz, the attenuation margin is well above the 10 dBµV for which the EMI filter design space was

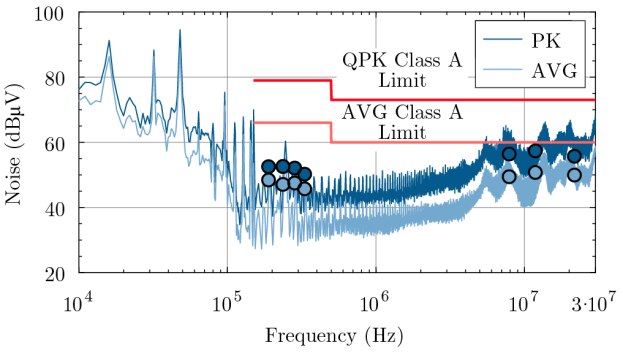

Fig. 16. Conducted EMI noise emission spectrum of the hardware demonstrator presented in Fig. 13, where the CISPR 11 peak and average detectors are used with a 1 kHz step, 200 Hz bandwidth, and 50 ms measurement time for frequencies < 150 kHz and a 4 kHz step, 9 kHz bandwidth, and 10 ms measurement time for frequencies ≥ 150 kHz. Selected peaks (markers) have been measured with quasi-peak and average detectors for a measurement time of 1 s.

restricted in the optimization.

V. Conclusion

In this paper, a 99.35% efficient 3.4 kW/dm^3 (55.9 W/in^3) all-silicon seven-level three-phase inverter is presented, setting a new benchmark for ultra-high efficient and power-dense converters. A topological alternative to the conventional FCC is employed, which has the advantage of halving the amount of FC cells by making use of a DC-link midpoint connection, and an ANPC stage front-end that uses switches rated for half the DC-link voltage and is switching at grid frequency. Substantial volume savings are obtained by halving the number of FC cells, particularly for the case of low switching frequencies, since the capacitance requirement to guarantee a certain voltage ripple of the FCs is inversely proportional to the switching frequency, which is limited for ultra-efficient converters. Additionally, no active cooling is required given the high efficiency of the system and the fact that the losses are spread among many switches and/or power components, reducing the design effort and increasing reliability.

With recently available 18 mΩ 600 V *CoolMOS CFD7* power MOSFETs (*Infineon*), which have a lower on-state resistance compared to the 31 mΩ switches used in this work, the efficiency and/or volume could be further improved, as the switching losses are negligible at grid frequency. Furthermore, a comprehensive optimization shows that it is feasible to reach the boundary of 99.5% efficiency with nextgeneration 200 V silicon devices, and 99.6% with state-of-the-art GaN devices.

Appendix

Accurate Efficiency Measurements: Electric vs. Calorimetric Methods

For power converters in the low- and mid-ninety percent efficiency range, the efficiency can be directly determined using a power analyzer. However, for ultra-efficient converters, particularly for those in the 99+% efficiency range [3], [14], [15], [41], accurately determining the efficiency characteristic requires additional calorimetric loss measurements. In the following, both the electric and calorimetric efficiency measurement methods are described, followed by a discussion and comparison between them.

A. Electric Efficiency Measurement

The first approach to determine efficiency is to measure the input and output powers, P_{out} and P_{in} respectively, using a precision power analyzer:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}}. \tag{5}$$

However, since P_{out} and P_{in} are large values in comparison with the power losses, a small error in the measurement of both power values can lead to a large deviation in the measured efficiency, and therefore has to be considered accordingly. Assuming relative measurement errors, $\varepsilon_{\text{Pout}}$ and ε_{Pin}, the worst-case absolute error of the efficiency measurement $\Delta\eta$ is

$$\Delta\eta = \eta\frac{(\varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}})}{(1 - \varepsilon_{\text{Pin}})}. \tag{6}$$

If the output and input power measurement shows the same error, ε_{P}, the error of the efficiency measurement can be approximated as

$$\Delta\eta \approx \varepsilon_{\text{Pout}} + \varepsilon_{\text{Pin}} \approx 2\varepsilon_{\text{P}}. \tag{7}$$

For the case at hand, the *Yokogawa WT3000* precision power analyzer was used to electrically measure the efficiency. To determine the efficiency measurement error, errors are specified for both the DC and the AC power measurement as follows: firstly, an error depending on the power reading, ε_{Y}, and secondly, an error depending on the power range in which the measurement has been taken, ε_{X}. With these two errors, the power measurement errors for the DC side input ε_{Pdc} and the three-phase AC power output ε_{Pac} can be calculated as

$$\varepsilon_{\text{Pdc}} = \frac{P_{\text{DC}}(1 + \varepsilon_{\text{Y,dc}}) + X_{\text{Pdc}}\varepsilon_{\text{X,dc}}}{P_{\text{DC}}} - 1 \tag{8}$$

$$\varepsilon_{\text{Pac}} = \frac{3\,(P_{\text{AC,1}\phi}(1 + \varepsilon_{\text{Y,ac}}) + X_{\text{Pac}}\varepsilon_{\text{X,ac}})}{P_{\text{AC,1}\phi}} - 3, \tag{9}$$

where X is the power range of the efficiency measurement. For an efficiency measurement at 10 kW, (8) yields $\varepsilon_{\text{Pdc}} = \pm 0.25\%$ and (9) $\varepsilon_{\text{Pac}} = \pm 0.13\%$, leading to a large error of the efficiency measurement of $\Delta\eta = \pm 0.38\%$.

B. Calorimetric Efficiency Measurement

For ultra-high efficiency converters, a second approach that leads to more accurate efficiency measurements is used, i.e., a calorimetric measurement, which by directly measuring the

power losses P_{loss}, allows to calculate the efficiency as

$$\eta = 1 - \frac{P_{loss}}{P_{in}}. \tag{10}$$

An error in the loss measurement leads to an absolute error in the efficiency of only

$$\Delta\eta = \frac{\Delta P_{loss}}{P_{in}} = (1 - \eta)\,\varepsilon_{loss}, \tag{11}$$

where ε_{loss} is the relative error in the power loss measurement.

The employed calorimeter is presented in [3], and determines the power losses by measuring the coolant volume flow $\dot{V}$ and the coolant temperature difference between the input and output of the calorimeter ΔT, with

$$P_{loss} = c_p \rho \dot{V} \Delta T, \tag{12}$$

where c_p is the specific heat capacity of the coolant, and ρ is the mass density [42]. The main advantage of calorimetric measurement method is that the power losses can be measured independent from the power processed by the converter, and its accuracy therefore only depends on the error with which P_{loss} can be measured. In this case, since the accuracy of both $\dot{V}$ and ΔT profit from higher measured values, which occur when measuring higher values of P_{loss}, the accuracy of the employed calorimeter increases for higher measured power losses, as shown in Table III. Finally, it has to be noted that the accuracy of the calorimetric measurements benefit further from calibration, which is performed before taking measurements on a device under test.

C. Accuracy Comparison of Electric and Calorimetric Efficiency Measurements

A general comparison between both measurement methods can be done by finding a relation between ε_P and ε_{loss}, which with (6) and (11) yields:

$$\varepsilon_{loss} = \frac{\eta\,(\varepsilon_{Pout} + \varepsilon_{Pin})}{(1 - \varepsilon_{Pin})(1 - \eta)} \approx \frac{2\varepsilon_P}{(1 - \eta)}. \tag{13}$$

The relation between ε_P and ε_{loss} can be seen in Fig. 17, where additionally the errors for the efficiency measurement for the converter at hand for 10 kW operation are shown for both the electric measurement with the precision power analyzer and the calorimeter. It is seen that for the electric efficiency measurement, the relative error in the power loss determination is above 50%. Accordingly, in order to achieve the same performance as with the calorimeter (ε_{loss} = 1%), the accuracy when measuring the input and output power would have to be 0.003%, which is not possible with state-of-the-art precision power analyzers.

Finally, the difference of the efficiency calculation confidence interval for both measurement methods is shown in Fig. 18 for the presented converter. It can be seen that for operation at two different power levels (2 kW and 10 kW), the uncertainty in the calorimetric efficiency measurement is much smaller than with an electric measurement.

TABLE III
CALORIMETER ACCURACY SPECIFICATIONS [3]

P_{loss}	Error (ε_{loss})
< 10 W	< ±3.5 %
< 100 W	< ±1 %
< 200 W	< ±0.5 %

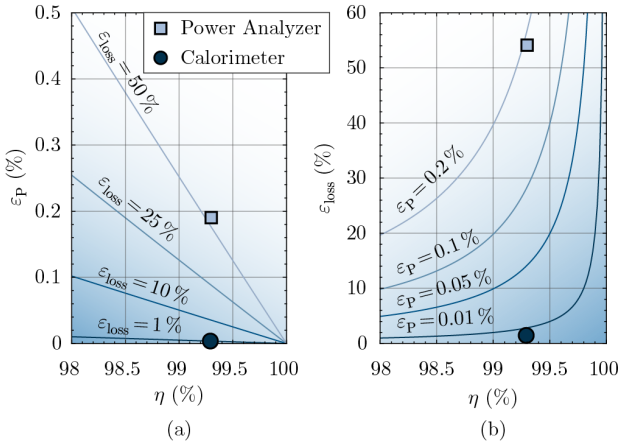

Fig. 17. Graphical representation of the relative power loss calculation error ε_{loss} as a function of the relative power measurement error ε_P and efficiency η (a), and vice versa (b). The accuracy of the performed efficiency measurements with the *Yokogawa WT3000* precision power analyzer (square symbol) and the calorimeter (round symbol) [3] is shown for a processed power of 10 kW.

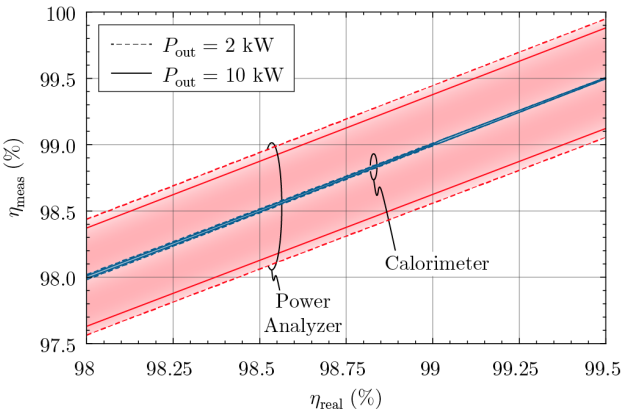

Fig. 18. The confidence interval for the measured efficiency (η_{meas}) vs. the real efficiency (η_{real}) for the presented inverter, where $\eta_{meas} = \eta_{real} \pm \Delta\eta$. Both electric (*Yokogawa WT3000* precision power analyzer) and calorimetric [3] efficiency measurements are shown for 2 kW and 10 kW of processed power.

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References

[1] *Renewables 2017: Analysis and Forecasts to 2022*, International Energy Agency, Oct. 2017.

[2] H. Wirth, *Recent Facts about Photovoltaics in Germany*, Fraunhofer ISE, Version: July 20, 2018. [Online]. Available: https://www.ise.fraunhofer.de/en/publications/studies/recent-facts-about-pv-in-germany.html

[3] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Mühlethaler, T. Nussbaumer, and J. Miniböck, "Extreme efficiency power electronics," in *Proc. Integrated Power Electron. Syst. Conf. (CIPS)*, Mar. 2012, pp. 1–22.

[4] K. A. Kim, Y.-C. Liu, M.-C. Chen, and H.-J. Chiu, "Opening the box: survey of high power density inverter techniques from the little box challenge," *CPSS Trans. Power Electron. Appl*., vol. 2, no. 2, pp. 131–139, Aug. 2017.

[5] C. W. Halsted and M. D. Manjrekar, "A critique of little box challenge inverter designs: breaking from traditional design tradeoffs," *IEEE Power Electron. Mag*., vol. 5, no. 4, pp. 52–60, Dec. 2018.

[6] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstübner, "Performance trends and limitations of power electronic systems," in *Proc. Integrated Power Electron. Syst. Conf. (CIPS)*, Mar. 2010, pp. 1–20.

[7] X. Zhang, T. Zhao, W. Mao, D. Tan, and L. Chang, "Multilevel inverters for grid-connected photovoltaic applications: examining emerging trends," *IEEE Power Electron. Mag.,* vol. 5, no. 4, pp. 32–41, Dec. 2018.

[8] J. W. Kolar, J. Biela, and J. Miniböck, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7kW/dm3 power density," in *Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC)*, Wuhan, China, May 2009, pp. 1–21.

[9] J. Azurza Anderson, L. Schrittwieser, M. Leibl, and J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," in *Proc. IEEE Int. Telecom. Energy Conf. (INTELEC)*, Broadbeach, Australia, Oct. 2017, pp. 456–463.

[10] P. Papamanolis, F. Krismer, and J. W. Kolar, "Minimum loss operation of high-frequency inductors," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 1756–1763.

[11] G. Deboy, O. Häberlen, and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," *CPSS Trans. Power Electron. Appl*., vol. 2, no. 2, pp. 89–100, June 2017.

[12] Y. Lei, C. Barth, S. Qin, W. C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kW, single-phase, 7-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.,* vol. 32, no. 11, pp. 8570–8581, Jan. 2017.

[13] C. B. Barth, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," in *Proc. IEEE Energy Conv. Cong. Expo. (ECCE USA)*, Montreal, Canada, Oct. 2015, pp. 6269– 6276.

[14] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "99% efficient three-phase buck-type SiC MOSFET PFC rectifier minimizing life cycle cost in DC data centers," *CPSS Trans. Power Electron. Appl*., vol. 2, no. 1, pp. 47–58, July 2017.

[15] L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar, and T. B. Soeiro, "99.3% efficient three-phase buck-type all-SiC SWISS rectifier for DC distribution systems," *IEEE Trans. Power Electron*., vol. 34, no. 1, pp. 126–140, Jan. 2019.

[16] P. Barbosa, J. Steinke, P. Steimer, L. Meysenc, and T. A. Meynard, "Converter circuit for switching a large number of switching voltage levels," US Patent 7,292,460, Feb. 2007.

[17] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, "Active-neutral-point-clamped (ANPC) multilevel converter technology," in *Proc. European Conf. Power Electron. Appl. (EPE)*, Dresden, Germany, Sept. 2005, pp. 1–10.

[18] C. B. Barth, T. Foulkes, W. H. Chung, T. Modeer, P. Assem, Y. Lei, and R. C. N. Pilawa-Podgurski, "Design and control of a GaN-based, 13-level, flying capacitor multilevel inverter," in *Proc. IEEE Control Modeling Power Electron. Workshop (COMPEL)*, Trondheim, Norway, Sept. 2016, pp. 1–6.

[19] G. Konstantinou, S. R. Pulikanti, M. Ciobotaru, V. G. Agelidis, and K. Muttaqi, "The seven-level flying capacitor based ANPC converter for grid intergration of utility-scale PV systems," in *Proc. IEEE Power Electron. Distrib. Generat. Syst. Symp. (PEDG)*, Aalborg, Denmark, 2012, pp. 592–597.

[20] J. Azurza Anderson, E. J. Hanak, L. Schrittwieser, J. W. Kolar and G. Deboy, "Towards a 99.5% efficient all-Silicon three-phase seven-level hybrid active neutral point clamped inverter," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo. (PEAC)*, Shenzhen, China, Nov. 2018, pp. 1–7.

[21] E. Burguete, J. López, and M. Zabaleta, "A new five-level active neutral-point-clamped converter with reduced overvoltages," *IEEE Trans. Ind. Electron*., vol. 63, no. 11, pp. 7175–7183, Apr. 2016.

[22] J. Azurza Anderson, L. Schrittwieser, C. Gammeter, G. Deboy, and J. W. Kolar, "Relating the figure of merit of power MOSFETs to the maximally achievable efficiency of converters." *Under Review for Electrical Engineering,* Springer.

[23] S. Bernet, "Comparison of medium voltage drives for industry applications," in *ECPE Workshop on Advanced Power Conversion-Concepts for Motor Drives*, Aalborg, Denmark, Apr. 2005.

[24] Y. Siwakoti, A. Mahajan, D. Rogers, and F. Blaabjerg, "A novel seven-level active neutral point clamped converter with reduced active switching devices and DC-link voltage," *IEEE Trans. Power Electron*., pp. 1–26, 2019, Early Access.

[25] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron*., vol. 44, no. 3, pp. 356–364, June 1997.

[26] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Trans. Power Electron*., vol. 23, no. 2, pp. 543–550, Mar. 2008.

[27] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: the general case," *IEEE Trans. Power Electron*., vol. 21, no. 6, pp. 1658–1666, Nov. 2006.

[28] P. Papamanolis, D. Neumayr, and J. W. Kolar, "Behavior of the flying capacitor converter under critical operating conditions," in *Proc. IEEE Intl. Symp. Ind. Electron. (ISIE)*, Edinburgh, Scotland, June 2017, pp. 628–635.

[29] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10kV SiC MOSFETs and diodes," *IEEE Trans. Power Electron*., vol. 33, no.6, pp. 5240–5250, June 2018.

[30] M. Guacci, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the origin of the coss-losses in soft-switching GaN-on-Si power HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron*., pp. 1–16, 2019, Early Access.

[31] D. Neumayr, M. Guacci, D. Bortis, and J. W. Kolar, "New calorimetric power transistor soft-switching loss measurement based on accurate temperature rise monitoring," in *Proc. IEEE Int. Symp. Power Semicond. Dev. IC's (ISPSD)*, Sapporo, Japan, May 2017, pp. 447–450.

[32] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. IEEE Ind. Appl. Soc. Ann. Meeting (IAS)*, vol. 2, Toronto, Canada, Oct. 1993, pp. 965–970.

[33] A. Yazdani and R. Iravani, *Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications*. John Wiley & Sons, 2010.

[34] M. Leibl, "Three-phase PFC rectifier and high-voltage generator," Ph.D. dissertation, ETH Zurich, 2017.

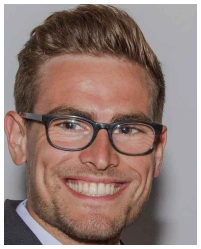
[35] M. Schweizer and T. B. Soeiro, "Heatsink-less quasi 3-level flying capacitor inverter based on low voltage SMD MOSFETs," in *Proc. European Conf. Power Electron. Appl. (EPE-ECCE Europe)*, Warsaw, Poland, Sept. 2017, pp. 1–10.

[36] International Special Committee on Radio Interference - C.I.S.P.R., Geneva, Switzerland, "*Specification for Industrial, Scientific and Medical (ISM) Radio-Frequency Equipment - Electromagnetic Disturbance Characteristics - Limits and Methods of Measurement - Publication 11*," 2004.

[37] M. Antivachis, D. Bortis, A. Avila, and J. W. Kolar, "New optimal common-mode modulation for three-phase inverters with DC-link referenced output filter," *CPSS Trans. Power Electron. Appl*., vol. 2, no. 4, pp. 331–340, 2017.

[38] N. Pallo, T. Foulkes, T. Modeer, S. Coday, and R. C. N. Pilawa-Podgurski, "Power-dense multilevel inverter module using interleaved GaN-based phases for electric aircraft propulsion," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 1656–1661.
[39] J. Wang, H. S.-H. Chung, and R. T.-h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.
[40] A. C. Nanakos, E. C. Tatakis, and N. P. Papanikolaou, "A weighted-efficiency-oriented design methodology of flyback inverter for AC photovoltaic modules," *IEEE Trans. Power Electron*, vol. 27, no. 7, pp. 3221–3233, July 2012.
[41] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10kV SiC-based medium voltage ZVS bidirectional single-phase PFC AC/DC stage." *IEEE J. Emerg. Sel. Topics Power Electron.*, pp. 1–19, 2019, Early Access.
[42] D. Christen, U. Badstübner, J. Biela, and J. W. Kolar, "Calorimetric power loss measurement for highly efficient converters," in *Proc. IEEE Int. Power Electron. Conf. (IPEC), 2010*, Sapporo, Japan, June 2010, pp. 1438–1445.

Jon Azurza Anderson received his B.Sc. degree in Industrial Technology Engineering from TECNUN School of Engineering of the University of Navarra in 2014, and his M.Sc. degree in Electrical Engineering from ETH Zurich (with distinction) in 2016, specializing in energy and power electronics. In 2013 and 2014 he worked for Fraunhofer IIS in Nuremberg, Germany, developing software in the RFID & Radio Systems group. In November 2016 he joined the Power Electronics Systems Laboratory (PES) as a scientific assistant, where in February 2017 he began his Ph.D. studies, focusing on ultra-high efficiency three-phase multi-level PWM converters.



Eli J. Hanak studied Electrical Engineering and Information Technology at the University of Stuttgart where he received his B.Sc. and M.Sc. degrees in 2015 and 2018 respectively. The focus of his undergraduate studies was electric mobility. This led him to study abroad at Purdue University and ETH Zurich where his main focus was electrical drives and power electronics. After completing his master thesis at the Power Electronic Systems Laboratory (PES) at ETH Zurich, he worked in PES from May 2018 to November 2018 as a scientific assistant working on ultra-efficient inverter concepts. In April 2019, he started the Explorer Trainee Program with ABB Switzerland.

Lukas Schrittwieser received the M.Sc. degree in Electrical Engineering 2014 (with distinction) and the Ph.D. degree in 2018, for the thesis entitled "Ultra-Efficient Three-Phase Buck-Type PFC Rectifier Systems" from the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland. During his studies, he focused on isolated and nonisolated, highly efficient three-phase buck-type PWM rectifiers for data centers, battery charging and dc distribution systems. His research interests include ultra-efficient converter systems, applications of wide bandgap semiconductor devices and measurement technologies. In 2018 he teamed with 3 colleagues to found *Technokrat*, a start-up offering electrical engineering consulting and research, based in Zurich.

Mattia Guacci studied Electronic Engineering at the University of Udine, Italy, where in July 2013 and in October 2015 he received his B.Sc. summa cum laude and his M.Sc. summa cum laude, respectively. In 2014 he was with Metasystems SpA in Reggio nell'Emilia, Italy working on on-board battery chargers for electric vehicles. In November 2015 he joined the Power Electronic Systems Laboratory (PES) at ETH Zurich as a scientific assistant investigating innovative inverter topologies. In September 2016 he started his Ph.D. at PES focusing on advanced power electronics concepts for future aircraft and electric vehicle applications.

Johann W. Kolar received his M.Sc. and Ph.D. degree (summa cum laude/promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria, in 1997 and 1999, respectively. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, modulation and control concepts and has supervised 70+ Ph.D. students. He has published 880+ scientific papers in international journals and conference proceedings, 4 book chapters, and has filed 190+ patents. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 27 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award and two ETH Zurich Golden Owl Awards for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an associate editor of the *IEEE Transactions on Power Electronics*. Since 2002 he also is an associate editor of the *Journal of Power Electronics of the Korean Institute of Power Electronics* and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*.

Gerald Deboy received the M.Sc. and Ph.D. degree in physics from the Technical University Munich in 1991 and 1996 respectively. He joined Infineon Technologies AG in 1994 and is currently heading a group looking into opportunities and requirements for emerging applications. He has authored and coauthored more than 70 papers in national and international journals including contributions to three student text books. He holds more than 60 granted international patents and has more applications pending.

Active Source Current Filtering to Minimize the DC-Link Capacitor in Switched Reluctance Drives

Annegret Klein-Hessling, Bernhard Burkhart, and Rik W. De Doncker

***Abstract*—Switched reluctance machines receive increased attention from the automotive industry because of their cost efficiency. However, the independent phase excitation and the resulting current reversal demand comparatively large dc-link capacitors to meet the requirements regarding the ripple on the dc-link voltage and current. This paper validates the effects of the usage of a dc-dc boost converter to reduce the size of the dc-link capacitor by actively filtering the source current. The active filter is compared with the state-of-the-art topology and a passive filter. The investigations show that the active filter is able to reduce the dc-link capacitance by 80%. The dc-dc converter also provides the feature of adjusting the inverter dc-link voltage level independently from the battery voltage level. The positive effect of this additional degree of freedom on the machine efficiency is investigated and due to this feature the total efficiency of the electrical drive train remains nearly unchanged despite the extra losses in the dc-dc converter. All presented results are based on detailed simulations and experimentally validated with a 20 kW switched reluctance generator.**

***Index Terms*—Active filters, converters, electric vehicles, reluctance generators, reluctance machines.**

I. Introduction

SWITCHED reluctance machines (SRMs) are cost effective, robust and very reliable. All these characteristics are required in electric generators used, for example, in electric vehicle range extenders. However, one drawback of SRMs is the comparatively large dc-link capacitor needed to smoothen the dc-link voltage caused by the high amount of magnetization energy oscillating between the dc-link capacitor and the machine [1]–[3]. A high ripple on the dc-link voltage is unwanted and increases the risk of over-voltage across the semiconductors. Additionally, in cases where the dc-link capacitor is directly connected to a voltage source such as a battery, a ripple on the dc-link voltage leads to a large source current ripple. This current ripple produces ohmic losses in the internal resistance of the source. Experiments showed that a 20 kW-SRM generator used as range extender for electric vehicles can cause extra losses in the battery that reach a few hundred watts [4]. The ripple increases even further if electric resonant frequencies of the system are excited by the frequency components of the SRM voltage waveforms.

A large dc-link capacitor increases the size, weight and price of the SRM inverter compared to inverters for conventional rotating field drives that are based on induction or synchronous machines [5]. Recent publications recommend phase switching techniques to minimize the size of the dc-link capacitor [1], [2], [6]–[8]. These switching techniques are aimed at commutating the magnetization energy stored in one phase to the next active phase without buffering it in the dc-link capacitor. However, the switching techniques assume an overlap between the SRM phases. This assumption is only fulfilled by SRMs with at least three phases. Additionally, the current in the SRM still has to remain actively controllable. Therefore, these switching techniques are not applicable for two-phase SRMs and/or SRMs in single-pulse operation.

In [6]–[8], a passive input filter is proposed to reduce the ripple on the source current. The presented passive input filter consists of an inductance L_{DC} and a dc-link capacitor with the capacitance C_{DC}. The active filter proposed in this paper is a bidirectional boost dc-dc converter. The dc-dc converter allows to actively control the current between the dc-link capacitor and the voltage source and, therefore, reduces the ripple on the source current. This filter topology is already applied for active power decoupling of single-phase systems [11]. However, this paper firstly proposed the application of the active filter to minimize the dc-link capacitor in switched reluctance drives.

Beside active filtering, the boost converter is able to eliminate the effects of the dc-link voltage level variation due to the battery state of charge (SOC) [9], [10]. The voltage of common 400 V automotive batteries in the discharged state is 100 V lower than that in the charged state [12]. On SRMs in single-pulse operation, this has a considerable effect on the machine efficiency [13].

II. Active Filtering Using a DC-DC Converter

Fig. 1 shows an equivalent circuit model of a two-phase SRM inverter connected to a battery via a cable. The battery is modeled as an ideal voltage source u_{bat} and an internal resistance $R_{i,bat}$. The cable, which connects the battery to the inverter, is modeled as a serial connection of a resistance R_{cable} and an inductance L_{cable}. The SRM inverter consists of a dc-link capacitance C_{DC} and two asymmetric half bridges with switches S_1, S_2 and S_3, S_4, respectively.

The two-phase current i_{ph} and the total SRM current i_{SRM} during single-pulse operation in generating mode [14] are shown in Fig. 1. The instantaneous total SRM current is positive

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The authors are with the Institute for Power Electronics and Electrical Drives (ISEA), RWTH Aachen University, 52066 Aachen, Germany. (email: post@isea.rwth-aachen.de)

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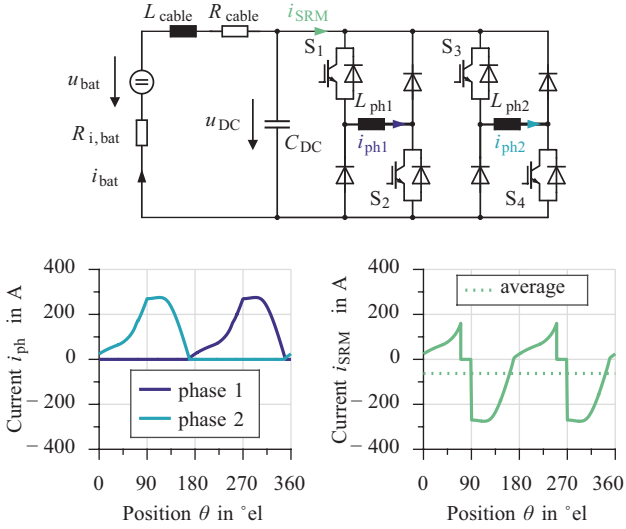


Fig. 1. Phase currents and total current of a two-phase SRM in generating mode.

TABLE I
PARAMETERS OF INVESTIGATED SRM

Parameter	Variable	Value
Number of phases	N_{ph}	2
Number of stator poles	N_s	12
Number of rotor poles	N_r	6
Rated dc-link voltage	u_{DC}	300 V
Rated speed	n_{mech}	7500 rpm
Rated power	P_{mech}	−20 kW
Outer core diameter	d_{SRM}	220 mm
Stack length	l_{SRM}	60 mm
Air gap length	l_{gap}	1 mm

during magnetization, zero during freewheeling and negative during demagnetization of one phase. No overlap of the phase currents occurs due to the low number of SRM phases. The average total SRM current $\bar{i}_{SRM} = -66.7$ A is negative because of the generating mode of the SRM. The average current is superposed with a very high peak-to-peak ripple (≈ 650%). The frequency of the oscillation is equal to the electric frequency of the SRM times the number of SRM phases.

The simulations presented in this paper are carried out using MATLAB Simulink [15] coupled with PLECS [16]. The SRM is modeled by look-up tables obtained from a stationary 2D finite element analysis (FEA) [17]. The parameters of the investigated SRM are given in Table I. The design of the SRM is investigated in detail in [4], [18]. The machine is designed for the automotive range extender application and, therefore, mainly operates in generator mode at a rated speed and power. However, due to the asymmetric rotor, the SRM is able to ramp up the combustion engine for starting.

An equivalent circuit model of the proposed active filter topology, battery, cable and SRM inverter is shown in Fig. 2. For simplification, only one SRM phase is depicted. The dc-dc converter consists of two switches $S_{DC,1}$ and $S_{DC,2}$, an inductance L_{DC} and an input capacitance C_{in}. The depicted dc-dc converter in Fig. 2 is a bidirectional boost converter with $u_{in} \leq u_{DC}$. Bidirectional

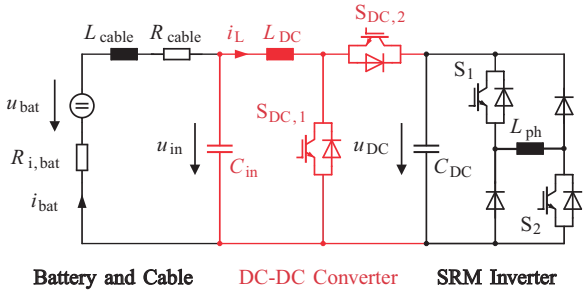


Fig. 2. Equivalent circuit of SRM with proposed active filter [13].

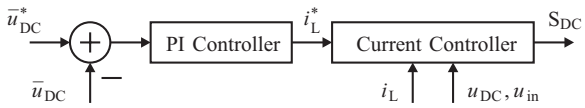


Fig. 3. Control of average dc-link voltage with active filter [13].

operation is required to operate the SRM as an integrated starter-generator (ISG), i.e., in motoring and generating mode ramp-up of the combustion engine and for nominal operation, respectively. If the SRM operates as a motor, the current through the inductor ($i_L > 0$) is controlled by switch $S_{DC,1}$. If the SRM operates as a generator, the current ($i_L < 0$) is controlled by switch $S_{DC,2}$.

A. Control of Average DC-Link Voltage

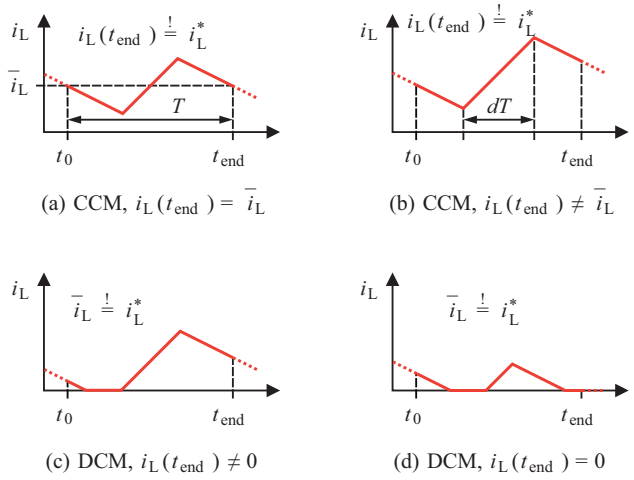
The aim of the boost converter is to supply the SRM inverter with a reference dc-link voltage u^*_{DC} and simultaneously filter the source current i_{bat}. Filtering the source current means holding the current through the inductor i_L at a nearly constant level and thereby ensuring a smooth battery current i_{bat}. This can be achieved by controlling the average dc-link voltage $\bar{u}_{DC}$ instead of the instantaneous dc-link voltage u_{DC}. In a stationary operating point, this results in a ripple on the dc-link voltage with a frequency that is equal to the electric frequency of the SRM times the number of SRM phases.

The average dc-link voltage controller is shown in Fig. 3. At the beginning of each voltage period, the average reference dc-link voltage $\bar{u}^*_{DC}$ is compared with the actual average voltage $\bar{u}_{DC}$ of the last period . The difference is fed to a PI controller, which provides the reference value for the inductor current i^*_L. Afterwards, a current controller determines the switching signals for the boost converter.

The current through the inductor is controlled with pulse-width modulation (PWM). The duty cycle d has to be calculated before each PWM period T . The current through an inductor is determined by the integration of the inductor voltage u_L divided by its inductance:

$$i_L(t) = i_L(t_0) + \frac{1}{L_{DC}} \int_{t_0}^{t} u_L(\tau)\,\mathrm{d}\tau \qquad (1)$$

As mentioned before, only one switch of the bidirectional



(a) CCM, $i_L(t_{end}) = \bar{i}_L$ (b) CCM, $i_L(t_{end}) \neq \bar{i}_L$

(c) DCM, $i_L(t_{end}) \neq 0$ (d) DCM, $i_L(t_{end}) = 0$

Fig. 4. Different cases of the predictive PWM-based current controller.

dc-dc converter is controlled in each switching period. For a positive reference current i_L^*, the duty cycle is applied to $S_{DC,1}$. Vice versa, in the case of a negative current, switch $S_{DC,2}$ is used. Therefore, the voltage u_{on} applied to the inductor during the switch conduction interval of the period depends on which switch is used:

$$u_{on} = \begin{cases} u_{in} & i_L^* > 0 \\ u_{in} - u_{DC} & \text{else.} \end{cases} \tag{2}$$

When the switches are open, the current conducts through the diodes. Depending on the sign of the current, the applied inductor voltage u_{off} is determined by:

$$u_{off} = \begin{cases} u_{in} & i_L^* < 0 \\ u_{in} - u_{DC} & \text{else.} \end{cases} \tag{3}$$

In the case of $i_L^* = 0$, both switches are open and no duty cycle is calculated. Assuming constant voltages u_{DC} and u_{in}, the current at the end of a PWM period t_{end} can be predicted from the quantities at the beginning of the PWM period t_0:

$$i_L(t_{end}) \approx i_L(t_0) + \frac{dT}{L_{DC}} u_{on}(t_0) + \frac{(1-d)T}{L_{DC}} u_{off}(t_0) \tag{4}$$

For simplification, voltage drops across the switches and diodes are not considered in the shown equations. However, they can be easily considered in the controller implementation. The duty cycle for the next PWM step can be determined by solving (4) for d depending on $i_L(t_{end})$. If center aligned PWM is assumed, four different cases have to be distinguished (Fig. 4):

(1) Steady State Continuous Conduction Mode (CCM)

SRM, dc-dc converter and its controller are in steady state. Therefore, the current reference i_L^* is the same as that of the previous PWM period. If $i_L(t_{end}) = i_L^*$ is applied to (4), the average current $\bar{i}_L$ is equal to the reference current i_L^* (Fig. 4(a)). The duty cycle is calculated by:

$$d_{CCM} = \frac{(i_L^* - i_L(t_0))L_{DC}/T - u_{off}(t_0)}{u_{on}(t_0) - u_{off}(t_0)} \tag{5}$$

(2) Transient Continuous Conduction Mode (CCM)

In this case, the current reference i_L^* has changed compared to the previous PWM period. As shown in Fig. 4(b), value $i_L(t_0)$ is not yet equal to i_L^*. To achieve steady state operation in the next PWM step, $i_L(t_{end}) = i_L^*$ is applied, resulting in the same duty cycle d_{CCM} as in (5). Due to the control of the average dc-link voltage, the current reference changes only at the first PWM step of the dc-link voltage averaging period. The averaging frequency is the electric frequency f_{el} of the SRM times the number of SRM phases N_{ph}. If $f_{el} \cdot N_{ph} << f_{PWM} = 1/T$, the average deviation from the reference current is negligible.

(3) Discontinuous Conduction Mode With $i_L(t_{end}) \neq 0$

If the absolute current reference $|i_L^*|$ becomes too small, the dc-dc converter has to change to discontinuous conduction mode (DCM). This is the case if the SRM operates in partial load. A control of $i_L(t_{end}) = i_L^*$ does not result in $\bar{i}_L = i_L^*$ anymore. With (4), the average current in dependence on the duty cycle d has to be calculated and resolved for d. Additionally, the interval in which the current is zero has to be considered. The resulting duty cycle is:

$$d_{DCM,1} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2aT} \tag{6}$$

with

$$a = \frac{u_{off}(t_0)}{8L_{DC}}$$

$$b = \frac{T}{4L_{DC}}(2u_{on}(t_0) - u_{off}(t_0))$$

$$c = \frac{u_{off}(t_0)T^2}{8L_{DC}} - \frac{i_L^2(t_0)L_{DC}}{2u_{off}(t_0)} - i_L^* T$$

(4) Discontinuous Conduction Mode With $i_L(t_{end}) = 0$

For very small current reference, the current at the end of the PWM period becomes zero. As in case (3), the average current $\bar{i}_L = i_L^*$ is controlled. Due to $i_L(t_{end}) = 0$, the duty cycle is calculated by:

$$d_{DCM,2} = \frac{1}{T}\sqrt{\frac{\frac{i_L^2(t_0)L_{DC}^2}{u_{off}(t_0)} + 2L_{DC} i_L^* T}{u_{on}(t_0) - u_{on}^2(t_0)/u_{off}(t_0)}} \tag{7}$$

To reduce the current through the inductor and increase the effective total switching frequency, it is possible to use a multi-phase dc-dc converter [19]. The multi-phase dc-dc converter

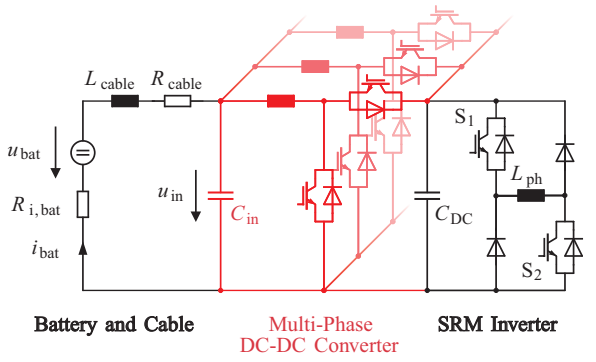


Fig. 5. Equivalent circuit of active filter with multi-phase dc-dc converter.

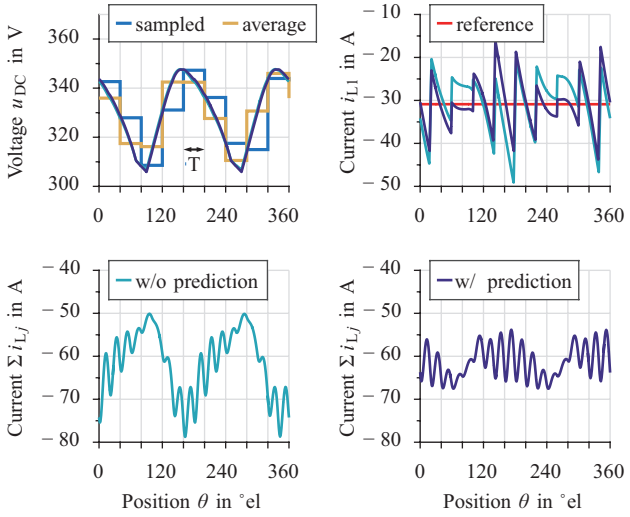


Fig. 6. Difference between sampled and predicted average dc-link voltage control.

consists of multiple single dc-dc converters connected in parallel as depicted in Fig. 5. For interleaved operation of the multi-phase dc-dc converter with N_{DC} parallel phases, the PWM signals of each converter leg j are phase shifted by jT/N_{DC} so that the resulting effective switching frequency of the converter is a multiple of the switching frequency of a single phase.

The usage of the measured voltages $u_{in}(t_0)$ and $u_{DC}(t_0)$ at the beginning of the actual PWM step in (4) is a simplification. It assumes that the voltages between two PWM steps do not vary. This does not necessarily apply to the dc-link voltage. The difference between $u_{DC}(t_0)$ and $u_{DC}(t_{end})$ depends on capacitance C_{DC} and the dc-dc converter switching frequency $f_{PWM} = 1/T$. A better approach is the usage of the average dc-link voltage during one PWM period (Fig. 6). This average voltage is not measurable at the beginning of a PWM period when the duty cycle has to be calculated.

The voltage of a capacitor is described by the integration of its current:

$$u_{DC}(t) = u_{DC}(t_0) + \frac{1}{C_{DC}} \int_{t_0}^{t} i_{DC}(\tau)\, \mathrm{d}\tau \qquad (8)$$

To calculate the dc-link voltage at the end of each PWM step,

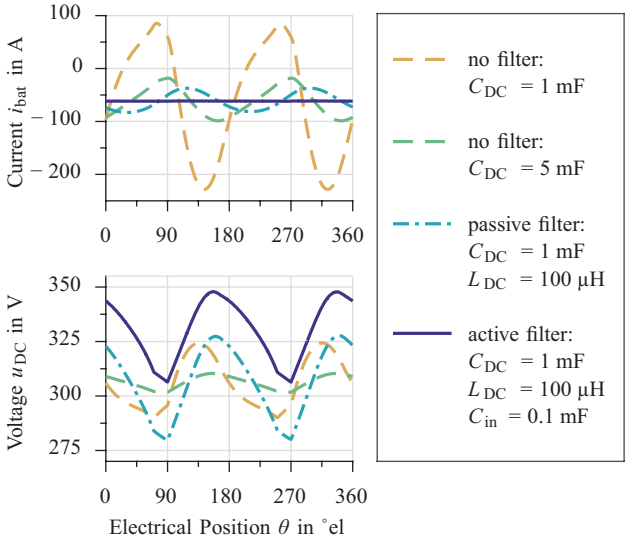


Fig. 7. Influence of different filters on source current and dc-link voltage at mechanical input power $P_{mech} = -20$ kW and speed $n = 7500$ rpm.

this equation is simplified to:

$$u_{DC}(t_{end}) \approx u_{DC}(t_0) + \frac{i_{DC}(t_0)T}{C_{DC}} \qquad (9)$$

whereas $i_{DC}(t_0) = i_L^* - i_{SRM}(t_0)$ is the average current in the dc-link capacitor during one PWM period. To improve the PWM current controller, the predicted average voltage $^1/_2\, u_{DC}(t_0) + {}^1/_2\, u_{DC}(t_{end})$ within the PWM step is calculated and used instead of the $u_{DC}(t_0)$ in (2)–(7).

Fig. 6 shows simulation results of the dc-link voltage, the current through one inductor i_{L1} of a two-phase dc-dc converter and the sum of both inductor currents $\Sigma\, i_{Lj}$. The switching frequency is $f_{PWM} = 15$ kHz. The approach without prediction uses the sampled dc-link voltage at t_0. The other approach uses the predicted average dc-link voltage. In particular, at the minimal dc-link voltage, the approach without prediction is not able to control the current through the inductor to its reference value. This results in an oscillation on $\Sigma\, i_{Lj}$. The oscillation has the same frequency as the dc-link voltage oscillation. The approach with prediction is able to eliminate this oscillation. Only the ripple due to the switching frequency has to be smoothened by the input capacitor C_{in}.

B. Filter Topology Comparison

The state-of-the-art approach to smoothen the i_{SRM}-oscillation is a conventional dc-link capacitor (Fig. 1). The resulting battery current i_{bat} and the dc-link voltage u_{DC} for the rated operating point of the SRM are shown in Fig. 7. The figure depicts the simulation results for two dc-link configurations: reduced capacitance (C_{DC} =1 mF) and required capacitance to avoid battery current reversal (C_{DC} = 5 mF).

Fig. 7 shows that only the larger dc-link capacitance suppresses the battery current reversal. However, the peak-to-peak ripple on the current is still around 120% of the average

current. With the smaller dc-link capacitance the ripple reaches around 470%.

The resulting battery current and dc-link voltage for a one-phase boost converter with f_{PWM} = 40 kHz switching frequency used as active filter are also shown in Fig. 7. The ripple on the source current is completely eliminated and the battery is charged with a dc current.

The passive input filter presented in [6]–[8] is included in the comparison in Fig. 7. The passive input filter consists only of an inductance L_{DC} and a dc-link capacitance C_{DC}. It does not have switches as the active filter. The passive filter with C_{DC} = 1 mF is able to reduce more current ripple than a 5mF-dc-link capacitance without any filter.

The comparison of the dc-link voltages shows that only the topology with large capacitance reduces the ripple to about 4% of the average voltage $\overline{u}_{DC}$ = 310 V. All topologies with a dc-link capacitance of C_{DC} = 1 mF experience a similar voltage ripple of approximately 20%. Due to the two-phase SRM, the voltage ripple appears twice per electric period. The dc-link voltage ripple has a minor influence on the SRM behavior. Due to the higher voltage at the unaligned position (θ = 180°el), the phase can be magnetized a little faster.

Since the active filter is a dc-dc boost converter, the average dc-link voltage of the active filter ($\overline{u}_{DC}$ = 335 V) is higher than the voltage in other topologies. The filter characteristic of the dc-dc converter is applicable if $u_{DC} > u_{in}$. Otherwise, the diode of switch $S_{DC,1}$ conducts and the current i_L is no longer actively controllable. The influence of the average dc-link voltage level on the SRM behavior will be discussed in Section III-A.

The passive filter is designed for one specific operating point. In this paper, for a better comparison between the topologies, the passive filter is designed for the rated operating point of the investigated SRM. In [6]–[8], a design for the 'worst case' operating point is recommended. For the observed SRM in this paper, this operating point would be at a low speed and rated torque. A design for this operating point results again in a large capacitance (> 5 mF) or a large inductance (> 1 mH). A large inductance limits the dynamic behavior of the SRM, e.g., during ramp-up. Fast changes of the SRM torque are no longer possible because of the slower current gradient ($di_L/dt \sim 1/L_{DC}$).

A comparison of the resulting battery current i_{bat} and the dc-link voltage u_{DC} for two different speeds (rated speed and half rated speed) with a passive and an active filter is displayed in Fig. 8. The mechanical input torque of the switched reluctance generator is kept constant for all operating points at a rated torque of −25.5 Nm, resulting in a mechanical input power of −10 kW and −20 kW, respectively. It can be seen, that in the case of the passive filter, the current ripple increases with decreasing speed. At 3750 rpm, the peak current reaches up to 60 A, i.e., the peak-to-peak ripple is about 200% of the average battery current.

With the active filter, different operating points have no influence on the battery current ripple. The battery current is kept constant for both speeds. In addition, the dc-link voltage ripple is affected more for the passive filter at a low speed. The investigation shows the major advantages of the active filter compared to the passive filter. Its behavior and filter capability

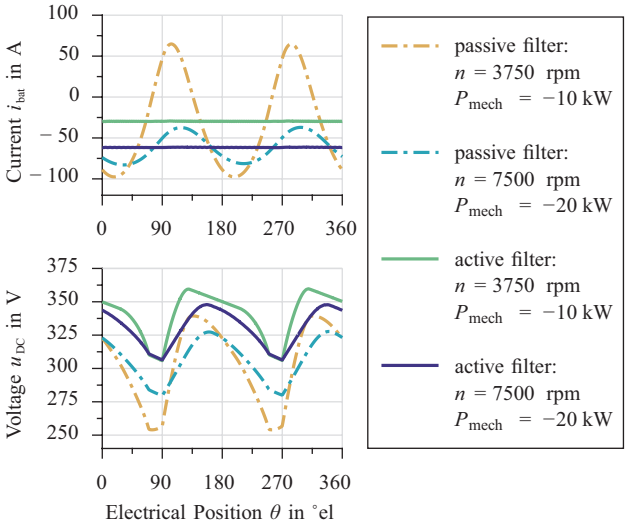


Fig. 8. Influence of speed on the operation of the range extender using active and passive current filter at a rated torque of −25.5 Nm.

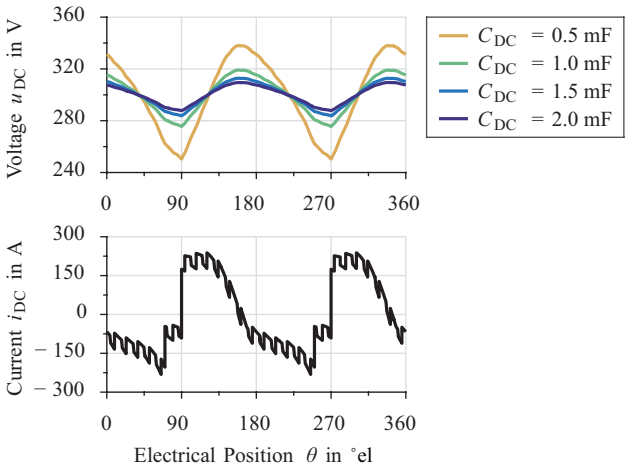


Fig. 9. Effect of different dc-link capacitances on dc-link voltage u_{DC} and capacitor current i_{DC}.

are independent of the SRM operating point.

C. DC-Link Capacitance Minimization

The main purpose of the dc-dc boost converter is the reduction of the dc-link capacitance by actively filtering the SRM dc power. The dc-link capacitance C_{DC} does not directly affect the filtering capability. Only the dc-link voltage oscillation and, therefore, the converter control are affected by the dc-link capacitance. The effect is investigated in Fig. 9 for the rated operating point and a battery voltage of u_{bat} = 250 V. The dc-link voltage u_{DC} and the capacitor current i_{DC} are shown.

The capacitor current is not affected by the capacitance C_{DC}. The capacitor current is the difference of the total SRM current i_{SRM} and the current through the diode or switch $S_{DC,2}$. The dc-link voltage ripple amplitude has an anti-proportional relation to the capacitance. In the converter design, the voltage ripple needs to be limited to avoid the risk of over-voltage across the semiconductors. In addition, the boost converter is only able to

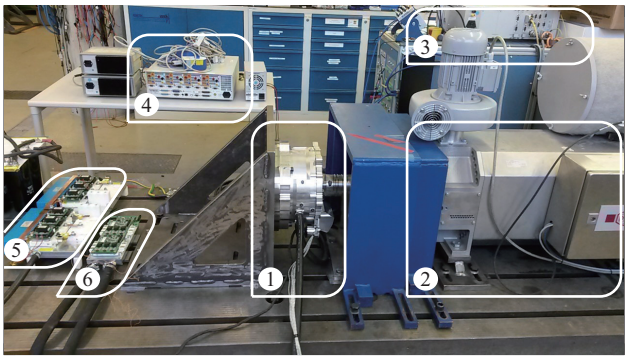


Fig. 10. Test bench setup: ① SRM. ② Load machine (IM). ③ Torque and speed probe unit. ④ Electrical power analyzer. ⑤ SRM inverter with integrated dc-dc converter switches. ⑥ DC-DC converter inductors.

apply its filter capability if the dc-link voltage is larger than the input voltage. The dc-link capacitance for the inverter is chosen to be C_{DC} = 1 mF. This is a reduction by 80% compared to the capacitance required by the state-of-the-art topology without the filter to avoid battery current reversal (C_{DC} = 5 mF).

The capacitor losses P_C can be separated into dielectric losses and ohmic losses [20]. Dielectric losses are mainly determined by the product of capacitance and peak-to-peak voltage ripple. As the dc-link voltage ripple is anti-proportional to the capacitance, the product remains constantly independent of the dc-link capacitance. The ohmic capacitor losses are affected by the rms inductor current. The inductor current remains constant for all capacitance variations. Therefore, the capacitor losses do not depend on the capacitance. The capacitor losses for the built-up capacitor are approximately $P_C \approx 6.7$ W in the rated operating point of the investigated SRM. The losses are small compared to the inductor and semiconductor losses and are neglected in the following.

III. Measurement Results and Validation

The proposed active filter is validated by measurements on a test bench for electrical drives. The parameters of the range extender SRM [4] are the same as investigated in the simulations in the previous section. The investigations focus on the rated operating point due to the range extender application. Especially, the internal combustion engine experiences a large efficiency drop under partial load operation. The SRM inverter consists of four half bridges of two B6-IGBT-modules (HybridPACK 2, Infineon [21]). The two unused phase legs of the B6-modules are used for a two-phase dc-dc converter. Each inductor is designed for an inductance L_{DC} = 214 µH. The input capacitance is C_{in} = 330 µF and the dc-link capacitance C_{DC}=1 mF.

A picture of the test bench setup is presented in Fig. 10. It shows the SRM inverter and the inductors of the dc-dc converter including printed circuit boards (PCBs) for voltage and current measurements. Due to the dc-dc converter, the capacitance is reduced by 80% (Section II-B). This leads to a volume and weight reduction of the drive system, as the capacitor weight and volume are proportional to the capacitance. Fig. 10 shows that the minimized capacitor (blue rectangle) is approximately

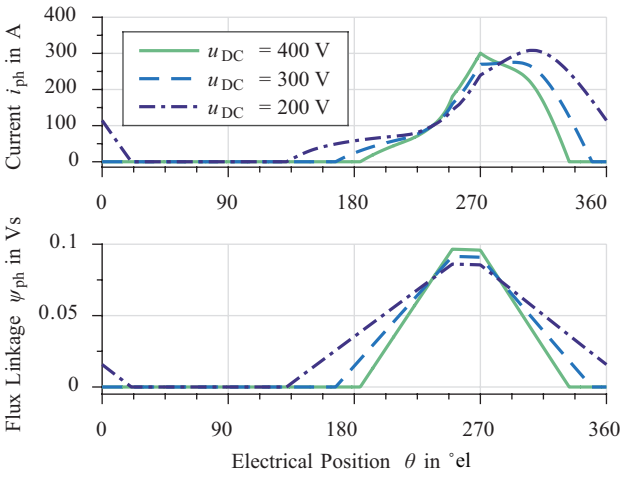


Fig. 11. Phase current and flux-linkage trajectories for different dc-link voltages at mechanical input power P_{mech} = −20 kW and 7500 rpm.

the same volume as the additional components due to the dc-dc converter. This results in a volume reduction by 60% of the proposed power electronic topology compared to the state-of-the-art topology without the filter.

A. Influence of DC-Link Voltage on SRM

Apart from filtering the source current, the dc-dc converter can be used to adjust the dc-link voltage level. The average dc-link voltage has an influence on the phase current i_{ph} and the phase-flux linkage ψ_{ph} of the SRM. Both values are important for the losses occurring in the SRM and, therefore, the efficiency of the drive system.

Fig. 11 shows the effect of the different dc-link voltages on the trajectories of the phase current and phase flux-linkage for one electrical period at the rated operating point (7500 rpm, −20 kW). The SRM is designed for a battery with a rated voltage of 300 V. The minimum voltage at a low SOC level is assumed to be 200 V. 400 V is assumed to be the maximum boosted voltage. Each operating point is optimized for the best efficiency as presented in [22]. The gradient of the flux-linkage is proportional to the dc-link voltage. Therefore, the conduction time per period increases with decreasing dc-link voltages. The efficiency optimization of the control parameters results in an increased free-wheeling time with increasing dc-link voltages. The peak value of the phase currents remains nearly constant for different voltage levels. The rms value of the phase current, however, increases for decreased dc-link voltages, as a longer conduction time is required.

The SRM losses are measured on a test bench as well as simulated by a coupled 2D-FEA simulation using MATLAB Simulink [15] and FLUX 2D [17]. On the test bench, the mechanical power is measured with a torque and speed probe [23]. The electrical powers are determined by current and voltage probes [24], [25] at the terminals of the SRM and at the dc terminals. The SRM losses and the inverter losses are calculated from the difference of the measured powers. Therefore, it is not possible to break down the different loss types of the SRM and its inverter. The simulation of the SRM

TABLE II
IRON LOSS PARAMETERS FOR MATERIAL NO30 [27]

$k_1 = 2.03 \cdot 10^{-2}$	$\alpha_1 = 1$	$\beta_1 = 1.76$
$k_2 = 2.63 \cdot 10^{-5}$	$\alpha_2 = 2$	$\beta_2 = 2$
$k_3 = 7.02 \cdot 10^{-6}$	$\alpha_3 = 1.5$	$\beta_3 = 1.5$
$k_4 = 4.43 \cdot 10^{-4}$	$\alpha_4 = 2$	$\beta_4 = 4.89$

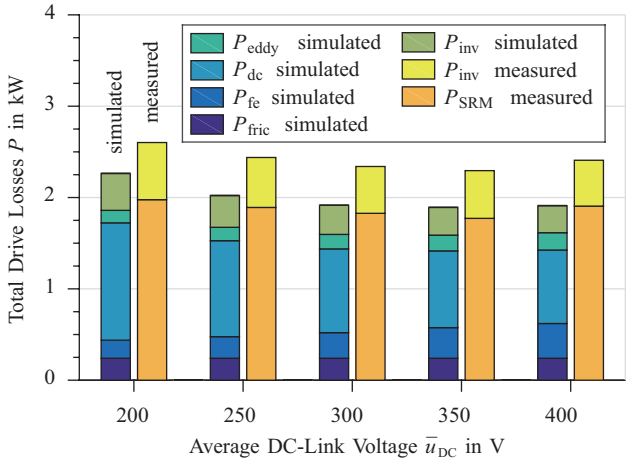


Fig. 12. Influence of different dc-link voltages on SRM losses.

considers copper losses in the windings, including ohmic losses P_{dc} and eddy current losses P_{eddy} [26], as well as iron losses P_{fe} in the rotor and stator. Equation (10) is applied to the simulated flux density of each finite element to determine the specific iron losses p_{fe} [27], [28]:

$$p_{fe} = k_1 \hat{B}^{\beta_1} f^{\alpha_1} + k_2 \hat{B}^{\beta_2} f^{\alpha_2} + k_3 \hat{B}^{\beta_3} f^{\alpha_3} + k_4 \hat{B}^{\beta_4} f^{\alpha_4} \quad (10)$$

The equation is the sum of four Steinmetz terms $k\hat{B}^{\beta} f^{\alpha}$, where $\hat{B}$ is the peak flux density and f is the fundamental frequency of the flux density [29]. The material-specific so-called Steinmetz parameters k, α and β are obtained by fitting of loss measurements and given for the used iron sheet material NO30 in Table II. Due to the non-sinusoidal flux waveforms of SRMs, the improved generalized Steinmetz equation (IGSE) [30] is applied to each Steinmetz term. The iron losses P_{fe} are determined from the specific iron losses p_{fe} by volume integration and multiplication with the material density as well as the stacking factor of the iron sheets.

Mechanical friction losses P_{fric} including bearing losses and windage losses due to the double salient structure of the SRM are considered [31], [32]. The losses in the semiconductors of the SRM inverter P_{inv} are calculated according to the data sheets provided by the manufacturer [21]. Switching and conduction losses in switches and diodes are considered.

The resulting total losses of the SRM and its inverter at a mechanical input power of −20 kW and 7500 rpm are shown in Fig. 12. The ohmic copper losses and inverter losses are strongly dependent on the rms current and, therefore, are reduced at higher voltages. The iron losses depend on the peak flux-linkage and the gradient of the flux linkage $d\psi/dt$. According

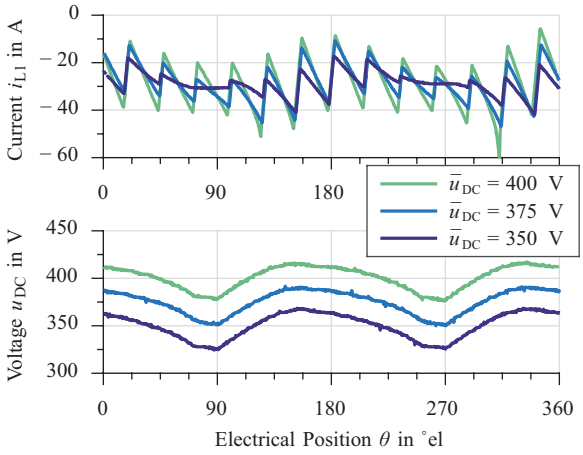


Fig. 13. Measured inductor current and dc-link voltage trajectories for different average dc-link voltages at u_{bat} = 325 V.

to the observation from Fig. 11, the iron losses increase for increased dc-link voltage level.

Simulation and measurement results show good correlation. The simulated losses are lower for all observed operating points. This might be due to non-simulated effects such as conducting resistance between connections and the thermal dependency of the iron loss parameters. The measurement inaccuracy of the torque sensor is approximately ±25 W at the rated SRM power [23].

The overall losses decrease with an increasing dc-link voltage level. Between 200 V and 350 V, the measured efficiency improves from η_{200V} = 87% to η_{350V} = 88.5%, i.e., $\Delta\eta \approx 1.5\%$, and decreases only slightly for 400 V. If only the SRM and its inverter are considered, it is recommended to operate the SRM at a dc-link voltage of 300 V or higher.

B. Influence of DC-Link Voltage on DC-DC Converter

Similar to the SRM and its inverter, the efficiency of the dc-dc converter also depends on the choice of the dc-link voltage. As visible in (4), the current through the inductor depends on the input voltage u_{in} and the difference between input voltage and dc-link voltage $\Delta u = u_{in} - u_{DC}$. The measured inductor currents of one-phase i_{L1} and dc-link voltages for a battery voltage of u_{bat} = 325 V at −20 kW and 7500 rpm for different levels of average dc-link voltages are shown in Fig. 13. The PWM current controller with a switching frequency f_{PWM} = 10 kHz and an average dc-link voltage prediction, as explained in Section II-A, is implemented.

The average inductor current i_{L1} is independent of the average dc-link voltage. The current is determined by the battery voltage, the mechanical power of the SRM and the number of dc-dc converter phases. The ripple on the current increases with the voltage difference Δu because the gradient di_L/dt during magnetization is proportional to this difference. The gradient of the current during demagnetization is proportional to the input voltage (equation (4)). Hence this gradient is constant for all cases. It can be noted that the inductor saturates around $|i_L|$ = 45 A. Fig. 13 also shows that

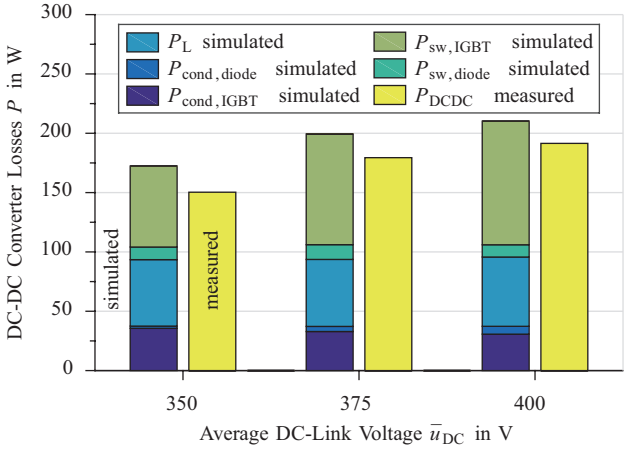


Fig. 14. Losses of dc-dc converter at battery voltage $u_{bat} = 325$ V .

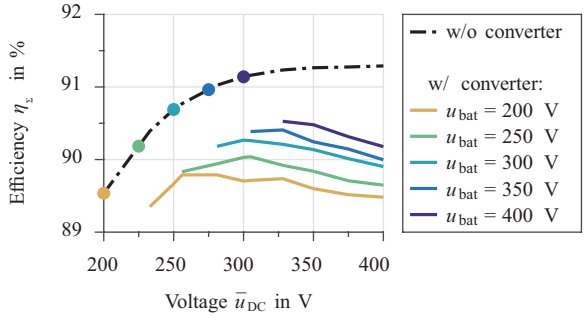


Fig. 15. Simulated total drive efficiency for different battery voltages at mechanical input power $P_{mech} = -20$ kW and speed $n = 7500$ rpm.

the ripple on the dc-link voltage depends on the average dc-link voltage level. The ripple decreases for increased voltage levels.

The resulting simulated inductor losses P_L and the simulated losses in the IGBTs and diodes of the dc-dc converter are depicted in Fig. 14. The semiconductor losses are separated into switching losses P_{sw} and conduction losses P_{cond}. Again the measurements show only the total dc-dc converter losses P_{DCDC}. Therefore, the simulation results are used to separate the losses by their origin.

The IGBT switching losses depend on the switching frequency, the voltage across the device and the current during turn-on and turn-off. The switching frequency is the same for all investigated average dc-link voltage levels. The negative current peaks and the voltage difference between input and dc-link voltage increase for higher average dc-link voltages (Fig. 13). Therefore, the IGBT switching losses increase.

The conduction losses are mainly affected by the rms current through the semiconductors. The duty cycle determines the ratio of the period in which the switch is closed and the current conducted through it. The average absolute duty cycle $|\bar{d}|$ per electrical period decreases with increasing average dc-link voltage. Therefore, depending on the duty cycle, the conduction losses of the IGBTs decrease while the conduction losses of the diode increase with an increasing dc-link voltage. The total semiconductor losses of the dc-dc converter increase with an increasing dc-link voltage.

Similar to the losses in an SRM, the losses occurring in the inductors consist of iron losses and copper losses. The inductors are built with ferrite cores and litz wire. The flux density in the inductor is calculated in an analytical approach. Due to the non-sinusoidal current waveforms, the iGSE is used [30]. Eddy currents are neglected in the copper loss calculation of the windings because high-frequency litz wire is used. For the considered operating points, the copper losses clearly dominate the iron losses. Therefore, the inductor losses increase slightly with the increasing average dc-link voltage as the rms inductor current increases slightly with a higher current ripple.

In conclusion, the losses in the dc-dc converter are mainly determined by the switching losses. The switching losses can be reduced by reducing the switching frequency of the converter [13]. However, this reduction is limited by the saturation of the inductor at the negative peak current. To increase the current level at which the inductors start to saturate, the magnetic cross section of the core has to be increased. A trade-off between the inductor size and dc-dc converter losses has to be made. As shown in Fig. 14, at a switching frequency of 10 kHz, the measured efficiency of the dc-dc converter $\eta_{DCDC} = P_{el,out}/P_{el,in}$ is above 98.9% for all operating points.

C. Total Drive Train Efficiency

The total drive train efficiency $\eta_\Sigma = P_{el,out}/P_{mech}$ without a dc-dc converter is shown by the dashed line in Fig. 15. The previously investigated battery voltage levels are marked with dots on this dashed trajectory. In addition, Fig. 15 presents the efficiency of the electric drive train consisting of SRM, machine inverter and dc-dc converter with a reduced dc-link capacitance (solid lines). The presented validation is simulation based to generate a complete efficiency map. The simulation assumes an inductor design which is able to boost the minimum battery voltage of $u_{bat} = 200$ V to the maximum allowed average dc-link voltage of $u_{DC} = 400$ V of the SRM drive train without reaching magnetic saturation. The horizontal gaps between the dots on the dashed line and the starting points of the trajectories with dc-dc converter result from the converter control condition $u_{DC} > u_{in}$.

For a battery voltage of $u_{bat} = 200$ V and an average dc-link voltage u_{DC} between 240 V and 350 V, the losses with the use of a dc-dc converter are lower than the losses without the use of a converter (dot at 200V on w/o converter trajectory). Therefore, for this operating points, the dc-dc converter increases the total efficiency of the electric drive train in addition to reducing the size of the dc-link capacitance and the dc-power filtering. For higher battery voltages, the losses with a dc-dc converter are higher than that without a dc-dc converter. In the worst case at $u_{bat} = 300$ V, the absolute difference between the efficiency with and without the converter is $\Delta\eta = 0.56\%$ of the absolute mechanical SRM power. Therefore, the total drive train efficiency remains nearly unchanged despite the extra losses in the dc-dc converter.

D. Transient Behavior of the Active Filter

To examine the dynamic performance of the dc-dc converter

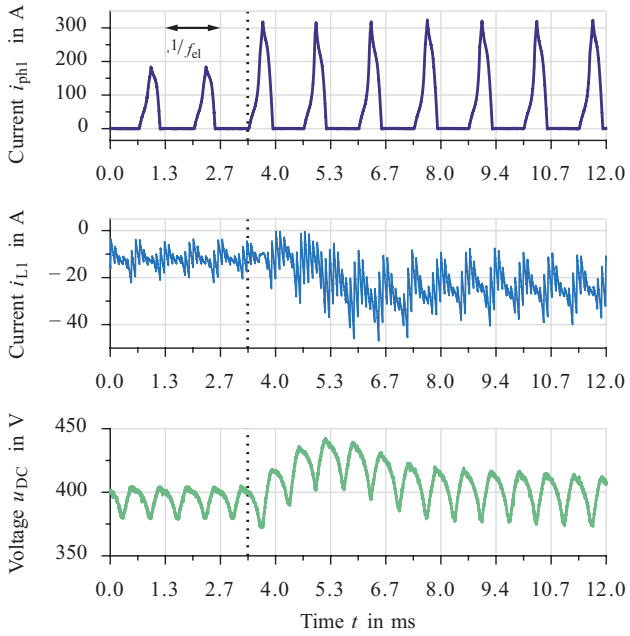


Fig. 16. Measured load step from $P_{mech} = -10$ kW to $P_{mech} = -20$ kW at constant speed $n = 7500$ rpm, $u_{bat} = 375$ V and $\vec{u}^{*}_{DC} = 395$ V.

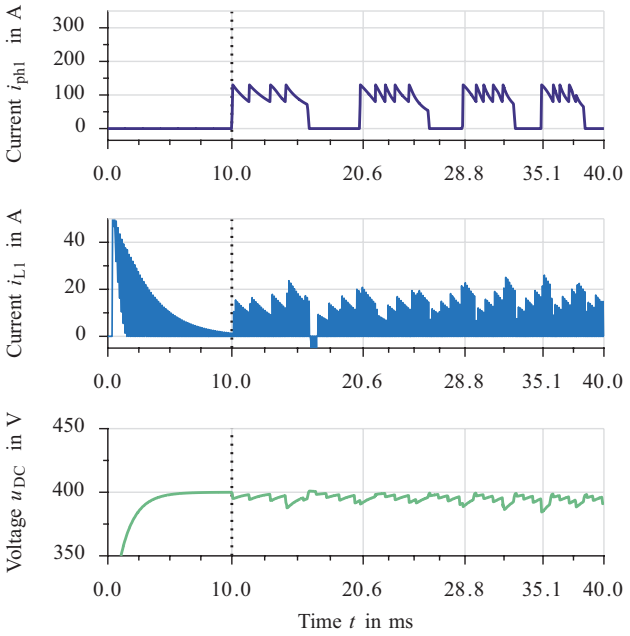


Fig. 17. Simulated ramp-up from $n = 0$ rpm to $n = 2000$ rpm at constant average torque $T = 6.3$ Nm, $u_{bat} = 300$ V and $\vec{u}^{*}_{DC} = 400$ V.

controller, an instantaneous load step of the SRM is investigated. Due to the highly dynamic behavior of an SRM, a load change within one electrical period $1/f_{el}$ is feasible. This investigation is a worst case scenario. Indeed, in a range extender application, load ramps over a few seconds are more realistic. Fig. 16 shows the load step response from half rated torque to rated torque after 2.5 electrical SRM periods ($t = 3.3$ ms). A constant speed is ensured by the load machine of the test bench.

Due to the load step, the average dc-link voltage $\bar{u}_{DC}$ increases. The PI controller responds to this increase by decreasing the current reference i^{*}_{L}. After approximately $\Delta t = 8$ ms (six electrical SRM periods equal one rotation of the SRM rotor), steady state operation is reached. The experiment proves that the controller of the dc-dc converter is able to respond to highly dynamic load changes.

Fig. 17 presents the transient behavior under motoring operation. In the range extender application, the motoring operation is only used to ramp up the combustion engine. In the first step, the dc-link is precharged to $u_{DC} = 400$ V. At $t = 10$ ms, an constant average torque is applied to ramp up the system from standstill to $n = 2000$ rpm. Due to the low speed, the SRM does not operate in single-pulse operation but in hysteresis current control. For this reason, the dc-link voltage controller operates at a fixed sampling rate instead of the average dc-link voltage. The dc-dc converter operates in DCM due to the lower required power compared to the rated operating point. The validation proves that the controller of the dc-dc converter is capable of handling the dynamic load change of the ramp-up routine.

IV. Conclusion

The investigations in this paper have shown that by using a dc-dc converter, it is possible to actively filter the source current. With the dc-dc converter, the value of the dc-link capacitor can be reduced by 80% compared to the state-of-the-art solution. The hardware setup showed that this results in a volume reduction by 60%. Contrary to the behavior of a passive filter, the operating point of the SRM has no effect on the filter quality. Additionally, the investigations have shown that the ability of the dc-dc converter to adjust the dc-link voltage independent of the state of charge of the battery improves the efficiency of the investigated switched reluctance machine and its inverter. The total efficiency of the electric drive train, therefore, remains nearly unchanged despite the extra losses in the dc-dc converter.

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References

[1] C. R. Neuhaus, N. H. Fuengwarodsakul, and R. W. De Doncker, "Control scheme for switched reluctance drives with minimized dc-link capacitance," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2557–2564, 2007.

[2] C. R. Neuhaus, "Schaltstrategien für geschaltete Reluktanzantriebe mit kleinem Zwischenkreis," Ph.D. dissertation, Shaker Verlag, Aachen, Germany, 2011.

[3] H. Wu, D. Winterborne, M. Ma, V. Pickert, and J. Widmer, "DC link capacitors for traction SRM drives in high temperature automotive environments: A review of current issues and solutions," in *Hybrid Elect. Veh. Conf. (2013)*, pp. 1–6.

[4] R. Inderka, S. von Malottki, C. Nizzola, B. Burkhart, A. Klein-Hessling, and R.W. De Doncker, "Cost efficient switched reluctance generator for range extension unit," in *25th Aachen Colloq. Automobile Engine Technol.*, 2016, pp. 1–10.

[5] D. Winterborne, M. Ma, H. Wu, V. Pickert, J. Widmer, P. Barrass, and L.

Shah, "Capacitors for high temperature dc link applications in automotive traction drives: Current technology and limitations," in *15th Eur. Conf. Power Electron. Appl. (EPE-ECCE Europe)*, 2013, pp. 1–7.
[6] W. Suppharangsan and J. Wang, "A new switching technique for dc-link capacitor minimisation in switched reluctance machine drives," in *5th IET Int. Conf. Power Electron., Mach. Drives (PEMD)*, 2013, pp. 1–6.
[7] W. Suppharangsan and J. Wang, "Experimental validation of a new switching technique for dc-link capacitor minimization in switched reluctance machine drives," in *IEEE Int. Elect. Mach. Drives Conf. (IEMDC)*, 2013, pp. 185–193.
[8] W. Suppharangsan and J. Wang, "Switching technique for minimisation of dc-link capacitance in switched reluctance machine drives," *IET Elect. Syst. Transport.*, vol. 5, no. 4, pp. 2557–2564, 2015.
[9] H.-C. Chang and C.-M. Liaw, "An integrated driving/charging switched reluctance motor drive using three-phase power module," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1863–1775, 2011.
[10] H.-C. Chang and C.-M. Liaw, "On the front-end converter and its control for a battery powered switched-reluctance motor drive," *IEEE Trans. Ind. Electron.*, vol. 23, no. 4, pp. 2143–2156, 2008.
[11] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, 2016.
[12] *Advanced Vehicles*, Idaho National Laboratory, [Online]. Available: https://avt.inl.gov/vehicle-type/all-powertrain-architecture, Accessed: Feb., 2018.
[13] A. Klein-Hessling, B. Burkhart, and R. W. De Doncker, "Active source current filtering to minimize the DC-link capacitor in switched reluctance drives," in *2nd IEEE Annu. Southern Power Electron. Conf. (SPEC)*, Dec. 2016, pp. 1–7.
[14] A. Klein-Hessling, B. Burkhart, and R. W. De Doncker, "The effect of excitation angles in single-pulse controlled switched reluctance machines on acoustics and efficiency," in *17th Int. Conf. Elect. Mach. Syst. (ICEMS)*, 2014, pp. 2661–2666.
[15] *Matlab Simulink*, MathWorks. [Online]. Available: http://de.mathworks.com/products/simulink/, Accessed: Feb., 2018.
[16] *Plecs*, Plexim. [Online]. Available: http://www.plexim.com/plecs/, Accessed: Feb., 2018.
[17] *Flux 2D*, CEDRAT. [Online]. Available: http://www.cedrat.com/software/flux/, Accessed: Feb., 2018.
[18] B. Burkhart, "Switched reluctance generator for range extender applications – Design, control and evaluation," Ph.D. dissertation, RWTH Aachen University, Aachen, Germany, 2018.
[19] B. A. Miwa, D. M. Otten, and M. E. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Appl. Power Electron Conf. Expo. (APEC)*, 1992, pp. 557–568.
[20] *Medium Power Film Capacitors*, AVX . [Online]. Available: http://www.avx.com/products/film-capacitors/medium-power-film-caps/ ffveffvi-ffweffwi-rohs-compliant/, Accessed: Apr., 2018.
[21] *HybridPack 2, FS800R07A2E3*, Infineon. [Online]. Available: http://www.infineon.com/, Accessed: Feb., 2018.
[22] B. Burkhart, A. Klein-Hessling, S. A. Hafeez, and R. W. De Doncker, "Influence of freewheeling on single pulse operation of a switched reluctance generator," in *19th Int. Conf. Elect. Mach. Syst. (ICEMS)*, 2016, pp. 1–6.
[23] *Torque meter* FLFM1, ATESTEO. [Online]. Available: http://www.atesteo.com/en/testing-equipment/torquemeters/, Accessed: Feb., 2018.
[24] *Power Analyzer LMG450*, ZES Zimmer, [Online]. Available:https://www.zes.com/en/Products/Precision-Power-Analyzers/LMG450, Accessed: Sept., 2018.
[25] *Current Transducer LF 2010-S/SPA7*, LEM. [Online]. Available: https://www.lem.com/sites/default/files/products_datasheets/lf_2010-s_spa7.pdf, Accessed: Sept., 2018.
[26] M. Schenk, "Simulative Untersuchung der Wicklungsverluste in Geschalteten Reluktanzmaschinen," Ph.D. dissertation, Shaker Verlag, Aachen, Germany, 2016.
[27] A. Klein-Hessling, B. Burkhart, and R.W. De Doncker, "Iron loss redistribution in switched reluctance machines using bidirectional phase currents," in *8th IET Int. Conf. Power Electron., Mach. Drives (PEMD)*, 2016.
[28] D. Eggers, S. Steentjes, and K. Hameyer, "Advanced iron-loss estimation for nonlinear material behavior," *IEEE Trans. Magn.*, vol. 48, no. 11, pp. 3012–3024, 2012.
[29] C. P. Steinmetz, "On the law of hysteresis," *Trans. Amer. Inst. Elect. Eng.*, vol. IX, no. 1, pp. 1–64, 1892.
[30] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *IEEE Workshop Comput. Power Electron.*, Dec. 2016, pp. 36–41.
[31] J. E. Vrancik, "Prediction of windage power loss in alternators," *NASA technical note D-4849*, Lewis Research Center, Cleveland, USA, 1968.
[32] R. Wrobel, G. Vainel, C. Copeland, T. Duda, D. Staton, and P. H. Mellor, "Investigation of mechanical loss components and heat transfer in an axial-flux PM machine," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3000–3011, 2015.

Annegret Klein-Hessling was born in Germany in 1986. She received the Diploma degree in electrical engineering and the Diploma degree in industrial engineering from the RWTH Aachen University, Germany, in 2012. Since October 2012, she has been a research associate at the Institute of Power Electronics and Electrical Drives (ISEA) at the RWTH Aachen University, Germany. Her research interests include the field of switched reluctance drives and their control.

Bernhard Burkhart was born in Germany in 1985. He received the Diploma degree in electrical engineering from the RWTH Aachen University of Aachen, Germany in 2011. Since November 2011, he has been a research associate at the Institute of Power Electronics and Electrical Drives (ISEA) at the RWTH Aachen University, Germany. His research interests include the field of switched reluctance machine design and control, especially for generators.

Rik W. De Doncker received the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1986. In 1987, he was appointed as a Visiting Associate Professor at the University of Wisconsin, Madison. After a short stay as an Adjunct Researcher with Interuniversity Microelectronics Centre, Leuven, he joined, in 1989, the Corporate Research and Development Center, General Electric Company, Schenectady, NY. In 1994, he joined the Silicon Power Corporation, a former division of General Electric Inc., as the Vice President of Technology. In 1996, he became a Professor at the RWTH Aachen University, Aachen, Germany, where he currently leads the Institute for Power Electronics and Electrical Drives. Since 2006, he has been the Director of the E.ON Energy Research Center, RWTH Aachen University. Dr. De Doncker was the President of the IEEE Power Electronics Society (PELS) in 2005 and 2006. He was the founding Chairman of the German IEEE Industry Applications Society PELS Joint Chapter. In 2002, he was the recipient of the IEEE IAS Outstanding Achievement Award. In 2008, he received the IEEE PES Nari Hingorani Custom Power Award. In 2009, he led a VDE/ETG Task Force on Electric Vehicles. In 2010, he received an honorary doctor degree from Riga Technical University, Latvia. In 2013, he received the IEEE William E. Newell Power Electronics Award.

Origin and Quantification of Increased Core Loss in MnZn Ferrite Plates of a Multi-Gap Inductor

Dominik Neumayr, Dominik Bortis, Johann W. Kolar, Stefan Hoffmann, and Eckart Hoene

Abstract—**Inductors realized with high permeable MnZn ferrite require, unlike iron-powder cores with an inherent distributed gap, a discrete air gap in the magnetic circuit to prevent saturation of the core material and/or tune the inductance value. This large discrete gap can be divided into several partial gaps in order to reduce the air gap stray field and consequently the proximity losses in the winding. The multi-gap core, realized by stacking several thin ferrite plates and inserting a non-magnetic spacer material between the plates, however, exhibits a substantial increase in core losses which cannot be explained from the intrinsic properties of the ferrite. In this paper, a comprehensive overview of the scientific literature regarding machining induced core losses in ferrite, dating back to the early 1970s, is provided which suggests that the observed excess core losses could be attributed to a deterioration of ferrite properties in the surface layer of the plates caused by mechanical stress exerted during machining. However, in a first experimental analysis no structural evidence for a deteriorated layer close to the surface is identified by means of Scanning Electron Microscopy (SEM). Therefore, in a next step, a new calorimetric measurement setup based on temperature rise monitoring is proposed in this paper in order to quantify and differentiate between core losses associated with the bulk and the surface of the ferrite plates and therefore to pinpoint the measured excess core loss to shallow layers of ferrite with deteriorated magnetic performance. Electrical measurement of the surface related core losses utilizing the widely accepted two-winding wattmeter method with reactive power compensation is outlined in the appendix but was not employed in this work due to comparably low measurement accuracy. By means of the proposed measurement technique, the bulk and surface core loss density of the MnZn ferrite material 3F4 from FerroxCube was determined for sinusoidal flux density amplitude varying from 75 mT up to 200 mT and excitation frequencies ranging from 200 kHz to 1 MHz. The measured core loss densities (W/cm^3) show good agreement with the Steinmetz model provided by the manufacturer validating the proposed calorimetric core loss measurement technique. The measured surface loss density (W/cm^2) can also be well predicted with a Steinmetz model, whereby the frequency exponent α in the surface is slightly smaller and the flux density exponent β is slightly larger compared to the Steinmetz parameter of the bulk ferrite. It is shown that the ratio between surface and bulk core losses of a composite core assembled from individual plates is only a function of plate thickness and does not depend on the actual cross section area. Critical plate thickness is then defined to be reached when the total power loss in the composite core has doubled compared to a solid (single-piece) core sample. This new quantity provides a very helpful figure for multi-gap inductor designs. Besides the deteriorated surface layers, several other mechanisms potentially contributing to increased core losses in multi-gap inductors were identified and are finally discussed in the appendix of this paper: flux crowding in the core due to tolerances and imperfections in machining and assembly; deterioration of ferrite properties due to pressure buildup in the stack of plates during the curing of the employed epoxy resin; ohmic loss in the ferrite associated with the current flowing in the conduction path provided by the low impedance of the ferrite material at high frequencies and the parasitic capacitance between winding and the ferrite core.**

Index Terms—**Distributed air gap, high Q inductor, machining induced loss, MnZn ferrite, multi-gap inductor, surface loss.**

I. Introduction

In high power density converter systems, the switching frequency is increased substantially in order to strongly reduce the required inductance value and the volume of the employed power inductor. Very compact input inductors of PFC rectifiers and output inductors of inverters or DC/DC converters also feature a high current ripple which demands suitable core materials — at high frequencies preferable ferrite — and sophisticated inductor designs in order to keep the core and winding losses to a minimum. Inductors realized with high permeable ferrite materials require, unlike iron-powder cores with an inherent distributed gap, a discrete air gap in the magnetic circuit to prevent saturation of the core material and/or tune the inductance value. This large discrete air gap can be divided into several partial gaps in order to reduce the air gap stray field and consequently the proximity losses in the winding, especially if copper foil is used to implement the winding (cf., Fig. 1(a) and (b)). If the partial gaps are distributed over the entire length of the inner limb of an E-type core, the H-field in the winding window shows a quasi one-dimensional field distribution running in parallel to the inner limb [1]–[3]. This allows to implement the winding with copper foil which achieves a higher filling factor compared to HF litz wire, since the individual layers of the foil winding are aligned in parallel with the H-field and excessive eddy current losses can be avoided.

Following this idea, ETH Zurich together with Fraunhofer

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D. Neumayr, D. Bortis, and J. W. Kolar are with the Power Electronic Systems Laboratory, ETH Zurich, ETL I12, Physikstrasse 3, 8092 Zurich, Switzerland (e-mail: neumayr@lem.ee.ethz.ch).

S. Hoffmann and E. Hoene are with Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin, Germany.

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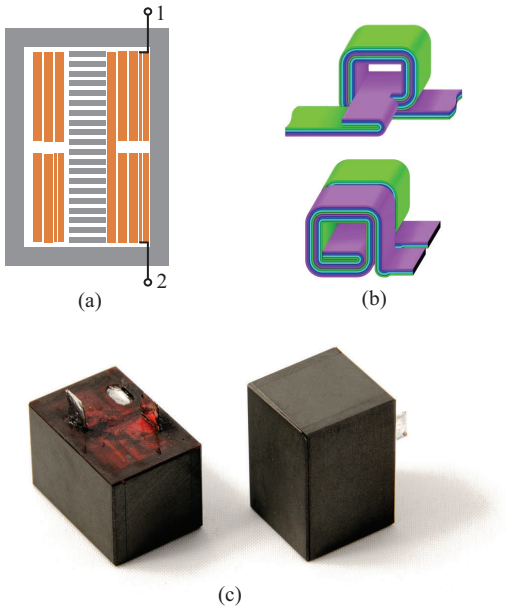

Fig. 1. (a) Structure of the foil winding multi-gap inductor with the center limb of the E-type core being composed of stacked ferrite plates. (b) Foil winding arrangement to achieve equal current sharing in parallel foils which has both connection terminals at the outside of the winding [4], [5]. (c) Hardware picture of the realized 10.5 µH multi-gap HF inductor employed in the Google Little Box Challenge converter [6].

Institute for Reliability and Microintegration (IZM) and Fraza company developed compact multi-gap foil winding inductors to realize a 8.2 kW/dm^3 (134 W/in^3) single-phase, full-bridge based PV inverter for the GOOGLE and IEEE Little Box Challenge (LBC) targeting the realization of the world smallest 2 kW inverter [7]. In order to achieve soft-switching throughout the mains period, Triangular Current Mode (TCM) modulation was employed resulting in a variable switching frequency in the range of 200 kHz −1 MHz for an inductance value of 10.5 µH. These system parameters were obtained from a Pareto optimization as described in detail in [6]. A picture of the realized inductor with dimension (14.5 × 14.5 × 22) mm^3 is shown in Fig. 1(c). The inner limb of the inductor is composed of 24 × 0.6 mm thick stacked ferrite plates with 80 µm partial air gaps between the plates, resulting in a total air gap length of 1.92 mm. The inner limb is surrounded by the foil winding with a total of 16 turns, where each turn is composed of four parallel 20 µm thin copper foils which are mutually isolated with a 7 µm thin layer of Kapton. Furthermore, a sophisticated winding arrangement is used as shown in Fig. 1(b), which forces the current to flow evenly distributed in all four parallel copper layer, thus counteracting the skin and proximity effect [4], [5], [8], [9]. Moreover, the arrangement features both connection terminals at the outside of the winding where the magnitude of the H-field in the winding window is small, reducing losses caused by the termination of the foil winding, where it is difficult to keep the copper foil aligned with the H-field, to a minimum. The used core material is DMR 51 from the manufacturer DMEGC, a MnZn ferrite optimized for the frequency range of 1 MHz − 2 MHz (similar in performance to 3F4 from Ferroxcube or PC200 from TDK).

TABLE I
TECHNICAL DATA OF THE MULTI-GAP FOIL WINDING INDUCTOR

Inductance	10.5 µH
Quality factor	≈ 600 between 200 kHz − 1000 kHz
R_{AC}	14 mΩ −120 mΩ between DC − 1 MHz
Dimension	(14.5 × 14.5 × 22) mm^3
Foil Winding	2 × 8 turns 4 parallel 20 µm copper foils 7 µm Kapton layer isolation
Core	MnZn Ferrite DMR 51 / DMEGC 24 × 80 µm air gaps 0.61 mm thick stacked plates (6.6 × 9.6 × 17.5) mm^3 center limb dimension

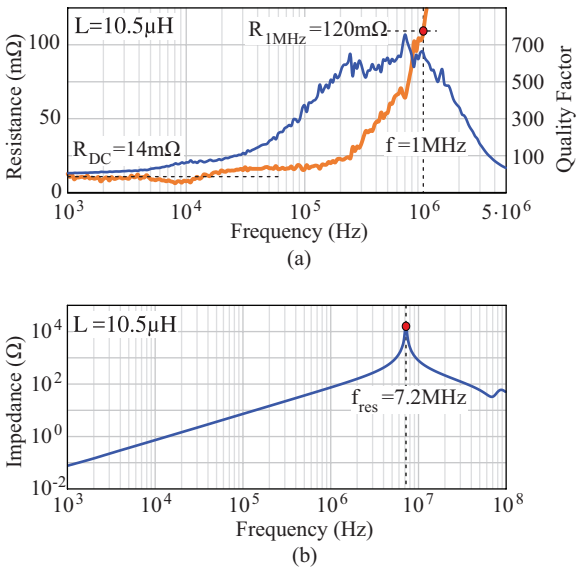

Fig. 2. Small-signal impedance analyzer measurements with Agilent 4294A of the multi-gap inductor depicted in Fig. 1(c). (a) Winding resistance and quality factor with respect to frequency. (b) Impedance with respect to frequency.

All technical specifications of the multi-gap inductor are summarized in Table I and impedance analyzer measurements are presented in Fig. 2. It can be seen that the implemented multi-gap foil winding inductor exhibits an excellent quality factor of 600 –700 between 200 kHz –1 MHz and a high resonance frequency of around 7.2 MHz.

Unfortunately, experimental measurements at an early stage of development revealed a substantially higher power loss than expected. By means of core loss measurements and thermographic inspection, the origin of additional losses could be attributed to the stacked ferrite plates constituting the center limb of the core. For this reason, the number of partial gaps was reduced from initially 50 to just 24 in the final inductor design (cf., Table I). Upon consultation of scientific literature and further experimental investigation, four main reasons for the increased core losses were identified:

- Formation of deteriorated ferrite layers at the plate surfaces due to mechanical stress introduced during machining.

- Flux crowding in the multi-gap core due to tolerances and imperfections in machining and assembly (Appendix A).
- Deterioration of ferrite properties due to pressure buildup in the stack of plates during the curing of the employed epoxy resin (Appendix B).
- Ohmic loss in the ferrite associated with the current flowing in the conduction path provided by the low impedance of the ferrite material at high frequencies and the parasitic capacitance between outer layer of the foil winding and the ferrite (Appendix C).

For the sake of brevity, only the surface loss related mechanism will be addressed in detail in this paper since it is by far the most significant contributor to the excess core loss. However, the interested reader is referred to the respective Appendix of this paper for a brief discussion of the other loss mechanism. The main scientific contribution of this work is an experimental method which allows to differentiate between core losses associated with the bulk and the surface of the ferrite plates required to implement the multi-gap inductor design and thus to pinpoint the measured excess core loss to shallow surface layers of ferrite with deteriorated magnetic performance as suggested in scientific literature dating back to the '70s. Moreover, the proposed technique allows to assess modern ferrite materials regarding their applicability in multi-gap inductor designs.

In Section II of this paper, the most important analyses and findings are shown in the literature regarding the impact of mechanical processing, such as cutting and grinding on the magnetic properties of ferrite are summarized and a microstructural analysis of the machined ferrite surface is presented. In Section III, mathematical expressions are derived to quantify core and surface loss densities from experimental temperature rise measurements using multi-gap core samples assembled from machined ferrite plates with distinct thicknesses. Moreover, the employed experimental setup based on Infrared (IR) thermometry is outlined. The proposed technique is then applied to characterize the MnZn ferrite material 3F4 at several peak flux densities and frequency values, that is to say at operating points $\{\hat{B}, f\}$ which resemble the Google Little Box Challenge application. The obtained experimental findings are presented in Section IV and subsequently discussed in Section V where the ratio between bulk and surface core loss is illustrated. Section VI concludes the paper and provides an outlook for future research.

II. Machining Induced Increase of Core Loss

The correct dimensions of ferrite plates or cuboidal pieces needed to implement a multi-gap core are typically not off-the-shelf available and must be machined from a larger ferrite piece. One option is to cut the plates from a long sintered ferrite bar using a precision saw as depicted in Fig. 3(a). Since ferrite is a very hard and brittle ceramic, the saw must be equipped with a diamond blade. As a consequence of the cutting process with the abrasive diamond particles, a mechanical stress is introduced into the ground surface of the plate. As will be summarized in the following, it is claimed in the scientific literature that the exerted

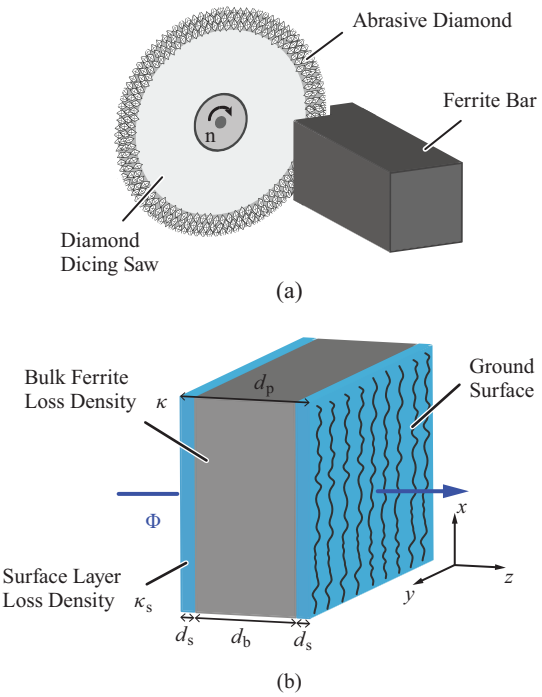

Fig. 3. (a) Cutting thin ferrite plates or cuboidal pieces from a long bar using a precision saw equipped with a diamond blade. (b) Abrasive machining causes residual mechanical stress in the ground surface; the magnetic properties of ferrite are degraded in these shallow layers and feature a much higher core loss density as opposed to the ferrite with intrinsic properties in the bulk of the plate.

mechanical stress is deteriorating the magnetic properties of the ferrite in a thin layer just underneath the surface resulting in an increase of overall core loss (cf., Fig. 3(b)).

The first investigations regarding the impact of mechanical stress on the properties of ferrite were conducted by E. Stern and D. Temme back in 1964 [10]. They observed that mechanical pressure applied to a toroidal core changes the remanent magnetization, coercive force and the shape of the BH-loop. They also claimed that compressive stress can result from abrasive machining and predominantly affects the ferrite close to the machined surface. Investigating several materials such as Garnet, NiZn and MgMn ferrite, Stern and Themme concluded that only magnetostrictive core materials are strongly affected by mechanical stress.

In 1970 John E. Knowles investigated how uniaxial stress affects the initial permeability — temperature curve, $\mu_i(T)$, of MnZn ferrite with different MnO/ZnO ratios [11]. Knowles compared the $\mu_i(T)$ curve of sintered and ground toroid core samples and learned that the permeability of the machined toroids (abrasion with a belt grinder or sandpaper) was lowered at high temperatures and raised at lower temperatures resulting in a sharp bend in the $\mu_i(T)$ curve and that the samples with higher MnO/ZnO-ratio were more sensitive. Knowles argued that the immense local pressure exerted during the grinding process caused a compressive stress in the surface layer and, consequently, a tensile stress in the interior of the ferrite. He further argued that it was hence possible for the compressed

surface to influence the magnetic properties of the bulk ferrite. However, how much the properties of the bulk are affected depends on the exerted stress in the interior of the ferrite which is a function of geometry and size. In a follow-up publication in 1974, Knowles found that the loss factor, $\frac{\tan\delta}{\mu}$, of a ferrite pot core at 100 kHz increased by up to 33% after machining the mating and air gap surfaces with a diamond-wheel precision grinding machine [12]. Knowles experimentally determined that the grinding process causes a very large residual compressive stress in the surface layer with magnitude of up to 700 MN/m^2 (almost the ultimate compressive stress of the material) reducing almost linearly towards the interior of the sample, becoming negligible at a depth of 5 μm below the surface. In another experiment, Knowles applied manually a pressure to both flat faces of a toroidal core in order to investigate the dependency of the loss factor, permeability and coercitive force on the compressive stress in the ferrite. Based on the results, Knowles estimated that the average loss factor of the ground surface is roughly 350 times larger than the intrinsic loss factor of the examined MnZn ferrite material. The magnetic properties of a ferrite rod subject to tensile and compressive stress were also studied by E. C. Snelling [13]. Snelling applied either a tensile or compressive stress and recorded the permeability, the residual and hysteresis loss factor and the coercitivity of the MnZn ferrite sample. In close agreement with Knowles, Snelling observed that above 30 °C tension reduces the permeability and compression increases it and below about −10 °C the opposite is true. Snelling could also show that for both compressive and tensile stress, the residual and hysteresis loss factors increase.

Kloholm *et al*. determined the magnetostrictive response of thin MnZn and NiZn ferrite plates (1 cm × 4.2 cm × 90 μm) as the applied magnetic field was decreased from saturation to magnetic remanence [14]. Additional abrasion of one side of the ferrite specimen with 180 grit SiC polishing paper caused a marked increase in magnetostrictive response of the sample, indicating that a deteriorated ferrite layer is formed underneath the machined surface. By knowing the magnetostriction constant of the investigated materials, Klokholm *et al*. estimated that the thickness of the deteriorated layer is about 40 μm − 50 μm in case of the MnZn ferrite and around 90 μm − 100 μm in the investigated NiZn ferrite.

The influence of machining on the properties of ferrite has also been studied extensively with respect to magnetic storage systems. NiZn and MnZn ferrite ceramics are widely used as recording head materials and are finished to a high degree of precision by diamond grinding and lapping. The finished ferrite surface is found to have a shallow magnetically inactive layer causing recording head performance to deteriorate [15]–[17].

For the sake of completeness it should furthermore be noted, that recently [18]–[20] reported that the cutting process has also a substantial influence on the ferromagnetic material properties of steel sheets used to manufacture laminated iron cores for electric machines.

A. Microanalysis of MnZn Ferrite Surface

From the review of the scientific literature it can be concluded that ferrite is extremely sensitive to mechanical stress and machining likely deteriorates the magnetic properties. In order to find structural evidence of a deteriorated layer close to the surface and assess the surface condition of the machined MnZn ferrite plates, a Scanning Electron Microscopy (SEM) analysis was performed and the results are depicted in Fig. 4. In Fig. 4(a) the surface with clearly visible individual grains of a sintered MnZn ferrite sample (3F4) is shown where no subsequent (i.e., after sintering) machining process was applied. In contrast, the ground surface as a result of cutting the plate from a long ferrite bar with a diamond saw is depicted in Fig. 4(b), showing deformed grains and grooves formed by the abrasive diamond particles. In order to assess the morphology of the ferrite underneath the surface, Focused Ion Beam (FIB) milling was performed as shown in Fig. 4(c) to expose the bulk ferrite material. The close-up view in Fig. 4(d) clearly indicates micro cavities and cracks roughly 5 μm − 10 μm below the surface. Fig. 4(e) depicts the plate surface after removing roughly 500 μm of material by means of abrasive polishing with SiC grinding paper and gradually decreasing the grain size from 22 μm down to 5 μm, using water as a lubricant. The last polishing step was performed with colloidal silica suspension with a grain size of 60 nm and a soft polishing cloth. Fig. 4(f) depicts the lateral view (i.e. orthogonal to the machined surface) of the ferrite sample embedded in a Bakelite support after removing roughly 1 mm of material to expose the bulk. From Figs. 4(e) and (f) it becomes clear that the cavities and cracks identified in Fig. 4(c) are not caused by mechanical stress exerted during cutting, but are the result of imperfections in the sintering of the MnZn ferrite. It should be noted that this is not vendor but rather process or technology specific, since the same cavities and cracks were also visible in ferrite samples from other vendors.

However, the presented SEM microanalyses did not reveal any structural abnormality which would allow to actually pinpoint the excess core loss to shallow layers of ferrite with deteriorated magnetic performance as suggested in the literature. Therefore, an experimental approach is derived in the following which allows to differentiate between core losses associated with the bulk and the surface of the examined ferrite plates.

III. Quantification of Surface Losses

The nonlinear characteristics of magnetic core materials require large-signal measurements to determine core losses accurately. It is a common technique to experimentally measure core losses for sinusoidal excitation of different amplitudes and frequencies and then obtain the parameters of the well known Steinmetz Equation (SE),

$$p = k f^{\alpha} \hat{B}^{\beta} \,(\mathrm{mW/cm^3}), \tag{1}$$

by means of least-mean-square regression. Using the SE with identified parameters k, α and β then allows to accurately predict core losses for a limited flux density and frequency range.

Considering again a ferrite plate with cross section A_p and thickness $d_p = 2d_s + d_b$ as shown in Fig. 3(b), where d_s and d_b are

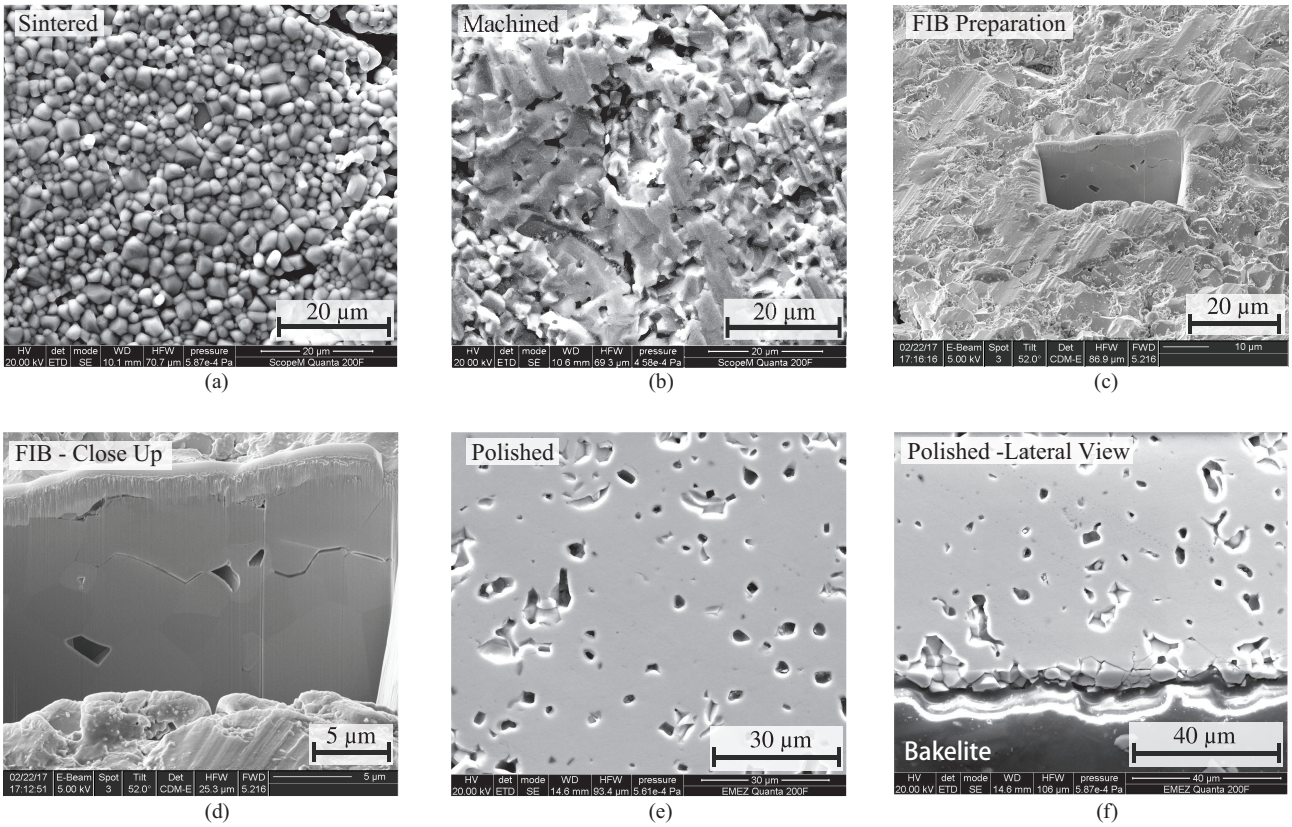

Fig. 4. Scanning Electron Microscopy (SEM) images of MnZn ferrite samples. (a) Surface of a ferrite plate after sintering (no machining). (b) Surface of a plate cut from a long ferrite bar with a diamond blade. (c) Focused Ion Beam (FIB) milling to expose bulk material underneath surface. (d) Close-up of the FIB prepared sample revealing cracks and cavities underneath surface. (e) Plate surface after removing roughly 500 µm of ferrite by means of polishing, gradually reducing grain size of SiC paper and surface finish with colloidal silica suspension and soft cloth. (f) Lateral view of plate embedded in Bakelite support after polishing.

the thicknesses of the deteriorated layers at the plate surfaces and the bulk ferrite with intrinsic properties, respectively. To keep the derivation simple, it is assumed that there is a strict separation of surface layer and intrinsic material and that these segments exhibit a strictly cuboidal shape as indicated in Fig. 3(b). It then follows that for homogenous flux density, ensured by the excitation circuit described in Section III-B, the total core losses in the ferrite plate are given by

$$\begin{aligned} P_\mathrm{l} &= \underbrace{k f^{\alpha} \hat{B}^{\beta}}_{\kappa} \underbrace{d_\mathrm{b} A_\mathrm{p}}_{\mathrm{Vol}_b} + \underbrace{k_\mathrm{s} f^{\alpha_\mathrm{s}} \hat{B}^{\beta_\mathrm{s}}}_{\kappa_\mathrm{s}} \underbrace{2 d_\mathrm{s} A_\mathrm{p}}_{\mathrm{Vol}_s} \\ &= (\kappa \cdot d_\mathrm{b} + \kappa_\mathrm{s} 2 d_\mathrm{s})\, A_\mathrm{p} = \left(\kappa + \kappa_\mathrm{s} \frac{2 d_\mathrm{s}}{d_\mathrm{b}} \right) d_\mathrm{b} A_\mathrm{p} \qquad (2) \\ &\approx \left(\kappa + \kappa_\mathrm{s} \frac{2 d_\mathrm{s}}{d_\mathrm{p}} \right) d_\mathrm{p} A_\mathrm{p}, \end{aligned}$$

wherein $d_\mathrm{p} = d_\mathrm{b} + 2d_\mathrm{s} \approx d_\mathrm{b}$ is the fair assumption that the thickness of the surface layer is negligible compared to the thickness of the bulk.

It is presented in the following, how a calorimetric measurement approach can be applied to experimentally determine both bulk and surface loss densities of a multi-gap core assembled from thin ferrite plates. The technique is based on determining core losses in ferrites by means of precise temperature rise monitoring as reported in [21]–[23].

A second experimental method based on electrical core loss measurements using ferrite samples with a distinct number of gaps is discussed in Appendix D. Since the calorimetric method fully excludes the loss of the test circuit required to adjust the magnetic excitation and therefore allows to capture the power loss in the sample directly, it features a significantly lower measurement error and is therefore the preferred choice in this study.

A. Linear Thermal Model

The power loss in the core given in (2) during continuous operation causes naturally a temperature rise of the ferrite plate over time which can be modeled by a lumped thermal network considering one-dimensional heat flow as shown in Fig. 5(a), wherein lumped parameters $C_{\mathrm{th,s}}$ and $C_{\mathrm{th,b}}$ capture the thermal capacitance of the surface layer and bulk material, respectively, and $R_{\mathrm{th,b\text{-}s}}$ models the virtual thermal resistance of the bulk-surface interface. Since the loss density in bulk and surface layer is homogeneous and a plate features a comparably low thermal conductivity towards ambient at its thin lateral faces in *x, y*-direction, i.e., $R_{\mathrm{th,b-a}} \to \infty$, it is sufficient to consider a strict one-dimensional heat flow in pos. and neg. *z*-direction (i.e., normal to the plate surface; cf. Fig. 3(b)). The power loss in bulk and surface region is captured with distinct current sources

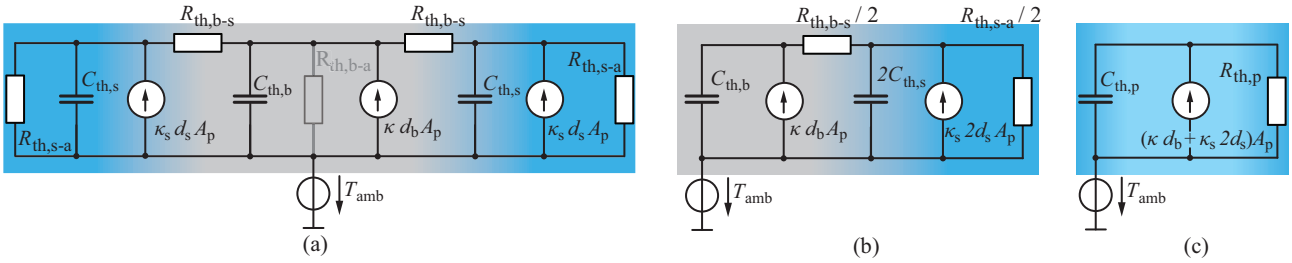

Fig. 5. (a) Thermal network of the ferrite plate considering one-dimensional heat flow in pos. and neg. z-direction (cf., Fig. 3(b)); lumped parameters $C_{th,s}$ and $C_{th,b}$ capture the thermal capacitance of the surface layer and bulk material, respectively, and $R_{th,b-s}$ models the thermal resistance of the bulk-surface interface. The power loss in bulk and surface region is captured with distinct current sources $\kappa d_p A_p$ and $\kappa_s d_s A_p$, and the transfer of heat to ambient is taken into consideration with $R_{th,s-a}$ and $R_{th,b-a}$. (b) Simplification of the circuit due to symmetry and neglecting heat transfer from bulk to ambient ($R_{th,b-a} \to \infty$). (c) The thermal conductivity of ferrite is high enough to support a homogenous temperature distribution within the plate, further simplifying the thermal network.

TABLE II
TECHNICAL DETAILS AND MATERIAL PARAMETER

Param.	Value	Unit	Description
A_p	7 × 6.4	mm^2	Cross section area of plate / sample
λ_m	0.154	W/(m K)	Thermal conductivity of Mylar
λ_{fe}	3.5−5	W/(m K)	Thermal conductivity of MnZn ferrite
$R_{th,b}$	13−20	K/W	Thermal resistance of a 3 mm MnZn ferrite plate
$R_{th,m}$	14.9	K/W	Thermal resistance of a 100 µm Mylar foil
$C_{th,p}$	0.51	J/K	Thermal capacitance of a 3 mm MnZn ferrite plate calculated with specific heat capacity
$C_{th,m}$	7.3	mJ/K	Thermal capacitance of 100 µm Mylar foil
c_m	1172	J/(kg K)	Specific heat capacity of Mylar
c_{fe}	800	J/(kg K)	Specific heat capacity of MnZn ferrite
ρ_{fe}	4800	kg/m^3	Density of MnZn ferrite (3F45)
ρ_m	1390	kg/m^3	Density of Mylar
$R_{th,a}$	117.8	K/W	Thermal resistance of 3 mm poly carbonate (PC) air-gap lattice
R_{th}	37.8	K/W	Equivalent thermal resistance from calibration (cf., Fig. 11(b))
C_{th}	3.83	J/K	Equivalent thermal capacitance from calibration (cf., Fig. 11(b))

(cf., $\kappa d_b A_p$ and $\kappa_s d_s A_p$) and a heat transfer to ambient in z-direction is taken into consideration with $R_{th,s-a}$. Due to symmetry, the network can be simplified as shown in Fig. 5(b). As will become evident from the thermography images provided in Section III-B, the thermal conductivity of the MnZn-ferrite (cf., Table II) is large enough to support a homogenous temperature distribution within the plate, i.e., $R_{th,b-s} \to 0$.

Accordingly, it is sufficient to consider the simplified first order thermal network with lumped parameters $R_{th,p}$ and $C_{th,p}$ as shown in Fig. 5(c), where the total dissipated power is combined in a single current source. It follows from (2) that the average loss density in a plate of thickness d_p is given by

$$\bar{\kappa} = P_l / d_p A_p = \kappa + \kappa_s 2d_s / d_p . \tag{3}$$

Thus, based on the hypothesis that the loss density is larger in the surface layer than in the bulk, the average loss density increases inverse proportional with the thickness of the plate. As illustrated in Fig. 6(a), a thin plate (d_1) is more governed by the characteristics of the surface layer and features a higher avg. loss density as opposed to a fairly thick plate (d_3) which approaches the loss density of the bulk ferrite.

If the heat transfer to ambient is negligible by means of sufficient thermal insulation (i.e., $R_{th,p} \to \infty$ in Fig. 6(a)),the temperature of the plate increases linearly over time,

$$T(t) = \frac{P_l}{C_{th,p}} \cdot t + T_{amb}, \tag{4}$$

where it is assumed that the initial temperature of the ferrite plate at $t = 0$ equals the ambient temperature, T_{amb}. Inserting expression (2) in (4) yields

$$T(t) = (\kappa + \kappa_s \frac{2d_s}{d_p}) \frac{d_p A_p}{C_{th,p}} t + T_{amb}. \tag{5}$$

The equivalent thermal capacitance of the plate, $C_{th,p}$, can be determined from a calibration measurement as described later in Section III-E or calculated according to

$$\begin{aligned} C_{th,p} &= (c_{f,s} \rho_{f,s} 2d_s + c_f \rho_f d_b) A_p \\ &\approx c_f \rho_f d_p A_p = \tilde{c}_f d_p A_p, \end{aligned} \tag{6}$$

where c_f and ρ_f is the specific heat capacity and density of MnZn ferrite as listed in Table II, respectively. Note that it is assumed that the thermal capacitance of the plate is predominantly governed by the bulk properties. Substituting (6) in (5) leads to

$$T(t) = \left(\frac{\kappa}{\tilde{c}_f} + \frac{\kappa_s}{\tilde{c}_f} \frac{2d_s}{d_p} \right) t + T_{amb}. \tag{7}$$

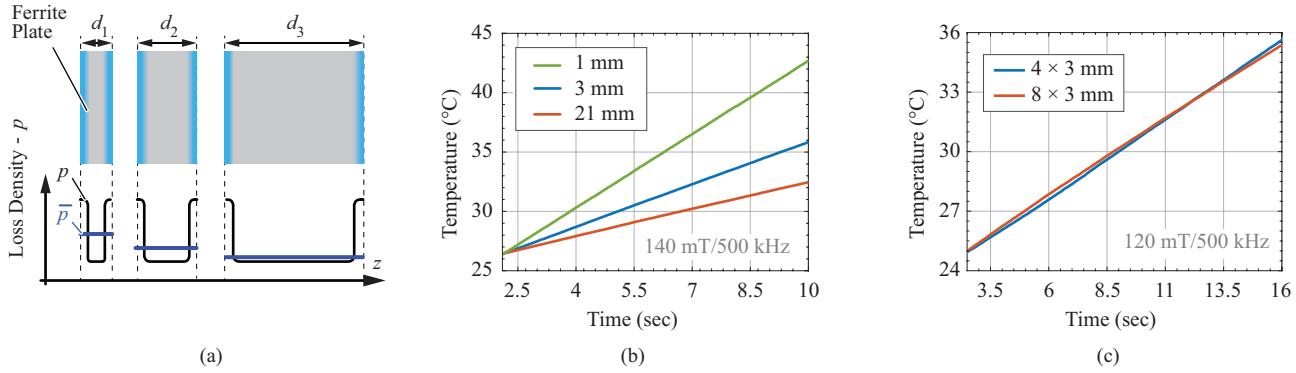

Fig. 6. (a) A thin plate (d_1) is more governed by the characteristics of the surface layer and features a higher avg. loss density, $\bar{p}$, as opposed to a fairly thick plate (d_3) which approaches the loss density of the bulk ferrite. (b) Experimental temperature rise measurement showing that a sample assembled from 1 mm plates results in a much steeper slope compared to 3 mm plates or the single-piece (21 mm) reference sample. (c) Experimental measurement showing that the slope of the temperature rise is not affected by the actual height of the stack (i.e., number of plates in the stack).

It can be seen that the temperature rise is governed by a constant contribution of the bulk material and a contribution of the power dissipation in the surface layer which depends on the actual ratio of surface to plate thickness. This trend is strongly supported by the experimental results depicted in Fig. 6(b), where it can be seen that a multi-gap sample assembled from thin 1 mm plates features a much steeper slope in contrast to thicker 3 mm plates and the (very thick) solid reference sample. Interestingly, since both total power loss and total thermal capacitance increases proportional to the number of stacked plates, the slope of the temperature rise is not affected by the actual height of the stack (i.e., number of plates in the stack) as confirmed by the measurement results depicted Fig. 6(c). This in turn allows to measure a stack rather than a single plate which is advantageous in accommodating the required flux sense winding and improves mechanical handling of the sample for a precise placement in the test circuit (cf., Section III-B).

Since the properties of ferrite are strongly depending on temperature, the duration t_x to reach a specified temperature difference, $\Delta T = T_{\text{end}} - T_{\text{amb}}$, is measured rather than a final temperature after a fixed time span Δt. Rearranging (7) leads to

$$t_\chi = \frac{\Delta T}{\frac{\kappa}{\tilde{c}_\text{f}} + \frac{\kappa_\text{s}}{\tilde{c}_\text{f}} \frac{2d_\text{s}}{d_{\text{p}\chi}}} \tag{8}$$

for a plate with thickness $d_{\text{p}\chi}$. Now, performing two consecutive measurements with identical operating point but using ferrite plates with different thicknesses, d_{p1} and d_{p2}, allows to solve (8) to obtain the loss density of the bulk ferrite,

$$\kappa = \frac{(d_{\text{p1}} t_2 - d_{\text{p2}} t_1)}{(d_{\text{p1}} - d_{\text{p2}}) t_1 t_2} \tilde{c}_\text{f} \Delta T, \tag{9}$$

and the loss per surface area,

$$\tilde{\kappa}_\text{s} = \kappa_\text{s} d_\text{s} = \frac{1}{2} \frac{d_{\text{p1}} d_{\text{p2}} (t_1 - t_2)}{(d_{\text{p1}} - d_{\text{p2}}) t_1 t_2} \tilde{c}_\text{f} \Delta T. \tag{10}$$

Note that since the actual thickness of the surface layer d_s is unknown, it is more suitable to define power loss per surface area, $[\tilde{\kappa}_\text{s}] = \text{mW/cm}^2$.

B. Experimental Setup

An excitation circuit is needed which ensures a homogeneous flux density distribution in the sample, allows to characterize the core loss for different flux density amplitudes and frequencies, and facilitates an easy installation of different samples. A magnetic circuit resembling an E-type core with the multi-gap sample located in the center limb as depicted in Fig. 7(a) is chosen in this study, since it only requires a single sample as opposed to a U-type setup and can be assembled by individual off-the-shelf available ferrite cuboids minimizing custom machining effort. The multi-gap sample in the center as well as the individual ferrite cuboids are fixated by means of a 3D printed mounting fixture and fastening screws. Consistent pressure applied to the ferrite regardless of the inserted sample is guaranteed by means of a torque wrench adjusted to 0.02 Nm. In Fig. 7(c), two multi-gap samples assembled with 1 mm and 3 mm thick plates, respectively, and a solid, single piece ferrite sample are shown. The equivalent circuit of the test setup is shown in Fig. 8, where the transformer equivalent circuit with open secondary winding represents the magnetic excitation circuit with flux sense winding. The reactive power of the magnetic circuit is compensated by means of a series connected capacitor in order to reduce the burden on the HF voltage source (Iwatsu IE-1125B) and attain all operating points $\{\hat{B}, f\}$ of interest given the output voltage limitation of the amplifier.

Since the outer magnetic circuit contributes to the total core losses (troublesome in the case of the electrical loss measurement, cf., Appendix D) and heat generation in the test circuit can affect sample temperature, the dimensions of the outer magnetic circuit are chosen such that its losses are minimized while keeping the flux density in the sample homogeneous. This can be achieved by increasing the cross section of the magnetic path while minimizing its avg. magnetic length, since the sample-to-core loss ratio considering homogenous flux density in the setup is given by

$$\frac{P_\text{sample}}{P_\text{test}} \propto \left(\frac{A_\text{test}}{A_\text{p}}\right)^{\beta-1} \frac{l_{\text{m, sample}}}{l_{\text{m, test}}}, \tag{11}$$

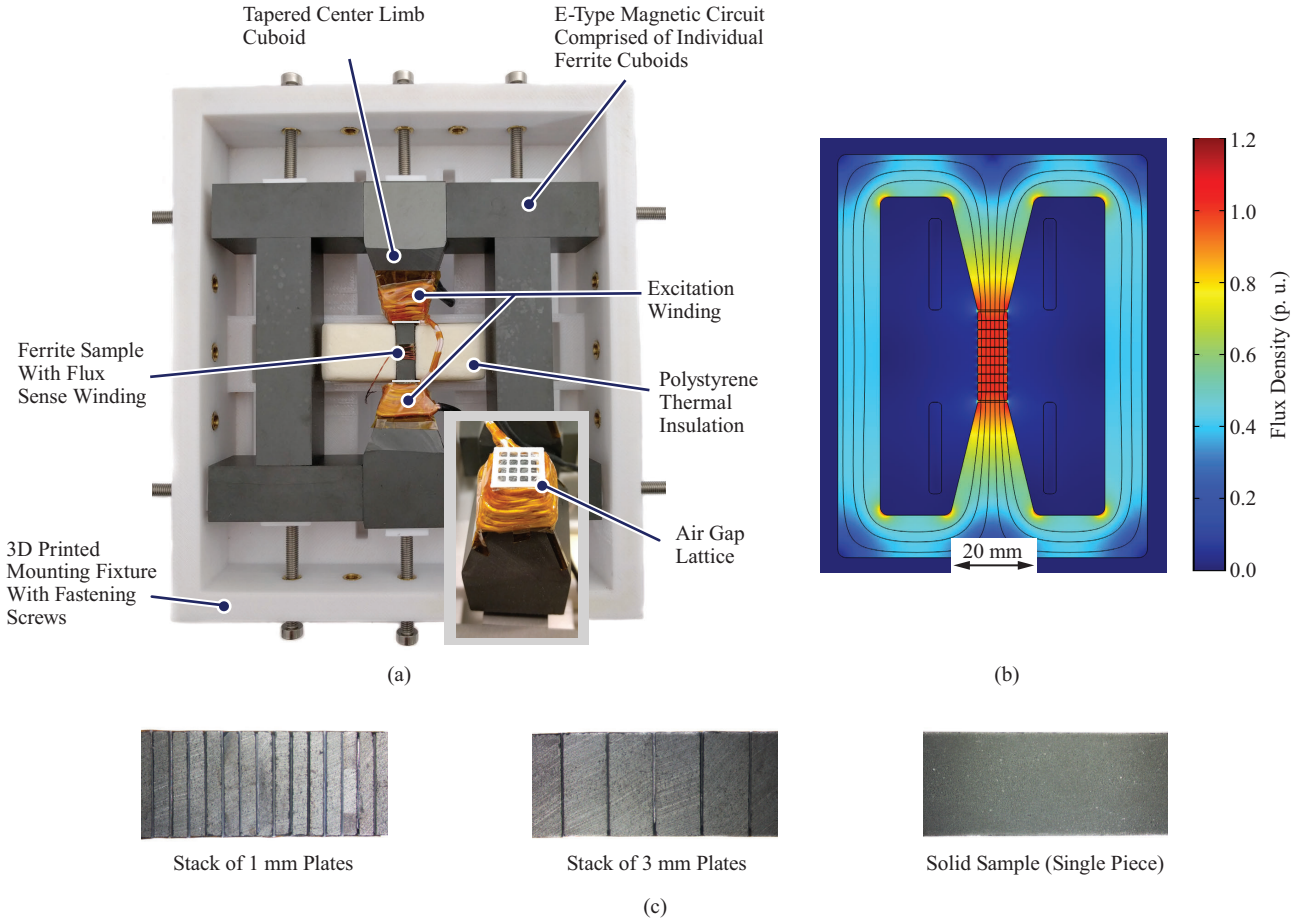

Fig. 7. (a) Test circuit resembling an E-type core with a multi-gap core sample located in the middle of the center limb; fastening screws and a 3D printed mounting fixture keeping the individual ferrite cuboids of the outer magnetic circuit and the sample in position; splitting the turns of the excitation winding in two sections above and below the sample and employing tapered center limbs to accommodate the cross section difference between outer magnetic circuit and sample facilitates a homogenous flux density distribution in the sample; a dedicated tightly wound sense winding is placed around the center of the sample to correctly adjust the peak flux density; measures to increase the thermal resistance to ambient are the polystyrene casing and the air gap lattice inserted between sample and test circuit. (b) FEM simulation result showing the homogenous flux density distribution in the sample. (c) Picture of multi-gap samples composed of 1 mm and 3 mm plates, respectively, and the single piece solid reference sample. To adjust the partial gap length, 100 µm thick Mylar foil is inserted between the plates.

where A_{test}, A_{p} and $l_{\text{m,test}}$, $l_{\text{m,sample}}$ denote the cross section area and avg. magnetic path length of the test circuit and sample, respectively. However, due to the distributed gap, the comparably large magnetic reluctance of the installed multi-gap sample in the center limb results in a significant leakage flux which potentially causes an inhomogeneous flux density distribution in the sample or bypasses it completely and only contributes to undesired loss in the test circuit. With the aid of magnetostatic field simulations (cf., Fig. 7(b)), optimal dimensions based on readily available core shapes were obtained which maximize the sample-to-core loss ratio of the setup while keeping the flux density distribution in the sample homogenous. As shown in Fig. 7(a), two measures were employed which greatly contribute to a homogenous flux density distribution in the sample: (i) the turns of the excitation winding are split in two sections directly above and below the sample and (ii) tapered center limbs are employed to accommodate the cross section difference between test circuit and sample. In order to correctly adjust the desired flux density amplitude in the multi-gap sample despite different cross section areas and leakage flux, a dedicated tightly wound sense winding is placed around the center of the sample as indicated in Fig. 7(a).

As mentioned previously in Section III-A, due to the constant loss density and the low thermal conductivity towards ambient in lateral direction, a uniform temperature distribution in (x, y)-direction (cf., Fig. 3) is present throughout the sample which allows to infer the correct temperature from a measurement at one of the lateral surfaces. In this paper, infrared thermography is the preferred temperature instrumentation since (i) it allows to compute the average temperature over the entire multi-gap sample as opposed to a single spot measurement provided by fiber optical temperature probes, thermistors (NTC, PTC) or thermocouples and (ii) is contactless, i.e., does not require to physically attach a probe to the delicate sample. Moreover, infrared thermography reveals non-uniform temperature distributions and the formation of hot spots and thus allows to detect inhomogeneous flux density distribution in the sample (f.i. flux crowding) caused by a potential sample misalignment and/or an excessive gap between sample and center limb pole pieces

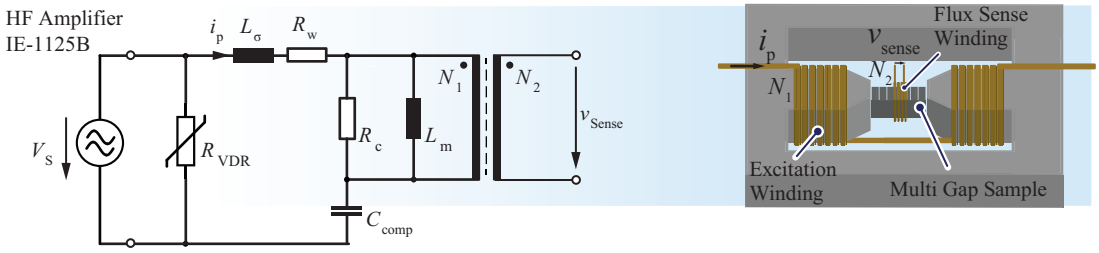

Fig. 8. Schematic of the employed excitation circuit; the dedicated sense winding with N_2 turns allows to precisely determine the flux density. The reactive power of the magnetic circuit is compensated by means of a capacitor bank to reduce the burden on the HF voltage source and attain all operating points $\{\hat{B}, f\}$ of interest despite the limited HF amplifier voltage range.

of the test circuit. Using thermography to determine core loss distribution in magnetic components has been reported in [24], [25] and to detect defects in ferromagnetic laminated sheets and soft mangetic composites in [26]. The authors in [27], applied infrared thermography to visualize the iron loss distribution in a permanent magnet motor. A picture of the experimental measurement setup is depicted in Fig. 9(a), showing the implemented test setup according to Fig. 8 with the magnetic circuit and capacitor bank and a FLIR A655sc high definition infrared camera pointed towards the multi-gap sample. The camera is equipped with additional close-up lens to allow a working distance of around 6 cm − 7 cm between sample and camera lens and provides 50 µm spatial resolution. The lower ±2 °C absolute measurement accuracy of a microbolometer [28] is not relevant here, since according to (9) and (10) only a temperature difference must be determined and the standard deviation per detector pixel of a high end infrared camera is typical around 0.1 °C − 0.2 °C [29]. Compensating the reactance of the magnetic test circuit is necessary to attain all $\{\hat{B}, f\}$ operating points of interest given the limited voltage range of the employed IWATSU IE-1125B HF power amplifier. For a good agreement with the linear model derived in Section III-A, the heat transfer from sample to ambient in the experimental setup must be reduced as much as possible. To prevent convective heat transfer from the lateral surfaces of each individual plate in the stack to ambient, the sample is encased in polystyrene except for the surface pointing towards the infrared camera as it can be seen from Fig. 7(a) and Fig. 9(a). Furthermore, to minimize conductive heat transfer from the multi-gap sample to the two center limb core pieces of the E-type test circuit, an additional gap between sample and adjacent pole pieces is inserted. A gap length of around 0.5 mm is a still acceptable trade-off between minimizing conductive heat transfer and establishing a homogenous flux density in the sample close to the interfaces. In order to achieve the lowest possible thermal conductivity, the gap is realized by means of a 3D printed lattice made out of polycarbonate as it is depicted in the detail view of Fig. 7(a).

The experimental results presented in Section IV of this paper were obtained by relating the slope of the temperature rise of a multi-gap sample with 7 stacked 3 mm ferrite plates (d_{p1} = 3 mm) to a solid, single-piece reference sample of 21 mm length (d_{p2} = 21 mm). Mylar foil is inserted between adjacent plates to establish a gap length of 100 µm, which,

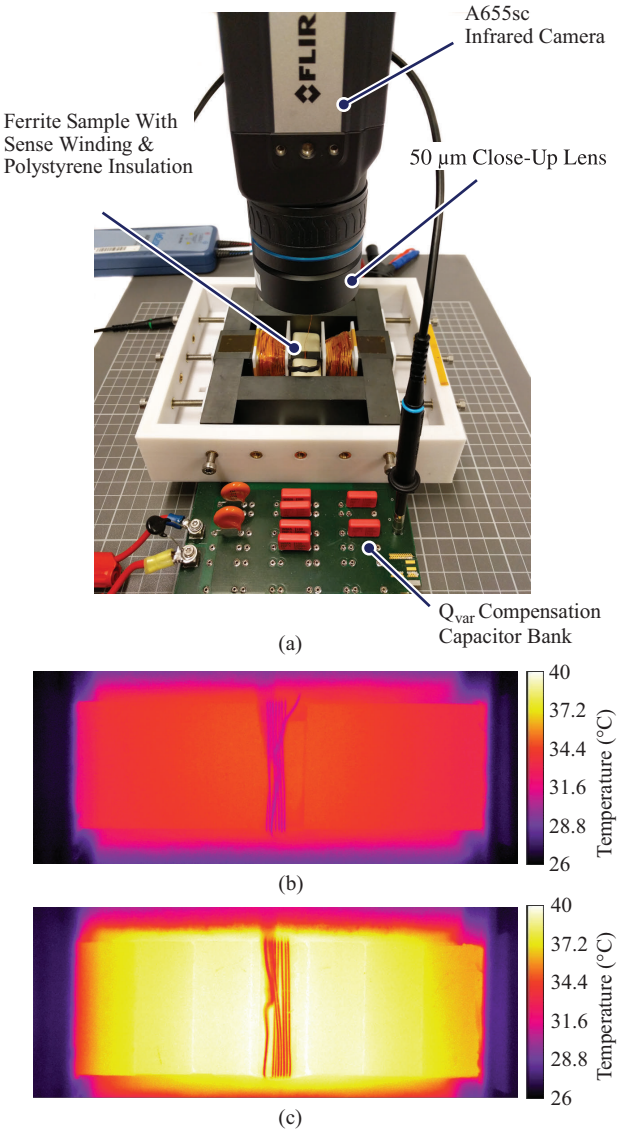

Fig. 9. (a) Picture of the experimental setup showing the magnetic test circuit with capacitor bank for reactive power compensation and the employed FLIR A655sc high definition infrared camera pointed towards the sample. Thermography image of the temperature rise of the solid (b) and multi-gap sample (c) subject to an excitation with 125 mT at 400 kHz exactly after 30 s of total elapsed measurement time. It is clearly visible that the multi-gap sample composed of 7 × 3 mm plates is heating up much quicker.

in combination with 3 mm plates, completely alleviates loss

contribution arising from flux crowding in the sample caused by assembly and mechanical tolerances as described in Appendix A.

At each operating point of interest, $\{\hat{B}, f\}$, the temperature rise after abruptly enabling the correctly adjusted power amplifier is recorded for both samples and the core and surface loss density are then computed according to (9) and (10). The elapsed time to reach a specific temperature difference ΔT starting from ambient temperature is extracted from the captured temperature rise in a subsequent post-processing step. Since the core loss and many other properties of ferrite depend strongly on operating temperature, a large temperature deflection would certainly have an impact on the results. However, the high frame rate of the infrared camera (up to 50 Hz with full resolution of 640 × 480) allows to determine the elapsed time even for a very small temperature difference of just a few °C. The experimental results presented in this paper were obtained for $\Delta T = 2.5$ °C.

A snapshot of the temperature rise of the solid and multi-gap sample subjected to an excitation with 125 mT at 400 kHz exactly after 30 s of total elapsed measurement time is shown in Fig. 9(b) and (c), respectively. Since both measurements were started from ambient temperature, $T_{amb} = 26.4$ °C, it can be clearly seen that the multi-gap sample heats up much faster showing a final temperature reading of around 38 °C in contrast to roughly 32 °C of the solid sample. Note that the interruption of the uniform temperature distribution by the sense winding is in the center of each sample.

C. Longitudinal Temperature Gradient

Referring to Fig. 9(b) and (c), it is noticeable that both samples exhibit a temperature gradient in longitudinal direction with slightly lower temperatures at both ends where the sample connects to the outer magnetic circuit. Fig. 10 depicts the computed temperature profile of both infrared images in longitudinal direction, whereby the temperature reading at every camera pixel in the plot represents the mean temperature of all sensor pixels encompassing the sample in transversal direction (i.e., orthogonal to the direction of the flux). It becomes evident that the temperature gradient in the multi-gap sample is more pronounced (≈ 3.75 °C) compared to the solid reference sample (≈ 1.25 °C). Moreover, the temperature profile of the multi-gap sample exhibits a clear local maximum whenever two surfaces of adjacent ferrite plates meet, i.e., at the surfaces of the plates. Now, a representative thermal network of stacked plates is shown in Fig. 11(a) which is helpful to explain the more pronounced temperature gradient in the case of the multi-gap sample. Note that the simplified thermal model of a single plate according to Fig. 5(c) is considered. Since the thermal capacitance of a piece of Mylar foil is negligible compared to the ferrite plate (cf., Table II) only the thermal resistance introduced by the gap material, $R_{th,m}$, is included in the model. Although the thermal conductivity of Mylar is at least a factor 10 lower compared to MnZn ferrite, the resulting thermal resistance of foil and ferrite plate is in the same order of magnitude (≈ 15 K/W as listed in Table II). However, since the length of both samples examined in this study is equal per design and the Mylar foil has virtually no contribution,

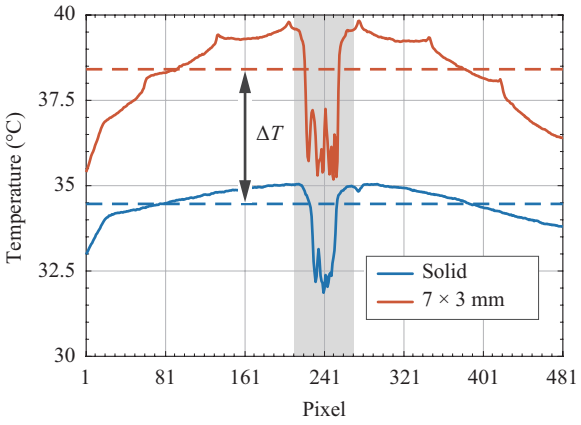

Fig. 10. Temperature profile in longitudinal direction of the IR images of solid and multi-gap sample shown in Fig. 9 (b) and (c); the dashed line represents the average value of the IR sensor and is used to compute ΔT.

the effective thermal capacitance of both solid and multi-gap sample is identical. Ideally, if $R_{th,a} \to \infty$ then each plate will exhibit exactly the same temperature rise irrespective of the actual position in the stack as confirmed by a circuit simulation. However, the thermal resistance achieved with the air gap lattice is estimated to be around $R_{th,a} = 117.8$ K/W considering the thermal conductivity of polycarbonate (PC) and air (air gap lattice, cf., Fig. 7(a)), and evidently not large enough to support uniform heating in longitudinal direction. It follows that the temperature gradient is more pronounced in the case of the stacked plate assembly since heat close to the center of the sample encounters an effectively larger thermal resistance in longitudinal direction towards both ends of the sample in comparison to the solid, single-piece sample. Now, in order to determine the elapsed time to reach a specific temperature difference, ΔT, the pragmatic way of averaging the IR sensor reading also in the longitudinal direction is followed as indicated with dashed lines in Fig. 10, naturally excluding the distortion in the center of the sample caused by the flux sense winding. The corresponding first order thermal model is shown in Fig. 11(b) and the expression for the core and surface loss densities based on the linear model are refined in the following. Note that in the following, R_{th} and C_{th} denote the equivalent thermal parameters of a stack of plates (cf., $R_{th,p}$ and $C_{th,p}$ of a single plate, Fig. 5(c)).

D. Exponential Thermal Model for Multi-Gap Assembly

Based on the equivalent circuit shown in Fig. 11(b), the temperature rise of an assembly with m plates of thickness d_p starting from T_{amb} at $t = 0$ is given by

$$\begin{aligned} T(t) &= P_{l\Sigma} R_{th}\left(1 - e^{-\frac{t}{\tau}}\right) + T_{amb} \\ &= \left(\kappa + \kappa_s \, {}^{2d_s}/_{d_p}\right) m V_p R_{th}\left(1 - e^{-\frac{t}{\tau}}\right) + T_{amb}, \end{aligned} \tag{12}$$

with the time constant $\tau = R_{th} C_{th}$ and the core volume of a plate $V_p = d_p A_p$. It should be emphasized, that the total core volume $V_{p\Sigma} = m V_p$ is kept constant by adopting the plate thickness in accordance to the number of gaps such that the examined

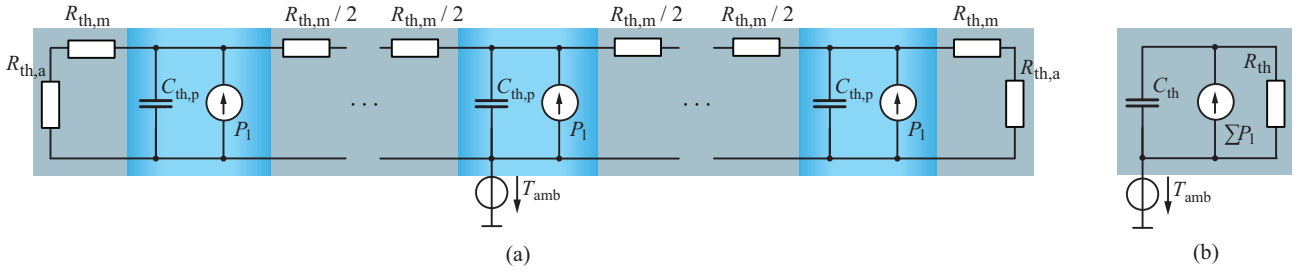

Fig. 11. (a) Representative thermal network of stacked plates using the simplified thermal model of a single plate according to Fig. 5(c) and considering the thermal resistance $R_{th,m}$ introduced by the gap material. (b) First order thermal model of a sample corresponding to averaged IR temperature reading in longitudinal direction.

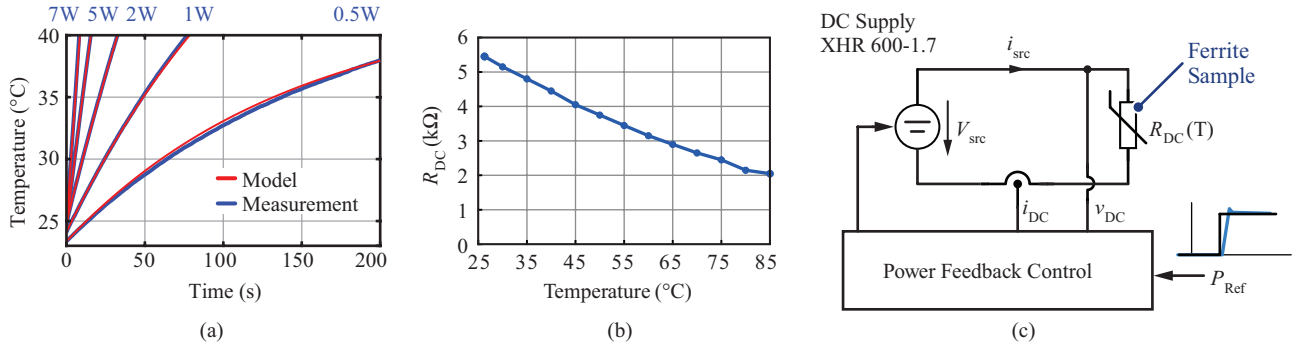

Fig. 12. (a) Measured temperature response obtained for the solid sample (blue) and the simulated response of the mathematical model with identified parameters (red) for several impressed power levels ranging from 0.5 W to 7 W. (b) Measured DC resistance of MnZn ferrite as a function of temperature. (c) Schematic of implemented power feedback control to impress constant power during calibration despite temperature dependent change of the ferrite DC resistance.

multi-gap samples feature equal thermal parameters R_{th}, C_{th}. Analogously to the derivation described in Section III-A, measuring the elapsed time t_1 and t_2 of two samples with distinct plate thickness d_{p1} and d_{p2} to reach a specific ΔT allows to calculate the core loss density

$$\kappa = \frac{d_{p1}\left(1-e^{-\frac{t2}{\tau}}\right)-d_{p2}\left(1-e^{-\frac{t1}{\tau}}\right)}{\left(d_{p1}-d_{p2}\right)\left(1-e^{-\frac{t1}{\tau}}\right)\left(1-e^{-\frac{t2}{\tau}}\right)}\frac{\Delta T}{R_{th}V_{p\Sigma}}, \tag{13}$$

and the surface loss density

$$\tilde{\kappa}_s = \frac{1}{2}\frac{d_{p1}d_{p2}\left(e^{-\frac{t2}{\tau}}-e^{-\frac{t1}{\tau}}\right)}{\left(d_{p1}-d_{p2}\right)\left(1-e^{-\frac{t1}{\tau}}\right)\left(1-e^{-\frac{t2}{\tau}}\right)}\frac{\Delta T}{R_{th}V_{p\Sigma}}, \tag{14}$$

given that thermal parameters R_{th} and C_{th} are known from a preceding DC calibration measurement as described in the next subsection.

E. DC Calibration

By means of capturing the temperature response of the sample subject to a stepwise impressed power loss of pre-determined value, the parameters of the model (12) can be identified by means of a least mean square regression. For good predictions of the model, it is crucial that the power range covered in the calibration actually resembles the core loss occurring in the respective operating point of interest, $\{\hat{B}, f\}$. Fig. 12(a) shows the excellent agreement between the measured temperature response obtained for the solid sample (blue) and the simulated response of the mathematical model with identified parameters (red) for several impressed power levels ranging from 0.5 W to 7 W. Treating the solid ferrite sample as an electric conductor with a DC resistance, R_{DC}, the power loss required for the calibration measurements can be impressed by means of Joule heating, $P_{DC} = R_{DC}I_{DC}^2$. The measured DC resistance of the solid sample amounts to 5.5 kΩ at room temperature and varies strongly with temperature as shown in Fig. 12(b). Since the temperature of the sample rises during the measurement but the impressed power must be kept constant (step response), feedback control is employed to tightly track P_{DC} reference by means of adjusting the applied DC voltage as schematically depicted in Fig. 12(c). Since DC quantities are involved, the power instrumentation is trivial. Terminals to connect the leads of the DC supply are formed with narrow stripes of 50 µm thick copper foil glued to both ends of the sample using conductive silver epoxy. Using thin copper foil for the contacts allows the sample to be properly installed in the magnetic test circuit during the calibration which is crucial to correctly identify the thermal resistance to ambient. The identified parameters, $C_{th} = 3.83$ J/K and $R_{th} = 37.8$ K/W are in reasonable agreement with estimates based on material constants as listed in Table II ($7 \cdot C_{th,p} \approx 3.6$ J/K, $1/2 \cdot R_{th,a} = 58.9$ K/W).

F. Measurement Error

Consolidating (13) and (14), two main sources of error can be identified: (i) The IR camera's standard deviation of the

temperature difference measurement ΔT denoted with $\sigma_{\Delta T}$ and (ii) uncertainty in the parameters R_{th}, C_{th} of the underlying model represented with standard deviations σ_R and σ_C. Potential uncertainty in the measured time intervals due to sampling delay and/or jitter of the IR camera is neglected because of the high sampling frame rate relative to the measurement time. In order to calculate the error propagation, the non-linear equations of κ and κ_S are linearized around $\chi = (t_{1\chi}, t_{2\chi}, \kappa_\chi, \tilde{\kappa}_{s\chi})$ resulting from a specific excitation $\{\hat{B}_\chi, f_\chi\}$. In the following the equations are only explicitly presented for κ for the sake of brevity. The standard deviation of κ around χ is then given by [30]

$$\sigma_\kappa(\chi) = \sqrt{J_\kappa(\chi) \Sigma J_\kappa(\chi)^T}, \tag{15}$$

where $\sum$ denotes the covariance matrix and $J_\kappa(\chi)$ is the Jacobi-matrix of κ at χ,

$$J_\kappa(\chi) = \left[\left.\frac{\partial \kappa}{\partial \Delta T}\right|_\chi, \left.\frac{\partial \kappa}{\partial R_{th}}\right|_\chi, \left.\frac{\partial \kappa}{\partial C_{th}}\right|_\chi \right]. \tag{16}$$

The covariance matrix is given by

$$\Sigma = \begin{pmatrix} \sigma^2_{\Delta T} & r^2_{\Delta T,R}\sigma_{\Delta T}\sigma_R & r^2_{\Delta T,C}\sigma_{\Delta T}\sigma_C \\ r^2_{\Delta T,R}\sigma_{\Delta T}\sigma_R & \sigma^2_R & r^2_{R,C}\sigma_R\sigma_C \\ r^2_{\Delta T,C}\sigma_{\Delta T}\sigma_C & r^2_{R,C}\sigma_R\sigma_C & \sigma^2_C \end{pmatrix}, \tag{17}$$

where $r_{x,y}$ represents the correlation coefficient between stochastic variables x and y. From a physical standpoint, there is only a weak correlation between variations in R_{th} and C_{th} and also between variations in ΔT and R_{th}. However, there is a more pronounced negative correlation between variance in ΔT and C_{th}, since a larger ΔT during calibration with a specific impressed power and measurement time interval leads to smaller C_{th}. Instead of presenting exhaustive analytical equations, some general facts should be highlighted. Naturally, a distinct difference in plate thickness between the examined multi-gap samples results in a significant difference in elapsed time to reach ΔT and thus supports a small measurement error.

Since the measurement time $t_{1\chi}$ and $t_{2\chi}$ for a specific ΔT increases inversely proportional to the dissipated power in the ferrite plate, a small (large) absolute error must be expected at a low (high) loss operating point, respectively. In principle, allowing a larger temperature difference ΔT increases the measurement time and leads to a reduction in error. However, ΔT cannot be increased too much (here ΔT = 2.5 °C cf., Section III-B) since the ferrite properties are a strong function of temperature. In order to calculate a worst case bound on the measurement error a deviation of $\sigma_{\Delta T}$ = 0.3 °C and a 15% deviation of the thermal parameters from their expected values as listed in Table II is assumed. Moreover, since in (17) the exact correlation between the variables is unknown, a worst case error of κ and $\tilde{\kappa}_s$ is determined by varying the coefficient $r_{x,y}$ in a numerical study. It then follows from (15) that for the operating points of interest, the worst case rel. measurement error is estimated to be

$$\frac{\sigma_\kappa}{\kappa}(\chi) \leqslant 20.3\% \quad \text{and} \quad \frac{\sigma_{\tilde{\kappa}s}}{\tilde{\kappa}_s}(\chi) \leqslant 19.9\%. \tag{18}$$

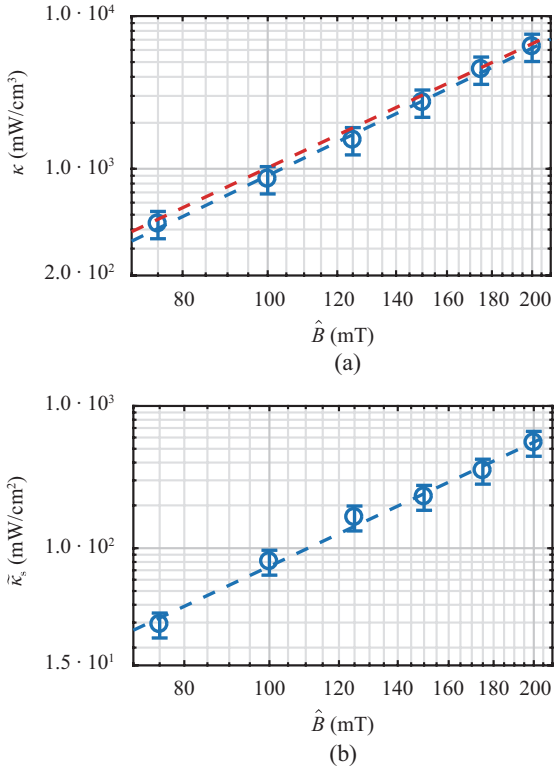

Fig. 13. Experimentally determined (a) bulk and (b) surface core loss density of MnZn ferrite material 3F4 at a fixed frequency of 400 kHz and varying flux density amplitude. The prediction obtained from the Steinmetz model fitted to the experimental data is indicated by the dashed blue line. In addition the prediction with Steinmetz parameters provided by the vendor (cf., Table III, [31]) is indicated by the dashed red line in (a).

IV. Experimental Results

In this section the bulk and surface core loss density of MnZn ferrite material 3F4 of Ferroxcube are presented. The experimental results were obtained by means of the thermometric measurement setup with IR camera as described in detail in Section III-B and expression (13) and (14) based on the exponential thermal model. The measurements were carried out for a sinusoidal flux density with amplitudes varying from 75 mT up to 200 mT and excitation frequencies ranging from 200 kHz up to 1 MHz. For this range of operating points $\{\hat{B}, f\}$, the worst case relative measurement error of both bulk and surface core loss density is limited to 20% as discussed in the previous section.

The bulk and surface core loss density at a fixed frequency of 400 kHz and varying flux density amplitudes is depicted in Fig. 13(a) and (b). The predictions obtained from the Steinmetz model (1) fitted to the experimental data and from parameters provided by the vendor are represented by the dashed blue and red line, respectively. The experimental and vendor parameter

TABLE III
STEINMETZ PARAMETERS FOR
MNZN FERRITE MATERIAL 3F4 FROM FERROXCUBE
$[\kappa] = \mathrm{mW/cm^3}$ AND $[\kappa_s] = \mathrm{mW/cm^2}$

	k	α	β
κ	1.32×10^{-2}	1.36	2.77
κ^{a}	35×10^{-2}	1.1	2.7
κ^{b}	1.2×10^{-4}	1.7	2.7
κ_s	2.72×10^{-2}	1.13	2.9

[a] [31], 100 kHz – 600 kHz and 30 °C
[b] [31], 600 kHz – 1000 kHz and 30 °C

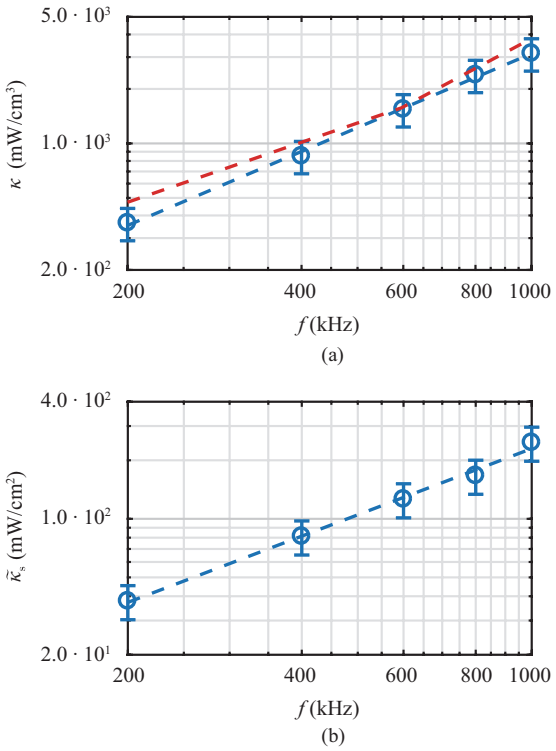

Fig. 14. Experimentally determined (a) bulk and (b) surface core loss density of MnZn ferrite material 3F4 at a fixed peak flux density of 100 mT and varying frequency. The prediction obtained from the Steinmetz model fitted to the experimental data is indicated by the dashed blue line. In addition the prediction with Steinmetz parameters provided by the vendor (cf., Table III, [31]) is indicated by the dashed red line in (a).

of the Steinmetz model are summarized in Table III. In a similar manner, the bulk and surface core loss density at a fixed flux density amplitude of 100 mT and varying excitation frequency is depicted in Fig. 14(a) and (b). Note that depending on the frequency range a different set of vendor Steinmetz parameter is employed which explains the slight kink in the dashed red line at 600 kHz as indicated in Fig. 14(a). However, the Steinmetz fit to the experimental data was performed over the entire frequency range which explains the discrepancy, especially in the frequency exponent α, between experimental and vendor parameters (cf., Table III). It can be seen from Fig. 13(b) and Fig. 14(b) that the measured surface loss density varies from 30 $\mathrm{mW/cm^2}$ to 600 $\mathrm{mW/cm^2}$ for the considered operating points.

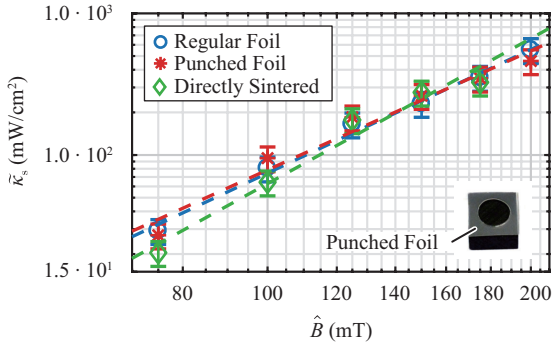

Fig. 15. Comparison of the surface loss density of different multi-gap samples at a fixed frequency of 400 kHz and varying flux density amplitude. The regular sample is composed of 7 × 3 mm plates with 100 µm Mylar foil in between. Roughly half of the Mylar foil area was removed in the case of the punched foil sample. The green grinded sample was constructed from ferrite plates which were pressed and then sintered to the desired dimensions without machining.

In order to assess whether the Mylar foil inserted between the plates has any contribution to the measured surface loss (e.g., by magnetostriction introduced friction), a multi-gap sample was prepared using Mylar foil with a punched round hole of approx. 5 mm diameter in the center of each foil as illustrated in the bottom right of Fig. 15. Punching a hole in the center ensures the desired gap distance and therefore still ensures equal flux distribution and/or prevents partial saturation while removing roughly 50% of the gap material. The measured surface loss density of a multi-gap sample with punched Mylar foil is compared to the regular multi-gap sample in Fig. 15, showing no difference between the results. To understand whether or not machining is actually the main cause of the increased core loss, ferrite plates directly sintered to the final dimension were provided by Ferroxcube in this study. These plates were manufactured by pressing and then machining ferrite powder into the appropriate dimensions before the actual sintering was performed (green grinding). Taking the size shrinkage caused by the sinter process into account, the correct final dimension of the plates has been immediately achieved eliminating the need of an additional machining step. The experimental measured surface loss density is also included in Fig. 15. It can be seen that $\tilde{\kappa}_s$ has slightly reduced at low flux density amplitudes in comparison to the regular sample composed of machined ferrite plates and exhibits a steeper slope corresponding to a Steinmetz parameter of $\beta_s = 3.4$.

V. DISCUSSION

The measured core loss densities shown in Fig. 13(a) and Fig. 14(a) show good agreement with the Steinmetz model provided by the manufacturer validating the proposed calorimetric core loss measurement technique. With regard to the surface loss densities (cf., Fig. 13(b) and Fig. 14(b)), the experimental data can be also well predicted with the Steinmetz model. Interestingly and as to be expected, the Steinmetz parameters of the surface layer are slightly different from the bulk material as listed in Table III. Compared to the bulk ferrite, the frequency exponent α in the surface is smaller (1.36 → 1.13)

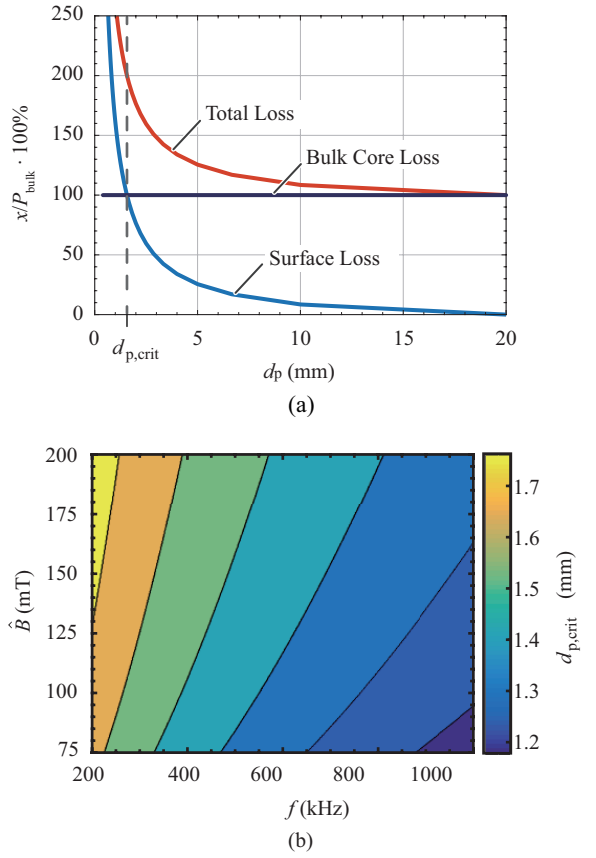

Fig. 16. (a) Surface and total core loss of a composite core assembled with individual d_p thick plates relative to the bulk core loss of a solid ferrite piece with d_{bulk} = 20 mm total length based on the experimental results obtained for 3F4 at 125 mT and 400 kHz. The critical plate thickness $d_{p,crit}$ is defined to be reached when the surface loss is equal to the bulk core loss. (b) Critical thickness of the examined 3F4 material depending on the actual operating point $\{\hat{B}, f\}$.

and the flux density exponent β is larger (2.77 → 2.9). Since the loss in the deteriorated surface layer is more sensitive to variation in flux density than it is to variation in frequency (almost linear relationship with frequency), it can be argued that hysteresis losses are more pronounced in the surface layer.

In order to illustrate the impact of $\tilde{\kappa}_s$ in more practical terms, the total power loss of a composite core assembled from individual d_p thick plates relative to the bulk core loss of a solid ferrite piece with d_{bulk} total length is computed,

$$\frac{P_{tot}}{P_{bulk}} \approx \frac{\left(\kappa d_{bulk} A_p + \kappa_s 2 d_s \frac{d_{bulk}}{d_p} A_p\right)}{\kappa d_{bulk} A_p} = 1 + \frac{\kappa_s}{\kappa}\frac{2d_s}{d_p} = 1 + \frac{\tilde{\kappa}_s}{\kappa}\frac{2}{d_p}, \tag{19}$$

and depicted in Fig. 16(a) based on the experimental results obtained for 3F4 at 125 mT and 400 kHz. The reference sample is constructed from a single piece of ferrite with a total length of 20 mm exhibiting only bulk core loss. With decreasing height of the ferrite plate, more and more plates must be stacked to reach the same length as the solid reference sample. Consequently, the total losses increase since more and more deteriorated surface layers are introduced in the sample. Note that the ratio between total and bulk core loss given by (19) is a function of only the plate thickness, d_p, since both bulk and surface core losses increase proportional with the core cross section, A_p, and the total sample length, d_{bulk}, assuming that d_{bulk} is varied in multiples of d_p. To further clarify, two composite core samples with different cross section area and/or different total sample length will exhibit the same total to bulk loss ratio (19) if the samples are constructed of plates with identical thickness. The critical plate thickness $d_{p,crit}$ is defined to be reached when the surface loss is equal to the bulk core loss, that is to say when the total power loss has doubled compared to the solid (single-piece) sample. In the case at hand, a composite core with 13 stacked 1.5 mm plates will exhibit roughly twice the core loss compared to the single-piece reference sample. Since κ and $\tilde{\kappa}_s$ exhibit a different dependency on flux density amplitude and frequency (cf., Table III), the critical plate thickness varies depending on the actual operating point $\{\hat{B}, f\}$ as depicted in Fig. 16(b). It should be noted that, the actual critical thickness depends not only on the properties of the ferrite but also on the exerted mech. stress during the machining of the plates. In an open discussion of the findings with the scientific community prior to this publication, it was argued that the measured excess core loss in the multi-gap core is actually the result of micro-vibrations causing friction between plate surface and gap material and that these micro-vibrations are excited by means of magnetostriction as discussed in detail in [32]–[34]. In this respect, if friction between plate surfaces and Mylar would indeed be the reason for the measured surplus core losses, then in case of the sample using punched Mylar foil, where roughly half of the interaction area was removed, a significant reduction in $\tilde{\kappa}_s$ should be observable. However, as depicted in Fig. 15, the measured surface loss density of the multi-gap sample with punched and regular Mylar foil is essentially identical, which strongly contradicts the notion that micro-vibration are the origin of the excess core losses. Furthermore, an experimental assessment with a laser vibrometer (Polytec CLV-2534) confirmed that within the considered excitation frequency range no micro-vibrations are excited.

Moreover, the idea was put forward that the measured excess core loss might be associated with machining and assembly tolerances. For instance, a pronounced tilt between the plates of the multi-gap assembly causes a non-uniform gap length which has a strong impact on the core loss due to flux crowding, especially if the assembly is composed of very thin plates and/or features small gap lengths. However, as analyzed in Appendix A, for a worst case machining and assembly tolerance, the plate thickness and gap length can be chosen such to minimize the resulting impact of flux crowding. The combination of using 3 mm plates and 100 µm gap length to implement the multi-gap sample examined in this study, results in a negligible contribution of flux crowding to the measured excess core loss in the multi-gap sample.

Very intriguing is also the fact that directly sintered plates still exhibit excess core loss in the same order of magnitude as the

machined plates which contradicts the hypothesis that mech. stress during machining is introducing the excess loss. However, it can be argued that the directly sintered plates also feature a layer of deteriorated ferrite performance close to the surfaces. These deteriorated layers are not caused by mech. stress introduced during machining but from an altered Fe^{2+} / Fe^{3+} ion concentration in the iron oxide close to the surface. Among other factors, the oxygen concentration in the atmosphere during sintering strongly affects the balance between Fe^{2+} and Fe^{3+} ions. Since the plate surfaces are directly exposed to the atmosphere inside the controlled temperature ferrite processing chamber in contrast to the bulk, and a deviation from the ideal, temperature dependent O_2 concentration is inevitable in a practical setting. Thus, a shallow ferrite layer close to the surface is likely to exhibit adverse magnetic properties which is an explanation why there is also excess core loss present in the case of the directly sintered plates.

VI. Conclusion

A multi-gap inductor design can potentially reduce winding losses due to a reduction in the magnetic air gap leakage field. Unfortunately, the manufacturing of a multi-gap core — composed of multiple stacked MnZn ferrite plates — can lead to an increase of core loss which potentially outweighs the saving in winding conduction loss. Based on the literature, the dominating cause of the excess core loss is shallow layers of deteriorated magnetic performance just underneath the plate surfaces. A sophisticated calorimetric measurement approach based on temperature rise monitoring was developed, allowing to differentiate between and quantify bulk and surface core loss densities. Experimental results were presented for the MnZn ferrite material 3F4 from Ferroxcube. Reasons for the deteriorated surface are mechanical stress exerted during machining of the plates as suggested by the literature and non-ideal conditions during sintering as suggested by the vendor. Several post machining treatments proposed in the literature — annealing, etching and stress-free polishing with colloidal silica — have been applied to the machined plates in order to restore the original ferrite properties and reduce core loss, unfortunately without significant success so far. Accordingly, more work needs to be done, especially considering an annealing treatment with defined atmosphere and temperature profile recommended by the vendor. Moreover, NiZn ferrite should be examined in future work since it is known from the literature that low-μ materials are less sensitive to mechanical stress. Thus, a multi-gap design using NiZn ferrite might not suffer from increased core losses as also the recent work in [35] seems to indicate.

Appendix A

Influence of Assembly and Machining Tolerances

In the multi-gap inductor design described in the introduction of this paper, the center limb of the E-type core is composed of thin ferrite plates stacked on top of each other. These plates are either cut from a long ferrite bar by means of a diamond saw or are manufactured by pressing ferrite powder into the desired shape prior to sintering. Due to mechanical tolerance in the manufacturing processes, it is possible that the plate surfaces exhibit a convex or concave curvature or are not ideally coplanar. In order to establish the correct gap length, a non-magnetic spacer material is inserted between the plates. The spacer, also intended to glue adjacent plates together, can be realized by means of a plastic film (e.g., Kapton or Mylar) with double sided adhesive or by a mix of epoxy resin with spherical silica powder as outlined in Appendix B, where the latter allows gap lengths below 30 µm. Due to mechanical tolerances, it is possible that the plates in the stack are not ideally coplanar but slightly tilted. In order to estimate how much these machining and assembly tolerances affect the core losses, a 2D FEM study was conducted. The static flux density distribution within the stacked plates considering a linear core material ($\sigma = 0$, $\epsilon_r = 1$, $\mu_r = 3000$) is computed based on Ampères's Law. In Fig. 17(a), the impact of several machining/assembly tolerances on the flux density distribution is shown. The ideal multi-gap core, composed of 15 × 1 mm thick plates with a 30 µm gap, is depicted at the very left indicating a homogeneous flux density distribution. The flux density component normal to the plate surface (y-direction) averaged with respect to the plate width (x-direction) in the very center of the stack (cf., red line in the image on the very left of Fig. 17(a)) for one ampere-turn of excitation is chosen as benchmark for an insightful comparison in per unit values. Since the effective permeability of the composite core changes depending on the magnitude of the simulated non-ideality, the excitation current is adopted accordingly such that the avg. flux density in y-direction in the center of the stack is identical under all considered scenarios. Introducing variable d_Δ to model tilt, curvature and non-coplanarity arising from mech. tolerances, leads to a pronounced flux crowding as it can be seen from the FEM simulation results in Fig. 17(a). The impact of flux crowding on the actual core loss is estimated considering $p \propto B_{\mathrm{pu}}^{\beta}$ according to (1), where $\beta = 2.4$ in this study. The avg. loss density of the multi-gap core is then given by,

$$\overline{p} = \frac{1}{A} \cdot \oiint_A p \mathrm{d}A = \frac{1}{A} \cdot \oiint_A B^{\beta} \mathrm{d}A, \tag{20}$$

where A denotes the total core area of the stack. Fig. 17(b) shows the avg. loss density for a fixed plate thickness and gap length ($d_p = 1$ mm, $d_{gap} = 30$ µm) but for a varying deviation. A tilt between plates has the most significant impact and results in an increase of the avg. loss density up to a factor of 2.3 for the worst considered error of $d_\Delta = 50$ µm. Note that the effective difference in gap length measured at both ends of the plate is actually twice d_Δ as indicated in Fig. 17(a). Fig. 17(c) depicts the avg. core loss density as a function of the gap length d_{gap} for a fixed plate thickness and the worst case error. It becomes evident that increasing the individual gap length allows to mitigate the impact of the error on the loss density. Likewise, Fig. 17(d) depicts how the loss density reduces when the stack is composed of thicker plates. It can be concluded from this study that even if all plates feature undisturbed ferrite properties, an excess of core loss can still be observed in a multi-gap inductor due to machining and assembly tolerances. A deviation of $d_\Delta = 50$ µm might reflect a worst case scenario, but it is reasonable to expect a deviation

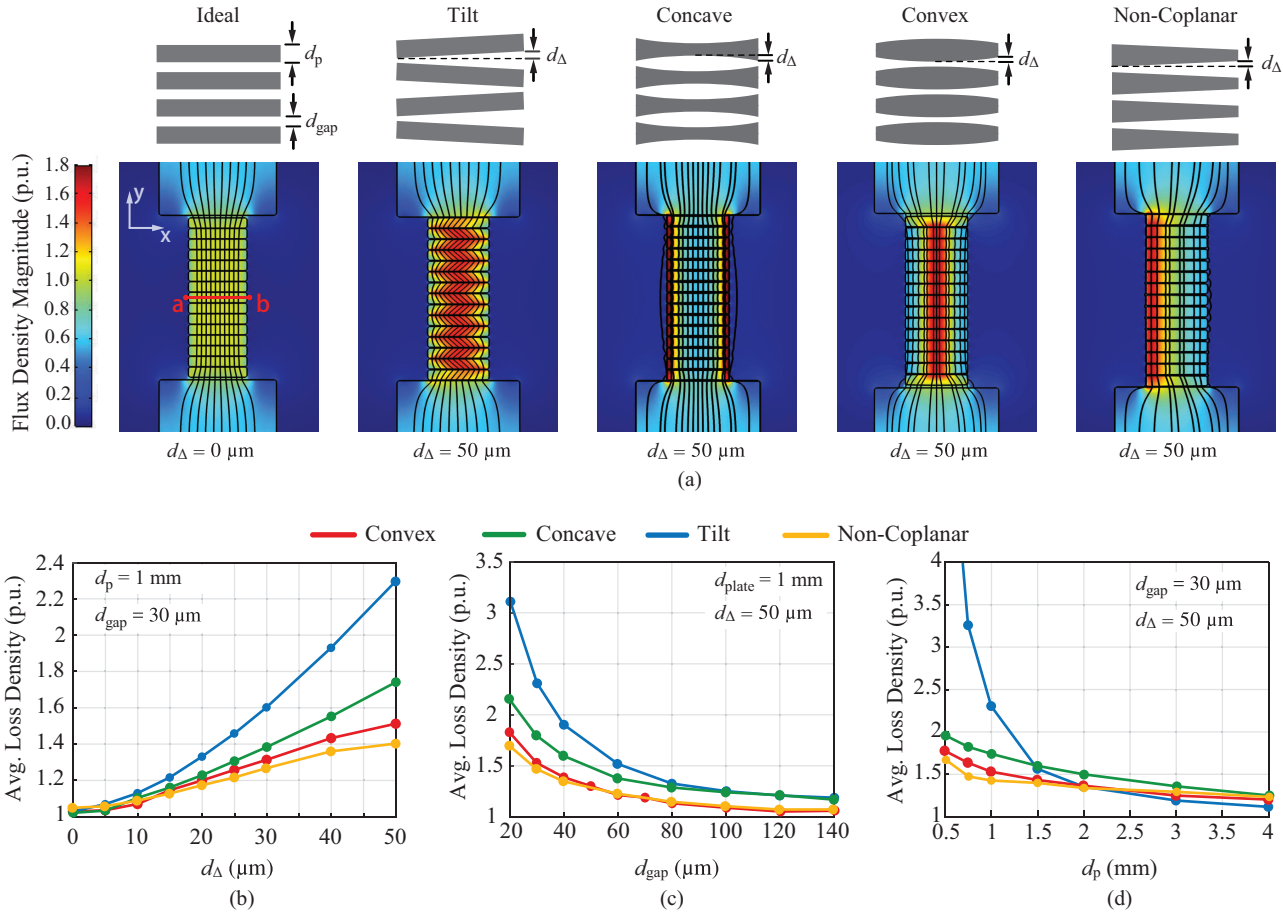

Fig. 17. (a) 2D FEM field simulation results indicating the impact of several machining / assembly tolerances on the flux density distribution in the sample. The ideal multi-gap core shown on the left side is composed of 15 × 1 mm thick plates with a 30 µm gap and serves as reference for the p.u. calculation. (b) Avg. core loss density in the sample for a fixed plate thickness and gap length (d_p = 1 mm, d_{gap} = 30 µm) but for a varying deviation d_Δ. (c) Avg. core loss density in the sample as a function of the gap length d_{gap} for a fixed plate thickness d_p and the worst case error (d_Δ = 50 µm). (d) Avg. core loss density in the sample as a function of the plate thickness d_p for a fixed gap length d_{gap} and the worst case error (d_Δ = 50 µm).

of d_Δ = 10 µm – 20 µm in practice. For instance the standard deviation in plate thickness measured with a precision caliper at all four lateral faces amounts to 5 µm in the case of the machined plates and to 23.7 µm in the case of the direct sintered plates (cf., Section IV and Section V) provided by Ferroxcube for this study. In order to isolate and correctly quantify surface related core loss, the multi-gap samples employed to obtain the experimental data presented in Section IV of this paper are constructed with 3 mm thick plates and 100 µm Mylar foil which limits the impact of mech. tolerances on the measured core loss to less than 5% for the (unlikely) worst case error.

Appendix B
Core Loss Increase Caused by Pressure Buildup

To ensure mechanical stability of the multi-gap inductor, the ferrite plates constituting the center limb have to be adhered to each other. The two-component adhesive Duralco 4460, which is based on epoxy resin was chosen for this task. Before application, the adhesive was mixed with spherical silica powder to provide a defined gap length [3]. Although the volume shrinkage of the glue is only 0.5% [36], the ferrite material is exposed to mechanical stress after this manufacturing process. Furthermore, since the cured glue shows a very low viscosity, the difference in thermal expansion coefficients of the glue (CTE of 64 ppm/K [36]) and the ferrite (CTE is approximately 12 ppm/K) can cause additional mechanical stress on the ferrite material. The impact of mechanical compression on the permeability and the saturation flux density was investigated in several publications, e.g., [37]–[39]. However, these property changes are not critical in the case of the designed multi-gap inductor (cf., Table I), since the effective permeability of the magnetic circuit is mainly determined by the length of the gap. Here, the most important observed parameter shift due to exerted mechanical stress on the ferrite is the increase in hysteresis losses. In [40] this effect was investigated on molded ferrites. E cores were glued on a PCB substrate and encapsulated using a transfer mold process at a temperature of 175 °C and a process pressure of approximately 10 MPa. The core losses before and after this technological process were determined electrically by applying the measurement principle described in [41] and reviewed in Appendix D of this paper. It was observed that the core losses of the investigated ferrite materials are increased after the molding process. Fig. 18(a)

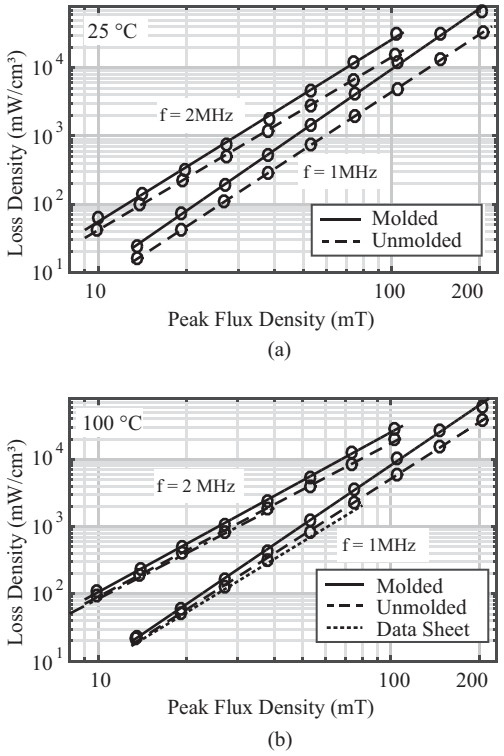

Fig. 18. Impact of molding on the core loss density of MnZn ferrite material 3F4 at (a) 25 °C and (b) at 100 °C.

and (b) depict the measured results for 3F4 at 25 °C and 100 °C, respectively (in [40] material G was examined). The results show a more distinctive increase of core loss at higher flux densities, e.g., increase of core loss after molding at 1 MHz, 100 °C and 20 mT by a factor of 1.2 and at 1 MHz, 100 °C and 150 mT by a factor of 1.7. Due to the larger share of eddy current losses at higher frequencies, the dependency of the core loss increase due to mechanical compression on the frequency is lower, e.g., an increase of core loss after molding at 100 mT, 100 °C and 1 MHz by a factor of 1.74 and at 100 mT, 100 °C and 2 MHz by a factor of only 1.45 occurs. It is concluded in [40] that only the hysteresis losses are increased by mechanical stress on the material. Furthermore, it is worth noting that the increase of the core losses is lower at a temperature of 100 °C compared to 25 °C. How much the additional hysteresis losses in the stack of ferrite plates can be reduced by using a more elastic adhesive, for instance Duralco 4538 with a shore hardness of only D70 [36], is the subject of ongoing research.

Appendix C
Ohmic Conduction Loss in Ferrite

Another origin of core loss in the multi-gap inductor design discussed in Section I is related to the finite conductivity of the MnZn ferrite and the high parasitic capacitance between the winding packages (cf., Fig. 1(a) and (b)) and the outer magnetic core. The effect can be explained by means of Fig. 19(a).

Between both outer turns of the top and bottom winding package and the ferrite of the magnetic return path (outer limb) a high parasitic capacitance is formed due to the comparably

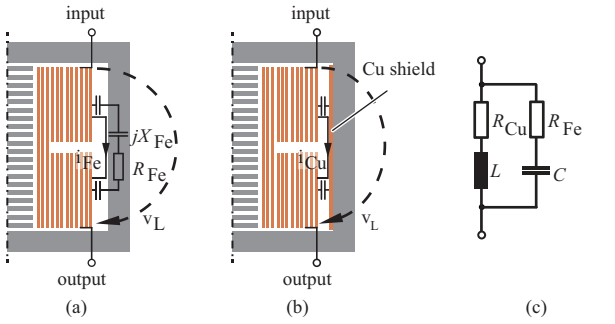

Fig. 19. (a) Explanation of the conduction loss effect in the ferrite material and (b) measure to minimize these additional losses by employing a low impedance copper shield. (c) Equivalent circuit of the inductor with winding resistance (R_{Cu} and L) and parasitic conduction path connected in parallel (R_{Fe} and C).

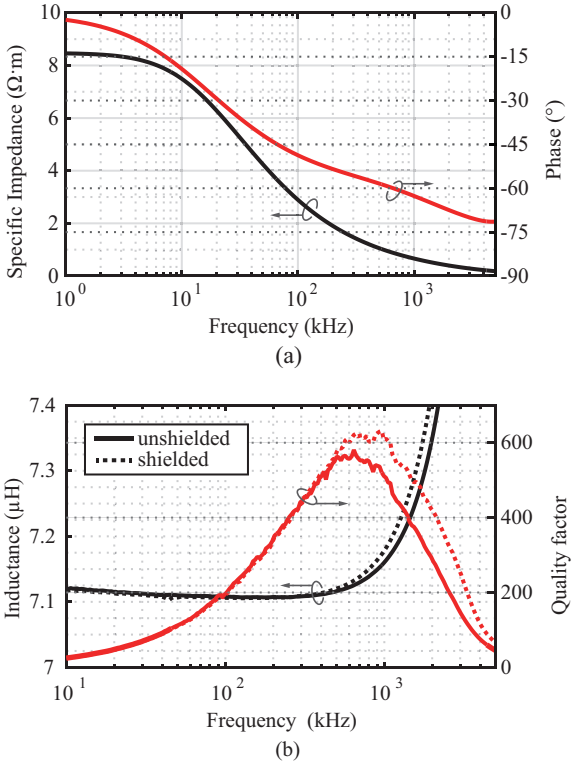

Fig. 20. (a) Measured specific impedance of the MnZn ferrite material DMR51 and (b) measured inductance and quality factor of the unshielded and shielded inductor.

large surface of the foil winding. By means of a simple plate capacitor model, the capacitance per winding package is estimated to be approximately 120 pF (relative permittivity of the insulation foil: 3.5, the foil thickness: 60 μm, surface of one winding package that is covered by ferrite: 240 mm^2). The voltage occurring between both turns is the total inductor voltage, because the outer turn of the top winding package is the first and the outer turn of the bottom winding package is the last turn of the inductor winding. Therefore, a high parasitic current through the ferrite material occurs at high frequencies and causes additional losses in the ferrite material due to the finite ohmic resistance of the ferrite. Fig. 20(a) shows the measured specific impedance of the MnZn ferrite DMR51. The measurement was performed on a ferrite cuboid (length:

8.2 mm, cross section: (2.6 × 3.0) mm^2) using the impedance analyzer Agilent 4294A. The MnZn ferrite material is comprised of grains with a relatively low specific ohmic resistance and layers of high resistivity between these ferrite grains. At frequencies up to 4 kHz the specific impedance is almost exclusively determined by the specific ohmic resistance of the grain boundaries and is approximately 8.3 Ωm. At higher frequencies an additional capacitive current flows across the isolating layers (grain boundaries), thus the impedance features a capacitive imaginary part and the magnitude reduces. The specific impedance of the DMR51 material at a frequency of 1 MHz is only (0.3 − 0.58i) Ωm.

Considering the geometry of the inductor, the resulting impedance of the average conduction path through the ferrite at a frequency of 1 MHz caused by the described parasitic capacitance is $Z_{Fe} = R_{Fe} + jX_{Fe} = (47 - 91i)\ \Omega$ (length of the conduction path: 9 mm, cross section: (1.9 × 30) mm^2). It follows then that the impedance of the equivalent circuit (cf., Fig. 19(c)) is given by

$$\begin{aligned} Z_{eq} &= (R_{Cu} + j\omega L) \,||\, \left(R_{Fe} + \frac{1}{j\omega C}\right) \\ &\approx (j\omega L) \,||\, \left(R_{Fe} + \frac{1}{j\omega C}\right), \end{aligned} \tag{21}$$

wherein the approximation holds since $\omega L >> R_{Cu}$ and parameter C represents the series connection of both parasitic capacitances between the outermost turns of the respective winding package and the outside magnetic core as well as the capacitive part of Z_{Fe} (120 pF || 120 pF || 1.7 nF in total C = 58 pF). Computing the real part of (21) allows to estimate the impact on the measured ohmic resistance ΔR of the inductor at a frequency of 1 MHz given by

$$\Delta R = \Re(Z_{eq}) = \frac{R_{Fe} \cdot (2\pi f L)^2}{R_{Fe}^2 + \left(2\pi f L - \frac{1}{2\pi f C}\right)^2} \approx 14\,\text{m}\Omega. \tag{22}$$

This is equivalent to an increase of the winding resistance and a decrease of the quality factor by roughly 20%, respectively. Considering a triangular current mode (TCM) inverter designed to comply with the Google Little Box Challenge specifications [7], similar to the converter presented in [6] but with lower output inductance value (7 µH instead of 10 µH), it is estimated that the ferrite conduction losses amount on average to an additional 240 mW core loss per inductor. To minimize these additional losses the distance between the outer magnetic core and the winding packages can be increased. However, this leads to an increase in inductor size. A further possibility is to insert a low impedance shielding layer between the ferrite and the winding packages in order to bypass the impedance of the core (cf., Fig. 19(b)). For this purpose a copper foil with a thickness in the range of 20 µm can be used or the ferrite material can be coated with copper by a galvanic process. As can be seen in Fig. 20 (measurement device Agilent 4294A) the utilization of the shield avoids the conduction losses in the ferrite material, the quality factor at high frequencies increases to the value corresponding to the HF winding resistance (e.g., at f = 1 MHz from Q = 505 to Q = 610). It can also be noticed that the apparent increase of inductance value due to the occurring resonance is shifted slightly to a lower frequency in case of the shielded inductor because of the increase in winding capacitance of roughly 2 pF.

Appendix D
Electrical Measurement of Surface Loss

Several electrical core loss measurement techniques have been presented in literature and a comprehensive overview is given in [42]. In the conventional two-winding wattmeter method, the core loss is calculated with the measured primary current and the induced voltage across a second auxiliary winding used to exclude ohmic losses of the excitation winding from the power measurement. The measurement error derived in [41] for a given phase-shift between voltage and current, φ_2, and a phase discrepancy introduced by the instrumentation, $\Delta\varphi$, is given by

$$\Delta = \tan(\varphi_2) \cdot \Delta\varphi \approx Q \cdot \Delta\varphi. \tag{23}$$

Thus, in order to minimize the potential measurement error caused by bandwidth limitations and/or uncompensated delays of the employed probes and to enable the characterization of high-Q, low-loss core materials at high frequencies,the sensitivity to phase errors is reduced by compensating the reactive impedance of the device under test (DUT) with a series connected capacitor or an air core inductor with opposing winding directions [41], [43]. A disadvantage of this technique is that add. power loss from the resonance capacitor (or air core inductor) is included in the power measurement and must be subtracted from the total loss based on a loss model of the component. The basic circuit schematic of the two-winding method with resonance capacitor is shown in Fig. 21(a) and typical waveforms for sinusoidal excitation are depicted in Fig. 21(b), showing that the aux. voltage $v_{aux} = v_L + v_C$ is in phase with the excitation current i_p. According to literature, the resistance modeling the core losses is typ. drawn in series with the magnetizing inductance rather than in parallel since this facilitates a straightforward calculation of the losses for given primary current. Fig. 21(c) shows the test circuit employed in this study with additional sense winding with N_2 turns and a varistor at the input to protect the HF voltage source (Iwatsu IE-1125B) from over voltages. The sense winding is not used for the power instrumentation but to ensure the correct flux density amplitude in the sample as mentioned previously. For the two-winding wattmeter method to correctly exclude the winding losses, the excitation and auxiliary winding must feature close to ideal coupling. Now, the total losses measured with the test circuit are the sum of core losses in the E-type test circuit, P_{test}, the losses of the inserted multi-gap sample, P_{sample}, and the additional loss in the resonance capacitor, P_{cap},

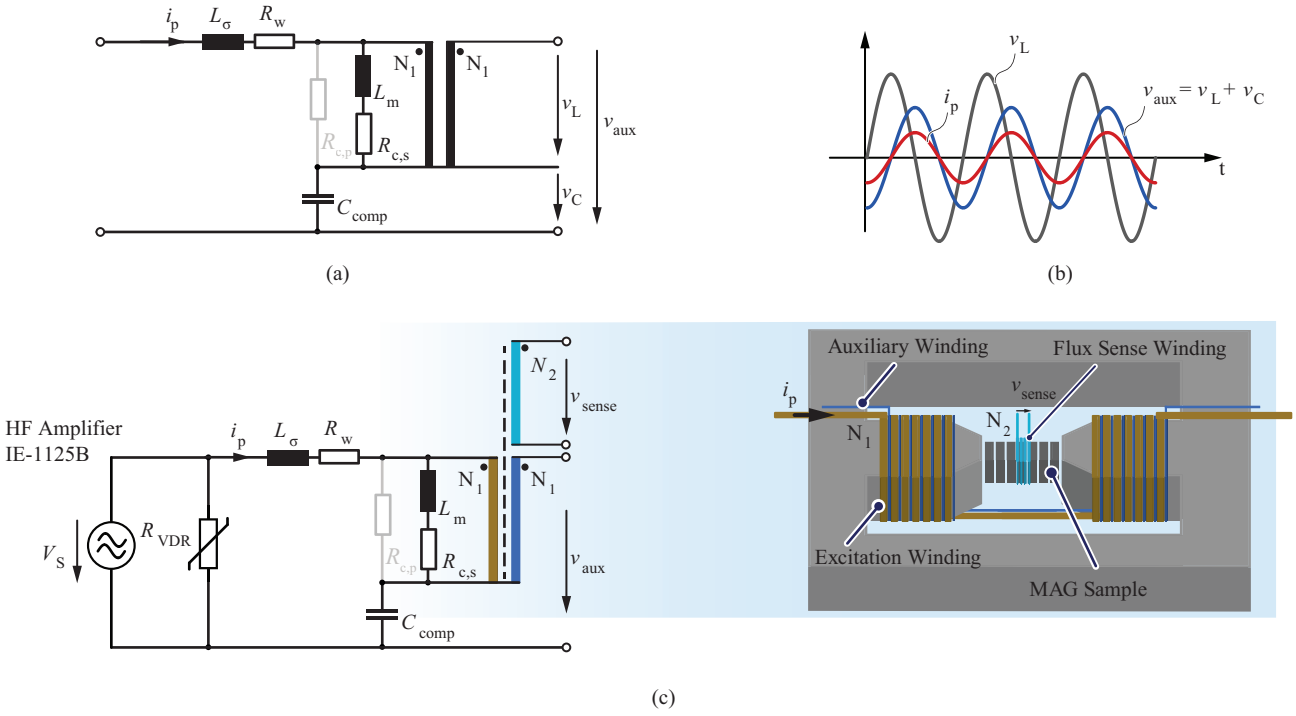

Fig. 21. (a) Circuit schematic of the two-winding wattmeter method with resonance capacitor and (b) typical waveforms for sinusoidal excitation showing that the aux. voltage $v_{aux} = v_L + v_C$ is in phase with the excitation current i_p. (c) Electrical core loss test circuit used in this study with additional sense winding with N_2 turns and a varistor at the input to protect the HF voltage source; for the two-winding wattmeter method to correctly exclude the winding loss, the excitation and auxiliary winding must feature close to ideal coupling. The sense winding in this work is not used for the power instrumentation but to ensure the correct flux density amplitude in the sample.

$$P_{tot} = \frac{1}{T_m}\int_0^{T_m} v_{aux} i_p \, dt = P_{sample} + P_{test} + P_{cap}. \tag{24}$$

As proposed at the beginning of Section III, the total losses in the multi-gap core are the sum of the conventional core losses associated with the bulk ferrite material of the individual plates, $P_{sample,c}$, and the surface related loss component, $P_{sample,s}$. It follows that,

$$P_{tot} = P_{sample,s} + P_{sample,c} + P_{core} + P_{cap}. \tag{25}$$

In order to extract $P_{sample,s}$ from the total measured loss the following idea is proposed. For a specific operating point $\{\hat{B}, f\}$, two loss measurements using multi-gap samples with distinct number of gaps are carried out. The samples are constructed in such a way that the total ferrite core volume remains constant and the individual gaps are adjusted to achieve identical reluctance. An example of two samples with 5 and 15 plates is provided in Table IV. It follows that for an identical reluctance of the two considered multi-gap samples, the equivalent reluctance of the entire magnetic test setup (test circuit and sample) remains constant and consequently the necessary excitation current to impress a specific flux density level in the sample will be equal. As a result, the losses of the test circuit and the resonance capacitor should ideally remain constant for a given operating point regardless of how many gaps are present in the installed sample. Now, the difference of two loss

TABLE IV
TWO DISTINCT SAMPLES WITH IDENTICAL CORE AND TOTAL GAP LENGTH

# Gaps	Plate Thickness	Gap Length	Sample Length
4	3 mm	175 µm	15 .7 mm
14	1 mm	50 µm	15 .7 mm

measurements with samples featuring a total of u and v gaps, is given by

$$\Delta P^{(u,v)} = P^u_{tot} - P^v_{tot}, \tag{26}$$

$$\overset{(25)}{=} (P^u_{sample,s} + P^u_{sample,c} + P^u_{test} + P^u_{cap}) - (P^v_{sample,s} + P^v_{sample,c} + P^v_{test} + P^v_{cap}) \tag{27}$$

$$= P^u_{sample,s} - P^v_{sample,s}, \tag{28}$$

wherein $P^u_{sample,c} = P^v_{sample,c}$ because the samples are designed to feature identical bulk volume (neglecting minus cule surface layer volume difference between samples), and $P^u_{core} = P^v_{core}$, $P^u_{cap} = P^v_{cap}$ because of the identical reluctance and excitation current as mentioned previously. The surface loss in a sample with u gaps can furthermore be expressed as

$$P^u_{sample,s} = \tilde{\kappa}_s (2(u+1)\cdot A_p), \tag{29}$$

where $\tilde{\kappa}_s$ is the surface loss density of plates with cross section

A_p. Inserting (29) in (26) and rearranging yields

$$\tilde{\kappa}_s = \frac{\Delta P^{(u,v)}}{2(u-v)\cdot A_p}. \tag{30}$$

Thus by subtracting two measurements with identical operating point but using samples with different number of gaps the surface loss density can be extracted.

Unfortunately, the perfect cancellation of the test circuit power loss cannot be achieved in reality. Although it is quite challenging, it is possible to tune the gap length such that the impedance analyzer reads similar inductance values of the test circuit with either of the two samples installed. However, achieving a similar overall inductance value does not imply identical leakage flux conditions in the test circuit. Depending on the installed sample (cf., Table IV), a difference of up to 15% – 20% of required magnetization current for a specific flux density amplitude was observed during first preliminary measurements.

Now, from (29) and (30) it can be seen that the measurement error of the surface loss density is directly determined by the error in computing ΔP. The error in ΔP is not only affected by the error in the power instrumentation but also takes into account the systematic error arising from different leakage flux conditions in the test circuit and uncertainty in the ESR of the resonance capacitor which can be mitigated by using a large number of turns in the primary winding in order to keep current i_p low. Still, a rel. error of 15% – 20% in the P_{tot} loss measurement is a reasonable estimate. Furthermore, for a sample with 15 plates and a mid-range operating point {125 mT, 400 kHz} the actual surface loss amounts to just 20% – 30% of the total measured power, P_{tot}. It follows then that the relative measurement error of $\tilde{\kappa}_s$ is likely in the range

$$\frac{\sigma\tilde{\kappa}_s}{P_{sample,s}} = \frac{(10\%-15\%)\cdot P_{tot}}{(20\%-30\%)\cdot P_{tot}} \approx 33\%-75\%, \tag{31}$$

which is too pronounced to obtain robust experimental results for a comparison of different ferrite materials and to examine the impact of different machining/manufacturing techniques and post-machining treatments on the surface loss. Since a direct measurement of the sample loss reduces the relative measurement error significantly, the thermometric measurement technique based on accurate temperature rise monitoring as discussed in Section III of this paper was developed.

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References

[1] J. Hu and C. R. Sullivan, "The Quasi-distributed gap technique for planar inductors: Design guidelines," in *Proc. IEEE Ind. Appl. Conf.*, Oct. 1997.

[2] J. Hu and C. R. Sullivan, "AC resistance of planar power inductors and the quasidistributed gap technique," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 558–567, 2001.

[3] F. Zajc, "Multi gap inductor core, multi gap inductor, transformer and corresponding manufacturing method and winding," European Union Patent Application EP 2 528 069 A1, Nov., 2012.

[4] Z. Franc, "Flat band winding for an inductor core," U.S. Patent US2 012 299 681(A1), Nov., 2012.

[5] Z. Franc, "Winding arrangement for inductive components and method for manufacturing a winding arrangement for inductive components," U.S. Patent US2 015 325 361(A1), Nov., 2015.

[6] D. Bortis, D. Neumayr, and J. W. Kolar, " $\eta\rho$-pareto optimizationand comparative evaluation of inverter concepts considered for thegoogle little box challenge," in *Proc. 17th IEEE Workshop Control Modeling Power Electron. (COMPEL)*, June 2016.

[7] GOOGLE, "Detailed inverter specifications, testing procedure, andtechnical approach and testing application requirements for the littlebox challenge," GOOGLE, Tech. Rep., 2015. [Online]. Available: https://www.littleboxchallenge.com

[8] C. R. Sullivan, H. Bouayad, and Y. Song, "Inductor design for lowloss with dual foil windings and quasi-distributed gap," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE US)*, 2013.

[9] C. R. Sullivan, "Layered foil as an alternative to litz wire: multiple-methods for equal current sharing among layers," in *Proc. 15th IEEE Workshop Control Modeling Power Electron. (COMPEL)*, 2014.

[10] E. Stern and D. Temme, "Magnetostriation effects in remanence phase shifters," *IEEE Trans. Microwave Theory Techn.*, vol. 13, no. 6, pp. 873–874, Nov. 1965.

[11] J. E. Knowles, "The effect of surface grinding upon the permeabilityof manganese - Zinc ferrites*," J. Physics D: Appl. Physics*, vol. 3, no. 9, pp. 1346, 1970.

[12] J. Knowles, "The origin of the increase in magnetic loss induced by machining ferrites," *IEEE Trans. Magn.*, vol. 11, no. 1, pp. 44–50, Jan. 1975.

[13] E. Snelling, "The effects of stress on some properties of MnZn ferrite," *IEEE Trans. Magn.*, vol. 10, no. 3, pp. 616–618, Sep. 1974.

[14] E. Klokholm and H. L. Wolfe, *Surface Damage in Manganese Zincand Nickel Zinc Ferrites*. Dordrecht: Springer Netherlands, 1984, pp.665–681.

[15] S. Chandrasekar and B. Bhushan, "Comparison of grinding and lapping of ferrites and metals," *J. Eng. Ind.*, vol. 109, no. 2, pp. 76–82, 1987.

[16] S. Chandrasekar and B. Bhushan, "Control of surface finishing residual stresses in magnetic recording head materials," *J. Tribol.*, vol. 110, no. 1, pp. 87–92, 1988.

[17] B. Bhushan, *Tribology and mechanics of magnetic storage devices*, 2nd ed. Springer-Verlag, 1990.

[18] H. Naumoski, B. Riedm¨uller, A. Minkow, and U. Herr, "Investigation of the influence of different cutting procedures on the global and local magnetic properties of non-oriented electrical steel," *J. Magnetism & Magn. Materials*, vol. 392, pp. 126–133, 2015.

[19] M. Hofmann, H. Naumoski, U. Herr, and H. G. Herzog, "Magnetic properties of electrical steel sheets in respect of cutting: micromagnetic analysis and macromagnetic modeling," *IEEE Trans. Magn.*, vol. 52, no. 2, pp. 1–14, 2016.

[20] M. Bali, H. De Gersem, and A. Muetze, "Determination of original nondegraded and fully degraded magnetic characteristics of material subjected to laser cutting," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4242–4251, 2017.

[21] V. Loyau, M. Lo Bue, and F. Mazaleyrat, "Measurement of magnetic losses by thermal method applied to power ferrites at high level of induction and frequency," *the Review of Scientific Instruments*, vol. 80, no. 2, 2009.
[22] T. Komma and H. Gueldner, "A method of determining core losses caused by a DC flux-density bias," in *Proc. Int. Exhibition Conf. Power Electron, Intell. Motion, Renewable Energy (PCIM Europe)*, Nuremberg, Germany, 2002.
[23] V. Loyau, M. Lobue, and F. Mazaleyrat, "Comparison of losses measurement in a ferrite with two calorimetric methods," *IEEE Trans. Magn*., vol. 46, no. 2, pp. 529–531, 2010.
[24] L. Ferraris, F. Franchini, and E. Pokovi, "A thermographic method for the evaluation of the iron losses distribution in electromagnetic devices," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2016.
[25] H. Shimoji, B. E. Borkowski, T. Todaka, and M. Enokizono, "Measurement of core-loss distribution using thermography," *IEEE Trans. Magn*., vol. 47, no. 10, pp. 4372–4375, Oct. 2011.
[26] L. Ferraris, E. Poskovic, and F. Franchini, "Defects detection in laminated and soft magnetic composites devices with a novel thermographic method," in *Proc. 11th IEEE Int. Symp. Diagnostics Elect. Machines Power Electron. Drives(SDEMPED)*, Aug. 2017.
[27] H. Shimoji, B. E. Borkowski, T. Todaka, and M. Enokizono, "Visualizing iron loss distribution in permanent magnet motors," in *Proc. 15th IEEE Int. Conf. Elect. Mach. Syst. (ICEMS)*, Oct. 2012.
[28] FLIR, "FLIR A655sc Infrared Camera Datasheet," Brochure, 2014. [Online]. Available: http://www.flirmedia.com/MMC/THG/Brochures/RNDn 011/RNDn 011n US.pdf
[29] Infrared Camera Accuracy and Uncertainty in Plain Language, Tech. Note, 2016. [Online]. Available: https://www.flir.com/discover/rd-science/infrared-camera-accuracy-and-uncertainty-in-plain-language/
[30] A. A. Clifford, *Multivariate Error Analysis: A Handbook of Error Propagation and Calculation in Many-Parameter Systems*. Wiley, 1973.
[31] Ferroxcube, "Ferroxcube Software Design Tool (SFDT 2010)," [Online]. Available: https: //www.ferroxcube.com/en-global/design tool/index, 2010, last accessed 2018-04-23.
[32] C. A. Baguley, U. K. Madawala, and B. Carsten, "Unusual effects measured under DC bias conditions on MnZn ferrite material," *IEEE Trans. Magn*., vol. 45, no. 9, pp. 3215–3222, 2009.
[33] C. A. Baguley, U. K. Madawala, and B. Carsten, "The impact of vibration due to magnetostriction on the corelosses of ferrite toroidals under DC bias," *IEEE Trans. Magn*., vol. 47, no. 8, pp. 2022–2028, 2011.
[34] C. A. Baguley, U. K. Madawala, B. Carsten, and M. Nymand, "The impact of magnetomechanical effects on ferrite B-H loop shapes," *IEEE Trans. Magn*., vol. 48, no. 8, pp. 2284–2292, 2012.
[35] R. S. Yang, A. J. Hanson, D. J. Perreault, and C. R. Sullivan, "A low-loss inductor structure and design guidelines for high-frequency applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2018.
[36] Duralco, "Duralco/Durapot Epoxide," [Online]. Available: http://www.polytec-pt.com/de/produkte/hochtemperaturklebstoffe-und-keramische-materialien/hochtemperatur-epoxide/,2010, last accessed 2018-03-26.
[37] H. Meuche, A. Nguyen, D. Lange, and M. Esguerra, "Influence of a mechanical stress on ferrite materials for broadband applications," in *Proc. 9th Int. Conf. Ferrites (ICF-9)*, 2004.
[38] V. Tsakaloudi, D. Holz, and V. Zaspalis, "The effect of externally applied uniaxial compressive stress on the magnetic properties of power MnZn-ferrites," *J. Material Sci*., vol. 48, no. 10, pp. 3825–3833, May 2013.
[39] M. Baumann, S. Sotier, and J. Weidinger, "A model of initial permeability of soft ferrite in dependence of biaxial stress," *J. Japan Soc. Powder & Powder Metallurgy*, vol. 61, no. S1, pp.70–74, May 2014.
[40] T. Thomas, S. Hoffmann, K.-F. Becker, H. Walter, V. Bader, T. Braun,E. Hoene, and M. Schneider-Ramelow, "Ferrite embedding for power SiPs - A packaging view," in *Proc. 10th IEEE Conf. Integrated Power Electron. Syst. (CIPS)*, 2018.
[41] M. Mu, Q. Li, D. J. Gilham, F. C. Lee, and K. D. T. Ngo, "New core loss measurement method for high-frequency magnetic materials," *IEEE Trans. Power Electron*., vol. 29, no. 8, pp. 4374–4381, Aug. 2014.
[42] C. R. Sullivan, "Survey of Core Loss Test Methods," 2017. [Online]. Available: http://sites.dartmouth.edu/power-magnetics/files/2017/03/Survey-of-Core-Loss-Test-Methods-Sullivan.pdf
[43] D. Hou, M. Mu, F. C. Lee, and Q. Li, "New high-frequency core loss measurement method with partial cancellation concept," *IEEE Trans. Power Electron*., vol. 32, no. 4, pp. 2987–2994, Apr. 2017.

Dominik Neumayr started his academic education at the University of Applied Sciences (FH) for Automation Engineering in Wels, Austria and received the Dipl.-Ing. (FH) degree in 2008.

He was with the Center for Advanced Power Systems (CAPS) in Tallahassee, FL, USA, working on Power/Controller Hardware-in-the-Loop Simulations and Control Systems Design for AC/DC/AC PEBB based converter systems from ABB. He continued his academic education at the Swiss Federal Institute of Technology in Zurich (ETH Zurich) with a focus on power electronics and control engineering and received the M.Sc. degrees in Electrical Engineering and information technology in 2015. Since spring 2015 he is a Ph.D. student at the Power Electronic Systems (PES) Laboratory, ETH Zurich. His current research focuses on the design and control of high power density converter systems.

Dominik Bortis received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Post-doctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 Dr. Bortis is heading the newly established research group Advanced Mechatronic Systems at PES.

Johann W. Kolar received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria, in 1997 and 1999, respectively. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 70 Ph.D. students. He has published over 650 scientific papers in international journals and conference proceedings, 3 book chapters, and has filed more than 160 patents. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 27 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, and the ETH Zurich Golden Owl Award for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an associate editor of the *IEEE Transactions on Power Electronics*. Since 2002 he also is an associate editor of the *Journal of Power Electronics of the Korean Institute of Power Electronics* and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*.

Stefan Hoffmann successfully completed his M.Sc. at the Technical University Berlin, Germany in 2010. At the beginning of 2011 he was assigned as a research assistant to the Power Electronics working group at Fraunhofer Institute for Reliability and Microintegration, Berlin, Germany. His current research interests include investigations on magnetic materials, design of power electronic systems and EMC.

Eckart Hoene received his Diploma degree in Electrical Engineering from the Technical University Berlin in 1997. He then joined Fraunhofer Institute for Reliability and Microintegration, Berlin, Germany as scientific assistant and worked in parallel towards his Ph.D., which he received in 2001 from the TU Berlin. He continued at Fraunhofer as Postdoc, group leader and business development manager. In 2014 he became adjunct professor at Aalborg University, in addition to the courses he conducts for the European Center for Power Electronics (ECPE) and his Fraunhofer affiliation. His technical interests are in high switching frequency power electronics, semiconductor packaging and EMC.

Online Junction Temperature Estimation Method for SiC Modules With Built-in NTC Sensor

Ping Liu, Changle Chen, Xing Zhang, and Shoudao Huang

***Abstract*—Silicon carbide (SiC) devices characterized by high efficiency, high power density and wide bandgap, have great potential in many advanced applications, such as electric automotive, aviation and military. Thermal management, condition monitoring and life estimation of SiC modules are essential to achieve high reliability. These control techniques require realtime monitoring or estimation of the module's junction temperature. This paper proposed a thermal model based on an integrated negative thermal coefficient (NTC) thermistor in SiC modules. The Finite Element Methods simulation results showed that the parameters of the thermal model are invariant under different heat dissipation conditions and ambient temperatures. The combination of the proposed thermal model with the reading of NTC sensor realized the online estimation of the junction temperature. The accuracy of the thermal model and the independence of thermal impedance were verified by simulation and experimental results.**

***Index Terms*—Boundary conditions, junction temperature, silicon carbide (SiC), thermal model.**

I. Introduction

SILICON carbide (SiC) power semiconductor devices, with great potential in future power electronic conversion systems, have been widely used in high-reliability applications, such as automotive, aerospace and military. The SiC modules have the features of higher power densities, more compact package and higher efficiency. These features make it crucial to find a precise method of measuring or estimating junction temperature of SiC devices during the operation. In addition, the precise real-time junction temperature plays an important role in the thermal management control, condition monitoring and lifetime estimation. It will facilitate the reliability and stability analysis of the SiC devices.

In the literature, many studies have been conducted on chip/power module thermal analysis. There are several advanced simulation tools used, such as Finite Element Method (FEM), Finite Difference Method (FDM) and Finite Volume Method (FVM) [1]–[3]. All of them can provide precise and detailed thermal information of the power devices during steady-state and transient operation. However, massive computation time are needed due to the complex three-dimensional structure of the power modules and multi-physics environments. Thus, they are not suitable for the long-time load profile analysis of the power modules and online temperature estimation.

Among other solutions, RC-lumped thermal network (RC-TN) and thermo-sensitive electrical parameters (TSEPs) are widely used with fast response [4]–[7]. The RC-TN-based method relies on a one-dimensional RC network with multiple time constants. Fixed thermal impedance values are used, which will change under some special conditions, such as nonlinear characterization, fatigue of thermal interface materials and abnormal cooling conditions. This high dependence on the multi-order thermal model reduces the accuracy of the RC-TN-based method. In addition, the TSEPs-based method has the following limitations: 1) complexity caused by additional circuit; 2) issues on measurement accuracy and robustness to noise; 3) impact of invasive methods on the normal operation. Hence, it is still a challenging task to rapidly and accurately estimate the temperature of the power semiconductor under real-time applications.

In fact, many existing power modules are equipped with a temperature sensor, which usually is a negative thermal coefficient thermistor (NTC). For the module under test in this work, the NTC was located on the same ceramic substrate as the SiC MOSFET and diode chips (see Fig. 1). It could be used to predigest the thermal model of the power module, making it easier to estimate the chip junction temperature under less impact of the thermal grease fatigue and cooling condition changes. Usually, the integrated NTC is only aimed at protecting and monitoring when the junction temperature reaches a threshold value, as well as ensuring turn-off procedures. Few thermal models estimating the junction temperature through the integrated NTC have been proposed in [8]–[10]. However, the fly in the ointment is the response or accuracy when tracking the dynamic junction temperature variation in real-time applications. In [9], an experimental method was put forward to extract the thermal network parameters, ignoring the thermal impedance of the diode. Also, the influence of the heat dissipation effect and ambient temperature on the thermal model was not considered.

In this paper, a thermal model was obtained by FEM simulation, aiming to estimate the junction temperature for the power devices in SiC power module [11], [12]. Based on this method, estimation of the junction temperature can be realized by the NTC sensor reading and the thermal network between the chips and NTC. Due to the use of NTC, analyzing the thermal

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The authors are with the College of Electrical and Information Engineering, Hunan University, Changsha, China (e-mail: lp1481@gmail.com; chenchangle@hnu.edu.cn; zhxing@hnu.edu.cn; hsd1962@hnu.edu.cn).

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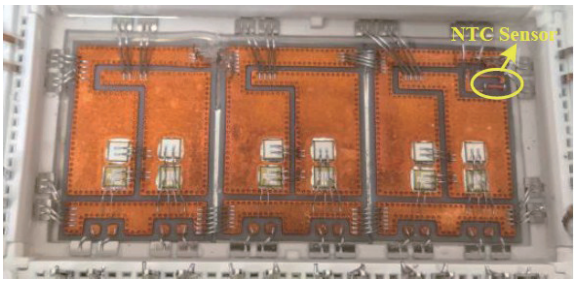
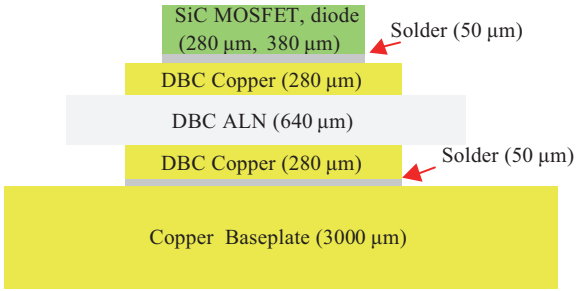
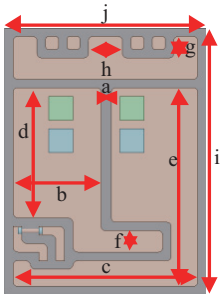


Fig. 1. Module under test (CREE 1200 V/20 A, SiC MOSFET module: CCS020M12CM2).



(a)



Dimension	Size(mm)
a	1.2
b	10.3
c	21.6
d	19.24
e	23.24
f	2.5
g	2.5
h	4.0
i	31.24
j	23.6

(b)

Fig. 2. Thickness and length dimension of each layer of the SiC MOSFET module.

resistance of the low physical layers becomes unnecessary. In addition, experimental results showed the thermal resistance remained unchanged under different heatsink or ambient temperature conditions. It proved the proposed model to be much applicable to the circuit simulator for long-time load profile analysis or the condition monitoring of the power modules.

II. Modeling of Thermal Impedance Network

The test SiC module CREE CCS020M12CM2 in the paper is shown in Fig. 1. In detail, the selected SiC MOSFET module consists of 3 half-bridge parallel converters, including 6 MOSFET and 6 diode chips, which are all installed on the Direct Copper Bonded (DCB). The three-dimensional finite element simulation model and structural parameters of this module are presented in Fig. 2. The finite element simulation model of the SiC MOSFET module is provided in Fig. 3.

When the SiC MOSFET module is operated under low-frequency and high-power or standstill conditions, a maximum DC current will flow through a single diode continuously. This may result in a rapid growth in the junction temperature of the

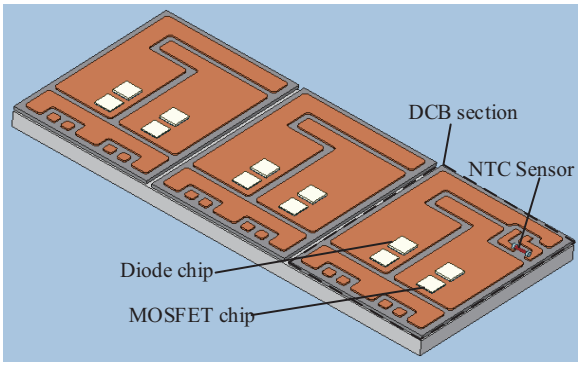


Fig. 3. Schematic of the 1200 V/20 A SiC MOSFET module modeled FEM analysis.

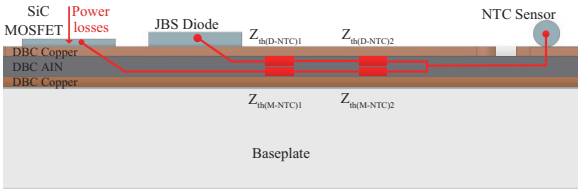


Fig. 4. Thermal model of the SiC MOSFET module with integrated NTC sensor.

diode. Therefore, establishing thermal models for both MOSFET and diode becomes essential. Fig. 4 shows the thermal model of the SiC MOSFET module established by NTC, where $Z_{th(M\text{-}NTC)}$ and $Z_{th(D\text{-}NTC)}$ represent the thermal resistance from the MOSFET and the diode respectively to NTC. The relationship between the transient thermal impedance $Z_{th(j\text{-}N)}(t)$ and the step power loss at the chip is defined as:

$$Z_{th(j-N)}(t) = \frac{T_j(t) - T_{NTC}(t)}{P(t)} \tag{1}$$

After obtaining the power loss P(t) of the SiC MOSFET module and the NTC temperature T_{NTC}, junction temperatures with any power dissipations can be expressed by (2), which is the form in s-domain. The power losses used in the thermal model are calculated based on the SiC module datasheet. The power loss for the power semiconductor devices is composed of two parts: conduction loss and switching loss, which has been well investigated [13].

$$\begin{aligned} T_{MOSFET}(s) &= (Z_{th(M-NTC)1}(s) + Z_{th(M-NTC)2}(s))*P_{MOSFET}(s) + T_{NTC}(s) \\ T_{Diode}(s) &= (Z_{th(D-NTC)1}(s) + Z_{th(D-NTC)2}(s))*P_{Diode}(s) + T_{NTC}(s) \end{aligned} \tag{2}$$

To get the junction temperatures, thermal impedance between the chip and NTC is in need. A second-order Foster thermal network is shown in Fig. 5, the dynamic response of which can well reflect the heat flow from the MOSFET or diode to the NTC sensor by the curve fitting method. Therefore, the thermal impedance elements in (2) are represented by this circuit impedance. The transfer function of the thermal network is obtained as:

$$Z_{th(j-N)}(s) = \frac{R_{th(j-N)1}}{1 + s\tau_{th(j-N)1}} + \frac{R_{th(j-N)2}}{1 + s\tau_{th(j-N)2}} \tag{3}$$

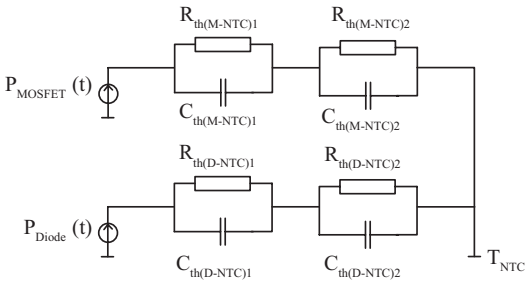


Fig. 5. Proposed Foster thermal model.

TABLE I
BOUNDARY CONDITIONS IN FEM SIMULATION

Power dissipation	40 W per chip
Ambient temperature	25~100 °C
Coefficient of convection with air	10~10000 W/(m^2•K)
Elements	18167

where the time constant $\tau_{th(j-N)}$ equals to $R_{th(j-N)} * C_{th(j-N)}$.

Generally, the fourth-order thermal model of the power module in the datasheet is provided by the power module manufacturer. In practical applications, the thermal model is converted into a difference equation in advance and then applied to achieve programming. The calculation of the thermal model in the datasheet requires 80 instruction cycles. The calculation of the proposed thermal model requires 40 instruction cycles. In terms of programming implementation, the proposed thermal model exhibits a higher response speed.

According to the zero-hold transform method, (3) is transformed into the z-domain transfer function (4), in which T_s is the sampling period. Thus, the z-domain form of (2) is obtained. Then, with the obtained parameters $R_{th(j-N)}$ and $\tau_{th(j-N)}$ in (3), junction temperature of the chip can be estimated by the processor.

$$Z_{th(j-N)}(z) = \frac{b_{th(j-N)1} z^{-1}}{1+z^{-1} a_{th(j-N)1}} R_{th(j-N)1} + \frac{b_{th(j-N)2} z^{-1}}{1+z^{-1} a_{th(j-N)1}} R_{th(j-N)2}$$
$$b_{th(j-N)} = \frac{T_s}{\tau_{th(j-N)}},\ a_{th(j-N)} = b_{th(j-N)} - 1 \quad (4)$$

The step response of the thermal network is expressed by an exponential term as given in (5).

$$Z_{th(j-N)}(t) = \sum_{m=1}^{2} R_{th(j-N)m}\left(1 - \exp\left(-\frac{t}{\tau_{th(j-N)m}}\right)\right) \quad (5)$$

To obtain the proposed thermal network parameters, parameters $R_{th(j-N)}$ and $\tau_{th(j-N)}$ in (5) under different boundary conditions should be derived by the curve fitting of the step response. The ANSYS Workbench was selected to conduct the transient thermal analysis and to obtain the step responses. The boundary conditions of the FEM simulation are listed in Table I.

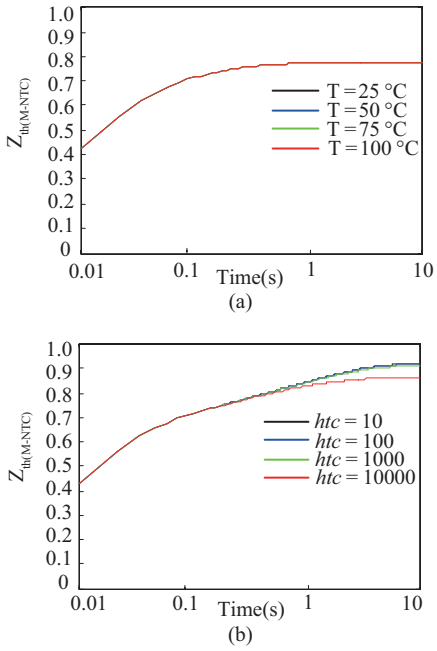


Fig. 6. (a) Thermal resistance $Z_{th(M-NTC)}$ under different ambient temperatures when *htc* is 10000 W/m^2•K. (b) Thermal resistance $Z_{th(M-NTC)}$ under different values of *htc* when ambient temperature is 25 °C.

To explore the impact of heatsink boundary condition on SiC MOSFET modules, a coefficient *htc* was introduced to represent the capability of the cooling system [14]. It can be defined as:

$$htc = \frac{q}{\Delta T}\left[W/m^2 \cdot K\right] \quad (6)$$

where q is the amount of heat transferred between two different materials and ΔT is the temperature difference. The equation indicates that, the higher the *htc*, the better the capability of the heat conduction between different layers with the same heat.

For SiC modules with a certain cooling system (constant *htc* coefficient), the heat is mainly localized beneath the chips. It not only leads to a smaller heat spreading, but also reduces the effective heat dissipation area and increases thermal resistance. This enlarges the temperature difference between the junction and the heatsink. According to the heat transfer textbook, the coefficient *htc* in this paper ranged from 10 W/m^2•K to 10000 W/m^2•K, representing common cooling method like forced convection-air and forced convection-water used in SiC modules [15]. On the other hand, the ambient temperature was set from 25 °C to 100 °C to study the effect on thermal resistance in FEM simulation. As the results shown in Fig. 6 and Fig. 7, little change was found in the thermal resistance $Z_{th(M-NTC)}$ and $Z_{th(D-NTC)}$ under different ambient temperatures, or under different *htc*. This phenomenon may originate from the stalling location of the NTC sensor, which was away from heatsinks and on the same layer with the heat sources.

The thermal model is provided in the datasheet, which shows the necessity to establish a thermal impedance network

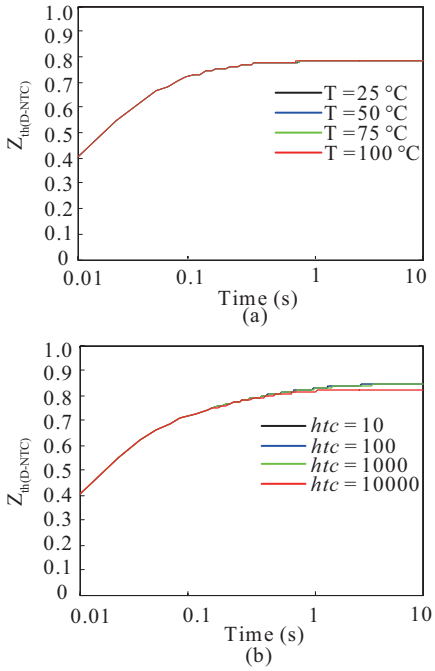


Fig. 7. (a) Thermal resistance $Z_{th(D-NTC)}$ under different ambient temperatures when *htc* is 10000 W/m^2•K. (b) Thermal resistance $Z_{th(D-NTC)}$ under different values of *htc* when ambient temperature is 25 °C.

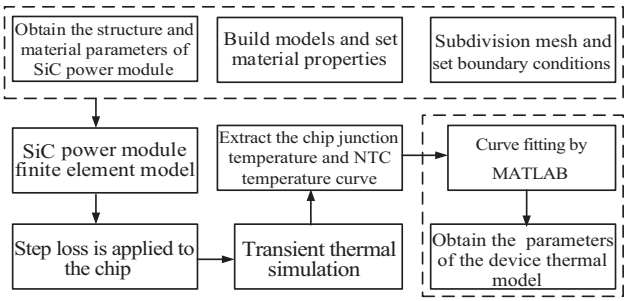


Fig. 8. Flowchart of thermal impedance extraction for SiC module.

from the chip to the heatsink. During the long-term operation of the power module, aging of the solder layer under the substrate plate and thermal grease are inevitable. In this case, the previously determined thermal resistance network model will be greatly offset, resulting in errors in junction temperature prediction. However, as described above, the heat dissipation conditions and ambient temperature of the heatsink have little impact on the heat model proposed in this paper. Therefore, from the perspective of long-term operation, the proposed model is more adaptable and accurate than that described in the datasheet.

Based on the above discussed cases and results, transient thermal impedance $Z_{th(j-N)}(t)$ was obtained from Fig. 8. The three-dimensional finite element model of the SiC module was established by using ANSYS finite element software. Then, a step power loss was loaded on the chip, and the temperature curves of the chips and the NTC sensor were detected. The junction temperature curves of the chips and NTC with ambient temperature T = 25 ˚C and *htc* = 10 W/m^2•K are shown in

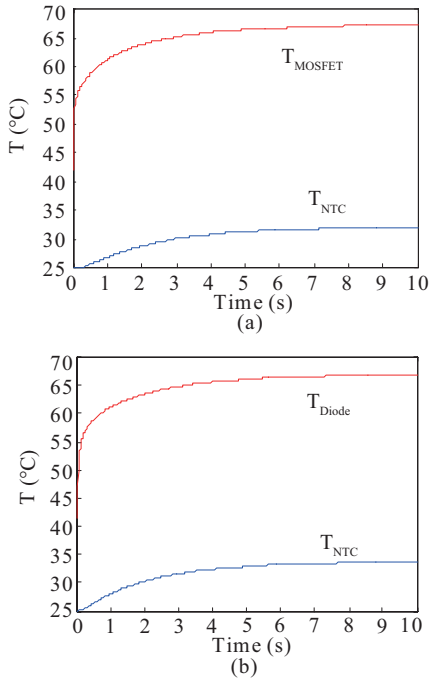


Fig. 9. (a) Thermal responses of the MOSFET chip and NTC. (b) Thermal responses of the diode and NTC.

TABLE II
THERMAL IMPEDANCE OF MOSFET-TO-NTC AND DIODE-TO-NTC

	MOSFET ($Z_{th(M-NTC)}$)		Diode ($Z_{th(D-NTC)}$)	
R_{th} [K/W]	0.7085	0.1682	0.6659	0.1642
C_{th} [J/K]	0.0141	2.9727	0.01502	1.2
τ_i [s]	0.01	0.5	0.01	0.2

Fig. 9. Finally, the parameters of the thermal impedance in (5) were acquired by means of the curve fitting method. Thermal impedance parameters under different coefficient *htc* and ambient temperatures were described as constants, listed in Table II. With all the impedance parameters obtained, junction temperatures were then estimated by the z-domain form of (2) in the microcontrollers.

III. SIMULATION AND EXPERIMENTAL VERIFICATION

To verify the accuracy of the presented thermal model, simulations were performed through MATLAB/Simulink and FEM. On basis of Fig. 5 and (2), a thermal model was built, in which MATLAB/Simulink was used to estimate the junction temperature of the chips in the SiC power module. The estimation results were indicated by the comparison between the FEM simulation and the experimental results.

Fig. 10 shows the simulated junction temperature under different load conditions. Parameters in MATLAB/Simulink simulation are listed in Table III. The experimental results using the proposed model were found to be in line with those of the FEM simulation.

The effectiveness of the presented method was verified by an experiment, in which an opened SiC module was mounted

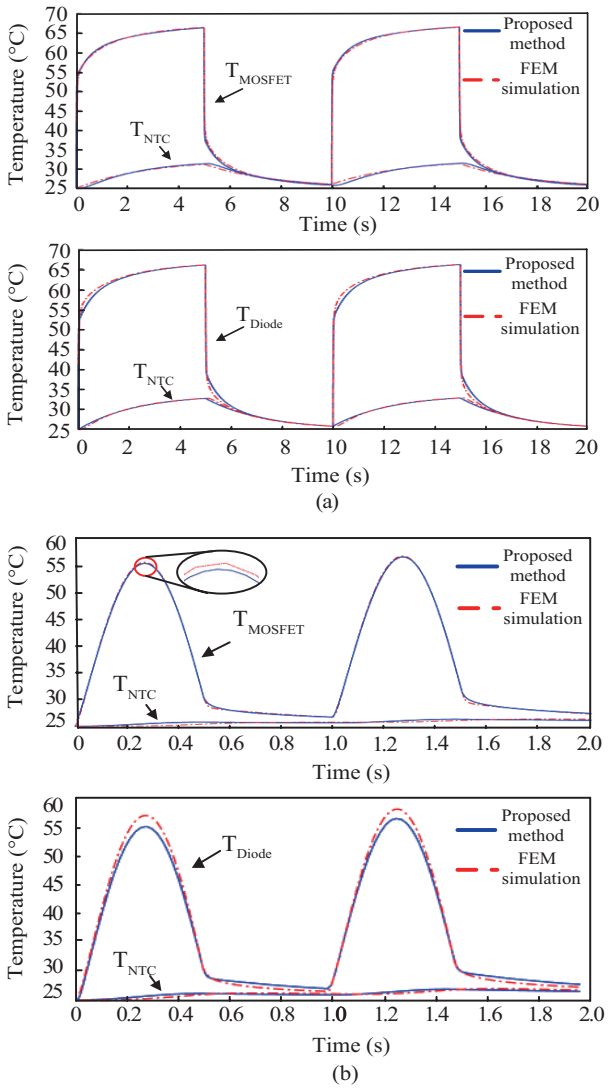


Fig. 10. Estimated junction temperatures of SiC MOSFET and diode under different load conditions: (a) Square wave load. (b) AC load.

TABLE III
SIMULATION PARAMETERS IN MATLAB/SIMULINK

	Square waveform load	AC load
Peak power	40 W	
Period	10 s	1 s
Duration	5 s	0.5 s
Ambient temperature	25 °C	

on a heatsink. An isolated optical fiber temperature sensor OTG-F-10 from Opsens was selected to directly measure the junction temperature of the power devices, as shown in Fig. 11(a). The test conditions for the inspected SiC MOSFET module were a square wave load with a peak current of 5 A and a heatsink temperature of 25 °C. The test period was set as 20 seconds with a duty cycle of 50%.

Fig. 11(b) shows the estimated temperature and measured

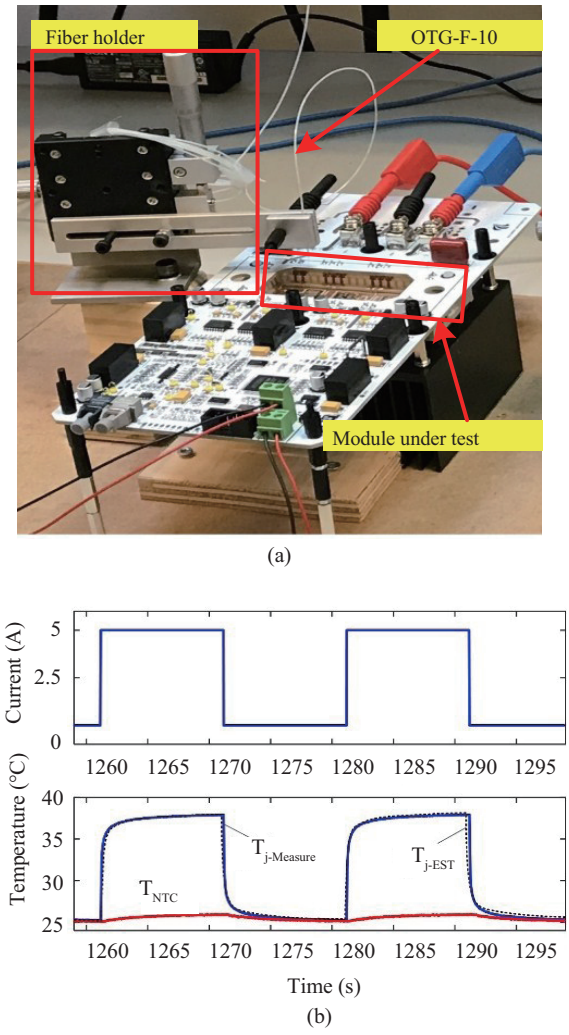


Fig. 11. Experimental set-up and results: (a) Photo of the set-up which shows SiC module with optical fibers for temperature measurement. (b) Experimental results during power cycling test: (upper) load current, (lower) measured $T_{j\text{-}Measure}$ of SiC MOSFET, and estimated $T_{j\text{-}EST}$ using proposed thermal model and T_{NTC}.

temperature during the power cycling test. It was found that the estimation junction temperature ($T_{j\text{-}EST}$) obtained by the proposed thermal model was consistent with the measured result ($T_{j\text{-}Measure}$).

IV. CONCLUSIONS

In this paper, a new junction temperature estimation method based on integrated NTC sensor for SiC modules was presented. A second-order Foster thermal network was established to represent the heat transfer between the chips and the integrated NTC. The comparison between the simulation and the experimental results demonstrates the following advantages of the proposed method: 1) compared with the conventional RC-TN-based solution, it has faster response and improved accuracy in junction temperature estimation with second-order RC lumped thermal network; 2) it is non-invasive with

simple implementation and gets little impact from the ambient temperature or heatsink condition changes; 3) it is able to realize quick, accurate and robust measurement of the power modules' online temperature; 4) it is much appropriate to be used in circuit simulators for long-time load profile analysis or the condition monitoring of power modules.

References

[1] D. Cottet, U. Drofenik, and J. Meyer, "A systematic design approach to thermal-electrical power electronics integration," in *2008 2nd Electron. System-Integration Technol. Conf.*, Greenwich, pp. 219–224.

[2] T. Kojima, Y. Yamada, Y. Nishibe, and K. Torii, "Novel RC compact thermal model of HV inverter module for electro-thermal coupling simulation," in *2007 Power Convers. Conf. - Nagoya*, Nagoya, pp. 1025–1029.

[3] S. Carubelli and Z. Khatir, "Experimental validation of a thermal modelling method dictated to multichip power modules in operating conditions," *Microelectron. J.*, vol. 34, pp. 1143–1151, Jun. 2003.

[4] *Thermal design and temperature ratings of IGBT modules*, App. Note 5SYA 2093–00, ABB, pp. 5–6.

[5] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters-A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.

[6] H. Kuhn and A. Mertens, "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters," in *2009 13th Eur. Conf. Power Electron. Appl.*, Barcelona, pp. 1–10.

[7] J. A. Butron Ccoa, B. Strauss, G. Mitic, and A. Lindemann, "Investigation of temperature sensitive electrical parameters for power semiconductors (IGBT) in real-time applications," in *PCIM Eur. 2014 Int. Exhibition Conf. Power Electron., Intell. Motion, Renewable Energy, Energy Manag.*, Nuremberg, Germany, pp. 1–9.

[8] M. Schulz and M. Xin, "Correlating NTC-reading and chip-temperature in power electronic modules," in *Proc. PCIM Eur. 2015 Int. Exhibition Conf. Power Electron., Intelli. Motion, Renewable Energy, Energy Manag.*, Nuremberg, Germany, pp. 1–5.

[9] Y. Zhou *et al.*, "Dynamic junction temperature estimation via built-in negative thermal coefficient (NTC) thermistor in high power IGBT modules," *in 2017 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Tampa, FL, pp. 772–775.

[10] G. Lo Calzo, A. Lidozzi, L. Solero, F. Crescimbini, and V. Cardi, "Thermal regulation as control reference in electric drives," in *2012 15th Int. Power Electron. Motion Control Conf. (EPE/PEMC)*, Novi Sad, pp. DS2c.18–1–DS2c.18–7.

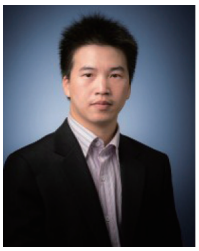
[11] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A 3-D-lumped thermal network model for long-term load profiles analysis in high-power IGBT modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1050–1063, Sept. 2016.

[12] A. J. Morgan, Y. Xu, D. C. Hopkins, I. Husain, and W. Yu, "Decomposition and electro-physical model creation of the CREE 1200V, 50A 3-Ph SiC module," in *2016 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, pp. 2141–2146.

[13] K. Ma, A. S. Bahman, S. Beczkowski, and F. Blaabjerg, "Complete loss and thermal model of power semiconductors including device rating information," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2556–2569, May 2015.

[14] A. S. Bahman, Ke. Ma, and F. Blaabjerg, "General 3D lumped thermal model with various boundary conditions for high power IGBT modules," in *2016 IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, pp. 261–268.

[15] J. H. Lienhard IV and J. H. Lienhard V, *A Heat Transfer Textbook*, 4th ed. Englewood Cliffs, NJ, USA: Prentice-Hall Inc., 2013.



Ping Liu is an Assistant Professor in the College of Electrical and Information Engineering, Hunan University, China. He received the B.S., M.S. and Ph.D. degrees from the department of Electrical Engineering at Chongqing University, China, in 2005, 2008 and 2013, respectively. He was a Research Assistant in the department of Electrical Engineering at Hong Kong Polytechnic University, Hong Kong (2012) and a Post-Doctoral Research Associate at the Mcmaster Institute for Automotive Research and Technology (MacAUTO), Mcmaster University, Canada (2013-2014). He was a visiting scholar in the department of Energy Technology at Aalborg University, Denmark (2017-2018). Liu received the Excellent Paper Award at the 2nd IEEE International Power Electronics and Application Conference and Exposition (PEAC) in 2018 at Shenzhen, China, and the Best Paper Award at the 6th International Conference on Smart Grid (ICSG) in 2018 at Nagasaki, Japan. His primary research interests are the design and control of power electronics and motor drive systems with applications in electric and hybrid electric vehicles.

Changle Chen was born in Nanchang, China. He received B.S. degree in Electrical Engineering from Wuhan University of Tecnology, in 2018. Now he is a graduate student in Hunan University. His research interests include control of permanent magnet synchronous motor and thermal management of power devices.

Xing Zhang was born in Hubei, China in 1994. He received the B.S. degree from Yangtze University, China, in 2016. He is currently a graduate student in Hunan University. His research interests include the active thermal management and lifetime estimation of inverter.

Shoudao Huang was born in Hunan, China, in 1962. He received the B.S. and Ph.D. degrees in Electrical Engineering from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 1983, and 2005, respectively. He is currently a full time Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include motor design and control, poelectronic system and control, and wind energy conversion system.

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ADMINISTRATIVE OFFICE

Add: 16th Floor, Datong Building, No.467 Huanghe Road, Nankai District, Tianjin, 300110, China

Tel: +86-22-27680796 Fax: +86-22-27687886

E-mail: cpss@cpss.org.cn Website: www.cpss.org.cn

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Address: 16th Floor, Datong Building, No.467 Huanghe Road,
Nankai Dist., Tianjin, 300110, China

Tel: +86-22-27680796-18#

Fax: +86-22-27687886

E-mail: tpea@cpss.org.cn

Website: tpea.cpss.org.cn