

Prediction Method of DC Bias in DC-DC Dual-Active-Bridge Converter

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Abstract—The dual-active-bridge (DAB) converter attracts more and more attentions due to its ability of bidirectional power transmission and high conversion efficiency. The adoption of high-frequency transformer provides galvanic isolation, but also brings the possibility of dc bias. In this paper, the causes of dc bias have been analyzed and relevant calculation methods are derived in details. With the calculation methods, the dc bias magnetizing current can be predicted considering the inconsistency of semiconductor switches and driver signals. In other words, if the maximum permitted dc bias of the transformer is given, the range of the inconsistency of semiconductor switches and driver signals can be obtained which helps guide the selection of semiconductor devices and design of the transformer. Therefore, extra flux balancing method can be avoided and the overall cost and volume will be further reduced. Additionally, simulation and experimental results show great agreement with the theoretical analysis.

Index Terms—DC bias, dual-active-bridge converter, prediction method.

I. INTRODUCTION

THE dual-active-bridge (DAB) converter has been widely adopted in the applications for bidirectional power transmission, such as energy storage system [1]. It comprises two active H-bridges and one high-frequency transformer to achieve large voltage transfer ratio and galvanic isolation. At present, the work mainly focuses on the control strategies of the DAB converter. The representative control methods including single-phase shift (SPS), dual-phase-shift (DPS) and triple-phase-shift (TPS) control [2]–[8], aiming to reduce current stress, widen power transmission range and improve conversion efficiency, especially the latter two control strategies. On the other hand, due to the adoption of high-frequency transformer, the dc bias of the transformer needs to be tackled, which can be classified into transient dc bias and steady dc bias. For the transient dc bias which always occurs with the abrupt change of phase-shift angle or input/output voltages, various transient phase shift control strategies are proposed to eliminate the phenomenon [9], [10]. For the steady dc bias, the dc excitation

to the transformer can be caused by non-ideal behavior of the system components, including unmatched turn-on/turn-off times, gate driving signal delays and inconsistency between the parameters of semiconductor devices [11].

In order to eliminate the dc bias of the transformer, various flux measuring and balancing methods have been proposed [11]–[18]. The flux balancing method mainly includes two types: passive balancing and active control. A blocking capacitor connected in series with the winding of the transformer or an air-gap inserted into the core's magnetic path are the main passive balancing methods to eliminate or alleviate the dc bias of the transformer [12], [13], in which no extra control strategy or monitoring devices are needed. However, the blocking capacitor can result in a low-frequency oscillation in response to variations in switching modes, and cause excessive low-frequency EMI [12]. Moreover, this approach can increase the power loss and the volume. Additionally, the air-gap does not eliminate the dc flux component. Hence, the active flux control methods were proposed [11], [14]–[18]. In order to control the dc magnetization of the core, the flux must be measured dynamically, and the flux measuring methods can be mainly classified into flux measurement and current measurement. For the flux measuring methods, extra processing or components such as magnetic ear [11], a slot in the core legs [14], air-gap in the magnetic flux [15], specific type of magnetic core [16], or special sensors are needed to dynamically detect the variation of the flux. For the current measuring methods, the primary and secondary winding currents are sampled to monitor the variation of the magnetizing current [17], [18]. Almost all the measuring methods require high sampling rate and precision, and analog-to-digital converters are even needed [17], [18], which increases the complexity and the overall cost.

With the development of the semiconductor devices manufacturing, the consistency between switches can be guaranteed within certain range. As long as the inconsistency of switches and driving circuits is smaller than certain limitation, the dc bias in the high-frequency transformer can be tolerated. Hence, one calculation method of the dc bias magnetizing current seems necessary, which can also be used to predict the required range of inconsistency with the maximum permitted dc bias magnetizing current given. This can guide the selection of semiconductor devices and the design of transformer, so that extra flux balancing methods can be avoided. One calculation method of the dc bias magnetizing current is proposed in [19] for the zero-voltage-switching (ZVS) converters with the consideration of the

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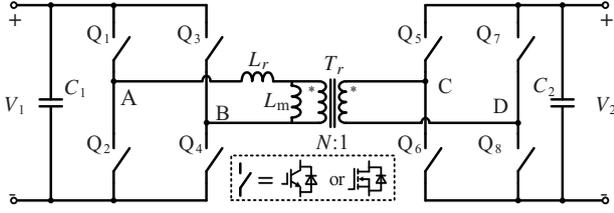


Fig. 1. Typical topology of the DAB converter.

parasitic capacitors in parallel with the switches. However, the calculation equation proposed in [19] is somewhat idealized to calculate the dc bias caused by the inconsistency of devices due to the neglect of on-resistance of the switches and windings. Hence, there is few methods to calculate the maximum dc bias magnetizing current considering the inconsistency of switches and driving circuits.

Considering the inconsistency of switches and driving circuits in practical circuit, a novel method of predicting the maximum dc bias magnetizing current of the DAB converter is proposed in this paper. The DAB converters with IGBTs and MOSFETs are analyzed separately in the paper for the DAB converters with different semiconductor devices have different current paths in some switching modes. The equivalent models are built in Section II firstly and the generation of dc bias is analyzed in Section III. Then, the prediction method is derived in Section IV and examples are given to introduce the predicting procedure in Section V. Experiments are also made to verify the theoretical analysis in Section VI and conclusions are made in Section VII.

II. EQUIVALENT MODEL OF DAB CONVERTER WITH IGBTs AND MOSFETs

In this section, equivalent models of the DAB converters employing IGBTs and MOSFETs are built to conduct the derivation of dc bias magnetizing current. A typical configuration of the DAB converter is shown in Fig. 1. The inductor L_r is the leakage inductor of the transformer T_r , or the summation of the leakage inductor and an external inductor. L_m is the magnetizing inductor of T_r . The turns ratio of T_r is $N:1$, and the primary and secondary winding resistances are set as r_p and r_s , respectively. The anti-parallel diodes or body diodes of $Q_1 \sim Q_8$ are denoted as $D_1 \sim D_8$. In order to simplify the analysis, the transient turn-on or turn-off processes of the switches are neglected.

Because the specific derivation of magnetic flux density dc component B_{dc} is affected by the employment of IGBTs or MOSFETs, the two situations are analyzed separately here and the equivalent models are built in Fig. 2. For IGBTs and diodes, it is assumed that the on-state voltage V_{CE} and forward voltage drop V_F are constant, while for MOSFETs, their on-state resistances R_{ON} are assumed to keep constant. Hence, the parameters in Fig. 2 possess different meanings in IGBTs and MOSFETs applications, which is shown in Table I. For the voltages across $Q_1 \sim Q_8$ and $D_1 \sim D_8$ have been represented as the parameters R_p/R_s and v_{dp}/v_{ds} , v_{AB} and v_{CD} in Fig. 2 can

TABLE I
SPECIFIC EXPLANATIONS OF PARAMETERS IN FIG. 2

	IGBTs Applications	MOSFETs Applications
R_p/R_s	0	Summation of resistance of on-state MOSFETs (R_{pM}/R_{sM})
v_{dp}/v_{ds}	Summation of forward voltages across ON switches or diodes on primary and secondary sides (v_{dp}/v_{dsI})	Summation of the voltage drops across conducted diodes on primary and secondary sides (v_{dpM}/v_{dsM})
v_{AB}/v_{CD}	Voltage across points A and B (C and D) of the DAB converter employing ideal switches in Fig. 1	
r_p/r_s	Resistance of primary/secondary windings	

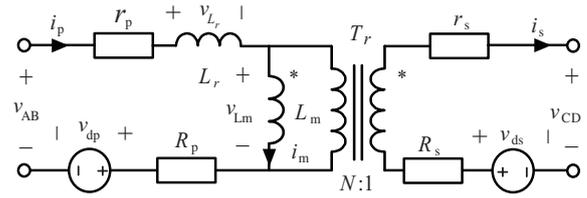


Fig. 2. Equivalent model of the DAB converter.

be seen as the voltage across A and B (C and D) of the DAB converter employing ideal switches. Hence, v_{AB} and v_{CD} are only affected by the voltages V_1 and V_2 , the on/off states of $Q_1 \sim Q_8$ and $D_1 \sim D_8$.

III. ANALYSIS OF THE GENERATION OF DC BIAS

As aforementioned, various factors can cause the magnetic flux density dc component B_{dc} , which can be classified into two types: unmatched turn-on/off times and the inconsistency between the devices. The unmatched turn-on/off times are usually caused by duty cycle loss, gate driving signal delay and so on, while the inconsistency refers to the difference between the on-state resistances or forward voltages of devices caused by differences in connection types, heat dissipation or device manufacturing.

A. Unmatched Turn-on/off Times

When the power is transmitted from V_1 to V_2 and no dc bias occurs, the typical waveforms of the DAB converter with SPS control strategy are shown in Fig. 3, in which the phase-shift time is t_ϕ and the dead time is t_d . And the specific ON switches in each mode are given in Table II. When discussing the effect of unmatched turn-on/off times, parameters of the switches are assumed to be consistent.

For the DAB converters with IGBTs, current i_p flows through the anti-parallel diodes of Q_1 and Q_4 during the time interval $[t_0, t_2]$. Whenever Q_1 and Q_4 returned on, as long as it is later than t_0 and earlier than t_2 , operating state of the converter will not be affected. Hence, the inconsistent time when $Q_1 \sim Q_8$ are turned on will not cause dc bias.

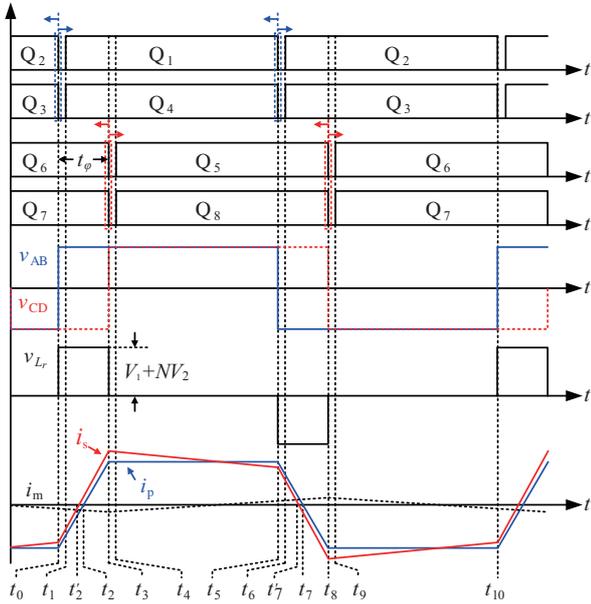


Fig. 3. The typical waveforms of the DAB converter with SPS control.

However, when MOSFETs are adopted as switches, current i_p flows through D_1 and D_4 during the dead zone $[t_0, t_1]$, and flows through the MOSFET channel as soon as Q_1 and Q_4 are turned on. So unmatched turn-on times will introduce an extra mode. Assuming that Q_1 is early turned on, current i_p will flow through D_1 and Q_4 before Q_1 is turned on. For the voltage drops of the body diodes and the voltages across the MOSFETs are different, the voltage across L_r changes and the variation of i_p in two half switching cycle can be unbalanced. Thus, the dc bias of i_p is generated. Moreover, duration of this extra mode is so short that the effect of inconsistent voltage across devices is limited and the dc bias of i_p will be small, which will be analyzed with mathematic derivation in the next section. For the secondary side of the DAB converter, the switching modes are not affected and no dc bias is generated, which will also be verified in the next section.

When the switches are early turned off or the turn-off time is delayed, the operating state will change and the dc bias will be generated in both IGBTs and MOSFETs applications. The situation where Q_2 is turned off earlier than the expected time is taken as an example to introduce how the dc bias is generated. As shown in Fig. 4, when Q_2 is early turned off, i_p increases before the expected time t_0 . The variation of i_p during $[t_0, t_3]$ becomes larger than that during $[t_5, t_8]$, resulting in the positive dc bias of i_p . At the same time, the positive dc bias of i_p causes a positive voltage across the resistances r_p and R_{pm} , which can counteract the extra variation of v_{Lr} during $[t_0, t_3]$ and reduce the increment of the dc bias of i_p . Similarly, the secondary side of the DAB converter is not affected either. Finally, the steady operating state under positive dc bias is achieved.

B. Inconsistency of the Devices

For the DAB converters with IGBTs, it is assumed that the

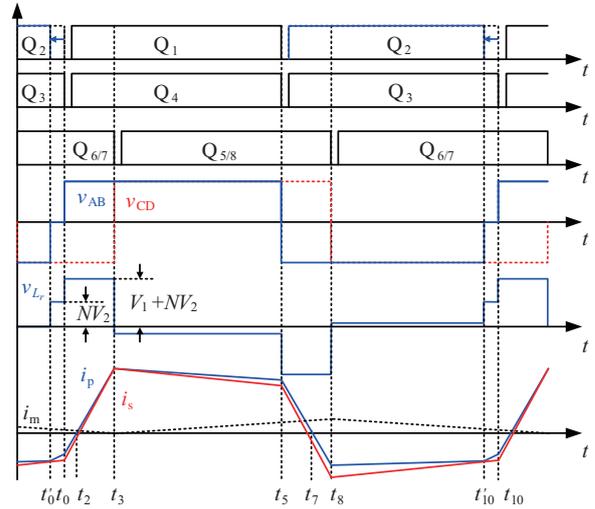


Fig. 4. The waveforms of the DAB converter when Q_2 is early turned off.

voltage drop across anti-parallel diode D_1 is smaller than that of other switches. When D_1 conducts, the voltage across L_r will reduce. So the amplitude of the volt-seconds across L_r during $[t_0, t_2]$ will become smaller than that during $[t_5, t_7]$, resulting in the variation of i_p during $[t_0, t_2]$ to be smaller than that during $[t_5, t_7]$. Hence, the negative dc bias of i_p is generated. Similarly, the negative dc bias of i_p causes a negative voltage across the resistance r_p , which can compensate the loss of v_{Lr} during $[t_0, t_2]$ and reduce the decrement of the dc bias of i_p . However, the operating state of the secondary side is not affected. Hence, the final steady state under negative dc bias can be obtained. In addition, the similar analysis can be applied to the DAB converters employing MOSFETs.

IV. DERIVATION OF DC BIAS MAGNETIZING CURRENT

The derivation of dc bias magnetizing current depends on the type of selected switches, so this section is divided into two parts to introduce the calculation method for IGBTs and MOSFETs, respectively. Before the derivation, following assumptions are made to simplify the derivation.

- 1) The DAB converter is controlled with SPS strategy;
- 2) The capacitors C_1 and C_2 are large enough to keep V_1 and V_2 stable, which satisfies $V_1 = NV_2$;
- 3) The capacity of T_r is large enough to tolerate the magnetic flux density dc component B_{dc} and its magnetizing inductance keeps constant.

A. IGBTs Applications

Considering the forward voltages across the switches and primary/secondary winding resistances of the transformer, the voltage across L_m can be calculated with (1). When inconsistency occurs, v_{Lm} will deviate from the expected value, causing unexpected variation of i_p and dc bias.

$$v_{Lm} = v_{AB} - r_p i_p - v_{dpl} - v_{Lr} \quad (1)$$

TABLE II
ON-STATE LIST OF EACH SWITCH DURING A SWITCHING CYCLE

Item Time	IGBTs Applications				MOSFETs Applications			
	Mode _{PjI}	H-bridge 1	Mode _{SjI}	H-bridge 2	Mode _{PjM}	H-bridge 1	Mode _{SjM}	H-bridge 2
$t_0 \sim t_1^1$ $t_1 \sim t_2/t_2^1$	M _{P1I}	D ₁ /D ₄	M _{S1I}	D ₆ /D ₇	M _{P1M}	D ₁ /D ₄	M _{S1M}	Q ₆ /Q ₇
		D ₁ /D ₄		D ₆ /D ₇		Q ₁ /Q ₄		Q ₆ /Q ₇
$t_2/t_2^1 \sim t_3$ $t_3 \sim t_4$	M _{P2I}	Q ₁ /Q ₄	M _{S2I}	Q ₆ /Q ₇	M _{P2M}	Q ₁ /Q ₄	M _{S2M}	Q ₆ /Q ₇
		Q ₁ /Q ₄		D ₅ /D ₈		Q ₁ /Q ₄		D ₅ /D ₈
$t_4 \sim t_5$ $t_5 \sim t_6$	M _{P3I}	Q ₁ /Q ₄	M _{S3I}	D ₅ /D ₈	M _{P3M}	Q ₁ /Q ₄	M _{S3M}	Q ₅ /Q ₈
		D ₂ /D ₃		D ₅ /D ₈		D ₂ /D ₃		Q ₅ /Q ₈
$t_6 \sim t_7/t_7^1$ $t_7/t_7^1 \sim t_8$	M _{P4I}	D ₂ /D ₃	M _{S4I}	D ₅ /D ₈	M _{P4M}	Q ₂ /Q ₃	M _{S4M}	Q ₅ /Q ₈
		Q ₂ /Q ₃		Q ₅ /Q ₈		Q ₂ /Q ₃		Q ₅ /Q ₈
$t_8 \sim t_9$ $t_9 \sim t_{10}$	M _{P4I}	Q ₂ /Q ₃	M _{S1I}	D ₆ /D ₇	M _{P4M}	Q ₂ /Q ₃	M _{S1M}	D ₆ /D ₇
		Q ₂ /Q ₃		D ₆ /D ₇		Q ₂ /Q ₃		Q ₆ /Q ₇

To calculate the dc part of the primary current, periodic time integrals are made for (1), and (2) is obtained. The periodic time integral of v_{L_m} keeps at zero when the converter reaches steady state with certain dc bias, otherwise the average value of magnetizing current will continue to change. Similarly, the third item of the right side of (2) is also zero when the converter reaches steady state.

$$\int_0^T v_{L_m} dt = \int_0^T v_{AB} dt - \int_0^T (r_p i_p + v_{dpl}) dt - L_r \int_0^T \frac{di_p}{dt} dt \quad (2)$$

$$= \Delta \lambda_{ABI} - \int_0^T (r_p i_p + v_{dpl}) dt = 0,$$

where T is the switching cycle. $\Delta \lambda_{ABI}$ refers to the volt-seconds across points A and B in one switching cycle. As aforementioned, for IGBTs applications, the unmatched turn-on times has no influence on the volt-seconds $\Delta \lambda_{ABI}$, while the unmatched turn-off times will affect $\Delta \lambda_{ABI}$ directly. For example, when Q_2/Q_3 are early turned off, $\Delta \lambda_{ABI}$ will increase over zero, on the contrary, when the turn-off times of Q_2/Q_3 are delayed, $\Delta \lambda_{ABI}$ will fall below zero.

From Table II, one switching cycle contains four modes, so (3) can be obtained as

$$\Delta \lambda_{ABI} = \int_0^T (r_p i_p + v_{dpl}) dt$$

$$= \int_{t_0}^{t_2} v_{dp11} dt + \int_{t_2}^{t_5} v_{dp21} dt + \int_{t_5}^{t_7} v_{dp31} dt + \int_{t_7}^{t_{10}} v_{dp41} dt + r_p \int_0^T i_p dt,$$

$$= v_{dp11} \tau_{11} + v_{dp21} \tau_{21} + v_{dp31} \tau_{31} + v_{dp41} \tau_{41} + r_p \bar{I}_{dcp1} T, \quad (3)$$

where \bar{I}_{dcp1} is the average current of i_p , namely, the dc part of i_p . v_{dpl} ($j = 1, 2, 3, 4$) are shown as (4), in which v_{Qj} and v_{Dj} ($j = 1, 2, 3, 4$) refer to the voltage drops across the switch Q_j and the anti-paralleled diode D_j , respectively. τ_{jl} ($j = 1, 2, 3, 4$) are the time intervals of the respective modes M_{PjI} , which are shown as (5). Some approximate treatments are made here to simplify the derivation procedure, including neglecting the effect of r_p on the duration τ_{jl} of each mode and ignoring

the extra short mode introduced by the unmatched turn-off times.

$$\begin{cases} v_{dp11} = -v_{D1} - v_{D4} & v_{dp21} = v_{Q1} + v_{Q4} \\ v_{dp31} = v_{D2} + v_{D3} & v_{dp41} = -v_{Q2} - v_{Q3} \end{cases} \quad (4)$$

$$\begin{cases} \tau_{11} = t_\varphi / 2 - \bar{I}_{dcp1} L_r / (V_1 + NV_2) \\ \tau_{21} = (T - t_\varphi) / 2 + \bar{I}_{dcp1} L_r / (V_1 + NV_2) \\ \tau_{31} = t_\varphi / 2 + \bar{I}_{dcp1} L_r / (V_1 + NV_2) \\ \tau_{41} = (T - t_\varphi) / 2 - \bar{I}_{dcp1} L_r / (V_1 + NV_2) \end{cases} \quad (5)$$

Then, with (3), (4) and (5), one can be derived as (6).

$$\bar{I}_{dcp1} = \frac{\Delta \lambda_{ABI} - (v_{dp11} + v_{dp31}) \frac{t_\varphi}{2} - (v_{dp21} + v_{dp41}) \left(\frac{T}{2} - \frac{t_\varphi}{2} \right)}{r_p T - (v_{dp11} - v_{dp21} - v_{dp31} + v_{dp41}) L_r / (V_1 + NV_2)} \quad (6)$$

It should be emphasized that the amplitude of \bar{I}_{dcp1} cannot be too large, otherwise i_p will be larger or smaller than zero in the whole switching cycle, causing (4) and (5) to fail. Moreover, (3)–(6) work only when the current i_p is continuous. Hence, it is required that the time intervals of M_{P1I}/M_{P3I} and M_{S2I}/M_{S4I} must be larger than the dead time. And the boundary condition of (6) should be checked up after calculation.

Similarly, the dc part of i_s can be calculated with (7).

$$\bar{I}_{dcp1} = \frac{\Delta \lambda_{CDI} - (v_{ds11} + v_{ds31}) \left(\frac{T}{2} - \frac{t_\varphi}{2} \right) - (v_{ds21} + v_{ds41}) \frac{t_\varphi}{2}}{-r_s T - (v_{ds11} - v_{ds21} - v_{ds31} + v_{ds41}) L_r / (V_1 + NV_2)}, \quad (7)$$

where $\Delta \lambda_{CDI}$ refers to the volt-seconds across points C and D in one switching cycle. For instance, when Q_5/Q_8 are early turned off, $\Delta \lambda_{CDI}$ will reduce below zero. On the contrary, when the turn-off times of Q_5/Q_8 are delayed,

$\Delta\lambda_{\text{ABM}}$ will increase over zero. $v_{\text{ds}i}$ ($i = 1, 2, 3, 4$) are shown as (8), in which v_{Q_j} and v_{D_j} ($j = 5, 6, 7, 8$) refer to the voltage drops across the switch Q_j and the anti-parallel diode D_j , respectively.

$$\begin{cases} v_{\text{ds}11} = v_{D6} + v_{D7} & v_{\text{ds}21} = -v_{Q6} - v_{Q7} \\ v_{\text{ds}31} = -v_{D5} - v_{D8} & v_{\text{ds}41} = v_{Q5} + v_{Q8} \end{cases} \quad (8)$$

With (6) and (7), the magnetic flux density dc component B_{dc} can be calculated with

$$B_{\text{dc}1} = \frac{N^2 \mu_0 \mu_r A_e}{l_m} (\bar{I}_{\text{dcp}1} - \bar{I}_{\text{dcs}1} / N), \quad (9)$$

where μ_0 is the permeability of vacuum, and μ_r is the relative permeability, A_e is the effective cross-sectional area, and l_m is the length of flux path.

With (6), (7) and (9), it is found that both $\bar{I}_{\text{dcp}1}$ and $\bar{I}_{\text{dcs}1}$ are only affected by the factors on their respective sides, including volt-seconds, winding resistance of the transformer and the voltage drops across devices. But they collaborate to result in the dc bias of the transformer. For the methods which detect the transformer directly and produce reverse excitation to counteract the dc bias, the magnetic flux density dc component B_{dc} can be eliminated. However, $\bar{I}_{\text{dcp}1}$ and $\bar{I}_{\text{dcs}1}$ still exist, which can cause uneven conduction and switching loss among switches and further result in inconsistent aging degree of the semiconductor devices. This may aggravate the inconsistency among devices and increase the dc bias of both sides in turn. With these methods [11], [14]–[18], the position (primary or secondary side or both sides) where the dc bias occurs cannot be ascertained, making it hard to eliminate the possible dc bias of i_p and i_s . From this perspective, detecting the dc parts of i_p and i_s and regulating the duty cycles of switches at the side where dc bias occurs seems to be a better choice to avoid this potential ill effect.

B. MOSFETs Applications

For MOSFETs applications, (2) is still workable. Assuming that the on-state resistance of MOSFETs and voltage drops across body diodes are constant, (10) can be obtained according to Table II.

With (10), the reason why unmatched turn-on times only cause small dc bias in the MOSFETs applications (mentioned in Section III) can be easily obtained. When the turn-on time of switches are early or delayed, current

i_p can flow through the body diodes and the operating state keeps unchanged. For example, in Fig. 3, as long as the turn-on time of Q_1 is later than t_0 and earlier than t_2 , $\Delta\lambda_{\text{ABM}}$ will keep unchanged, because it has been mentioned in Section II that v_{AB} is only affected by the voltages V_1 and V_2 , the on/off states of Q_1 – Q_8 and D_1 – D_8 . However, due to the difference between the voltage drops of body diodes and the voltages across MOSFETs channel, the first item on the left side varies, which results in the dc bias of i_p . But this duration is too short, so the dc bias of i_p will be small.

$$\begin{aligned} \Delta\lambda_{\text{ABM}} &= \int_0^T (R_{\text{p}1\text{M}} i_p + v_{\text{dp}1\text{M}}) dt \\ &= \int_{t_0}^{t_1} v_{\text{dp}1\text{M}} dt + \int_{t_1}^{t_5} R_{\text{p}2\text{M}} i_p dt \\ &\quad + \int_{t_5}^{t_6} v_{\text{dp}3\text{M}} dt + \int_{t_6}^{t_{10}} R_{\text{p}4\text{M}} i_p dt + r_p \int_0^T i_p dt \quad (10) \\ &= v_{\text{dp}1\text{M}} t_d + R_{\text{p}2\text{M}} \int_{t_1}^{t_5} i_p dt + v_{\text{dp}3\text{M}} t_d \\ &\quad + R_{\text{p}4\text{M}} \int_{t_6}^{t_{10}} i_p dt + r_p \bar{I}_{\text{dcpM}} T \end{aligned}$$

One switching cycle contains four modes according to the on-state devices, and the expressions of $v_{\text{dp}1\text{M}}$, $R_{\text{p}2\text{M}}$, $v_{\text{dp}3\text{M}}$ and $R_{\text{p}4\text{M}}$ are shown as (11).

$$\begin{cases} v_{\text{dp}1\text{M}} = -v_{D1} - v_{D4} & R_{\text{p}2\text{M}} = R_{Q1} + R_{Q4} \\ v_{\text{dp}3\text{M}} = v_{D2} + v_{D3} & R_{\text{p}4\text{M}} = R_{Q2} + R_{Q3} \end{cases} \quad (11)$$

By neglecting the variation of i_p during $[t_3, t_5]$ and $[t_8, t_{10}]$ and ignoring the extra short modes introduced by the unmatched turn-off times, the integrals of i_p during $[t_1, t_5]$ and $[t_6, t_{10}]$ can be calculated as (12).

$$\begin{cases} \int_{t_1}^{t_5} i_p dt = \bar{I}_{\text{dcpM}} \left(\frac{T}{2} - t_d \right) + \frac{kTt_\varphi}{4} + \frac{kt_\varphi t_d}{2} - \frac{k}{2} t_\varphi^2 - \frac{k}{2} t_d^2 \\ \int_{t_6}^{t_{10}} i_p dt = \bar{I}_{\text{dcpM}} \left(\frac{T}{2} - t_d \right) - \frac{kTt_\varphi}{4} - \frac{kt_\varphi t_d}{2} + \frac{k}{2} t_\varphi^2 + \frac{k}{2} t_d^2 \end{cases} \quad (12)$$

where k is the rate of rise of i_p during $[t_0, t_4]$, namely, $(V_1 + NV_2)/L_r$.

Therefore, \bar{I}_{dcpM} can be calculated as (13). Similarly, \bar{I}_{dcsM} can also be obtained as (14), with the expressions of $R_{\text{s}1\text{M}}$, $v_{\text{ds}2\text{M}}$, $R_{\text{s}3\text{M}}$ and $v_{\text{ds}4\text{M}}$ shown as (15).

$$\bar{I}_{\text{dcpM}} = \frac{\Delta\lambda_{\text{ABM}} - (v_{\text{dp}1\text{M}} + v_{\text{dp}3\text{M}})t_d - (R_{\text{p}2\text{M}} - R_{\text{p}4\text{M}})(Tt_\varphi + 2t_\varphi t_d - 2t_\varphi^2 - 2t_d^2)(V_1 + NV_2)/(4L_r)}{r_p T + (R_{\text{p}2\text{M}} + R_{\text{p}4\text{M}})(T/2 - t_d)} \quad (13)$$

$$\bar{I}_{\text{dcsM}} = \frac{\lambda_{\text{CDM}} - (v_{\text{ds}2\text{M}} + v_{\text{ds}4\text{M}})t_d - (R_{\text{s}1\text{M}} - R_{\text{s}3\text{M}})(Tt_\varphi + 2t_\varphi t_d - 2t_\varphi^2 - 2t_d^2)(V_1 + NV_2)/(4L_r)}{-r_s T - (R_{\text{s}1\text{M}} + R_{\text{s}3\text{M}})(T/2 - t_d)} \quad (14)$$

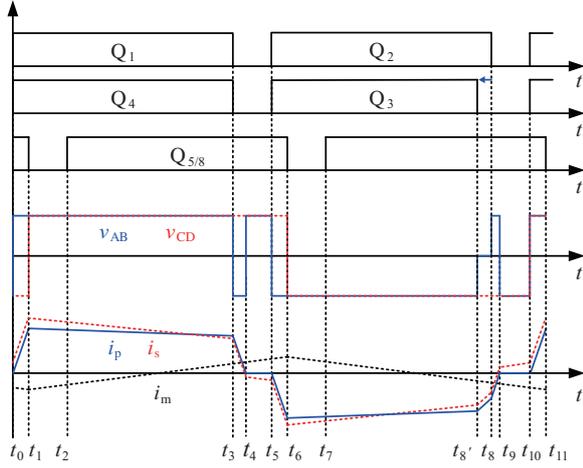


Fig. 5. The waveforms of the DAB converter when Q_3 is early turned off and i_p is discontinuous.

$$\begin{cases} R_{s1M} = R_{Q6} + R_{Q7} & v_{ds2M} = -v_{D5} - v_{D8} \\ R_{s3M} = R_{Q5} + R_{Q8} & v_{ds4M} = v_{D6} + v_{D7} \end{cases} \quad (15)$$

Then, similar to (9), the dc magnetizing current can be calculated with (13) and (14). Similar to the IGBTs applications, the dc magnetizing current is caused by the dc bias on both primary and secondary sides, and the dc bias on primary and secondary sides has no effect on each other. Hence, it is also recommended that dc bias currents \bar{I}_{dcPM} and \bar{I}_{dcSM} should be treated separately.

C. Analysis for Discontinuous Current Mode (DCM)

The aforementioned analysis of dc bias magnetizing current is based on the condition that i_p and i_s are continuous, while for the discontinuous current mode (DCM) some conclusions changes. As shown in Fig. 5, when the power is transferred from V_1 to V_2 , the phase-shift angle is too small to keep i_p continuous. But due to the magnetizing current i_m , i_s can be kept continuous. When Q_3 is early turned off, an extra operating mode will be introduced, and the volt-seconds $\Delta\lambda_{AB}$ can be calculated as (16).

$$\begin{aligned} \lambda_{AB} &= \int_{t_0}^{t_5} v_{AB} dt + \int_{t_5}^{t_{10}} v_{AB} dt \\ &= V_1 \left(\frac{T}{2} - \frac{2i_p(t_3)L_r}{V_1 + NV_2} \right) \\ &\quad - V_1 \left(\frac{T}{2} - t_d - \frac{2L_r}{-V_1 - NV_2} \left(i_p(t'_8) - \frac{NV_2}{L_r} t_d \right) \right) \quad (16) \\ &= V_1 \frac{2(-i_p(t'_8) - i_p(t_3))L_r}{V_1 + NV_2} \end{aligned}$$

For that the current i_p keeps almost unchanged during the durations $[t_1, t_3]$ and $[t_6, t_8]$, $i_p(t_3)$ is considered to be very close to $-i_p(t'_8)$ and $\Delta\lambda_{AB}$ is very close to zero. Hence, the dc bias will be very tiny in this situation. However, since

that i_s is still continuous, unmatched turn-off time of the switches still causes obvious dc bias. Although the shape of i_s varies, the dc bias current can still be predicted with (6), (7), (13) and (14) since that the time intervals of $[t_4, t_5]$ and $[t_9, t_{10}]$ are very short. Similarly, the inconsistency of devices at the primary side just results in very small dc bias, while the inconsistency of devices at the secondary side can cause large dc bias, which can be predicted with (6), (7), (13) and (14). Furthermore, when the phase-shift time is smaller than the dead zone, the transmission power will be zero if $V_1 = NV_2$, and no dc bias will be generated.

The aforementioned analysis can be generalized as follow:

- 1) When the phase shift angle is small, the winding current of leading bridge will be discontinuous, while the winding current on lagging side keeps being continuous due to the magnetizing current;
- 2) Unmatched turn-on and turn-off time and inconsistency of devices in leading bridge only result in very tiny dc bias, which can hardly be measured;
- 3) Unmatched turn-on and turn-off time and inconsistency of devices in lagging bridge results in obvious dc bias, which can be calculated with (6), (7), (13) and (14);
- 4) When the phase-shift time reduces smaller than dead zone, no dc bias will be generated if $V_1 = NV_2$.

D. Analysis for $V_1 \neq NV_2$

Considering the situation $V_1 \neq NV_2$, i_p and i_s will vary obviously during the time intervals $[t_1, t_3]$ and $[t_6, t_8]$. But as long as the difference between V_1 and NV_2 is not very large, (6), (7), (13) and (14) still work. But if V_1 and NV_2 mismatch seriously, i_p and i_s will cross zero during $[t_1, t_3]$ and $[t_6, t_8]$, and operating stage will change, so that the prediction accuracy of dc bias will decrease. Additionally, when $V_1 \neq NV_2$, the transmission power is not zero even if the phase-shift time is smaller than the dead zone, so that the unmatched turn-on/off times and inconsistency of devices will still result in dc bias. However, for the operating states in such situation and normal situation are totally different, the accuracy of the aforementioned expressions will decrease a lot.

E. Generalization

With the aforementioned analysis, for the DAB converters, the dc components of primary and secondary current are only affected by the factors on their respective sides, and they collaborate to cause the dc part of magnetizing current. Hence, the aforementioned calculation methods can be generalized to the multi-active-bridge converter, which is shown in Fig. 6. With (2), similar derivation procedure can be applied to calculate integrals and the dc part \bar{I}_{dci} ($i = 1, 2, \dots, N$) of current through each winding can be obtained. Hence, by reflecting \bar{I}_{dci} to the 1# side uniformly, the dc magnetizing current can be expressed as the summation of the reflected dc current.

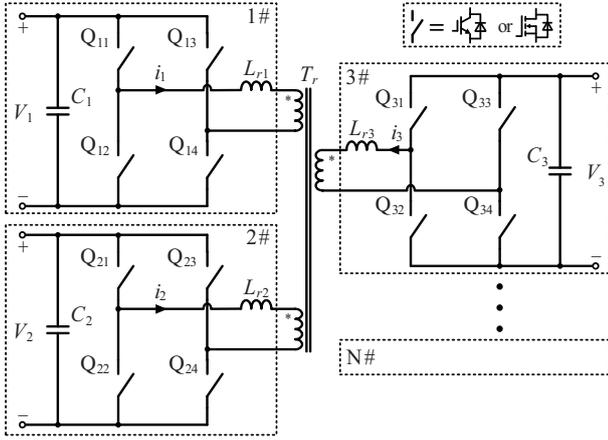


Fig. 6. The topology of multi-active-bridge converter.

V. THE PREDICTION METHOD OF THE DC BIAS

In order to obtain the maximum permitted inconsistency of devices and drivers, an example is taken here to introduce the detailed calculation procedure. The parameters are shown in Table III. Moreover, the maximum inconsistency of forward voltage or on-state resistance is set as $\pm 5\%$.

The maximum unmatched turn-on/off time is set as 10 ns. Hence, considering that only one switch on primary side turns off 10 ns earlier or later than the expected time, $\Delta\lambda_{AB}$ can reach the maximum value (7.5×10^{-6} Vs) or the minimum value (-7.5×10^{-6} Vs).

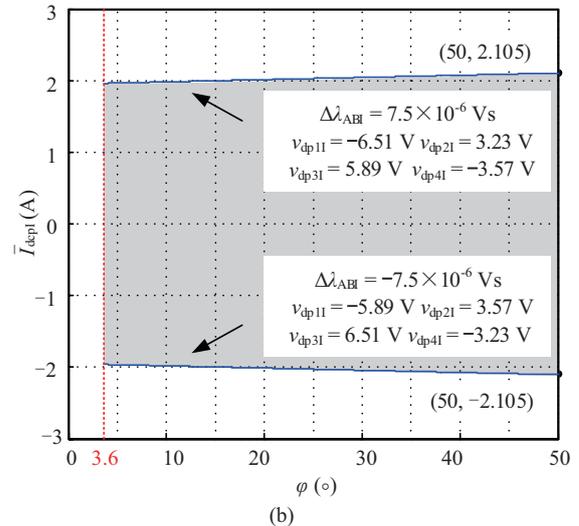
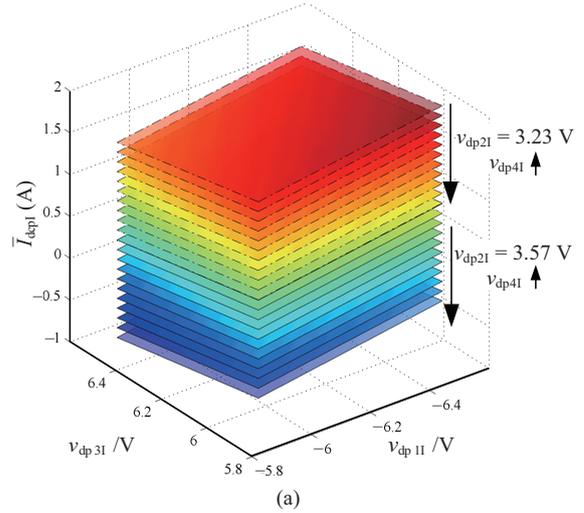
For IGBTs applications, if $\Delta\lambda_{AB1}$ is fixed at 7.5×10^{-6} Vs and ϕ is set as 50° , the curves of \bar{I}_{dcp1} versus $v_{dp11} \sim v_{dp41}$ are shown in Fig. 7(a), in which each layer of curve represents a set of v_{dp21} and v_{dp41} . The curves surrounded by dash dot lines and solid lines represent the data with v_{dp21} fixed at 3.23 V and 3.57 V, respectively. It can be noted that \bar{I}_{dcp1} increases with the decrease of $v_{dp11} \sim v_{dp41}$. The range of \bar{I}_{dcp1} versus the phase-shift angle ϕ is shown in Fig. 7(b). As aforementioned, if $V_1 = NV_2$, the dc bias will decrease to zero when the phase-shift time is shorter than the dead time. The dead time is set as $1\mu s$, so that when ϕ is smaller than 3.6° , the dc bias will be zero. And noticeably, the situation that V_1 and V_2 mismatch is not considered here. The range of \bar{I}_{dcp1} is given as the gray area, which is slightly broadened with the increase of ϕ . When ϕ increases to 50° , the maximum and minimum values can reach 2.105 A and -2.105 A, with the maximum inconsistency limited within $\pm 5\%$.

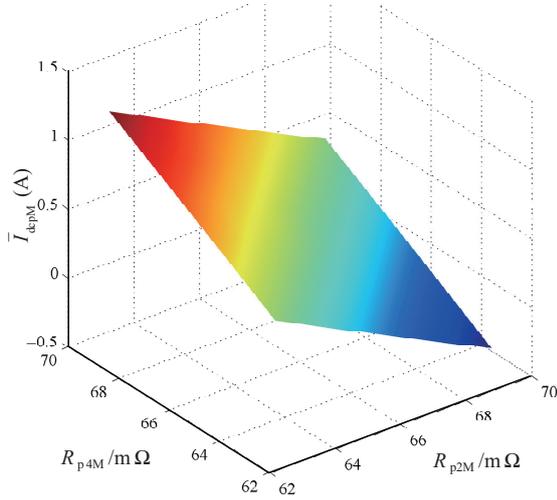
For MOSFETs applications, the curves of \bar{I}_{dcpM} versus R_{p2M} and R_{p4M} is shown in Fig. 8(a). Because the time intervals of modes M_{p1M} and M_{p3M} are very short, v_{dp1M} and v_{dp3M} have little effect on \bar{I}_{dcpM} . Hence, they are fixed at 6.6 V here to simplify the analysis. In Fig. 8(a), \bar{I}_{dcpM} increases with the decrease of R_{p2M} and increase of R_{p4M} . And \bar{I}_{dcpM} increases along with ϕ according to Fig. 8(b). The maximum and minimum values can reach 1.269 A and -1.269 A with ϕ increasing to 50° .

It can be found that the rate of rise of the maximum value of \bar{I}_{dcp1} is smaller than \bar{I}_{dcpM} . For the DAB converters employing MOSFETs, the differences between the on-

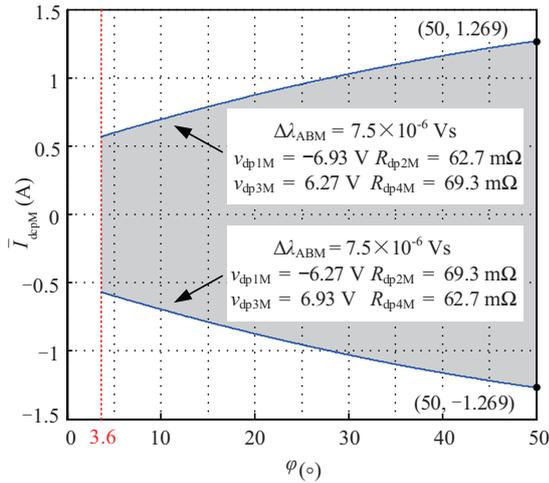
TABLE III
MAIN PARAMETERS OF DAB CONVERTER

	IGBTs Applications	MOSFETs Applications
Input voltage V_1	750 V	
Output voltage V_2	750 V	
Switching cycle T	100 μs	
Phase-shift angle ϕ	50°	
Dead time t_d	1 μs	
Leakage inductor L_r	200 μH	
Magnetizing inductance L_m	20 mH	
Turns ratio of T_r	1:1	
Winding resistance r_p/r_s	100 m Ω	
Device type	IHW25N120R2	L227F18Y
Device parameters	forward voltage (1.7 V)	ON resistance (33 m Ω)
	Diode forward voltage drop (3.1 V)	Diode forward voltage drop (3.3 V)

Fig. 7. The curves of \bar{I}_{dcp1} . (a) Versus $v_{dp11} \sim v_{dp41}$. (b) Versus phase-shift angle ϕ .



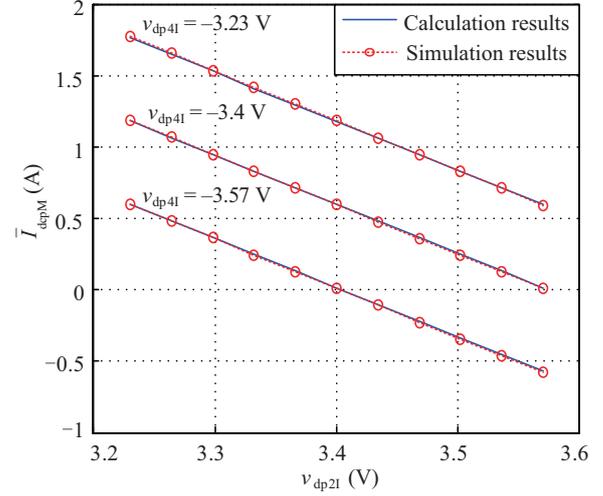
(a)



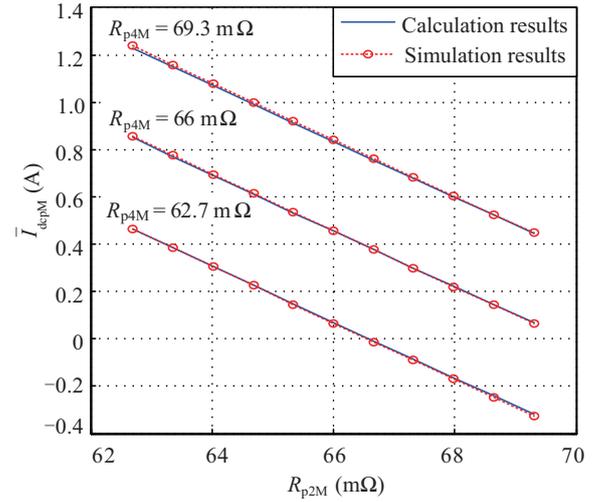
(b)

Fig. 8. The curves of \bar{I}_{dcpM} . (a) Versus R_{dp1M} and R_{dp4M} . (b) Versus phase-shift angle ϕ .

state resistance of MOSFETs are confirmed once the type and maximum inconsistency of MOSFETs are given. With the increase of phase shift-angle ϕ , the maximum value of i_p increases, which causes differences between the voltages across inconsistent MOSFETs to be magnified. Hence, the maximum of \bar{I}_{dcpM} increases rapidly. From another perspective, the item of numerator in (13), namely, $-2t_\phi^2 + t_\phi(T+t_d) - 2t_d^2$ is positive and is proportional to the square of t_ϕ . When R_{p2M} is smaller than R_{p4M} , the third item of numerator in (13) is proportional to the square of t_ϕ , while the denominator keeps unchanged, resulting in the quadratic increase of the maximum of \bar{I}_{dcpM} . However, for the DAB converters with IGBTs, the forward voltages of IGBTs and voltage drops of anti-parallel diodes are assumed to be constant. Once the type of IGBTs is selected, the differences between the voltage across switches are determined, which do not vary with the increase of ϕ . Hence, according to (6), it can be found that the maximum of \bar{I}_{dcpM} increases linearly



(a)



(b)

Fig. 9. The comparison between simulation and calculation results for (a) IGBTs applications. (b) MOSFETs applications.

along with ϕ . Actually, the rate of rise of the maximum value of \bar{I}_{dcpM} and \bar{I}_{dcpL} depends on the parameters of semiconductor switches and the given maximum inconsistency.

For some approximate treatments are made to simplify the derivation, the PLECS software is employed to verify the aforementioned results. For IGBTs applications, the error between simulation and calculation results is always smaller than 0.02 A with the given conditions, which is shown in Fig. 9(a). For MOSFETs applications, the comparison between simulation and calculation results is shown in Fig. 9(b), in which the error keeps being smaller than 0.02A. Hence, it can be concluded that the accuracy of aforementioned equations can be guaranteed.

VI. EXPERIMENTAL ANALYSIS

In order to verify the aforementioned analysis, an experimental prototype was built with the parameters given in Table IV.

TABLE IV
EXPERIMENTAL PARAMETERS

	IGBTs Applications	MOSFETs Applications
Input voltage V_1	50 V	
Output voltage V_2	50 V	
Switching cycle T	100 μ s	
Phase-shift angle ϕ	36°	
Dead time t_d	1 μ s	
Leakage inductor L_r	206.4 μ H	
Magnetizing inductance L_m	19.64 mH	
Turns ratio of T_r	1:1	
Winding resistance r_p/r_s	60 m Ω	
Device type	IKW30N60T	IXFX 55N50
Device parameters	forward voltage (1.5 V)	ON resistance (80 m Ω)
	diode forward voltage drop (1.65 V)	diode forward voltage drop (1.5 V)

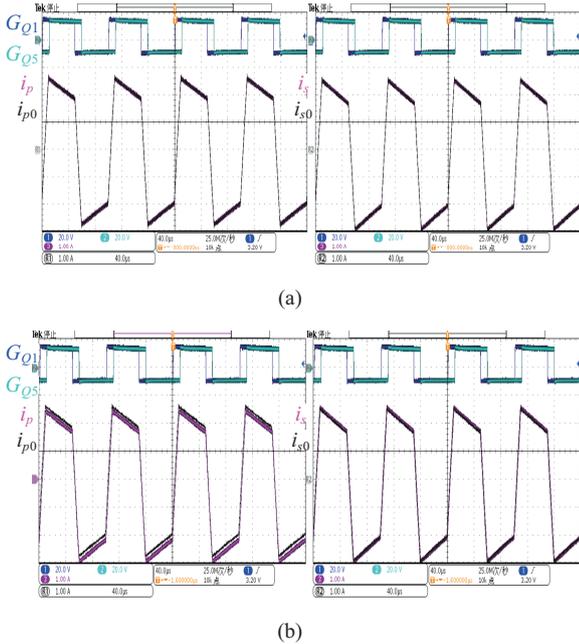


Fig. 10. The main waveforms of the DAB converters employing IGBTs. (a) Unmatched turn-on times. (b) Unmatched turn-off times.

The experimental results are shown in Figs. 10–12.

The waveforms of the DAB converter with IGBTs are given in Fig. 10. When the turn-on and turn-off times of Q_1 are not early or delayed, the currents through the primary and secondary windings of the transformer are shown as i_{p0} and i_{s0} , respectively. When Q_1 is turned on 500 ns later than the expected time as shown in Fig. 10(a), the primary and secondary currents are shown as i_p and i_s , which keep unchanged comparing to i_{p0} and i_{s0} . However, when Q_1 is set to be turned off 150 ns earlier than the expected time as shown in Fig. 10(b), the dc part of i_p decreases obviously while i_s keeps unchanged, which agrees with the aforementioned analysis.

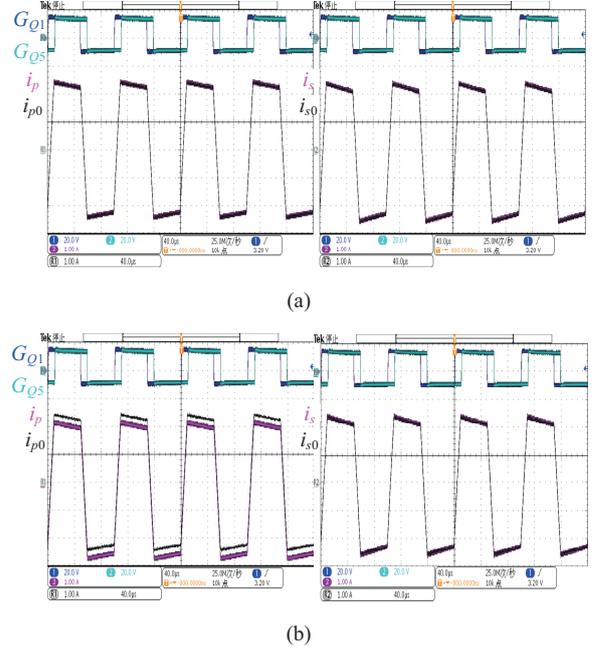


Fig. 11. The main waveforms of the DAB converters employing MOSFETs. (a) unmatched turn-on times. (b) unmatched turn-off times.

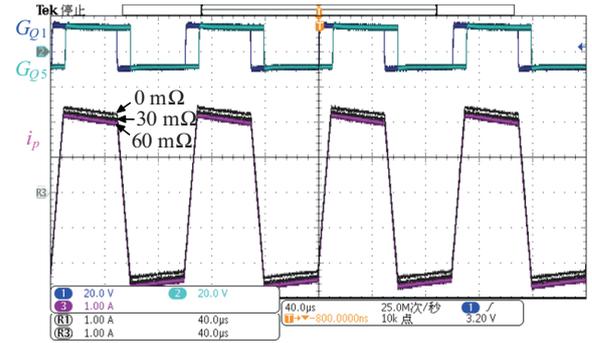


Fig. 12. The main waveforms of the DAB converters employing MOSFETs with different R_{p2M} .

The waveforms of the DAB converter with MOSFETs are shown in Fig. 11. Similarly, i_{p0} and i_{s0} refer to the original currents through the primary and secondary windings, respectively. When Q_1 is turned on 500ns later than the expected time as shown in Fig. 11(a), the primary and secondary currents are shown as i_p and i_s . The dc bias in i_p is affected slightly and the dc bias in i_s keeps unchanged. As mentioned in Section III, even though the turn-on time of Q_1 is delayed, i_p can still flow through its body diode during this mode. Hence, the only difference introduced by the unmatched turn-on time of Q_1 is the change of the voltage across Q_1 in this duration. Also because this duration is too short, the effect on the dc part of i_p is hardly observed. When Q_1 is turned off 150 ns earlier than the expected time, the dc part of i_p decreases obviously comparing to the initial situation, which is shown as Fig. 11(b). However, the dc part of i_s keeps unchanged for no change is put the secondary side. It can also be noted that there is an initial dc bias in the

converter due to the inconsistency of devices.

In order to verify the relation between \bar{I}_{dcpM} and R_{p2M} , a small resistor is connected in series with Q_1 . By changing the resistance from 0 to 30 m Ω , and 60 m Ω , it can be noted that the dc part of i_p reduces gradually as in Fig. 12. As the duration of M_{p1M} is so short that the effect of the extra resistor on v_{dp1M} can be neglected, it can be concluded that \bar{I}_{dcpM} decreases with the increase of R_{p2M} , which agrees with Fig. 8(a).

VII. CONCLUSION

In this paper, dc bias in the DAB converters with SPS control has been analyzed, and one prediction method of dc bias magnetizing current is proposed considering the inconsistency of switches and driving circuits, which can also be generalized to the multi-active-bridge converters. Some conclusions can be made here:

- 1) For IGBTs applications, unmatched turn-on times has no effect on the dc bias, while unmatched turn-off times will cause an obvious dc bias;
- 2) For MOSFETs applications, unmatched turn-on times has a very slight influence on the dc bias, while unmatched turn-off can introduce an obvious dc bias;
- 3) Unbalanced factors can only affect the dc bias current on the respective side, while they collaborate to create a dc flux density component in the transformer core.

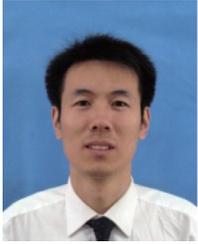
With the prediction method, if the maximum permitted dc bias of the transformer is given, the range of the inconsistency of semiconductor switches and driver signals can be obtained, which is helpful for the selection of semiconductor devices and the design of the transformer. Hence, extra flux measurement and balancing methods can also be avoided.

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