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System Realization of CASHIPS DC High Power Test Facility

Xiaojiao Chen, Liansheng Huang, Peng Fu, Ge Gao, Zhiquan Song, Liuwei Xu, Shiying He, and Xiuqing Zhang

***Abstract*—Aims to complete the test of the International Thermonuclear Experimental Reactor (ITER) poloidal field (PF) converter system, and to meet future continuous upgrading needs of a modern industrial power system and scientific research, direct current (DC) high-power test facility of Hefei Institutes from Physics science, Chinese Academy of Sciences (CASHIPS) is built in 2011. As the largest DC high-power test facility in China, the rated steady state DC current is 120 kA and the pulse peak current is 500 kA. Four thyristor-based AC/DC converter modules are paralleled to handle this huge current. In May 2017, 15 testing items are accredited by the China National Accreditation Service (CNAS) for Conformity Assessment . Up to now, the test for 17 devices of 16 companies and manufacturers in the world have been completed. In this paper, the topology and the control of DC High-Power test facility are presented. In addition, the testing capability and the completed tests of DC high-power test facility are illustrated.**

***Index Terms*—120 kA steady state DC current, 500 kA pulse peak current, DC high-power test facility.**

I. Introduction

With the development of modern industrial power systems, scientific research, the capacity of the high-power electrical equipment test facility is expanded and upgraded continuously to satisfy the needs of economic and social development. At present, there are more than 10 well-known power labs with DC high-power test facility all over the world. Most of the leading electric companies have their own high-power labs, in addition to some independent high-power laboratory. According to the investigation, the biggest DC testing voltage is 7 kV and the largest DC testing current is up to 320 kA before 2011 [1].

International Thermonuclear Experimental Reactor (ITER) is an international collaboration project located in south France to demonstrate the scientific and technological feasibility of fusion energy for peaceful purposes [2], [3]. The ITER poloidal field (PF) AC/DC converter system mainly provides the controlled current thereby implementing the plasma shape and position control, which is one of the key systems for ITER [4], [5]. The ITER PF AC/DC converter Procurement Arrangement (PA) was signed between China Domestic Agency (DA) and ITER Organization (IO) in April 2011. The Institute of Plasma Physics, Chinese Academy of Science (ASIPP) takes the responsibility of ITER PF AC/DC converter PA. The PF AC/DC converter system is a major AC/DC converter system, and the total installation power is 1.2 GVA. The ITER PF AC/DC converter system required DC short-circuit impulse test current is 400 kA and the DC steady state testing current is up to 100 kA for type test [6]. Hence, the existing test facilities cannot satisfy the test requirements of the ITER PF AC/DC converter system.

Considering the testing requirements of ITER PF AC/DC converter system components and continuous upgrading capacity of high-power test capability, the steady-state current of DC high-power test facility is rated at 120 kA and the pulse current is 500 kA. 120 kA steady-state current make it the largest steady state DC current test facility in China until now. The DC high-power test facility of Hefei Institutes of Physics science, Chinese Academy of Sciences (CASHIPS) is a professional test facility. 15 testing items are accredited by the China National Accreditation Service (CNAS) for Conformity Assessment in May 2017. The relevant reports are accredited by 35 countries including France, Germany, Italy, United Kingdom, United States, etc.

Designed and constructed by ASIPP, co-phase counter parallel connection topology structure is selected on account of the low voltage and the high current of DC high power test facility. In this paper, the characters, parameters and operation modes of DC high power test facility are presented. In addition, the configuration of the control system, hardware and software of the local controller is illustrated in detail. Moreover, the relevant qualification experiments including the testing capability and some completed tests are also provided. The paper is organized as follows. The topology and the control of DC high-power test facility is presented in Section II and Section III respectively. The qualification experiments are performed in Section IV. In this part, the experiment of 120 kA rated steady state DC current and 500 kA pulse current is carried out to demonstrate the testing capabilities. Moreover, some typically completed tests are also provided in this part. At last, the conclusion is drawn in Section V.

II. Topology of the DC High-Power Test Facility

A. Topology Structure

Four AC/DC converter modules are paralleled to handle

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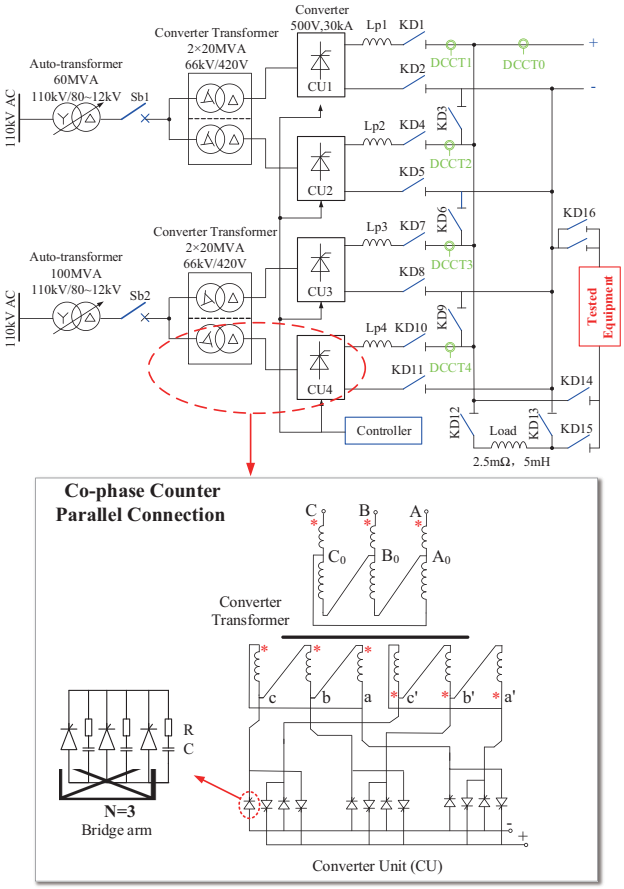

Fig. 1. DC high-power test facility scheme.

120 kA steady-state DC current and 500 kA pulse current. 30 kA rated steady-state DC current and 0.5 kV rated DC voltage of each converter module make the co-phase counter parallel connection topology structure the suitable choice for DC high power test facility as Fig. 1. Co-phase counter parallel connection topology structure not only reduces the current carrying load of transformer individual windings, but also reduces the eddy power loss and heat generation of the transformer because the adjacent two-phase windings currents are reversed. In addition, the magnetic flux density in the converter cabinet is near to zero, which improve the operating environment of the semiconductor component [7].

IGBT, IGCT and other semiconductor is wildly studied and used in high power electronic field [8], [9], [10]. However, with the outstanding advantages that heavy current, high voltage, relatively small heat dissipation density and low cost, the thyristor-based AC/DC converter module is chosen and each bridge arm is paralleled with 3 thyristors and RC snubber circuit. The type of thyristor is ABB 5STP 50Q1800.

As shown in Fig. 1, the DC high-power test facility is composed by 110/66 kV 100 MVA and 115/66 kV 60 MVA autotransformers, four 20 MVA converter transformers, four 30 kA/0.5 kV converters, four DC reactors (50 uH), load (2.5 mΩ, 5 mH) and sixteen DC disconnectors. Each

Fig. 2. DC high-power test facility.

TABLE I
OPERATION MODES

Operation Mode	Operation Converter Module	Parameter
Single converter operating	CU1 / CU2 / CU3 / CU4	30 kA, 0.5 kV
Two converters in parallel	CU1&CU2 / CU3&CU4	60 kA, 0.5 kV
Four converters in parallel	CU1&CU2&CU3&CU4	120 kA, 0.5 kV
Two converters in series	CU1&CU2 / CU3&CU4	30 kA, 1.0 kV
Four converters in series	CU1&CU2&CU3&CU4	30 kA, 2.0 kV

thyristor-based AC/DC converter module is connected to a converter transformer. The converter transformers are phase shifting to each other in order to implement the 24 pulses output in DC terminal thereby eliminating harmonics at specific frequencies on the AC side and reducing current ripple in DC side. The DC high-power test facility scheme and parameters are shown as Fig. 1 [11]. CU1−CU4 are the four AC/DC converter modules, KD1−KD16 are the DC disconnectors, Lp1−Lp4 are the DC reactors, DCCT0−DCCT4 are the current sensors [12]. The DC high-power test facility is shown as Fig. 2.

B. Operation Modes

The converters can operate in different operation modes to satisfy the different test requirements. As shown in Table I, the operating modes include single converter operating mode, converters in parallel operating mode, and converters in series operating mode. DC disconnector array is designed to change the circuit connection to implement multiple operating modes according to the different test requirements. The autotransformers are set in different position according to the required maximum voltage and

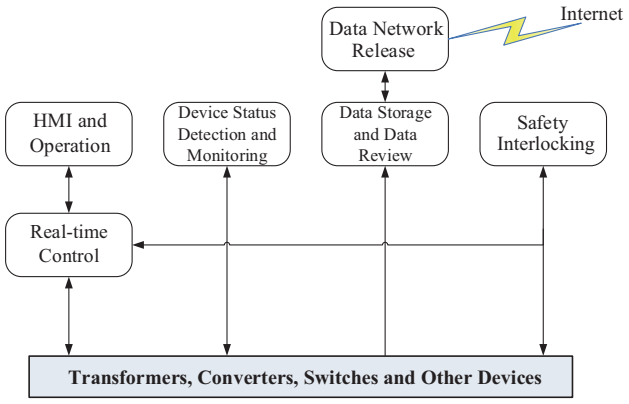

Fig. 3. The structure of the control system.

current ripple, and which is helpful to reduce the current ripple in some case.

III. The Control System of DC High-Power Test Facility

A. The Configuration of Control System

The test facility control system is divided into the following different parts according to the functions: human machine interface (HMI) and operation, real-time control, device status detection and monitoring, data storage and data review, data network release, and interlock. The structure of the control system is shown in Fig. 3.

- HMI and operation: to set the operation parameters such as waveform preset, converter operation mode, converter control mode, and to operate the converter state machine.
- Real-time control: to complete voltage open-loop and current closed-loop control operation, and to change the operation mode in real time according to the rectifier operating parameters, and to act the interlock action.
- Device status detection and monitoring: to detect the status of transformers, rectifiers and switchgears periodically, and to monitor the status. And to act the remote operation of switches.
- Data storage and data review: to measure the circuit voltage, current of transformer and converters. To store the data and review the data.
- Safety interlock: to act the occupation safety function.

Each part of the control system is interconnected through the network. According to the different performance and function requirements, the control network is divided into two types: shared memory real-time network and Ethernet. Each network is independent, and all devices are in the same network layer to ensure data transmission efficiency. As the core controller of the DC high-power test facility, the real-time controller is also called the local controller.

B. The Local Controller

The local controller is based on Compact PCI computer [13],

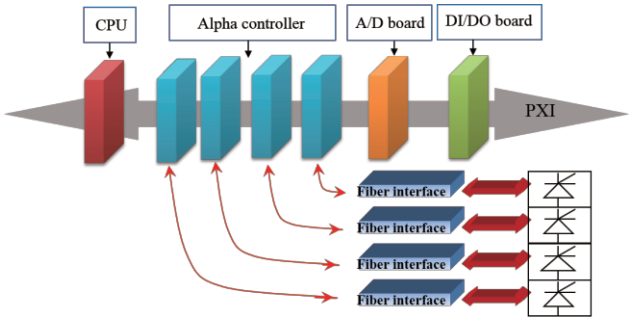

Fig. 4. The configuration of loacl controller.

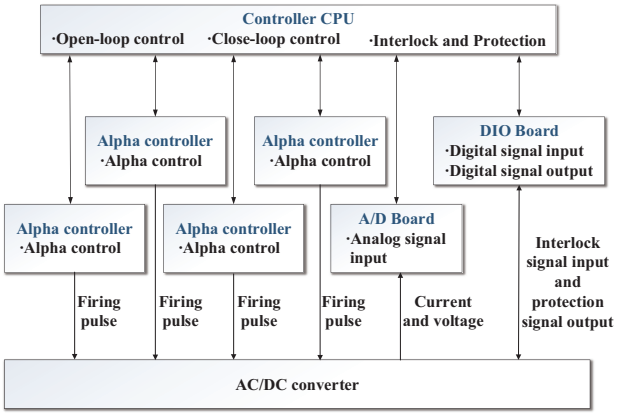

Fig. 5. The control block of local controller.

and the Compact PCI chassis is 12V18OPX98Y5VQ2X/ELMA; According to the real-time reference voltage, the trigger angle is calculated by CPU and the CPU board type is CP6005; Then, the converter bridge control and the trigger pulses generating is implemented by the alpha controller. Alpha controller outputs and modulates the trigger signal into a 15 kHz pulse to reduce the amplifier power and send the trigger pulse at the corresponding time to the thyristors by optical fiber, and the alpha controller type is CPCI-2008. Each converter module is controlled by an independent alpha controller. The configuration of the local controller is shown in Fig. 4. The AD board type is CPCI-9116 for analog signal input and the DIO board type is CPCI-7432 for digital signal input and output. The control block of local controller is shown in Fig. 5.

Fig. 6 shows the cubicle configuration of the local controller. The synchronization board is used to obtain the synchronization signal. The synchronization signal is delivered to the local controller to provide an accurate phase synchronization and frequency synchronization for the trigger time. The feedback signal and protection signal is collected by fast A/D.

IV. Testing Capability

A. 120 kA Steady State DC Current

The DC test facility is composed of four 30 kA/0.5 kV

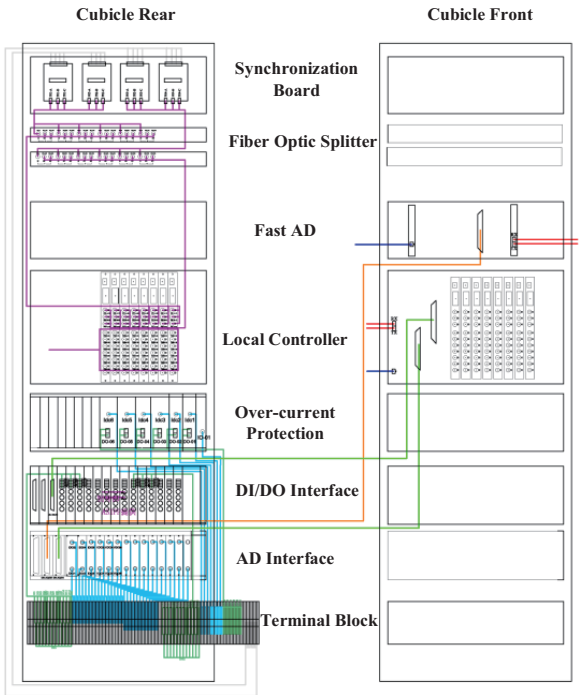

Fig. 6. The cubicle configuration of local controller.

converters. These converters could be operated in different modes to implement different required output. The output performance of different operation mode is shown in Table II.

When the four converter modules are in parallel, the steady state output current is rated to 120 kA. The huge DC continues current could be outputted to implement superconducting coil test, high temperature current lead test, DC disconnect test, etc. During steady state operation, the current closed loop control is adopted. The typical experiment results that rated current of 120 kA is shown as Fig. 7.

B. 500 kA Pulse Current

1) The Output Capability Calculation Based on System Parameters

Based on the analysis of the system parameters, the pulse current test capability of DC test platform is calculated. The equivalent circuit of four paralleled converter units is shown in Fig. 8. The U_{d0} is the no-load voltage of the converter; R_{S4} is the internal resistance of the four paralleled converter units; L_p is the inductance of DC reactor; L_d is the inductance of DC circuit; R_d is the DC resistance; R_1 is the resistance of the stainless steel resistor.

According to Fig. 8, the (1) can be obtained as:

$$\begin{cases} U_{d0} - R_{S4} i_d - \dfrac{L_p}{4} \times \dfrac{\mathrm{d}i_d}{\mathrm{d}t} = (R_d + R_1) i_d + L_d \dfrac{\mathrm{d}i_d}{\mathrm{d}t} \\ U_{d0} = 1.35 U_2 \cos\alpha \end{cases} \tag{1}$$

TABLE II
OPERATION PARAMETERS OF DC HIGH-POWER TEST FACILITY

Operation Mode	Parameter	Value	Ripple
Single converter operating	Rated DC voltage	500 V	-
	Rated DC current	30 kA	⩽1%
Two converters in parallel	Rated DC voltage	500 V	-
	Rated DC current	60 kA	⩽1%
Four converters in parallel	Rated DC voltage	500 V	-
	Rated DC current	120 kA	⩽1%
	Short pulse current	500 kA	-
Two converters in series	Rated DC voltage	1.0 kV	-
	Rated DC current	30 kA	-
Four converters in series	Rated DC voltage	2.0 kV	-
	Rated DC current	30 kA	-

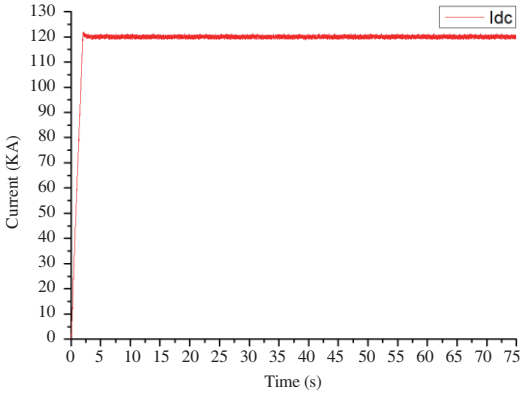

Fig. 7. The 120 kA steady state current profile (I_{dc} is the dc terminal current).

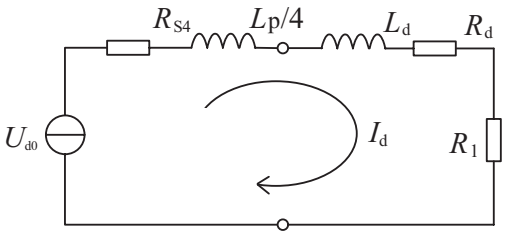

Fig. 8. The equivalent circuit of four paralleled converter units.

The U_2 is the secondary phase to phase voltage of the converter transformer. Then (1) can be equivalent to (2).

$$(R_{S4} + R_d + R_1) i_d + \left(L_d + \frac{L_p}{4}\right) \frac{\mathrm{d}i_d}{\mathrm{d}t} = 1.35 U_2 \cos\alpha \tag{2}$$

The I_d can be calculated:

$$I_d = \frac{1.35 U_2 \cos\alpha}{R_{S4} + R_d + R_1} \left(1 - e^{-t/\tau_4}\right) \tag{3}$$

$$\tau = \frac{L_d + L_p / 4}{R_d + R_1 + R_{S4}} \tag{4}$$

Different transformer tap position corresponds to the

TABLE III
OUTPUT CAPABILITY OF FOUR PARALLELED CONVERTER UNITS

	U_2 (V)	R_{S4} (mΩ)	R_{Σ} (mΩ)	τ (ms)	I_d^* (kA)
115/80	487	0.48	0.88	59.7	721.7
115/42	256	0.27	0.67	78.4	498.3
115/12	73	0.20	0.60	87.5	158.7

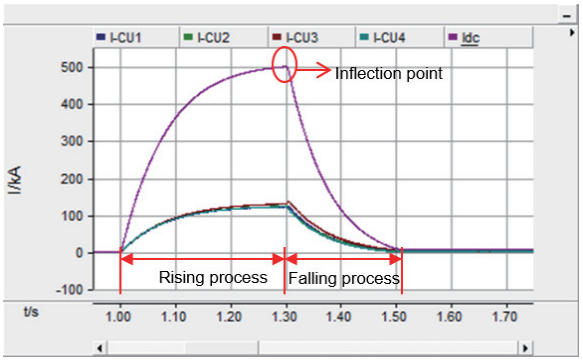

Fig. 9. The simulation of 500 kA peak pulse current output.

different parameters. The internal resistance of the four paralleled converter units R_{S4}, the total resistance R_{Σ}, the (3) and (4) can be obtained as Table III.

The calculated output capability of the DC current in Table III is not the experiment current that the converter can withstand. The experiment peak current and its pulse width is limited by the thyristor limiting load integral parameter, the thyristor internal silicon temperature, and should be with some safety margins.

2) The 500 kA Output Capability Experiment

For the pulse current operation, the whole process of the pulse can be divided into three stages, rising process, inflection point and falling process as Fig. 9. All of these three stages current control is required very fast dynamic response within milliseconds.

During the rising process, the converters work in the converter model. Because of the AC and DC loop impedance difference between each paralleled converter, the control purpose is not the same DC average voltage but the same current for each paralleled converter. During inflection point, it is, in fact, in a transient process, the converters should be changed from converter model to inverter model. Because of the phase shifting between each converter transformer, the DC voltage transient values of each converter is different, the DC output transient current is hard to be controlled. And any current overshoot could lead the converter failure because of the huge transient current. While during the falling process, the converters work in the inverter model. Because of the inherent characteristics commutation failure of thyristor-based converter when in inverter model, this process should be controlled carefully according to each converter DC current. And in this phase, the current sharing control is a very important task to make

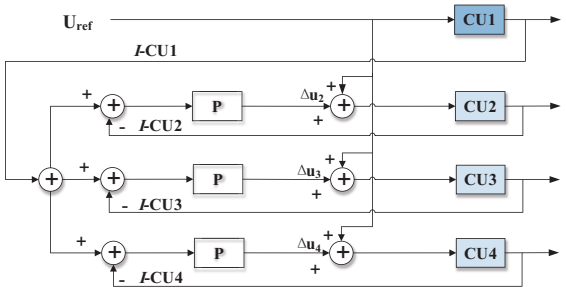

Fig. 10. Dynamic current sharing control strategy of 500 kA pulse current. (*I*-CU1: CU1 converter current; *I*-CU2: CU2 converter current; *I*-CU3: CU3 converter current; *I*-CU4: CU4 converter current; I_{dc}: the dc terminal current).

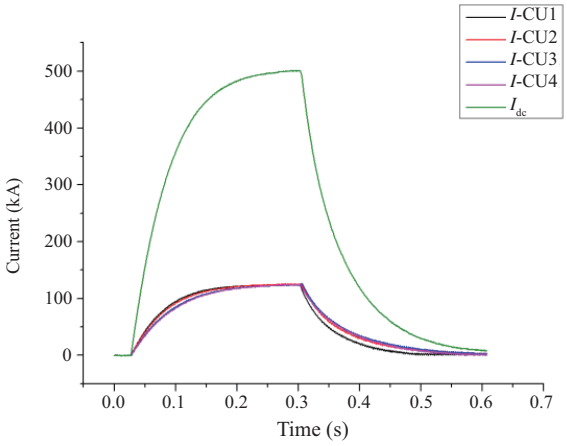

Fig. 11. The 500 kA Peak Pulse Current Profile (*I*-CU1: CU1 converter current; *I*-CU2: CU2 converter current; *I*-CU3: CU3 converter current; *I*-CU4: CU4 converter current; I_{dc} is the dc terminal current).

sure the system safe.

As the key technology of DC high power test facility, the dynamic current sharing control strategy of 500 kA pulse current is shown as Fig. 10.

The proportional control with the incremental control algorithm is adopted to ensure the dynamic characteristics and the system stability [14], [15]. U_{ref} is the control reference voltage. The *P* controller parameters are designed carefully to ensure the short response time, and to avoid overshoot or shock in operation. $\Delta u1$, $\Delta u2$ and $\Delta u3$ are the incremental voltage.

With the characteristics that short pulse time, large output current and fast current rising, the voltage open loop and current closed loop are adopted for the pulse output operation. One of the paralleled converter CU1 is selected as the master module, and the other ones (CU2 to CU4) are treated as the slave modules, each slave module will perform current sharing adjustment according to the current of the master module *I*-CU1.

The experiment is carried out on DC high power test facility to verify the effectiveness and the feasibility of this control strategy. The 500 kA pulse peak current output is shown as Fig. 11. In pulse operation, the output peak current is 500 kA within 0.3 s, the profile is shown in Fig. 11. These

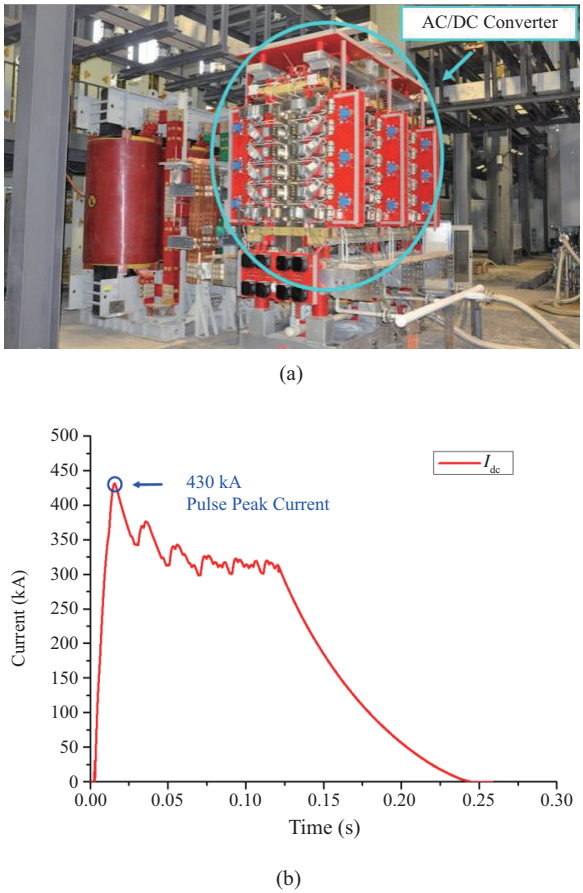

Fig. 12. AC/DC converter type test. (a) Test photo. (b) Test profile (I_{dc} is the dc terminal current).

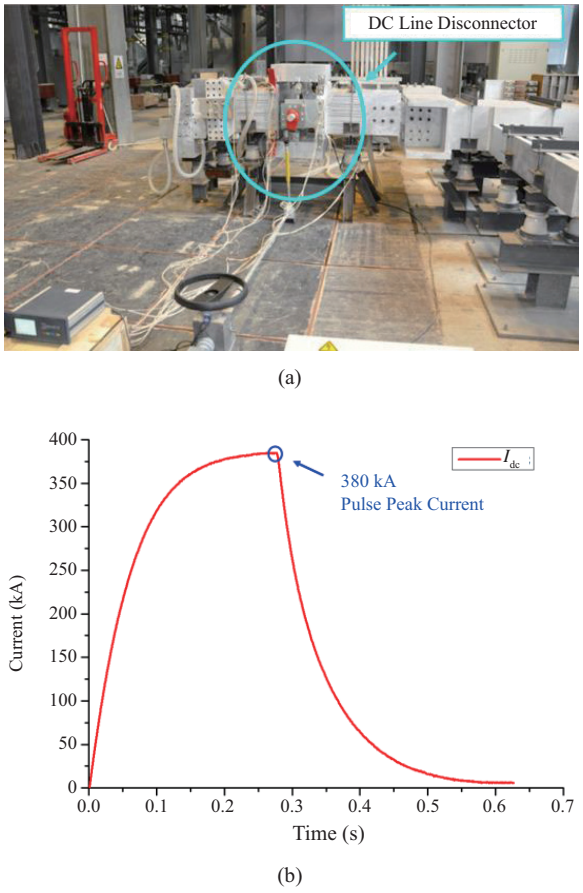

Fig. 13. DC Line Disconnector type test. (a) Test photo. (b) Test profile (I_{dc} is the dc terminal current).

performance could be used for DC high-power equipment type test.

C. The Completed Test

Until now, 17 devices type test of 16 companies and manufacturers have been done, including AC/DC converter type test, bypass the type test, DC reactor type test, feeder type test, DC line disconnector type test, and traction distribution DC switchgear type test, etc.

AC/DC converter is implemented the type test, in order to verify the converter structural strength in case of the converter reactor upstream short. The thyristors were all replaced by high power diodes in order to achieve the peak current without control. In this test, the converter bridge was subjected to 430 kA peak short current test. There is no deformation or damage to the structure, and the test results showed that the structural strength of the converter meets the design requirements. The test photo and the current profile is shown in Fig. 12.

DC line disconnector type test is realized in the pulse mode to verify mechanical stability and thermal stability under shock current conditions of 380 kA peak current. The DC line disconnector is not deformed or damaged, and the test results showed that the designed disconnector meets the design requirements. The test photo and the current profile is shown in Fig. 13.

DC busbar type test is realized in the steady state current mode to verify the thermal stability. The steady state current is 27.5 kA, the test continues until the bus temperature reaches equilibrium. The test results showed that design of the DC busbar meets the design requirements. The test photo and the current profile is shown in Fig. 14.

V. Conclusion

The DC high-power test facility is designed and constructed by ASIPP which aims to perform the test of ITER PF AC/DC converter system and meets the future continuous upgrading needs of the modern industrial power system and scientific research. Certified by CNAS in May 2017, 15 test reports are accepted by 35 countries in the world. The steady-state current of DC high-power test facility is rated at 120 kA. The pulse peak current is 500 kA. The DC high-power test facility is developed into a high-power electrical professional test facility, which is capable of the type test and routine test of the components in industry, rail traffic and electric power. In this paper, the topology and the control of the DC high-power test facility are presented. Then the performance results from the experiments of

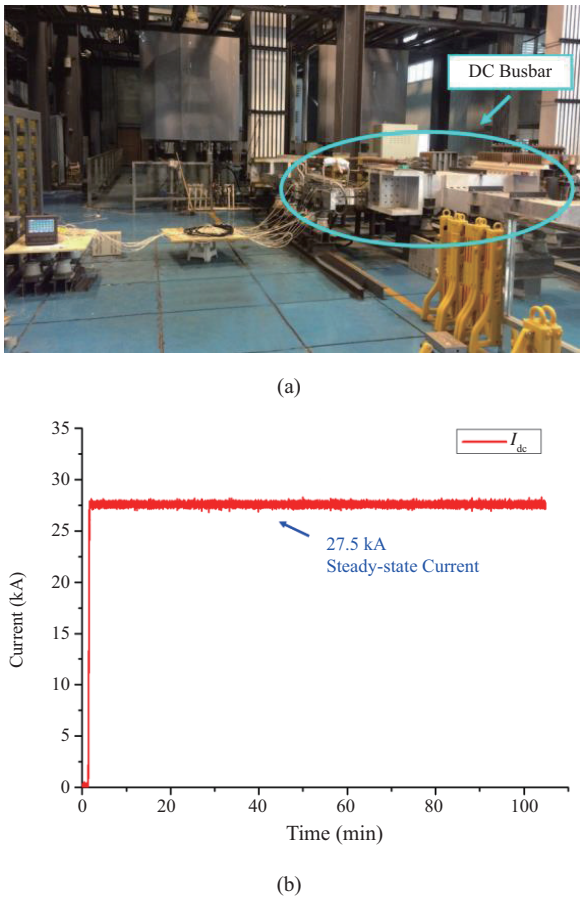

Fig. 14. DC Busbar type test. (a) Test photo. (b) Test profile (I_d is the dc busbar current).

its testing capability are reported. The experiment results illustrated that the testing capability that 120 kA steady-state continuous current and 500 kA pulse current of DC high-power test facility is qualified.

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A Modified Aalborg Inverter Extracting Maximum Power From One PV Array Source

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***Abstract*—Distributed Photovoltaic Generation (DPVG) systems have become more important in recent years because of energy pinch and air pollution. Grid-tied inverters, as the indispensable parts of the DPVG systems, have drawn a lot of research attentions. Among various constructors, the Aalborg inverter was proposed as a candidate for the interface between the PV arrays and the power grid for some potential advantages, such as the wide range of input DC voltages, high efficiency, low cost and no leakage current. For a conventional Aalborg inverter, however, in order to gain a symmetrical gird-injected current, when the input DC voltages generated by the PV arrays are not equal, part of the input DC energy has to be discarded, which will reduce the conversion efficiency of the whole system. In this paper, a modified Aalborg inverter with a single input DC source is proposed to extract the maximum DC energy of PV arrays. The operating principle is illustrated via equivalent circuits. The control strategy is designed to balance the capacitor voltages and smooth the grid-injected current. A 110 V/50 Hz/800 W prototype has been built to verify the validity of the proposed inverter together with the effectiveness of the control strategy.**

***Index Terms*—Aalborg inverter, Buck-Boost, maximum power piont tracking (MPPT), photovoltaic system, voltage balance.**

I. Introduction

With the development of global economy and the increase of population, environmental pollution and energy shortage are becoming increasingly serious. Distributed Photovoltaic Generation (DPVG), as one of the most important renewable energy resources, has experienced dramatic growth worldwide due to its environmental friendliness [1]–[3]. The grid-tied inverters, connecting the power grid with PV arrays, play an integral role in DPVG systems and have been investigated [4]–[6]. Owning to the advantages of low cost, high efficiency and small size, transformerless inverters using MOSFET switches are regarded as one of the most promising topologies [7]–[9].

Recently, a grid-tied inverter called Aalborg inverter has been proposed in [5], where it is a new family of high efficiency MOSFET-switch-based half-bridge type inverter with a wide variation of input DC voltage. Similar to the conventional dual mode time-sharing inverters [10], [11], since only one power stage chops at high frequency at any time, the minimum switching power losses and high efficiency of the Aalborg inverter can be realized. Meanwhile, a low drop voltage across the filtering inductors in power loop can further reduce the power losses [12]. So this type of inverter is suitable for the connection between power grids and PV arrays. However, in order to ensure the grid-injected current amplitude value is equal during both positive and negative half line cycles, the maximum energy would not be extracted when the input DC voltages are unbalanced, which will result in sacrificing the whole conversion efficiency of the DPVG systems.

In real PV applications, the output energy of each independent PV array is influenced by many factors, such as the shape of PV panels, the air humidity [13], the incidence angle [14] and the irradiation temperature [15]. In this scenario, output DC voltages of the two independent PV sources are not always equal. Consequently, input DC energy from the PV modules cannot be fully utilized for the conventional Aalborg inverter if no other measures are taken. Thus, it is significant to make full use of each input source energy and improve the efficiency of Aalborg inverter, when the output DC voltages of independent PV arrays are unequal.

To fully utilize the DC power generated by the PV arrays, a PV string boost stage is generally applied to the interface between the inverters and PV arrays [4], [16]–[18]. The boost circuit could improve the lower input DC voltage and enable both input DC voltages to be the same for conventional Aalborg inverter, but the auxiliary hardware circuit needs extra devices which leads to a two-stage architecture which inevitably increases the cost and the complexity of the whole system. Based on the operating principle of the coupled inductor, [19] presented a coupled-inductor-based inverter which can regulate the input energy and enable the maximum energy of each PV array to be extracted. The merit of this method is that a magnetic core can be saved and a smaller size and lower cost can be attained [19], [20]. Nevertheless, the leakage inductor of the coupled inductor is required to be very small so that it can be ignored, which will increase the

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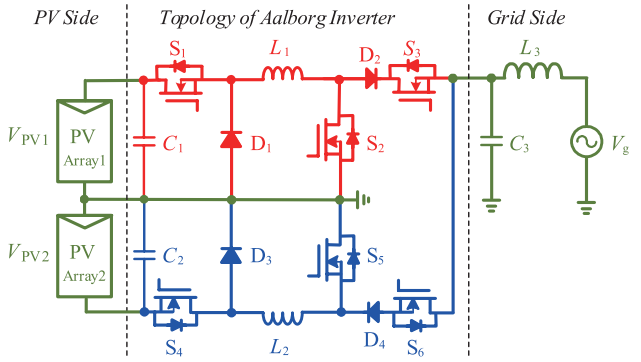


Fig. 1. Conventional Aalborg inverter with two separate input DC sources.

difficulty of the manufacturing process. On the other hand, in terms of software, some methods, like the space vector PWM (SVPWM) [21]–[23], and the predictive control strategy [24], [25], are applied to solve the imbalance issue of DC link capacitor voltage in multilevel multiphase converters, but not applicable to the conventional single-phase Aalborg inverter presented in [5]. This paper presents a modified Aalborg inverter with a single input DC source. Compared with the conventional Aalborg inverter, the main difference in configuration is that the two PV-array sources are replaced with one PV-array source and the mid-line connected ground is dismissed in the proposed inverter. The voltage balance controller is employed in the outer voltage control loop to balance the voltages of electrolytic capacitors.

The rest of this paper is organized as follows. The conventional Aalborg inverter and its principle of operation are first briefly introduced in Section II. Then, the modified Aalborg inverter is presented and analyzed through the equivalent circuits in different working states in Section III. The leakage current of the proposed inverter is analyzed in Section IV. Continuously, in Section V, the whole control strategy is designed to balance the capacitor voltages and get a sinusoidal grid-injected current. The criteria to select the values of passive element are presented in Section VI. Next, an experimental setup is built in Section VII, to verify the validity of the operating principle and the effectiveness of the control strategy. Finally, conclusions are drawn in Section VIII.

II. Conventional Aalborg Inverter

Fig. 1 shows the conventional Aalborg inverter with two separate input DC sources. The red devices work during the positive period of grid voltage. The blue devices work during the negative period of grid voltage. As shown in Fig. 2, according to the amplitude relation between the grid voltage (V_g) and the input DC voltage (V_{PV1}, V_{PV2}), the Aalborg inverter can operate in pure "Buck" mode and "Buck-Boost" mode. When the amplitude value of the grid voltage is lower than the DC voltage, it operates in "Buck" state. Otherwise, it operates in "Boost" state. Therefore, it can regulate the output voltage by changing its working states and is suitable for a wide range of input DC voltage. Furthermore, MOSFET devices are adopted, the inductor voltage drop in the power loop is minimized and only one switch is chopping at high

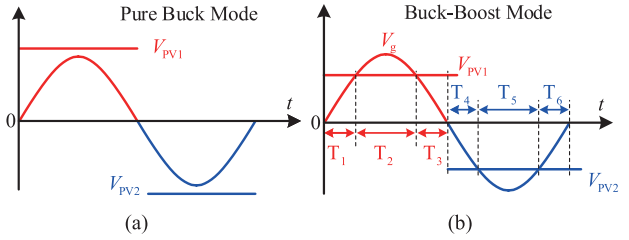


Fig. 2. Operating modes of the Aalborg inverter: (a) Pure "Buck" mode, $|V_g|$ is lower than V_{PV1} and V_{PV2}, (b) "Buck-Boost" mode, $|V_g|$ is higher than V_{PV1} and V_{PV2}.

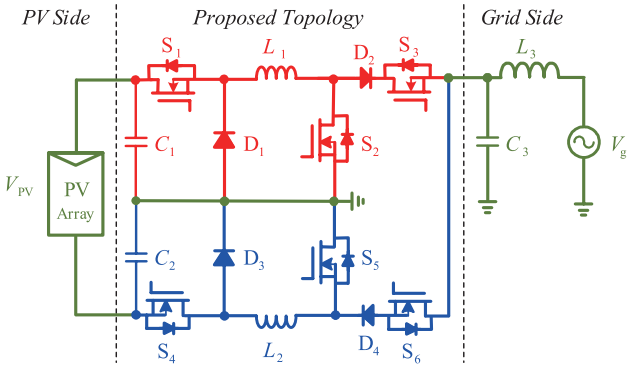


Fig. 3. The modified Aalborg inverter with a single input DC source.

frequency at any time. Thus, high efficiency can be achieved. Besides, no leakage current exists.

However, due to the overshadowed solar panels, installation angle or some other factors in the photovoltaic system [13]–[15], it is very hard for two different PV arrays to generate and output equal DC energy. In order to get a symmetrical grid-injected current, differential DC energy of the two PV arrays has to be lost [4]. Therefore, some extra measures should be taken to fully utilize the output energy of the independent PV array sources.

III. Proposed Single-Input-DC-Source Aalborg Inverter and Its Operation

A single-input-DC-source Aalborg inverter is proposed and shown in Fig. 3. The modified Aalborg inverter inherits the advantages of the conventional Aalborg inverter, such as high efficiency, no leakage current and wide range of input DC voltage. The main difference is that the PV array1 source and array2 source are replaced with one PV array source, and the mid-line connected ground is dismissed. The PV array source first supplies power to the electrolytic capacitors (C_1, C_2), then the electrolytic capacitors will supply the energy to the grid side respectively during the positive and negative period of line frequency. The modified Aalborg inverter can fully extract the energy of the PV array.

Similar to the conventional Aalborg inverter, working states of the proposed inverter are also dependent on the amplitude relation between input DC voltage and grid voltage. When $V_{PV}/2 \geqslant |V_g|$, the proposed inverter operates in "Buck" state. While when $V_{PV}/2 < |V_g|$, the proposed inverter operates in

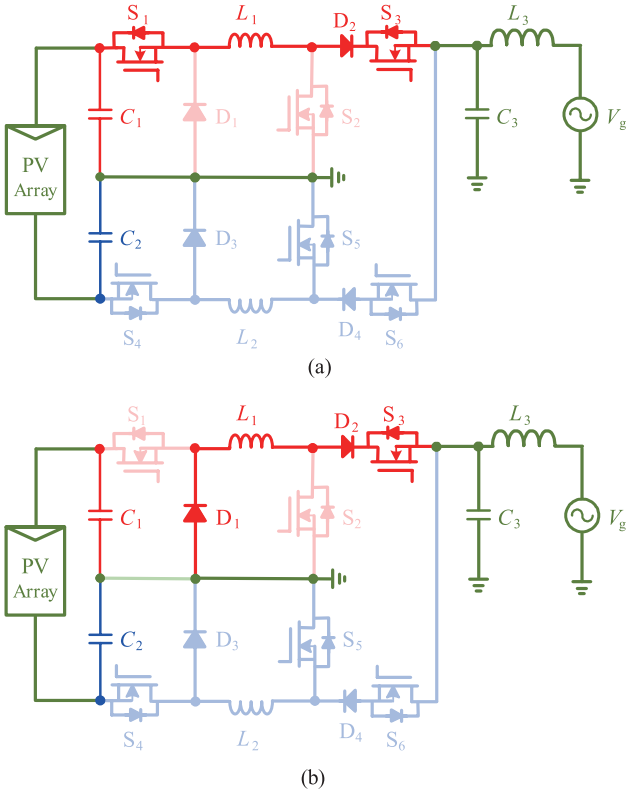


Fig. 4. Equivalent circuits during "Buck" stage in the positive period of line frequency: (a) Energy storing and (b) energy releasing.

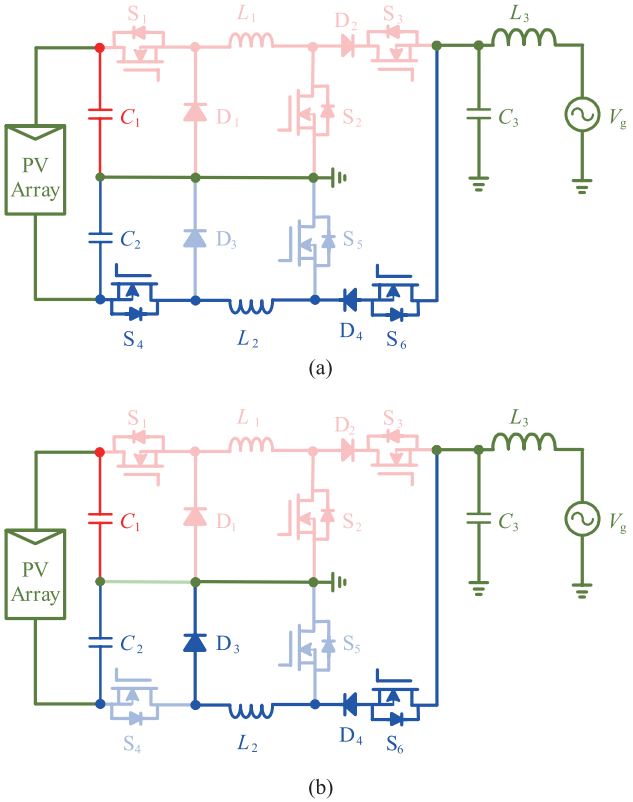


Fig. 5. Equivalent circuits during "Buck" stage in the negative period of line frequency: (a) Energy storing and (b) energy releasing.

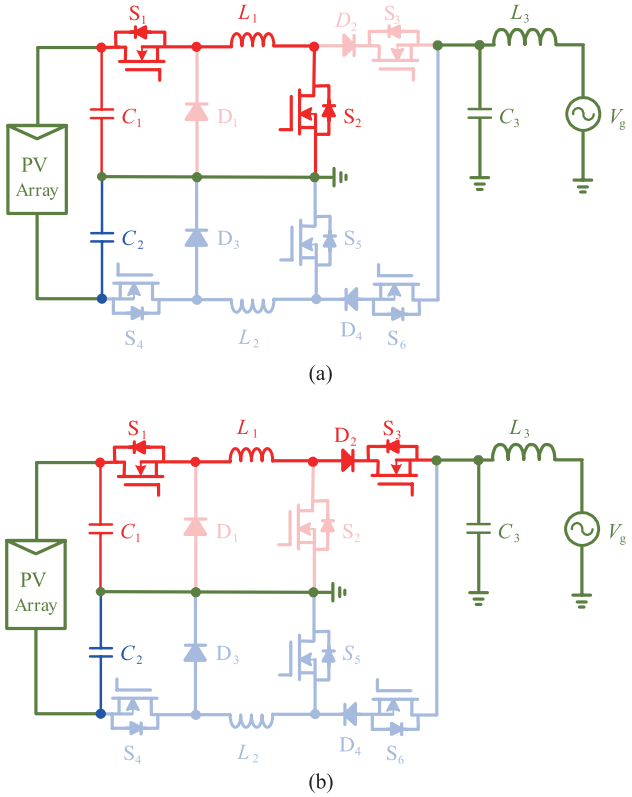


Fig. 6. Equivalent circuits during "Boost" stage in the positive period of line frequency: (a) Energy storing and (b) energy releasing.

"Boost" state. The operating principle of the proposed single-input-DC-source Aalborg inverter will be illustrated through the equivalent circuits.

When the proposed inverter works in "Buck" state, the equivalent circuits are shown in Fig. 4 and Fig. 5. During the positive period of line frequency, S_3 is on, S_1 works in high frequency and the rest of the switches are off. Fig. 4(a) shows that when S_1 is on, capacitor C_1 supplies the energy to L_1 and the grid. When S_1 is off, as shown in Fig. 4(b), the energy stored in L_1 will be released to the grid. During the negative period of line frequency, S_6 is on, S_4 works in high frequency and the rest of the switches are off. Fig. 5(a) shows that when S_4 is on, capacitor C_2 supplies the energy to L_2 and the grid. When S_4 is off, as shown in Fig. 5(b), the energy stored in L_2 will be released to the grid.

Fig. 6 and Fig. 7 show the equivalent circuits when the proposed inverter works in "Boost" state. During the positive period of line frequency, S_1 and S_3 are on, S_2 works in high frequency and the rest of the switches are off. When S_2 is on, capacitor C_1 supplies the energy to L_1. When S_1 is off, capacitor C_1 and L_1 provide energy for the grid. During the negative period of line frequency, S_4 and S_6 are on, S_5 works in high frequency and the rest of the switches are off. When S_5 is on, capacitor C_2 supplies the energy to L_2. When S_5 is off, capacitor C_2 and L_2 provide energy for the grid.

It should be noted that the PV array supplies the energy to both capacitor C_1 and capacitor C_2.

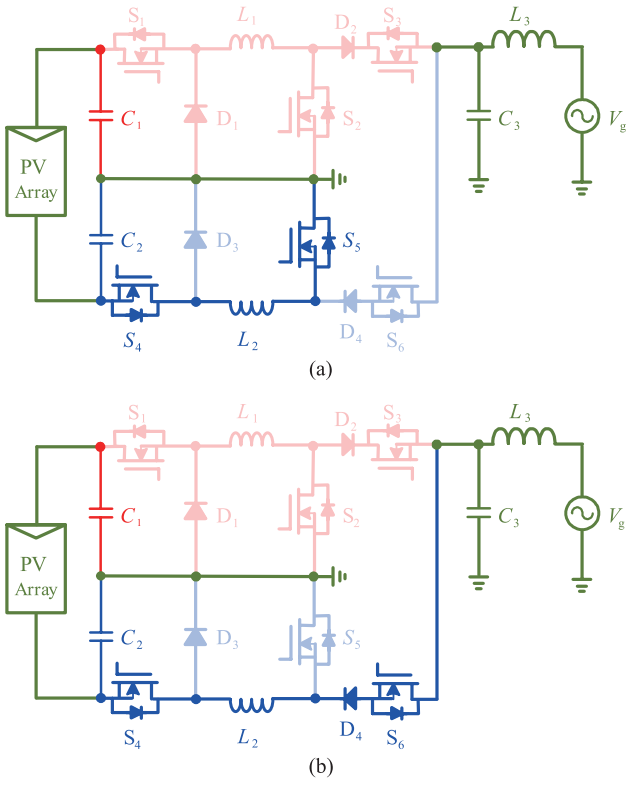


Fig. 7. Equivalent circuits during "Boost" stage in the negative period of line frequency: (a) Energy storing and (b) energy releasing.

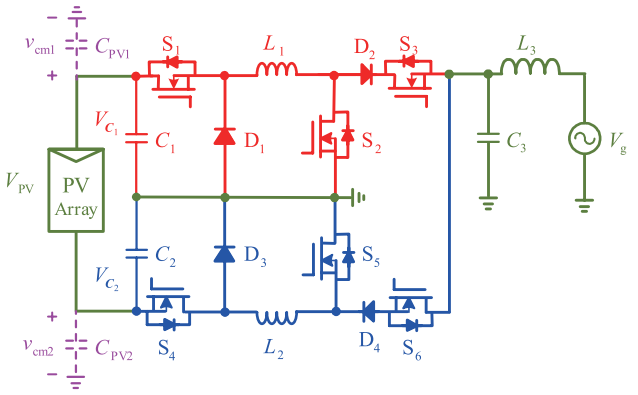


Fig. 8. The structure of the proposed topology with parasitic capacitor.

IV. Leakage Current Analysis of the Modified Inverter

As shown in Fig. 1, since one terminal of the PV panel is connected to the earth, there is no leakage current in the conventional Aalborg inverter. Fig. 8 shows the proposed inverter with parasitic capacitor. The leakage current can be derived as

$$i_{cm}(t) = C\frac{dv_{cm}}{dt} \tag{1}$$

Similar to the half bridge topology, the common mode voltage (v_{cm1} or v_{cm2}) across the parasitic capacitor is not affected

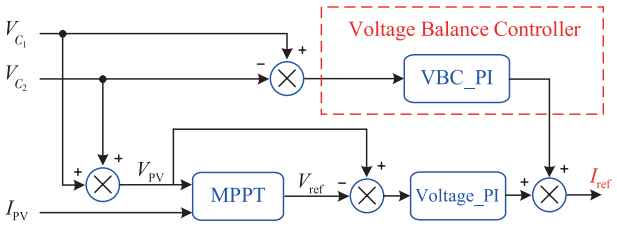


Fig. 9. The outer voltage loop control diagram.

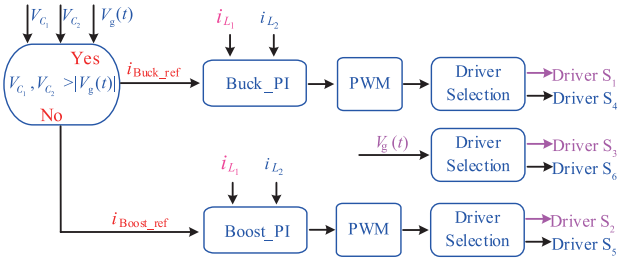


Fig. 10. The internal current loop control diagram.

by switching frequency. If the capacitance of C_1 and C_2 are equal and the capacitance value is large enough, the common mode voltage can be derived as

$$v_{cm1} = v_{cm2} = V_{C_1} = V_{C_2} = \frac{1}{2}V_{PV} \tag{2}$$

Thus, the leakage current caused by the switch operation is almost equal to zero.

V. System Control Strategy

In real applications, some factors, such as the difference of device parameters, the error of sensor and the asymmetric impedance of circuits [19], may cause the electrolytic capacitor voltages to be unbalanced, which distorts the injected current, worsens the circuit performance or even makes the system out of control. In order to balance the electrolytic capacitor voltages, a voltage balance controller (VBC) is employed in this paper. Fig. 9 depicts the outer voltage loop control diagram. The electrolytic capacitor voltages (V_{C_1}, V_{C_2}) are measured, and the difference between V_{C_1} and V_{C_2} will be regarded as the input of the VBC, the output of the VBC and the output of Voltage_PI are superimposed as the grid-injected reference current I_{ref}. VBC is a traditional PI controller. It should be pointed out that the difference of average capacitor voltages is much smaller than the value calculated by PV Maximum Power Point Tracking (MPPT).

Assuming that the electrolytic capacitors (C_1 and C_2) are large enough so that the voltage disturbance coming from the PV arrays can be ignored, and the AC source can be regarded as an ideal source. The small signal model of the modified Aalborg inverter is the same as the conventional Aalborg inverter [5].

Fig. 10 describes the internal current loop control diagram of the modified Aalborg inverter, where the input signals include the grid voltage ($V_g(t)$), the capacitor voltages ($V_{C_1}(t)$, $V_{C_2}(t)$) and the feedback current of DC inductors (i_{L_1}, i_{L_2}). When the capacitor voltage is higher than the amplitude value of grid

voltage, the modified Aalborg inverter operates in "Buck" state and it is a classical voltage source inverter with *LCL* filter, which has been analyzed in [26]–[30]. The reference current of "Buck" can be derived as

$$i_{\text{Buck\_ref}}(t) = I_{\text{ref}}(t) \tag{3}$$

When the modified Aalborg inverter works in "Boost" state, an indirect current control method is adopted since character frequency of the filter is much higher than the control bandwidth [5]. Based on the instantaneous input power equals the instantaneous output power, which can be described as,

$$V_{C_X}(t)\cdot i_{L_X}(t) = V_{\text{g}}(t)\cdot i_{\text{g}}(t),\ (\text{X} = 1, 2), \tag{4}$$

the reference current of "Boost" can be derived as,

$$i_{\text{Boost\_ref}}(t) = \frac{V_{\text{g}}(t)\cdot I_{\text{ref}}(t)}{V_{C_1}(t)(\text{or } V_{C_2}(t))} \tag{5}$$

VI. Parameter Selection of C_1, C_2, C_3, and L_1, L_2, L_3

A. The Selection of C_1 and C_2

Similar to the conventional half-bridge type converter, by proper design, the voltage fluctuation could be limited to values which would not affect the MPPT.

The output power P_{O} can be obtained by the instantaneous voltage and the current of the output power grid.

$$\begin{aligned} P_{\text{O}}(t) = v_{\text{g}}\cdot i_{\text{g}} &= V_{\text{gm}}\sin\omega t\cdot I_{\text{gm}}\sin\omega t \\ &= \frac{V_{\text{gm}}\cdot I_{\text{gm}}}{2} - \frac{V_{\text{gm}}\cdot I_{\text{gm}}\cdot\cos 2\omega t}{2} \\ &= P_{\text{dc}} + \hat{P}_{\text{ac}}(t) \end{aligned} \tag{6}$$

where V_{gm} is the peak value of the grid voltage, I_{gm} is the peak value of the grid-side current, $\omega = 2\cdot\pi\cdot f$, f is the grid frequency. It can be seen that the output power P_{O} consists of DC component (P_{dc}) and AC component ($\hat{P}_{\text{ac}}(t)$).

Since the input of the inverters is DC power and the output is AC power, according to the conservation of energy, there is power fluctuation on the DC bus. The instantaneous power difference can be obtained by using (6).

$$\hat{P}_{\text{ac}}(t) = -\frac{V_{\text{gm}}\cdot I_{\text{gm}}\cdot\cos 2\omega t}{2} \tag{7}$$

When $\hat{P}_{\text{ac}}(t) > 0$, the capacitor release the energy, which can be derived as

$$\Delta W = \int \hat{P}_{\text{ac}}(t)\,\text{d}t = \frac{V_{\text{gm}}\cdot I_{\text{gm}}}{2\omega} \tag{8}$$

At the same time, the change of capacitance energy can be obtained according to the change of DC bus voltage.

$$\begin{aligned} \Delta W &= \frac{1}{2}C_X(V_{C_X} + \Delta V_{C_X})^2 - \frac{1}{2}C_X(V_{C_X} - \Delta V_{C_X})^2 \\ &= 2C_X V_{C_X}\cdot\Delta V_{C_X},\ (\text{X} = 1, 2), \end{aligned} \tag{9}$$

where V_{C_X} is the average value of C_1 or C_2, ΔV_{C_X} is the voltage ripple of C_1 or C_2. The capacitance value of C_1 or C_2 can be attained from (8) and (9).

$$C_X = \frac{V_{\text{gm}}\cdot I_{\text{gm}}}{4\omega\cdot V_{C_X}\cdot\Delta V_{C_X}} = \frac{P_{\text{dc}}}{2\omega\cdot V_{C_X}\cdot\Delta V_{C_X}} = \frac{P_{\text{O}}}{2\omega\cdot V_{C_X}\cdot\Delta V_{C_X}\cdot\eta}, \tag{10}$$

where η is the efficiency of the whole system. It can be seen that the minimum value of capacitor C_X is determined by the maximum value of voltage ripple.

Suppose $P_{\text{O\_max}} = 800$ W, $\eta = 98\%$, for a maximum ripple of 5%, and substitute other corresponding parameters into (10), the minimum value of C_1 or C_2 can be obtained when the inverter works in "Buck-Boost" mode ($V_{C_1} = V_{C_2} = 100$ V).

$$C_1 = C_2 = 2598\ \mu\text{F} \tag{11}$$

Considering some factors, such as power losses, capacitor aging and steady-state characteristics of the system, the DC bus capacitor [31] is finally selected as $C_1 = C_2 = 4000\ \mu$F.

B. The Selection of L_1, L_2, L_3, and C_3

In this paper, inductors L_1 and L_2 work in continuous conduction mode. The design principle of L_1, L_2 and C_3 given in [32] is followed. When the inverter operates in pure "Buck" mode, values of L_1 and L_2 are obtained from the expression given in [32]

$$\begin{aligned} L_1 &= \frac{V_{C_1}(t) - V_{\text{g}}(t)}{2\,\Delta i_{L_1}}\text{D}\cdot T_{\text{S}}, \\ L_2 &= \frac{V_{C_2}(t) - V_{\text{g}}(t)}{2\,\Delta i_{L_2}}\text{D}\cdot T_{\text{S}} \end{aligned} \tag{12}$$

Typical values of Δi_{L_X} (X = 1, 2) lie in the range of 10% to 20% of the full-load [32]. In this paper $P_{\text{O\_max}} = 800$ W, $V_{\text{g}} = 110$ V, $T_{\text{S}} = 1/40$ k, and suppose the current ripple Δi_{L_X} is

$$\Delta i_{L_X} \leqslant 15\%\cdot i_{\text{g}} \tag{13}$$

By combining (12) and (13), when the inverter works in pure "Buck" mode and D = 0.5, the minimum DC inductor (L_1 or L_2) can be calculated as

$$L_1 = L_2 \approx 0.631\ \text{mH} \tag{14}$$

Considering that the inductance value decreases with the increase of current, $L_1 = L_2 = 0.8$ mH is chosen in this paper. In order to achieve wide stability margin and large control band width, a value which is not larger than L_1 or L_2 is selected for L_3 [33].

Likewise, when the proposed inverter works in "Boost" state,

TABLE I
PARAMETERS FOR EXPERIMENTS

Parameter	Value
DC inductor L_1, L_2	0.8 mH
Electrolytic capacitor C_1, C_2	4000 μF
Filter inductor L_3	0.8 mH
Filter capacitor C_3	2 μF
Grid voltage V_g	110 V
Grid frequency f_o	50 Hz
Switching frequency f_{sw}	40 kHz
Input DC voltage V_{PV}	200 V/400 V

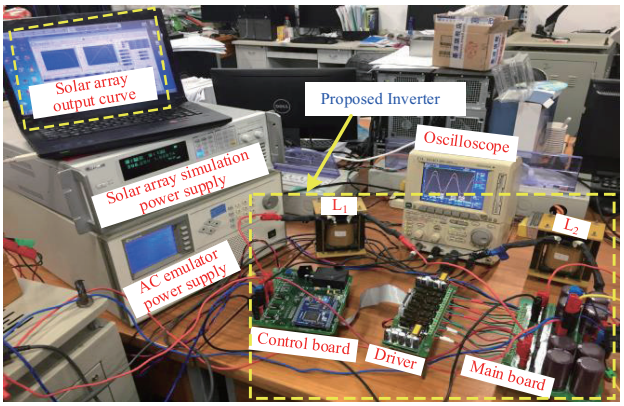
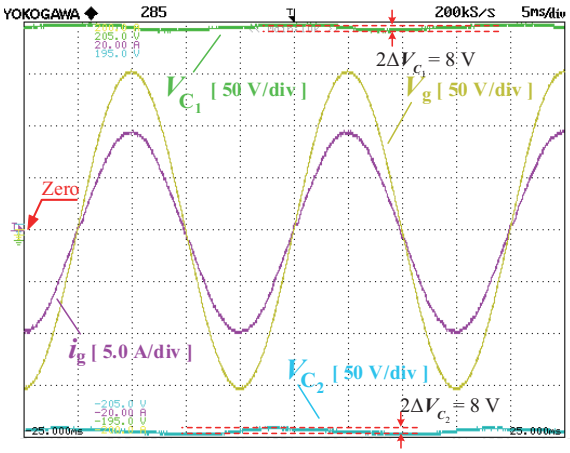
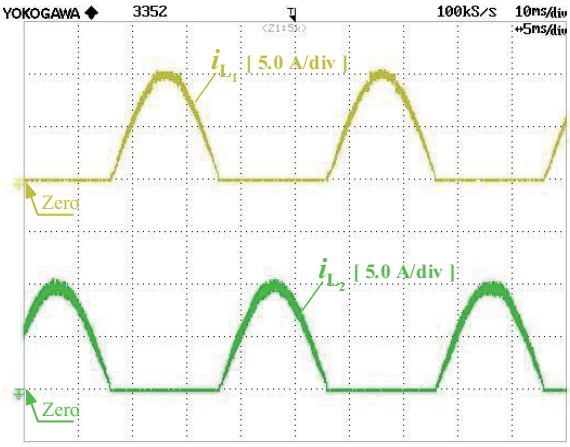


Fig. 11. Experimental prototype developed for the proposed inverter.



(a)



(b)

Fig. 12. Experimental waveforms in pure "Buck" mode, when V_{PV} = 400 V, V_g = 110 V and P_O = 770 W. (a) Measured capacitor voltages (V_{C_1}, V_{C_2}), grid-injected current ($i_g(t)$), grid voltage ($V_g(t)$). (b) Measured DC inductor currents (i_{L_1}, i_{L_2}).

the value of C_3 can also be obtained from the expression derived in [32]

$$C_3 = \frac{V_g(t)}{2R_f \Delta v} \mathrm{D} \cdot T_S, \tag{15}$$

wherein, R_f is the equivalent resistor for calculating the generated power. Suppose the voltage ripple Δv is

$$\Delta v \leqslant 15\% \cdot v_g \tag{16}$$

Based on (15) and (16), when the inverter works in pure "Boost" mode and D = 0.3548, the minimum capacitor (C_3) can be calculated as

$$C_3 \approx 1.955\ \mu\mathrm{F}, \tag{17}$$

C_3 = 2 μF is chosen in this paper.

VII. EXPERIMENTS

As shown in Fig. 11, a 110 V/50 Hz/800 W prototype has been constructed to verify previous analysis. The parameters of the system are listed in Table I. A DSP controller (TMS320LF28335) is adopted to complete all the control tasks. A solar array power supply (Chrome 62150H-600s) is provided to imitate the PV array, and the grid voltage is emulated by using a programmable AC Source of Chroma 6530. The experimental results are displayed in Figs. 11–14, respectively.

Figs. 12–14 show the experimental results when V_{PV} = 400 V, V_g = 110 V, the proposed inverter operates in pure "Buck" mode. Fig. 12 depicts the measured electrolytic capacitor voltages of $V_{C_1}(t)$ and $V_{C_2}(t)$, the grid voltage of $V_g(t)$ and the grid-injected current of $i_g(t)$. From Fig. 12, it can be seen that the grid-injected current is in a good sinusoidal shape and the electrolytic capacitor voltages are almost balanced through the control of VBC (V_{C_1} = 198.68 V, V_{C_2} = 200.45 V). Moreover, the electrolytic capacitor ripple voltage is very small and the ripple voltage is about 4 V. The power factor (PF) and the THDs of the grid-injected current and voltage are measured in Fig. 13. The PF is almost one unit (0.9974) and the THD of the grid-injected current is only 1.86%. Fig. 14 shows that the proposed inverter has a very high MPPT's efficiency, which is around 99.20%.

When V_{PV} = 200 V, V_g = 110 V, the proposed inverter operates in "Buck-Boost" mode and the experimental results are shown in Figs. 15–17. Fig. 15 shows the capacitor voltages of $V_{C_1}(t)$ and $V_{C_2}(t)$, the grid voltage of $V_g(t)$ and the injected current of

(a)

(b)

Fig. 13. The measured results in pure "Buck" mode, when V_{PV} = 400 V, V_g = 110 V and P_O = 760 W. (a) The power factor of the system. (b) The THD values of output voltage and current.

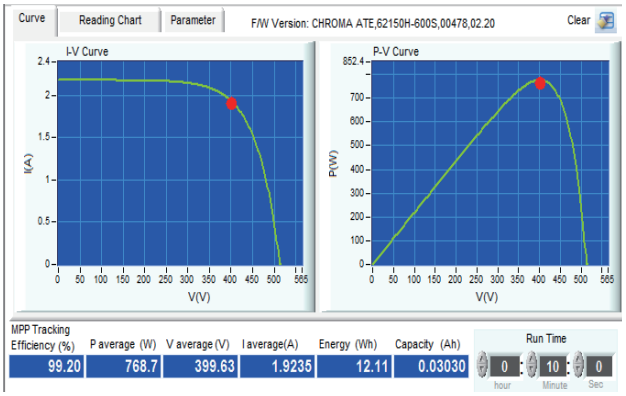
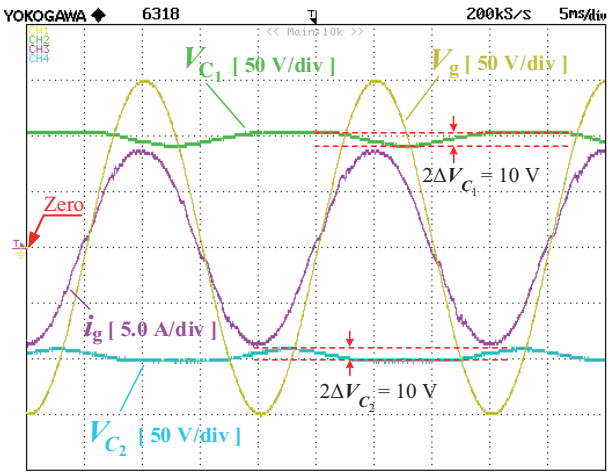
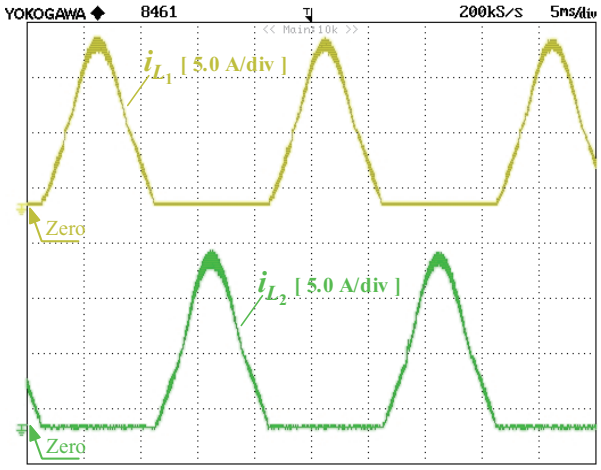


Fig. 14. MPPT results in pure "Buck" mode, when V_{PV} = 400 V, V_g = 110 V and P_O = 770 W.

$i_g(t)$. It can be seen that grid-injected current also has a pretty sinusoidal waveform except for a little distortion resulted from the Buck-Boost switching point. The electrolytic capacitor voltages are kept balanced (V_{C_1} = 101.3 V, V_{C_2} = 101.2 V) and the average voltage of each capacitor is equal to half of the PV array output



(a)

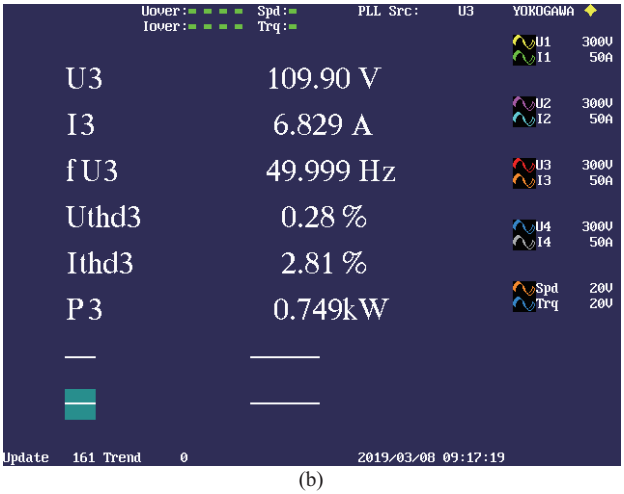


(b)

Fig. 15. Experimental waveforms in "Buck-Boost" mode, when V_{PV} = 200 V, V_g = 110 V and P_O = 770 W. (a) Measured capacitor voltages (V_{C_1}, V_{C_2}), grid-injected current ($i_g(t)$), grid voltage ($V_g(t)$). (b) Measured DC inductor currents (i_{L_1}, i_{L_2}).

(a)

Fig. 16. Measured results in "Buck-Boost" mode, when V_{PV} = 200 V, V_g = 110 V and P_O = 750 W. (a) The power factor of the system.



(b)

Fig. 16. (*Continued*..) The measured results in "Buck-Boost" mode, when V_{PV} = 200 V, V_g = 110 V and P_O = 750 W. (b) The THD values of output voltage and current.

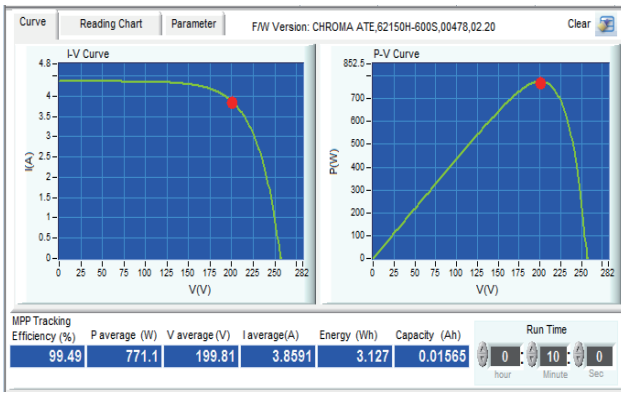


Fig. 17. MPPT results in "Buck-Boost" mode, when V_{PV} = 200 V, V_g = 110 V and P_O = 770 W.

voltage, which means the proposed control method can realize the capacitor voltage balance of the modified Aalborg inverter. At the same time, compared with the electrolytic capacitor voltages, value of the voltage ripple is about 5 V, which is consistent with previous analysis. Fig. 16 shows that the PF is equal to 0.9978 and the THD of the output current and voltage are slightly larger than that in pure "Buck" mode, because of the Buck-Boost switching point. MPPT's results are shown in Fig. 17, it can be seen that the MPPT's efficiency, about 99.49 %, is also very high.

VIII. Conclusion

This paper presents a modified Aalborg inverter with a single input DC source to maximize power yield from the PV array. The characteristics of this inverter can be summarized as follows.

1) Similar to the conventional Aalborg inverter proposed in [5], the inductor voltage drop in power loop is minimized, MOSFET switches are adopted and only one switch operates at high frequency at any time, which ensures that the proposed inverter has a high efficiency. Besides, the input DC voltage can vary widely and no leakage current exists.
2) Different from the conventional Aalborg inverter proposed in [5], the modified Aalborg inverter only requires one PV array source, rather than two. The mid-line connected ground is dismissed. The PV array source first supplies power to the electrolytic capacitors (C_1, C_2), then the electrolytic capacitors will supply the energy to the grid side respectively during positive and negative period of line frequency. The modified Aalborg inverter can fully extracted the energy of the PV array.

The operating principle of the proposed inverter has been illustrated through the equivalent circuits. The whole control strategy is designed to balance the capacitor voltages and obtain a sinusoidal grid-injected current. Experimental results based on an 110 V/50 Hz/800 W prototype have verified the feasibility of theoretical analysis and the effectiveness of the control strategy.

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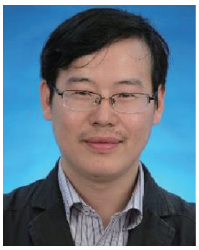

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Control Strategy to Start a Shaft Generator System Employing DFIM Under Power Take Me Home Mode

Tong Zhao, Dawei Xiang, and Yan Zheng

***Abstract*—Comparing to the traditional synchronous or induction electric machines, the doubly-fed induction machine (DFIM) with the partially rated converter is a good solution for a shaft generator system which normally operates within a relatively small adjustable speed range. However, the application of DFIM is limited in the real systems due to the lack of self-start capability under the power take me home (PTH) mode when the main engine fails. To overcome this problem, an approach is proposed in this paper. The basic idea is first to start the machine in the induction machine (IM) mode feeding from the ship-borne power grid (SPG) and then to switch over into the DFIM mode when the speed reaches its normal speed range. The hardware scheme, start procedure and control algorithm of the start approach are presented in the paper. Simulation and experimental studies were carried out to validate the feasibility and effectiveness of the approach.**

***Index Terms*—doubly-fed induction machine (DFIM), power take me home (PTH), shaft generator system.**

I. Introduction

OWING to the increasing pressure on global environmental and energy resources, there is a technical trend to continuously reduce fossil fuel consumption and the CO_2 emission for ships [1]−[3]. Moreover, the global economic crisis makes managers more sensitive about the cost of international sea transportation [4]−[8]. As a result, more and more attention has recently been paid to the shaft generation (SHG) technology.

In an SHG system as shown Fig. 1, a shaft machine is connected with the main engine (mostly a diesel engine) by clutches and gear box, which can operate as a generator or a motor. It helps the conventional ship propulsion system to improve not only the energy efficiency but also the system reliability. When the main engine (ME) fails, the shaft machine can drive the whole ship independently at a lower speed in order to return to a port, which is called as the power take me home (PTH) mode.

According to the rating of the power converter, the SHG systems could be divided into two types, i.e., the full-power shaft generator (FPSG) system and doubly-fed shaft generator (DFSG) system. The FPSG system has a wide speed range which can be easily started to drive the ship without ME in PTH mode. However, a larger capacity of the converter is demanded in the FPSG system, which increases the cost and volume of the system in the limited room on board [9]−[10]. DFSG system has less cost and smaller volume because of the smaller capacity of the converter. Unfortunately, its speed range is relatively small, which cannot be directly started from a standstill and operated in PTH mode [11]−[15].

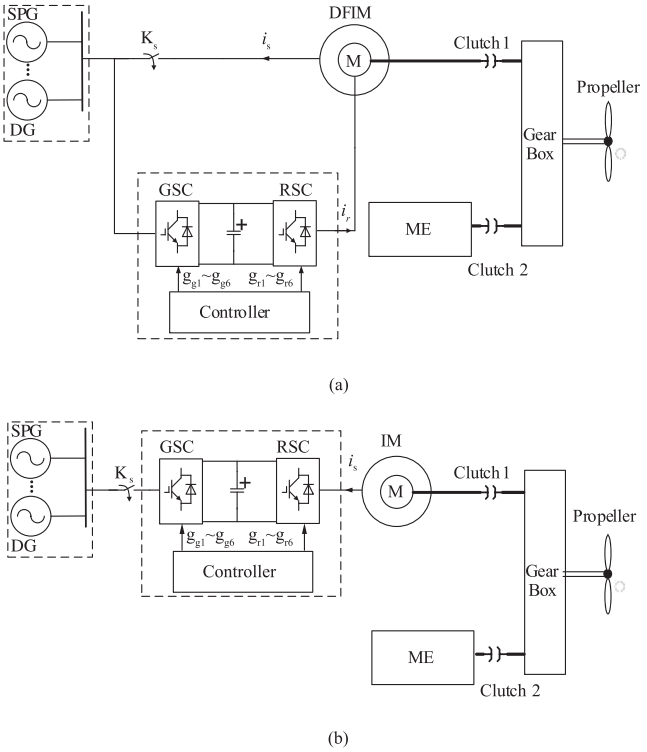

Fig. 1. Structures of SHG system. (a) Doubly-fed shaft generator system. (b) Full-power shaft generator system.

To overcome the self-start difficulty of DFSG system, an approach is proposed in this paper. The basic idea is first to start the machine in the induction machine (IM) mode feeding from the ship-borne power grid (SPG) and then to switch over into the DFIM mode when the speed reaches its normal speed range. Simulation is carried out to verify the feasibility and effectiveness of this approach. To clarify the method, the remaining paper is organized as follows. Firstly, the principle of this approach is described in Section II including the hardware scheme, start process and control algorithm. Then, a typical 500 kW DFSG system is studied using MATLAB/Simulink in Section III to prove the method. After that, an experimental platform is built and

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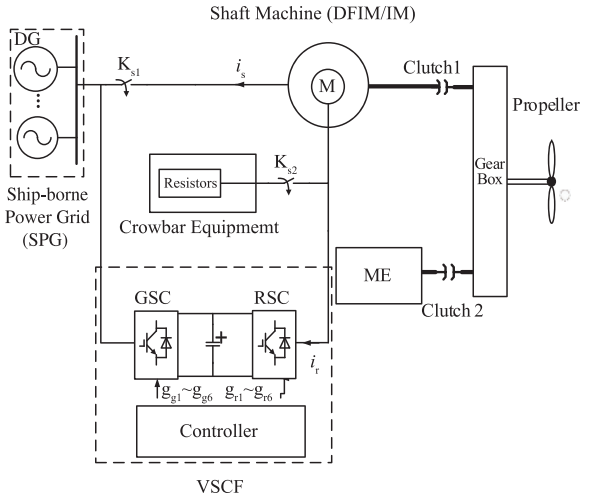


Fig. 2. Structure of the improved DFSG system.

experimental results show the practical application effect of this method in Section IV. Finally, the conclusion is made in Section V to highlight the advantages of the method.

II. DFIM Shaft Generator System Start Approach Under PTH Mode

A. Principle

The method proposed in this paper aims at starting the DFIM from a standstill under PTH mode, which can hardly be realized in a conventional DFIM system. The key of this approach is to modify the DFIM into an induction machine to start it from a standstill. Specifically, the machine is firstly converted into an IM by shorting the three-phase rotor windings. Then, the machine can be started as an IM until its speed reaches the DFIM speed range. After that, the three-phase rotor windings will be opened to allow the machine operating in the DFIM mode to drive the ship independently under PTH mode.

This method switches the machine operating between the IM and DFIM modes. By combining the advantages of IM (self-start) and DFIM (partial-rated converter) together, it can effectively improve the technical and economic performance of SHG technology.

B. Hardware Scheme

Comparing with the conventional solution, a crowbar with K_{s2} and resistors (for rotor current limitation) are added in the improved DFSG system (see in Fig. 2), which enables the machine to switch between DFIM and IM modes. When K_{s2} is closed, the rotor windings are short-circuited and the machine works like an IM. K_{s2} cannot be opened until the speed exceeds the minimum speed of DFIM mode.

As shown in Fig. 2, the ship-borne power grid (SPG) is powered by several diesel generators (DG). The improved DFSG system has two switches, K_{s1} and K_{s2}. K_{s1} connects the stator to the SPG directly. K_{s2} connects with the three-phase rotor windings. Meanwhile, the rotor is also connected with a variable-speed constant-frequency (VSCF) equipment, which consists of a back-to-back grid side converter (GSC) and rotor side converter (RSC). There is a controller inside the VSCF equipment that controls RSC and GSC by PWM signals.

Two clutches are connected between the gearbox and the shaft machine and ME respectively, by which the propulsion power can be independently transmitted to the propeller to drive the ship.

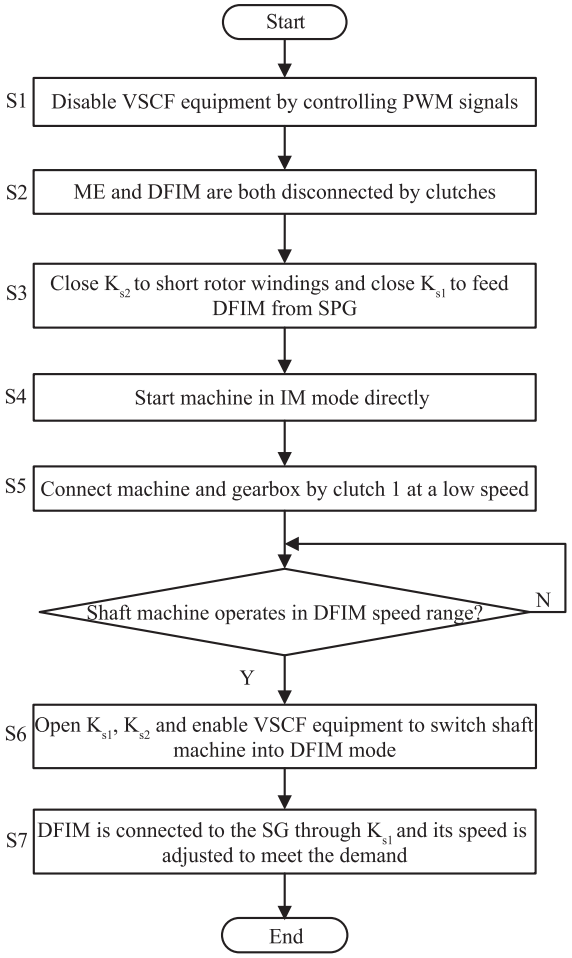


Fig. 3. Flow chart of start process of DFSG system under PTH mode.

C. Start Procedure

1) Process

The flow chart of the start process is shown in Fig. 3. Firstly, the VSCF equipment is disabled by blocking the PWM signals. Secondly, both the ME and DFIM are disconnected by clutches. Then, K_{s2} will be closed and the machine works in IM mode. After that, the machine is started by closing K_{s1} feeding from the SPG. Then the machine will be connected to the gear box and propeller by closing the clutch 1 at a low speed (e.g., 150 rpm).

After the speed increases gradually and exceeds the minimum speed of DFIM, the machine is ready to switch over into the DFIM mode. Then, K_{s1} and K_{s2} will be opened to disconnect the SPG and shorting the rotor windings. Due to the large inertia, the machine speed will be maintained for a while, during which the stator voltage can be established and stabilized. Finally, K_{s1} is closed and the machine controlled by the VSCF equipment is connected to the SPG. At this time, the start process is finished and the ship can be driven by the DFIM under PTH mode. Note that, the step S6 could be simplified by only open K_{s2} with K_{s1} remaining closed, but K_{s2} must be switched at current zero crossing point to avoid switching over-voltage.

2) Mode Switching

As the key step in the whole start process, the mode switching process between IM and DFIM modes (S6 in Fig. 3) can be divided into 2 sub-steps as follows:

Sub-Step 1: Field Energy Dissipation

K_{s1} is opened and K_{s2} is kept closed until the stator voltage reduces to an acceptable level. During this sub-step, the electromagnetic field energy in the shaft machine is mainly dissipated by the crowbar resistor.

Sub-Step 2: Re-Excitation

After field energy dissipation, open K_{s2} and re-excite the machine by the VSCF equipment to establish a stable stator voltage identical to voltage of SPG ready for grid integration.

D. Control Algorithms

During the start process, the machine operates in two modes depending on whether the rotor windings are close or open. While the speed is less than the minimum DFIM speed, the rotor windings are shorted by K_{s2}. The machine is fed from the SPG by closing K_{s1} and started directly in IM mode. As the machine's speed increases, K_{s1} and K_{s2} will not be opened until the machine enters into the DFIM normal speed range. And then, the machine is converted to DFIM mode by switching K_{s1} and K_{s2} properly.

In IM mode, the shaft machine is directly started by the SPG. Some electromechanical impact (over-current and electromagnetic torque oscillation) will occur, due to the low power factor at low speed and the effect of transient DC stator flux. However, since the transient is short (typically several seconds), it is considered that the impact is tolerable for the system.

In DFIM mode, the machine is controlled by the VSCF equipment using the grid voltage oriented control algorithm (GVOC) [16]–[17]. The structure of GVOC is shown in Fig. 4. The active and reactive powers are decoupled through Park transformation and controlled by i_{rd_ref} and i_{rq_ref} respectively.

θ_g is the angle of Park transformation obtained from the phase locked loop (PLL) as shown in Fig. 5. U_{sq} and U^*_{sq} are

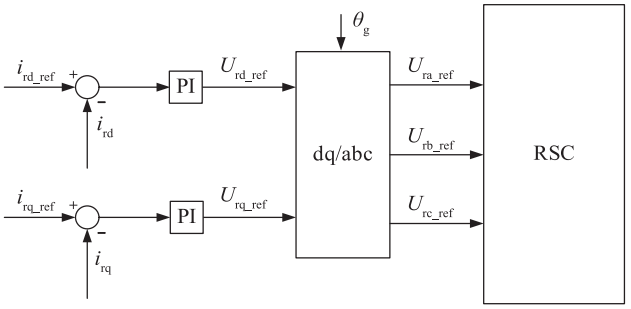


Fig. 4. Block diagram of GVOC control algorithm for DFIM.

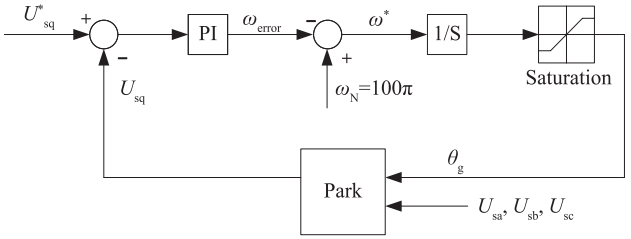


Fig. 5. Block diagram of PLL.

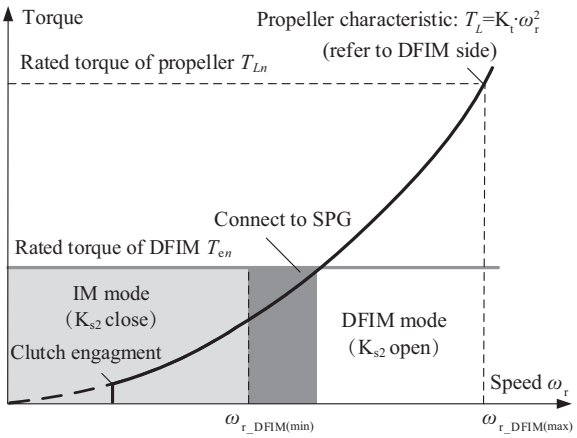


Fig. 6. The torque-speed characteristics of DFSG system with PTH capability.

used to calculate ω_{error}, which is added to ω_N to estimate ω^*. Then, ω^* is integrated to obtain θ_g. The detailed description of PLL can be found in [18].

The control algorithm proposed above allows the machine to start from the standstill and propel the ship under PTH mode. By overcoming the difficulty of DFIM self-start, the method will facilitate the application of DFIM in the SHG systems.

E. Capacity Matching Relationship in DFSG System

As shown in Fig. 2, a DFSG system is mainly composed of DFIM, VSFC, SPG, propeller and ME. To ensure a reliable PTH start, their capacities must be well matched. Theoretically, the capacity matching relationship is decided by the torque-speed characteristics of DFSG system as show in Fig. 6, where the critical constrain is that the rated torque

of DFIM $T_{e(n)}$ must be greater than the propeller torque (refer to DFIM side) at the minimum speed of DFIM mode $\omega_{r\_DFIM(min)}$ to ensure the system can be started in PTH mode. Consequently, the capacity matching relationship between different units could be derived in the equations as below.

$$T_{e(n)} > T_L @ \omega_{r\_DFIM(min)} \Rightarrow P_{DFIM} > \frac{(1-s_{max})^2}{(1+s_{max})^3} = P_{PP} \quad (1)$$

$$P_{VSFC} = s_{max} P_{DFIM} \quad (2)$$

$$P_{DE} = (1+s_{max}) P_{DFIM} + P_{PP} \quad (3)$$

$$P_{SPG} > P_{DFIM} \quad (4)$$

Where, $T_{e(n)}$ and T_L are the torques of DFIM and propeller (refer to DFIM side) respectively; $\omega_{r\_DFIM(min)}$, $\omega_{r\_DFIM(max)}$, s_{max} are the minimum speed, maximum speed and maximum slip ratio of DFIM; P_{DFIM}, P_{VSFC}, P_{PP}, P_{DE}, P_{SPG} are the nominal power ratings of DFIM, VSFC, propeller, the main engine and ship-borne power grid. It is noted that the equations above are the theoretical critical limitations. In a real system, some design margins must be given for system safety and reliability.

It can be seen in (1) and (2) that a larger speed operation range is preferred for a less power rating of DFIM with PTH capability but at the cost of higher power rating of VSFC. The tread-off between the capacities of DFIM and VSFC must be carefully considered at the stage of design, which affects the overall economic and technical performance of the system.

III. Simulation Study

A. Simulation Model

In order to verify the feasibility and effectiveness of the proposed method, a 500 kW DFSG system was designed and simulated using MATLAB/Simulink as shown in Fig. 7. The parameters of the simulation system and DFIM are listed in Table I and Table II respectively. Note that, the rated values are used as the basic values of per unit (p.u.) in this paper.

The torque-speed characteristics of the shaft machine and propeller are plotted in Fig. 8. It is shown that the propeller can be driven by the shaft machine operating in IM mode at low speed. When rotor speed ω_r reaches the minimum speed of DFIM (700 rpm), the operation mode will be changed from IM to DFIM by switching K_{s1} and K_{s2}. Then, the machine is connected into the SPG so that the ship can be driven in DFIM mode while its speed is between 700 rpm and 800 rpm. During the start process, the propeller prefers to connect into the shaft machine by clutch 1 at a relatively low speed for safety reason.

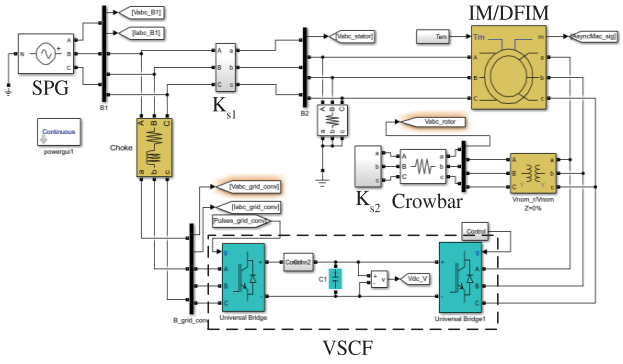


Fig. 7. Simulation model of the improved DFSG system.

TABLE I
Parameters of Simulation DFSG System

Rated ME power	2.15 MW
Rated propeller power	1.5 MW
Rated propeller speed	216.7 rpm
Rated DC bus voltage	700 V
Rated RSC capacity	160 kVA
Switching frequency	3 kHz
Gearbox speed ratio	1:6
Clutch engagement speed	150 rpm
Crowbar resistor	0.2 Ω
Inertia time constant of drive train	5.5 s

TABLE II
Parameters of DFIM

Rated power	500 kW
Rated stator line-to-line voltage	400 V
Rated frequency of stator	50 Hz
Open circuit voltage of rotor	1150 V
Pole pairs	3
Rated speed	1300 rpm
Normal speed range	700~1300 rpm

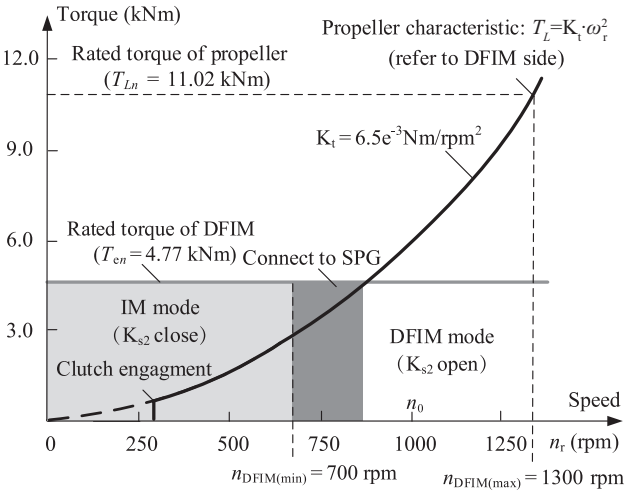


Fig. 8. The torque-speed characteristics of the improved DFSG system.

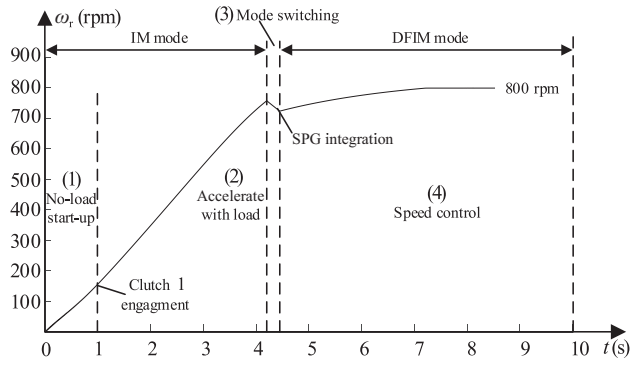


Fig. 9. Speed of shaft machine during start process under PTH mode.

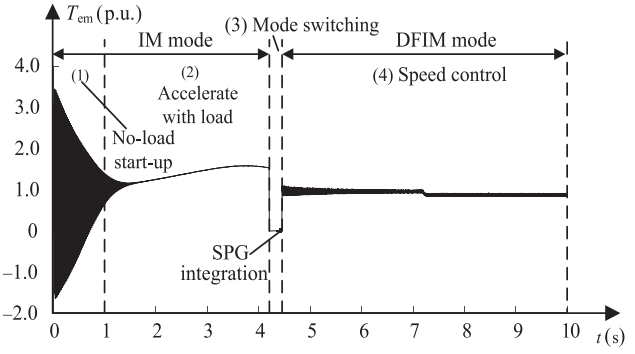


Fig. 10. Electromagnetic torque of shaft machine during start process under PTH mode.

B. Simulation Results

1) Results of the Start Process

Simulation has been carried out to study the performance of the proposed DFSG start approach under PTH mode. The simulation results are as summarized in Figs. 9−16.

The speed of shaft machine during the start process is plotted in Fig. 9. Firstly, the shaft machine starts under no-load condition by closing K_{s1} and K_{s2} in IM mode. Secondly, the propeller is connected into the machine by clutch 1 at a low speed (150 rpm). While its speed enters the normal DFIM speed region (> 700 rpm), the machine is then switched into DFIM mode by opening K_{s1}, K_{s2} and enabling VSCF equipment. During the mode switching process, a small speed decrease can be observed in Fig. 9 since the shaft machine is out of power and the speed is maintained by the inertia effect of the drive train. It, therefore, requires that the mode switching process could be completed as soon as possible.

After the SPG integration, the ship can finally be driven by the shaft machine under PTH mode independently. It takes about 10 s to complete the whole start process, which is fast enough for ship and mainly decided by the capacity of shaft machine and the aggregated inertia of drive train (including shaft machine, gear box and propeller). Note that, the adjustable maximum speed (about 800 rpm) is limited by the rated torque of shaft machine as shown in Fig. 8, which is much less than its nominal maximum speed under the hybrid generation and propulsion modes with ME (1300 rpm).

As shown in Fig. 10, the electromagnetic torque T_{em} oscillates at the beginning of the start-up, which is a typical characteristic of induction machine being started directly in full voltage. The oscillation only lasts for a short time (within 2 s) so that it will not damage the machine.

The waveform of stator voltage U_{stator} is plotted in Fig. 11. It is shown that the stator voltage is restrained by the SPG when the stator connects with SPG in both IM and DFIM modes. In the mode switching process, the stator voltage drops as the result of field energy dissipation.

The waveform of stator current I_{stator} and rotor current I_{rotor} are plotted in Figs. 12 and 13. While the machine works

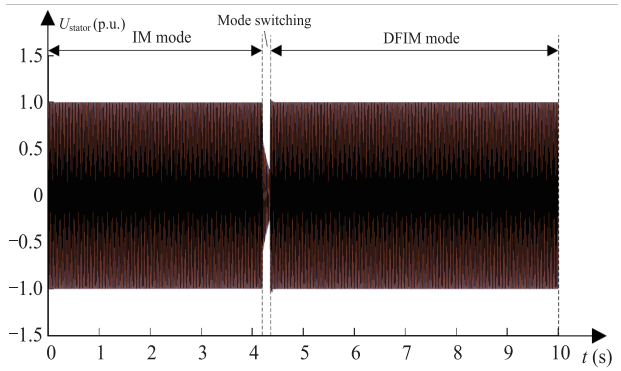


Fig. 11. Stator voltage of shaft machine during start process under PTH mode.

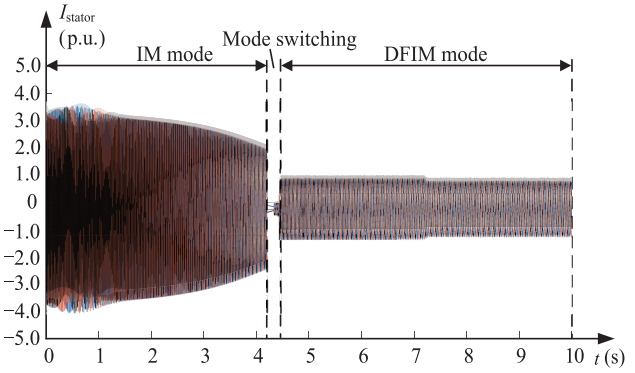


Fig. 12. Stator current of shaft machine during start process under PTH mode.

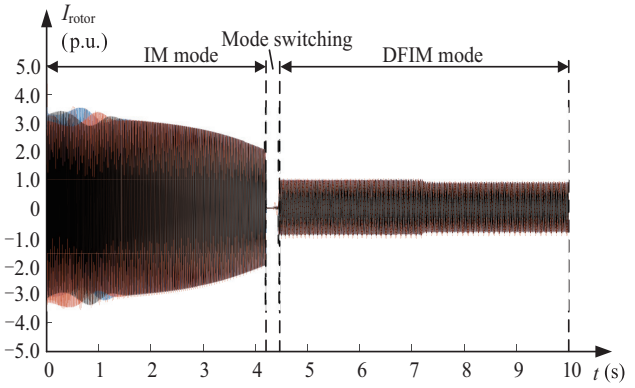


Fig. 13. Rotor current of shaft machine during start process under PTH mode.

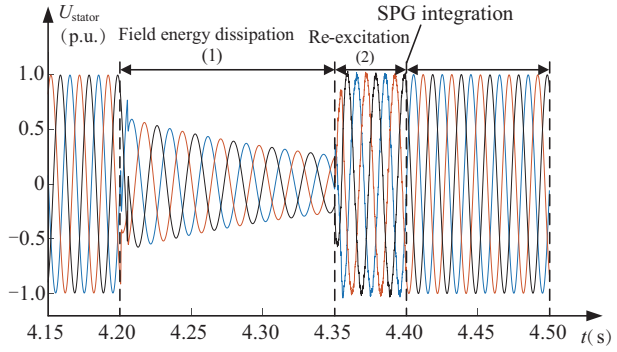


Fig. 14. The detailed waveform of stator voltage during mode switching.

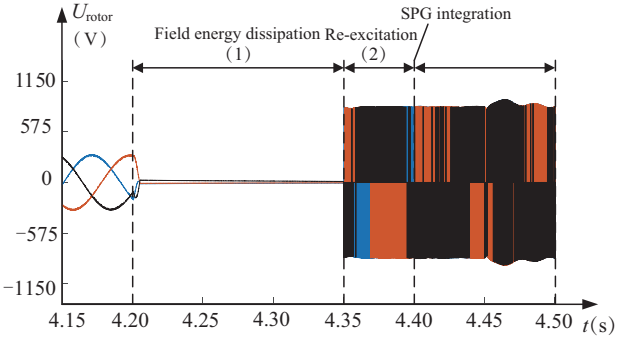


Fig. 15. The detailed waveform of rotor voltage during mode switching.

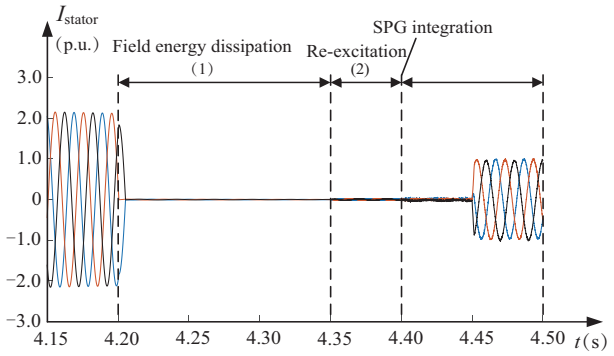


Fig. 16. The detailed waveform of stator current during mode switching.

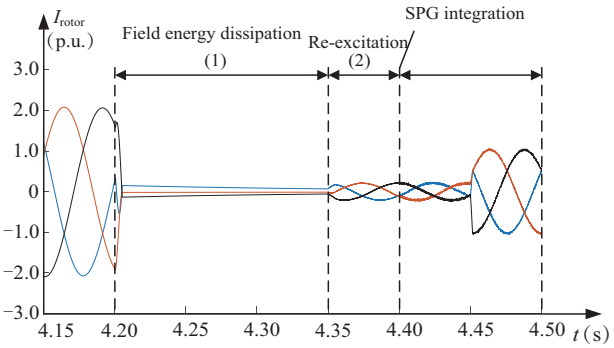


Fig. 17. The detailed waveform of rotor current during mode switching.

in IM mode, about 3 times over-current can be seen in the simulation results immediately after the machine is started up. The currents decrease gradually following the speed increase within 4 s. Note that, the large starting current will cause a non-negligible impact on both SPG and the electric machine. This could be suppressed by using the SCR based soft-start technique but with some additional equipment and cost. After switch into the DFIM mode, the currents are controlled in the nominal value to propel the ship under PTH mode safely.

2) Results of the Mode Switching Process

To further clarify the method, the detailed simulation results during mode switching process are plotted in Figs. 14 −17.

After K_{s1} is opened, the VSCF equipment cannot be directly enabled to control the shaft machine. Before re-excitation by the VSCF equipment, the electromagnetic field energy in the machine must be well dissipated. To speed the process, K_{s2} is kept closed and the energy is mainly consumed by the crowbar resistor in the sub-step (1). As a result, U_{stator}, U_{rotor} and I_{rotor} reduce gradually (shown in Figs. 14-17). Meanwhile, Istator reduces to zero quickly (shown in Fig. 16). K_{s2} will not be opened until U_{stator}, U_{rotor} and I_{rotor} reduce to an acceptable level which is ready for enabling the VSCF equipment.

In the sub-step of re-excitation, the machine is controlled by the VSCF equipment. It is shown that the rotor current I_{rotor} increases within 50 ms to the magnetization current level (see Fig. 17) and the stator voltage Ustator is established (see Fig. 15) ready for grid integration. As shown in Fig. 16, the impact of SPG integration is ignorable.

IV. Experimental Study

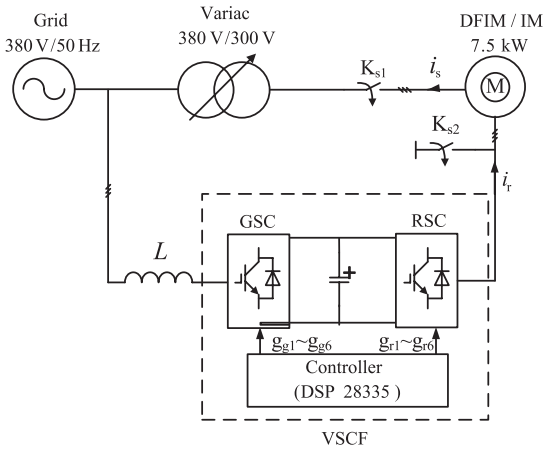
Experimental study was carried out to validate the feasibility and effectiveness of the method.

A. Setup of Experimental Platform

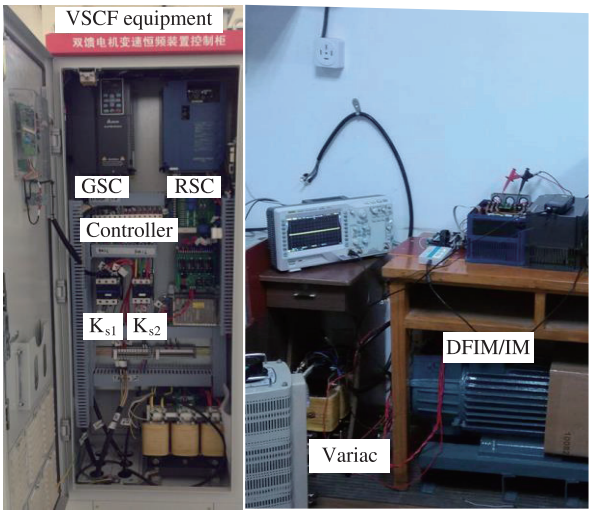
The experimental platform is shown in Fig. 18 and the parameters are listed in Table III. In this experimental platform, a wound-rotor induction machine is installed to operate as a DFIM. The VSCF equipment contains two PWM converters, where GSC adopts a commercial 15 kW active front end (AFE) and RSC is built using a 1200 V/100 A IGBT power module. The controller is designed based on the TMS320F28335 DSP. For safety reason, the DFIM operates under the derating conditions (less than 300 V/3.5 kVA) through a variac. Switching of the machine between DFIM and IM modes is realized by K_{s2}.

B. Experimental Results

The proposed method is tested on the experimental platform. The waveforms of stator voltage U_{sab}, grid voltage



(a)



(b)

Fig. 18. Setup of experimental platform. (a) Schematic diagram. (b) Picture of experimental platform.

TABLE III
PARAMETERS OF EXPERIMENTAL PLATFORM

DFIM/IM	Rated power	7.5 kW
	Rated speed	1300 rpm
	Rated rotor current	26.5 A
	Rated stator current	18 A
	Stator/rotor ratio	2.05
	Pole pairs	3
	Range of slip	−0.3~0.3
RSC	IGBT module	7MBR100U4B120
	Rated dc voltage	580 V
	Rated current	50 A
GSC	Model	Delta:AFE150A43
	Rated power	15 kW
	Rated input	323~528 V 35 A
	Rated output	DC 660 V 33 A
	L filter	4.18 mH/35 A

U_{gab}, stator current i_{sa} and rotor current i_{ra} during the start process under PTH mode are plotted in Figs. 19–22.

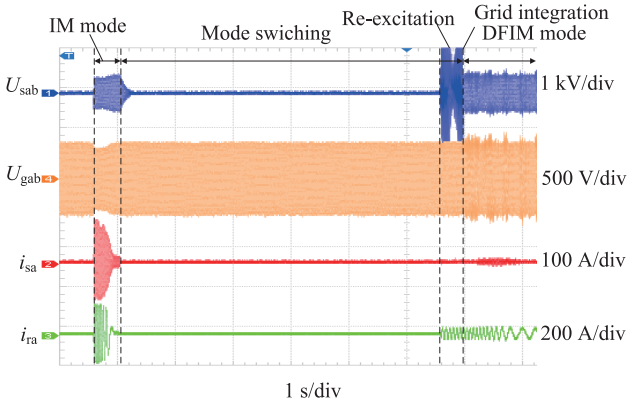


Fig. 19. The waveforms of start process under PTH operation.

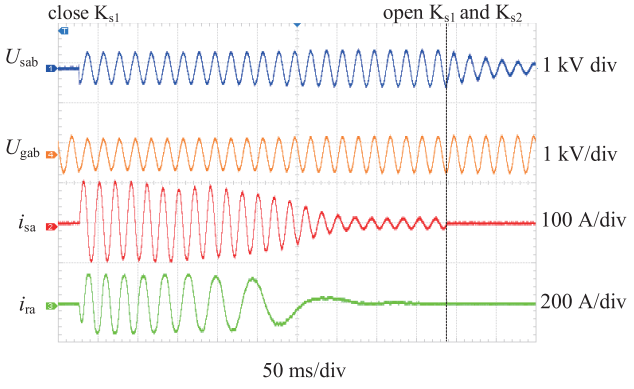


Fig. 20. The detailed waveforms during machine start in IM mode.

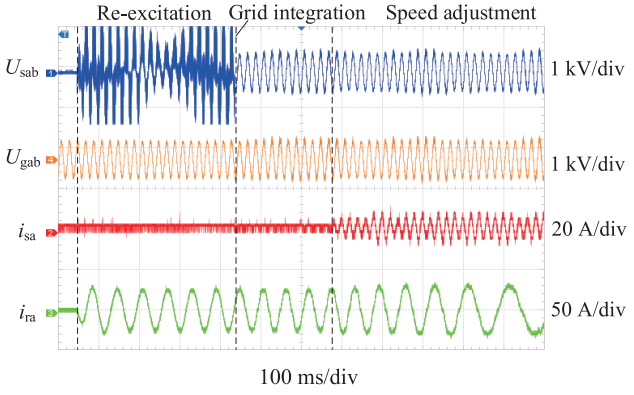


Fig. 21. The detailed waveforms during mode switching process.

The waveforms of the whole start process under PTH operation are shown in Fig. 19. Firstly, the machine with rotor windings shorted by K_{s2} is connected to the grid directly through K_{s1}. Then, K_{s1} and K_{s2} are opened when the speed exceeds the normal range of DFIM. After that, the machine is re-excited and integrated into the grid so that it can operate as a normal DFIM. So far, the whole start process is completed.

The detailed waveforms during machine start in IM mode are shown in Fig. 20. It can be seen that the stator voltage U_{sab} increases to the grid voltage U_{gab} immediately after K_{s1} is closed and decreases rapidly after K_{s1} and K_{s2} are opened.

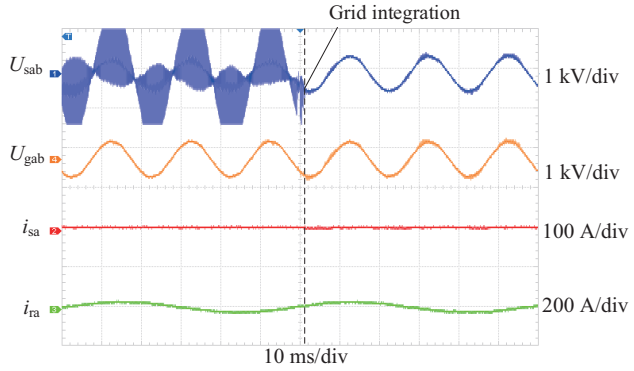


Fig. 22. The detailed waveforms during grid integration.

The stator and rotor currents (i_{sa} and i_{ra}) reach about 4 times over-current shortly (less than 350 ms) after K_{s1} is closed, which is consistent with the simulation results. When the speed increases, the frequency of rotor current i_{ra} reduces to 0 Hz gradually and the stator current i_{sa} also reduces to a relatively small magnetizing current. The speed reaches 1000 rpm at the end of the IM mode.

Fig. 21 shows the detailed waveforms during mode switching process to DFIM mode. A stable stator voltage U_{sab} is established with the machine re-excitation control, which is critical for grid integration. From Fig. 22, it can be seen that the impact of grid integration is ignorable as a result of precise control. In additionally, the frequency rotor current at the moment grid connection is 15 Hz, which means the speed of DFIM is 700 rpm just within the normal speed range. After grid integration, the stator current i_{sa} maintains zero until the speed is adjusted.

V. Conclusion

In this paper, an approach to start an SHG system employing DFIM under PTH mode is presented to reduce the cost and volume of the traditional synchronous or induction machines based SHG systems. The principle of the method is discussed in detail and its feasibility and effectiveness are confirmed by simulation and experimental studies. Research results show that the DFIM SHG system can be easily started under PTH mode with a minor hardware modification and adequate control algorithm. It is expected that this study is helpful to improve the technical and economic performance of SHG technology.

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Investigation on the Small Signal Characteristic Based on the LLC Hybrid Hysteretic Charge Control

Richard (Hua) Yang, Brent A. McDonald, and Yalong Li

***Abstract*—In this paper, an analytical small-signal model applied for hybrid hysteretic charge (HHC) control has been proposed and analyzed with the advantages over direct frequency control (DFC). Based on the approach of extended describing function method and average concept, for the first time, the systematical analytical open loop transfer functions from control to output, input to output, output impedance and the closed transfer functions of the overall loop, audio susceptibility and output impedance are proposed and verified through simulation. Additionally, some important physical insights have been extracted, analyzed and verified. Finally, the experiments on a design example of 12 VDC&12 A output power are conducted and verified. It shows that the calculations match well with the results from both the simulation and experiment, which reveals the proposed analytical transfer functions are very useful for the practical power design to achieve good prediction result.**

***Index Terms*—Analytical small signal model, hybrid hysteretic charge (HHC), hybrid hysteretic charge control, LLC, UCC25630.**

I. Introduction

With the increasing requirement on power efficiency and power density, the LLC topology has become into one of the most popular topologies of the isolated power converters. Numerous articles [1]−[6] have been created to show the best design optimization methods. However, there are the challenges for the conventional DFC LLC converter regarding the control design and loop optimization when input voltage and output voltage have been specified strictly to be within a varied range, in which the task of loop design is hard to be optimized. As for the small signal modeling on PWM converters, the state-space approach based on the average concept proposed by Middlebrook and Cuk [7] is accurate within a limited frequency bandwidth. Later R. Ridley [8] had proposed an improved methodology with the concept of the three-terminal switch, on which the good prediction result in many PWM converters are achieved [9], [10], [11], [12]. In recent years, the advanced describing function method has been successfully applied to most of current control converters with the accurate analytical transfer functions up to the switching frequency in [13]−[14]. However, all these methodologies are hard to obtain a good result if applying to the resonant converter where the switching frequency components and its harmonics have been turned into the dominant variable part and the beat frequency dynamics has occurred. Then the extended describing function method proposed by E. X. Yang [15]−[16] had been successfully applied to the resonant converter to predict the beat frequency dynamic behavior accurately.

To work out the model of LLC converter, lots of researches [17]−[20] based on the extended describing function or other similar averaged modeling concept [21] have been employed and the results are proved to be accurate to predict the beat frequency dynamics. However, the models are still hard to meet the practical engineering design due to its lack of analytical transfer functions for the physical insight extraction and most precise modes are only based on the simulation in which the physical insight is hard to yield. It is not until recent years that S. Tian [22]−[23] simplified the model from the 5th order to a 3th one with a result of an analytical transfer function for both SRC and LLC converter. Followed by this, Y. Hsieh has employed a novel rotating coordinate modeling concept to the SRC converter and achieved the most precise prediction results based on the describing transfer function [24]−[25], in which the best accurate analytical transfer function has also been extracted but it is still expected to extend to the LLC converter. As a conclusion, there is the challenge for the conventional DFC LLC control to apply to most of the applications due to its not good transient performance by the intrinsic loop characteristic.

To solve this problem, several new LLC loop control schemes have been proposed in recent years. The first one is the average current control [26]−[27], in which the tank current has been sensed and scaled and then participate in the loop control, it is proved to be with the advantages over the DFC control on input ripple cancellation but still owns the room for the further improvement in terms of the load transient performance. The second one is the charge control [28], which compares the total input charge with the control voltage to modulate the switching frequency, then an inner current loop is offered to yield the fast-transient response. Another hysteretic charge control [29]−[30] can also achieve the good dynamic load performance by sensing the current of tank current or voltage of resonant capacitor, but the DC gain of control to output is with a little big variation during the full load range which will bring the difficulty of loop design at light load. However, there are not the detail analytical transfer functions to describe the whole physical insight regarding their small signal characteristics.

In view of the metioned above issues, the HHC control, with the combination of charge current control and hysteretic charge control, is proposed to achieve the best-in-class

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transient performance by overcoming the disadvantage of charge control and avoiding unstable condition by adding into the frequency compensation ramp [31]−[33]. It has changed the plant transfer function to an equivalent first order system characterized by a relatively stable cross frequency and small variation of DC gains, which has made the loop design easy to compensate.

In this paper, the small signal model for new LLC converter will be proposed firstly, which is not purely depend on the approach of extended describing function and the related superposition theorem, but the improved results of a third order transfer function from this theorem. In Section II, the transfer functions of the proposed model are derived and simplified for the purpose of physical insight investigation. Different from the conventional DFC control, the proposed model replaces the small signal variable of F_s by that from feedback control. In Section III and IV, the derived analytical transfer functions regarding the open loop of control to output, input to output, output impedance and that of the closed loop are verified through simulation, in which, the detail physical insight analysis are provided. In section V, the experiment of practical design is conducted to verify the proposed transfer functions. Section VI summarizes the paper.

II. Small-Signal Model for HHC Control

As shown in Fig.1, the key difference between HHC and the conventional DFC is the added feedback signal of VCR, which is a combination of the internal current ramp part and the divided scaling part from the voltage of the resonant capacitor C_s [31]−[32]. Refer to Fig. 1, VHS is the input voltage of the half bridge LLC tank, VTL and VTH come from the compensation voltage V_{comp}, they are symmetrical based on a reference voltage VCM (for example 3 V) and then will be compared with VCR. So v_{crl} and v_{crh} are produced henceforth to provide the input signal for the S/R latch, therefore, the final drive signal Gate_L and Gate_H can be produced based on another deadtime control signal for the S/R latch. As shown in Fig. 2, v_{crl} will turn high and then pull Gate_L low when VTL crosses VCR at time of t_0, then the VHS begin to rise, when the rising of VHS completes or the dead time elapses at t_1, Gate_H will turn high. At the next time of t_2 when VTH has crossed VCR, v_{crh} will turn high and then pull Gate_ H low, then the VHS begins to decrease, when VHS finishes this process or the dead time has been elapsed at t_3, Gate_L will turn high.

A. Small Signal Model for LLC HHC Control

For a conventional DFC control, the simplified analytical transfer functions have been proposed [22]−[23], in which the capacitor small signal model has turned into an inductor small signal model. So, the original small signal model of LLC tank has been simplified greatly from an above fifth-order equivalent circuit into a third-order equivalent circuit. This has provided the great possibility to extend this result

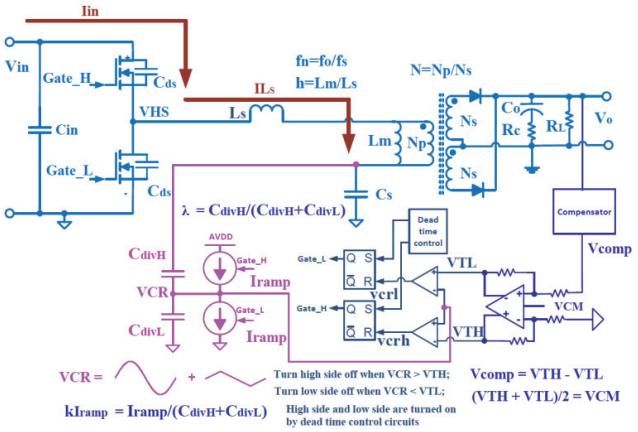

Fig. 1. The proposed HHC control used in LLC HB converter.

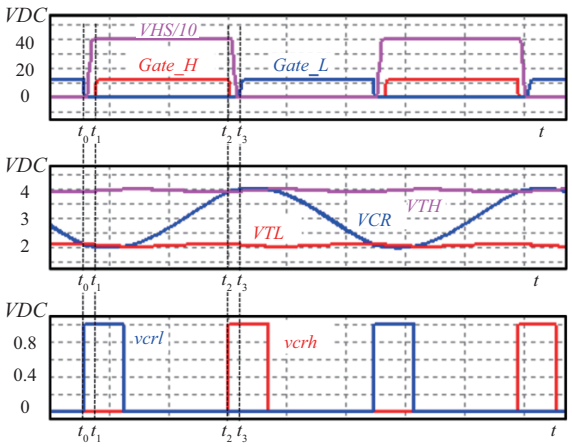

Fig. 2. Proposed hybrid hysteretic control used in LLC converter.

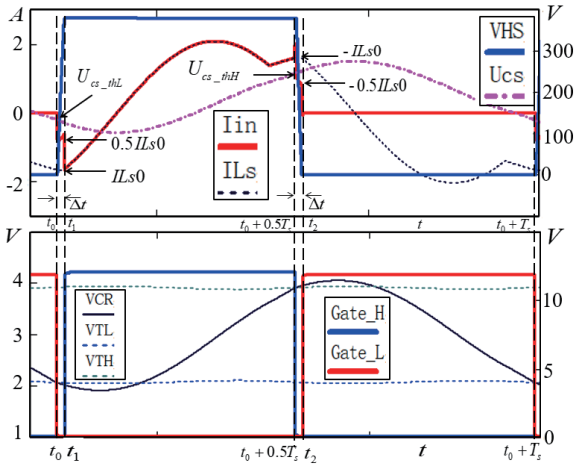

Fig. 3. Waveforms between the tank part and the VCR part for HHC control.

to other kinds of LLC control topology.

As for HHC, it is critical to investigate the key difference compared with DFC, which is the scaling voltage sense of the resonant capacitor voltage. Fig. 3 shows the key waveforms between input current I_{in}, tank current I_{Ls}, voltage of resonant capacitor U_{cs}, tank input voltage VHS, High side Gate drive Gate_H, low side Gate drive Gate_L, VCR, VTH

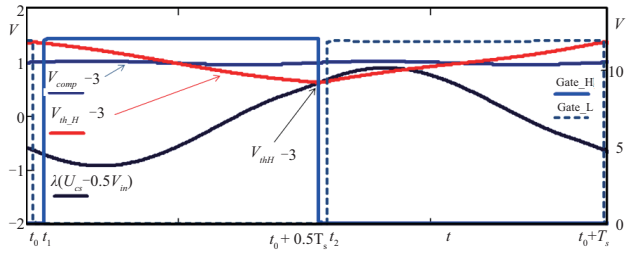

Fig. 4. Operation principle of TI HHC control with ramp current.

and VTL.

As shown in Fig. 1, the scaling voltage part in VCR is obtained from the divided voltage of C_s by the capacitors C_{divH} and C_{divL}. The scaling down coefficient can be defined as:

$$\lambda = \frac{C_{divH}}{C_{divL} + C_{divH}} \tag{1}$$

It is generally assumed the dead time Δt of the gate drives to be equal. Fig. 3 shows the details regarding the I_{in} and VHS, and then the average input current can be obtained as:

$$I_{in\_avg} = \frac{\int_{t_0}^{t_0+0.5T_s} i_{Ls}(t)\mathrm{d}t - 0.5\int_{t_0}^{t_1} i_{Ls}(t)\mathrm{d}t + 0.5\int_{t_0+0.5T_s}^{t_2} i_{Ls}(t)\mathrm{d}t}{T_s} \tag{2}$$

If defining the voltage of U_{cs} at t_0 and $t_0 + 0.5T_s$ as U_{cs_thL} and U_{cs_thH}, and the tank current as I_{Ls0} at t_0, then (2) can be re-written as:

$$\begin{aligned} I_{in\_avg} &= \frac{\int_{t_0}^{t_0+0.5T_s} i_{Ls}(t)\mathrm{d}t + 2\left|0.5I_{Ls}\ \ 0\right|\Delta t}{T_s} \\ &= \frac{\int_{t_0}^{t_0+0.5T_s} i_{Ls}(t)\mathrm{d}t + 2C_{ds}V_{in}}{T_s} \\ &= F_s(C_s(U_{cs\_thH} - U_{cs\_thL}) + 2C_{ds}V_{in}) \end{aligned} \tag{3}$$

It shows the minimum dead time is considered from (3), so the input power under steady status can be finally written as:

$$P_{in} = V_{in}F_sC_s(2U_{cs\_thH} - V_{in}) + 2C_{ds}F_sV_{in}^2 \tag{4}$$

In the configuration of HHC method products such as TI UCC25630X series, the quantity of U_{cs_thH} can be sensed by the voltage of VCR pin even though there is another combination of ramp current by the internal frequency compensation. Shown as in Fig. 4, the scaling voltage λ (U_{cs}–0.5 V_{in}) will cross th e quantity of V_{th_H}-VCM (the combined quantity of feedback and ramp current) with a value of V_{thH}-VCM when Gate_H turns off, the operation principle will be elaborated by the formulas (5)–(7).

From the operation principle of HHC control, the compensation part in terms of integrating frequency control into VCR voltage is paramount for the investigation, if we define the internal coefficient for the ramp compensation as:

$$k_{Iramp} = \frac{I_{ramp}}{C_{divL} + C_{divH}} \tag{5}$$

Then the following equations can be obtained as:

$$V_{comp} - \frac{0.25\,k_{Iramp}}{F_s} = V_{thH} \tag{6}$$

$$\lambda(U_{cs\_thH} - 0.5V_{in}) + \mathrm{VCM} = V_{thH} \tag{7}$$

If we define the conversion efficiency from primary side to secondary side as η, V_f as the average forward voltage for a rectifier on the output side, I_{sec} as the LLC tank's output current, I_o as the external load current, and $Z(s)$ as the LLC output impedance, then the following equation can be obtained if the formulas of (5)–(7) are combined into (4).

$$I_{sec} = \frac{\eta\left(V_{in}F_sC_s\dfrac{2(V_{thH} - \mathrm{VCM})}{\lambda} + 2C_{ds}F_sV_{in}^2\right)}{V_o + V_f} = I_o + \frac{V_o}{Z(s)} \tag{8}$$

In above (8), there are four variables V_o, V_{in}, V_{thH} and I_o,which are mainly with DC components but not include the switching frequency components and its harmonics, then the conventional average concept [1] can be applied to derive the related small signal small equation. For the theoretical manipulation, we can ignore the quantities of V_f and η. Perturbing on the above formula (8) with the quantities of V_o, V_{in}, V_{thH} and I_o by $\hat{v}_o$, $\hat{v}_{in}$, $\hat{v}_{thH}$, $\hat{i}_o$ respectively, we can obtain the following small signal equations:

$$\hat{v}_o = Z(s)\left(-\frac{\hat{v}_o}{R_L} + k_{th}\hat{v}_{thH} + \left(\frac{V_o}{R_LF_s} + \frac{2C_{ds}V_{in}^2}{V_o}\right)\hat{f} + k_{in}\hat{v}_{in} - \hat{i}_o\right), \tag{9}$$

where:

$$Z(s) = \frac{R_L(1 + sR_cC_o)}{1 + sR_LC_o} \qquad k_{in} = \frac{V_o}{R_LV_{in}} - \frac{2C_{ds}V_{in}F_s}{V_o} \qquad k_{th} = \frac{2C_sV_{in}F_s}{V_o\lambda}$$

Refer to Fig. 4, the small signal average concept can also be employed based on (6). Perturbing on the variables of V_{comp}, F_s and V_{thH} by $\hat{v}_{comp}$, $\hat{f}$, $\hat{v}_{thH}$, then we can obtain the following:

$$\hat{v}_{comp} + \frac{0.25\,k_{Iramp}}{F_s^2}\hat{f} = \hat{v}_{thH} \tag{10}$$

Combining (10) into (9), we have:

$$\begin{aligned} \hat{v}_o\,/\,Z(s) &= k_v\hat{v}_o + k_{th}\hat{v}_{comp} + k_f\hat{f} + k_{in}\hat{v}_{in} - \hat{i}_o \\ k_f &= \frac{V_o}{R_LF_s} + \frac{2C_{ds}V_{in}^2}{V_o} + \frac{0.5V_{in}C_sI_{ramp}}{V_oF_sC_{divH}} \end{aligned} \tag{11}$$

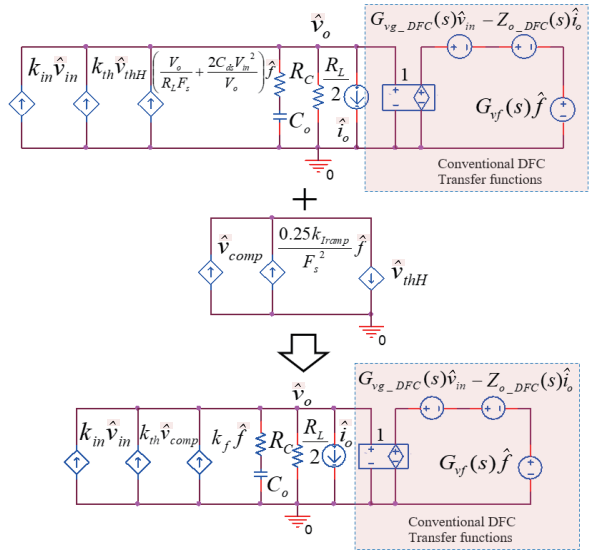

Fig. 5. Small signal equivalent circuit for the LLC HHC control.

So, the correlation in terms of small signal variables among input voltage, output voltage, compensation voltage, operation (7) frequency and external output current have been built by (11).

B. Implementation of the Analytical HHC Small Signal Transfer Function

Equation (11) shows that the small signal perturbation of the output V_o has one more of the small signal variable V_{comp} than the conventional DFC control due to the characteristic of HHC control, where the compensation feedback signal is only directly related to Vcomp but not F_s from the control block. It is taken for granted that only one variable V_{comp} is incorporated into the open loop of control to output finally, then the small signal variable of F_s is required to be cancelled in the final control block. However, it is not straightforward to implement such a behavior in the control block directly; therefore, it is required to make a mathematic manipulation from the conventional DFC control to replace the small signal variable of F_s provided that the analytic small transfer function is given. Refer to the simplified analytic transfer functions applied for a DFC control [23], the perturbation of V_o can be expressed by the open loop transfer functions of input to output $G_{vg\_DFC}(s)$, control to output $G_{vf}(s)$ and output impendence $Z_{o\_DFC}(s)$, which is shown as:

$$\hat{v}_o = G_{vg\_DFC}(s)\hat{v}_{in} + G_{vf}(s)\hat{f} - Z_{o\_DFC}(s)\hat{i}_o \tag{12}$$

Fig. 5 shows the small signal equivalent circuit for the LLC HHC control.

Even the concept of extended describing function proposed by Dr. E. Yang has been used widely for the small signal analysis both for SRC, LLC and other types of resonant converters [16], most of the models are accurate enough to make a good prediction regarding the small signal characteristic over a wide frequency range. However, most of them are featured by complicated mathematics expressions or the circuit simulation-oriented way, their analytical based

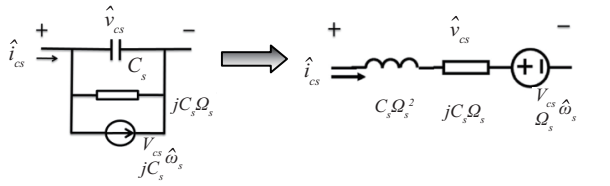

Fig. 6. Simplified equivalent small signal model for the resonant capacitor proposed by S. Tian.

formulas are still hard to be derived due to the higher order of the model. To simplify the order of the model, Shown in Fig. 6. Tian had tried to propose a simplified model successfully by turning the equivalent signal model circuit of the resonant capacitor into an equivalent model featuring inductor behavior [22]–[23], then the original small signal circuit of LLC tank has been simplified greatly from the original fifth-order equivalent circuit into a third-order one, which has provided the great possibility to obtain the analytical expression.

However, the ESR of the output capacitors is neglected due to the practical use of ceramic capacitors as far as the analytical small signal transfer function is concerned [23]. For the scenarios of using electrolytic capacitors, the ESR shall be considered. Shown in Table I, the analytical transfer functions have been modified to achieve this.

The combination of the formulas (11)–(13) will result in a final small signal transfer function shown as below:

$$\hat{v}_o(s)\left(\frac{1}{Z(s)} - \left(\frac{k_f}{G_{vf\_DFC}(s)} - \frac{1}{R_L}\right)\right) = k_{th}\hat{v}_{comp}(s) + \left(k_{in} - \frac{k_f G_{vg\_DFC}(s)}{G_{vf\_DFC}(s)}\right)\hat{v}_{in}(s) + \left(\frac{k_f Z_o(s)}{G_{vf\_DFC}(s)} - 1\right)\hat{i}_o \tag{13}$$

Then the transfer function of LLC HHC control can be obtained as follows:

$$\hat{v}_o = G_{vg\_HHC}(s)\hat{v}_{in} + G_{vc\_HHC}(s)\hat{v}_{vc} - Z_{o\_HHC}(s)\hat{i}_o \tag{14}$$

where:

$$G_{vc\_HHC}(s) = \frac{k_{th}Z(s)}{1 - Z(s)\left(\frac{k_f}{G_{vf\_DFC}(s)} - \frac{1}{R_L}\right)}$$

$$G_{vg\_HHC}(s) = Z(s)\left(k_{in} - k_f\frac{G_{vg\_DFC}(s)}{G_{vf\_DFC}(s)}\right) \Big/\!\Big/ \left(1 - Z(s)\left(\frac{k_f}{G_{vf\_DFC}(s)} - \frac{1}{R_L}\right)\right)$$

$$Z_{o\_HHC}(s) = Z(s)\left(k_{in} - k_f\frac{Z_{o\_DFC}(s)}{G_{vf\_DFC}(s)}\right) \Big/\!\Big/ \left(1 - Z(s)\left(\frac{k_f}{G_{vf\_DFC}(s)} - \frac{1}{R_L}\right)\right)$$

If we define G_{DC_vg} as the DC gain of $G_{vg\_DFC}(s)$, G_{DC_dm} and G_{DC_cm} as the DC gain of $G_{vf\_DFC}(s)$ under the conditions of $f_n \leqslant 1$ and $f_n \geqslant 1$ respectively (f_n is the normalized operation frequency), then the transfer functions of open control to output loop $G_{vc\_HHC}(s)$, open input to output loop $G_{vg\_HHC}(s)$, open output impedance $Z_{o\_HHC}(s)$ can be simplified into the analytical formula expression after the mathematic manipulations [33], which is also shown in Table II.

TABLE I
TRANSFER FUNCTIONS FOR CONVENTIONAL LLC HB CONVERTER

Transfer Functions for the Conventional DFC LLC Converter	
G_{DC_cm} $(f_n \geqslant 1)$	$\frac{V_{in} f_n h}{2F_s N} \frac{\left(\frac{1}{f_n^2} - f_n^2\right)\left(\frac{\pi^2 Q_r h}{8}\right)^2 - \left(h + 1 - \frac{1}{f_n}\right)\frac{2}{f_n^2}}{\left[\sqrt{\left(h + 1 - \frac{1}{f_n^2}\right)^2 + \left(\left(\frac{1}{f_n} - f_n\right)\frac{\pi^2 h Q_r}{8}\right)^2}\right]^3}$
G_{DC_dm} $(f_n \leqslant 1)$	$\frac{V_{in} f_n h}{2N} \frac{\left(\left(\frac{1}{f_n^2} - f_n^2\right)\left(\frac{\pi^2 Q_r h}{8}\right)^2 - \left(h + 1 - \frac{1}{f_n}\right)\frac{2}{f_n^2}\right)\frac{1}{f_n \sin\left(\frac{\pi f_n}{2}\right)}}{\left[\sqrt{\left(h + 1 - \frac{1}{f_n^2}\right)^2 + \left(\left(\frac{1}{f_n} - f_n\right)\frac{\pi^2 h Q_r}{8}\right)^2}\right]^3}$ $- \frac{V_{in} f_n h}{2N} \frac{\frac{\pi \cos\left(\frac{\pi f_n}{2}\right)}{2\sin^2\left(\frac{\pi f_n}{2}\right)}}{\sqrt{\left(h + 1 - \frac{1}{f_n^2}\right)^2 + \left(\left(\frac{1}{f_n} - f_n\right)\frac{\pi^2 h Q_r}{8}\right)^2}}$
$G_{vf\_DFC}(s)$	$G_{DC\_cm} \frac{(1 + sR_c C_o)\left(R_{eq}^2 + X_{eq}^2\right)}{\left(s^2 L_e^2 + sL_e R_{eq} + X_{eq}^2\right)(1 + sR_L C_o) + R_{eq}(sL_e + R_{eq})(1 + sR_c C_o)}$ $(f_n \geqslant 1)$ $G_{DC\_dm} \frac{1 + sR_c C_o}{1 + \frac{s}{Q_p \omega_p} + \frac{s^2}{\omega_p^2}}$ $(f_n \leqslant 1)$
G_{DC_vg}	$\frac{1}{2N} \frac{1}{\sqrt{\left(h + 1 - \frac{1}{f_n^2}\right)^2 + \left(\left(\frac{1}{f_n} - f_n\right)\frac{\pi^2 h Q_r}{8}\right)^2}}$ $(f_n \geqslant 1)$ $\frac{1}{2N\sin\left(\frac{\pi f_n}{2}\right)} \frac{h}{\sqrt{\left(h + 1 - \frac{1}{f_n^2}\right)^2 + \left(\frac{1}{\sin\left(\frac{\pi f_n}{2}\right)}\left(\frac{1}{f_n} - f_n\right)\frac{\pi^2 h Q_r}{8}\right)^2}}$ $(f_n \leqslant 1)$
$G_{vg\_DFC}(s)$	$G_{DC\_vg} \frac{(1 + sR_c C_o)\left(sL_e R_{eq} + R_{eq}^2 + X_{eq}^2\right)}{\left(s^2 L_e^2 + sL_e R_{eq} + X_{eq}^2\right)(1 + sR_L C_o) + R_{eq}(sL_e + R_{eq})(1 + sR_c C_o)}$ $(f_n \geqslant 1)$ $G_{DC\_vg} \frac{1 + sR_c C_o}{1 + \frac{s}{Q_p \omega_p} + \frac{s^2}{\omega_p^2}}$ $(f_n \leqslant 1)$
$Z_{o\_DFC}(s)$	$R_L \frac{(1 + sR_c C_o)\left(s^2 L_e^2 + sL_e R_{eq} + X_{eq}^2\right)}{\left(s^2 L_e^2 + sL_e R_{eq} + X_{eq}^2\right)(1 + sR_L C_o) + R_{eq}(sL_e + R_{eq})(1 + sR_c C_o)}$ $(f_n \geqslant 1)$ $\frac{\pi^2 L_e}{8N^2} \frac{s(1 + sR_c C_o)}{1 + \frac{s}{Q_p \omega_p} + \frac{s^2}{\omega_p^2}}$ $(f_n \leqslant 1)$

$$L_e = \begin{cases} L_s\left(1 + \frac{1}{f_n^2}\right) & (f_n \geqslant 1) \\ L_s\left(1 + \frac{1}{f_n^2}\right) + L_m(1 - f_n) & (f_n \leqslant 1) \end{cases} \qquad \omega_p = \sqrt{\frac{8N^2}{L_e C_o \pi^2 \left(1 + \frac{\pi R_c}{\sqrt{8} R_L}\right)}} \qquad R_{eq} = \frac{8N^2 R_L}{\pi} \qquad h = \frac{L_m}{L_s}$$

$$Q_p = \sqrt{R_L + \frac{\pi R_c}{\sqrt{8}}} \cdot \frac{8\pi N \sqrt{L_e C_o R_L}}{16\sqrt{2} N^2 R_L C_o R_c + \pi^3 L_e} \qquad X_{eq} = 2\pi F_s C_s - \frac{1}{2\pi F_s C_s} \qquad Q_r = \sqrt{\frac{L_s}{C_s}} \frac{1}{R_L N^2} \qquad f_n = \frac{F_s}{F_o}$$

TABLE II
TRANSFER FUNCTIONS FOR LLC HHC HB CONVERTER

Open Loop Transfer Functions for the HHC LLC Converter		
$G_{vc\_HHC}(s)$	$\dfrac{k_{th}}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_dm}}}\dfrac{1+sR_cC_o}{1+s\dfrac{C_o\left(1+\dfrac{R_c}{R_L}\right)-\dfrac{k_f}{G_{DC\_dm}Q_p\omega_p}}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_dm}}}+\dfrac{s^2}{\omega_p^2\left(1-\dfrac{2G_{DC\_dm}}{R_Lk_f}\right)}}$	$(f_n\leqslant 1)$
	$\dfrac{k_{th}}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_cm}}}\dfrac{1+sR_cC_o}{1+\dfrac{s}{\omega_1}+\dfrac{s^2}{\omega_2}+\dfrac{s^3}{\omega_3}}$	$(f_n\geqslant 1)$
$G_{vg\_HHC}(s)$	$\dfrac{k_{in}-k_f\dfrac{G_{DCvg}}{G_{DC\_dm}}}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_dm}}}\dfrac{1+sR_cC_o}{1+s\dfrac{C_o\left(1+\dfrac{R_c}{R_L}\right)-\dfrac{k_f}{G_{DC\_dm}Q_p\omega_p}}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_dm}}}+\dfrac{s^2}{\omega_p^2\left(1-\dfrac{2G_{DC\_dm}}{R_Lk_f}\right)}}$	$(f_n\leqslant 1)$
	$\dfrac{\left(k_{in}-k_f\dfrac{G_{DCvg}}{G_{DC\_cm}}\right)}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_cm}}}\dfrac{(1+sR_cC_o)\left(1+s\dfrac{G_{DCvg}L_eR_{eq}k_f}{\left(R_{eq}^2+X_{eq}^2\right)\left(k_fG_{DCvg}-k_{in}G_{DC\_cm}\right)}\right)}{1+\dfrac{s}{\omega_1}+\dfrac{s^2}{\omega_2}+\dfrac{s^3}{\omega_3}}$	$(f_n\geqslant 1)$
$Z_{o\_HHC}(s)$	$\dfrac{1}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_dm}}}\dfrac{(1+sR_cC_o)\left(1+s\dfrac{(-k_f)L_e\pi^2}{8N^2}\right)}{1+s\dfrac{C_o\left(1+\dfrac{R_c}{R_L}\right)-\dfrac{k_f}{G_{DC\_dm}Q_p\omega_p}}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_dm}}}+\dfrac{s^2}{\omega_p^2\left(1-\dfrac{2G_{DC\_dm}}{R_Lk_f}\right)}}$	$(f_n\leqslant 1)$
	$\dfrac{\left(1-\dfrac{k_fR_LX_{eq}^2}{G_{DC\_cm}\left(R_{eq}^2+X_{eq}^2\right)}\right)}{\dfrac{2}{R_L}-\dfrac{k_f}{G_{DC\_cm}}}\dfrac{(1+sR_cC_o)\left(1+\dfrac{s}{\omega_4}+\dfrac{s^2}{\omega_5}\right)}{1+\dfrac{s}{\omega_1}+\dfrac{s^2}{\omega_2}+\dfrac{s^3}{\omega_3}}$	$(f_n\geqslant 1)$

$$\omega_1=\frac{\left(R_{eq}^2+X_{eq}^2\right)\left(\dfrac{2G_{DC\_cm}}{R_Lk_f}-1\right)}{\left(1+\dfrac{R_c}{R_L}\right)\dfrac{G_{DC\_cm}C_o}{k_f}\left(R_{eq}^2+X_{eq}^2\right)-2R_{eq}L_e-R_LC_oX_{eq}^2-R_cC_oR_{eq}}$$

$$\omega_2=\frac{\left(R_{eq}^2+X_{eq}^2\right)\left(1-\dfrac{2G_{DC\_cm}}{R_Lk_f}\right)}{L_e^2+L_eR_LC_oR_{eq}+R_{eq}L_eR_cC_o}\qquad \omega_3=\frac{\left(R_{eq}^2+X_{eq}^2\right)\left(1-\dfrac{2G_{DC\_cm}}{R_Lk_f}\right)}{L_e^2R_cC_o}$$

$$\omega_4=\frac{G_{DC\_cm}\left(R_{eq}^2+X_{eq}^2\right)-k_fR_LX_{eq}^2}{R_{eq}L_eR_L(-k_f)}\qquad \omega_5=\frac{G_{DC\_cm}\left(R_{eq}^2+X_{eq}^2\right)-k_fR_LX_{eq}^2}{L_e^2R_L(-k_f)}$$

$$k_{th}=\frac{2C_sV_{in}F_s}{V_o\lambda}\quad k_{in}=\frac{V_o}{R_LV_{in}}-\frac{2C_{ds}V_{in}F_s}{V_o}\quad k_f=\frac{V_o}{R_LF_s}+\frac{2C_{ds}V_{in}^2}{V_o}+\frac{0.5V_{in}C_sI_{ramp}}{V_oF_sC_{divH}}$$

III. Verification on the Analytical Transfer Funcntions

The small signal characteristic of LLC HHC converter will be fully verified and investigated in this section through simulation based on a design example with major power stage parameters setting by: V_{in} = 370 VDC−410 VDC, V_o = 24 VDC, R_L = 2 Ω, L_m = 330 uH, L_s = 50 uH, C_s = 44 nF, C_o = 470 uF×4, R_c = 24 mΩ/4, N = Np/Ns = 25/3. The related SIMPLIS simulation is used based on the circuits shown as in Fig. 7.

A. Verification and Analysis on the Transfer Function of Open Control to Output

Based on the transfer functions presented in Table I and Table II, the open loop transfer functions for the HHC control for the UCC25630X products can be verified further by using the same approach, in which the related small signal plots regarding the open control to output under the scenarios of $f_n > 1$ and $f_n < 1$ are obtained through calculation. To have a contrast, the simulation is conducted. As shown in Fig. 8, the results between SIMPLIS simulation and calculation are given under the input condition of 370 VDC and 410 VDC with the output being 24 VDC&12 A. The dashed lines show the simulation results and the solid lines show the calculation results.

It is shown from Fig. 8 that the calculation results match well with the simulation results in both the conditions. However, the calculation results do not match the simulation results well when frequency increases up to half of the operation frequency due to the simplified third-order of the model and the incorporated average concept, but it does not have any impact on the practical prediction.

In order to investigate the characteristic of HHC and the advantage over the conventional hysteretic control, the DC gain of $G_{vc}(s)$ for these two approaches are analyzed. Refer to Table I, the DC gain of $G_{vc}(s)$ can be simplified as:

$$Gdc_{vc\_HHC} = \frac{\dfrac{2C_s V_{in} F_s}{V_o \lambda}}{\dfrac{2}{R_L} - \left(\dfrac{V_o}{R_L} + \dfrac{V_{in}}{V_o} k_{Iramp}\right)\dfrac{1}{G_{DC\_vf} F_o f_n}} = \frac{\dfrac{4NC_s F_o f_n}{G_{DC\_vg}\lambda}}{\dfrac{2}{R_L} + \left(\dfrac{V_o}{R_L} + \dfrac{2k_{Iramp}N}{G_{DC\_vg}}\right)\dfrac{1}{(-G_{DC\_vf})F_o f_n}} \tag{15}$$

While

$$G_{DC\_vf} = \begin{cases} G_{DC\_cm} & (f_n \geq 1) \\ G_{DC\_dm} & (f_n \leq 1) \end{cases} \qquad k_{Iramp} = \frac{C_s \cdot 10^{-3}}{C_{divH}}$$

For the HHC, the DC Gain will be inversely proportional to λ from (15), another variable is k_{Iramp}, in which the variable

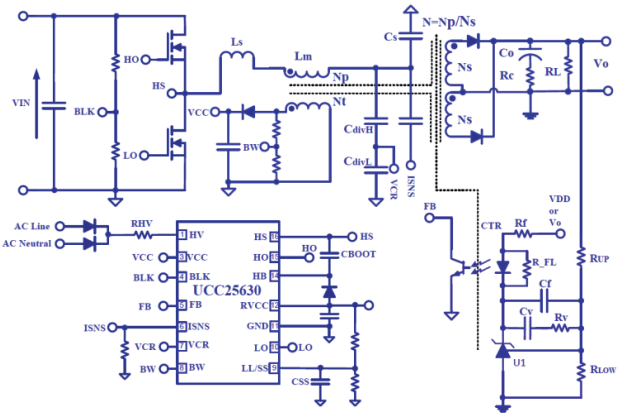

Fig. 7. Circuit for the simulation verification (dead time is set as 200 ns).

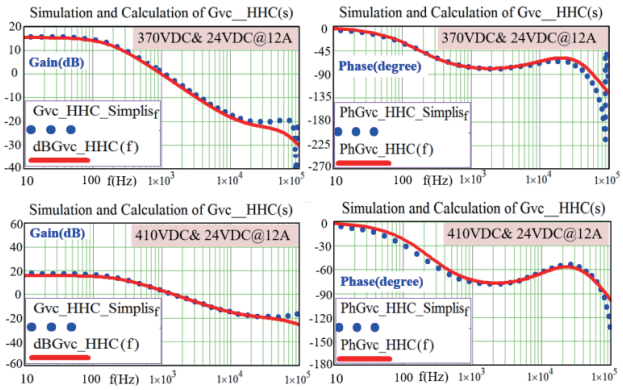

Fig. 8. Plot comparison of control to output between simulation and calculation under the condition of 370 VDC@24 VDC&12 A (f_n = 0.82) and 410 VDC (f_n = 1.08) @24 VDC&12 A.

of I_{ramp} has been incorporated. However, it is not the case for the conventional charge control. So, the difference can be found through the approximate DC gain plot referring to the variables of R_L and f_n. Shown in (16), the normal constant of k_{Iramp} can be removed and the DC gain for the conventional charge control can be obtained.

$$Gdc_{vc\_HHC}(R_L, f_n) = \frac{\dfrac{4NC_s F_o f_n}{G_{DC\_vg}(R_L, f_n)\lambda}}{\dfrac{2}{R_L} + \left(\dfrac{V_o}{R_L} + \dfrac{2k_{Iramp}N}{G_{DC\_vg}(R_L, f_n)}\right)\dfrac{1}{(-G_{DC\_vf}(R_L, f_n))F_o f_n}} \tag{16}$$

With the incorporation of $G_{DC\_vg}(R_L, f_n)$ and $G_{DC\_vf}(R_L, f_n)$ shown in Table I, the approximate DC gain plot between the HHC control and the conventional hysteretic charge (HC) control can be illustrated in Fig. 9. To have the investigation on the DC gain over a practical design input voltage range, the plotting under different output load for HHC control is shown in the left part of Fig. 9, where three items of the curve tendency can be observed: firstly, the overall DC gain is proportional to V_{in} under a certain output load even though there is a special case when f_n is below 1, in which the gain will not decrease at once but it will decrease finally with respect to the decreasing of f_n. Secondly, the

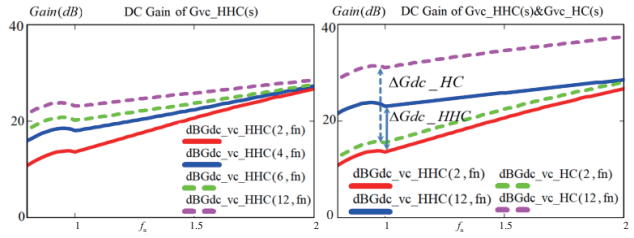

Fig. 9. DC gain plot comparison between the HHC and the conventional hysteretic charge control.

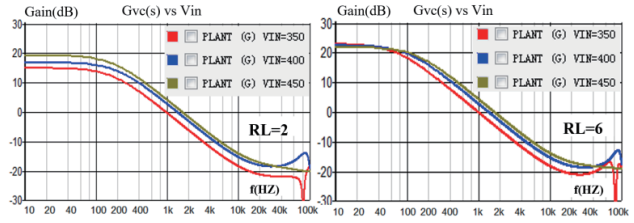

Fig. 10. Loop simulation of control to output when the input voltage varies.

gain will decrease when more of the output current is loaded, which means it will increase under a light load condition. To the third, the delta value of DC gain under those two different load conditions will decrease when f_n is increased. As shown in the right part of Fig. 9, we can obtain the comparison results between proposed HHC control and conventional hysteric charge control: firstly, it is concluded that the gain in HC control is with the similar operation discipline, it will increase when f_n increases under a certain output current, but the delta value of DC gain under those two conditions is different. Refer to right part of Fig. 9, the solid line and the dashed line represent the plot curves of HHC control and HC control respectively, it shows the DC gain of HC control nearly approaches that of HHC control under full load condition, but it increases more under light load condition. As a conclusion, the control design for a conventional hysteric charge control still faces some challenges if compared to HHC control.

To verify this conclusion, the simulation is conducted under two different output load conditions of $R_L = 2\ \Omega$ and $6\ \Omega$ when input voltage is varied from 350 VDC to 450 VDC. Shown as in Fig. 10, it can be observed that the DC gain follows the similar operation discipline concluded above: the gain will decrease as output load increases from $R_L = 6\ \Omega$ to $R_L = 2\ \Omega$, the delta value of the gain under a same varied input range will decrease as output load decreases from $R_L = 2\ \Omega$ to $R_L = 6\ \Omega$.

Fig. 11 shows another investigation when the output varies under a certain input, it can be concluded that the DC gain of the Gvc(s) has some small variation under the rated output load, the lower the input voltage is, the lower the gain can be obtained. From another point of review, the DC gain will decrease with the increase of output load under these two input conditions, the delta value of the gain under a same varied output load range will decrease with the increase of input voltage.

It shows from Figs.10–11 that the cross frequency for the closed loop shall be below the zero of output electrolytic capacitors and also required to avoid the impact range of high frequency dynamics occurring behavior. In order

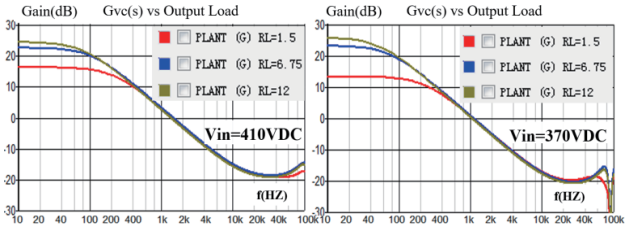

Fig. 11. Sweep of control to output when output current varies.

to yield an easy design for the compensation circuit, the transfer function of open control to output is required to be simplified. Take the scenario of $f_n \geqslant 1$, for example, if the high order poles shown in $G_{vc}(s)$ are neglected, then the transfer function of open control to output can be simplified further as follows:

$$G_{vc\_HHC\_design}(s) \approx \frac{k_{th}}{\frac{2}{R_L} - \frac{k_f}{G_{DC\_cm}}} \frac{1 + sR_c C_o}{1 + \frac{s}{\omega_1}} \quad (f_n \geqslant 1) \tag{17}$$

The cross frequency can be approximated as:

$$f_{c\_Gvc} = \frac{\omega_1}{2\pi} \frac{k_{th}}{\frac{2}{R_L} - \frac{k_f}{G_{DC\_cm}}} = \frac{1}{2\pi} \frac{k_{th}/k_f}{\frac{C_o}{k_f} - \frac{2R_{eq}L_e + R_L C_o X_{eq}^2}{G_{DC\_cm}\left(X_{eq}^2 + R_{eq}^2\right)}} \tag{18}$$

The above (18) can be further simplified as:

$$f_{c\_Gvc} = \frac{1}{2\pi} \frac{\frac{k_{th}}{k_f}}{\frac{C_o}{k_f} - \delta(R_L, f_n)}$$

$$\delta(R_L, f_n) = \frac{R_L L_s f_n h\left(\frac{16N^2}{\pi^2} + \frac{C_o}{C_s}\left(f_n - \frac{1}{f_n}\right)^2\right)}{2V_o\left(\frac{L_s}{C_s}\left(f_n - \frac{1}{f_n}\right)^2 + R_L^2\left(\frac{8N^2}{\pi^2}\right)^2\right)} \tag{19}$$

The investigation regarding the cross frequency on (19) has been revealed that the factor $\delta(R_L, f_n)$ is much smaller than the value of the variable C_o/k_f in the practical application, then the cross frequency can be simplified further as:

$$f_{c\_Gvc} \approx \frac{1}{2\pi} \frac{k_{th}}{C_o} = \frac{C_s V_{in} F_s}{\pi \lambda V_o C_o} \tag{20}$$

Equation (20) shows that the cross frequency for the open control to output is firmly related to the operation frequency no matter whatever the output load is, which can be verified from the results shown in Fig. 11, where the cross frequency is proved not to be affected by the output load directly.

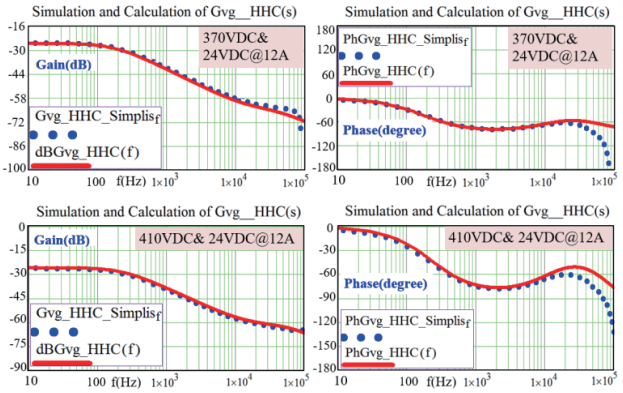

Fig. 12. Plot comparison of input to output between simulation and calculation under the condition of 370 VDC@24 VDC&12 A (f_n = 0.82) and 410 VDC (f_n = 1.08) @24 VDC&12 A.

Another scenario of $f_n \leqslant 1$ can also be verified by using the same approach mentioned above. With this characteristic, it is concluded that the compensation circuit can be easily designed for the HHC control.

B. Verification and Analysis on the Analytical Transfer Function of Audio Susceptibility

To investigate the audio susceptibility, the plot of open transfer function of the input to output is carried out. Fig. 12 illustrates such a result comparison between simulation and calculation in both the input condition of 370 VDC and 410 VDC. It is revealed that the mathematical calculation results match well with the simulation results except the occurrence of the error when the frequency goes up to half of the operation frequency.

As shown in Fig. 12, it can be seen the gain decreases more after the first poles ω_T ($f_n \leqslant 1$) and ω_1 ($f_n \geqslant 1$). As for the practical applications where the ripple frequency of PFC is around 100 Hz, the closed audio acceptability shall be firmly related to the DC gain of the transfer function. Equation (21) shows the formulas of the DC gain based on the variables of output load and the normalized frequency, the approximated gain can be obtained by (22) at the operation condition of the resonant frequency. As for the conventional HC control, the DC gain can be obtained by setting k_{ramp} as zero based on (21)–(22).

$$G_{DC\_vg\_HHC}(R_L, f_n) = \frac{\dfrac{G_{DC\_vg}(R_L, f_n)}{2N \cdot R_L} - \left(\dfrac{V_o}{R_L} + \dfrac{2k_{Iramp}N}{G_{DC\_vg}(R_L, f_n)}\right) \cdot \dfrac{G_{DC\_vg}(R_L, f_n)}{2f_n F_o N G_{DC\_vf}(R_L, f_n)}}{\dfrac{2}{R_L} + \left(\dfrac{V_o}{R_L} + \dfrac{2k_{Iramp}N}{G_{DC\_vg}(R_L, f_n)}\right) \dfrac{1}{(-G_{DC\_vf}(R_L, f_n))f_n F_o}} \tag{21}$$

$$DC_{\_Gvg\_HHC\_fo} \approx \frac{V_o + \left(V_o + \dfrac{V_{in}k_{Iramp}}{I_o}\right)\dfrac{h}{2}}{2V_{in} + N\left(V_o + \dfrac{V_{in}k_{Iramp}}{I_o}\right)h} \tag{22}$$

Fig. 13 illustrates the operation principle regarding the DC gain versus output load for both the conditions under HHC control and HC control. It is revealed that the gain decreases with the increase of V_{in} or output current for HHC control. As shown in the left part of Fig. 13, the gain is with small variation when LLC operators near the resonant frequency (f_n = 1) during the load range of 2 A to 12 A. However, it drops much as the output current increases. As a contrast, the gain nearly remains the same when LLC operates below the resonant frequency point (f_n < 1) for the conventional HC control and the overall variation shall be relatively smaller than that in the HHC control.

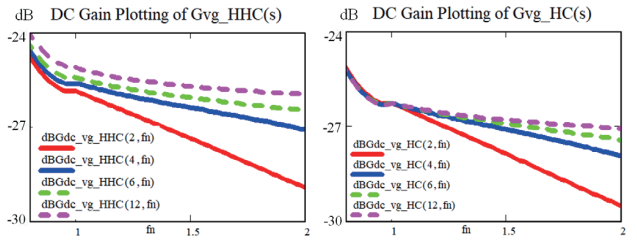

Fig. 13. DC gain plot of input to output under HHC control and conventional HC control.

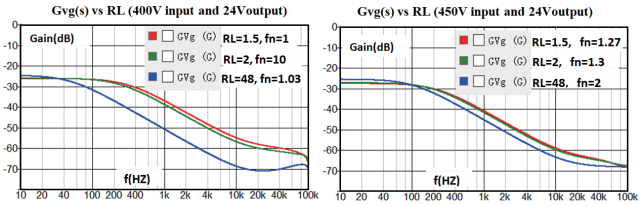

Fig. 14. Plot of input to output under the variation of output load.

To verify this principle for HHC control, the simulation is implemented to make load sweep analysis based on the transfer function of $G_{vg\_HHC}(s)$ when input is 400 VDC and 450 VDC respectively. As shown in Fig. 14. the DC gain increases as output current decreases for both conditions, which matches the result obtained from Fig. 13, the overall variation is small when LLC operates at the resonant frequency point and the gain at 450 VDC is relatively smaller than that of the condition at 400 VDC, which is consistence with the calculation result in (21). With this analysis, we can refer to (22) for the further physical insight analysis regarding the practical design as far as the closed transfer function is concerned.

C. Close the Voltage Loop

Based on the good match between theoretical calculation and simulation for the open loop control-to-output transfer function, the feedback voltage loop can be constructed for the overall closed loop stabilization. Fig. 15 shows two kinds of compensation circuit regarding the way of R_f's power connection, one way is connecting to the output V_o, another way is connecting to a regulated voltage VDD. In this paper, let's take the second connection way for example, in which only the DC gain of the OPTO is considered to have a simple transfer function derivation for the compensation circuit.

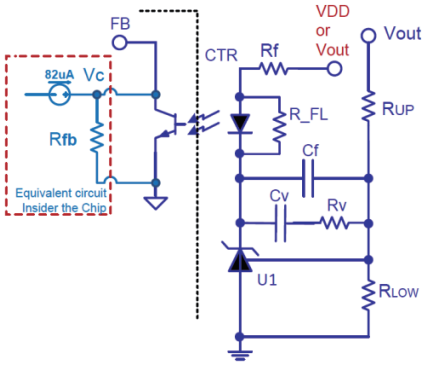

Fig. 15. Feedback circuit for the loop compensation.

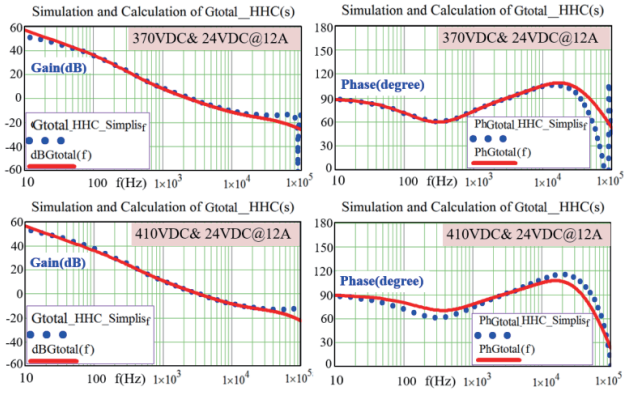

Fig. 16. Overall loop plot comparison between simulation and calculation under the condition of 370 VDC@24 VDC&12 A (f_n = 0.82) and 410 VDC (f_n = 1.08) @24 VDC&12 A.

Shown in Fig. 15, the parameters are set by R_{up} = 97.7 kΩ, R_v = 60 kΩ, C_v = 4.7 nF, R_f = 5 kΩ, C_f = 20 pF, and CTR = 0.35. Care need to be taken that the additional soft ramp circuit for the purpose of avoiding the output overshot may be suggested to add in the practical design. As for the UCC25630x series, it is specially noted that the equivalent circuit consist of 82 uA inner current source and R_{fb} insider the chip shall be considered to form a whole compensation circuit. Since V_{comp} in $G_{vc\_HHC}(s)$ is 0.5 times of the voltage on R_{fb} inside the chip from Table II, we can use this value for the calculation. So, the transfer function for the compensation circuit can be obtained as:

$$G_{cv}(s) = \frac{R_{fb}\,\mathrm{CTR}}{R_f} \frac{1}{(C_v + C_f)\cdot R_{up}} \frac{1 + R_v C_v s}{\left(1 + \dfrac{s\cdot R_v C_v C_f}{C_v + C_f}\right)s} \quad (23)$$

The overall loop is then obtained as follows:

$$G_{total}(s) = G_{vc\_HHC}(s)\, G_{cv}(s) \quad (24)$$

Fig. 16 shows the plot comparison of the overall loop between simulation and calculation under the input condition of 370 VDC and 410 DC respectively.

It shows the good matched result between the simulation and calculation can be achieved within a wide range of frequency, in which both the cross frequency and phase margin are nearly the same. The cross frequency of the closed loop is nearly in proportion to the operation frequency in these two conditions.

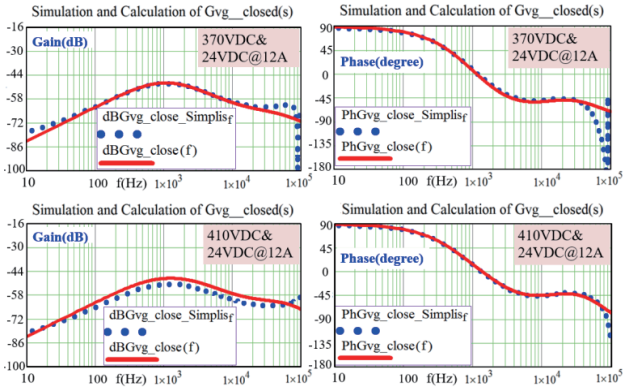

Fig. 17. Results comparison of closed audio susceptibility between simulation and calculation under the condition of 370 VDC@24 VDC&12 A (f_n = 0.82) and 410 VDC (f_n = 1.08) @24 VDC&12 A.

IV. Characteristics Under Line Change and Load Change

A. The Closed Audio Susceptibility and Characteristic of AC Ripple Rejection

Based on $G_{vg\_HHC}(s)$ shown in Table I, the closed audio susceptibility can be obtained as follows:

$$G_{vg\_closed}(s) = \frac{G_{vg\_HHC}(s)}{1 + G_{vc\_HHC}(s)\cdot G_{cv}(s)} \quad (25)$$

To verify the result at the condition of 12 A output, the comparison between simulation and calculation under 370 VDC and 410 VDC can be obtained as shown in Fig. 17.

It can be seen the good matched results can be achieved between the simulation and calculation and then it can be proposed to evaluate converter's line regulation by applying into the time domain.

To characterize the input voltage rejection, the PFC input voltage is applied by a combinated value of DC part and AC ripple part. Based on the AC line frequency of F_{line}, the AC voltage part can be written as:

$$V_{in\_AC}(t) = V_{PFC\_AC}\,\sin(2\pi F_{line} t) \quad (26)$$

So, the corresponding output voltage can be calculated as:

$$V_{o\_in}(t) = V_{o\_DC} + V_{in\_AC}(t)\, G_{vg\_closed}(j\cdot 2\pi F_{line}) \quad (27)$$

Take the condition of $f_n > 1$ for example, when the input varies from 405 V to 425 V based on an AC line frequency of 100 Hz, the calculation result of output from (27) is shown in the right part of Fig. 18, it reveals the average variation of

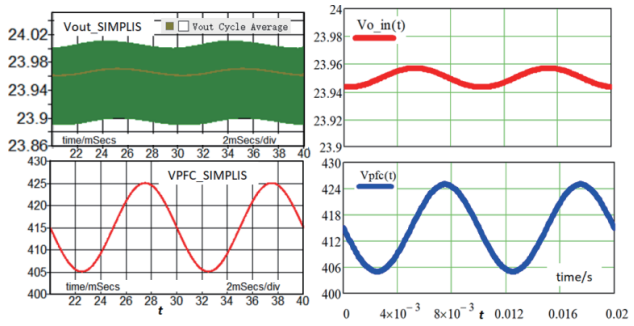

Fig. 18. Comparison of the output between calculation and simulation, in which PFC is with a 20 VAC ripple based on the input of 415 VDC.

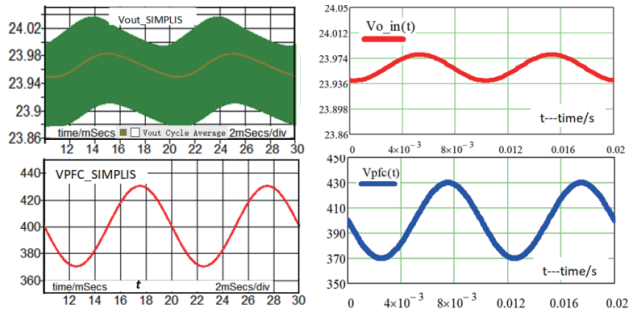

Fig. 19. Comparison of output between calculation and simulation when PFC is with 60 V's AC ripple based on 400 VDC input.

output ripple is only 20 mVDC, which is consistent with the result of simulation shown in the left part of Fig. 18.

To demonstrate the input ripple rejection characteristic further, a big ripple of 60 VAC is applied based on the 400 VDC under the same line frequency, the comparison results between simulation and calculation are obtained as shown in Fig. 19, which is observed that the output variation from the calculation is 38 mV, which matches well with the simulation result.

So, it is concluded that the LLC HHC control has the advantage over the conventional DFC control regarding the input voltage rejection, which means the decreased value of PFC electrolytic capacitors for HHC control will not affect the performance of output characteristic.

B. The Closed Output Impedance and Dynamic Load Transient Characteristic

Since the transfer function of open output impedance is derived in Table II, it can be used to obtain the closed output impedance, which is shown as:

$$Z_{\text{out\_closed}}(s)=\left.\frac{\Delta v_{\text{o}}}{\Delta i_{\text{o}}}\right|_{\text{closed}}=\frac{-Z_{\text{o\_HHC}}(s)}{1+G_{\text{vc\_HHC}}(s)G_{\text{cv}}(s)} \tag{28}$$

The comparison between simulation and calculation under the input condition of 370 VDC and 410 VDC and the output condition of 24 VDC&12 A can be obtained from Fig. 20. It shows the results match well over a wide frequency range,

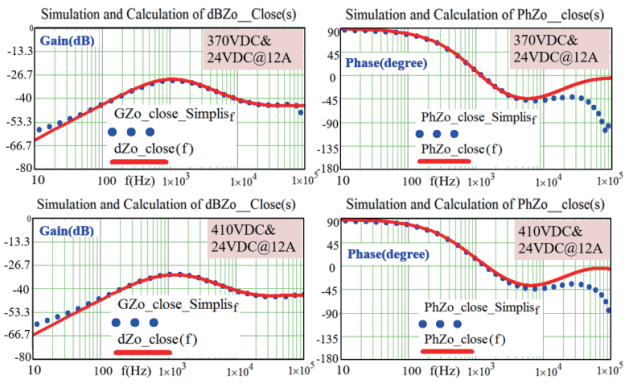

Fig. 20. The plot comparison of closed output impendence between simulation and calculation under the condition of 370 VDC@24 VDC&12 A (f_{n} = 0.82) and 410 VDC (f_{n} = 1.08) @24 VDC&12 A.

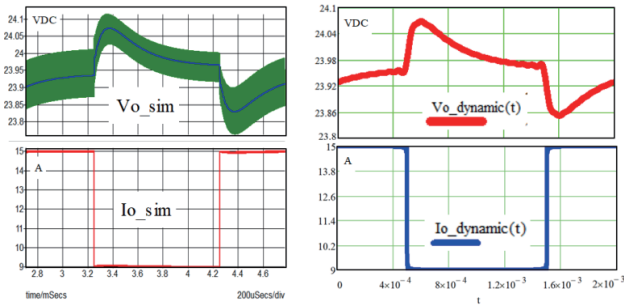

Fig. 21. Results comparison between simulation and calculation under the condition of 410 VDC input and 24 VDC&9 A−15 A−9 A output.

especially for the bode plot. However, there is some variation for the phase plot comparison when frequency approaches the operation frequency. Further investigation shows it is caused by the non-precise zeros of $Z_{\text{o\_HHC}}(s)$ occurred in the high frequency range due to the averaged concept employing on a simplified LLC tank model [22]−[23], which has been hard for us to obtain the precise high frequency dynamics. However, the phase calculation will match the simulation well if the high frequency zeros are assumed high beyond the operation frequency. Then the closed output load dynamic response can be investigated through the conversion from frequency domain into time domain based on (28).

Since the dynamic step load can be simplified by a squared wave with a certain repetition frequency f_{ts}, the equation for the square wave under the transient frequency f_{ts} can be expressed as a Fourier series, which is given by:

$$i_{\text{o\_dynamic}}(t)=\frac{2I_{\text{step}}}{\pi}\cdot\sum_{n=1}^{\infty}\frac{(-1)^{n=1}}{2n-1}\cos\left((2n-1)\cdot 2\pi f_{ts}t\right) \tag{29}$$

where I_{step} is the load step and the corresponding output voltage can be calculated as:

$$V_{\text{o\_dynamic}}(t)=V_{\text{o}}+i_{\text{o\_dynamic}}(t)\,Z_{\text{out\_closed}}(j\cdot 2\pi f_{ts}) \tag{30}$$

Fig. 21 shows the comparison results between simulation and calculation under the input condition of 410 VDC and

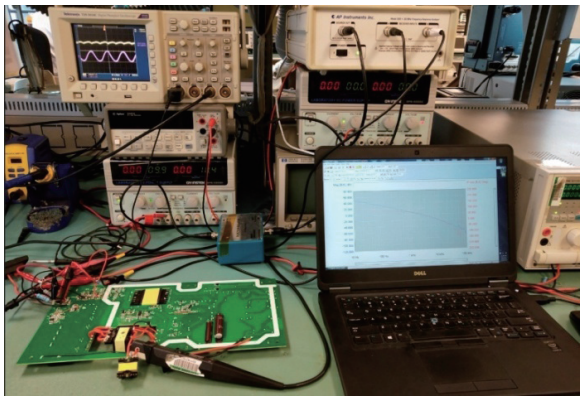

Fig. 22. The loop verification platform based on a TV power board.

TABLE III
PARAMETERS OF LLC CONVERTER FOR THE EXPERIMENT

Parameter	Description	Value
V_{in}	Nominal input PFC voltage [VDC]	398
V_o	Nominal output voltage [VDC]	12
I_{o_max}	Maximum output current [A]	12
C_s	Resonant Tank capacitor [nF]	27
L_s	Resonant Tank conductance [uH]	107
L_m	Magnetizing conductance [uH]	840
N	Transformer ratio Np/Ns [uH]	32/2
C_{divH}	U_{CS} scaling capacitor (upside) [pF]	82
C_{divL}	U_{CS} scaling capacitor (downside) [nF]	8.2
C_o	Output capacitor [uF]	330×5
R_c	ESR of output capacitor [mR]	28/5
CTR	CTR of OPTO	0.4

the output load condition of 24 VDC&9 A–15 A–15 A. It can be observed that the result of calculation matches well with the simulation result.

V. EXPERIMENTAL VERIFICATION

Shown as in Fig. 22, the proposed analytical small signal transfer functions regarding the open control to output loop and the closed overall loop can be verified further through the experiment on a 70″250 W TV power board by using UCC256304, in which, the output is 12 VDC&12 A. The main design parameters are given in Table III.

Based on the dead time setting of 200 ns, the operating frequency on the design board is: 94.3 kHz for 2 A, 90.5 kHz for 4 A, 89.6 kHz for 5 A, 88.5 kHz for 6 A, 86.5 kHz for 8 A and 86.3 kHz for 10 A. The steady operation waveforms are shown in Fig. 23, in which the output ripple and the current though the resonant inductor are given. For the loop measurement, the AP instruments Model 300 is used as shown in Fig. 22. In order to obtain the plant loop, a 50 kΩ resistor is used to be in series with the lower output side of the OPTO FOD817A for the V_c pin measurement.

The open loop of power plant stage can be measured from UCC256304's FB voltage, which is actually located on the terminal of the added 50 kΩ resistor from the lower output side of FOD817A. Fig. 24 shows the plot comparison results between the measurements and the calculations when it

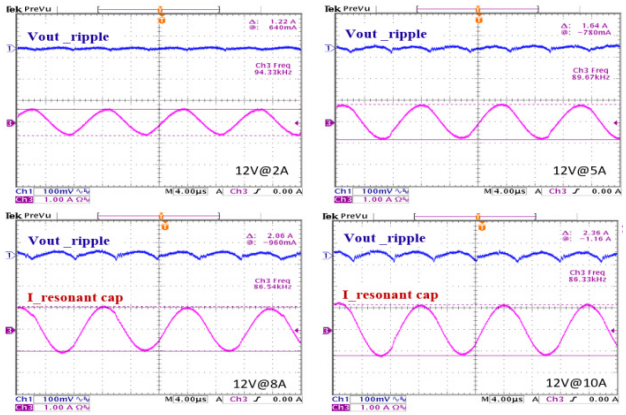

Fig. 23. Waveforms of output ripple and current of resonant tank under the output condition of 12 VDC @2 A, 5 A, 8 A and 10 A.

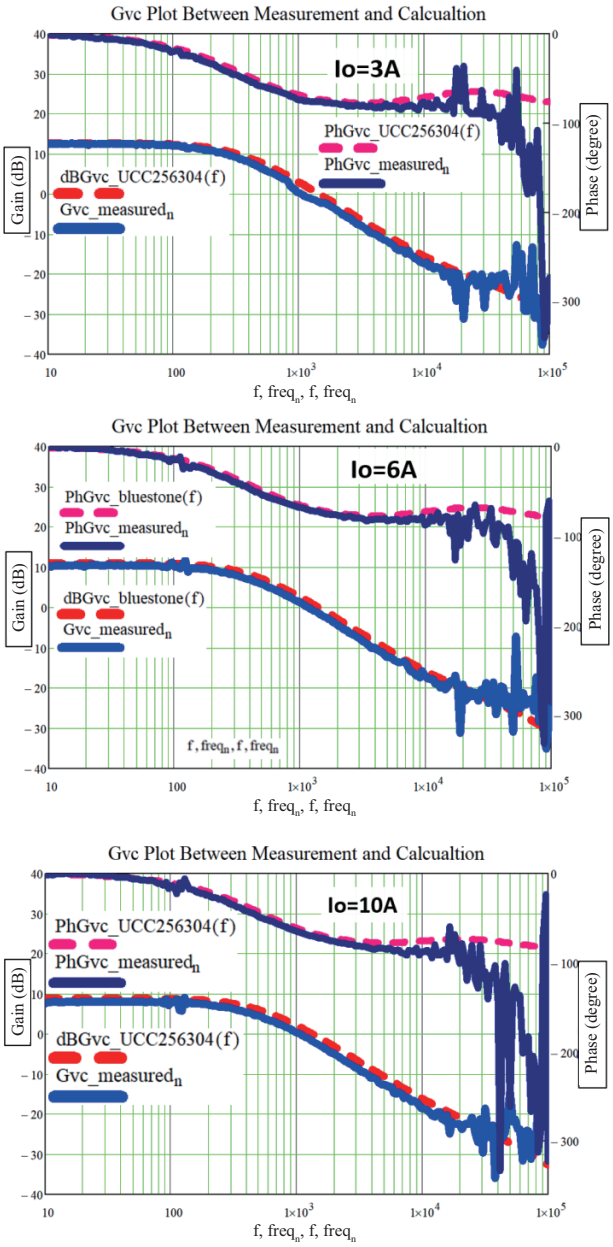

Fig. 24. Control to output plot comparison between measurement and calculation under the steady operation of 3 A, 6 A and 10 A output.

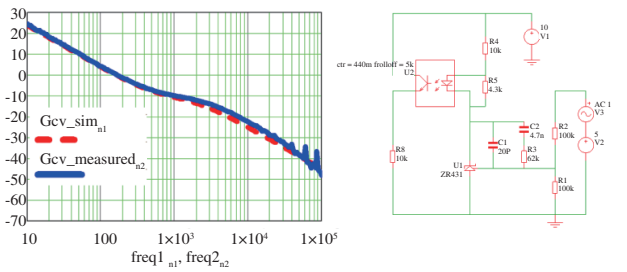

Fig. 25. Compensation plot comparison between simulation and measurement.

operates at 3 A, 6 A and 10 A respectively. The solid green lines represent the measurement results and the red dashed lines represent the calculation results, which show that these results match well practically. Though there may be concerns of dead time, it does not have impact from the prediction of the calculations if the frequency is given correctly. It is obvious to observe that the DC gain decreases with the increase of output current but the variation is relatively small compared to other hysteretic charge LLC converter. The cross frequency nearly remains the same result since the frequency variation is relatively very small.

To verify the transfer function of the overall loop, a practical precise model for the compensation circuit is required for this purpose because the transfer functions (23) is not with the consideration of the roll off frequency for FOD817A and TL431, which is necessary to obtain in practical measurement. Fig. 25 shows such a simulation example by pulling a 10 kΩ resistor at the emitter pin side of the opto-coupler for the rolling off frequency identification, in which the CTR is measured by 0.44 and the roll off frequency is verified to be 5 kHz. Refer to Fig. 15, with the other compensation parameters being set by C_v = 4.7 nF, C_f = 20 pF, R_v = 62 kΩ, R_{up} = 100 kΩ and R_f = 10 kΩ, the open loop plot of output to control can be obtained through simulation and measurement. Shown in Fig. 25, it can be seen the simulation result marked by the dashed red line matches well with the measurement result marked by the green solid line. With this consideration, a roll off pole is therefore added into (23) additionally, so the overall loop can be calculated precisely.

Fig. 26 shows the measurement results for the overall loop under the output of 12 VDC&4 A and 12 VDC&10 A respectively, it can be observed both the cross frequency and phase margin are featured by a very small variation under the two kind of output conditions, which is a special and comforting result characterized by HHC control.

To verify the result of the calculation by (24), the comparison between calculation and measurement are obtained under the output of 12 VDC&6 A. Shown in Fig. 27, the upside figure presents the measurement result and the downside figure shows the comparison under the output of 6 A. It reveals that the measurement result marked by solid line match very well with the calculation result marked by a dashed line up to half of the operating frequency.

In order to verify the characteristic under dynamic load condition, the waveforms of output voltage and resonant

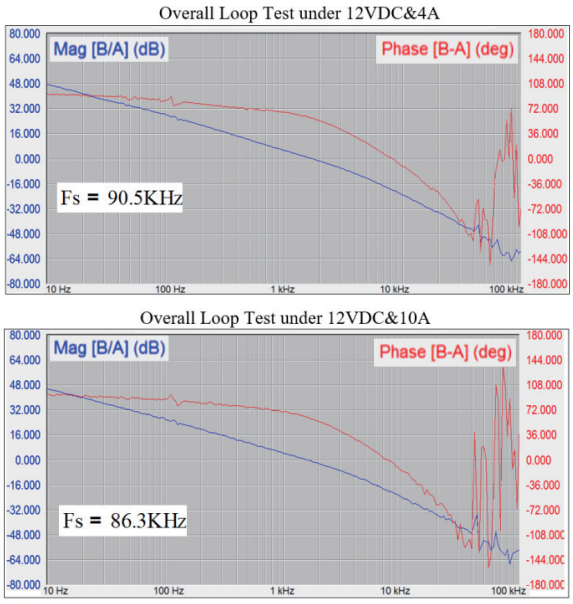

Fig. 26. Measurement results for the overall loop under the output condition of 12 VDC&4 A (upside) and 12 VDC&10 A (downside).

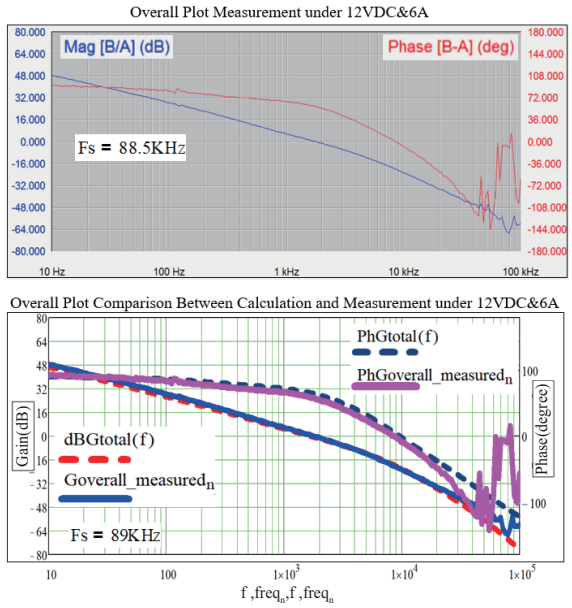

Fig. 27. Overall loop measurement under the output of 12 V&6 A (on the topside) and the related comparison between the measurement and calculation (on the downside).

tank current are measured under the dynamic load condition of 12 VDC&(4 A-8 A-4 A) and 12 VDC&(8 A-12 A-8 A). Shown in Fig. 28, it can be observed the good dynamic performance can be achieved.

To verify the transfer function of closed output impedance given by (28), the dynamic load measurement is conducted based on a step current of 4 A-8 A-4 A with the slew rate setting by 3 A/us and step period-setting by 1 ms. Fig. 29 shows such a comparison between calculation and measurement. It can be observed both results match well, which proves that the closed impendence is with good practical use for the practical design and applications based on LLC HHC control.

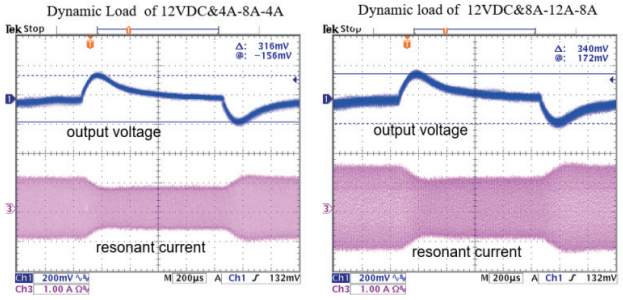

Fig. 28. Measurement of output voltage and resonant tank current.

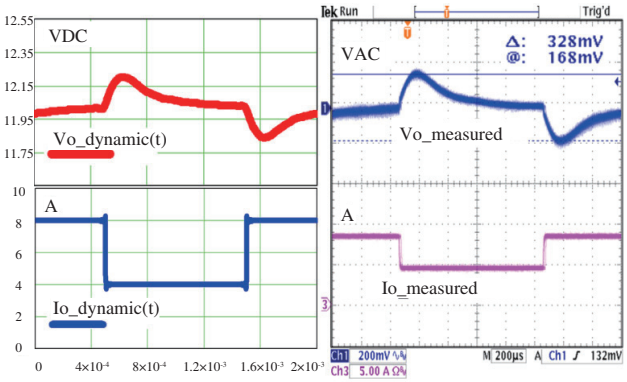

Fig. 29. Dynamic load response between calculation and measurement under the condition of 370 VDC input and 12 VDC&6 A output by 4 A–8 A–4 A.

VI. Conclusions

In this paper, the LLC HHC control has been introduced with the advantage of easy loop compensation and good dynamic characteristic compared to the conventional DFC control. The analytical small signal transfer functions applied for this control method have been therefore proposed and illustrated, in which the transfer functions of control to output, input to output, output impedance and the closed overall loop have been elaborated and verified. The overall comparison results based on the proposed transfer functions have been proved to match well with both the results from simulation and measurement in the most part of operating frequency range. More importantly, some physical insights related to the transfer functions are extracted and the design guideline for practical applications has been provided.

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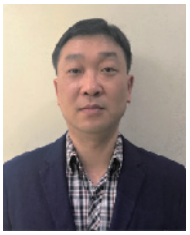

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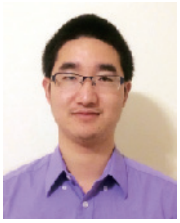

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Design of MMC Hardware-in-the-Loop Platform and Controller Test Scheme

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***Abstract*—The hardware-in-the-loop (HIL) simulation is an effective method to verify the overall function of the flexible HVDC transmission control and protection device. With this method, debugging the control and protection device can make the system run safely and stably after being put into operation. Therefore, a hardware-in-the-loop simulation platform modular multilevel converter (MMC) based on RT-LAB is established in this paper. Data merging between a converter valve control system and the real-time simulator is realized by high-speed optical fiber communication protocol conversion chassis, and the high-speed communication interface is designed to meet the requirements of the communication rate. Aiming at the control performance of the physical device, the test scheme is designed, and the test methods of voltage balance control and circulating current suppression are proposed. The closed-loop test of control and protection device is carried out by the active power step and AC/DC fault test. The above test verifies the validity of the HIL simulation platform of the MMC and the rationality of the testing scheme, and can meet the performance testing requirements of the control and protection device.**

***Index Terms*—Control and protection device, device debugging, hardware-in-the-loop (HIL) , modutar miltilevel converter (MMC), simulation test.**

I. Introduction

NOWADAYS, building up of a global energy ntework has become an international consensus. It is urgent to innovate the advanced transmission methods to develop long distance and large capacity transmission, and to improve not only the efficiency of transmission and the utilization of resources, but also the security, flexibility, and controllability of the power grid. Flexible high voltage direct current (HVDC) transmission has an independent, accurate, flexible and convenient active/reactive power control mode, and it has the advantages of rapid recovery and control after power grid fault, which has a wide application prospect [1]–[4]. The modular multilevel converter (MMC) has become a trend in the future, because of its outstanding advantages, such as high output waveform quality and minimal loss. Compared with the traditional DC commutation valve, two-level, and three-level converter valves, the modules of the modular multilevel converter need to be controlled independently. The complex structure of the control system also brings new problems to the design and test of the control system.

In order to ensure the reliable operation of the flexible HVDC converter valve, the domestic and foreign scholars and the research institutes have conducted a lot of research work on the design and simulation tests of the flexible HVDC transmission control system. In recent years, the modular multilevel converter real-time digital simulation of MMC based on FPGA (Field-Programmable Gate Array) technology has been greatly developed, because of the difficulties in the electromagnetic transient simulation of the switch valve caused by a large number of switching devices. The FPGA real-time digital simulation system and the control system are combined with the hardware-in-the-loop simulation which provides a means of improve the performance testing of the control system [5]–[6]. At the same time, the appropriate equivalent model is conducive to the simulation analysis of the system. For modular multilevel converter topology, the following three methods are usually used for steady-state analysis. The IGBT and its anti-series diode in the sub-module are equivalent to one switch to improve the simulation speed [7]; MMC averagely simplified model method [8]; the capacitor in the sub-module is replaced by the time-domain Thevenin equivalent branch, and then the sub-module is equivalent to a Thevenin equivalent branch. Finally, the sub-module Thevenin equivalent branch is cascaded to form the Thevenin equivalent branch of the whole bridge arm [9]. The efficiency of steady-state simulation analysis is greatly improved by the methods above, but there are still some limitations in the system simulation with blocking sub-modules. In order to better simulate the dynamic response process of MMC, an equivalent sub-module is used to replace an arm, which is equivalent to a Thevenin equivalent circuit in the case of deblocking MMC, while the arm is equivalent to a half-bridge uncontrolled sub-module with lumped parameters in the case of MMC blocking [10].

The control and protection system is the "brain" of the whole flexible HVDC transmission project. In the field of control and protection testing, MMC has a large number of sub-modules. Owing to the complexity of the control system, the system test is difficult and the workload is large before the actual project is put into operation. In order to simulate and debug the control and protection devices, it is an effective means of testing and de

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bugging all kinds of steady-state, transient and fault conditions of the controller using the HIL simulation method [11]–[12]. The HIL simulation test can verify the real-time performance of the controller and the correctness of the protection device action under conditions close to the actual operating conditions, and modify the relevant settings of the actual controller. The HIL simulation is a relatively mature test method and has been widely used in the design verification of control platforms [13]–[15].

Most of the existing hardware-in-the-loop simulation methods introduced in the literature are still aimed at the verification of the designed controller, and few of them are fully tested and validated for the whole system. However, how to realize the communication interface between the digital simulation system and the actual device has not been referenced [16]–[17]. Therefore, in order to test the MMC flexible HVDC transmission control protection device, this paper designs a hardware-in-the-loop simulation test system based on RT-LAB. The MMC main circuit using the Thevenin equivalent model of reference [10] runs in RT-LAB. The data merge is realized through a high-speed fiber-optic communication protocol conversion chassis. The physical side accesses control protection devices and forms a closed loop. According to the performance of the control protection device, the test scheme of converter station control and valve control is designed, and the dynamic performance test and function test of the actual control and protection device are completed by using the built platform. Unlike the traditional method, this method can reduce the actual project site debugging process and shorten the development cycle of the control and protection system.

II. Flexible DC System Structure

The overall structure and control system structure of the MMC flexible HVDC transmission system is given in Fig. 1(a) and (b). The control system is mainly composed of inner loop current controller, outer loop controller, phase locked loop, and pulse generation link. The two-terminal of the converter station needs to control the active component and the reactive component. Under normal circumstances, for a two-terminal active AC system, the rectifier side is generally used to control the active power and reactive power, and the inverter side controls the DC side voltage and reactive power. The converter valve control system receives the voltage reference wave from the converter station control and modulates the voltage using the nearest level modulation (NLM) or pulse width modulation (PWM) [18]–[19]. The trigger signal is applied to the sub-module to complete the switching of the state so that the output voltage waveform is close to a sine wave. The converter valve control system also needs to complete the control of the sub-module capacitance voltage balance.

The safe and stable operation of the equipment in the flexible HVDC transmission system is the main responsibility of the protection system. In the event of a fault or abnormality, the faulty or abnormal operating equipment is quickly removed from the system to prevent equipment damage or other normal working parts from being affected so that it can ensure the safe operation of the DC system. This ensures the safe operation

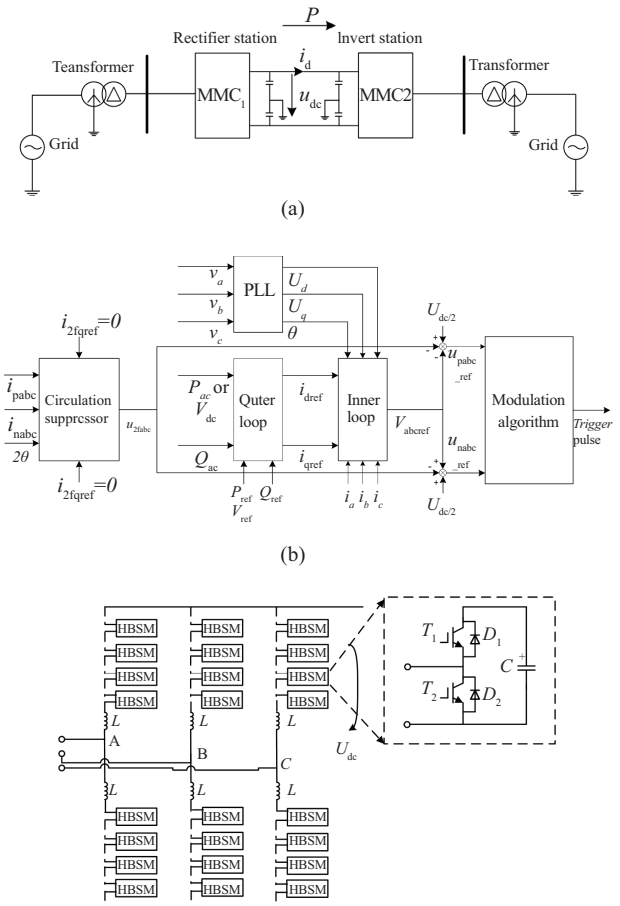

Fig. 1. MMC-HVDC system and control structure. (a) MMC-HVDC system. (b) Control system. (c) Equivalent model.

of the DC system. According to the different protected areas, protection can be generally divided into AC area protection [20]–[21], converter area protection, and DC area protection [22].

Due to the high controllability of the MMC-HVDC, the control and protection system largely determines its dynamic performance. Therefore, it is necessary to carry out simulation tests on the converter station control, converter valve control and protection devices by the HIL simulation platform to test whether the performance can fulfill operational requirements.

III. Simulation Platform Design

A. Real-Time Simulator

The characteristics and safety requirements of the power system determine that the exploration and research of the actual power grid greatly depend on simulation. Due to the high precision of the switching action of the power electronic devices in the flexible HVDC transmission, the simulation step size used in the simulation analysis is generally about 100 μs in order to accurately simulate and analyze the switching behavior of the device. Therefore, electromagnetic transient simulation tools are mainly used in the research of flexible HVDC transmission, such as MATLAB/Simulink in RT-LAB.

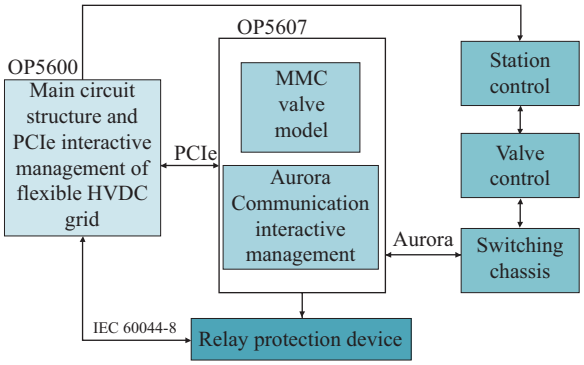

Fig. 2. System interface device overall structure.

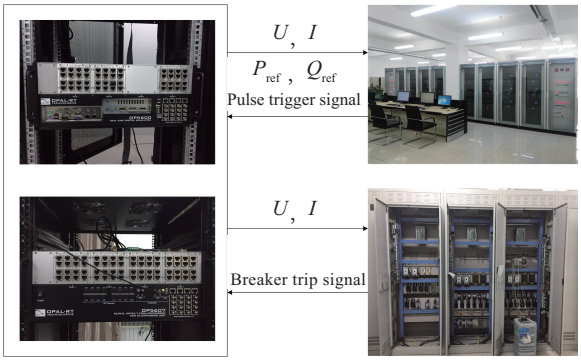

Fig. 3. Diagram of hardware-in-the-loop simulation platform hardware connection.

The implementation of the MMC main circuit depends on the upper computer and the target machine. The upper computer completes tasks, such as modeling, on-line parameter adjusting, signal monitoring, and C code generating to download the target machine. The target computer adopts the OP5600 with the Redhat operating system and the FPGA-based OP5607 as the real-time simulator for the HIL simulation applications.

By using the RT-LAB software running on the upper computer to achieve the connection between the upper computer and the target computer, RT-LAB can divide the complex model into multiple parallel subsystems and then allocate it to different CPU cores of the OP5600. The first is to build the system in the MATLAB/ Simulink environment. Then, according to the principle of model segmentation under RT-LAB, a series of operations such as model compilation, interface definition, and loading code are completed. The digital model is then converted to real-time code running on the target machine. Finally, the target machine will output all the signals.

The HIL simulation experiment platform designed in this paper completes the construction of the MMC main circuit on the upper computer. The real-time monitoring of the running state of the converter station is completed by the computer, and its functions are verified.

B. Overall System Architecture

Fig. 2 shows the overall system architecture of the interface devices. The OP5600 in the diagram is mainly used as the main circuit calculation. The main circuit components and the corresponding parameter settings are calculated in the CPU of the OP5600. OP5607 is mainly used for converter valve simulation and IO interface, which It receives the drive signal through the optical fiber and sends out the corresponding sub-module voltage. The IO interface is mainly used for the analog output and the corresponding digital signal input and output. The converter valve control device converts multi-channel optical signals into one or more signals by means of a communication protocol conversion chassis, completes the data integration work, and connects the OP5607 through the Aurora protocol to achieve information exchange including switching commands, capacitor voltage, and bridge arm current. The OP5607 internally completes part of the functional simulation of the sub-modules, and the data of the capacitance voltage of the sub-module is transmitted to the OP5600 via PCIe. The human-computer interaction interface is set in the monitoring background to realize the sub-module state, the function of the sub-module, and the display and setting of the control target and instruction. The converter station control device and the relay protection device are respectively connected with the OP5600, OP5607 through the IEC60044-8 protocol.

Fig. 3 shows the hardware connection diagram of the HIL simulation platform. The converter station control device needs to collect voltage signals on the AC side to complete the phase locked loop control. It uses the received DC voltage, active and reactive power reference values, and the voltage reference waves of the six bridge arms which are calculated through the inner and outer loop control. After electro-optical conversion, it is transmitted from the optical fiber to the converter valve control. The converter valve control passes through the photoelectric conversion and will receive the reference wave generated by the converter station control, adopting the nearest level modulation method to determine the number of sub-module inputs. It then sorts each sub-module according to the capacitor voltage based on the current direction of the bridge arm (positive or negative) that the sub-module with low or high capacitor voltage should be charged or discharged to generate the trigger signal of the sub-module. This completes the sub-modules' voltage balance control. The converter valve control also needs to collect the bridge arm current to complete the suppression of the interphase circulating current of the converter. The protection device needs to collect the DC-side signals in addition to the above-mentioned voltage and current signals to determine whether a protection action is triggered when a fault occurs and send the protection action signal and breaker trip signal back to the RT-LAB. In this way, a closed loop system is formed, which can accurately reflect the characteristics of the flexible HVDC transmission system and can better test the control and protection device.

C. Data Merge

Because of the large number of sub-modules and the need for the digital simulator to send the capacitor voltage and operating status of the sub-module to the converter valve control device, and to receive the trigger command, RT-LAB has a one-to-one

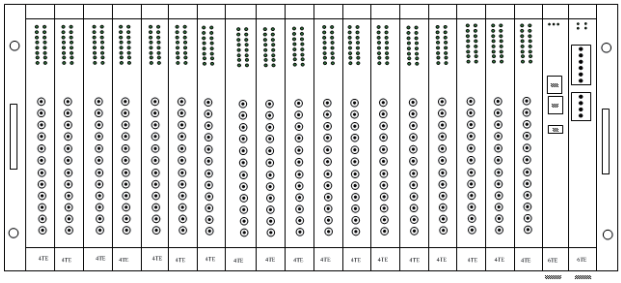

Fig. 4. Protocol conversion control box.

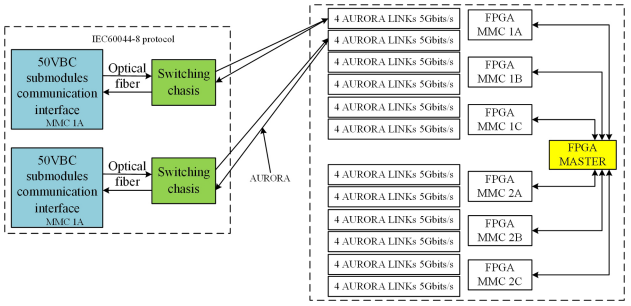

Fig. 5. Data merging method.

correspondence with the converter valve control interface. For the 300 sub-module capacitance voltages (without considering redundancy) of the single converter valve, this is complicated to operate. For this reason, the protocol conversion control chassis adopts the Aurora communication protocol, which is connected the valve base controller (VBC) device with through the Small Form-factor Pluggables (SFP) optical fiber module. All of the communication optical fibers between the VBC and the MMC sub-module digital model need to be connected to the protocol conversion control chassis. The protocol conversion control chassis assumes the task of connecting the entire simulation system. Each fiber interface board has six pairs of fiber interfaces and has a one-to-one correspondence with the VBC interface, and the structure of the interface board has a similar structure to the bridge control board of the VBC. The multimode optical fiber serves as a communication medium. The optical transmitter uses the HFBR-1414 optical transmitter module and the optical receiver uses the HFBR-2412 optical receiver module. A full-duplex information exchange channel is formed by the VBC and each sub-module via two optical fiber lines.

The protocol conversion control box Shown in Fig. 4 is responsible for the task of the whole simulation system. The standard 6U19 inch cabinet chassis design is adopted, it has 18 fiber interface cards, 1 main control board, 1 power board, and 1 back board. As shown in Fig. 5 for a data merge method, the real-time simulator OP5607 connects with the SFP light module on the FPGA board in the protocol conversion control chassis through the ultra-high-speed optical fiber. The communication protocol uses Aurora 8 B/10 B, bandwidth 5 GHz. It can be connected with the valve control system through FC7161 optical signal processing board. The protocol adopts IEC60044-8, which realizes the data merge between the multi-channel optical fiber data of the converter valve control system and the OP5607 real-time simulator, thus completing the HIL simulation of the MMC system. The design of the high-speed communication interface adopts SFP fiber with 2.5 Gbps bandwidth and AURORA protocol to complete the communication. The optical signal processing board is connected to the valve control system, and the data is encapsulated in 8 B/10 B. The data transmission of 8 K can be completed in 2 μs. The protocol conversion control chassis uses IEC60044-8 protocol to communicate with VBC. The interface is set to 32 bits. It takes four microseconds to complete a full data transmission. The FPGA uses a 200 MHz clock parallel operation. If the 300 sets of data are completely reorganized, it needs 2.5 μs which is the data transmission time plus the data reorganization time (up to 6.5 μs). In addition to data transmission time and data reorganization time, there is also backplane transmission delay in the process of data transmission. Each optical fiber interface board is responsible for communicating with VBC, and the data received by the optical fiber interface board needs to be transmitted to the main control board through the backplane bus. The backplane uses high-speed LVDS point-to-point data transmission, and the transmission time of 32 bit data is about 6.25×10^{-6} s. Therefore, the backplane transmission delay can be ignored in the communication rate calculation. The high-speed communication interface should be able to complete the transmission of 300 sub-module capacitor voltages in 10 μs step.

IV. Design of the Device Test Method

The test of the control and protection device for the flexible DC transmission system can be divided into a functional test and a dynamic performance test. The purpose of the functional test is to verify, optimize and test the overall functions of the complete control and protection equipment, including the verification of the accuracy of the design of the control and protection software, the test of the mutual cooperation between the control and protection equipment along with its functions under various operating modes as well as the accuracy of the interaction between the AC and DC system, and the verification of the correctness of sequence control logic and operation procedures.

The dynamic performance test mainly tests the transient characteristics of the flexible DC transmission system, checks the interaction between the control and protection device and the AC/DC system, and selects and verifies the control protection parameters. It also optimizes the response of the complete control equipment under various operating conditions and checks whether the protection configured in each area is reliable. The tests for the performance of the control device include sequential control, converter charging, open line test, deblock/block test, control mode switching, reactive power control, voltage balance control, circulation suppression, power lift, power step, DC voltage step, etc. In order to verify the reliable operation of the protection device, it is necessary to test AC bus fault, valve fault, and DC polar fault.

According to the control function of the physical device, on the basis of completing the equipment interface signal,

the internal communication, and the trigger pulse test, the performance test of the converter station control should be completed first. After the station control performance is accurate, the performance of the converter valve control is verified, and the steady performance test is carried out.

The converter station control performance test is divided into six tests. 1) The purpose of the converter charging test is to verify the accuracy of the valve trigger phase sequence and the control protection system phase-locked link. The sub-module charge is divided into two processes of uncontrolled rectifier charge and controllable charge, in which the controlled charge is completed under the control of the constant DC voltage. 2) The open line test (OLT) test is the deblocking test for the first active state of the converter valve. The purpose is to check whether the control system can correctly control the DC voltage and test the insulation of the main equipment. In order to ensure that the DC voltage does not exceed the maximum limit, simply set the DC voltage target value and voltage change rate and monitor the actual value of the DC voltage. 3) The sequential deblocking test provides insight as to whether the DC bus voltage and the system operation is stable after the uncontrolled rectifier charging is completed and the charging resistor exits to the end of the inverter deblocking process. 4) Control mode switching is when the converter station is converted from PQ to PV (or PV switching to PQ). It is observed whether the voltage and current waveform are smooth, whether there is a large fluctuation, and whether the system can maintain stable operation. 5) During the power (voltage) step, it is tested whether the system can respond quickly and complete the accurate tracking of the target value for the given power (voltage) instruction value. 6) STATCOM verifies the performance of the static var compensator and checks the current second harmonic frequency of the control protection system current.

As the core element in the secondary system of HVDC transmission, the converter valve control device is the interface device which connects the converter valve and the DC control system. It is an important part to control and protect the converter valve. Converter valve control is mainly responsible for pulse generation, voltage balance control, and circulation suppression.

The converter valve control performance test can be divided into three different tests, including voltage balance control, circulation suppression, and the protection function. 1) Voltage balance control keeps the deviation between the capacitor voltage and the calculated value of the sub-module within the target value. 2) During the circulating current suppressing test, the bridge arm current is monitored, and Fourier decomposition is performed to observe the proportion of the secondary harmonic negative sequence component. 3) When a fault occurs inside the valve or an over-current or over-voltage occurs in the bridge arm, the protection function checks the requested trip command to see whether it can be sent to the upper computer in time.

Because there are too many test projects mentioned above, this paper only designs two test methods to verify the control function of the voltage balance control and circulating current suppression control in the valve control test. The test flow is introduced as follows.

Fig. 6 is a flowchart for the test of voltage balance control.

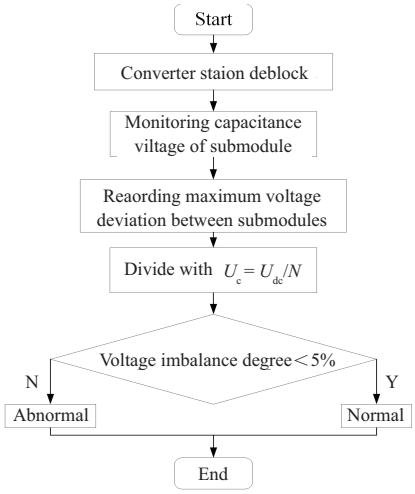

Fig. 6. The test flowchart of voltage sharing control.

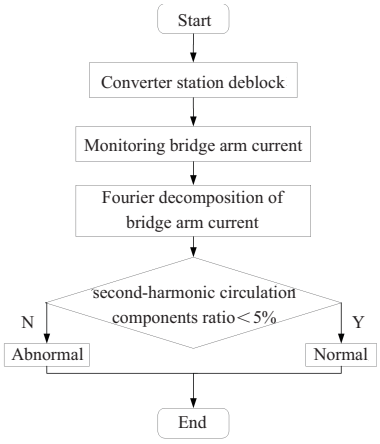

Fig. 7. The test flowchart of circulation suppression.

When the converter is unlocked, the voltage balance control begins to be put in. The capacitance voltage of each module is monitored and records the ratio of the maximum deviation value of each capacitance voltage to $U_c = U_{dc}/N$. If the voltage unbalance is less than 5%, the effect of voltage sharing control is better.

Fig. 7 shows the circulating current suppression test flow chart. It monitors the current of each phase of the bridge arm in the converter valve, decomposes the bridge arm current by Fourier decomposition, and observes the content of the secondary harmonic component. If the circulation component is less than 5%, the control effect of the circulation suppression is proved to be normal.

V. Simulation Verification

In order to verify the performance and testability of the built simulation platform, multiple tests were conducted under steady state, dynamic and fault conditions respectively. A two-terminal active system with a 51-level MMC-HVDC is running in the real-time simulator RT-LAB. The MMC modulates using the nearest level modulation. Station 1 adopts the control method of constant active power and reactive power; station 2 adopts

TABLE I
PARAMETERS OF SIMULATION TEST SYSTEM

AC voltage	230 kV
AC frequency	50 Hz
DC voltage	±160 kV
Converter rated capacity	500 MVA
Bridge arm inductor	28 mH
Number of sub-modules	50
Submodule capacitance	5 mF
DC capacitance	2 μF

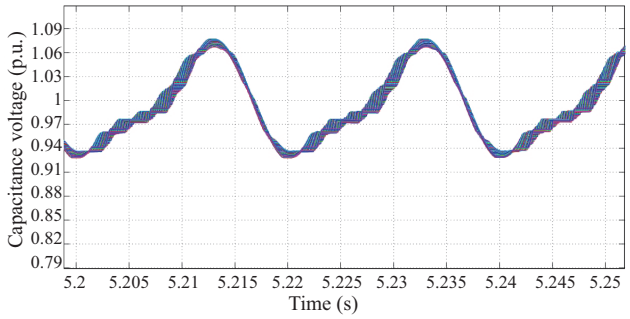

Fig. 8. Waveforms of voltage sharing control test.

the control method of constant DC voltage and reactive power, of which, P = −500 MW and Q = 100 MVar. The converter transformers connections are connected using Y_Nd. The main circuit related parameters are shown in Table I.

This article will mainly analyze the test contents of voltage balance control test, circulation suppression test, power step test, and AC/DC side fault (converter valve side single-phase grounding and DC bipolar short-circuit).

A. Voltage Balance Control Test

Fig. 8 shows the results of the voltage balance control test waveform. As previously mentioned, it can be determined that the voltage balance control of the sub-module capacitance voltage is performed well after the converter station is deblocked and voltage balance control is applied. The voltage fluctuation is small, and the maximum deviation of the capacitor voltage imbalance is not more than 3%. This is less than the specified 5%, which verifies that the converter valve control has a normal effect on the capacitor voltage balance control.

B. Circulation Suppression Test

In order to verify the suppressing performance of the VBC to the interphase circulating current of the bridge arm, the circulating current suppression control test is carried out.

Fig. 9 shows the current and circulating current of the upper and lower arm of phase A, the waveform of the grid side current and the harmonic content. The current has no obvious distortion and the waveform quality is better. The secondary harmonic content in the bridge arm current is less than 2%, which is far below 5%, indicating that the converter valve control has an

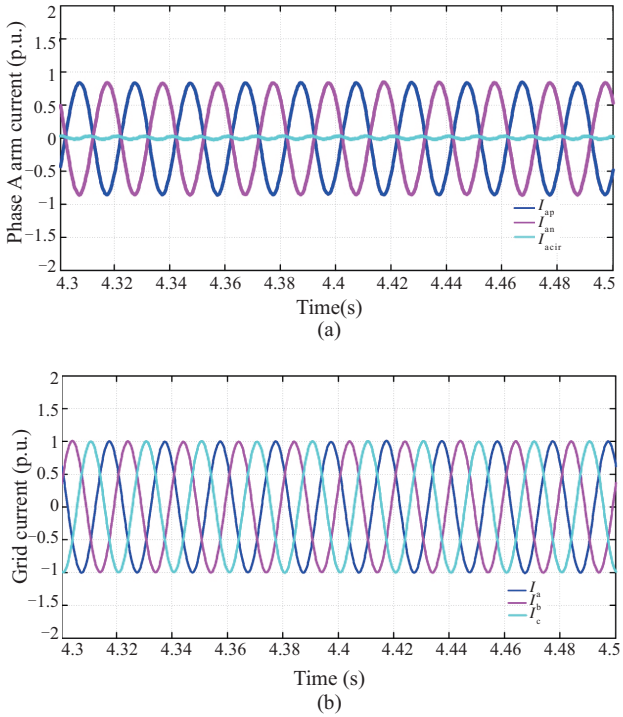

Fig. 9. Circulation suppression waveforms. (a) Phase A arm current. (b) AC current. (c) Harmonic content waveforms.

obvious effect on suppressing the phase-to-phase circulation of the bridge arm, and the control performance is good.

C.Power Step Test

In order to verify the dynamic performance of the platform, the active power test was carried out. Active power is reversed from −500 MW to 300 MW at 5 s, and reactive power is maintained at 100 Mvar. Fig. 10 shows the waveform of power, phase A arm current and capacitance voltage.

According to Fig. 10, the active power step is rapidly completed and the tracking is accurate. Reactive power is subject to a certain disturbance, but within 0.3 s the fixed value is restored. The internal current I_{acir} of phase A is fluctuated greatly during the transition process. It can transit smoothly under the action of the circulating current suppressor. The amplitude of AC component of arm current I_{ap} and I_{an} is decreased, and there is a more obvious distortion in the transition process. The capacitance voltage is fluctuated slightly after reversing, but it

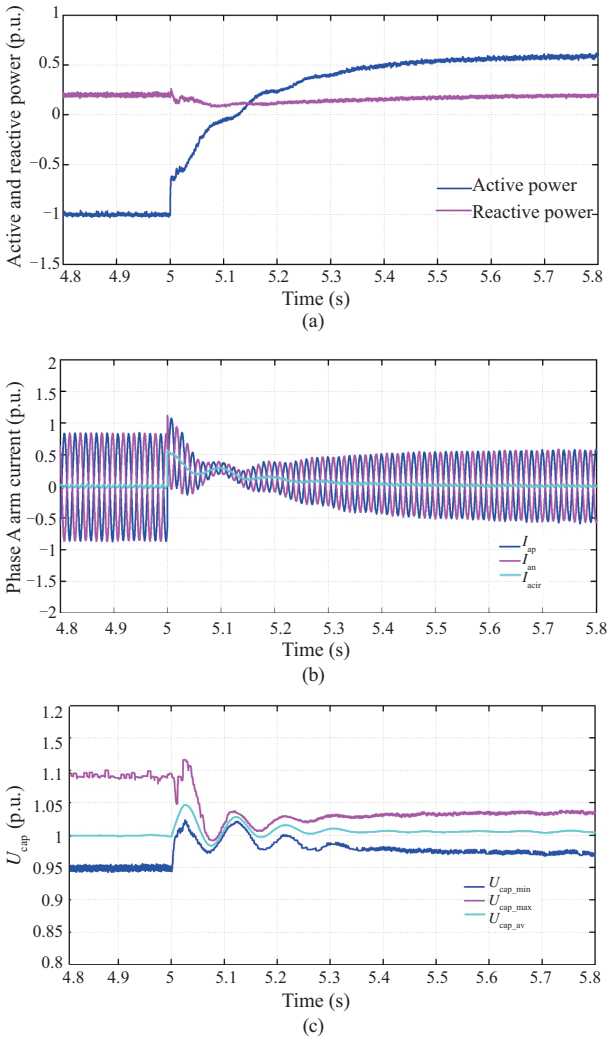

Fig. 10. Waveforms of active step power response. (a) Active and reactive power. (b) Phase A arm current. (c) Capacitance voltage.

can maintain balance under the action of voltage balance control.

The power step test shows that the control effect of the converter station control device is stable, the dynamic performance of the experimental platform is good, and the control targets can respond quickly to the instruction value and can be tracked accurately.

D. AC Fault Test

In order to verify the fault test capability of the built platform, examine the ability of the control protection system to handle the fault, and understand the influence of the fault on the system operation, the AC side single-phase to ground fault was carried out.

The AC side fault is set to single-phase grounding of the phase A valve side. After the system is in stable operation, the fault is triggered at t = 3.3 s. The relevant voltage and current waveforms are shown in Fig. 11.

When the phase A single-phase to ground fault occurs on the valve side, the DC current fluctuates with a small amplitude.

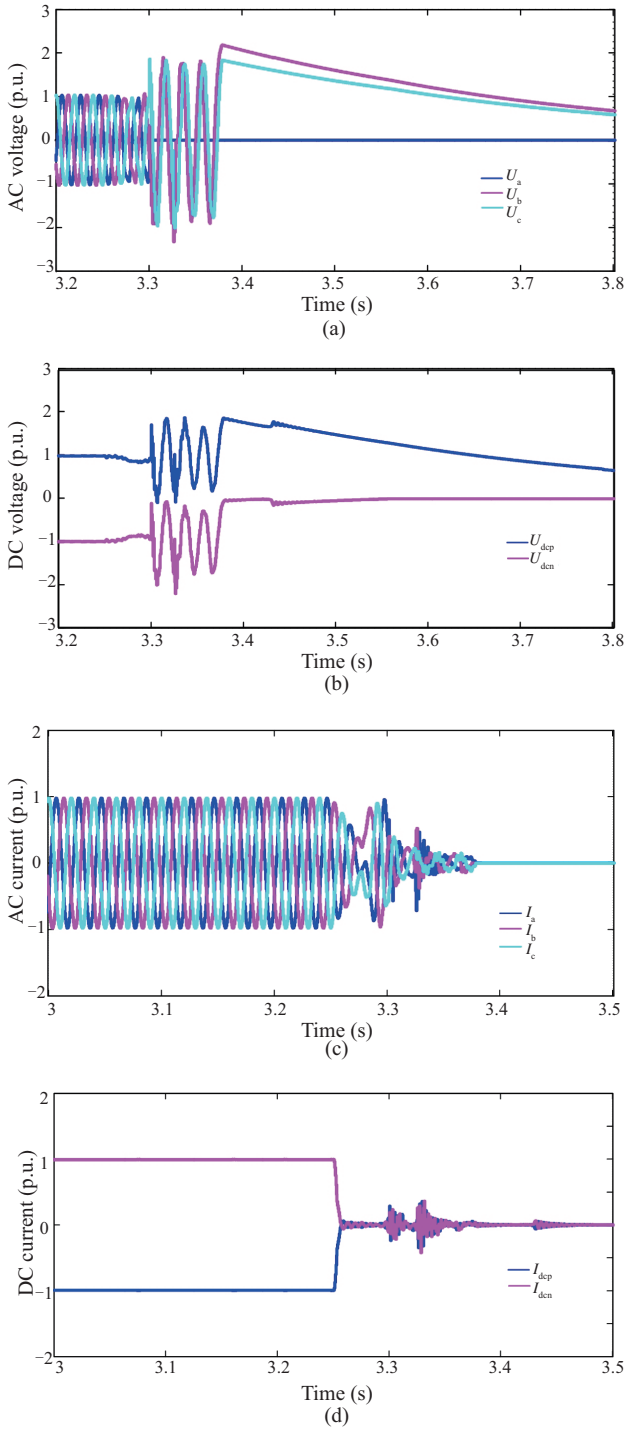

Fig. 11. Waveforms of valve side single-phase to ground fault. (a) AC voltage. (b) DC voltage. (c) AC current. (d) DC current.

Although the DC voltage appears similar to the sinusoidal fluctuation, the DC voltage can be maintained at 320 kV. The three-phase AC current remains basically stable, and the phase A voltage drop on the valve side is 0 while the voltage of B and C increases to 1.732 times that of the original one. Due to the converter blocking, the discharge path between the sub-module capacitance and the short-circuit point is cut off and the AC current is reduced when t = 3.33 s. When t = 3.37 s, the protection occurs and the AC circuit breaker trips. Power

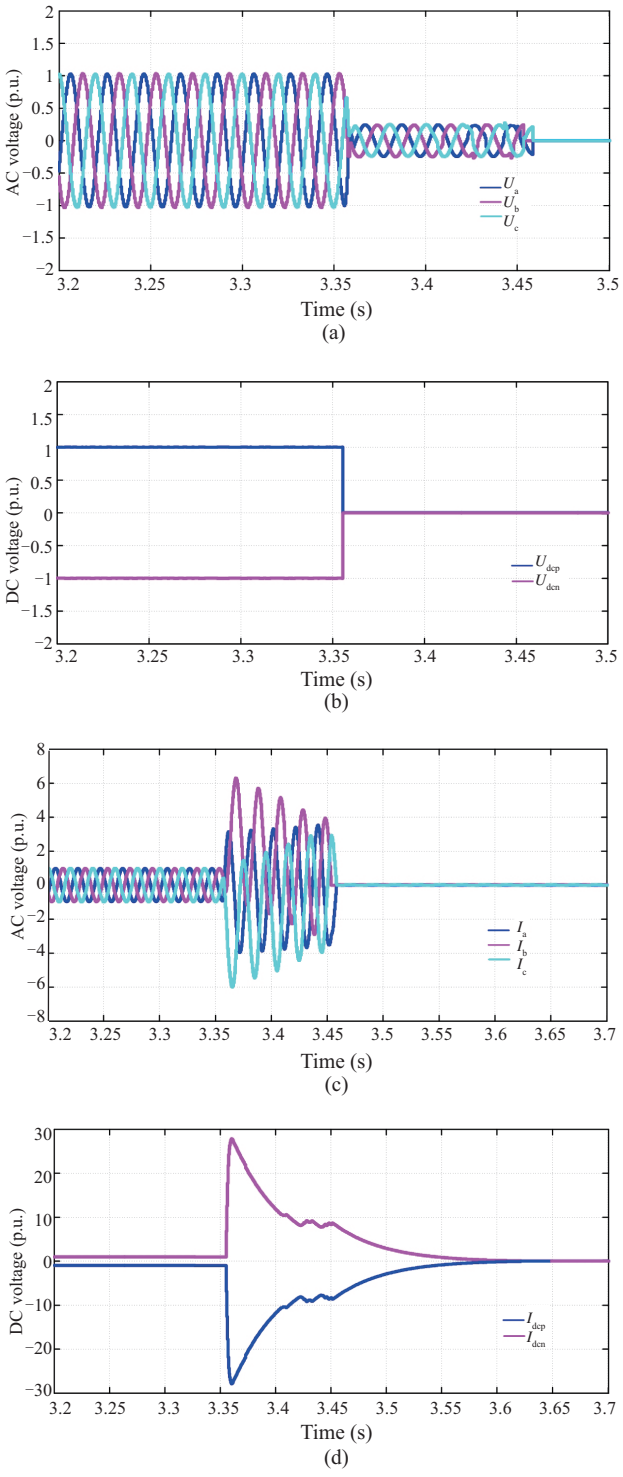

Fig. 12. Waveforms of valve side single-phase to ground fault. (a) AC voltage. (b) DC voltage. (c) AC current. (d) DC current.

transmission stops and the AC side can no longer feed current to the DC side. Therefore, AC and DC currents both change to zero.

E. DC Fault Test

For bipolar short-circuit fault, after the system operates stably, the fault is triggered at t = 3.35 s, the inverter is blocked after 25 ms, and the AC circuit breaker trips at t = 3.45 s. The relevant waveforms obtained from the simulation are given in Fig. 12.

It can be seen from the results in Fig. 12 that after a fault occurs, the capacitance of the submodules in each bridge arm rapidly discharges through the short-circuit path on the DC side, resulting in the rapid reduction of the DC voltage to 0, and both the DC current and the bridge arm current will increase rapidly in a short time. With the IGBT blocking, the fault characteristics of the AC side are similar to the three-phase short circuit. It can be seen that the AC current rises and the AC voltage decreases. When AC circuit breaker acts, AC current changes to zero. The DC current is also affected by the inverter blocking and the circuit breaker tripping. Because of the system blocking, the discharge circuit of the bridge arm capacitance is blocked. The DC current no longer contains the capacitor discharge current, and only the AC side feed current. With the tripping operation of the circuit breaker, the AC system does not feed the current to the DC side anymore, and the DC current gradually decays to zero.

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VI. Conclusion

In this paper, an HIL platform based on RT-LAB for MMC system of two-terminal is built, which has favorable steady-state and dynamic performance. A data merging method between the converter valve control system and the real-time simulator is designed to meet the requirements of communication speed. The test methods of voltage balance control and circulating current suppressing control are proposed. A series of dynamic and fault tests are carried out according to the performance indexes of control and protection devices. The tests show that the proposed test scheme is reasonable and can meet the requirements of the control and protection system test, which can provide an effective means for the study of control strategies. It has certain practical significance for the test of the control and protection device in the flexible DC project and can reduce on-site debugging process and meet its requirements.

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Prediction Method of DC Bias in DC-DC Dual-Active-Bridge Converter

Liangcai Shu, Wu Chen, and Zhanfei Song

***Abstract*—The dual-active-bridge (DAB) converter attracts more and more attentions due to its ability of bidirectional power transmission and high conversion efficiency. The adoption of high-frequency transformer provides galvanic isolation, but also brings the possibility of dc bias. In this paper, the causes of dc bias have been analyzed and relevant calculation methods are derived in details. With the calculation methods, the dc bias magnetizing current can be predicted considering the inconsistency of semiconductor switches and driver signals. In other words, if the maximum permitted dc bias of the transformer is given, the range of the inconsistency of semiconductor switches and driver signals can be obtained which helps guide the selection of semiconductor devices and design of the transformer. Therefore, extra flux balancing method can be avoided and the overall cost and volume will be further reduced. Additionally, simulation and experimental results show great agreement with the theoretical analysis.**

***Index Terms*—DC bias, dual-active-bridge converter, prediction method.**

I. Introduction

THE dual-active-bridge (DAB) converter has been widely adopted in the applications for bidirectional power transmission, such as energy storage system [1]. It comprises two active H-bridges and one high-frequency transformer to achieve large voltage transfer ratio and galvanic isolation. At present, the work mainly focuses on the control strategies of the DAB converter. The representative control methods including single-phase shift (SPS), dual-phase-shift (DPS) and triple-phase-shift (TPS) control [2]−[8], aiming to reduce current stress, widen power transmission range and improve conversion efficiency, especially the latter two control strategies. On the other hand, due to the adoption of high-frequency transformer, the dc bias of the transformer needs to be tackled, which can be classified into transient dc bias and steady dc bias. For the transient dc bias which always occurs with the abrupt change of phase-shift angle or input/output voltages, various transient phase shift control strategies are proposed to eliminate the phenomenon [9], [10]. For the steady dc bias, the dc excitation to the transformer can be caused by non-ideal behavior of the system components, including unmatched turn-on/turn-off times, gate driving signal delays and inconsistency between the parameters of semiconductor devices [11].

In order to eliminate the dc bias of the transformer, various flux measuring and balancing methods have been proposed [11]−[18]. The flux balancing method mainly includes two types: passive balancing and active control. A blocking capacitor connected in series with the winding of the transformer or an air-gap inserted into the core's magnetic path are the main passive balancing methods to eliminate or alleviate the dc bias of the transformer [12], [13], in which no extra control strategy or monitoring devices are needed. However, the blocking capacitor can result in a low-frequency oscillation in response to variations in switching modes, and cause excessive low-frequency EMI [12]. Moreover, this approach can increase the power loss and the volume. Additionally, the air-gap does not eliminate the dc flux component. Hence, the active flux control methods were proposed [11], [14]−[18]. In order to control the dc magnetization of the core, the flux must be measured dynamically, and the flux measuring methods can be mainly classified into flux measurement and current measurement. For the flux measuring methods, extra processing or components such as magnetic ear [11], a slot in the core legs [14], air-gap in the magnetic flux [15], specific type of magnetic core [16], or special sensors are needed to dynamically detect the variation of the flux. For the current measuring methods, the primary and secondary winding currents are sampled to monitor the variation of the magnetizing current [17], [18]. Almost all the measuring methods require high sampling rate and precision, and analog-to-digital converters are even needed [17], [18], which increases the complexity and the overall cost.

With the development of the semiconductor devices manufacturing, the consistency between switches can be guaranteed within certain range. As long as the inconsistency of switches and driving circuits is smaller than certain limitation, the dc bias in the high-frequency transformer can be tolerated. Hence, one calculation method of the dc bias magnetizing current seems necessary, which can also be used to predict the required range of inconsistency with the maximum permitted dc bias magnetizing current given. This can guide the selection of semiconductor devices and the design of transformer, so that extra flux balancing methods can be avoided. One calculation method of the dc bias magnetizing current is proposed in [19] for the zero-voltage-switching (ZVS) converters with the consideration of the

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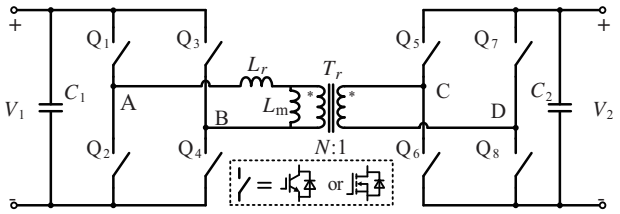


Fig. 1. Typical topology of the DAB converter.

parasitic capacitors in parallel with the switches. However, the calculation equation proposed in [19] is somewhat idealized to calculate the dc bias caused by the inconsistency of devices due to the neglect of on-resistance of the switches and windings. Hence, there is few methods to calculate the maximum dc bias magnetizing current considering the inconsistency of switches and driving circuits.

Considering the inconsistency of switches and driving circuits in practical circuit, a novel method of predicting the maximum dc bias magnetizing current of the DAB converter is proposed in this paper. The DAB converters with IGBTs and MOSFETs are analyzed separatly in the paper for the DAB converters with different semiconductor devices have different current paths in some switching modes. The equivalent models are built in Section II firstly and the generation of dc bias is analyzed in Section III. Then, the prediction method is derived in Section IV and examples are given to introduce the predicting procedure in Section V. Experiments are also made to verify the theoretical analysis in Section VI and conclusions are made in Section VII.

II. Equivalent Model of DAB Converter With IGBTs and MOSFETs

In this section, equivalent models of the DAB converters employing IGBTs and MOSFETs are built to conduct the derivation of dc bias magnetizing current. A typical configuration of the DAB converter is shown in Fig. 1. The inductor L_r is the leakage inductor of the transformer T_r or the summation of the leakage inductor and an external inductor. L_m is the magnetizing inductor of T_r. The turns ratio of T_r is N:1, and the primary and secondary winding resistances are set as r_p and r_s, respectively. The anti-paralleled diodes or body diodes of $Q_1 \sim Q_8$ are denoted as $D_1 \sim D_8$. In order to simplify the analysis, the transient turn-on or turn-off processes of the switches are neglected.

Because the specific derivation of magnetic flux density dc component B_{dc} is affected by the employment of IGBTs or MOSFETs, the two situations are analyzed separately here and the equivalent models are built in Fig. 2. For IGBTs and diodes, it is assumed that the on-state voltage V_{CE} and forward voltage drop V_F are constant, while for MOSFETs, their on-state resistances R_{ON} are assumed to keep constant. Hence, the parameters in Fig. 2 possess different meanings in IGBTs and MOSFETs applications, which is shown in Table I. For the voltages across $Q_1 \sim Q_8$ and $D_1 \sim D_8$ have been represented as the parameters R_p/R_s and v_{dp}/v_{ds}, v_{AB} and v_{CD} in Fig. 2 can

TABLE I
Specific Explanations of Parameters in Fig. 2

	IGBTs Applications	MOSFETs Applications
R_p/R_s	0	Summation of resistance of on-state MOSFETs (R_{pM}/ R_{sM})
v_{dp}/v_{ds}	Summation of forward voltages across ON switches or diodes on primary and secondary sides (v_{dpI}/ v_{dsI})	Summation of the voltage drops across conducted diodes on primary and secondary sides (v_{dpM}/ v_{dsM})
v_{AB}/v_{CD}	Voltage across points A and B (C and D) of the DAB converter employing ideal switches in Fig. 1	
r_p/r_s	Resistance of primary/secondary windings	

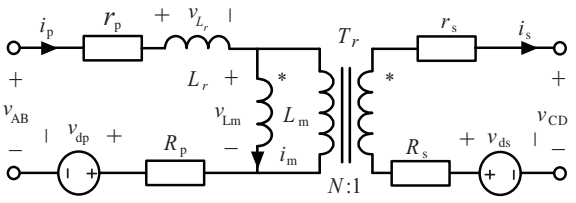


Fig. 2. Equivalent model of the DAB converter.

be seen as the voltage across A and B (C and D) of the DAB converter employing ideal switches. Hence, v_{AB} and v_{CD} are only affected by the voltages V_1 and V_2, the on/off states of $Q_1 \sim Q_8$ and $D_1 \sim D_8$.

III. Analysis of the Generation of DC Bias

As aforementioned, various factors can cause the magnetic flux density dc component B_{dc}, which can be classified into two types: unmatched turn-on/off times and the inconsistency between the devices. The unmatched turn-on/off times are usually caused by duty cycle loss, gate driving signal delay and so on, while the inconsistency refers to the difference between the on-state resistances or forward voltages of devices caused by differences in connection types, heat dissipation or device manufacturing.

A. Unmatched Turn-on-off Times

When the power is transmitted from V_1 to V_2 and no dc bias occurs, the typical waveforms of the DAB converter with SPS control strategy are shown in Fig. 3, in which the phase-shift time is t_φ and the dead time is t_d. And the specific ON switches in each mode are given in Table II. When discussing the effect of unmatched turn-on/off times, parameters of the switches are assumed to be consistent.

For the DAB converters with IGBTs, current i_p flows through the anti-paralleled diodes of Q_1 and Q_4 during the time interval $[t_0, t_2]$. Whenever Q_1 and Q_4 areturned on, as long as it is later than t_0 and earlier than t_2, operating state of the converter will not be affected. Hence, the inconsistent time when $Q_1 \sim Q_8$ are turned on will not cause dc bias.

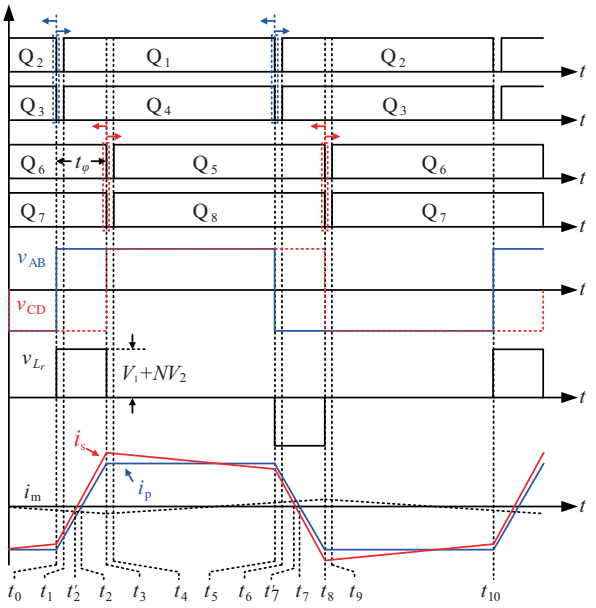


Fig. 3. The typical waveforms of the DAB converter with SPS control.

However, when MOSFETs are adopted as switches, current i_p flows through D_1 and D_4 during the dead zone $[t_0, t_1]$, and flows through the MOSFET channel as soon as Q_1 and Q_4 are turned on. So unmatched turn-on times will introduce an extra mode. Assuming that Q_1 is early turned on, current i_p will flow through D_1 and Q_4 before Q_1 is turned on. For the voltage drops of the body diodes and the voltages across the MOSFETs are different, the voltage across L_r changes and the variation of i_p in two half switching cycle can be unbalanced. Thus, the dc bias of i_p is generated. Moreover, duration of this extra mode is so short that the effect of inconsistent voltage across devices is limited and the dc bias of i_p will be small, which will be analyzed with mathematic derivation in the next section. For the secondary side of the DAB converter, the switching modes are not affected and no dc bias is generated, which will also be verified in the next section.

When the switches are early turned off or the turn-off time is delayed, the operating state will change and the dc bias will be generated in both IGBTs and MOSFETs applications. The situation where Q_2 is turned off earlier than the expected time is taken as an example to introduce how the dc bias is generated. As shown in Fig. 4, when Q_2 is early turned off, i_p increases before the expected time t_0. The variation of i_p during $[t_0, t_3]$ becomes larger than that during $[t_5, t_8]$, resulting in the positive dc bias of i_p. At the same time, the positive dc bias of i_p causes a positive voltage across the resistances r_p and R_{pM}, which can counteract the extra variation of v_{L_r} during $[t_0, t_3]$ and reduce the increment of the dc bias of i_p. Similarly, the secondary side of the DAB converter is not affected either. Finally, the steady operating state under positive dc bias is achieved.

B. Inconsistency of the Devices

For the DAB converters with IGBTs, it is assumed that the voltage drop across anti-paralleled diode D_1 is smaller than that of other switches. When D_1 conducts, the voltage across L_r will reduce. So the amplitude of the volt-seconds across L_r during $[t_0, t_2]$ will become smaller than that during $[t_5, t_7]$, resulting in the variation of i_p during $[t_0, t_2]$ to be smaller than that during $[t_5, t_7]$. Hence, the negative dc bias of i_p is generated. Similarly, the negative dc bias of i_p causes a negative voltage across the resistance r_p, which can compensate the loss of v_{L_r} during $[t_0, t_2]$ and reduce the decrement of the dc bias of i_p. However, the operating state of the secondary side is not affected. Hence, the final steady state under negative dc bias can be obtained. In addition, the similar analysis can be applied to the DAB converters employing MOSFETs.

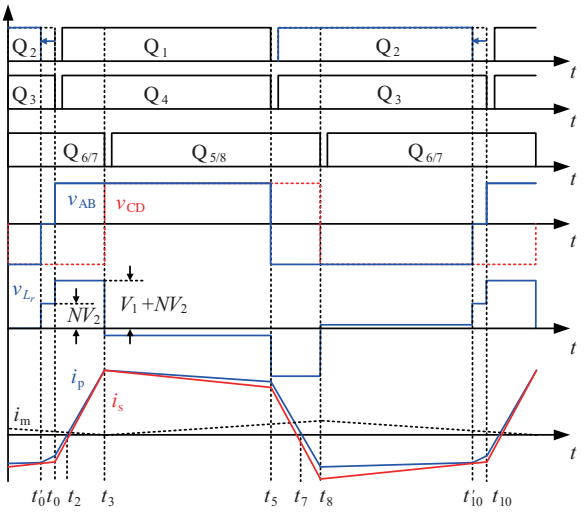


Fig. 4. The waveforms of the DAB converter when Q_2 is early turned off.

IV. Derivation of DC Bias Magnetizing Current

The derivation of dc bias magnetizing current depends on the type of selected switches, so this section is divided into two parts to introduce the calculation method for IGBTs and MOSFETs, respectively. Before the derivation, following assumptions are made to simplify the derivation.

1) The DAB converter is controlled with SPS strategy;
2) The capacitors C_1 and C_2 are large enough to keep V_1 and V_2 stable, which satisfies $V_1 = NV_2$;
3) The capacity of T_r is large enough to tolerate the magnetic flux density dc component B_{dc} and its magnetizing inductance keeps constant.

A. IGBTs Applications

Considering the forward voltages across the switches and primary/secondary winding resistances of the transformer, the voltage across L_m can be calculated with (1). When inconsistency occurs, v_{L_m} will deviate from the expected value, causing unexpected variation of i_p and dc bias.

$$v_{L_m} = v_{AB} - r_p i_p - v_{dpl} - v_{L_r} \tag{1}$$

TABLE II
ON-STATE LIST OF EACH SWITCH DURING A SWITCHING CYCLE

Time \ Item	IGBTs Applications				MOSFETs Applications			
	Mode_{pJI}	H-bridge 1	Mode_{SJI}	H-bridge 2	Mode_{PJM}	H-bridge 1	Mode_{SJM}	H-bridge 2
t_0~$t_1^!$	M_{P1I}	D_1/D_4	M_{S1I}	D_6/D_7	M_{P1M}	D_1/D_4	M_{S1M}	Q_6/Q_7
t_1~$t_2/t_2^!$		D_1/D_4		D_6/D_7	M_{P2M}	Q_1/Q_4		Q_6/Q_7
$t_2/t_2^!$ ~t_3	M_{P2I}	Q_1/Q_4	M_{S2I}	Q_6/Q_7		Q_1/Q_4		Q_6/Q_7
t_3~t_4		Q_1/Q_4	M_{S3I}	D_5/D_8		Q_1/Q_4	M_{S2M}	D_5/D_8
t_4~t_5		Q_1/Q_4		D_5/D_8		Q_1/Q_4	M_{S3M}	Q_5/Q_8
t_5~t_6	M_{P3I}	D_2/D_3		D_5/D_8	M_{P3M}	D_2/D_3		Q_5/Q_8
t_6~$t_7/t_7^!$	M_{P4I}	D_2/D_3		D_5/D_8	M_{P4M}	Q_2/Q_3		Q_5/Q_8
$t_7/t_7^!$ ~t_8		Q_2/Q_3	M_{S4I}	Q_5/Q_8		Q_2/Q_3		Q_5/Q_8
t_8~t_9		Q_2/Q_3	M_{S1I}	D_6/D_7		Q_2/Q_3	M_{S4M}	D_6/D_7
t_9~t_{10}		Q_2/Q_3		D_6/D_7		Q_2/Q_3	M_{S1M}	Q_6/Q_7

To calculate the dc part of the primary current, periodic time integrals are made for (1), and (2) is obtained. The periodic time integral of v_{L_m} keeps at zero when the converter reaches steady state with certain dc bias, otherwise the average value of magnetizing current will continue to change. Similarly, the third item of the right side of (2) is also zero when the converter reaches steady state.

$$\begin{aligned}\int_0^T v_{L_m}\mathrm{d}t &= \int_0^T v_{\mathrm{AB}}\mathrm{d}t - \int_0^T (r_{\mathrm{p}} i_{\mathrm{p}} + v_{\mathrm{dpI}})\mathrm{d}t - L_r \int_0^T \frac{\mathrm{d}i_{\mathrm{p}}}{\mathrm{d}t}\mathrm{d}t \\ &= \Delta\lambda_{\mathrm{ABI}} - \int_0^T (r_{\mathrm{p}} i_{\mathrm{p}} + v_{\mathrm{dpI}})\,\mathrm{d}t = 0,\end{aligned} \tag{2}$$

where T is the switching cycle. $\Delta\lambda_{\mathrm{ABI}}$ refers to the volt-seconds across points A and B in one switching cycle. As aforementioned, for IGBTs applications, the unmatched turn-on times has no influence on the volt-seconds $\Delta\lambda_{\mathrm{ABI}}$, while the unmatched turn-off times will affect $\Delta\lambda_{\mathrm{ABI}}$ directly. For example, when Q_2/Q_3 are early turned off, $\Delta\lambda_{\mathrm{ABI}}$ will increase over zero, on the contrary, when the turn-off times of Q_2/Q_3 are delayed, $\Delta\lambda_{\mathrm{ABI}}$ will fall below zero.

From Table II, one switching cycle contains four modes, so (3) can be obtained as

$$\begin{aligned}\Delta\lambda_{\mathrm{ABI}} &= \int_0^T (r_{\mathrm{p}} i_{\mathrm{p}} + v_{\mathrm{dpI}})\,\mathrm{d}t \\ &= \int_{t_0}^{t_2} v_{\mathrm{dp1I}}\mathrm{d}t + \int_{t_2}^{t_5} v_{\mathrm{dp\,2I}}\mathrm{d}t + \int_{t_5}^{t_7} v_{\mathrm{dp3I}}\mathrm{d}t + \int_{t_7}^{t_{10}} v_{\mathrm{dp4I}}\mathrm{d}t + r_{\mathrm{p}}\int_0^T i_{\mathrm{p}}\mathrm{d}t, \\ &= v_{\mathrm{dp\,1I}}\tau_{1\mathrm{I}} + v_{\mathrm{dp\,2I}}\tau_{2\mathrm{I}} + v_{\mathrm{dp\,3I}}\tau_{3\mathrm{I}} + v_{\mathrm{dp4I}}\tau_{4\mathrm{I}} + r_{\mathrm{p}}\bar{I}_{\mathrm{dcpI}}T,\end{aligned} \tag{3}$$

where $\bar{I}_{\mathrm{dcpI}}$ is the average current of i_{p}, namely, the dc part of i_{p}. v_{dpJI} (j = 1, 2, 3, 4) are shown as (4), in which $v_{\mathrm{Q}j}$ and $v_{\mathrm{D}j}$ (j = 1, 2, 3, 4) refer to the voltage drops across the switch Q_j and the anti-paralleled diode D_j, respectively. $\tau_{j\mathrm{I}}$ (j = 1, 2, 3, 4) are the time intervals of the respective modes $\mathrm{M}_{\mathrm{pJI}}$, which are shown as (5). Some approximate treatments are made here to simplify the derivation procedure, including neglecting the effect of r_{p} on the duration $\tau_{j\mathrm{I}}$ of each mode and ignoring the extra short mode introduced by the unmatched turn-off times.

$$\begin{cases} v_{\mathrm{dp\,1I}} = -v_{\mathrm{D1}} - v_{\mathrm{D4}} & v_{\mathrm{dp\,2I}} = v_{\mathrm{Q1}} + v_{\mathrm{Q4}} \\ v_{\mathrm{dp\,3I}} = v_{\mathrm{D2}} + v_{\mathrm{D3}} & v_{\mathrm{dp4I}} = -v_{\mathrm{Q2}} - v_{\mathrm{Q3}} \end{cases} \tag{4}$$

$$\begin{cases} \tau_{1\mathrm{I}} = t_\varphi/2 - \bar{I}_{\mathrm{dcpI}} L_r / (V_1 + NV_2) \\ \tau_{2\mathrm{I}} = (T - t_\varphi)/2 + \bar{I}_{\mathrm{dcpI}} L_r / (V_1 + NV_2) \\ \tau_{3\mathrm{I}} = t_\varphi/2 + \bar{I}_{\mathrm{dcpI}} L_r / (V_1 + NV_2) \\ \tau_{4\mathrm{I}} = (T - t_\varphi)/2 - \bar{I}_{\mathrm{dcpI}} L_r / (V_1 + NV_2) \end{cases} \tag{5}$$

Then, with (3), (4) and (5), one can be derived as (6).

$$\bar{I}_{\mathrm{dcpI}} = \frac{\Delta\lambda_{\mathrm{ABI}} - (v_{\mathrm{dp\,1I}} + v_{\mathrm{dp3I}})\frac{t_\varphi}{2} - (v_{\mathrm{dp2I}} + v_{\mathrm{dp4I}})\left(\frac{T}{2} - \frac{t_\varphi}{2}\right)}{r_{\mathrm{p}} T - (v_{\mathrm{dp\,1I}} - v_{\mathrm{dp2I}} - v_{\mathrm{dp3I}} + v_{\mathrm{dp4I}}) L_r / (V_1 + NV_2)} \tag{6}$$

It should be emphasized that the amplitude of $\bar{I}_{\mathrm{dcpI}}$ cannot be too large, otherwise i_{p} will be larger or smaller than zero in the whole switching cycle, causing (4) and (5) to fail. Moreover, (3)−(6) work only when the current i_p is continuous. Hence, it is required that the time intervals of $\mathrm{M}_{\mathrm{p1I}}/\mathrm{M}_{\mathrm{p3I}}$ and $\mathrm{M}_{\mathrm{s2I}}/\mathrm{M}_{\mathrm{s4I}}$ must be larger than the dead time. And the boundary condition of (6) should be checked up after calculation.

Similarly, the dc part of i_{s} can be calculated with (7).

$$\bar{I}_{\mathrm{dcpI}} = \frac{\Delta\lambda_{\mathrm{CDI}} - (v_{\mathrm{ds1I}} + v_{\mathrm{ds3I}})(\frac{T}{2} - \frac{t_\varphi}{2}) - (v_{\mathrm{ds2I}} + v_{\mathrm{ds4I}})\frac{t_\varphi}{2}}{-r_{\mathrm{s}} T - (v_{\mathrm{ds1I}} - v_{\mathrm{ds2I}} - v_{\mathrm{ds3I}} + v_{\mathrm{ds4I}}) L_r / (V_1 + NV_2)}, \tag{7}$$

where $\Delta\lambda_{\mathrm{CDI}}$ refers to the volt-seconds across points C and D in one switching cycle. For instance, when $\mathrm{Q}_5/\mathrm{Q}_8$ are early turned off, $\Delta\lambda_{\mathrm{CDI}}$ will reduce below zero. On the contrary, when the turn-off times of $\mathrm{Q}_5/\mathrm{Q}_8$ are delayed,

$\Delta\lambda_{\mathrm{ABI}}$ will increase over zero.$v_{\mathrm{ds}i\mathrm{I}}$ (i = 1, 2, 3, 4) are shown as (8), in which $v_{\mathrm{Q}j}$ and $v_{\mathrm{D}j}$ (j = 5, 6, 7, 8) refer to the voltage drops across the switch Q_j and the anti-paralleled diode D_j, respectively.

$$\begin{cases} v_{\mathrm{ds1I}} = v_{\mathrm{D6}} + v_{\mathrm{D7}} & v_{\mathrm{ds2I}} = -v_{\mathrm{Q6}} - v_{\mathrm{Q7}} \\ v_{\mathrm{ds3I}} = -v_{\mathrm{D5}} - v_{\mathrm{D8}} & v_{\mathrm{ds4I}} = v_{\mathrm{Q5}} + v_{\mathrm{Q8}} \end{cases} \tag{8}$$

With (6) and (7), the magnetic flux density dc component B_{dc} can be calculated with

$$B_{\mathrm{dcI}} = \frac{N^2 \mu_0 \mu_r A_e}{l_{\mathrm{m}}} (\bar{I}_{\mathrm{dcpI}} - \bar{I}_{\mathrm{dcsI}} / N), \tag{9}$$

where μ_0 is the permeability of vacuum, and μ_r is the relative permeability, A_e is the effective cross-sectional area, and l_{m} is the length of flux path.

With (6), (7) and(9), it is found that both $\bar{I}_{\mathrm{dcpI}}$ and $\bar{I}_{\mathrm{dcsI}}$ are only affected by the factors on their respective sides, including volt-seconds, winding resistance of the transformer and the voltage drops across devices. But they collaborate to result in the dc bias of the transformer. For the methods which detect the transformer directly and produce reverse excitation to counteract the dc bias, the magnetic flux density dc component B_{dc} can be eliminated. However, $\bar{I}_{\mathrm{dcpI}}$ and $\bar{I}_{\mathrm{dcsI}}$ still exist, which can cause uneven conduction and switching loss among switches and further result in inconsistent aging degree of the semiconductor devices. This may aggravate the inconsistency among devices and increase the dc bias of both sides in turn. With these methods [11], [14]−[18], the position (primary or secondary side or both sides) where the dc bias occurs cannot be ascertained, making it hard to eliminate the possible dc bias of i_{p} and i_{s}. From this perspective, detecting the dc parts of i_{p} and i_{s} and regulating the duty cycles of switches at the side where dc bias occurs seems to be a better choice to avoid this potential ill effect.

B. MOSFETs Applications

For MOSFETs applications, (2) is still workable. Assuming that the on-state resistance of MOSFETs and voltage drops across body diodes are constant, (10) can be obtained according to Table II.

With (10), the reason why unmatched turn-on times only cause small dc bias in the MOSFETs applications (mentioned in Section III) can be easily obtained. When the turn-on time of switches are early or delayed, current i_p can flow through the body diodes and the operating state keeps unchanged. For example, in Fig. 3, as long as the turn-on time of Q_1 is later than t_0 and earlier than t_2, $\Delta\lambda_{\mathrm{ABM}}$ will keep unchanged, because it has been mentioned in Section II that v_{AB} is only affected by the voltages V_1 and V_2, the on/off states of Q_1–Q_8 and D_1–D_8. However, due to the difference between the voltage drops of body diodes and the voltages across MOSFETs channel, the first item on the left side varies, which results in the dc bias of i_{p}. But this duration is too short, so the dc bias of i_{p} will be small.

$$\begin{aligned} \Delta\lambda_{\mathrm{ABM}} &= \int_0^T (R_{\mathrm{pM}} i_{\mathrm{p}} + v_{\mathrm{dpM}})\,\mathrm{d}t \\ &= \int_{t_0}^{t_1} v_{\mathrm{dplM}}\,\mathrm{d}t + \int_{t_1}^{t_5} R_{\mathrm{p2M}} i_{\mathrm{p}}\,\mathrm{d}t \\ &\quad + \int_{t_5}^{t_6} v_{\mathrm{dp3M}}\,\mathrm{d}t + \int_{t_6}^{t_{10}} R_{\mathrm{p4M}} i_{\mathrm{p}}\,\mathrm{d}t + r_{\mathrm{p}} \int_0^T i_{\mathrm{p}}\,\mathrm{d}t \\ &= v_{\mathrm{dp1M}} t_{\mathrm{d}} + R_{\mathrm{p2M}} \int_{t_1}^{t_5} i_{\mathrm{p}}\,\mathrm{d}t + v_{\mathrm{dp3M}} t_{\mathrm{d}} \\ &\quad + R_{\mathrm{p4M}} \int_{t_6}^{t_{10}} i_{\mathrm{p}}\,\mathrm{d}t + r_{\mathrm{p}} \bar{I}_{\mathrm{dcpM}} T \end{aligned} \tag{10}$$

One switching cycle contains four modes according to the on-state devices, and the expressions of v_{dp1M}, R_{p2M}, v_{dp3M} and R_{p4M} are shown as (11).

$$\begin{cases} v_{\mathrm{dp1M}} = -v_{\mathrm{D1}} - v_{\mathrm{D4}} & R_{\mathrm{p2M}} = R_{\mathrm{Q1}} + R_{\mathrm{Q4}} \\ v_{\mathrm{dp3M}} = v_{\mathrm{D2}} + v_{\mathrm{D3}} & R_{\mathrm{p4M}} = R_{\mathrm{Q2}} + R_{\mathrm{Q3}} \end{cases} \tag{11}$$

By neglecting the variation of i_{p} during [t_3, t_5] and [t_8, t_{10}] and ignoring the extra short modes introduced by the unmatched turn-off times, the integrals of i_{p} during [t_1, t_5] and [t_6, t_{10}] can be calculated as (12).

$$\begin{cases} \int_{t_1}^{t_5} i_{\mathrm{p}}\,\mathrm{d}t = \bar{I}_{\mathrm{dcpM}} \left(\frac{T}{2} - t_{\mathrm{d}}\right) + \frac{kTt_\varphi}{4} + \frac{kt_\varphi t_{\mathrm{d}}}{2} - \frac{k}{2} t_\varphi^2 - \frac{k}{2} t_{\mathrm{d}}^2 \\ \int_{t_6}^{t_{10}} i_{\mathrm{p}}\,\mathrm{d}t = \bar{I}_{\mathrm{dcpM}} \left(\frac{T}{2} - t_{\mathrm{d}}\right) - \frac{kTt_\varphi}{4} - \frac{kt_\varphi t_{\mathrm{d}}}{2} + \frac{k}{2} t_\varphi^2 + \frac{k}{2} t_{\mathrm{d}}^2 \end{cases} \tag{12}$$

where k is the rate of rise of i_{p} during [t_0, t_4], namely, $(V_1+NV_2)/L_r$.

Therefore, $\bar{I}_{\mathrm{dcpM}}$ can be calculated as (13). Similarly, $\bar{I}_{\mathrm{dcsM}}$ can also be obtained as (14), with the expressions of $R_{s1\mathrm{M}}$, v_{ds2M}, R_{s3M} and v_{ds4M} shown as (15).

$$\bar{I}_{\mathrm{dcpM}} = \frac{\Delta\lambda_{\mathrm{ABM}} - (v_{\mathrm{dp1M}} + v_{\mathrm{dp3M}}) t_{\mathrm{d}} - (R_{\mathrm{p2M}} - R_{\mathrm{p4M}})(Tt_\varphi + 2t_\varphi t_{\mathrm{d}} - 2t_\varphi^2 - 2t_{\mathrm{d}}^2)(V_1 + NV_2)/(4L_r)}{r_{\mathrm{p}} T + (R_{\mathrm{p2M}} + R_{\mathrm{p4M}})(T/2 - t_{\mathrm{d}})} \tag{13}$$

$$\bar{I}_{\mathrm{dcsM}} = \frac{\lambda_{\mathrm{CDM}} - (v_{\mathrm{ds2M}} + v_{\mathrm{ds4M}}) t_{\mathrm{d}} - (R_{\mathrm{s1M}} - R_{\mathrm{s3M}})(Tt_\varphi + 2t_\varphi t_{\mathrm{d}} - 2t_\varphi^2 - 2t_{\mathrm{d}}^2)(V_1 + NV_2)/(4L_r)}{-r_{\mathrm{s}} T - (R_{\mathrm{s1M}} + R_{\mathrm{s3M}})(T/2 - t_{\mathrm{d}})} \tag{14}$$

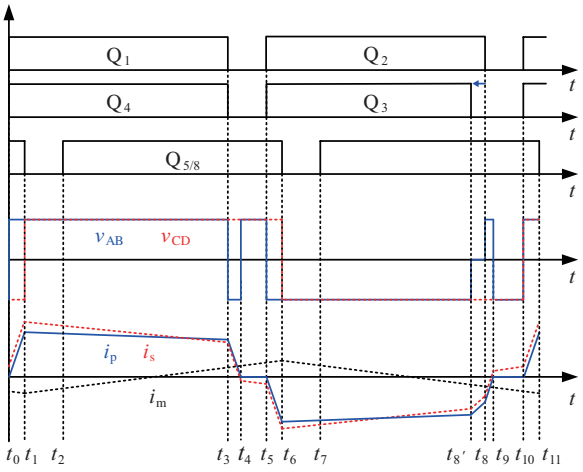


Fig. 5. The waveforms of the DAB converter when Q_3 is early turned off and i_p is discontinuous.

$$\begin{cases} R_{s1M} = R_{Q6} + R_{Q7} & v_{ds2M} = -v_{D5} - v_{D8} \\ R_{s3M} = R_{Q5} + R_{Q8} & v_{ds4M} = v_{D6} + v_{D7} \end{cases} \tag{15}$$

Then, similar to (9), the dc magnetizing current can be calculated with (13) and (14). Similar to the IGBTs applications, the dc magnetizing current is caused by the dc bias on both primary and secondary sides, and the dc bias on primary and secondary sides has no effect on each other. Hence, it is also recommended that dc bias currents $\bar{I}_{dcpM}$ and $\bar{I}_{dcsM}$ should be treated separately.

C. Analysis for Discontinuous Current Mode (DCM)

The aforementioned analysis of dc bias magnetizing current is based on the condition that i_p and i_s are continuous, while for the discontinuous current mode (DCM) some conclusions changes. As shown in Fig. 5, when the power is transferred from V_1 to V_2, the phase-shift angle is too small to keep i_p continuous. But due to the magnetizing current i_m, i_s can be kept continuous. When Q_3 is early turned off, an extra operating mode will be introduced, and the volt-seconds $\Delta\lambda_{AB}$ can be calculated as (16).

$$\begin{aligned} \lambda_{AB} &= \int_{t_0}^{t_5} v_{AB}\mathrm{d}t + \int_{t_5}^{t_{10}} v_{AB}\mathrm{d}t \\ &= V_1\left(\frac{T}{2} - \frac{2i_p(t_3)L_r}{V_1 + NV_2}\right) \\ &\quad - V_1\left(\frac{T}{2} - t_d - \frac{2L_r}{-V_1 - NV_2}\left(i_p(t_8') - \frac{NV_2}{L_r}t_d\right)\right) \\ &= V_1\frac{2(-i_p(t_8') - i_p(t_3))L_r}{V_1 + NV_2} \end{aligned} \tag{16}$$

For that the current i_p keeps almost unchanged during the durations $[t_1, t_3]$ and $[t_6, t_8]$, $i_p(t_3)$ is considered to be very close to $-i_p(t_8')$ and $\Delta\lambda_{AB}$ is very close to zero. Hence, the dc bias will be very tiny in this situation. However, since that i_s is still continuous, unmatched turn-off time of the switches still causes obvious dc bias. Although the shape of i_s varies, the dc bias current can still be predicted with (6), (7), (13) and (14) since that the time intervals of $[t_4, t_5]$ and $[t_9, t_{10}]$ are very short. Similarly, the inconsistency of devices at the primary side just results in very small dc bias, while the inconsistency of devices at the secondary side can cause large dc bias, which can be predicted with (6), (7), (13) and (14). Furthermore, when the phase-shift time is smaller than the dead zone, the transmission power will be zero if $V_1 = NV_2$, and no dc bias will be generated.

The aforementioned analysis can be generalized as follow:

1) When the phase shift angle is small, the winding current of leading bridge will be discontinuous, while the winding current on lagging side keeps being continuous due to the magnetizing current;
2) Unmatched turn-on and turn-off time and inconsistency of devices in leading bridge only result in very tiny dc bias, which can hardly be measured;
3) Unmatched turn-on and turn-off time and inconsistency of devices in lagging bridge results in obvious dc bias, which can be calculated with (6), (7), (13) and (14);
4) When the phase-shift time reduces smaller than dead zone, no dc bias will be generated if $V_1 = NV_2$.

D. Analysis for $V_1 \neq NV_2$

Considering the situation $V_1 \neq NV_2$, i_p and i_s will vary obviously during the time intervals $[t_1, t_3]$ and $[t_6, t_8]$. But as long as the difference between V_1 and NV_2 is not very large, (6), (7), (13) and (14) still work. But if V_1 and NV_2 mismatch seriously, i_p and i_s will cross zero during $[t_1, t_3]$ and $[t_6, t_8]$, and operating stage will change, so that the prediction accuracy of dc bias will decrease. Additionally, when $V_1 \neq NV_2$, the transmission power is not zero even if the phase-shift time is smaller than the dead zone, so that the unmatched turn-on/off times and inconsistency of devices will still result in dc bias. However, for the operating states in such situation and normal situation are totally different, the accuracy of the aforementioned expressions will decrease a lot.

E. Generalization

With the aforementioned analysis, for the DAB converters, the dc components of primary and secondary current are only affected by the factors on their respective sides, and they collaborate to cause the dc part of magnetizing current. Hence, the aforementioned calculation methods can be generalized to the multi-active-bridge converter, which is shown in Fig. 6. With (2), similar derivation procedure can be applied to calculate integrals and the dc part $\bar{I}_{dci}$ (i = 1, 2, …, N) of current through each winding can be obtained. Hence, by reflecting $\bar{I}_{dci}$ to the 1# side uniformly, the dc magnetizing current can be expressed as the summation of the reflected dc current.

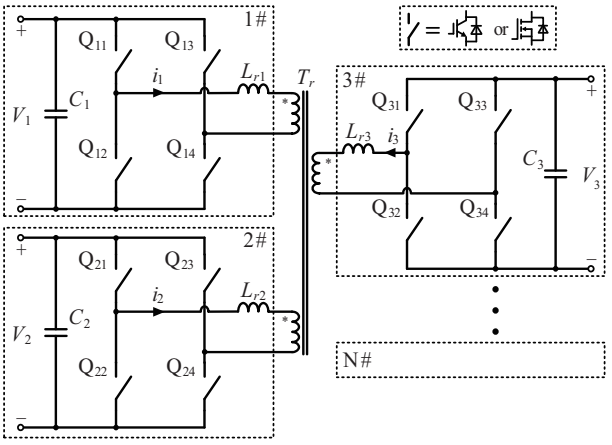


Fig. 6. The topology of multi-active-bridge converter.

V. The Prediction Method of the DC Bias

In order to obtain the maximum permitted inconsistency of devices and drivers, an example is taken here to introduce the detailed calculation procedure. The parameters are shown in Table III. Moreover, the maximum inconsistency of forward voltage or on-state resistance is set as ±5%.

The maximum unmatched turn-on/off time is set as 10 ns. Hence, considering that only one switch on primary side turns off 10 ns earlier or later than the expected time, $\Delta\lambda_{AB}$ can reach the maximum value (7.5×10^{-6} Vs) or the minimum value (-7.5×10^{-6} Vs).

For IGBTs applications, if $\Delta\lambda_{ABI}$ is fixed at 7.5×10^{-6} Vs and φ is set as 50°, the curves of $\bar{I}_{dcpI}$ versus $v_{dp1I}\sim v_{dp4I}$ are shown in Fig. 7(a), in which each layer of curve represents a set of v_{dp2I} and v_{dp4I}. The curves surrounded by dash dot lines and solid lines represent the data with v_{dp2I} fixed at 3.23 V and 3.57 V, respectively. It can be noted that $\bar{I}_{dcpI}$ increases with the decrease of $v_{dp1I}\sim v_{dp4I}$. The range of $\bar{I}_{dcpI}$ versus the phase-shift angle φ is shown in Fig. 7(b). As aforementioned, if $V_1 = NV_2$, the dc bias will decrease to zero when the phase-shift time is shorter than the dead time. The dead time is set as 1μs, so that when φ is smaller than 3.6°, the dc bias will be zero. And noticeably, the situation that V_1 and V_2 mismatch is not considered here. The range of $\bar{I}_{dcpI}$ is given as the gray area, which is slightly broadened with the increase of φ. When φ increases to 50°, the maximum and minimum values can reach 2.105 A and –2.105 A, with the maximum inconsistency limited within ±5%.

For MOSFETs applications, the curves of $\bar{I}_{dcpM}$ versus R_{p2M} and R_{p4M} is shown in Fig. 8(a). Because the time intervals of modes M_{p1M} and M_{p3M} are very short, v_{dp1M} and v_{dp3M} have little effect on $\bar{I}_{dcpM}$. Hence, they are fixed at 6.6 V here to simplify the analysis. In Fig. 8(a), $\bar{I}_{dcpM}$ increases with the decrease of R_{p2M} and increase of R_{p4M}. And $\bar{I}_{dcpM}$ increases along with φ according to Fig. 8(b). The maximum and minimum values can reach 1.269 A and –1.269 A with φ increasing to 50°.

It can be found that the rate of rise of the maximum value of $\bar{I}_{dcpI}$ is smaller than $\bar{I}_{dcpM}$. For the DAB converters employing MOSFETs, the differences between the on–

TABLE III
Main Parameters of DAB Converter

	IGBTs Applications	MOSFETs Applications
Input voltage V_1	750 V	
Output voltage V_2	750 V	
Switching cycle T	100 μs	
Phase-shift angle φ	50°	
Dead time t_d	1 μs	
Leakage inductor L_r	200 μH	
Magnetizing inductance L_m	20 mH	
Turns ratio of T_r	1:1	
Winding resistance r_p/r_s	100 mΩ	
Device type	IHW25N120R2	L227F18Y
Device parameters	forward voltage (1.7 V)	ON resistance (33 mΩ)
	Diode forward voltage drop (3.1 V)	Diode forward voltage drop (3.3 V)

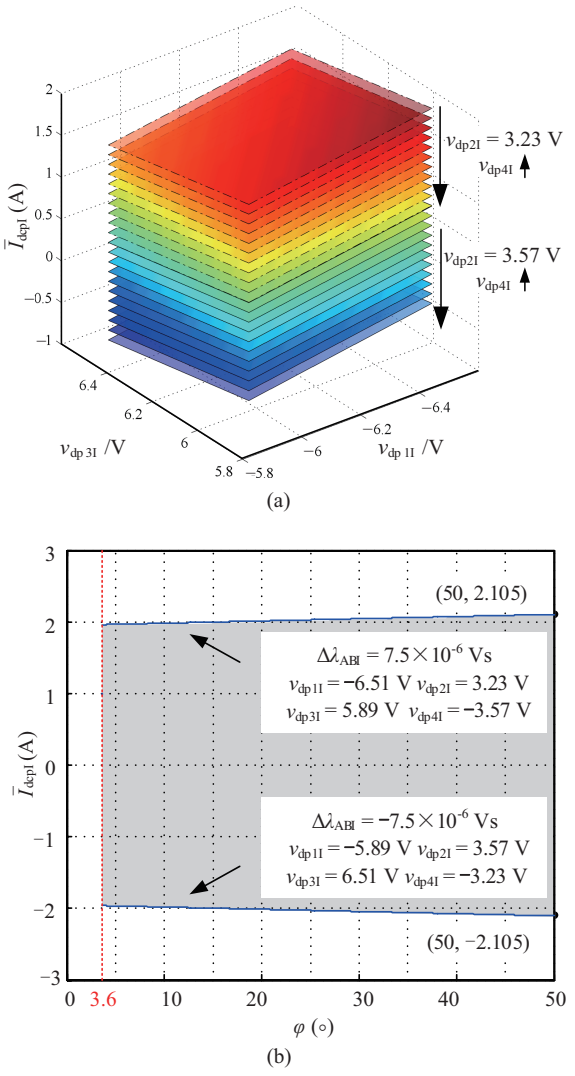


Fig. 7. The curves of $\bar{I}_{dcpI}$. (a) Versus $v_{dp1I}\sim v_{dp4I}$. (b) Versus phase-shift angle φ.

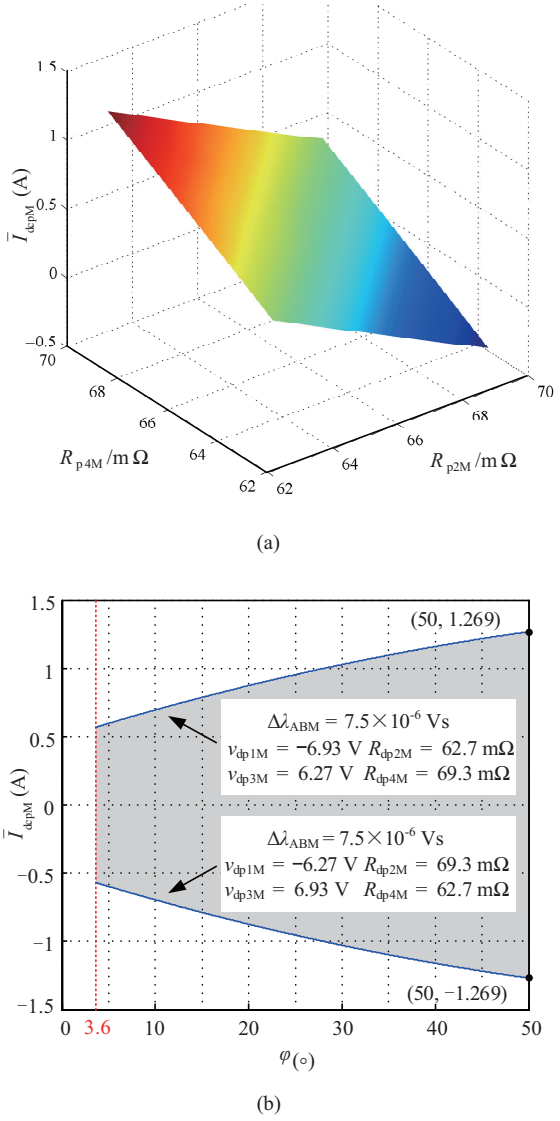


Fig. 8. The curves of $\bar{I}_{dcpM}$. (a) Versus R_{dp1M} and R_{dp4M}. (b) Versus phase-shift angle φ.

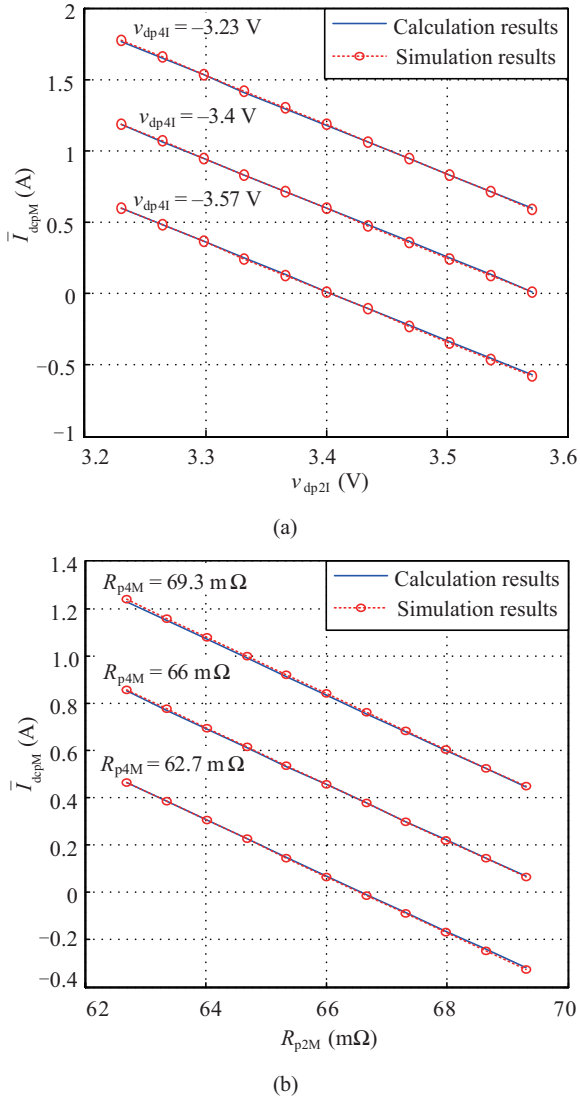


Fig. 9. The comparison between simulation and calculation results for (a) IGBTs applications. (b) MOSFETs applications.

state resistance of MOSFETs are confirmed once the type and maximum inconsistency of MOSFETs are given. With the increase of phase shift-angle φ, the maximum value of i_p increases, which causes differences between the voltages across inconsistent MOSFETs to be magnified. Hence, the maximum of $\bar{I}_{dcpM}$ increases rapidly. From another perspective, the item of numerator in (13), namely, $-2t_\varphi^2+t_\varphi(T+t_d)-2t_d^2$ is positive and is proportional to the square of t_φ. When R_{p2M} is smaller than R_{p4M}, the third item of numerator in (13) is proportional to the square of t_φ, while the denominator keeps unchanged, resulting in the quadratic increase of the maximum of $\bar{I}_{dcpM}$. However, for the DAB converters with IGBTs, the forward voltages of IGBTs and voltage drops of anti-paralleled diodes are assumed to be constant. Once the type of IGBTs is selected, the differences between the voltage across switches are determined, which do not vary with the increase of φ. Hence, according to (6), it can be found that the maximum of $\bar{I}_{dcpI}$ increases linearly along with φ. Actually, the rate of rise of the maximum value of $\bar{I}_{dcpI}$ and $\bar{I}_{dcpM}$ depends on the parameters of semiconductor switches and the given maximum inconsistency.

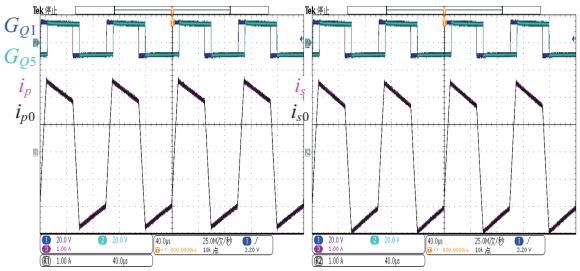
For some approximate treatments are made to simplify the derivation, the PLECS software is employed to verify the aforementioned results. For IGBTs applications, the error between simulation and calculation results is always smaller than 0.02 A with the given conditions, which is shown in Fig. 9(a). For MOSFETs applications, the comparison between simulation and calculation results is shown in Fig. 9(b), in which the error keeps being smaller than 0.02A. Hence, it can be concluded that the accuracy of aforementioned equations can be guaranteed.

VI. Experimental Analysis

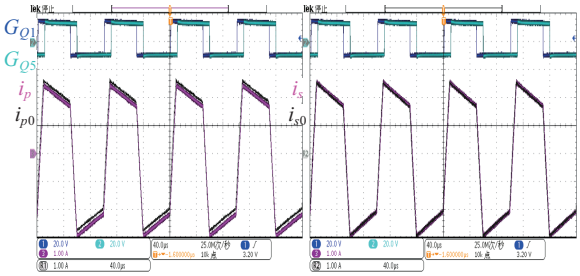
In order to verify the aforementioned analysis, an experi mental prototype was built with the parameters given in Table IV.

TABLE IV
EXPERIMENTAL PARAMETERS

	IGBTs Applications	MOSFETs Applications
Input voltage V_1	50 V	
Output voltage V_2	50 V	
Switching cycle T	100 μs	
Phase-shift angle φ	36°	
Dead time t_d	1 μs	
Leakage inductor L_r	206.4 μH	
Magnetizing inductance L_m	19.64 mH	
Turns ratio of T_r	1:1	
Winding resistance r_p/r_s	60 mΩ	
Device type	IKW30N60T	IXFX 55N50
Device parameters	forward voltage (1.5 V)	ON resistance (80 mΩ)
	diode forward voltage drop (1.65 V)	diode forward voltage drop (1.5 V)



(a)

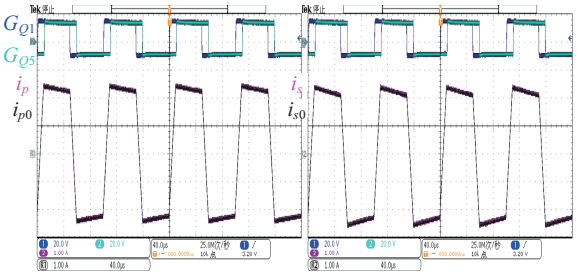


(b)

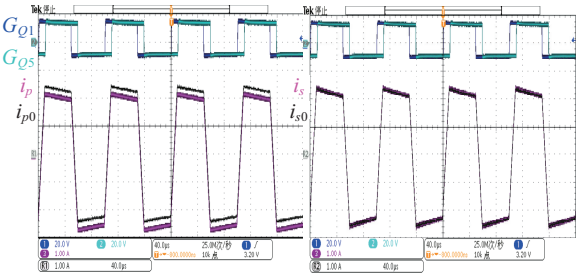
Fig. 10. The main waveforms of the DAB converters employing IGBTs. (a) Unmatched turn-on times. (b) Unmatched turn-off times.

The experimental results are shown in Figs. 10–12.

The waveforms of the DAB converter with IGBTs are given in Fig. 10. When the turn-on and turn-off times of Q_1 are not early or delayed, the currents through the primary and secondary wingdings of the transformer are shown as i_{p0} and i_{s0}, respectively. When Q_1 is turned on 500 ns later than the expected time as shown in Fig. 10(a), the primary and secondary currents are shown as i_p and i_s, which keep unchanged comparing to i_{p0} and i_{s0}. However, when Q_1 is set to be turned off 150 ns earlier than the expected time as shown in Fig. 10(b), the dc part of i_p decreases obviously while i_s keeps unchanged, which agrees with the aforementioned analysis.



(a)



(b)

Fig. 11. The main waveforms of the DAB converters employing MOSFETs. (a) unmatched turn-on times. (b) unmatched turn-off times.

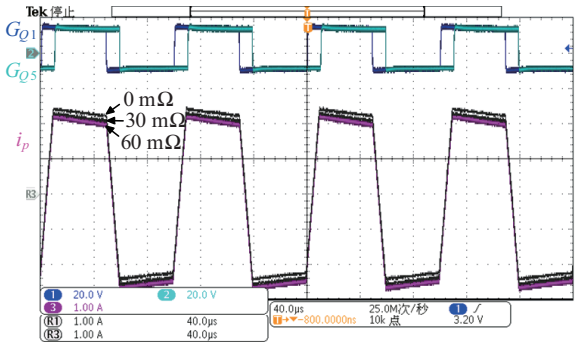


Fig. 12. The main waveforms of the DAB converters employing MOSFETs with different R_{p2M}.

The waveforms of the DAB converter with MOSFETs are shown in Fig. 11. Similarly, i_{p0} and i_{s0} refer to the original currents through the primary and secondary windings, respectively. When Q_1 is turned on 500ns later than the expected time as shown in Fig. 11(a), the primary and secondary currents are shown as i_p and i_s. The dc bias in i_p is affected slightly and the dc bias in i_s keeps unchanged. As mentioned in Section III, even though the turn-on time of Q_1 is delayed, i_p can still flow through its body diode during this mode. Hence, the only difference introduced by the unmatched turn-on time of Q_1 is the change of the voltage across Q_1 in this duration. Also because this duration is too short, the effect on the dc part of i_p is hardly observed. When Q_1 is turned off 150 ns earlier than the expected time, the dc part of i_p decreases obviously comparing to the initial situation, which is shown as Fig. 11(b). However, the dc part of i_s keeps unchanged for no change is put the secondary side. It can also be noted that there is an initial dc bias in the

converte r due to the inconsistency of devices.

In order to verify the relation between $\bar{I}_{dcpM}$ and R_{p2M}, a small resistor is connected in series with Q_1. By changing the resistance from 0 to 30 mΩ, and 60 mΩ, it can be noted that the dc part of i_p reduces gradually as in Fig. 12. As the duration of M_{p1M} is so short that the effect of the extra resistor on v_{dp1M} can be neglected, it can be concluded that $\bar{I}_{dcpM}$ decreases with the increase of R_{p2M}, which agrees with Fig. 8(a).

VII. Conclusion

In this paper, dc bias in the DAB converters with SPS control has been analyzed, and one prediction method of dc bias magnetizing current is proposed considering the inconsistency of switches and driving circuits, which can also be generalized to the multi-active-bridge converters. Some conclusions can be made here:

1) For IGBTs applications, unmatched turn-on times has no effect on the dc bias, while unmatched turn-off times will cause an obvious dc bias;
2) For MOSFETs applications, unmatched turn-on times has a very slight influence on the dc bias, while unmatched turn-off can introduce an obvious dc bias;
3) Unbalanced factors can only affect the dc bias current on the respective side, while they collaborate to create a dc flux density component in the transformer core.

With the prediction method, if the maximum permitted dc bias of the transformer is given, the range of the inconsistency of semiconductor switches and driver signals can be obtained, which is helpful for the selection of semiconductor devices and the design of the transformer. Hence, extra flux measurement and balancing methods can also be avoided.

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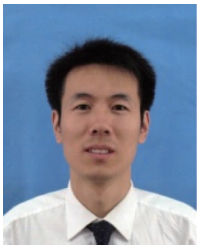

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Improved Quasi-Y-Source DC-DC Converter for Renewable Energy

Xupeng Fang, Xiaokang Ding, Shixiang Zhong, and Yingying Tian

***Abstract*—In order to improve the performance of dc-dc converter circuit in renewable energy power generation system, and overcome the problems of input current discontinuity and high inrush current in traditional Y-source converter, an improved Y-source dc-dc boost converter topology is presented in this paper. The voltage gain formula is derived by analyzing the topology and operating principle of the converter circuit. The proposed circuit topology inherits all the benefits of the existing Y-source converter and has several more advantages, including the higher voltage gain, continuous input current and small inrush current. The simulation and the experiments based on the prototype are performed. And the simulation and experimental results verify the rationality and superiority of the circuit topology.**

***Index Terms*—Boost converter, dc-dc converter, improved quasi-Y-source converter, renewable energy.**

I. Introduction

THE rapid development of the human society and the industrial production causes increasing energy consumption, and thus the reserved non-renewable energy declines rapidly, especially for the fossil fuels, has led to a growing supply shortage. At present, renewable energy has become a hot spot for many researchers because of its clean and sustainable development. For new energy generation, such as photovoltaic, wind power and fuel cell power generation, there are disadvantages of low output voltage. Therefore, it is necessary to increase the output voltage to a higher dc voltage by a high voltage gain dc-dc converter.

Although the traditional boost converter has the characteristics of simplicity, high conversion efficiency, due to the low voltage gain, its application in renewable energy systems is limited. This is caused by the following reasons: the conventional boost converter can only obtain a higher output voltage by increasing the duty cycle, which also causes the current peaks of the output diode and the controllable power switch to increase. This will lead to a large conduction loss of the diode and the power switch and an increase of the voltage stress of the capacitor, which reduces the conversion efficiency and the service life of the circuit. The high-boost gain converters were proposed with the switched inductor unit in [1] and the voltage multiplication unit in [2]. They were designed to increase the voltage gain and the higher the voltage gain need to be obtained, the more cascaded units should be used theoretically. But it increases the cost and complexity of the circuit and affects its conversion efficiency. Prof. F. Z. Peng proposed Z-source inverter topology to overcome the problems of the traditional inverter in 2002 [3]. Subsequently, a quasi-Z-source inverter topology was presented in [4], which reduces the voltage stress of the passive components in the impedance source network and makes the input current continuous compared to the conventional Z-source inverter. Furthermore, the Z-source network can also be applied to dc-dc converters, which also have excellent characteristics [5]. From then on, the Z-source and quasi-Z-source concept have been widely applied in lots of areas such as electric vehicles, photovoltaic generation, and wind power generation, etc.

In order to further increase the voltage gain of the Z-source-based converters, many scholars have applied coupled inductors in impedance source network in recent years[6], [7]. Many new high voltage gain topologies are proposed: high frequency transformer isolated Z-source inverter [8], TZ-source inverter [9], trans-Z-source inverter[10], [11], Γ-source inverter [12], a family of T-source networks [13], [14], Y-source inverter [15], [16] and quasi-Y-source inverter [17], [18]. It is worth noting that the Y-source inverter uses a three-winding transformer to flexibly adjust its voltage gain, and compared with other converters, it can achieve higher boost gain with the same shoot-through duty cycle. The Y-source converter concept could be extended to dc-dc conversion, and the Y-source dc-dc converter topology is shown in Fig. 1. Similar to the Z-source converter, the operating mode of the Y-source converter can also be divided into two states: the shoot-through state and the non-shoot-through state.

The capacitor voltage stress in the Y-source converter is known from [12]:

$$V_{C1} = \frac{1-D}{1-\frac{N_1+N_3}{N_3-N_2}D} V_{\text{in}} \tag{1}$$

Where D is defined as the duty cycle of the controllable power switch and N_1, N_2 and N_3 are the winding turns of the coupled inductors.

Then, the output voltage of the Y-source converter is:

$$V_{\text{o}} = \frac{1}{1-K'D} V_{\text{in}} \tag{2}$$

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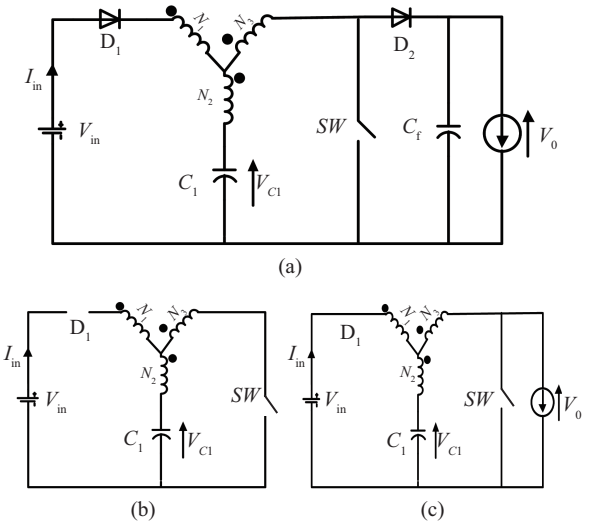


Fig. 1. Illustration of (a) Y-source dc-dc converter, (b) the equivalent circuit in shoot-through state and (c) the equivalent circuit in non-shoot-through state.

where $K' = \dfrac{N_3 + N_1}{N_3 - N_2}$

So when diodes D_1 and D_2 are reverse biased, the reverse bias voltages of the two diodes are:

$$V'_{D1} = (1 - K')V_o \tag{3}$$

$$V'_{D2} = V_o \tag{4}$$

Although the Y-source converter has very prominent advantage, it also has many shortcomings. In this paper, an improved quasi-Y-source converter (IQY) is presented for renewable energy generations, using a Y-source and boost impedance network. Compared with the traditional boost converter, the improved Y-source converter not only has higher voltage-gain, continuous input current and no inrush current, but also has flexible selection of the shoot-through duty ratio range and the turns ratio of the coupled inductors. It is more suitable for new energy generation systems.

II. Proposed Topology and Operating States

The proposed dc-dc converter is shown in Fig. 2, which consist of a quasi-Y-source dc-dc converter combined with a boost converter. The input of the converter is V_{in}, which can come from a photovoltaic power generation system or other dc source. Same as Z-source converters, the proposed converter also has two operating states: (1) SW_1 is on, SW_2 is off, and (2) SW_2 is on, SW_1 is off. Given that the switching cycle is T, T_0 is the turn-on time of SW_1, T_1 is its turn-off time, apparently $T = T_0 + T_1$, so the duty cycle of SW_1 is $D = T_0 / T$. And the equivalent circuits during two operating states are shown in Fig. 3(a) and (b), respectively.

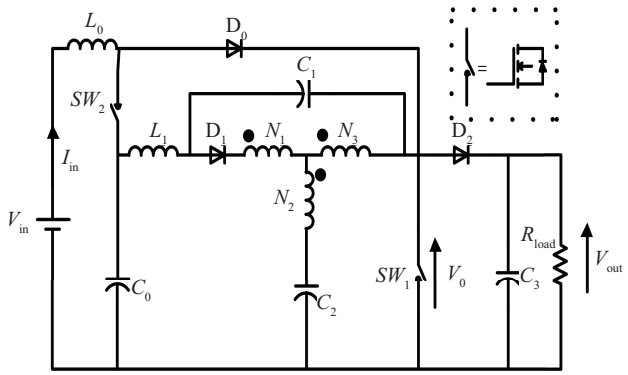


Fig. 2 Illustration of the proposed dc-dc converter.

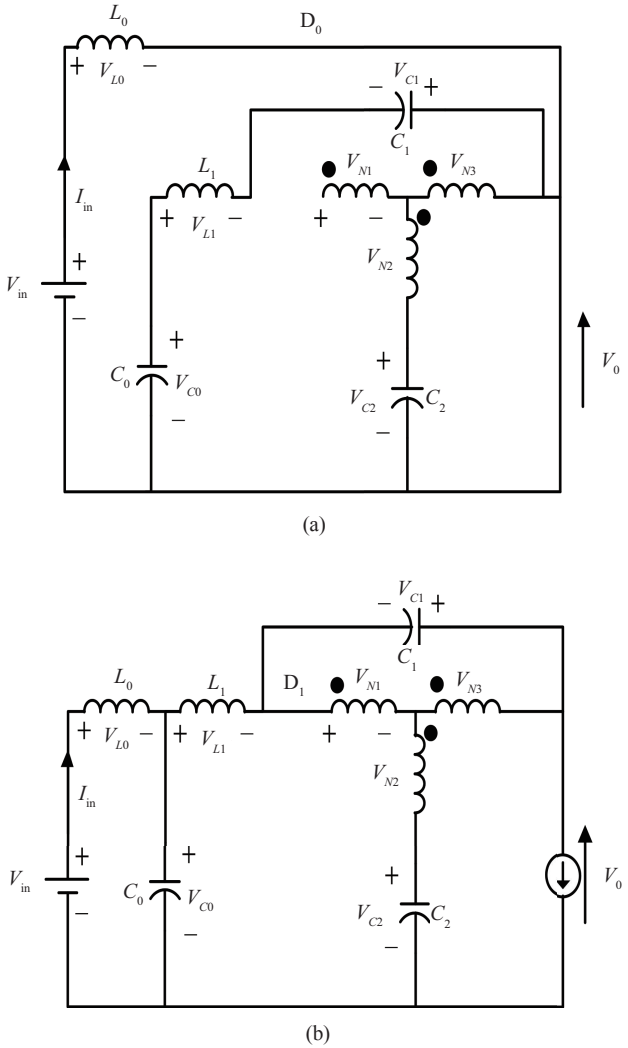


Fig. 3 Equivalent circuits of improved quasi-Y-source converter : (a) SW_1 is on, SW_2 is off and (b) SW_2 is on, SW_1 is off.

In the turn-on time of SW_1, the diode D_0 is turned on and the diode D_1 is in reverse bias state. By applying Kirchhoff's voltage law (KVL) in this mode, the voltage equations in this state are:

$$-V_{in}+V_{L0}=0 \tag{5}$$

$$-V_{C0}+V_{L1}-V_{C1}=0 \tag{6}$$

$$V_{C2}+V_{N2}-V_{N3}=0 \tag{7}$$

$$N_1:N_2:N_3=V_{N1}:V_{N2}:V_{N3} \tag{8}$$

where N_1、N_2 and N_3 are the winding turns of the coupled inductors. By inserting (8) in (7), we have:

$$V_{N2}=\frac{N_2}{N_3-N_2}V_{C2} \tag{9}$$

In the turn-off time of SW_1, the diode D_0 is in reverse bias and the diode D_1 is turned on. From the equivalent circuit diagram, Fig. 3(b), one has:

$$-V_{in}+V'_{L0}+V_{C0}=0 \tag{10}$$

$$-V_{C0}+V'_{L1}-V_{C1}-V_0=0 \tag{11}$$

$$-V_{C0}+V'_{L1}+V'_{N1}+V'_{N2}+V_{C2}=0 \tag{12}$$

$$V_{C1}+V'_{N1}+V'_{N3}=0 \tag{13}$$

By replacing (8) in (13) we will have:

$$V_{C1}+\frac{N_1}{N_2}V'_{N2}+\frac{N_3}{N_2}V'_{N2}=0 \tag{14}$$

Thus:

$$V'_{N2}=-\frac{N_2}{N_1+N_3}V_{C1} \tag{15}$$

By applying voltage-second balance principle to the inductors L_0、L_1 and windings of transformer, the average voltage over the inductor is equal to zero, hence:

$$DV_{L1}+(1-D)V'_{L1}=0 \tag{16}$$

$$DV_{L2}+(1-D)V'_{L2}=0 \tag{17}$$

$$DV_{L0}+(1-D)V'_{L0}=0 \tag{18}$$

By inserting (9) and (15) in (18), we will have:

$$\frac{V_{C1}}{V_{C2}}=\left(\frac{N_1+N_3}{N_2-N_3}\right)\left(\frac{-D}{1-D}\right) \tag{19}$$

Then by combining (6), (8), (12), (15) and (19) in (17) , we have:

$$V_{C0}=\frac{DN_1+(1-D)N_2-(1-2D)N_3}{(1-D)(N_2-N_3)}V_{C2} \tag{20}$$

By replacing (6), (11) and (20) in (17), we will have:

$$V_0=\frac{N_2-N_3}{DN_1+(1-D)N_2-(1-2D)N_3}V_{C0} \tag{21}$$

Defining $K=\frac{N_3+N_1}{N_3-N_2}$, so equation (21) can be rewritten as (22).

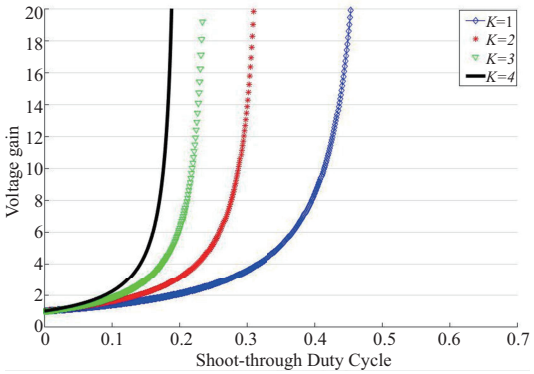


Fig. 4 The theoretical voltage gain of the proposed converter for different winding factors *K*.

$$V_o=\frac{1}{1-(1+K)D}V_{C0} \tag{22}$$

Similarly, by inserting (5) and (10) in (16), we will have:

$$V_{C0}=\frac{1}{1-D}V_{in} \tag{23}$$

Now, using (21) and (23), the voltage gain is obtained as follow:

$$V_o=\frac{1}{[1-(1+K)D](1-D)}V_{in} \tag{24}$$

So when the diode D_1 is in reverse bias state, using (7), (8) and (19), the voltage over D_1 is:

$$V_{D1}=\left(\frac{D}{1-D}-1\right)KV_o \tag{25}$$

When the diode D_2 is in reverse bias state, the voltage over D_2 is:

$$V_{D2}=V_o \tag{26}$$

The overall gain can be varied by changing *D* (the shoot-through duty cycle) and *K* (turn ratios), in order to better illustrate the boosting performance of the proposed converter, which can be depicted in Fig. 4. It will be shown that high transfer gains can be achieved with small shoot-through (ST) duty cycle by increasing the turn ratio *K*. It can be seen from Fig. 4 that the improved quasi-Y-source converter has a higher voltage gain than the conventional Y-source converter. Different winding turns ratios (N_1: N_2: N_3) have been collectively summarized in Table I. The same winding factor *K*, voltage gain and range for *D* have been given in each of these groups.

From (2) and (24), we can know that the voltage gain of the proposed topology is higher than the conventional Y-source converter. As shown in Fig. 5, in order to more intuitively observe the difference between the two topologies, let $K = K' = 3$, and plot the voltage gain curves of the two

TABLE I
GAIN OF PROPOSED CONVERTER VERSUS WINDING FACTOR AND TURNS RATIOS

K	Range of D	Voltage Gain	Possible Turns Ratios N_1: N_2: N_3
1	$0<D<1/2$	$1/(1-2D)(1-D)$	1:1:3, 2:1:4, 1:2:5, 3:1:5 4:1:6, 1:3:7
2	$0<D<1/3$	$1/(1-3D)(1-D)$	1:1:2, 3:1:3, 2:2:4 1:3:5, 4:2:5
3	$0<D<1/4$	$1/(1-4D)(1-D)$	2:1:2, 1:2:3, 4:2:4 5:1:3, 8:1:4
4	$0<D<1/5$	$1/(1-5D)(1-D)$	3:1:2, 2:2:3, 1:3:4 7:1:3, 6:2:4

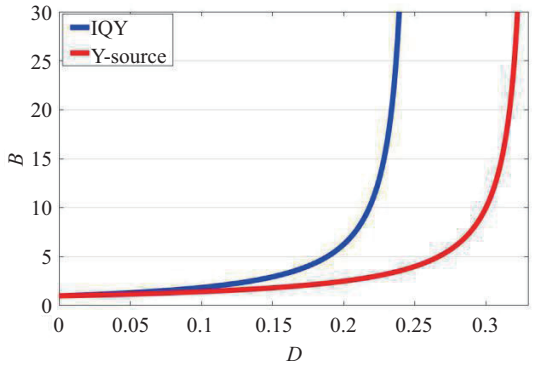


Fig. 5 Theoretical voltage gain of the proposed converter and Y-source converter when the winding factors $K = K' = 3$.

topologies.

From [12], we can know the range of variation for K' and D can be determined as $K' \geqslant 2, D \leqslant \frac{1}{K'}$. Under the same output voltage, the voltage stress of the diode D_2 of the IQY is as large as the Y-source converter, however, the voltage stress of the diode D_1 of the IQY is much smaller than the Y-source converter. From (3) and (25), we have:

$$K \geqslant 1, D \leqslant \frac{1}{1+K} \Rightarrow \begin{cases} 0 < \dfrac{D}{1-D} < 1 \\ K' > 1 + K \end{cases} \tag{27}$$
$$\Rightarrow -1 < \frac{D}{1-D} - 1 < 0 \Rightarrow |V_{D1}| < |K V_o| < |V'_{D1}|$$

Where V_{D1} is the voltage stress of the diode D_1 of the IQY, V'_{D1} is the voltage stress of the diode D_1 of the Y-source converter.

It is worth noting that the leakage inductance between the coupled inductors can't be ignored, which can cause large switching transients and reduce the effective switching duty cycle, resulting in a reduction in the system's voltage gain and efficiency. Therefore, the leakage inductance should be reduced as much as possible.

In summary, in order to better understand the difference between the Y-source converter and the proposed topology, we list the advantages and shortcomings between both of them in the Table II.

TABLE II
THE DIFFERENCE BETWEEN IMPROVED QUASI-Y-SOURCE CONVERTER AND Y-SOURCE CONVERTER

	B	$V_{D1}(V'_{D1})$	Inrush current	Input current
Y-source	$1/(1-KD)$	high	high	Discontinuous
I-QY source	$1/[1-(1+K)D](1-D)$	low	low	Continuous

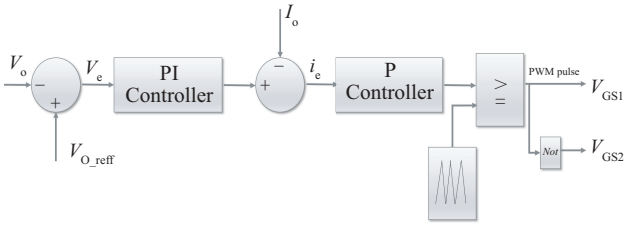


Fig. 6 Control block diagram of the switches.

A double closed loop structure is used in the controller to adjust the output voltage to follow the given. Its inner loop is a current loop that allows the output current to follow the input quickly. The outer voltage loop adopts PI controller to meet the requirements of output stability, and the current inner loop adopts P controller to meet the requirements of rapidity. Besides, the controller also reduces the influence of leakage inductance on the duty cycle. The structure diagram of the controller is shown in Fig. 6. The PWM pulse generated by the controller is used to control the on and off of the switches.

III. SIMULATION AND EXPERIMENTAL RESULTS

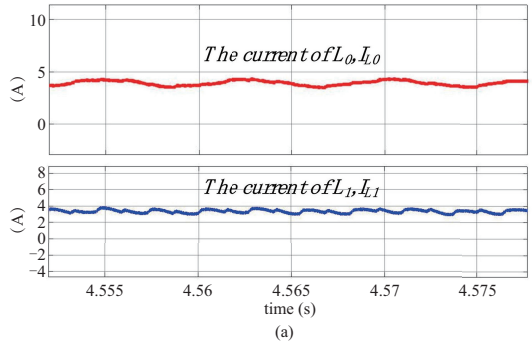
Simulation is performed in MATLAB/Simulink environment, using the parameters listed in Table III, which are also the parameters of the experimental prototype.

According to (24) derived above, when $D = 0.15$ and $V_{in} = 36$ V, the output voltage of the improved quasi-Y-source is theoretically $V_o = 105.9$ V. It can be seen from Fig. 7 that the simulation results are basically consistent with the theoretical values. In addition, it shows that the improved quasi-Y-source converter has high voltage gain, no inrush current and continuous input current.

In order to verify the correctness of the theoretical analysis, a low-power open-loop test prototype is set up in the laboratory. Use the DSP TMS320F2812 to output a set of complementary PWM pulse signals to control the on and off of the switches. Fig. 8 shows a three-winding coupled inductor and a physical circuit diagram. To reduce leakage

TABLE III
PARAMETERS AND COMPONENT VALUES OF THE CONVERTER

Parameter/Description	Value/Part Number
Maximum output power	105 W
Input voltage V_{in}	36 V
Output voltage V_o	105 V
Switching frequency f_s	20 kHz
Turns ratio of coupled inductor	1:3:5 (10:30:50)
Winding factor K	3
Permitted ranges of D	$0<D<0.25$
Inductor L_0 and L_1	500 μH
Capacitor C_1	100 μF/100 V
Capacitor C_0 and C_2	470 μF/160 V
Switching devices SW_1 and SW_2	V_{DS} = 1200 V, I_{DS} = 20 A H20R1203
Diode D_0 and D_1	STPSC20H12-Y-Silicon Carbide Schottky Diode



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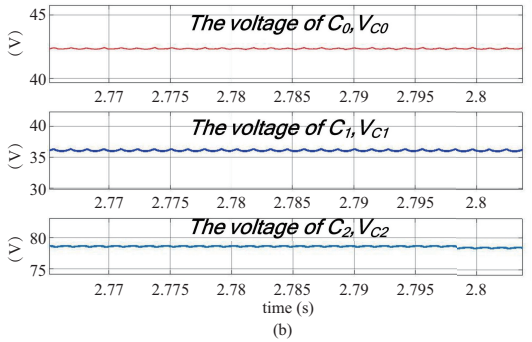

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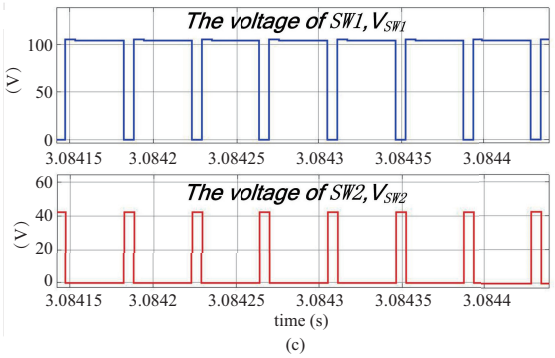

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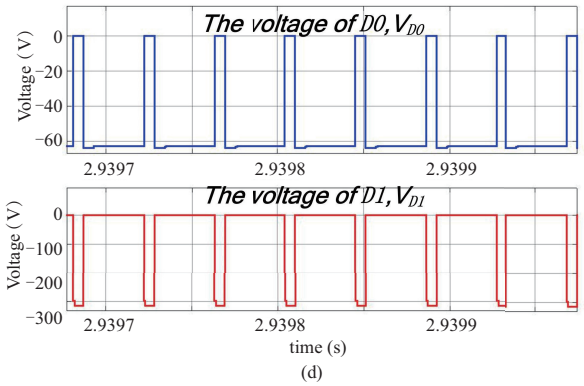

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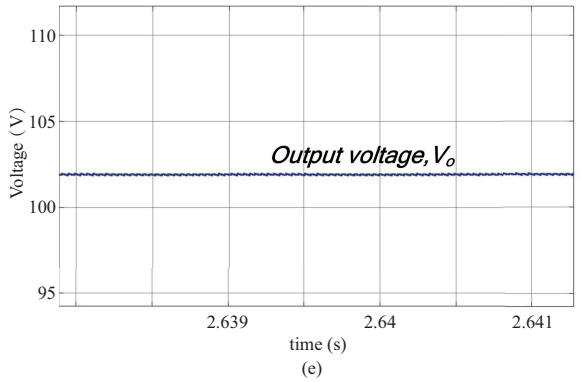


(e)

Fig. 7 Simulation results of improved quasi-Y-source converter at D = 0.15 and K = 3 when V_{in} = 36 V. (a) I_{L0}, I_{L1}. (b) V_{C0}, V_{C1}, V_{C2}. (c) V_{SW1}, V_{SW2}. (d) V_{D0}, V_{D1}. (e) Output voltage V_o.

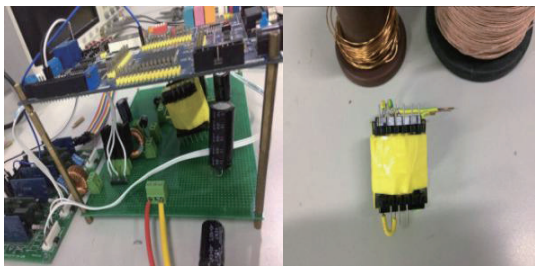
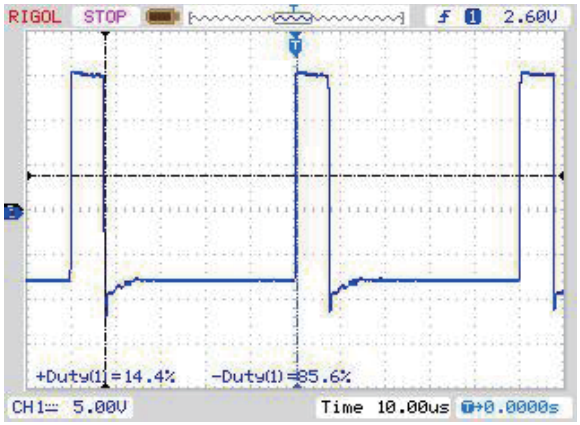


Fig. 8 The experimental setup of proposed converter and three-winding coupled inductor.

inductance, an E-core instead of a toroidal core is used, and a flyback winding is chosen when make the coupled inductor. In this way, the leakage inductance of each winding of the coupled inductor can be controlled within 10 μH. Although the proposed new topology has small leakage inductance, there are still surge voltages and currents. In order to get better output voltage and current waveforms, and protect the controllable power switch, a RCD snubber circuit is added to the circuit, where the parameters of the resistor and capacitor are R = 50 Ω and C = 10 μF, and the diode uses a fast recovery diode.

When D = 0.144 and K = 3, the experimental waveforms of each inductor current, capacitor voltage, the voltages of the controllable switches and the diodes, and output voltage at steady state are shown in Fig. 9. From the experimental



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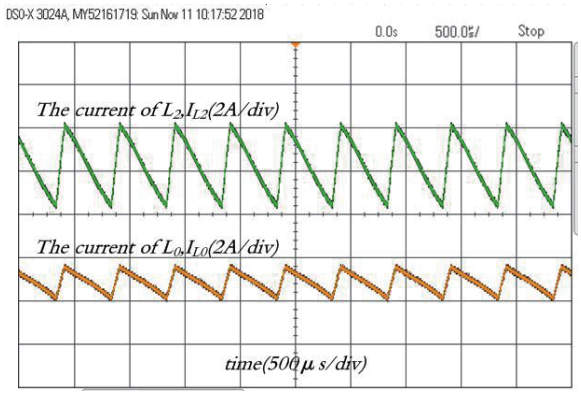

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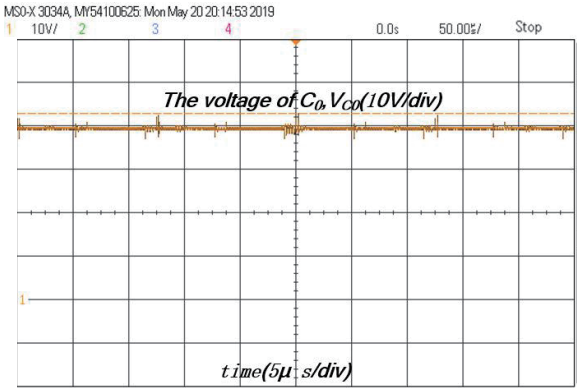

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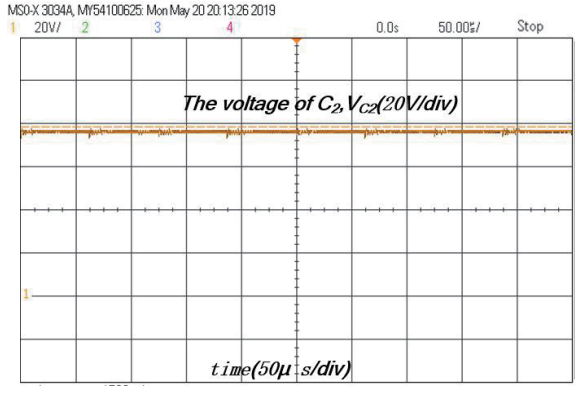

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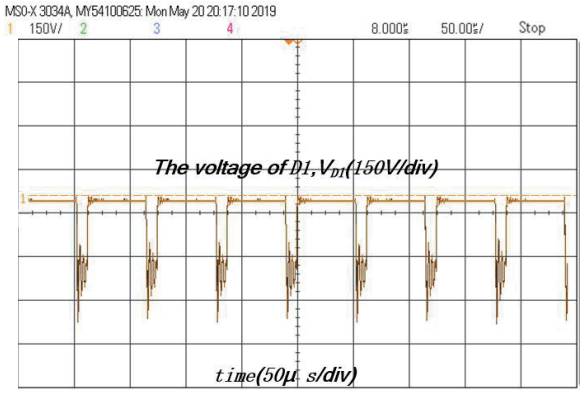

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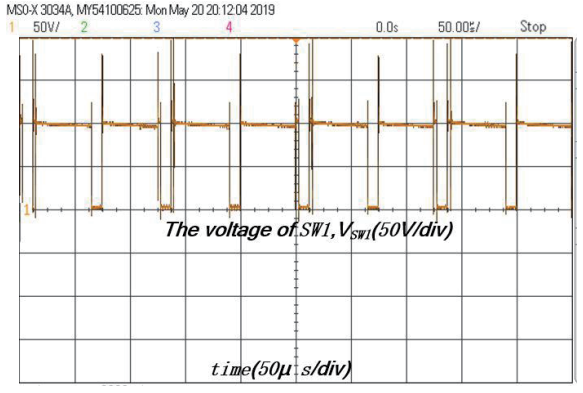

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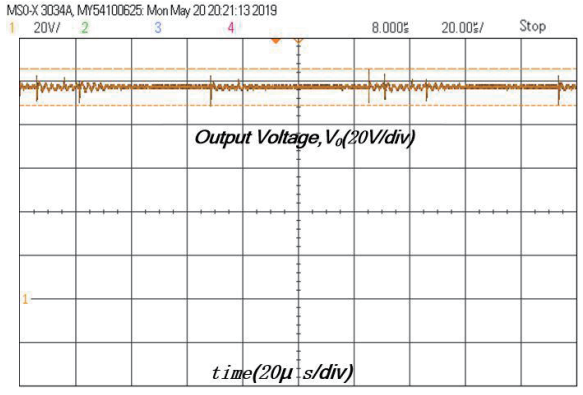

(g)

Fig. 9 Experimental results. (a) The pulse signal of switch SW_1. (b) The current of L_0 and L_1. (c) The voltage of C_0 and C_2. (d) The voltage of C_2. (e) The voltage of D_1. (f) The voltage of SW_1. (g) Output voltage V_o of the improved quasi-Y-source converter when $K = 3$, $D = 0.144$.

waveforms, it can be concluded that the measured values are consistent with the theoretical values and the simulation results.

Fig. 10 shows the measured efficiency and voltage gain of the converter at $K = 3$, where D changes to keep the output voltage constant at 105 V. It can be seen from this figure that the recorded efficiency is the highest when $D = 0.05$, which is 96.2%. At $D = 0.2$, it drops to 89.9%. The drop in efficiency may be related to a large breakdown current, which can cause large leakage current and reduce the

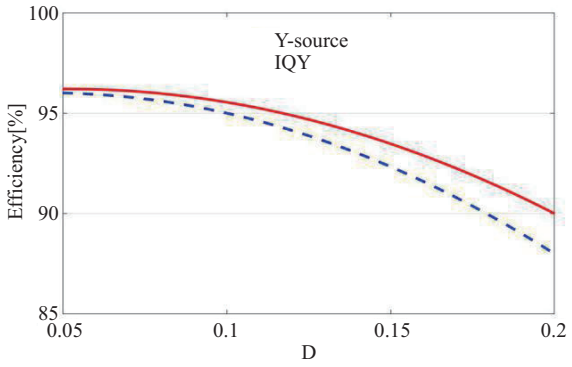

Fig. 10 The measured efficiency of the Y-source converter and IQY converter when $K = 3$ and $0.05 \leqslant D \leqslant 0.2$.

effective switching duty cycle, resulting in a reduction in the system's voltage gain and efficiency, which can be reduced by using better wire or bus-bar to reduce the parasitic parameters and the stray losses. As for the efficiency of the Y-source converter, it becomes lower at higher duty cycles because it is more affected by the leakage inductance.

IV. Conclusions

In this paper, a new type of improved quasi-Y-source dc-dc converter based on the traditional quasi-Y-source structure is introduced, which own all the benefits of the existing Y-source dc-dc converter, such as extremely high boost gain and flexibility in designing winding magnetics. In addition, the converter has higher voltage gain, continuous input current and small starting inrush current. Undoubtedly, it is better than the quasi-Y-source converter for renewable energy systems. The mathematical derivation and experimental results for verification clearly demonstrates the expected performance of the proposed dc-dc converter and its practicality.

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Open-Loop Power Sharing Characteristic of a Three-Port Resonant LLC Converter

Yan-Kim Tran, Francisco D. Freijedo, and Drazen Dujic

***Abstract*—The Solid State Transformer (SST) is an attractive solution for highly flexible, cost-effective, compact and efficient power transfer among different grids. Furthermore, a three-port topology is proven as a suitable solution to integrate energy storage resources, the key functionality of emerging SST concept. Among other alternatives, the resonant LLC series resonant converter (SRC) is the cost-effective solution to implement the DC-transformer functionality, which is a core part of the SST. This paper addresses the power sharing characteristics and the zero-voltage switching (ZVS) conditions of a galvanically isolated three-port SRC, operated in DC-transformer mode. A mathematical model, which effectively decouples principal from circulating currents and power flows, is proposed and developed. This new mathematical framework eases the analysis; and reveals a constant power sharing characteristic tightly dominated by the resonant tank parameters even though some degrees of freedom are allowed thanks to the introduction of a differential voltage at the input terminals. Subsequently, design aspects and assessments of working operation conditions are also reported. The accuracy of the proposed model is verified by experimental validation on a lab-scale prototype.**

***Index Terms*—DC-DC converters, medium-voltage DC (MVDC), multiport, resonant converter, solid state transformer.**

I. Introduction

SOLID State Transformer (SST) defines an emerging technology aiming for a more reliable, flexible, compact and efficient alternative to bulky line-frequency transformers (LFTs). The SST concept includes power conversion among DC and/or AC grids of a different kind [1]–[4]. The high expectations from SST solutions also include new functionalities, such as integration of energy storage, which can be made by multi-port topologies [5]–[10]. SST is already a competitive solution in several applications such as traction propulsion chain [11], [12], on-board distribution networks for marine [13], [14], photovoltaic parks [15], offshore wind-farms [16], data centers [17], or distribution in urban areas [18].

Fig. 1 shows a three-port SST solution with integrated energy storage. The overall system comprises two main kinds of subsystems: (i) DC external grids, which are interfaced by an active front-end that tightly regulate voltage/current/power at their terminals; different high level regulation strategies may be considered at this stage [1]–[4]. (ii) The DC-transformer

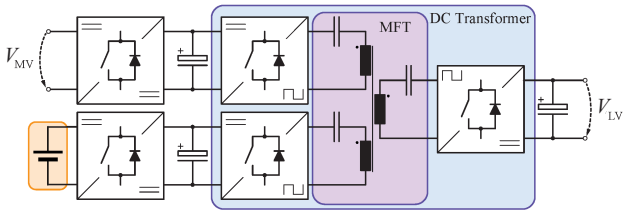

Fig. 1. A three-port SST with integrated energy storage, interfacing a medium voltage (MV) DC-grid and a low voltage (LV) DC-grid. The core of the system is a three-port resonant DC-transformer. Two active regulation stages are added in order to control the power through the DC voltage on the MV and the storage side.

operation is implemented using a three-port LLC series resonant converter; it provides voltage adaptation, natural power sharing and galvanic isolation among the different electric subsystems (in a similar manner as LFT) [4], [11], [12]. It provides a tight voltage coupling between the three ports and may, therefore, be operated in open-loop; the power conversion blocks work at a relatively high switching frequency that allows to drastically decrease the size of the so-called medium frequency transformer (MFT) [4], [11], [12], [19], [20].

Meanwhile, there is an ever increasing number of works focused on the system-level advantages of SST, the state-of-the-art addressing multi-port SRC based DC-transformer contains only a few works [5]–[10]. From these works, there is an overall agreement that the resonant frequency has to be the same for all the ports, which implies a careful design of the resonant tank and parameters as well as the operation with 50% duty cycle and equal switching frequency for all the active terminals. The suitability for integration of low vottage (LV) storage elements (batteries or ultra-capacitors) is presented in [8]. Clearly, besides the feasibility of the multi-port SRC topologies, a systematic and rigorous mathematical analysis describing the natural power sharing principles is not available in the literature. The systematic evaluation is needed to address the limits of the topology and derive design rules that permit to consider the technology at an industry level. And even though the modelling with the well known First Harmonic Approximation (FHA) [6], [7] is possible, the detailed description of the waveforms, required for the soft switching and the losses evaluation is not captured by this method.

To cover the lack of analysis that may help in the elaboration of design rules, this paper presents a rigorous mathematical modeling of the three-port LLC-based DC transformer; the natural power sharing, as a function of the MFT parameters, is derived and characterized. To do so, an equivalent model that simplifies significantly the original mathematical model of the

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multi-port DC transformer, but still enables the precision required for the soft switching characterization, is proposed. Subsequently, it is discussed how the natural power sharing can be modified by acting on the input voltages; the influence of the source voltages is accurately quantified using the proposed model. This part of the analysis gives an idea of how effective is SST regulation at an interface level (point i) of the operation described above). The conditions that lead to a loss of zero-voltage switching (ZVS) operation, and hence to a potential efficiency drop, are also identified from the equivalent model provided. Comprehensive experimental tests fully verify the theoretical modelling and, therefore, validate the proposed design insights.

The organization of the rest of the paper is summarized as follows. The next section presents the problem description and the modelling challenges to provide self-contained design guidelines. Section III shows the proposed mathematical approach, which is based on a change of variable that allows obtaining two equivalent decoupled systems. Section IV derives the power sharing characteristics as a function of the MFT parameters, input-voltages and losses. Section V shows the ZVS regions for the DC-transformer operation. Section VI shows and discusses the experimental results. Finally, the conclusion summarizes the most important findings.

II. Circuit and Problem Description

While all three ports are made from active switching elements, they can be operated with active switching actions or be used as passive diode rectifier, depending on the power flow. The mode of operation analyzed in details in this paper, considering the DC-transformer with two inputs and one output, is depicted in Fig. 2. The circuit includes a three-winding MFT with the number of turns given by n_1, n_2, n_3. The input ports (1 and 2) are active sources equipped with two resonant tanks of the identical resonant frequency f_{res} composed by the capacitors C_1 and C_2' combined with the leakage inductance L_1 and L_2'. The third port acts as a passive load. The semiconductors of the input ports are switched at the same fixed frequency with a constant duty-cycle of 50% and the same phase [10]. In order to benefit not only from ZVS [21] and reduced turn-off current on the primary switches but also from zero-current switching (ZCS) on the secondary diode rectifier, the switching frequency is set slightly below the resonant frequency ($f_{sw} < f_{res}$) [22]. The DC bus capacitors C_{DC} are sized much bigger than the resonant capacitors, so, for the purpose of modelling their voltage V_{DC} can be considered constant; i.e., square-wave voltage sources of amplitude $V_1 = V_{CD_1}/2$ and $V_2' = V_{CD_2}'/2$ are considered. The power transferred to the load port ($P_{load} = P_3$) is the sum of both contributions P_1 and P_2 from each active ports.

The converter is sized to be operated in a half-cycle discontinuous mode (HC-DCM) [23] over its complete operating range [10]. Thus two intervals can be identified per half-period, as depicted in Fig. 3 and detailed in the following. It may also be noticed that, for modelling purposes, the circuit parameters L_2', C_2' , V_2' and V_3' are referred to the port 1 of the transformer and represented by $L_2 = L_2' n_1^2/n_2^2$, $C_2 = C_2' n_2^2/n_1^2$, $V_2 = V_2' n_1/ n_2$ and $V_3 = V_3' n_1/n_3$ (for the sake of simplicity,

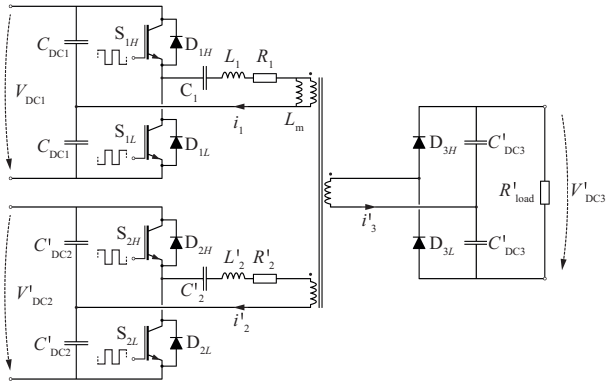

Fig. 2. Topology of a three-port resonant DC-DC converter working as DC transformer (two actively switched ports and one passive load).

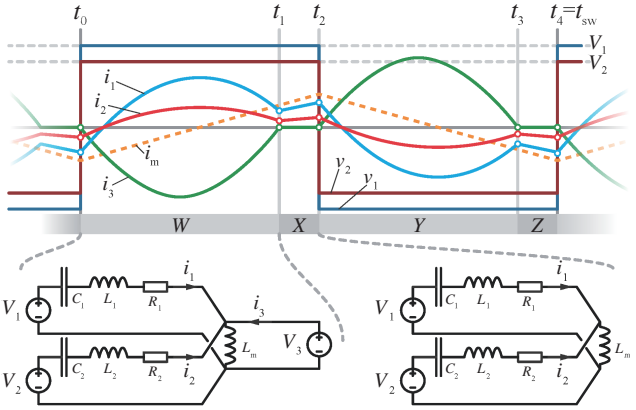

Fig. 3. Equivalent circuits and steady state voltage and current waveforms during the two different intervals of three-port DC transformer operation.

a loss-less converter without parasitic resistances, i.e., $R_1 = R_2 = 0$, is considered firstly). During the interval W, the two active ports are delivering power to the load as well as the magnetizing current i_m; the voltage seen at the magnetizing inductance terminals is clamped by the voltage on the load port due to the conduction of the diodes [9], [10]. When the output diode rectifier stops conducing, interval X starts. The two active ports are only supporting i_m, and the magnetizing inductance terminals are no longer clamped, while the load is supported by the output capacitors. Intervals Y and Z are the same as W and X respectively with opposite voltage and current polarity. The circuit time-domain equations should be calculated for each interval. For the interval W, the two input (k = 1, 2) voltages, and currents are given respectively by:

$$\begin{aligned} v_k(t) &= v_{C_k}^{W}(t) + L_k \frac{\mathrm{d}i_k^{W}(t)}{\mathrm{d}t} + v_3(t) \\ i_k(t) &= C_k \frac{\mathrm{d}v_{C_k}^{W}(t)}{\mathrm{d}t}. \end{aligned} \tag{1}$$

The voltage and current of the third port (output) are given by:

$$\begin{aligned} v_3(t) &= L_m \frac{\mathrm{d}i_m^{W}(t)}{\mathrm{d}t} \\ i_3^{W}(t) &= -i_1^{W}(t) - i_2^{W}(t) + i_m^{W}(t). \end{aligned} \tag{2}$$

The Laplace transform with initial conditions is considered to obtain time-domain expressions. From the step response at $t = 0$, and assuming ideal voltage sources, of amplitudes V_1, V_2 and V_3, respectively:

$$\begin{aligned}\frac{V_1}{s} &= \frac{v_{C_1}(t_0)}{s} + \frac{1}{sC_1}i_1^W(s) + sL_1 i_1^W(s) - L_1 i_1(t_0) + \frac{V_3}{s}\\ \frac{V_2}{s} &= \frac{v_{C_2}(t_0)}{s} + \frac{1}{sC_2}i_2^W(s) + sL_2 i_2^W(s) - L_2 i_2(t_0) + \frac{V_3}{s}\\ i_{\mathrm{m}}^W(s) &= \frac{V_3}{s^2 L_{\mathrm{m}}} + \frac{i_1(t_0) + i_2(t_0)}{s}.\end{aligned} \tag{3}$$

Expressions for $i_1(s)$ and $i_2(s)$ can be simplified by introducing $\omega^2 = 1/(L_1C_1) = 1/(L_2C_2)$, which gives (for $k = 1, 2$):

$$i_k^W(s) = \left(\frac{V_k - v_{C_k}(t_0) - V_3}{\omega L_k}\right)\frac{\omega}{\omega^2 + s^2} + i_k(t_0)\frac{s}{\omega^2 + s^2} \tag{4}$$

Back in time domain, it yields:

$$i_k^W(t) = i_k(t_0)\cos(\omega t) + \left(\frac{V_k - v_{C_k}(t_0) - V_3}{\omega L_k}\right)\sin(\omega t) \tag{5}$$

and

$$i_{\mathrm{m}}^W(t) = i_1(t_0) + i_2(t_0) + \frac{V_3}{L_{\mathrm{m}}}t. \tag{6}$$

For the interval X, the voltage equations are:

$$\begin{aligned}V_1 &= v_{C_1}^X(t) + L_1\frac{\mathrm{d}i_1^X(t)}{\mathrm{d}t} + L_{\mathrm{m}}\frac{\mathrm{d}(i_1^X(t) + i_2^X(t))}{\mathrm{d}t}\\ V_2 &= v_{C_2}^X(t) + L_2\frac{\mathrm{d}i_2^X(t)}{\mathrm{d}t} + L_{\mathrm{m}}\frac{\mathrm{d}(i_1^X(t) + i_2^X(t))}{\mathrm{d}t}.\end{aligned} \tag{7}$$

Using the Laplace transform and the initial conditions $i_1(t_1)$, $i_2(t_1)$, $v_{C_1}(t_1)$ and $v_{C_2}(t_1)$:

$$\begin{aligned}\frac{V_1}{s} &= \frac{v_{C_1}(t_1)}{s} + \frac{1}{sC_1}i_1^X(s) + sL_1 i_1^X(s) - L_1 i_1(t_1) + v_{\mathrm{m}}^X(s)\\ \frac{V_2}{s} &= \frac{v_{C_2}(t_1)}{s} + \frac{1}{sC_2}i_2^X(s) + sL_2 i_2^X(s) - L_2 i_2(t_1) + v_{\mathrm{m}}^X(s).\end{aligned} \tag{8}$$

And subsequently, it yields:

$$\begin{aligned}i_1^X(s) &= \left(\frac{V_1}{s} - \frac{v_{C_1}(t_1)}{s} + L_1 i_1(t_1) - v_{\mathrm{m}}^X(s)\right)\frac{1}{\frac{1}{sC_1} + sL_1}\\ i_2^X(s) &= \left(\frac{V_2}{s} - \frac{v_{C_2}(t_1)}{s} + L_2 i_2(t_1) - v_{\mathrm{m}}^X(s)\right)\frac{1}{\frac{1}{sC_2} + sL_2}\\ v_{\mathrm{m}}^X(s) &= sL_{\mathrm{m}}(i_1(s) + i_2(s)) - L_{\mathrm{m}}(i_1(t_1) + i_2(t_1)).\end{aligned} \tag{9}$$

Solving the system given by the equations (9), the three currents in the interval X become:

$$\begin{aligned}i_1^X(t) &= A\cos(\omega t) + B\sin(\omega t)\\ &\quad + \frac{L_2}{L_1 + L_2}(C\cos(\omega_X t) + D\sin(\omega_X t))\\ i_2^X(t) &= -A\cos(\omega t) - B\sin(\omega t)\\ &\quad + \frac{L_1}{L_1 + L_2}(C\cos(\omega_X t) + D\sin(\omega_X t))\\ i_{\mathrm{m}}^X(t) &= C\cos(\omega_X t) + D\sin(\omega_X t)\end{aligned} \tag{10}$$

with the constants being equal to:

$$\begin{aligned}A &= \frac{L_1}{L_1 + L_2}i_1(t_1) - \frac{L_2}{L_1 + L_2}i_2(t_1)\\ B &= \frac{V_1 - V_2 - v_{C_1}(t_1) + v_{C_2}(t_1)}{\omega(L_1 + L_2)}\\ C &= i_1(t_1) + i_2(t_1)\\ D &= \frac{L_2(V_1 - v_{C_1}(t_1)) + L_1(V_2 - v_{C_2}(t_1))}{\omega_X(L_1L_2 + L_1L_{\mathrm{m}} + L_2L_{\mathrm{m}})}\\ \omega_X &= \sqrt{\frac{1}{\left(\frac{L_1L_2}{L_1 + L_2} + L_{\mathrm{m}}\right)(C_1 + C_2)}}.\end{aligned} \tag{11}$$

By inspection of (10) and (11), the two input subsystems are strongly coupled during the X interval. Eventually, in the search for insightful design guidelines, dealing with a high order highly coupled model has been found forbiddingly complex. Alternatively, a change of variable taking into account the topology is proposed, as detailed in the next section.

III. Proposed Model

A systematic analytic development, based on changes of variable, which permits to derive power sharing rules is provided in this section. The idea is to obtain a set of variables that are decoupled during all the intervals. Looking at the parallel/series symmetries in Fig. 2, the following substitutions in (5) and (10) are proposed. A common mode equivalent or parallel combination of the input ports is identified. The input voltage and current become

$$\begin{aligned}v_{\mathrm{P}}(t) &= \frac{L_2 v_1(t) + L_1 v_2(t)}{L_1 + L_2}\\ i_{\mathrm{P}}(t) &= i_1(t) + i_2(t)\end{aligned} \tag{12}$$

while the parallel equivalent resonant tank is given by

$$\begin{aligned}L_{\mathrm{P}} &= \frac{L_1L_2}{L_1 + L_2}\\ C_{\mathrm{P}} &= C_1 + C_2.\end{aligned} \tag{13}$$

Then, the differential mode equivalent is characterized by the voltage and current expressed as

$$v_S(t) = v_1(t) - v_2(t)$$
$$i_S(t) = \frac{L_1}{L_1 + L_2} i_1(t) - \frac{L_2}{L_1 + L_2} i_2(t). \quad (14)$$

The series combination of the resonant tank gives

$$L_S = L_1 + L_2$$
$$C_S = \frac{C_1 C_2}{C_1 + C_2}. \quad (15)$$

The "P" and "S" subscripts refer to parallel and series equivalents, but may be also related to common and differential modes. After substituting original variables by "P" and "S" equivalents, the interval *W* circuit is described by

$$i_S^W(t) = i_S(t_0)\cos(\omega t) + \left(\frac{V_S - v_{C_S}(t_0)}{\omega L_S}\right)\sin(\omega t) \quad (16)$$

$$i_P^W(t) = i_P(t_0)\cos(\omega t) + \left(\frac{V_P - v_{C_P}(t_0) - V_3}{\omega L_P}\right)\sin(\omega t). \quad (17)$$

Similarly, for the interval *X*

$$i_S^X(t) = i_S(t_1)\cos(\omega t) + \left(\frac{V_S - v_{C_S}(t_1)}{\omega L_S}\right)\sin(\omega t) \quad (18)$$

$$i_P^X(t) = i_P(t_1)\cos(\omega_X t) + \left(\frac{V_P - v_{C_P}(t_1)}{\omega_X (L_P + L_m)}\right)\sin(\omega_X t). \quad (19)$$

It is worth noting that $i_S^W(t)$ and $i_S^X(t)$ can be merged in

$$i_S(t) = i_S(t_0)\cos(\omega t) + \left(\frac{V_S - v_{C_S}(t_0)}{\omega L_S}\right)\sin(\omega t) \quad (20)$$

which holds valid for all intervals defined by $(0, t_{sw}/2)$.

After the transformation, two fully decoupled "P" and equivalent systems are obtained. The sub-circuits correspond to each circuit and interval are depicted in Figs. 4 and 5. By inspection of Figs. 4 and 5, the power delivery to the load depends on the "P" circuit, meanwhile the "S" circuit represents power re-circulation between the sources.

IV. Power Sharing Expressions

As early mentioned, the ideal loss-less case is considered firstly (in order to ease the mathematical development). However, the losses are also included in subsection IV-B, since they have a relevant role in the power sharing characteristics.

A. Ideal Case

The power delivered to the load is modelled in the "P" circuit (cf., Fig. 4), which is defined by

$$\langle P_P \rangle = \frac{1}{t_{sw}} \int_0^{t_{sw}} v_P(t) i_P(t) \mathrm{d}t = \frac{2V_P}{t_{sw}} \int_0^{t_{sw}/2} i_P(t) \mathrm{d}t. \quad (21)$$

It should be noticed that "S" circuit is purely reactive (cf., Fig. 5), so

$$\int_0^{t_{sw}/2} i_S(t)\,\mathrm{d}t = 0. \quad (22)$$

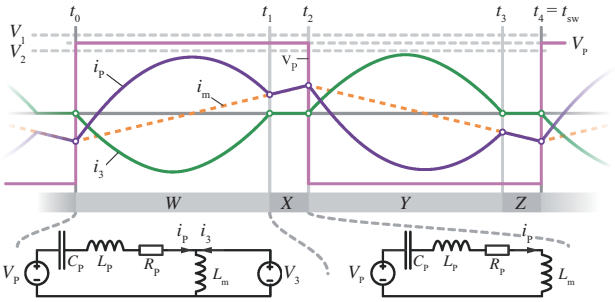

Fig. 4. "P" equivalent intervals and sub-circuits (common mode power component).

The average power transferred to the load by each active port ($k = 1, 2$) is given by

$$\langle P_k \rangle = \frac{2}{t_{sw}} \int_0^{t_{sw}/2} v_k(t) i_k(t)\,\mathrm{d}t = \frac{2V_k}{t_{sw}} \int_0^{t_{sw}/2} i_k(t)\,\mathrm{d}t. \quad (23)$$

Development of this expression for the port 1, and also having into account (22) and the changes of variable in (12) to (15), gives

$$\begin{aligned}\langle P_1 \rangle &= \frac{L_2}{L_1 + L_2} \frac{2V_P}{t_{sw}} \int_0^{t_{sw}/2} i_P(t)\,\mathrm{d}t \\ &\quad + \frac{2V_S L_1 L_2}{t_{sw}(L_1 + L_2)^2} \int_0^{t_{sw}/2} i_P(t)\,\mathrm{d}t \\ &= \frac{L_2}{L_1 + L_2}\langle P_P \rangle + \frac{L_1 L_2}{(L_1 + L_2)^2} \frac{V_S}{V_P} \langle P_P \rangle.\end{aligned} \quad (24)$$

And, for the second port

$$\langle P_2 \rangle = \frac{L_1}{L_1 + L_2}\langle P_P \rangle - \frac{L_1 L_2}{(L_1 + L_2)^2} \frac{V_S}{V_P} \langle P_P \rangle. \quad (25)$$

By inspection of (24) and (25), in a rated condition, the part of the total power that corresponds to each port is a function of the MFT leakage inductances. A deviation from the ratio is caused by the presence of a differential voltage V_S (which may be regulated outside the resonant multi-port stage), but will, in practice, remain rather small as $V_S << V_P$ is expected.

At this point, it is key to stress that the "P" and "S" equivalents permit to calculate the power sharing rules without needing to solve the initial conditions of the circuit, which drastically eases the analysis and reveals design rules insights based on natural power sharing characteristics.

Anyway, as the equivalent circuits "P" and "S" are fully decoupled, the steady-state boundary conditions may be calculated solving:

$$\begin{aligned} i_{\mathrm{P}}^{W}(t_0) &= -i_{\mathrm{P}}^{X}(t_2) \\ v_{C_{\mathrm{P}}}^{W}(t_0) &= -v_{C_{\mathrm{P}}}^{X}(t_2) \\ i_{\mathrm{S}}^{W}(t_0) &= -i_{\mathrm{S}}^{X}(t_2) \\ v_{C_{\mathrm{S}}}^{W}(t_0) &= -v_{C_{\mathrm{S}}}^{X}(t_2). \end{aligned} \tag{26}$$

These expressions are employed to assess the ZVS conditions, in Section V.

1) Worst Case Analysis for Tolerances of the Resonant Tank Parameters

If tolerance values are considered for the resonant tank parameters, the assumption of an identical resonant frequency for both resonant tanks, used to get (4), is no longer valid and $\omega_1 = \sqrt{1/L_1 C_1} \neq \omega_2 = \sqrt{1/L_2 C_2}$. The expressions for power sharing becomes:

$$\begin{aligned} <P_1> = &\frac{L_2\omega_2}{L_1\omega_1 + L_2\omega_2} <P_{\mathrm{P}}> \\ &+ \frac{L_1 L_2 \omega_1 \omega_2}{(L_1\omega_1 + L_2\omega_2)^2} \frac{V_{\mathrm{S}}}{V_{\mathrm{P}}} <P_{\mathrm{P}}>. \end{aligned} \tag{27}$$

And, for the second port

$$\begin{aligned} <P_2> = &\frac{L_1\omega_1}{L_1\omega_1 + L_2\omega_2} <P_{\mathrm{P}}> \\ &- \frac{L_1 L_2 \omega_1 \omega_2}{(L_1\omega_1 + L_2\omega_2)^2} \frac{V_{\mathrm{S}}}{V_{\mathrm{P}}} <P_{P}>. \end{aligned} \tag{28}$$

Assuming $V_{\mathrm{S}} = 0$,

$$<P_1> = \frac{\sqrt{L_2/C_2}}{\sqrt{L_2/C_2} + \sqrt{L_1/C_1}} <P_{\mathrm{P}}>. \tag{29}$$

And, for the second port

$$<P_2> = \frac{\sqrt{L_1/C_1}}{\sqrt{L_1/C_1} + \sqrt{L_2/C_2}} <P_{\mathrm{P}}>. \tag{30}$$

The worst case scenarios correspond to the values that maximize/minimize $< P_1 >$ and $< P_2 >$; by inspection of (29) and (30) these correspond to the combinations of i) ($L_1^{\min}$, $C_1^{\max}$, $L_2^{\max}$, $C_2^{\min}$) and ii) ($L_1^{\max}$, $C_1^{\min}$, $L_2^{\min}$, $C_2^{\max}$).

B. Consideration of System Losses

The circuit losses during operation, such as conduction and switching ones, are reflected on the system dynamics and, therefore, can be modeled by equivalent resistors [24]. An a priory estimation of their values is a complex task, but they can be measured from the experimental curves [24]. Equivalent series resistors per port (i.e., R_1 and R_2) are included in the analysis, with $R_1/L_1 \approx R_2/L_2$ being assumed. Subsequently, the "P" and "S"equivalents are defined as

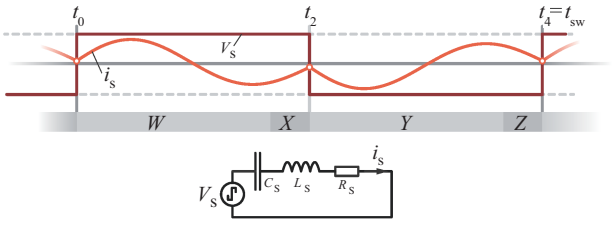

Fig. 5. "S" equivalent intervals and sub-circuits (differential mode power component).

$$R_{\mathrm{P}} = \frac{R_1 R_2}{R_1 + R_2} \quad \text{and} \quad R_{\mathrm{S}} = R_1 + R_2. \tag{31}$$

Figs. 4 and 5 already include these terms. (23) is re-calculated considering the voltage drops at R_{P} and R_{S} and also taking into account that (22) is no longer true (i.e., "S" circuit is not purely reactive) and gives:

$$\begin{aligned} <P_1> = &\frac{L_2}{L_1 + L_2} <P_{\mathrm{P}}> + \frac{L_1 L_2}{(L_1 + L_2)^2} \frac{V_{\mathrm{S}}}{V_{\mathrm{P}}} <P_{\mathrm{P}}> \\ &+ <P_{\mathrm{S}}> + \frac{L_2}{L_1 + L_2} < P_{\mathrm{P_{loss}}} > + \frac{L_1}{L_1 + L_2} < P_{\mathrm{S_{loss}}} > \\ <P_2> = &\frac{L_1}{L_1 + L_2} <P_{\mathrm{P}}> - \frac{L_1 L_2}{(L_1 + L_2)^2} \frac{V_{\mathrm{S}}}{V_{\mathrm{P}}} <P_{\mathrm{P}}> \\ &- <P_{\mathrm{S}}> + \frac{L_1}{L_1 + L_2} < P_{\mathrm{P_{loss}}} > + \frac{L_2}{L_1 + L_2} < P_{\mathrm{S_{loss}}} >. \end{aligned} \tag{32}$$

The losses are included within the new terms in (32):

$$\begin{aligned} <P_{\mathrm{P_{loss}}}> &= \frac{R_{\mathrm{P}}}{t_{\mathrm{sw}}} \int_0^{t_{\mathrm{sw}}} i_{\mathrm{P}}^2(t)\mathrm{d}t \\ <P_{\mathrm{S_{loss}}}> &= \frac{R_{\mathrm{S}}}{t_{\mathrm{sw}}} \int_0^{t_{\mathrm{sw}}} i_{\mathrm{S}}^2(t)\mathrm{d}t \\ <P_{\mathrm{S}}> &= V_{\mathrm{P}} \frac{2}{t_{\mathrm{sw}}} \int_0^{t_{\mathrm{sw}}/2} i_{\mathrm{S}}(t)\mathrm{d}t. \end{aligned} \tag{33}$$

It has to be noted that the active component of the differential current $i_{\mathrm{S}}(t)$ is due to the presence of R_{S}. In order to simplify the notation, the factor k_{12} and k_{21} are introduced and are given by:

$$\begin{aligned} k_{12} &= \frac{L_2}{L_1 + L_2} \\ k_{21} &= \frac{L_1}{L_1 + L_2} \end{aligned} \tag{34}$$

Since k_{12} and k_{21} are smaller than 1 and $V_{\mathrm{S}} << V_{\mathrm{P}}$, the second term of (32) becomes very small and can be neglected. If the same is applied to the losses, which are also expected very small, (32) can be simplified in (35) which leads to the graphical representation of Fig. 6.

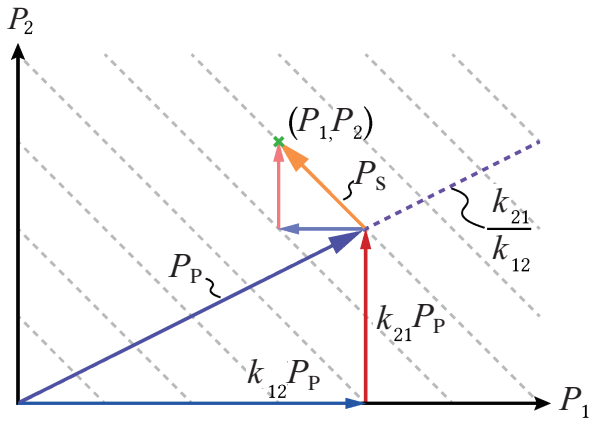

Fig. 6. Graphical representation of P_1 and P_2 in function of P_P and P_S. The axis where $P_S = 0$ is defined by the resonant tank design with k_{12} and k_{21}.

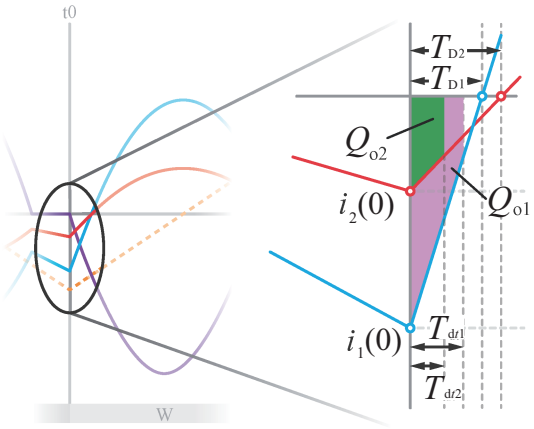

Fig. 7. Variables that set ZVS conditions.

$$\begin{aligned} <P_1> &\simeq k_{12}<P_P> + <P_S> \\ <P_2> &\simeq k_{21}<P_P> - <P_S> \end{aligned} \tag{35}$$

V. Assessment of ZVS Operation

ZVS operation is defined electrically by a set of conditions described in Fig. 7. First, during the turn-on event of a semiconductor, the dead time $T_{dt,k}$ (adequately applied for the selected semiconductor voltage class) must be shorter than $T_{D,k}$ (according to Fig. 7, this interval starts with a load switching event and ends when $i_k(t)$ crosses zero): i.e,

$$T_{dt,k} < T_{D,k} \quad \text{for } k = 1, 2. \tag{36}$$

Second, the current flowing through the switch during $T_{dt,k}$ must be large enough to charge the output capacitance $C_{oes,k}$ (available from semiconductor data-sheet): from 0 to $V_{dc,k}$ during the turning off; from $V_{dc,k}$ to 0 during the turning on. This condition can be mathematically described by

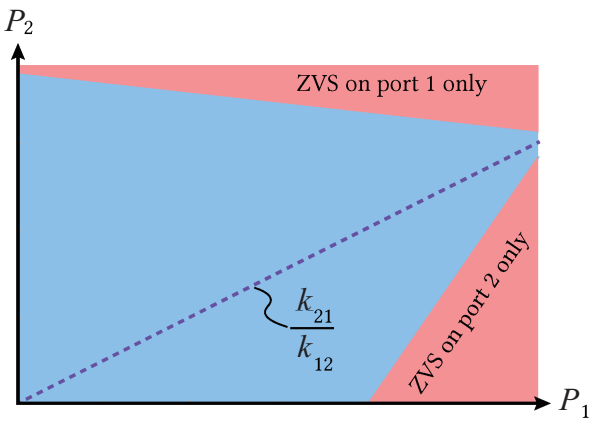

Fig. 8. Theoretical ZVS operation area. It shows that the ZVS region is well impacted by the design of the resonant tank, with k_{21}/k_{12}.

$$Q_{o,k} = \int_0^{T_{dt,k}} i_k(t)\,dt > 2V_{dc,k}C_{oes,k} \quad \text{for } k = 1, 2. \tag{37}$$

with $Q_{o,k}$ being the integral of current during $T_{dt,k}$. For a given operation point, $Q_{o,k}$ can be approximated by the area of the trapeze defined by:

$$Q_{o,k} = \frac{T_{dt,k}\,i_k(0)}{2}\left(1 + \frac{T_{dt,k}}{T_{D,k}}\right) \tag{38}$$

Currents $i_1(t)$ and $i_2(t)$ are needed to assess ZVS conditions at any operation point. The use of "P" and "S" equivalents helps in this assessment. First the original variables i_1 and i_2 are considered with the inverse of (12) and (14).

$$\begin{aligned} i_1(t) &= i_S(t) + \frac{L_2}{L_1 + L_2} i_P(t) \\ i_2(t) &= -i_S(t) + \frac{L_1}{L_1 + L_2} i_P(t). \end{aligned} \tag{39}$$

The initial conditions of $i_P(t)$ may be evaluated in function of P_P as well as $i_S(t)$ is expressed in function of P_S and the ZVS conditions may be verified over the complete operation plane defined by P_1 and P_2. Applying bi-port LLC design rules [25] to the "P" circuit, ZVS can be ensured on the axis given by k_{21}/k_{12}. By inspection of Fig. 7, Fig. 6 and (39), it can be noticed that the presence of increasing i_S tends to push one of the subsystems out of the ZVS condition. This is illustrated in Fig. 8 which reveals the ZVS region over the plane (P_1, P_2). It can be drawn that by sizing the resonant tank (L_1 and L_2) adequately, the ZVS region can be influenced in order to match a specific operation region.

VI. Experimental Results

To demonstrate the validity of the developed model and power sharing in practice, a 4 kW rated converter comprising a three-winding transformer with a 1:1:1 turn ratio is realized. Fig. 9 shows a photograph of the lab-scale prototype. The

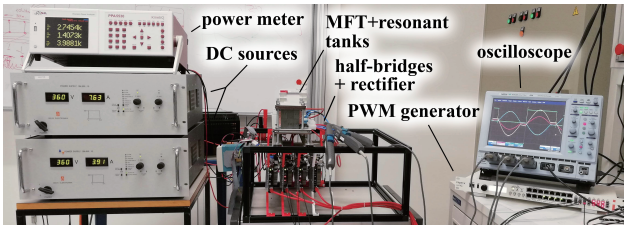

Fig. 9. 4 kW/360 V rated experimental test-setup.

TABLE I
RESONANT TANK PARAMETERS

L_m	L_1	C_1	L_2	C_2	f_{res}
400 μH	17.5 μH	5 μF	35 μH	2.5 μF	17 kHz

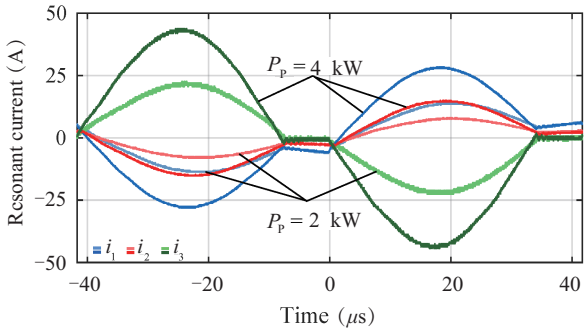

Fig. 10. Resonant current waveforms (oscilloscope import) from measurement at 2 kW (light colors) and 4 kW (dark colors).

MFT is designed to be operated at f_{sw} = 12 kHz. The load port has a leakage inductance around 0.8 μH, and the two active ports are equipped with resonant tanks with the parameters presented in Table I. Assuming a 5% tolerance for the resonant tank components in Table I, the maximum deviations for P_1 and P_2 are 6.8% and 3.4%, respectively. The voltages V_1 and V_2 are generated with two DC power supplies, allowing to vary precisely the voltage of the two DC buses and test various operating points around 360 V. The three half-bridge converters are made of PEB-4046 modules from Imperix [26] which integrates the two IGBTs (IXYS MMIX1X200N60B3H1) and the DC-bus capacitors (825 μF). Two of them (on ports 1 and 2) are actively switched at f_{sw} while the third one is passive and is used as a rectifier.

The experiments is carried out with resistive loads rated to 1, 2, 3 and 4 kW. Fig. 10 shows figure of merit for different load conditions, which are in good agreement with the model, i.e., the amplitude of two input currents are proportional to the load and have the ratio $\frac{1}{3}$,$\frac{2}{3}$ as defined by the components of the resonant tanks in Table I. Then, for the 4 kW load, different values of V_S, between −15 V and 25 V, are considered in order to show the effects of circulating currents. Fig. 11 shows the measured current waveforms for two different operating points. The powers P_1, P_2 and P_3 are directly measured at the DC terminals (using a N4L PPA5500 power analyzer). Power analyzer measurements well match calculations computed from

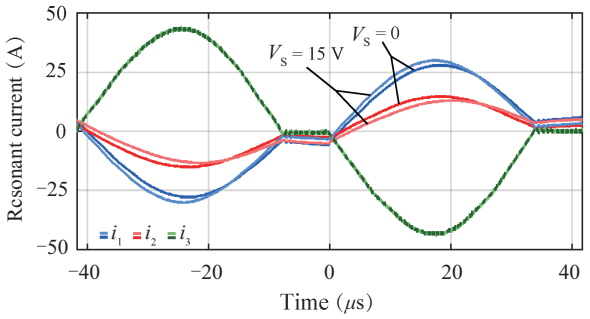

Fig. 11. Resonant current waveforms (oscilloscope import) from measurement at 4 kW. The currents i_1 and i_2 are affected by the introduction of differential voltage V_S, but the current to the load, namely i_3 is not affected. To be noted that from t = −40 μs to 0, the currents flow in S_{1L}, S_{2L} and D_{3L} while from t = 0 to 40 μs, the currents currents circulate in S_{1H} and S_{2H} and S_{3H}.

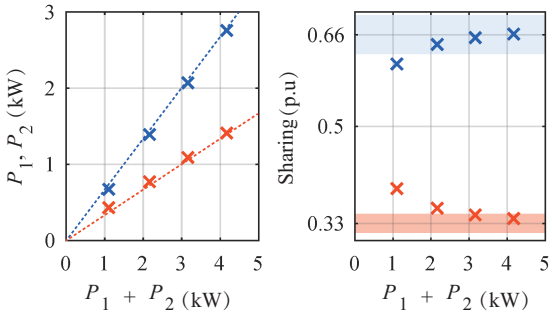

Fig. 12. On the left, powers (P_1 in blue and P_2 in red) and, on the right, their corresponding sharing part $P_k/(P_1+P_2)$ when V_S = 0. Apart from some deviations at light load conditions, the power sharing is constant and reflecting the ratio of the inductance defined in Table I, namely $L_2/(L_1+L_2)$ = 2/3 and $L_1/(L_1+L_2)$ = 1/3 (at low power operation, the impact of switching losses, which are load independent and not included in the model, is not negligible).

the time-domain waveforms (acquired by the oscilloscope). P_P and P_S are computed from these latter. Fig. 12 depicts the influence of the tank impedance ratio on the sharing of P_P between P_1 and P_2. The natural sharing characteristic is defined by the tank design and is maintained with changing load on the output (third) port. The losses effects on this result are clear: when the output power increases, the weight of losses terms in (32) is smaller and, therefore, (24)−(25) are more accurate. However, when P_P is small, all the terms of (32) have an impact. In order to deep into the accuracy of the model with losses consideration, Figs.13 and 14 are assessed. The effect of V_S on P_S is shown in Fig. 13, illustrating that for the constant output load, the power sharing is highly sensitive to variation of V_S. The impact of V_S on the efficiency is depicted in Fig. 14 for the different loads although the lab set-up hardware has not been optimized in that sense, and its purpose is to validate power sharing characteristics.

VII. CONCLUSION

This paper presents the model and the power sharing characteristics for a three-terminal SRC based DC-transformer for SST applications requiring an energy storage functionality. Among the possible modes of operation, the one considering

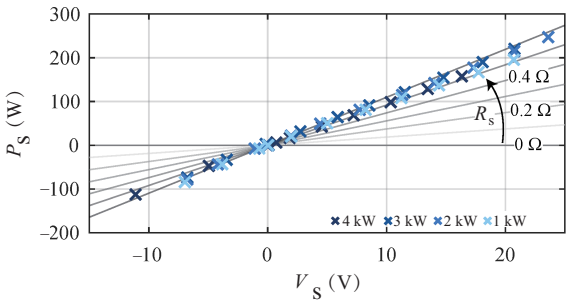

Fig. 13. Measured P_S and effect of R_S on the theoretical curve. For $R_S = 0$, it would be zero for any V_S. The experiments show that R_S, which represent the conduction losses and the switching losses associated to the circulating power flow, is around 0.55 Ω.

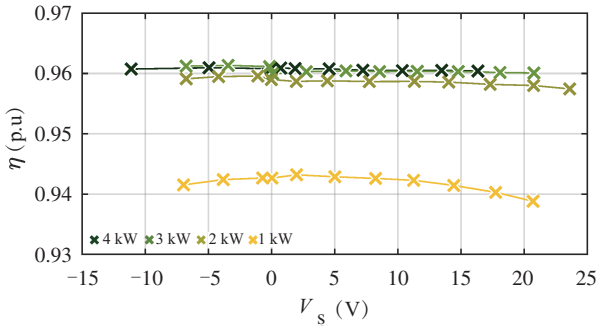

Fig. 14. Efficiency for various operating points. The switching losses depending on the turn off currents ($i_1(0)$ and $i_2(0)$) which are set by L_m and are load independent, the efficiency is reduced for light load conditions. Additional losses appear with the circulation of current i_S , which explains the drop of efficiency for increasing $|V_S|$.

two inputs and one output is the most complex and is therefore analyzed in this paper. In order to get a compact analytic solution, a model based the separation of the power flow into a main power (from the active ports to the load port) and a circulating power (between the active ports) is proposed ("P" and "S" equivalent circuits). The modelling reveals that the natural power sharing is mostly impacted by the resonant tank design parameters. The sharing is preserved in the absence of differential voltage between the active ports and can be, to some extent, influenced by further manipulation on the differential voltage which introduces a circulating power flow (influenced as well by the losses and parasitic resistances). However, if high circulating currents are forced, the ZVS conditions may be compromised. This gives basic design insights to size the resonant tank inductances in a way to benefit from soft switching in a specified operating region. The experimental results, obtained with a lab-scale prototype, match and effectively verify the proposed model.

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