Real-Time Diagnosis of Multiple Transistor Open-Circuit Faults in a T-Type Inverter Based on Finite-State Machine Model

Borong Wang, Zhan Li, Zhihong Bai, Philip T. Krein, and Hao Ma

***Abstract*—This paper proposes a fault diagnosis method to diagnose multiple transistor open-circuit faults in a T-type three-level inverter. In this method, a finite-state machine (FSM) tracks state transitions caused by abnormal fault-linked current paths, and rough set theory (RST) is employed to optimize and obtain a minimum set of variables necessary to distinguish state transitions under various fault scenarios. After applying RST, voltage state variables expressed by Boolean logic relationships are adopted in the FSM to identify faults. This can also effectively reflect state transitions between single and multiple fault cases. The approach is immune to load disturbances and dead times. Through logic relationships, a circuit is designed for fast online fault location to minimize the impact of sampling frequency on diagnosis. Factors that affect diagnosis time and accuracy are considered and analyzed to ensure the reliability of the proposed method. Experimental results obtained under various conditions verify the effectiveness of this approach.**

***Index Terms*—Fault diagnosis, finite-state machine, multiple open-circuit faults, rough set theory, T-type inverter.**

I. Introduction

COMPARED to other multilevel inverters, T-type three-level inverters ($T^2$3LI) have better performance in low-voltage and medium switching frequency (4–30 kHz) applications because of low output harmonic content, low conduction loss, and high efficiency [1], [2].

Improved reliability of multilevel inverters is beneficial for economy and safety, especially in reliability-critical applications [3], and fault tolerance is a preferred approach for enhancing their reliability [4]. Thus, fast, accurate real-time diagnosis is essential to ensure that a timely post-fault reconfiguration can be implemented to maintain sustained system operation [5]. Since semiconductor power devices are relatively vulnerable components [6], most prior work emphasizes semiconductor switching device failures [7], [8].

Open circuit (OC) and short circuit (SC) failures can occur in switching devices, such as insulated gate bipolar transistors (IGBTs). SC faults may occur as a result of high temperature, local thermal runway, or incorrect gate voltage. Typically, SC faults are difficult to handle because of linked overcurrents, which have a destructive impact on other components [9], [10]. SC faults should be isolated immediately, for instance by applying desaturation detection in gate drivers or fast fuses [11], [12]. Unlike SC faults, OC faults, which mostly arises from bond wire fracture, gate drive failure, or solder joint fracture, cannot be detected in the same way. Generally, OC faults will not cause immediate system breakdown, but may cause secondary damage and destroy the inverter following propagation of increasing current or voltage stress [13], [14]. Thus, effective OC fault diagnosis is required for reliability.

In the past work, many detection methods for transistor OC faults have been proposed. For conventional voltage source inverters, detection based on analysis of current signals was introduced in [15]–[17]. Current-based detection can produce false alarms with light load or nonlinear loads. To improve the robustness of fault detection, a normalized current method and multiple-variable method were proposed, but these are relatively slowly [18], [19]. Methods based on voltage signals were presented in [20]–[24]. In [20], [21], a detection circuit monitored bridge arm pole-to-pole voltages. The detection circuit may increase cost and complexity, but faults can be diagnosed quickly. Model based methods are proposed in [22]–[24]. Based on existing control signals, these methods identify faults by detecting errors between reference values and estimated values. To improve diagnosis and avoid misdiagnosis, factors such as dead time, switching noise, signal delay, and parameter errors should be considered.

Compared to a conventional two-level inverter, multilevel inverters have more diagnostic targets and potential fault modes. In [25], an OC fault detection method was developed for a $T^2$3LI, based on neutral point current magnitude. Diagnosis can be achieved within a few switching cycles, but variations in the neutral point current are related to the

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diverse loads. In [26], currents are evaluated in state space. An OC fault will distort the current pattern. In [27], methods that combine voltage and current signals are proposed to detect single-transistor OC faults by evaluating capacitor voltage deviations and three-phase current polarities. In both approaches, robustness was improved by means of normalization. However, the detected signals are insensitive to device faults, which extends the diagnosis time to several fundamental periods. Fault propagation may be difficult to restrain immediately. To improve diagnosis speed, [28] presents a method based on switching functions to detect transistor OC faults in different phases, but the delay between detection variables should be eliminated to increase diagnosis accuracy. A nonintrusive fault diagnosis technique was applied in a neutral point clamped (NPC) inverter in [29]. An external antenna and an electromagnetic interference filter collected near-field emission signatures and common-mode noise signatures. Only one extra sensor was needed, and the method is decoupled from the electrical circuit. However, this approach is only able to detect a few types of OC faults.

For multilevel inverters, if OC faults can be located accurately and rapidly, corresponding fault tolerance methods can be adopted to achieve seamless fault recovery, and reduce system repair time and cost [30], [31]. Therefore, changes in power devices should be tracked in real time to achieve better fault diagnosis speed and robustness. Generally, software-based methods can be embedded in the control strategies. The response time will be longer to evaluate samples, set time criteria for fault triggering, and to cover analogue-to-digital converter processing time. To distinguish various operating states accurately, a high sampling frequency may be needed, and the diagnosis algorithms should be completed in each sampling period since any possible runaway may cause diagnosis failure. Hardware-based methods can provide fast fault response by processing detected analog signals, and are independent from system control strategies [20], [21]. The detection time limits rely on added devices. Extra cost can be limited with a simple circuit, which is easily integrated in control boards or power modules. Multiple faults are relatively likely in T-type inverters because of the high power device count, whereas prior diagnostic schemes proposed emphasize single transistor faults.

This paper presents a method to detect multiple OC faults in a $T^2$3LI. Real-time detection can be achieved by identifying abnormal state transitions based on a finite-state machine (FSM) model. To reduce the number of detection variables, rough set theory (RST) is employed to extract diagnosis eigenvalues from voltages across half-bridge transistors. Diagnosis results can be represented as logic expressions independent of dead times, load changes, and imbalance. Additional factors that may induce misdiagnosis, such as switching noise and signal delays, are considered.

II. Analysis of Open-Circuit Faults in T-Type Inverters

The $T^2$3LI topology is shown in Fig. 1. Capacitors C_1 and C_2 split the dc-link input (V_{dc}) and provide a neutral point Z. Each phase has two IGBT half-bridge transistors (T_{x1}, T_{x4}, x = a, b, c)

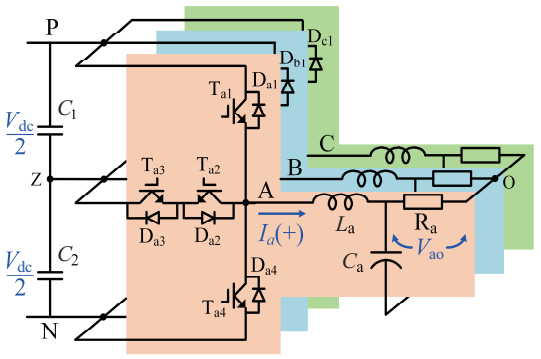

Fig. 1. Diagram of three-phase $T^2$3L inverter system.

TABLE I
Switching Signals and Operating Modes

Operating mode	S_{x1}, S_{x2}, S_{x3}, S_{x4}	Current path	Pole voltage
Mode I [P]	1, 0, 1, 0	Z–P–X	$0.5V_{dc}$
Mode II/IV [O]	0, 1, 1, 0	Z–X	0
Mode III [N]	0, 1, 0, 1	X–N–Z	$-0.5V_{dc}$

and a pair of common emitter IGBTs (T_{x2}, T_{x3}) connected to the point Z. D_{x1}–D_{x4} are reverse parallel diodes.

The switching signals S_{x1}–S_{x4} ($S_{xn} \in \{0,1\}$), function such that the output terminal X (X = A, B, C) can connect to the positive dc bus, the neutral point Z, or the negative dc bus. Assuming T_x –T_{x4} are ideal transistors and ignoring dead time, an output pole voltage V_{XZ} can be obtained on the basis of switching functions,

$$q_X = \begin{cases} 2 & (S_{x1}, S_{x2}, S_{x3}, S_{x4}) = (1, 0, 1, 0) \\ 1 & (S_{x1}, S_{x2}, S_{x3}, S_{x4}) = (0, 1, 1, 0) \\ 0 & (S_{x1}, S_{x2}, S_{x3}, S_{x4}) = (0, 1, 0, 1) \end{cases}, \quad (1)$$

$$V_{XZ} = 0.5V_{dc}(q_X - 1). \quad (2)$$

Given switching signals corresponding to the devices, relationships between operating modes, current paths and pole voltages in a fundamental period are listed in Table I, which defines operating states associated with positive [P], negative [N], and neutral [O] voltage levels.

In Table I, two transistors per phase conduct simultaneously in each operating state. The analysis here will emphasize the possibility of single or multiple OC faults during states [P] or [N]. Operating behavior will be explored for phase A, and the discussion can be extended to the other phases.

A. Effect of Open-Circuit Faults on Each Operating Mode

Several circuit operating modes are illustrated in Fig. 2. These configurations are used here to consider current paths under normal and fault conditions.

1) OC fault in T_{a1} during mode I: When the inverter operates normally in mode I, $q_A = 2$ and the operating state is [P]. Current I_a will flow through T_{a1} or D_{a1}, and the current path is

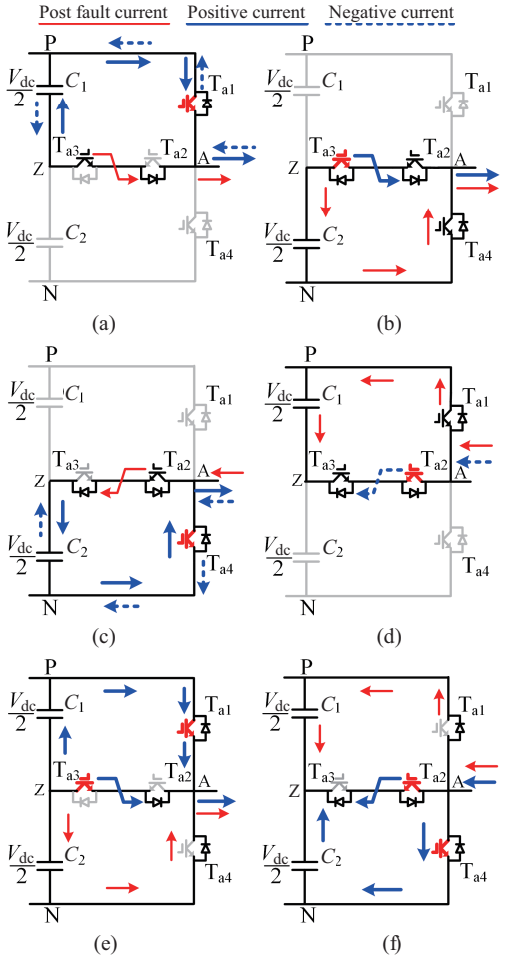

Fig. 2. Current path: (a) T_{a1} fault during mode I. (b) T_{a3} fault during mode II. (c) T_{a4} fault during mode III. (d) T_{a2} fault during mode IV. (e) T_{a1} and T_{a3} faults during mode I. (f) T_{a2} and T_{a4} faults during mode III.

Z–P–A. If an OC fault occurs in T_{a1} when $I_a > 0$, operating state [P] is no longer possible because the output terminal cannot be connected to the positive dc bus. The current will flow through T_{a3} and D_{a2} instead, as shown in Fig. 2(a). In this scenario, the post-fault current path is Z–A and V_{AZ} becomes 0 rather than 0.5 V_{dc}. If $I_a < 0$, the fault current path is still Z–P–A due to current flowing through D_{a1}, and there is no immediate impact on circuit operation.

2) OC fault in T_{a3} during mode II: During mode II, output terminal A is connected to Z since $q_A = 1$ and the neutral point current is positive. When T_{a3} fails open, the current path is Z–N–A instead of Z–A, as shown in Fig. 2(b), since D_{a3} becomes reverse biased. The operating state changes to [N], and V_{AZ} becomes $-0.5V_{dc}$.

3) OC fault in T_{a4} during mode III: When the inverter operates in mode III, q_A is equal to 0 and the operating state is [N]. The current path is A–N–Z. Following an OC fault in T_{a4}, the negative current path A–Z will be formed through T_{a2} and D_{a3} instead of T_{a4}, as shown in Fig. 2(c). The operating state becomes [O] instead of [N]. If current is positive during mode III, the post-fault current path can be formed through D_{a4} and there is no immediate operating effect.

4) OC fault in T_{a2} during mode IV: The overall analysis in mode IV is similar to that in mode II except for the current direction. The normal operating state is [O], and the current path is A–Z. If T_{a2} fails open, negative current flows instead through diode D_{a1} as shown in Fig. 2(d). The post-fault operating state becomes [P] due to current path A–P–Z and V_{AZ} increases to $0.5V_{dc}$.

5) OC faults in T_{a1} and T_{a3} during mode I: Given OC faults both in T_{a1} and T_{a3} with $I_a > 0$ during mode I, the faulty leg cannot output positive voltage and current will flow through D_{a4}. In this instance, the post-fault current path is Z–N–A, as shown in Fig 2(e). Voltage V_{AZ} becomes $-0.5V_{dc}$.

Since $V_{AN} > V_{ZN}$ during mode I, an OC fault in T_{a3} will not affect operation immediately. An abnormal current path Z–N–A will not form until mode II appears. Therefore, only an OC fault in T_{a1} or OC faults in T_{a1} and T_{a3} can be detected.

6) OC faults in T_{a2} and T_{a4} during mode III: Given simultaneous T_{a2} and T_{a4} OC faults, Fig. 2(f) shows that negative current cannot flow through A–Z and A–N–Z during mode III. The fault current path becomes A–P–Z and V_{AZ} will become $0.5V_{dc}$.

It should be noted that a fault in T_{a2} during mode III will not affect circuit operation until the inverter reaches mode IV, since $V_{AN} > V_{AZ}$ and the negative current can flow through T_{a4}. During mode IV, an abnormal current path A–P–Z will form. An OC fault in T_{a2} cannot be detected during mode III.

7) OC faults in T_{a2} and T_{a3} during modes II and IV: When simultaneous OC faults occur in T_{a2} and T_{a3} during mode II, positive current will flow through Z–N–A rather than Z–A. However, if only T_{a2} has an OC fault, positive current can flow through D_{a2}, the current path is still Z–A, and there is no immediate operating effect.

During mode IV, the current path becomes A–P–Z instead of A–Z and V_{AZ} changes to $0.5V_{dc}$, which is similar to a T_{a2} fault in Fig. 2(d). If an OC fault occurs only in T_{a3}, the current path and output pole voltage will remain the same since negative current can flow through D_{a3}. Thus, a T_{a3} fault has no immediate impact on system operation in mode IV.

B. Modeling Based on FSM

A finite-state transition diagram showing the effects of faults is given in Fig. 3(a). The switching signals serve as inputs, and guards in the model are defined by a fault signal S_{OC} and a current direction signal S_{CD}. $S_{OC} = 1$ indicates that transistors have an OC fault. $S_{CD} = 1$ implies positive current. There are four states (states I–IV), each corresponding to the current path in one of the operating modes (modes I–IV) as listed in Table I. The transitions between states rely on rules shown in the diagram. For example, when $q_A = 2$, the current path is Z–P–A and the circuit operates normally in state I. If $S_{OC\_a1} = 1$ and $S_{CD} = 1$, indicating that T_{a1} has failed and $I_a > 0$, an abnormal transition will occur into state II since the current path changes to Z–A. When $S_{OC\_a3} = 1$, the transition will start and end in state I. It should be noted that, due to the series structure of the neutral point transistors, a state transition caused by simultaneous T_{a2} and T_{a3} OC faults will occur in modes II

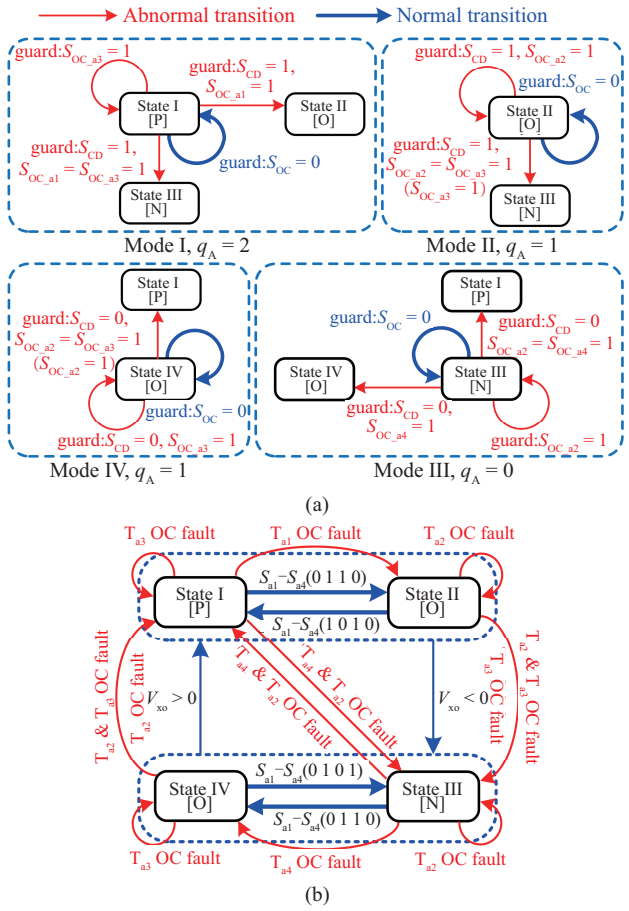

Fig. 3. Finite-state machine model. (a) State transition diagram in each mode. (b) Combined state transition.

and IV. It would be equivalent to an abnormal state transition caused by single failure in the corresponding mode. Thus, it is necessary to identify T_{a2} and T_{a3} faults by combining state transitions in modes II and IV. Due to FSM symmetry, state transitions in states I and II are

$$s(1)\big|_{q_A=2} = \begin{cases} s(1) & S_{OC} = 0 \\ s(1) & S_{OC\_a3} = 1 \\ s(2) & S_{CD} = 1,\ S_{OC\_a1} = 1 \\ s(3) & S_{CD} = 1,\ S_{OC\_a1} = S_{OC\_a3} = 1 \end{cases}, \quad (3)$$

$$s(2)\big|_{q_A=1} = \begin{cases} s(2) & S_{OC} = 0 \\ s(2) & S_{CD} = 1,\ S_{OC\_a2} = 1 \\ s(3) & S_{CD} = 1,\ S_{OC\_a3} = 1 \\ s(3) & S_{CD} = 1,\ S_{OC\_a2} = S_{OC\_a3} = 1 \end{cases}. \quad (4)$$

Here, $s(1)$, $s(2)$, and $s(3)$ refer to states I, II, and III.

The combined transition model is shown in Fig. 3(b). During normal operation, switching signals govern the transitions. When a fault occurs, state transitions caused by the abnormal current path depend on current direction, fault location, and the initial state. Faulty transistors can be identified by detecting abnormal state transitions.

TABLE II
STATE TRANSITIONS UNDER VARIOUS OPERATING CONDITIONS

Original state	Guard	Current path	V_{sw_a1}	Next state
State I [P]	$S_{OC} = 0$	Z–P–A	0	State I
	$S_{OC\_a1} = 1$, $S_{CD} = 1$	Z–A	$0.5V_{dc}$	State II
	$S_{OC\_a3} = 1$	Z–P–A	0	State I
	$S_{OC\_a1} = S_{OC\_a3} = 1$ $S_{CD} = 1$	Z–N–A	V_{dc}	State III
State II [O]	$S_{OC} = 0$	Z–A	$0.5V_{dc}$	State II
	$S_{OC\_a3} = 1$, $S_{CD} = 1$	Z–N–A	V_{dc}	State III
	$S_{OC\_a2} = 1$, $S_{CD} = 1$	Z–A	$0.5V_{dc}$	State II
	$S_{OC\_a2} = S_{OC\_a3} = 1$ $S_{CD} = 1$	Z–N–A	V_{dc}	State III
State III [N]	$S_{OC} = 0$	A–N–Z	V_{dc}	State III
	$S_{OC\_a4} = 1$, $S_{CD} = 0$	A–Z	$0.5V_{dc}$	State IV
	$S_{OC\_a2} = 1$	A–N–Z	V_{dc}	State III
	$S_{OC\_a2} = S_{OC\_a4} = 0$ $S_{CD} = 1$	A–P–Z	0	State I
State IV [O]	$S_{OC} = 0$	A–Z	$0.5V_{dc}$	State IV
	$S_{OC\_a2} = 1$, $S_{CD} = 0$	A–P–Z	0	State I
	$S_{OC\_a3} = 1$, $S_{CD} = 0$	A–Z	$0.5V_{dc}$	State IV
	$S_{OC\_a2} = S_{OC\_a3} = 1$ $S_{CD} = 0$	A–P–Z	0	State I

TABLE III
INFORMANTION SYSTEM OF FSM MODEL FOR VARIOUS SCENARIOS

UA	CA						DA
	S_{a1}–S_{a4}	I_{AZ}	I_{AN}	I_{AP}	S_{p1}	S_{p2}	
(1)	1 0 1 0	0	0	i_{AP}	0	0	Normal
(2)	0 1 1 0	i_{AZ}	0	0	1	0	Normal
(3)	0 1 0 1	0	i_{AN}	0	1	1	Normal
(4)	1 0 1 0	i_{AZ}	0	0	1	0	OC (T_{a1})
(5)	1 0 1 0	0	i_{AN}	0	1	1	OC (T_{a1}, T_{a3})
(6)	0 1 1 0	0	i_{AN}	0	1	1	OC (T_{a3})
(7)	0 1 0 1	i_{AZ}	0	0	1	0	OC (T_{a4})
(8)	0 1 0 1	0	0	i_{AP}	0	0	OC (T_{a2}, T_{a4})
(9)	0 1 1 0	0	0	i_{AP}	0	0	OC (T_{a2})

III. PRINCIPLE OF FAULT DIAGNOSIS

A. Extraction of Diagnosis Eigenvalue Based on RST

State transitions in the FSM can be represented by current paths listed in Table II. The voltage across T_{a1} (V_{sw_a1}) is also used to track the state change. Here, a method based on RST [32] is employed to reduce the number of variables in Table II and obtain the minimum set of indispensable detection signals. Assuming Table II is an information system based on the FSM model, all state transitions are defined by objective cases (UA), and state variables of the circuit, including V_{sw_a1}, switching signals, and current paths, are defined as conditional attributes (CA). For all state transitions, if the next state is different from the original state, the circuit is considered to be operating under fault conditions. Operating conditions are represented by decision attributes (DA). If all subsets of CA corresponding to different objective cases are identical, the variables are redundant and can be removed from the information system. The information system of the FSM consists of UA, CA and DA, and is presented in Table III.

TABLE IV
DISCERNIBLITY MATRIX BASED ON RST

	EC(1)	EC(2)	EC(3)	EC(4)	EC(5)	EC(6)	EC(7)	EC(8)	EC(9)
EC (1)	φ								
EC (2)	S_{a1}, S_{a2}, i_{AZ}, i_{AP}, S_{p1}	φ							
EC (3)	S_{a1}, S_{a2}, i_{AN}, i_{AP}, S_{p1}, S_{p2}	S_{a3}, S_{a4}, i_{AZ}, i_{AP}, S_{p2}	φ						
EC (4)	i_{AZ}, i_{AP}, S_{p1}	S_{a1}, S_{a2}	S_{a1}, S_{a2}, S_{a3}, S_{a4}, i_{AZ}, i_{AN}, S_{p2}	φ					
EC (5)	i_{AP}, i_{AN}, S_{p1}, S_{p2}	S_{a1}, S_{a2}, i_{AZ}, i_{AN}, S_{p2}	S_{a1}, S_{a2}, S_{a3}, S_{a4}	i_{AZ}, i_{AN}, S_{p2}	φ				
EC (6)	S_{a1}, S_{a2}, i_{AP}, i_{AN}, S_{p1}, S_{p2}	i_{AZ}, i_{AN}, S_{p2}	S_{a3}, S_{a4}	S_{a1}, S_{a2}, i_{AZ}, i_{AN}, S_{p2}	S_{a1}, S_{a2}	φ			
EC (7)	S_{a1}, S_{a2}, S_{a3}, S_{a4}, i_{AP}, i_{AZ}, S_{p1}	S_{a3}, S_{a4}, i_{AP}, S_{p2}	i_{AZ}, i_{AN}, S_{p2}	S_{a1}, S_{a2}, S_{a3}, S_{a4}	S_{a1}, S_{a2}, S_{a3}, S_{a4}, i_{AZ}, i_{AN}, S_{p2}	S_{a3}, S_{a4}, i_{AZ}, i_{AN}, S_{p2}	φ		
EC (8)	S_{a1}, S_{a2}, S_{a3}, S_{a4}	S_{a3}, S_{a4}, i_{AP}, i_{AZ}, S_{p1}	i_{AP}, i_{AN}, S_{p1}, S_{p2}	i_{AZ}, i_{AN}, S_{p2}	S_{a1}, S_{a2}, S_{a3}, S_{a4}, i_{AP}, i_{AN}, S_{p1}, S_{p2}	S_{a3}, S_{a4}, i_{AP}, i_{AN}, S_{p1}, S_{p2}	i_{AZ}, i_{AP}, S_{p1}	φ	
EC (9)	S_{a1}, S_{a2}	i_{AZ}, i_{AP}, S_{p1}	S_{a3}, S_{a4}, i_{AP}, i_{AN}, S_{p1}, S_{p2}	i_{AZ}, i_{AN}, S_{p2}	S_{a1}, S_{a2}, i_{AP}, i_{AN}, S_{p1}, S_{p2}	i_{AP}, i_{AN}, S_{p1}, S_{p2}	S_{a3}, S_{a4}, i_{AZ}, i_{AP}, S_{p1}	S_{a3}, S_{a4}	φ

S_{p1} and S_{p2} are voltage state variables defined as

$$S_{p1} = \begin{cases} 1 & V_{sw\_a1} \geqslant V_{ref1} \\ 0 & V_{sw\_a1} < V_{ref1} \end{cases}, \tag{5}$$

$$S_{p2} = \begin{cases} 1 & V_{sw\_a1} \geqslant V_{ref2} \\ 0 & V_{sw\_a1} < V_{ref2} \end{cases}. \tag{6}$$

where V_{ref1} is in the interval [0, $0.5V_{dc}$] and V_{ref2} is chosen between [$0.5V_{dc}$, V_{dc}].

From Table III, there is an equivalence relation between different objective cases. For example, the value of I_{AP} is 0 in cases UA(2) through UA(7). Thus, I_{AP} cannot reflect enough information to identify all objective cases in Table III. UA(i) and UA(j) with equivalence relationships are defined as equivalence cases EC(i) and EC(j). To further reduce redundant data, discernible attributes are obtained in

$$md_{i,j} = \left[x_i \in \mathrm{EC}(i), x_j \in \mathrm{EC}(j) \mid \forall c \in B, c(x_i) \neq c(x_j) \right], \tag{7}$$

where $md_{i,j}$ is an element in the discernibility matrix, as listed in Table IV, B is the subset of CA, and $c(x_i)$ refers to the state variable with respect to B in the case EC(i).

From (7), a discernibility function $F(B)$ can be expressed in the form of a Boolean function.

$$F(B) = \bigwedge_{1 \leqslant i,j \leqslant n} \left(\bigvee md_{i,j} \mid md_{i,j} \neq 0 \right) \tag{8}$$

where n refers to the number of equivalent cases.

Combing Table IV and (8), the simplified discernibility function $F^*(B)$ is expressed in (9), where "+" refers to the operator "or", and "·" refers to the operator "and". This function is the sum of 32 minterms, and each minterm is the minimum set of variables that can distinguish one equivalent case from another. The state variables in each minterm can be used to identify normal and fault cases in Table III. Switching signals are essential variables in all minterms. Extra current signals through two branches are involved in each minterm of part I, and detection signals including current and voltage variables are added in each minterm of part II. In part III, only S_{p1} and S_{p2} are needed. In proposed solution, detection variables are selected from any minterm in part III.

Based on this analysis, state transitions in the FSM can be tracked by signals (S_{a1}, S_{a4}) and state variables (S_{p1} and S_{p2}), as shown in Table V. From this table, logic relationships to identify faults are given by Boolean expressions

$$S_{F\_a1} = S_{a1} \ \& \ S_{p1} = \begin{cases} 1 & q_A = 2, S_{CD} = 1, S_{OC\_a1} = 1 \\ 0 & S_{OC\_a1} = 0 \end{cases} \tag{10}$$

$$S_{F\_a2} = \overline{S_{a1} \parallel S_{p1}} = \begin{cases} 1 & q_A = 1, S_{CD} = 0, S_{OC\_a2} = 1 \\ 0 & S_{OC\_a2} = 0 \end{cases} \tag{11}$$

$$\begin{aligned} F^*(B) &= (S_{a1} + S_{a2}) \cdot (S_{a3} + S_{a4}) \cdot (i_{AZ} + i_{AN} + S_{p2}) \cdot (i_{AZ} + i_{AN} + S_{p2}) \cdot (i_{AP} + i_{AN} + S_{p1} + S_{p2}) \\ &= \underbrace{S_{a2} \cdot S_{a3} \cdot i_{AZ} \cdot i_{AP} + S_{a2} \cdot S_{a3} \cdot i_{AZ} \cdot i_{AN} + S_{a2} \cdot S_{a3} \cdot i_{AP} \cdot i_{AN} + S_{a1} \cdot S_{a3} \cdot i_{AZ} \cdot i_{AN} + S_{a1} \cdot S_{a3} \cdot i_{AP} \cdot i_{AZ} + S_{a1} \cdot S_{a3} \cdot i_{AP} \cdot i_{AN} + S_{a1} \cdot S_{a4} \cdot i_{AP} \cdot i_{AZ}}_{\text{PART I}} \\ &+ \underbrace{S_{a1} \cdot S_{a4} \cdot i_{AN} \cdot i_{AZ} + S_{a1} \cdot S_{a4} \cdot i_{AN} \cdot i_{AP} + S_{a2} \cdot S_{a4} \cdot i_{AN} \cdot i_{AP} + S_{a2} \cdot S_{a4} \cdot i_{AZ} \cdot i_{AP} + S_{a2} \cdot S_{a4} \cdot i_{AZ} \cdot i_{AN}}_{\text{PART I}} + \underbrace{S_{a2} \cdot S_{a3} \cdot i_{AZ} \cdot S_{P1} + S_{a2} \cdot S_{a3} \cdot i_{AN} \cdot S_{P1}}_{\text{PART II}} \\ &+ \underbrace{S_{a2} \cdot S_{a3} \cdot i_{AZ} \cdot S_{P2} + S_{a2} \cdot S_{a3} \cdot i_{AP} \cdot S_{P2} + S_{a1} \cdot S_{a4} \cdot i_{AZ} \cdot S_{P1} + S_{a1} \cdot S_{a4} \cdot i_{AN} \cdot S_{P1} + S_{a1} \cdot S_{a4} \cdot i_{AZ} \cdot S_{P2}}_{\text{PART II}} + \underbrace{S_{a1} \cdot S_{a4} \cdot i_{AP} \cdot S_{P2} + S_{a1} \cdot S_{a3} \cdot i_{AZ} \cdot S_{P1}}_{\text{PART II}} \\ &+ \underbrace{S_{a1} \cdot S_{a3} \cdot i_{AN} \cdot S_{P1} + S_{a1} \cdot S_{a3} \cdot i_{AZ} \cdot S_{P2} + S_{a1} \cdot S_{a3} \cdot i_{AP} \cdot S_{P2} + S_{a2} \cdot S_{a4} \cdot i_{AZ} \cdot S_{P1} + S_{a2} \cdot S_{a4} \cdot i_{AN} \cdot S_{P1}}_{\text{PART II}} + \underbrace{S_{a2} \cdot S_{a4} \cdot i_{AZ} \cdot S_{P2} + S_{a2} \cdot S_{a4} \cdot i_{AP} \cdot S_{P2}}_{\text{PART II}} \\ &+ \underbrace{S_{a1} \cdot S_{a3} \cdot S_{p1} \cdot S_{P2} + S_{a1} \cdot S_{a4} \cdot S_{p1} \cdot S_{P2} + S_{a2} \cdot S_{a3} \cdot S_{p1} \cdot S_{P2} + S_{a2} \cdot S_{a4} \cdot S_{p1} \cdot S_{P2}}_{\text{PART III}} \end{aligned} \tag{9}$$

TABLE V
STATE TRANSITION AND DETECTION SIGNALS

Original state	Next state	DA	S_{a1}	S_{a4}	S_{p1}	S_{p2}
State I	State I	Normal	1	0	0	0
State II	State II	Normal	0	0	1	0
State III	State III	Normal	0	1	1	1
State IV	State IV	Normal	0	0	1	0
State I	State II	OC (T_{a1})	1	0	1	0
State IV	State I	OC (T_{a2})	0	0	0	0
State II	State III	OC (T_{a3})	0	0	1	1
State III	State IV	OC (T_{a4})	0	1	1	0
State I	State III	OC (T_{a1}, T_{a3})	1	0	1	1
State III	State I	OC (T_{a2}, T_{a4})	0	1	0	0

TABLE VI
VALUES OF FAULT DIAGNOSIS RESULTS

Operating condition		S_{a1}–S_{a4}	S_{p1}, S_{p2}	S_{F_a1}–S_{F_a4}
Normal condition	Mode I	1 0 1 0	0 0	0 0 0 0
	Mode II	0 1 1 0	1 0	
	Mode III	0 1 0 1	1 1	
	Mode IV	0 1 1 0	1 0	
Fault condition	T_{a1}	1 0 1 0	1 0	1 0 0 0
	T_{a2}	0 1 1 0	0 0	0 1 0 0
	T_{a3}	0 1 1 0	1 1	0 0 1 0
	T_{a4}	0 1 0 1	1 0	0 0 0 1
	T_{a1}&T_{a3}	1 0 1 0	1 1	1 0 1 0
	T_{a2}&T_{a4}	0 1 0 1	0 0	0 1 0 1
	T_{a2}&T_{a3}	0 1 1 0	1 0	(0 1 0 0) (0 0 1 0)

$$S_{F\_a3} = \overline{S_{a4}} \ \& \ S_{p2} = \begin{cases} 1 & q_A = 1, S_{CD} = 1, S_{OC\_a3} = 1 \\ 0 & S_{OC\_a3} = 0 \end{cases} \tag{12}$$

$$S_{F\_a4} = \overline{\overline{S_{a4}} \parallel S_{p2}} = \begin{cases} 1 & q_A = 0, S_{CD} = 0, S_{OC\_a1} = 1 \\ 0 & S_{OC\_a1} = 0 \end{cases}, \tag{13}$$

where S_{F_a1}–S_{F_a4} are indicator signals for respective T_{a1}–T_{a4} OC faults. During normal operation, these indicator signals are 0. When an OC fault on T_{a1} occurs during mode I, S_{F_a1} in (10) becomes 1. Similarly, OC faults in T_{a2}, T_{a3}, and T_{a4} can be determined by (11)–(13), and multiple faults can be represented by combinations of indicator signals. Diagnosis results in various fault scenarios are illustrated in Table VI.

B. Design Logic Circuit for OC Fault Diagnosis

The analysis has shown how to choose fault detection signals based on the FSM and RST, and form fault indicator signals. Basic logic circuits to implemented (10)–(13) are shown in Fig. 4. However, IGBT switching delays [21] need to be considered, since they will induce misdiagnosis during normal operation.

Fig. 5 shows the total delay between S_{a1} and S_{p1}, which includes delay time of the IGBTs and sampling circuits (T_{delay_sig}), comparator delay (T_{delay_cmp}), and IGBT rise and fall times

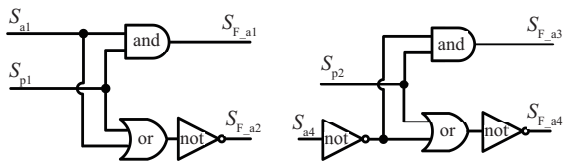

Fig. 4. Logic gate circuit.

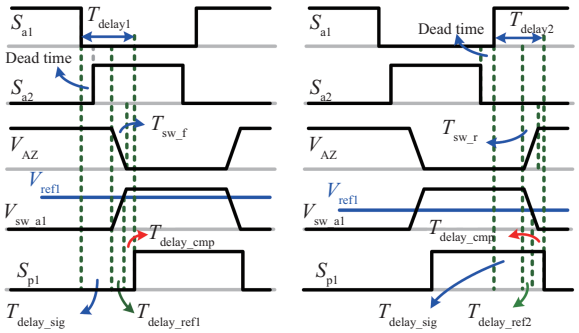

Fig. 5. The total delay time between drive signals and fault characteristic signals.

(T_{sw_r} and T_{sw_f}). T_{delay1} is the delay between the falling edge of S_{a1} and the rising edge of S_{p1}. T_{delay2} is the delay between the rising edge of S_{a1} and the falling edge of S_{p1}. Dead time (T_{dead}) is not considered since it does not alter the logic results. The total delay can be expressed as

$$\begin{aligned} T_{delay1} &= T_{delay\_sig} + T_{delay\_ref1} + T_{delay\_cmp} \\ &= T_{delay\_sig} + \frac{V_{ref1}}{V_{dc}} T_{sw\_f} + T_{delay\_cmp}, \end{aligned} \tag{14}$$

$$\begin{aligned} T_{delay2} &= T_{delay\_sig} + T_{delay\_ref2} + T_{delay\_cmp} \\ &= T_{delay\_sig} + \left(1 - \frac{V_{ref1}}{V_{dc}} T_{sw\_r}\right) + T_{delay\_cmp}. \end{aligned} \tag{15}$$

It can be seen from (14) and (15) that increasing V_{ref1} can prolong T_{delay1} and shorten T_{delay2}. The value of V_{ref1} will change the pulse width of misdiagnosis signals in S_{F_a1} and S_{F_a2}, as shown in Fig. 6. To avoid misdiagnosis caused by the delay in the rising edge and falling edge of V_{AZ} (T_{delay_ref1} and T_{delay_ref2}), there is a tradeoff to set the voltage threshold. Similar analysis can be extended to the value of V_{ref2}.

Signal and IGBT delays shown in Fig. 6 will cause various gaps during which the detection signals S_{F_a1}–S_{F_a4} will indicate false faults. To mitigate these effects, the dead time between transistors operating in complement can be made long enough to cover total delay and eliminate false diagnosis signals in S_{F_a2} and S_{F_a3}, as shown in Fig. 7. Boolean expressions (11) and (12) can be modified to give

$$S_{F\_a2} = \overline{\overline{S_{a2}} \parallel S_{p1}} = \begin{cases} 1 & q_A = 1, S_{CD} = 0, S_{OC\_a2} = 1 \\ 0 & S_{OC\_a2} = 0 \end{cases} \tag{16}$$

$$S_{F\_a3} = S_{a3} \ \& \ S_{p2} = \begin{cases} 1 & q_A = 1, S_{CD} = 0, S_{OC\_a3} = 1 \\ 0 & S_{OC\_a3} = 0 \end{cases} \tag{17}$$

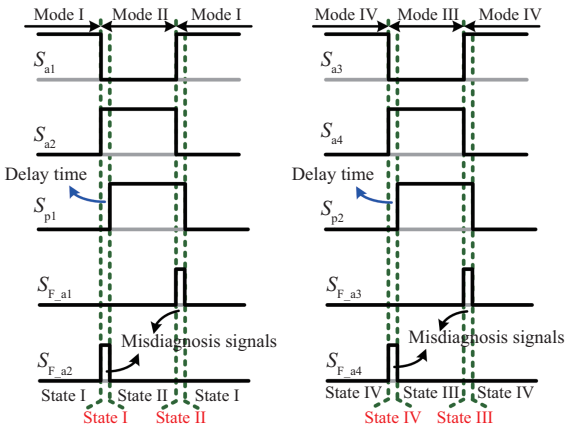

Fig. 6. Misdiagnosis due to signal delay.

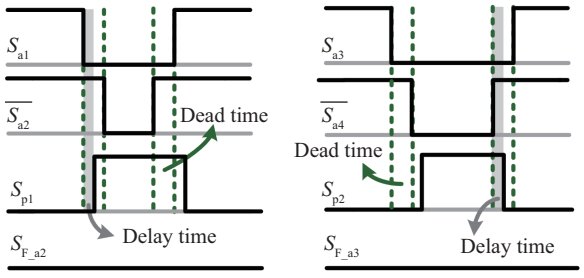

Fig. 7. Using dead time to eliminate misdiagnosis due to signal delay.

From Figs. 6 and 7, effects of signal delay on S_{F_a1} and S_{F_a4} cannot be addressed by prolonging dead time. In some applications, control timing is constrained such that misdiagnosis in S_{F_a2} and S_{F_a3} may still be possible. To address this, an RC filter can be added to delay the rising edge of switching signals and minimize switching noise effects.

In Fig. 8, V_{th_lg} is the high logic threshold, t_3–t_1 is the rising edge delay of S_{a2} and t_6–t_5 is rising edge delay of S_{a1}. Here, S'_{a1} and S'_{a2} are the delayed rising edge signals linked to S_{a1} and S_{a2}. To eliminate delay time between input signals of the logic circuit, rising edge delay must follow:

$$t_3 - t_1 > T_{delay1} - T_{dead} \tag{18}$$

$$t_6 - t_5 > T_{delay2}\,. \tag{19}$$

Parameters for the delay circuits used for S_{a1} and S_{a2} can be obtained as

$$\frac{1}{R_1 C_1} = \frac{1}{t_6 - t_5} \ln \frac{V_{high}}{V_{high} - V_{th\_lg}} \tag{20}$$

$$\frac{1}{R_2 C_2} = \frac{1}{t_3 - t_1} \ln \frac{V_{high}}{V_{high} - V_{th\_lg}}, \tag{21}$$

where V_{high} refers to the voltage value when S_{a1} and S_{a2} are high.

To guarantee the accuracy of diagnosis results, narrow voltage pulses in S_{p1} should be avoided by a suitable value of the reference voltage (V_{ref1}). As shown in Fig. 8, since voltage overshoot may be generated in V_{sw_a1} during IGBT turn-on and turn-off, the low-level logic signal S_{p1} might mistrigger

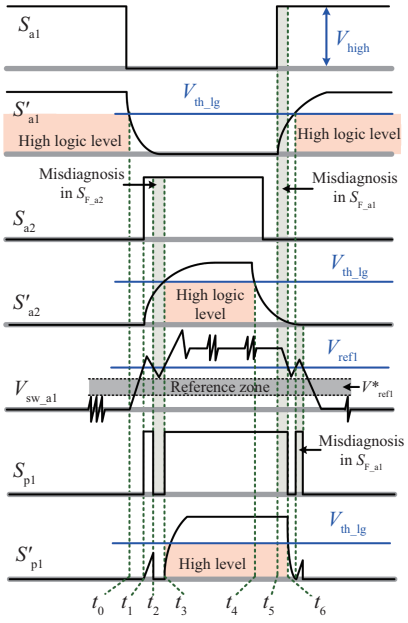

Fig. 8. Delay adjustment to eliminate misdiagnosis.

during t_2 to t_3 if the reference voltage is too high. On the other hand, high frequency noise will occur during the on and off states of T_{a1} as signals propagate from other legs. To minimize effects of voltage pulses and oscillation, a divider is able to set the reference voltage V^*_{ref1} online within a preferred reference zone (represented in grey on Fig. 8) which can be determined according to the practice. Combined with previous analysis, a proper V_{ref1} should avoid selecting boundary values within the given range (0, $0.5V_{dc}$). In addition, the inevitable narrow S_{p1} can be suppressed by adjusting parameters of the low pass filter, such as with a variable resistor. S'_{p1} represents the sampled voltage signals after eliminating noise pulses. Delays for indicator signals S_{F_a1} and S_{F_a2} can be obtained as

$$T_s D_{a2} > T_{delay\_Fa2} > t_3 - t_1 + T_{dead} \tag{22}$$

$$T_s (1 - D_{a1}) > T_{delay\_Fa1} > t_6 - t_5 \tag{23}$$

where T_{delay_Fa1} and T_{delay_Fa2} refer to the delay time of S_{F_a1} and S_{F_a2}, T_s refers to the switching period, and D_{a1} and D_{a2} refer to the duty ratios of S_{a1} and S_{a2}.

A circuit to detect OC faults in phase A is shown in Fig. 9, which can also be applied to other phases. The circuit consists of a sampler, comparator, delay adjustment, and logic. If the dead time is long enough to cover misdiagnosis in S_{F_a2} and S_{F_a3}, RC filters are not needed. The sampler extracts voltage V_{sw_a1}, and K is the sampling ratio. Voltage state variables (S_{p1}, S_{p2}) are obtained by comparing the sampled value to threshold voltages (V_{ref1}, V_{ref2}). The logic processes voltage state variables (S_{p1}, S_{p2}) and switching signals (S_{a1}–S_{a4}) to obtain indicator signals (S_{F_a1}–S_{F_a4}) corresponding to the Boolean expressions. In this circuit, only detected analog signals are processed. Real-time diagnosis results can be obtained as quickly as possible to ensure immediate post-fault reconfiguration and minimize harmful effects.

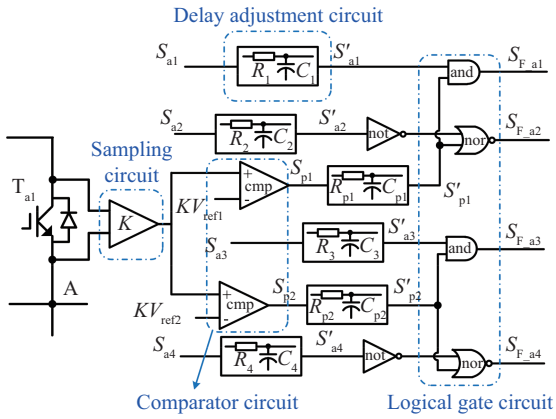

Fig. 9. Diagnostic circuit for expeditious OC fault location in phase A.

TABLE VII
SPECIFICATIONS OF THE T-TYPE INVERTER

Parameter	Symbol	Value
Input dc-link voltage	V_{dc}	400 V
Filter inductances	L_a, L_b, L_c	4 mH
Filter capacitors	C_a, C_b, C_c	4.7 μF
Switching frequency	f_s	10 kHz
Rated output frequency	f	50 Hz
DC-link capacitors	C_1,C_2	2200 μF
Phase voltages	V_{ao}, V_{bo}, V_{co}	110 V(rms)

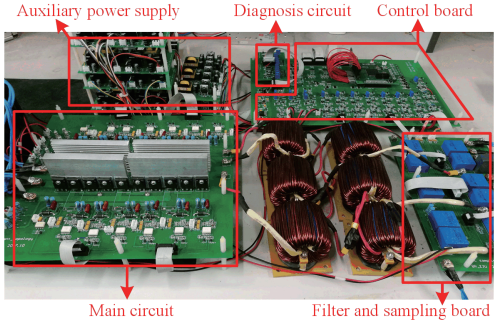

Fig. 10. Experimental platform for T^{2}3LI.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed fault diagnosis method, simulations and experiments have been performed on a T^{2}3LI. The specifications are given in Table VII, and the experimental platform is shown in Fig. 10. The control is based on a TMS320F28335 processor and OC faults in IGBTs are simulated by disabling the corresponding gate driver.

A. Simulation Results

Fig. 11 shows the effect of signal delay during normal operation. Due to delay between T_{a1} and V_{sw_a1}, indicator signal S_{F_a1} can become high when the system operates during a positive half cycle. Delay adjustment will eliminate the potential for misdiagnosis.

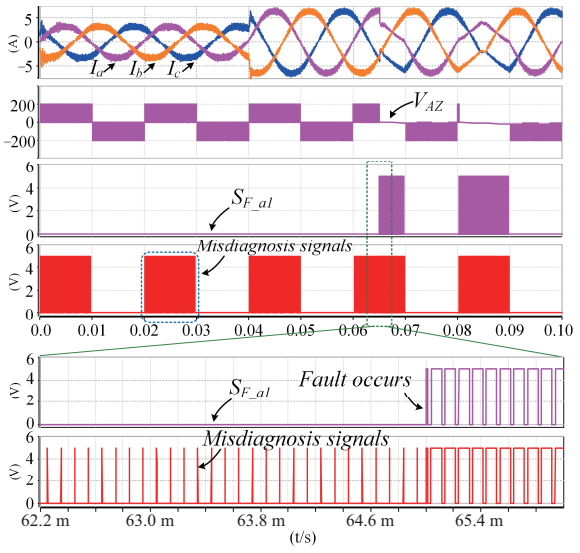

Fig. 11. Simulation waveforms of misdiagnosis due to delay between T_{a1} and V_{sw_a1}.

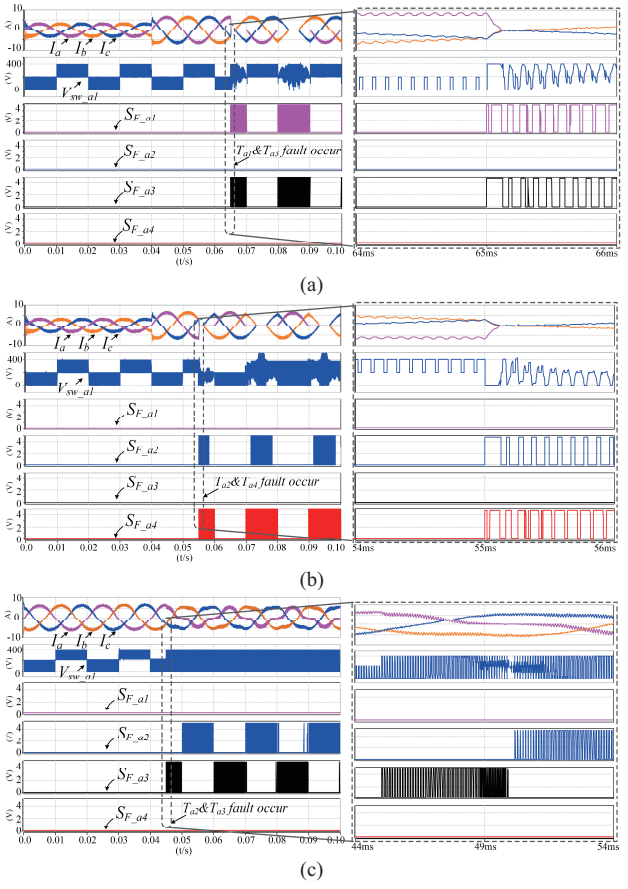

Fig. 12. Simulation waveforms of multi simultaneous OC faults. (a) OC faults in T_{a1} and T_{a3}. (b) OC faults in T_{a2} and T_{a4}. (c) OC faults in T_{a2} and T_{a3}.

Simulated waveforms during normal operation and multiple fault operation are shown in Fig. 12. Fig. 12(a) shows normal operation as a three-phase load changes from 50 Ω to 25 Ω and abnormal operation with simultaneous OC faults in T_{a1} and

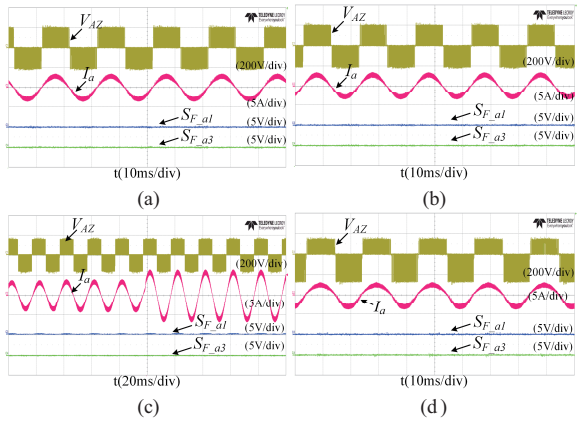

Fig. 13. Robustness of diagnostic methods. (a) Dead time is 1.5 μs. (b) Dead time is 2.5 μs. (c) Load changes from 50 Ω to 25 Ω. (d) Neutral point imbalanced.

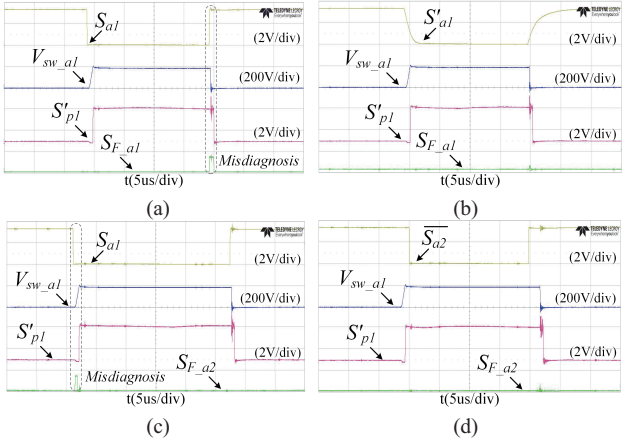

Fig. 14. Misdiagnosis caused during normal operation: (a) Signal delay causes a high-level of S_{F_a1}. (b) Delay adjustment eliminates the misdiagnosis. (c) Signal delay causes a high-level of S_{F_a2}. (d) Dead time of S_{a1} and S_{a2} eliminates the misdiagnosis.

T_{a3}. When faults occur at 0.65 s, the circuit operates in mode I and the phase A current path forms through D_{a4} instead of T_{a1} and T_{a3}. Consequently, indicator signals S_{F_a1} and S_{F_a3} become high. Simulation results for T_{a2} and T_{a4} OC faults are given in Fig. 12(b). When faults occur at 0.55 s, the inverter operates in mode III. Faulty devices correspond to high signals S_{F_a2} and S_{F_a4}. Signals S_{F_a1} and S_{F_a3} remain low, and no misdiagnosis occurs. In Fig. 12(c), simultaneous OC faults in T_{a2} and T_{a3} occur at 0.45 s. Since T_{a3} is open, positive current cannot flow through the neutral point, and S_{F_a3} becomes high. A fault is detected immediately, even though not all faulty transistors will be identified until the circuit shifts to mode IV. After that, at a time of about 0.5 s, signal S_{F_a2} goes high.

B. Experimental Results

In Fig. 13, the experimental prototype is tested to validate the diagnosis method for various dead times, loads, and neutral point imbalance conditions. Fig. 13(a) and (b) show experimental results when the dead time changes from 1.5 μs to

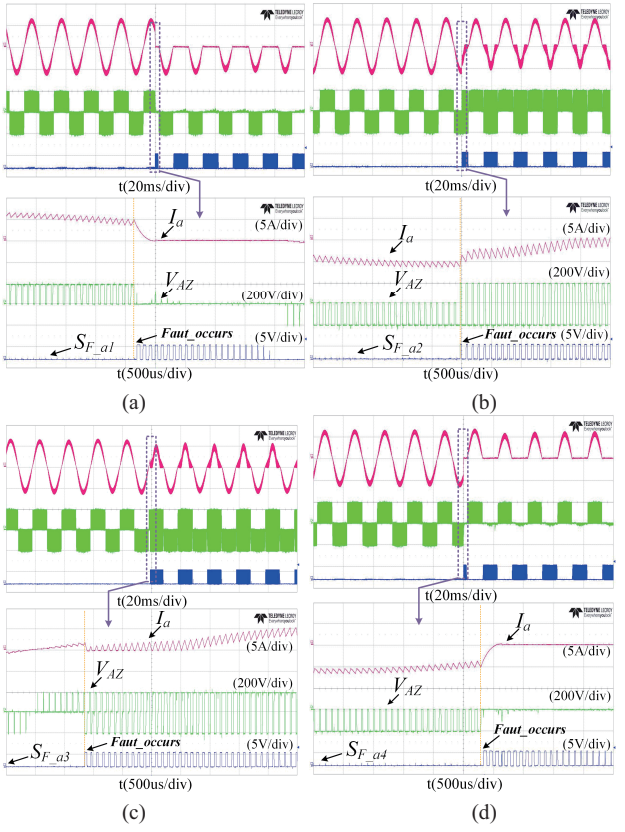

Fig. 15. Diagnosis results for open circuit fault in single transistor: (a) OC fault occurs in T_{a1}. (b) OC fault occurs in T_{a2}. (c) OC fault occurs in T_{a3}. (d) OC fault occurs in T_{a4}.

2.5 μs during normal operation. These dead times do not affect detection. In Fig. 13(c), the transition from half load to full load does not yield a false detection. Fig. 13(d) gives diagnosis results when the dc-link capacitor voltages are unequal (V_{C1} = 140 V, V_{C2} = 260 V). Suitable thresholds for V_{ref1} and V_{ref2} can be set to avoid potential false detection.

In Fig.14, the influence of delay on diagnosis results is given. Threshold voltages can be regulated in accordance with the operating condition to ensure the accurate diagnosis. In the test, V_{ref1} and V_{ref2} are set to 100 V and 300 V, respectively. Fig. 14(a) and (c) show misdiagnosis occurring on S_{F_a1} and S_{F_a2} during normal operation due to delay between S_{a1} and S'_{p1}. Misdiagnosis in S_{F_a1} can be eliminated by using an RC filter to delay the rising edge of S_{a1}, as shown in Fig. 14(b). Fig. 14(d) shows that increasing the dead time from 1 us to 1.5 us eliminates misdiagnosis in S_{F_a2}. This is true provided the dead time of S_{a1} and S_{a2} is long enough to cover the delay.

Fig. 15 provides diagnosis results when each transistor in phase A has an OC fault. When a fault in T_{a1} is detected during mode I, signal of S_{F_a1} goes high, as shown in Fig. 15(a), since pole voltage V_{AZ} changes to 0 instead of $0.5V_{dc}$. If T_{a2} fails when $I_a < 0$, phase A operates in state [P] since no current flows through the neutral point. Similarly, state [O] will be unreachable when $I_a > 0$ due to an OC fault in T_{a3}. Phase A will operate in states [P] and [N]. The inverter can output positive and negative voltages, but current distortions will increase.

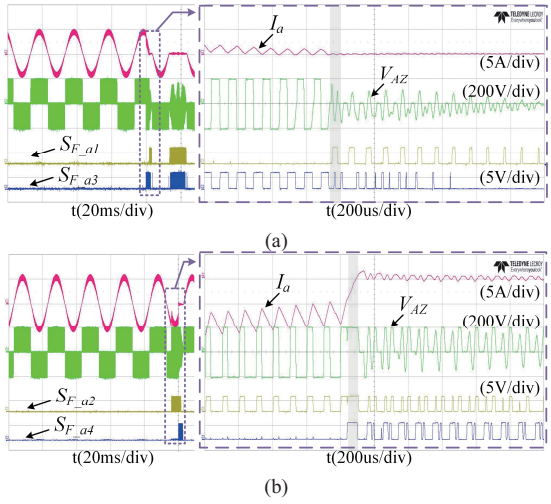

Fig. 16. Experimental results of OC fault diagnosis for multi transistors: (a) OC faults occur in T_{a1} and T_{a3} during the positive half cycle. (b) OC faults occur in T_{a2} and T_{a4} during the negative half cycle.

Signals S_{F_a2} and S_{F_a3} become high immediately for their respective faults, as shown in Fig. 15(b) and (c). Fig. 15(d) shows that, during the negative half cycle, an OC fault in T_{a4} is identified when an abnormal current path forms through the neutral point and V_{AZ} changes to 0.

Waveforms for multiple OC faults are given in Fig. 16. After faults in T_{a1} and T_{a3} are triggered, the current flows through D_{a4} and V_{AZ} becomes $-0.5V_{dc}$ during the positive half cycle, as shown in Fig. 16(a). Faults in T_{a1} and T_{a3} correspond to high signals S_{F_a1} and S_{F_a3}. In Fig. 16(b), when a fault occurs in T_{a2}, the post-fault current path forms through D_{a1} and operating state [O] is replaced by state [P]. If T_{a4} fails during mode III, the current flows through diode D_{a1}. The pole voltage remains $0.5V_{dc}$. Faulty transistors correspond to high signals S_{F_a2} and S_{F_a4}.

As illustrated in Figs. 15 and 16, both single and multiple transistor OC faults in the T^{2}3LI can be identified within a switching cycle.

V. Conclusion

This paper presents a fast diagnosis method for OC faults in a T-type three-level inverter. Post-fault state transitions in the FSM model can represent single and multiple fault scenarios. A circuit was designed and employed to gather real-time fault information by comparing and processing logical relationships between detected analog signals. It can improve the diagnosis reliability and shorten the response time without being affected by the control strategy, sampling frequency, and computational effort. The detection time limits depend on sensor delays, switching delays, edge blanking, and fault timings. The maximum fault detection time is less than a switching cycle, which facilitates quick implementation of post-fault reconfiguration. The contributions in this paper can be summarized as follows: 1) For multiple diagnosis targets, a systematic analysis method combining FSM with RST is presented to minimize detection signals that identify all possible operating states. 2) To distinguish abnormal state transitions and avoid repetitive detection characteristics in single and multiple fault scenarios, current path variations are adopted to establish the FSMs. 3) A simple circuit with flexible debugging is designed to detect system operating states in real time; 4) Complementary switching signals with longer dead time than the delay time are used to eliminate misdiagnosis due to switching noise and delay. Experimental results under various conditions verify the effectiveness of the proposed method.

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