Application of GaN Devices for 1 kW Server Power Supply with Integrated Magnetics

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Abstract—In today's power electronics products, quality and reliability are given. Great emphases are placed on high efficiency, high power density and low cost. With recent advances made in gallium nitride power devices (GaNs), it is expected that GaNs will make significant impacts to all three areas mentioned above. Thanks to the absence of reverse recovery charge and smaller junction capacitances, the turn-on loss of GaN is significantly reduced and Turn-off loss and driving loss are negligible, for the first time. These desired properties coupled with ZVS techniques will drastically reduce all switching related losses, thus enabling GaN to operate at a switching frequency more than ten times higher than its silicon counterparts. To illustrate the impact of GaN on efficiency, density and even design practice, a 1 kW server power supply is demonstrated which employs an interleaved CRM totem-pole PFC followed with an LLC resonant converter. Both operate beyond 1 MHz. All magnetic components are integrated into PCB with much reduced EMI noises, thus, only a simple one-stage EMI filter is required. The system achieves a power density more than 150 W/in^3, an efficiency above 96%, and much improved manufacturability with minimum labor content.

Index Terms—GaN device, soft switching, MHz, totem-pole PFC, LLC converter, coupled inductor, balance technique, matrix transformer, shielding.

I. INTRODUCTION

IN today's power electronics products, quality and reliability are given, Great emphases are placed on high efficiency, high power density and low cost. Further advances alone these areas will be closely linked to advancement we can make in the area of power devices and materials and fabrication techniques. With recent advances made in wide-band-gap (WBG) power devices, the new generation of switches will make significant impacts to all three areas mentioned above.

It is evident that, for any given design, if simply replacing silicon devices with WBG, an improvement in efficiency can be made. Although it is an important contribution, to leave it at that, it does not do the justice to WBG. It is also clear that WBG devices can operate at much higher frequencies compared to their silicon counterparts. Consequently, as much as a factor of 5-10 reduction in size/weight using WBG are achievable and have been demonstrated in some

applications. Still it leave it at that, it does not realize the full potential of WBG. If we can design a converter with 10X, 20X or even 50X in switching frequency, comparing to our current practice using silicon devices, what has been taken for granted in our design practice is being challenged.

The ever increasing demand for high-efficiency and high-density switch-mode AC/DC power supplies include but not limited to computers, telecommunication, data centers, electrical vehicle battery chargers, PV inverters, numerous industrials, and aerospace applications. Collectively, these products consume more than 10% of the total electric power. One percent of efficiency improvement, in this sector, represents 20 TWH of energy saving. The amount of energy saving is equivalent to the total energy outputs of three average size nuclear power plants, each at 7 TWH annual production. Moreover, with the increasing of cloud computing and big data, it is expected that data center alone will consume 10% of the total electricity by 2020. A typical example of a 1 kW AC/DC server power supplies is illustrated in Fig. 1. With 40% of the components manually inserted, manufacturing of this power supply is labor intensive. The trend will not reverse unless there is a paradigm shift in the way we design and manufacture these power supplies.
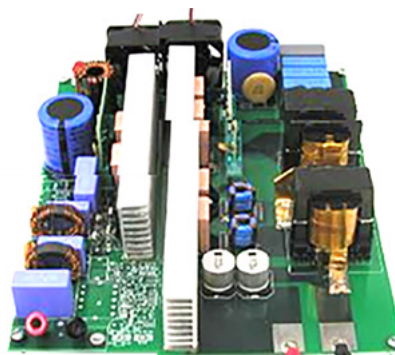

Fig. 1. A typical 1 kW AC/DC converter.

Within this industry sector, data center server power supplies are the most performance driven, energy and cost conscious. Within a data center, all major processor/ memory devices are powered from a 12V bus. This 12V bus architecture was developed in the early 90's, when the power consumption was minuscule in comparison with today's usage. For example, each microprocessor is consuming 100A-200A current. The i^{2}R loss for a 12V bus is excessive. To mitigate the heavy bus-bar loss in the power distribution

path, industry leaders such as Google, Facebook, Cisco and IBM are already implementing new data center design with higher voltage distribution bus, such as 48V or 400V instead of 12V.

To support these power architecture changes, it is mandatory that the power supplies off the utility lines to be in a form of distributed power on the printed circuit board in the vicinity of the core processors and memory devices. The distributed power supplies have to be very efficient and with high power density to be compatible with core processors, memories, et al. Present power supplies are operating at 50-100 kHz with a power density less than 50 W/in^3. An order of magnitude power density improvement is necessary for the wide spread use of the distributed power for all computer servers and data centers.

Advanced power semiconductor devices have consistently proven to be a major force in pushing the progressive development of power conversion technology. The emerging gallium-nitride-based power semiconductor device is considered a promising candidate to achieve high-frequency, high-efficiency, and high-power-density power conversion [1]-[17]. Due to the advantages of the material, the GaN HEMT has the features of a wide band gap, high electron mobility, and high electron velocity [1], [2]. Thus a better figure of merit can be projected for the GaN HEMT [3] than for the state-of-the-art Si MOSFETs, which allows the GaN HEMT to switch with faster transition and lower switching loss. By using the GaN HEMT in a circuit design, the switching frequency can be pushed up to MHz frequencies, and continue to have high efficiency [4]-[11].

To realize the benefits of GaN devices resulting from significantly higher operating frequency, a number of issues have to be addressed, such as converter topology, magnetics, control, packaging, and thermal management. In Section II, the switching characteristic of high voltage GaN devices is studied including comparison between hard switching and soft switching; a 1-3 MHz CRM totem-pole PFC with integrated coupled inductor is demonstrated in Section III; then an 1 MHz LLC resonant converter with integrated matrix transformer is presented in Section IV; finally, complete EMI performance is evaluated and the corresponding EMI filter design for this MHz server power supply is verified in Section V.

II. SWITCHING CHARACTERISTICS OF GALLIUM NITRIDE TRANSISTORS

Gallium Nitride devices are gathering momentum, with a number of recent market introductions for a wide range of applications such as point-of-load converters (POL), off-line switching power supplies, battery chargers and motor drives. GaN devices have a much lower gate charge and lower output capacitance than silicon MOSFETs and, therefore, are capable of operating at a switching frequency 10 times greater. This can significantly impact the power density, form factor and even the current design and manufacturing practices.

A. Modeling of double-pulse tester

Understanding the switching characteristic of GaN switches is essential to use GaN devices in circuit design correctly and more efficiently.

In hard-switching converters, the overlap of voltage and current across drain and source of the device leads to significant power losses during switching event. To better illustrate the switching characteristic of high voltage GaN switches, a typical switching waveforms of the top switch in a buck converter, are shown in Fig. 2. During turn on transition, a large current overshoot is induced by the junction capacitor charge of the bottom switch. In addition, cascode GaN has additional charge due to the reverse recovery of the low voltage silicon MOSFET in the cascode configuration. The integral of voltage and current during turn on transition generates significant power dissipation, which is in the magnitude of tens of uJ. Even through, the turn on switching loss of GaN is still much lower compared with Si MOSFET which has the same breakdown voltage and same on resistance.

On the other hand, the cross time of the drain-source voltage and current during turn off transition is quite short and the energy dissipation is less than a few uJ. The major reason for such a small loss is due to high transconductance of GaN devices. In addition, the cascode GaN has smaller turn off loss at higher current condition due to intrinsic current source driving mechanism [18], [19]. The cascode structure minimizes the miller effect during turn off transition, and therefore, the loss is not sensitive to the turn off current.

(a) Turn on transition waveforms   (b) Turn off transition waveforms waveforms

(c) Turn on switching energy (Solid line: Cascode GaN; Dash line: E-mode GaN)   (d) Turn off switching energy (Solid line: Cascode GaN; Dash line: E-mode GaN)
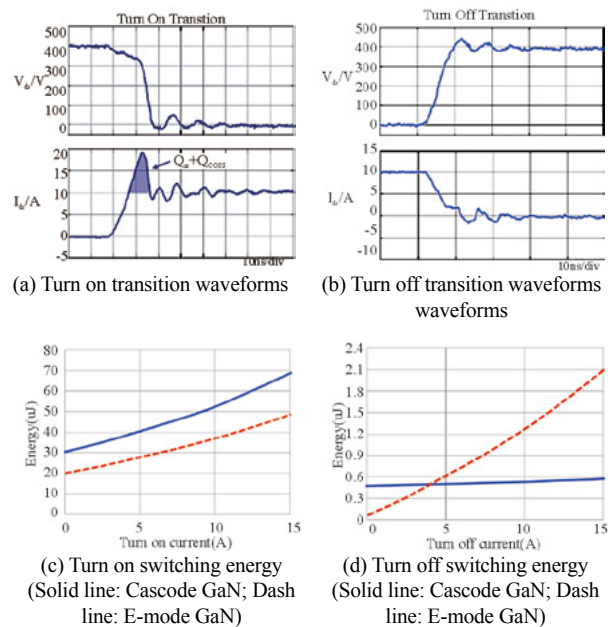
Fig. 2. Switching characteristic of high voltage GaN transistors.

B. Packaging Influence

Both e-mode GaN devices and cascode GaN devices

are able to switch very fast. However, parasitic inductance introduced by the bulky package became a limit which results in large switching loss and severe oscillations during switching transitions.

Regarding packaging influence study, many efforts are spent on the Si MOSFET with monolithic structure [20]-[22]. It is well studied the common-source inductance (CSI), which is defined as the inductance shared by power loop and driving loop, is most critical. The CSI acts as negative feedback to slow down the driver during the turn-on and turn-off transitions, and thus prolongs the voltage and current crossover time, and significantly increases the switching loss.

Similar theory can be applied to e-mode GaN devices. Fig. 3 shows package related parasitic inductance of a typical through-hole package (TO-220) and a typical surface-mount package (PQFN), while their inductance based on real devices are listed in TABLE I. Here the inductance value is extracted by FEA simulation in Ansoft Q3D. Through this comparison, it can be observed that surface mount package is effective to reduce the value of parasitic inductance while Kelvin connection (K) is able to decouple power loop with driving loop so that the source inductance is no longer the common source inductance.

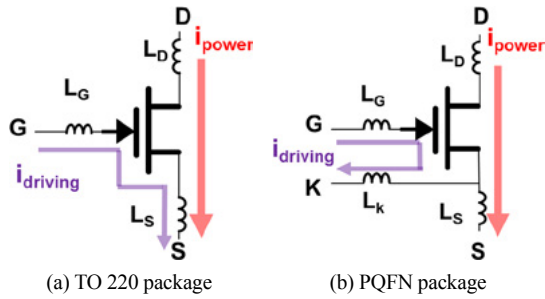
(a) TO 220 package   (b) PQFN package

Fig. 3. Package related parasitic inductance distribution of e-mode GaN.

TABLE I
PACKAGE RELATED PARASITIC INDUCTANCE VALUE

	LG	LD	LS	LK
TO-220	3.6nH	2.3nH	3.9nH	N/A
PQFN	2.4nH	1.3nH	0.9nH	1.3nH

Unlikely to e-mode GaN devices, the cascode GaN device has much complex parasitic inductance distribution and the identification of the CSI is not straight-forward [23], [24]. In the first step, the CSI of the low-voltage Si MOSFET and of the high-voltage GaN HEMT are analyzed separately. From the perspective of the Si MOSFET, L_{int3} and L_S are the CSIs of the Si MOSFET; while from the perspective of the GaN HEMT, L_{int3} and L_{int1} are the CSIs of the GaN HEMT. Therefore, in terms of the cascode GaN device (Fig. 4), since L_{int3} is the CSI for both the GaN HEMT and the Si MOSFET, it is the most critical parasitic inductance. L_{int1} is the second critical inductance, since it is the CSI of the high-voltage GaN HEMT, which has the major switching loss. Finally, L_S

is the third critical inductance.

According to the analysis, the traditional package has significant side effect on the device switching performance. Then stack-die package is proposed to solve the package related issues [25]-[27].
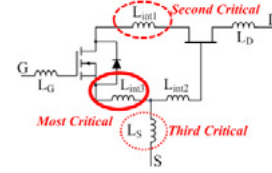

Fig. 4. Common source inductance distribution in cascode GaN device.

The stack-die package is able to eliminate all common source inductance. As shown in Fig. 5(b), in the stack-die package of cascode GaN device, the Si MOSFET (drain pad) is mounted on top of the GaN HEMT (source pad) directly. The interconnection between two dies are minimized in this way, thus the stack-die package is considered as the optimized package for cascode GaN device.
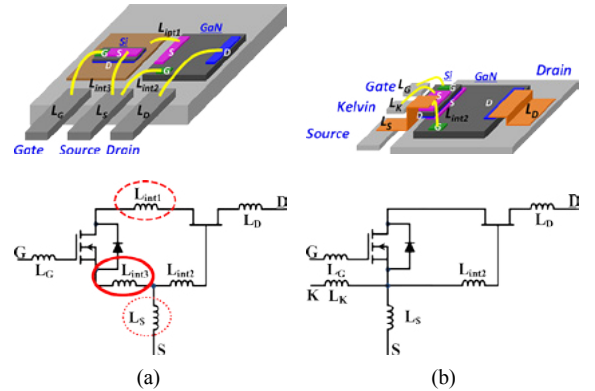

(a)   (b)

Fig. 5. Package bonding diagram and schematic for cascode GaN HEMT (a) TO-220, and (b) stack-die.

C. Comparison Between Hard-switching and Soft-switching

Even with a better package, the turn-on switching loss of high voltage GaN switch under hard-switching conditions is significant and dominant in high frequency applications, where the loss could be 10-20 W loss at 500 kHz operation, for example. ZVS turn-on is strongly desired to fully exploit the potential of the GaN switch. Critical conduction mode (CRM) operation is the most simple and effective way to achieve ZVS turn-on and is widely used in medium-low power applications.

Fig. 6 shows the efficiency comparison of soft-switching and hard-switching buck converter with GaN devices. The switching frequency at 6A full load output is designed to be 500 kHz. Fig. 6(b) shows the loss breakdown under full load condition. The chart clearly shows that the turn on loss is minimized with ZVS and only introduces a little more conduction loss. The increase of conduction loss is due to the increased ripple current and corresponding circulating

energy which is used to achieve ZVS.
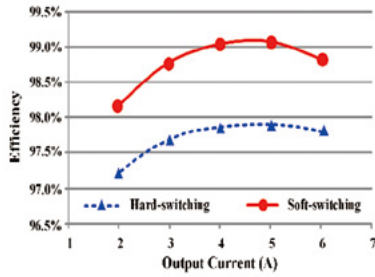
(a) Efficiency comparison.
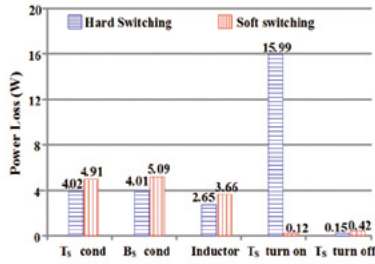
(b) Loss breakdown at full load.

Fig. 6. Soft-switching vs. Hard-switching.

III. Totem-Pole PFC with Integrated Coupled Inductor and Balance Technique

A. GaN-Based MHz Totem-Pole PFC

With the advent of 600V gallium-nitride (GaN) power semiconductor devices, the totem-pole bridgeless power factor correction (PFC) rectifier [28], [29], which was a nearly abandoned topology, is suddenly become a popular front end candidate for applications like 2-stage high-end adaptor, server and telecommunication power supply, and on-board battery charger. This is mostly attributed to the significant performance improvement of the GaN HEMT compared to Si MOSFET, particularly better figure-of-merit and significantly smaller body diode reverse recovery effect.

GaN-based hard-switching totem-pole PFC rectifier is demonstrated in literature [30]. As the reverse recovery charge of the GaN HEMT is much smaller than the Si MOSFET, hard-switching operation in totem-pole bridge configuration turned to be practical. By limiting switching frequency around or below 100 kHz, the efficiency could be above 98% for a 1 kW level single-phase PFC rectifier. Even the simple topology and high efficiency are attractive, the system level benefit is limited because the switching frequency is still similar to Si-based PFC rectifier.

Based on previous study, soft switching truly benefits the cascode GaN HEMT. As the cascode GaN HEMT has high turn-on loss and extremely small turn-off loss due to the current-source turn-off mechanism, critical mode (CRM) operation is very suitable. A GaN-based critical mode (CRM) boost PFC rectifier is first demonstrated which shows the high-frequency capability of the GaN HEMT and significant

system benefits as the volume of the boost inductor and the DM filter is dramatically reduced [31], [32].

With a similar system-level vision, the cascode GaN HEMT is applied in the totem-pole PFC rectifier while pushing frequency to above 1 MHz. Several important high-frequency issues, which used to be less significant at low-frequency, are emphasized and the corresponding solutions are proposed and experimentally verified. They are including ZVS extension in order to solve switching loss caused by non-ZVS valley switching; variable on-time control to improve the power factor, particularly the zero-crossing distortion caused by traditional constant on-time control; and interleaving control for input current ripple cancellation.
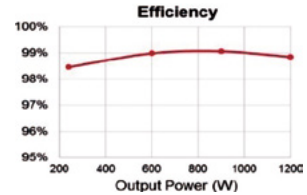
A 1.2 kW dual-phase interleaved MHz totem-pole PFC rectifier is built with 99% peak efficiency and 700W/in^3 power density (without bulk cap), as shown in Fig. 7 in which the inductor is significantly smaller compared to state-of-the-art industrial practice [33]-[37].
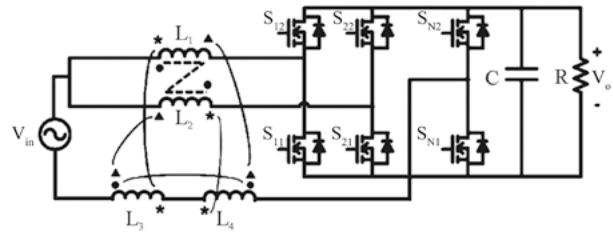
(a)
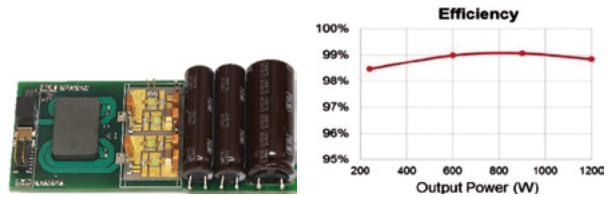
(b)   (c)

Fig. 7. GaN-based MHz totem-pole PFC (a) topology, (b) prototype, and (c) measured efficiency.

B. Integrated Coupled Inductor with Balance Technique

The concept of coupled inductor, developed at CPES [38], has been widely used in multi-phase VRM to reduce loss and improve transient performance. This concept has been extended to two-phase interleaved totem-pole PFC rectifier. One special feature of the coupled inductor in this application is that the effective inductance value will change with duty cycle, in a manner that when duty cycle is approaching 0.5, L value will increase. Subsequently, the switching frequency will decrease as shown in Fig. 8. The net benefit is a reduction of the switching losses by 35%.

One of the important concerns with using the GaN devices is the potential high EMI noises resulting from high di/dt and dv/dt during switching. While the concern may be a genuine one with the conventional design practice, the use of PCB integrated magnetics offers the opportunity for significant reduction of common mode (CM) noises. This is achieved

by incorporating CPES developed balancing technique [37] relatively easy in the PCB winding structure.
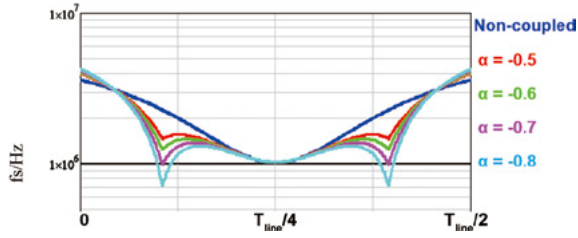

Fig. 8. Switching frequency variance during half line cycle.

In order to use the balance principle for CM noise reduction, two additional inductors L3 and L4 are employed and are coupled with L1 and L2 respectively. Fig. 9 shows the circuit topology and the integrated magnetic structure. By use the superposition theory to Fig. 10 (a), the equivalent circuit for the noise source Vs1, is shown in Fig. 10 (b). The number of turns of L1 and L2 is N1. The number of turns of L3 and L4 is N2. Thus, we have the balance condition for source V1 is $N_1 / N_2 = C_b / C_d$.
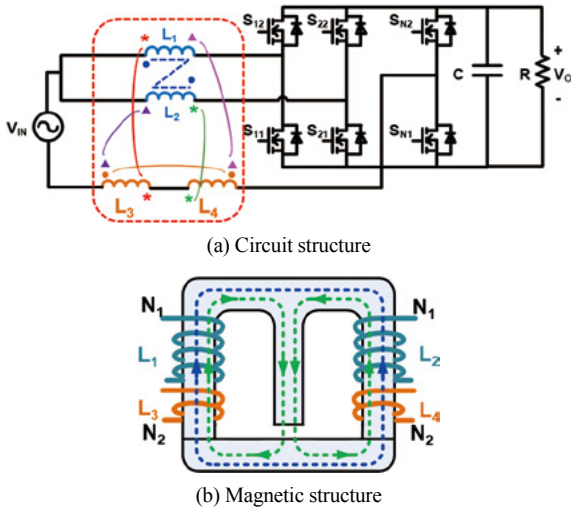

(a) Circuit structure

(b) Magnetic structure

Fig. 9. Improved balance technique for interleaved totem-pole PFC converter with coupled inductor.
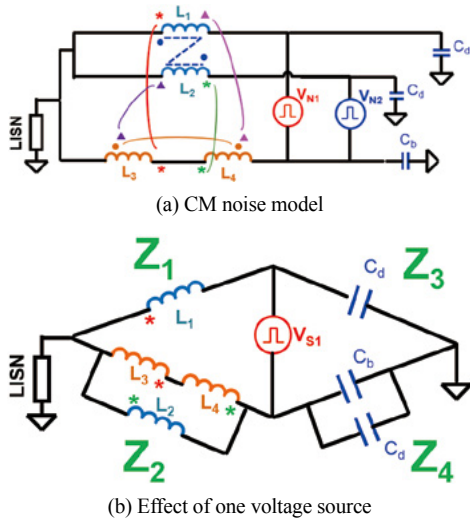

(a) CM noise model

(b) Effect of one voltage source

Fig. 10. Equivalent circuit of CM noise.

Similarly, the balance condition for noise source V_{N2} is also $N_1 / N_2 = C_b / C_d$. The CM noise of this PFC converter can be minimized as long as this balance condition is achieved. Fig. 11 shows that with balance technique, CM noise can be effectively reduced.
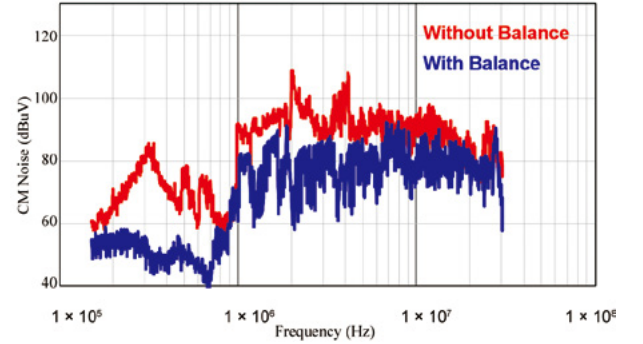

Fig. 11. CM noise reduction result with balance technique. v

Fig. 12 shows the proposed coupled inductor with coupling coefficient, α = -0.7. The windings are partially interleaved to reduce winding losses and in the same time provide the desired negative coupling. The windings near the air gap are tapered to avoid fringing flux [37].

With the PCB winding, balance technique can be applied to reduce CM noise [37]. The balance winding can be easily implemented by replace the bottom layer of PCB winding with the one-turn balance inductor L3 and L4, as shown in Fig. 12. TABLE II shows the simulated loss breakdown of this coupled inductor with balance technique. The total loss is similar as the non-coupled inductor with litz wire.

Fig. 12. Coupled inductor with balance.

TABLE II
LOSS BREAKDOWN FOR INDUCTOR

	DC W. Loss/W	AC W. Loss/W	Core Loss/W	Total Loss/W
PCB winding coupled inductor	0.6	2.1	1.9	4.6
Litz wire non coupled inductor	0.7	1.6	2.3	4.6

For the sake of comparison, TABLE II also shows the loss breakdown for two non-coupled inductors using two ER23 core. The winding is 250/46 litz wire with 10 turns for each inductor. According to conventional wisdom, the PCB based inductor design is inferior to the conventional litz wire wrapped around a core. However with proposed design,

similar total loss is achieved by the proposed PCB based coupled inductor.

IV. LLC CONVERTER WITH INTEGRATED MATRIX TRANSFORMER

For the DC/DC stage, the LLC resonant converter is deemed the most desired topology because of its high efficiency and high power density. The LLC converter can achieve ZVS for the primary devices and ZCS for the secondary SRs. These features are not only beneficial for achieving higher efficiency but also for lower EMI noises.

For applications that require low-voltage, high-current outputs, such as computer servers, there are several important design considerations: 1) the state-of-the-art synchronous rectifiers (SRs) are best operated with 10-15A. For server applications, one should consider paralleling 4-8 SRs. Both static and dynamic current sharing, when paralleling a large number of SRs, are difficult to achieve. 2) The large sum of high frequency and high di/dt ac currents much flow through a common termination point between the transformer and the SRs. This can result in large termination losses. 3) Large leakage inductances at the transformer secondary-side windings result in large winding losses.

To overcome the challenges in low-voltage, high-current outputs application, the traditional single core structure was divided into a 4-core matrix transformer structure, as shown in Fig. 13, whose primary windings in series and the secondary windings in parallel. Since the primary current for the 4 transformers are the same, the secondary current are perfectly balanced. The termination point, where all currents are summed, occurs on the DC side, thus, no termination loss. Transformer winding losses are significantly reduced as well as the leakage inductances [39], [40].
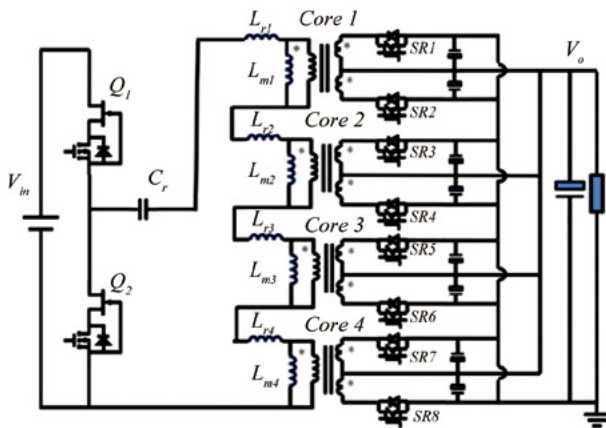

Fig. 13. LLC converter with matrix transformers incorporating 4 sets of outputs.

Furthermore, the four transformers can be integrated into two-core structure by means of flux cancellation, thus, resulting in reduced core volume and core loss [40]. The first generation of the prototype LLC converter, as shown in Fig. 15(a), achieved a peak efficiency of 95.5% and power

density over 700W/inch^3. By increasing the switching frequency to be ten times higher than the state-of-the-art industry practice, the power density is much better than the state-of-the-art even the output is changed from 1 set of output to 4 sets of outputs.

In the loss analysis, it is found that the winding losses are dominating. Further division of the 4-transformer structure into an 8-transformer structure, as shown in Fig. 14, would yield a significant reduction in losses, both in transformer windings and SRs. The transition from 4 sets of outputs to 8 sets of outputs, although at the expense of increased core loss, is worth doing since the core loss is a small portion of the total loss with MHz switching frequency. Increasing the number of outputs to improve efficiency is only achievable with high switching frequency due to the much reduced core loss [41] and higher di/dt ac currents compared to the state-of-the-art industrial practice operating at around 100 kHz.
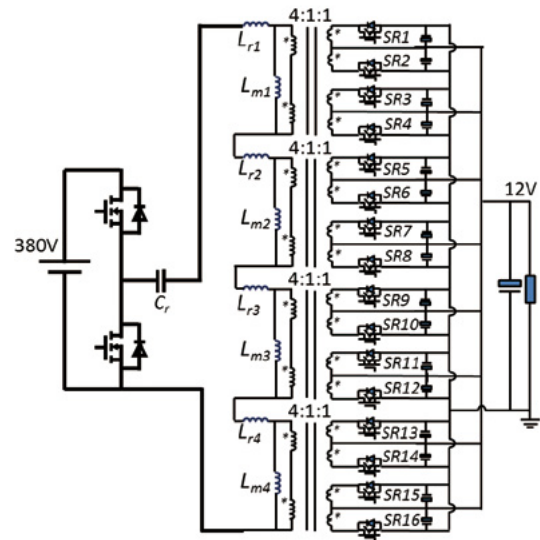

Fig. 14. LLC converter with matrix transformers incorporating 8 sets of outputs and flux cancellation.

Subsequently, the second-generation prototype was developed as shown in Fig. 15(b), leading to a much improved efficiency as shown in Fig. 16 [42]. It should be noted that the improvement of efficiency is not at the expense of power density. The power density remains essentially the same, at 700W/in^3. The efficiency is higher than the state-of-the-art industry practice while the power density is ten times better. The windings were implemented using only 4-layer PCB. The system cost is considerably lower and the design can be fully automated.
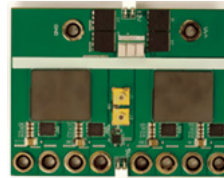

Fig. 15. (a) Prototype of 1st generation.

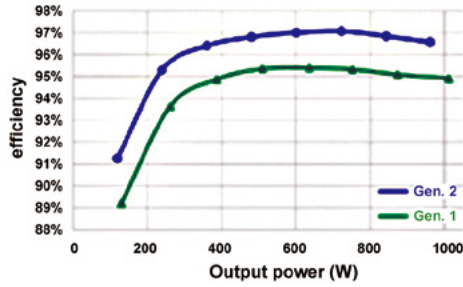Fig. 15. (b) Prototype of 2nd generation.

Fig. 16. Efficiency of the two generations.

For the matrix transformer, the PCB windings are fully interleaved, which leads to large distributed inter-winding capacitors and, hence, large CM noise current. In this design, the inter-winding capacitance is estimated at 800pF. The CPES patent shielding technique [43], [44] is incorporated in the design, by placing shielding layers in between primary and secondary windings. Fig. 17 illustrate the transformer structure with shielding. Each shielding layer is connected to the primary ground. Therefore the CM noise current can only circulate in the primary side.

Fig. 17. Transformer structure with shielding.

The shielding layers are made identical to the secondary windings, both are single-turn windings. Therefore, there is zero potential difference between the shielding winding and the secondary winding, thus, no CM current. Fig. 18 demonstrated the effectiveness of this shielding concept. The noise spectrum in red is without shielding and the noise spectrum in blue is with shielding. A maximum 23 dBuV CM noise reduction is realized by this simple technique.
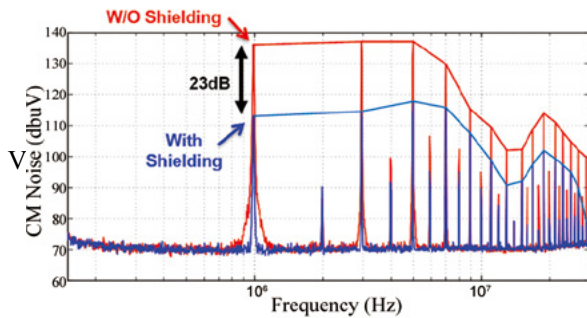

Fig. 18. CM noise test result.

When operating LLvvC converter at very high switching frequency, the control is very challenging due to the fast dynamics of the resonant tank. Recently, CPES has successfully developed a digital based state-trajectory control with a nearly one-cycle response. This proposed controller incorporates the state-trajectory control techniques [45], [46]. A multitudes of technology breakthroughs have been reported in recent literature including: soft start-up and short-circuit protection to minimize stresses; auto-tuning to minimize SR losses; fast load transient response; burst mode for improved light load efficiency [47]-[52]. These techniques, over several generations of developments, have reached a point where they can finally be realized using a low-cost digital controller to control the high frequency LLC converters.

In summary, the transformer design methodology, CM noise reduction and digital control for high frequency LLC converters have been successfully demonstrated.

V. System Demonstration

Conventionally, in order to achieve enough noise attenuation, people have to use two stage EMI filter, which has high cost and large volume. Thanks to the high switching frequency and all the EMI reduction techniques, it is possible to use simple one stage filter to achieve required attenuation. Fig. 19 and Fig. 20 show the demonstration of single stage filter. Compared to traditional two stage filter, the single stage filter can achieve 80% volume reduction.
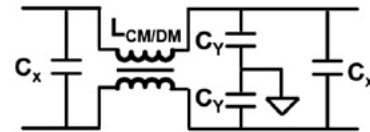

Fig. 19. Single stage EMI filter topology.

Fig. 20. Picture of single stage EMI filter.

Fig. 21 and Fig. 22 show the EMI noise measurement results. It can be seen that with one stage filter, the noise is below EMI EN55022B standard.
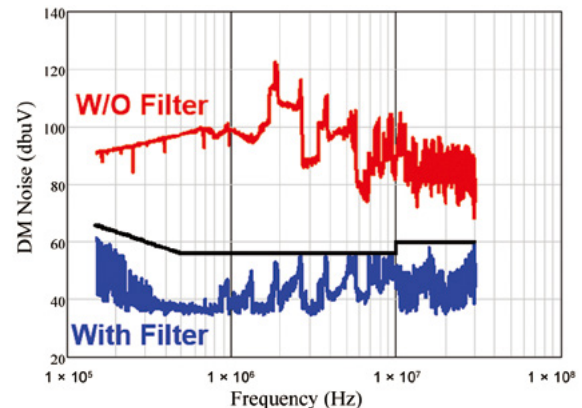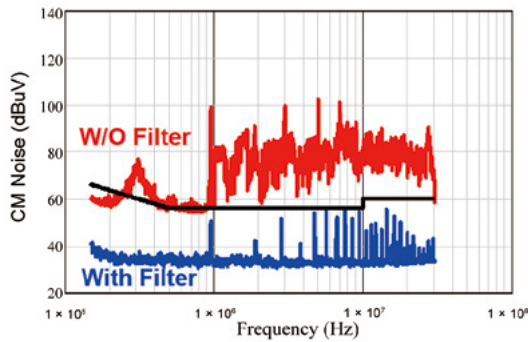

Fig. 21. DM noise measurement.

Fig. 22. CM noise measurement.

Finally, the total system is demonstrated as Fig. 23 and Fig. 24. The key features are including 1-3 MHz high frequency, soft switching for all GaN devices, integrated magnetics design, simple 1-stage EMI filter, and designed for manufacturability. Fig. 25 shows the efficiency curve of the system. It even outperforms the state-of-the-art products who is qualified of 80 Plus Titanium standard.
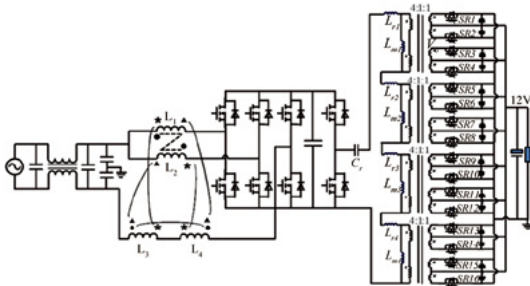

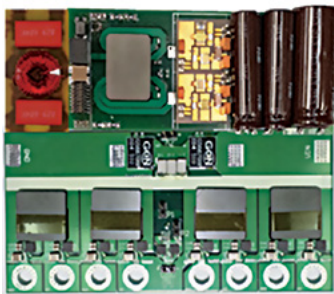Fig. 23. Topology of total system.

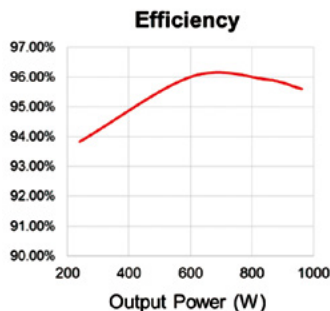Fig. 24. Prototype of total system.

Fig. 25. Tested system efficiency.

VI. Conclusion

The switching characteristics of high voltage GaN devices are evaluated. It is shown that the switching related losses are significantly reduced when compared to silicon MOSFET. Specifically, the turn-off loss and driving loss are negligible. If the ZVS technique is employed to eliminate the turn-off loss, the GaN based converters are capable of operating at a switching frequency more than ten times higher than its silicon counterparts. However, a number of important issues have to be address in order to better utilize GaN devices in high-frequency circuit design. Advanced packaging and circuit layout with minimized parasitics are essential to realize the promising performance of GaN.

At the system level, a design of 1 kW server power supply operating at a switching frequency beyond 1 MHz is used to demonstrate the impact of GaN in such important issues as efficiency, power density and manufacturability. As the switching frequency is extended beyond 1 MHz, windings for both PFC inductors and LLC transformers can be integrated into PCB with significantly improvement in efficiency, density, and EMI.

The impact of GaN devices on power electronics goes beyond efficiency and power density improvement. Even though GaN is still in an early stage of development, it is presumably a game-changing device with a scale of impact yet to be defined. Certain design trade off previously inconceivable can be realized with not only significant performance enhancement but also drastic reduction of the labor contents in the manufacturing.

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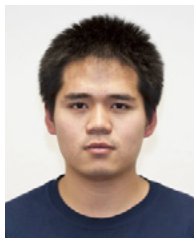
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