Turn-On Oscillation Damping for Hybrid IGBT Modules

Nan Zhu, Xingyao Zhang, Min Chen, Seiki Igarashi, Tatsuhiko Fujihira, and Dehong Xu

***Abstract*—In a hybrid IGBT module with SiC diodes as free-wheeling diodes, high frequency oscillation occurs during turn-on due to the fast switching transient of SiC diode and the resonance between circuit parasitic inductances and the junction capacitance of SiC diode. Such oscillation causes EMI noise which may affect the performance of the system. Methods to mitigate the turn-on oscillation are studied. Firstly, the effect of gate drive parameters on turn-on oscillation is investigated with respect to different gate voltages and gate charging currents. Then a novel turn-on oscillation suppression method is proposed with combination of damping circuit and active gate driver. The proposed oscillation suppression method can achieve the lowest EMI noise while remaining the advantage of lower switching loss brought by SiC diodes. Detailed theoretical analysis of the turn-on oscillation is conducted, and experimental results are given to verify the effectiveness of the proposed oscillation suppression method.**

***Index terms*—Hybrid IGBT module, SiC SBD, turn-on oscillation damping, active gate driver**

NOMENCLATURE

v_{CE1}, v_{CE2}, v_{CE}	Collector-emitter voltage of the IGBT
i_{C1}, i_{C2}, i_C	Collector current of the IGBT
v_{GE}	Gate-emitter voltage of the IGBT
i_{G1}, i_{G2}, i_G	Gate current of the IGBT
v_G	Gate voltage provided by the voltage source gate drive circuit
V_+, V_-	High and low level voltages of the voltage source gate driver
I_G	Gate current of IGBT provided by the current source gate driver
V_{DC}	DC bus voltage
I_L	Load current of the inductive switching test
$R_{g,int}$	Internal gate resistance of IGBT module
$R_{g,ext}$	External gate resistance of IGBT module
C_S	Capacitance of the RC damping circuit
R_S	Resistqance of the RC damping circuit
v_{Cs}	Voltage of the damping capacitor
i_S	Current flowing though the RC damping circuit
i_{dc}	DC bus current
I_{OSC_MAX}	Maximum oscillation current
t_s	Settling time of oscillation
L_p	Stray inductance of the DC bus bar
L_{1C}, L_{1eE}, L_{1E}, L_{2C}, L_{2eE}, L_{2E}	Stray inductances in the IGBT module
$L_m=L_{1C}+L_{1eE}+L_{1E}+L_{2C}+L_{2eE}+L_{2E}$	Lumped stray inductance of the IGBT module
R_p	Parasitic resistance of the commutation loop
C_{CE1}, C_{CE2}	Combination of the collector-emitter capacitance of IGBT and junction capacitance of the anti-parallel SiC SBD
C_{GE1}, C_{CG1}, C_{GE2}, C_{CG2}	Gate-emitter and collector-gate capacitances of the IGBT
g_{fe}	Transconductance of the IGBT
E_{on}	Turn-on energy loss of the IGBT
$E_{damp,on}$, $E_{damp,off}$	Loss in the damping resistor during turn-on and turn-off

Manuscript received December 10,2016. This work is supported by National Natural Science Foundation of China (51277163, 51337009, 51477152), and the National High Technology Research and Development Program of China 863 Program (2012AA053601). This work is also partly supported by Zhejiang University and Fuji Electric joint research project. Part of this research has been published in Conference Proceeding of 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia).

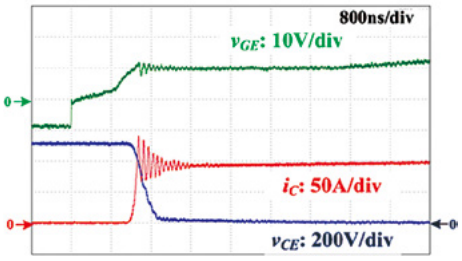
Nan Zhu, Xingyao Zhang, Min Chen, and Dehong Xu are with College of Electrical Engineering, Zhejiang University, Hangzhou, China, Seiki Igarashi, Tatsuhiko Fujihira are with Fuji Electric Co., Ltd., Japan (e-mail: xdh@zju.edu.cn).

Digital Object Identifier 10.24295/CPSSTPEA.2016.00005

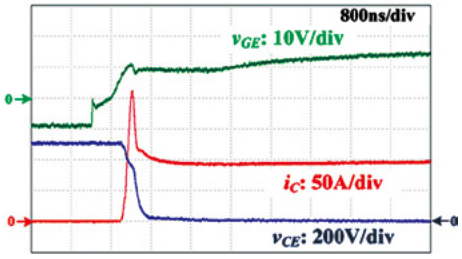
I. INTRODUCTION

HOW to reduce power semiconductor device losses seems to be a permanent topic in power electronics world. In recent years, SiC devices have attracted more and more attention due to their superior characteristics. Since the reverse recovery loss of free-wheeling diode has a big share of the total switching loss of all-Si IGBT module, hybrid IGBT modules occurs by replacing the Si free-wheeling diodes with SiC schottky barrier diodes (SiC SBDs) [1]-[3]. Hybrid IGBT module has eliminated the diode reverse recovery process so that the IGBT turn-on loss and diode reverse recovery loss are largely reduced. It is a promising solution with the optimization of both performance and cost. However, although diode reverse recovery process is eliminated by using SiC SBD, the effects caused by junction capacitance are still present. Since the drift layer of a SiC SBD is thinner than Si diode, with the same chip area, the junction capacitance of SiC SBD is larger than Si diode [4]. Due to the extremely fast recovery process of SiC SBD and the resonance between the junction capacitance of SiC

SBD and the circuit parasitic inductances, high frequency oscillation occurs during the turn-on process of hybrid IGBT module. This problem has been found by previous researchers as reported in [1]. In [5], the conducted EMI noise in a Boost converter utilizing SiC diode is evaluated. It is shown that compared to Si diode, the Boost converter with SiC SBD has larger conducted noise in the high frequency range caused by the oscillations in the SiC SBD. Fig. 1 shows the turn-on waveforms under 500 V DC bus voltage and 100 A load current. Fig. 1(a) is the result of a hybrid IGBT module while Fig. 1(b) is the result of a traditional all-Si IGBT module, where v_{CE} is the collector-emitter voltage, iC is the collector current and v_{GE} is the gate-emitter voltage, respectively. The reverse recovery current is significantly reduced in the hybrid IGBT module. However, a high frequency oscillation occurs in the collector current of IGBT during turn-on process. It may cause EMI problems affecting the operation of other systems [1].



(a)



(b)

Fig. 1. Turn-on waveforms of (a) Hybrid IGBT module and (b) All-Si IGBT module.

It is natural to consider about improving the gate driver to damp this turn-on oscillation. Previous studies have considered using active gate driver to solve the EMI issues related to *di/dt* and *dv/dt* and the current and voltage overshoots that may affect the safe operation of IGBT module [6]-[22]. Applying the active gate driver solutions, the collector current overshoot during the turn-on interval of an IGBT can be reduced by steering the current slew rate. Meanwhile, by accelerating the other stages the total turn-on time and loss would not increase significantly. In [20], a method of optimizing the gate resistance of the low side switch is proposed to accelerate the damping of the phase node ringing in a synchronous Buck converter. A simplified RLC model is developed to study the relation between the phase node ringing and circuit parasitics. In [21], a gate charge control method is studied to suppress the turn-off voltage oscillation of SiC MOSFET. However the effectiveness of active gate driver on suppressing the high frequency turn-on oscillations of hybrid IGBT modules has not been fully analytically and experimentally discussed which will be one of the purposes of this paper.

Another possible solution for the oscillations is the application of additional damping circuits. As illustrated in [23], RC and RCD snubber networks are effective in suppressing the voltage overshoot during IGBT turn-off and the diode voltage spike during IGBT turn-on (free-wheeling diode turn-off). In [24], RC snubbers are parallel connected to SiC MOSFETs to mitigate the *dv/dt* and voltage oscillation during turn-off. In [25], SiC PiN diodes are used with Si IGBTs in a Buck converter. The oscillations during diode turn-off (IGBT turn-on) are studied. To mitigate the oscillations, an RC circuit is parallel connected to the SiC PiN diode. The added capacitor charges and discharges in every switching cycle, causing a regardless amount of extra loss. In [26], methods to damp the switching oscillations of normally-off SiC JFET are studied. An RC circuit is used across the DC bus, and the values of the resistor and capacitor are experimentally adjusted to reach the most satisfied performance. In [27], SiC SBD and SiC MOSFET are used in a double pulse switching test circuit, and the turn-on and turn-off oscillations are analyzed. A similar RLC model as in [21] is derived to analyze the oscillation effects. RC snubbers are used to bring the system into overdamped condition so that oscillations can be mitigated. However, the side-effects such as the extra loss caused by the RC snubber circuit are not evaluated. It is still unclear whether the snubber circuit is effective in mitigating the turn-on oscillation of hybrid IGBT module without causing significant side-effects. Therefore, it is one of the objectives of this paper to find the appropriate structure and design of the damping circuit which can effectively suppress the turn-on oscillation of hybrid IGBT module without causing large increases in current overshoot and switching losses.

In this paper, a turn-on oscillation suppression method is proposed with combination of damping circuit and active gate driver. First to evaluate the influences of active gate driving on turn-on oscillation, different gate voltages and gate charging currents are used. It is found that by changing gate drive parameters the current overshoot can be reduced, however the duration of oscillation cannot be shortened. To accelerate the damping of turn-on oscillation, oscillation damping circuits are studied. The detailed theoretical analysis of the damping circuit is given to illustrate the optimized design of damping circuit parameters. Then the experimental results of the damping circuit are given to verify its effectiveness in accelerating the damping of turn-on oscillation and to validate the theoretical analysis. At last, to suppress the turn-on current overshoot, active gate driver method is used without largely increasing the turn-on energy loss. The combination of damping circuit and active gate driver makes it possible to simultaneously realize turn-

on current overshoot suppression and turn-on oscillation damping, which will be an optimized solution to achieve the desired low EMI performance.

II. Influences of Gate Driver on Turn-On Oscillation

To study the gate drive controllability of turn-on current oscillation in hybrid IGBT module (Fuji Electric: 400 A/1700 V, 2MSI400VE-170-50), experimental research on the influence of gate driver is carried out. Basically IGBT gate drivers can be divided into two categories: voltage source gate driver and current source gate driver. Therefore, by analyzing the performances of different voltage source and current source gate drivers, the influence of gate drive parameters on turn-on oscillation can be evaluated.

A. Voltage Source Gate Drive

First, turn-on characteristics of the hybrid IGBT module are tested using the voltage source gate driver with different positive gate drive voltages. The tests are done in a double-pulse test circuit shown in Fig. 2 with 550 V DC bus voltage and 200 A load current, the external gate resistance used is 10 Ω. In Fig. 2, V_{DC} is the DC bus voltage, I_L is the current of the load inductor at the turn-on event, i_C is the collector current of the lower arm IGBT, R_{G_ext} is the externally connected gate resistor, v_G is the gate voltage provided by the gate drive circuit and v_{GE} is the gate-emitter voltage measured at the terminals of the module. The positive gate voltage of v_G provided by the gate driver is denoted as V_+. The turn-on waveforms under different positive gate voltages (V_+) are shown in Fig. 3. The maximum oscillation current I_{OSC_MAX} and the oscillation settling time t_s are measured as shown in Fig. 4 (a) and (b). The maximum oscillation current I_{OSC_MAX} is the maximum current overshoot exceeding the load current as shown in Fig. 3. The oscillation settling time t_s, which is the time for the amplitude of oscillation current to drop from I_{OSC_MAX} to 5%•I_{OSC_MAX}, represents the duration of oscillation.

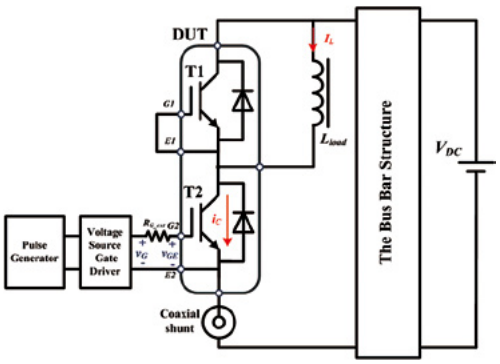


Fig. 2. Test setup for turn-on characteristics under different gate voltages.

It can be seen from the test results that when the applied gate voltage is reduced from 17 V to 11 V, the maximum oscillation current decreases from 87.3 A to 47 A, however the oscillation settling time fluctuates around 1200 ns with no clear link with the applied gate voltage.

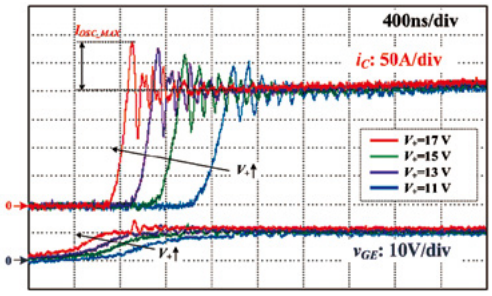


Fig. 3. Turn-on waveforms under different voltage source gate drivers.

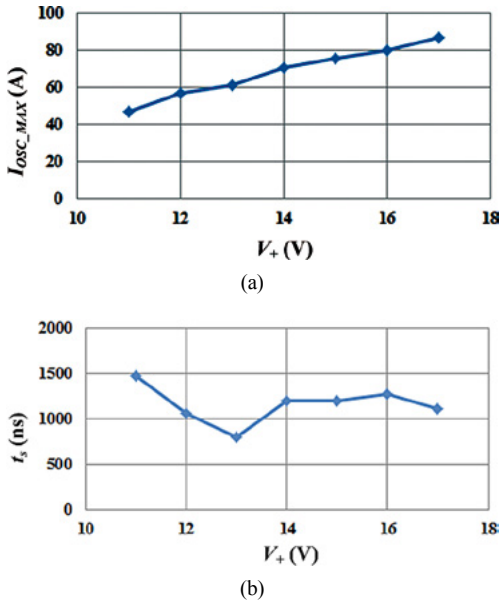


Fig. 4. Turn-on current oscillation under different gate voltages: (a) Maximum oscillation current; (b) Oscillation settling time.

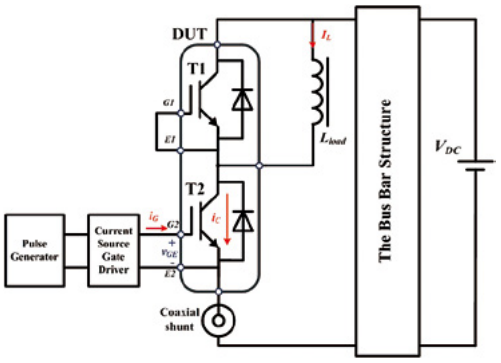


Fig. 5. Test setup for turn-on characteristics under different gate currents.

B. Current Source Gate Drive

Then a current source gate driver is used to study the turn-on characteristics under different gate charging currents. The test setup is shown in Fig. 5 with 550 V DC bus voltage and 200 A load current. In Fig. 5, i_G is the gate current provided by the current source gate driver while all the other variables

have the same definitions as in Fig. 2. During a turn-on interval, a constant gate charging current IG is provided by the current source gate driver. The turn-on waveforms under different gate charging currents (I_G) are shown in Fig. 6. Similarly, the maximum oscillation current I_{OSC_MAX} and the oscillation settling time t_s are measured as shown in Fig. 7 (a) and (b).

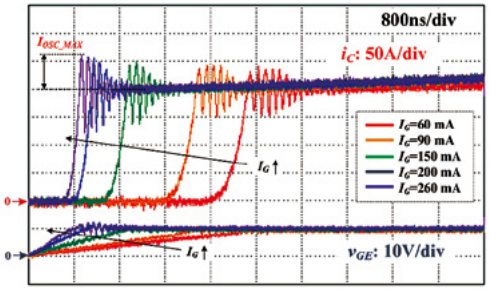
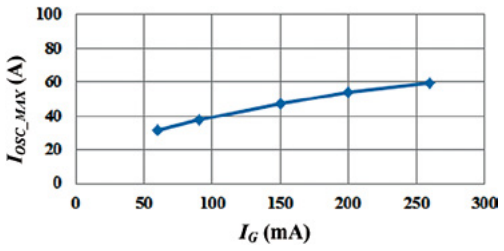
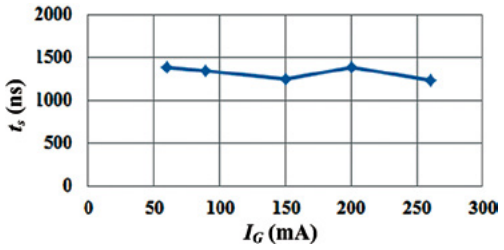


Fig. 6. Turn-on waveforms under different current source gate drivers.



(a)



(b)

Fig. 7. Turn-on current oscillation under different gate currents: (a) Maximum oscillation current; (b) Oscillation settling time.

It can be seen that when the gate charging current changes from 260 mA to 60 mA, the maximum oscillation current decreases from 59.3 A to 31.7 A, however the oscillation settling time fluctuates around 1200 ns and does not have a clear relation with the gate charging current.

To sum up, by lowering the gate voltage and reducing gate charging current, the maximum oscillation current can be mitigated but the switching speed will be reduced and the on-state voltage drop will increase, thus causing increase in switching and conduction losses. Moreover, the attenuation of the oscillation cannot be accelerated by changing the gate drive parameters alone. Therefore, lowering gate voltage and reducing gate charge current are not the recommended methods to suppress turn-on oscillation. To accelerate the damping of turn-on oscillation, further countermeasures should be taken.

III. Turn-On Oscillation Suppression with Damping Circuit

A. Theoretical Analysis of Turn-on Oscillation

To accelerate the damping of turn-on oscillation, the utilization of additional damping circuits is investigated. To have a better understanding of turn-on oscillation, first the theoretical analysis of the oscillation is carried out to reveal the relation between turn-on oscillation and circuit parasitics. The inductive switching test circuit is shown in Fig. 8 where the lower arm IGBT is switching and the upper arm SiC SBD is the free-wheeling diode. As depicted in Fig. 8, L_p represents the stray inductance of the DC bus, R_p stands for the parasitic resistance of the commutation loop, L_{1C}, L_{1eE}, L_{1E}, L_{2C}, L_{2eE}, L_{2E} are the stray inductances in the hybrid IGBT module, C_{CE1} and C_{CE2} are the combination of the collector-emitter capacitance of the IGBT and the junction capacitance of the anti-parallel SiC SBD, C_{GE1}, C_{CG1}, C_{GE2}, C_{CG2} are the gate-emitter and collector-gate capacitances of the IGBT, Rg,ext and Rg,int are the external and internal gate resistors of the IGBT respectively. In the figure, V_{DC} is the DC bus voltage, I_L is the load current, i_{dc} is the DC bus current, i_{C1} and i_{C2} are the collector currents of the upper arm and lower arm devices respectively, v_{CE1} and v_{CE2} are the collector-emitter voltages of upper arm and lower arm devices respectively, and v_{GE2}, v_{CG2}, i_{G2} are the gate-emitter voltage, collector-gate voltage and the gate current of the lower arm IGBT.

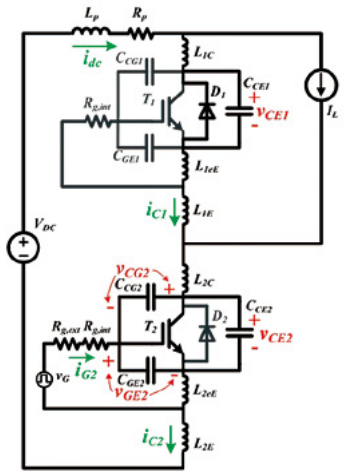


Fig. 8. Inductive switching circuit of hybrid IGBT module

The conceptual waveforms of a turn-on event of the lower arm IGBT T2 are shown in Fig. 9, where $V_{GE,\text{th}}$ is the gate threshold voltage, $V_{GE,\text{miller}}$ is the miller plateau voltage.

The parasitic capacitances of the IGBT are highly non-linear depending on the collector-emitter voltage. To simplify the analysis, the similar approximation as in [28] is adopted that the capacitances are approximated as two discrete values in different operating regions. The output characteristic of

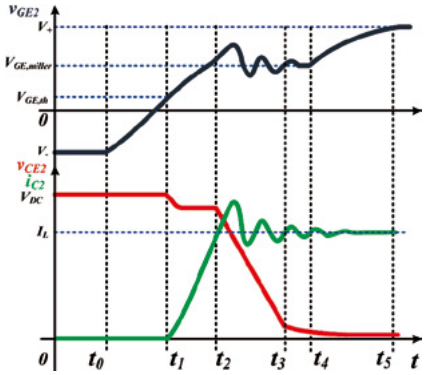


Fig. 9. Conceptual turn-on waveforms of the hybrid IGBT module.

the IGBT can be divided into three regions: cut-off region, linear region and saturation region. The capacitances in each operating region are shown in TABLE I where $C_{CE,L} << C_{CE,H}$ and $C_{CG,L} << C_{CG,H}$.

TABLE I
OPERATING REGIONS AND PARASITIC CAPACITANCES OF THE IGBT

Time interval	t_0~t_1	t_1~t_2	t_2~t_3	t_3~t_4	t_4~t_5
Operating region of T2	Cut-off	Linear	Linear	Linear	Saturation
$\boldsymbol{C_{CE2}}$	$C_{CE,L}$	$C_{CE,L}$	$C_{CE,L}$	$C_{CE,H}$	$C_{CE,H}$
$\boldsymbol{C_{CG2}}$	$C_{CG,L}$	$C_{CG,L}$	$C_{CG,L}$	$C_{CG,H}$	$C_{CG,H}$
$\boldsymbol{C_{CE1}}$	$C_{CE,H}$	$C_{CE,H}$	$C_{CE,H}$	$C_{CE,L}$	$C_{CE,L}$

As shown in Fig. 9, the turn-on interval can be roughly divided into five stages:

● Stage 1 (t_0~t_1): turn-on delay time

Gate-emitter voltage v_{GE2} rises from the negative gate potential V- and reaches the threshold voltage $V_{GE,th}$ at t_1. The IGBT operates in cut-off region in this stage.

● Stage 2 (t_1~t_2): collector current rising stage

After t_1, the collector current i_{C2} begins to rise and reaches the load current I_L at t_2. The IGBT operates in linear region in this stage.

● Stage 3 (t_2~t_3): collector-emitter voltage dropping stage 1

After t_2, the upper arm diode begins to take up voltage, and the collector-emitter voltage of the lower arm IGBT v_{CE2} begins to drop at a high slew rate and reaches a certain level at t_3. The IGBT operates in linear region in this stage.

The value of the collector-emitter voltage at the stage transition needs some more insight into the device physical model, as discussed in [29]. Since the physical modeling of IGBT is not the focus of this study, the value of v_{CE2} at stage transition is approximated from the test waveforms.

● Stage 4 (t_3~t_4): collector-emitter voltage dropping stage 2

After t_3, the collector-gate capacitance C_{CG} of the IGBT increases to a much larger value so the slew rate of v_{CE2} decreases dramatically. At t_4, v_{CE2} drops to the on-state voltage, and the IGBT enters saturation region. The IGBT operates in linear region in this stage.

For the sake of simplicity, the on-state voltage drop is approximated as 0 in this analysis.

● Stage 5 (t_4~t_5): gate-emitter voltage rises to positive supply voltage

After t_4, the gate-emitter voltage v_{GE2} starts to rise again and reaches the positive gate potential V_+ at t_5. The IGBT operates in saturation region in this stage.

The detailed analytical expressions of each stage are presented as follows.

Stage 1 (t_0~t_1) - turn-on delay time:

At t_0, the voltage v_G provided by the gate driver jumps from V_- to V_+. The input capacitance starts to charge up. The gate-emitter voltage v_{GE2} in this stage can be expressed as:

$$v_{GE2}(t) = V_+ \cdot \left[1 - e^{-(t-t_0)/\tau_{ies}}\right] - V_- \tag{1}$$

where $\tau_{ies}=R_g\cdot(C_{GE2}+C_{CG2})=R_g\cdot(C_{GE}+C_{CG,L})$, $R_g=R_{g,ext}+R_{g,int}$.

In this stage, the collector current i_{C2} remains at 0, and the collector-emitter voltage v_{CE2} remains at V_{DC}. At t_1, v_{GE} reaches V_{GE},th and the IGBT enters Stage 2.

Stage 2 (t_1~t_2) - collector current rising:

In this stage, the collector current i_{C2} begins to rise. Free-wheeling diode D1 still conducts part of the load current, so the voltage v_{CE1} remains at 0 in this stage.

The initial conditions of this stage are listed below:

$$\begin{cases} i_{C2}(t_1) = 0 \\ v_{GE2}(t_1) = V_{GE,th} \\ v_{CE2}(t_1) = V_{DC} \end{cases} \tag{2}$$

As the IGBT is operating in the linear region, the collector current can be expressed with the following equation:

$$i_{C2}(t) = g_{fe}\left[v_{GE2}(t) - V_{GE,th}\right] \tag{3}$$

where gfe is the transconductance of the IGBT. Note that in this stage the collector-emitter voltage is not changing abruptly, thus the current flowing through the output capacitance is neglected in equation (3).

For the gate loop, the following equations can be derived:

$$R_g \cdot i_{G2}(t) = V_+ - v_{GE2}(t) - L_{eE2}\frac{di_{C2}(t)}{dt} \tag{4}$$

$$i_{G2}(t) = C_{GE}\frac{dv_{GE2}(t)}{dt} - C_{CG,L}\frac{dv_{CG2}(t)}{dt} \tag{5}$$

$$v_{GE2}(t) = v_{CE2}(t) - v_{CG2}(t) \tag{6}$$

For the main power loop, the following equation can be obtained:

$$V_{DC} = (L_p + L_m)\frac{di_{C2}(t)}{dt} + R_p \cdot i_{C2}(t) + v_{CE2}(t) \tag{7}$$

where L_m(=L_{1C}+L_{1eE}+L_{1E}+L_{2C}+L_{2eE}+L_{2E}) represents the stray inductance within the hybrid module.

Combining equations (3)-(7), $i_{C2}(t_2)$, $v_{GE2}(t_2)$ and $v_{CE2}(t_2)$ can be derived which are the initial conditions of the next stage.

Stage 3 (t_2~t_3) – collector-emitter voltage dropping 1:

When the collector current i_{C2} reaches the load current I_L at t_2 shown in Fig. 9, the upper arm diode D1 starts to take up voltage, so the collector-emitter voltage of the lower arm IGBT v_{CE2} begins to drop, and the collector current starts to oscillate.

The initial conditions of this stage are listed as below:

$$\begin{cases} i_{C2}(t_2) = I_L \\ v_{GE2}(t_2) = I_L / g_{fe} + V_{GE,th} \\ v_{CE2}(t_2) \quad \text{derived from the last stage} \\ v_{CE1}(t_2) = 0 \end{cases} \tag{8}$$

For the main power loop, the following equations can be derived:

$$V_{DC} = L_p \frac{di_{dc}(t)}{dt} + R_p i_{dc}(t) + (L_{1C} + L_{1E} + L_{1eE}) \frac{di_{C1}(t)}{dt} + v_{CE1}(t) + (L_{2C} + L_{2E} + L_{2eE}) \frac{di_{C2}(t)}{dt} + v_{CE2}(t) \tag{9}$$

$$i_{dc}(t) = i_{C2}(t) \tag{10}$$

$$i_{C1}(t) = i_{C2}(t) - I_L \tag{11}$$

Combining with equations (10) and (11), equation (9) can be simplified as:

$$V_{DC} = (L_p + L_m) \frac{di_{C2}(t)}{dt} + R_p i_{C2}(t) + v_{CE1}(t) + v_{CE2}(t) \tag{12}$$

For the upper arm IGBT T1, the following equation can be obtained:

$$C_{CE,H} \frac{dv_{CE1}(t)}{dt} = i_{C1}(t) = i_{C2}(t) - I_L \tag{13}$$

For the gate loop, equations (4)-(6) are still valid in this stage. Since the collector-emitter voltage drops rapidly in this stage, the current flowing through the output capacitance of the IGBT cannot be neglected. Therefore, equation (3) has to be modified as the following equation:

$$i_{C2}(t) = g_{fe}\left[v_{GE2}(t) - V_{GE,th}\right] + C_{CE,L} \cdot \frac{dv_{CE2}(t)}{dt} + C_{CG,L} \cdot \frac{dv_{CG2}(t)}{dt} \tag{14}$$

Combining equations (4)-(6) and (12)-(14), the current and voltages of this stage can be derived. As mentioned before, the value of v_{CE2} at stage transition is approximated from the test waveforms. When v_{CE2} drops to the transition voltage, the IGBT enters the next stage.

Stage 4 (t_3~t_4) – collector-emitter voltage dropping 2:

The initial conditions ($i_{C2}(t_3)$, $v_{GE2}(t_3)$, $v_{CE1}(t_3)$ and $v_{CE2}(t_3)$) of this stage can be obtained by solving the equations describing the last stage. Since the circuit status in this stage is the same as last stage, equations (4)-(6) and (12)-(14) are still valid in this stage with only the changes in parasitic capacitances. The capacitances in (5) and (14) change from $C_{CE,L}$, $C_{CG,L}$ to $C_{CE,H}$, $C_{CG,H}$. The capacitance in (13) changes from $C_{CE,H}$ to $C_{CE,L}$.

At t_4, the collector-emitter voltage v_{CE2} drops to the on-state voltage, and the IGBT enters the saturation region. For the sake of simplicity, the on-state voltage drop is approximated as 0 in this analysis.

Stage 5 (t_4~t_5) – gate-emitter voltage rises to positive supply voltage:

After t_5, the IGBT enters saturation region. The gate-emitter voltage begins to charge up again, and reaches the positive gate potential V_+ at the end of this stage.

Equation (14) is no longer valid in this stage since the IGBT enters the saturation region. While all the other equations describing the last stage can still be used in this stage.

According to the device datasheet and some preliminary test waveforms, the parasitic parameters of the module are estimated as L_m=15 nH, L_{eE}=1 nH, C_{GE}=15 nF, $C_{CG,L}$=0.05 nF, $C_{CG,H}$=9 nF, R_p=0.4 Ω, g_{fe}=200. In the calculations, the DC bus voltage is V_{DC}=550 V, the load current is I_L=200 A, the positive gate voltage is V_+=15 V and the gate resistance used is R_g=$R_{g,int}$+$R_{g,ext}$=15 Ω. For the sake of simplicity, the collector-emitter capacitance of the IGBT in combination with the junction capacitance of SiC SBD is approximated as a constant value C_{CE}.

The maximum oscillation current I_{OSC_MAX} and oscillation settling time ts under different DC bus stray inductance L_p and device parasitic capacitance C_{CE} are calculated using the equations given above and the results are shown in Fig. 10 (a) and (b) respectively.

As shown in Fig. 10, with the increase of DC bus stray inductance, both the maximum oscillation current and oscillation settling time increases significantly. At a fixed stray inductance, with the increase of parasitic capacitance C_{CE}, the maximum oscillation current increases rapidly while the changes in the settling time of oscillation is not significant.

To evaluate the accuracy of the calculations, as shown in Fig. 11, the calculated maximum oscillation current and oscillation settling time are depicted alongside the tested results shown in Fig. 4 (a) and (b). Different positive gate potentials are used, and the parasitics parameters used for the calculations are: L_p=70 nH and C_{CE}=6 nF.

As shown in Fig. 11, the analytical model introduced in this paper is able to provide a relatively accurate estimation of turn-on oscillation of hybrid IGBT modules.

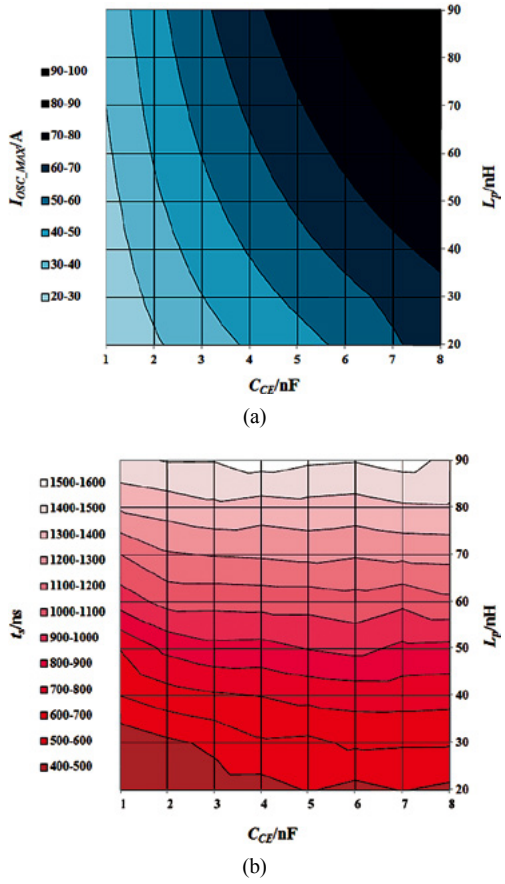


Fig. 10. Calculated results of current oscillation under different circuit parasitics: (a) Maximum oscillation current; (b) Oscillation settling time.

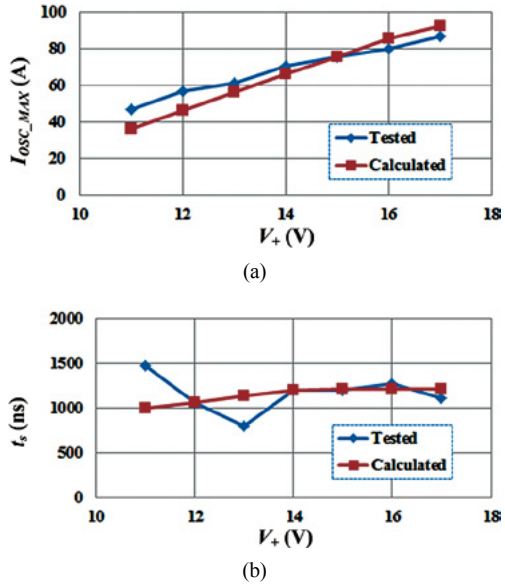


Fig. 11. Comparison between the calculated and tested current oscillation characteristics under different gate voltages:
(a) Maximum oscillation current; (b) Oscillation settling time.

Note from Fig. 11 (b) that some deviations from the theoretical values are present in the experimental oscillation settling time characteristics. The noise and inaccuracy in the test system may be the cause of the fluctuations in the test results. The deviations from the theoretical values are in the range of several hundred nanoseconds which is just a few oscillation cycles. However, the trend in the figure still shows that the oscillation settling time is not clearly relevant with the gate voltage. Therefore, the faster attenuation of turn-on oscillation cannot be achieved by modifying the gate driver alone.

B. Theoretical Analysis of Damping Circuit

RC and RCD networks have previously been used on Si and SiC power devices to mitigate the turn-off voltage overshoot and oscillations caused by circuit parasitics [23]-[27], [30]-[33]. The RC damping circuit may also be able to mitigate the turn-on current oscillations of hybrid IGBT module. However, since the primary purpose of the damping circuit is to mitigate the turn-on oscillation, the design and working principles of the damping circuit is different from the snubber circuit which is primarily aimed at suppressing the turn-off voltage overshoot. Two typical damping circuits are shown in Fig. 12 (a) and (b) respectively.

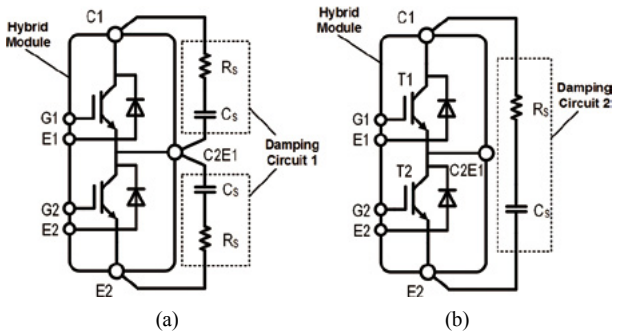


Fig. 12. Typical damping circuit topologies: (a) Damping circuit 1; (b) Damping circuit 2.

The damping circuit provides a conducting path for high frequency currents during the turn-on process, and the damping resistor damps the high frequency components of the current. The damping capacitor and resistor should be carefully chosen to achieve the best trade-off between oscillation damping and extra energy loss caused in the damping circuit.

A theoretical analysis is conducted for damping circuit 2 to illustrate the influence of damping circuit parameters on the performance of oscillation damping and additional switching loss. The inductive switching test circuit with the application of damping circuit is shown in Fig. 13. The damping circuit should be placed closely to the module and the connections are kept as short as possible to minimize the loop stray inductance, thus, for the sake of simplicity, the stray inductance of the damping circuit is not included in the circuit diagram.

The conceptual waveforms and the stages of the turn-on interval are the same as demonstrated in the last section, which will not be repeated here. The detailed analytical

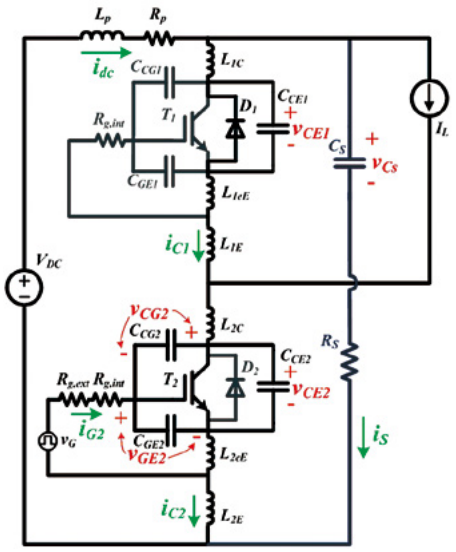


Fig. 13. Inductive switching circuit of hybrid IGBT module with damping circuit.

expressions of each stage with the presence of damping circuit are presented as follows.

Stage 1 (t_0~t_1) – turn-on delay time:

The expressions of this stage are the same with those without damping circuit and will not be repeated here.

Stage 2 (t_1~t_2) – collector current rising:

The initial conditions of this stage are listed below:

$$\begin{cases} i_{C2}(t_1)=0 \\ v_{GE2}(t_1)=V_{GE,th} \\ v_{CE2}(t_1)=V_{DC} \\ v_{Cs}(t_1)=V_{DC} \\ i_{dc}(t_1)=0 \end{cases} \tag{15}$$

For the gate loop, equations (3)-(6) are still valid with the presence of damping circuit.

For the main power loop, the following equations can be derived:

$$V_{DC}=L_m\frac{di_{C2}(t)}{dt}+L_p\frac{di_{dc}(t)}{dt}+R_p\cdot i_{dc}(t)+v_{CE2}(t) \tag{16}$$

$$V_{DC}=v_{Cs}(t)+R_SC_S\frac{dv_{Cs}(t)}{dt}+L_p\frac{di_{dc}(t)}{dt}+R_pi_{dc}(t) \tag{17}$$

$$i_{dc}(t)=i_{C2}(t)+C_S\frac{dv_{Cs}}{dt} \tag{18}$$

Solving equations (3)-(6) and (16)-(18), $i_{C2}(t_2)$, $v_{GE2}(t_2)$, $v_{CE2}(t_2)$, $v_{Cs}(t_2)$ and $i_{dc}(t_2)$ can be derived which are the initial conditions of the next stage.

Stage 3 (t_2~t_3) – collector-emitter voltage dropping 1:

The initial conditions of this stage are listed as below:

$$\begin{cases} i_{C2}(t_2)=I_L \\ v_{GE2}(t_2)=I_L/g_{fe}+V_{GE,th} \\ v_{CE1}(t_2)=0 \\ v_{CE2}(t_2) \quad \text{derived from the last stage} \\ v_{Cs}(t_2) \quad \text{derived from the last stage} \\ i_{dc}(t_2) \quad \text{derived from the last stage} \end{cases} \tag{19}$$

For the main power loop, equations (17) and (18) are still valid in this stage, while equation (16) should be modified as:

$$V_{DC}=L_m\frac{di_{C2}(t)}{dt}+L_p\frac{di_{dc}(t)}{dt}+ R_p\cdot i_{dc}(t)+v_{CE1}(t)+v_{CE2}(t) \tag{20}$$

For the upper arm IGBT T1, equation (13) still holds with the presence of damping circuit.

For the gate loop, equations (4)-(6) and (14) can still be used here.

Combining equations (4)-(6), (13), (14) and (20), the current and voltages of this stage can be derived. When the collector-emitter voltage drops to a certain level, the IGBT enters the next stage.

Stage 4 (t_3~t_4) – collector-emitter voltage dropping 2:

The initial conditions ($i_{C2}(t_3)$, $v_{GE2}(t_3)$, $v_{CE1}(t_3)$, $v_{CE2}(t_3)$, $v_{Cs}(t_2)$ and $i_{dc}(t_2)$) of this stage can be obtained by solving the equations describing the last stage. Since the circuit status is the same as last stage, equations (4)-(6), (13), (14) and (20) are still valid in this stage with only the changes in parasitic capacitances. The capacitances in (5) and (14) changes from $C_{CE,L}$, $C_{CG,L}$ to $C_{CE,H}$, $C_{CG,H}$, respectively. The capacitance in (13) changes from $C_{CE,H}$ to $C_{CE,L}$.

Stage 5 (t_4~t_5) – gate-emitter voltage rises to positive supply voltage:

After t_5, the IGBT enters saturation region. The gate-emitter voltage begins to charge up again, and reaches the positive gate potential V_+ at the end of this stage.

Equation (14) is no longer valid in this stage since the IGBT enters the saturation region. While all the other equations describing the last stage can still be used in this stage.

According to the device datasheet and preliminary test results, the parasitic parameters of the module and the test circuit are estimated as: L_p=70 nH, L_m=15 nH, L_{eE}=1 nH, C_{GE}=15 nF, $C_{CG,L}$=0.05 nF, $C_{CG,H}$=9 nF, C_{CE}= 6nF R_p=0.4 Ω, g_{fe}=200. In the calculations, the DC bus voltage is V_{DC}=550 V, the load current is I_L=200 A, the positive gate voltage is V_+=14 V and the gate resistance used is R_g=$R_{g,int}$+$R_{g,ext}$=15 Ω.

The maximum oscillation current I_{OSC_MAX} and oscillation settling time ts are the most concerned parameters of the oscillation. The calculated maximum oscillation current I_{OSC_MAX} and oscillation settling time ts under different damping resistors and damping capacitors are shown in Fig. 14 (a) and (b) respectively. The additional energy loss caused in the damping resistor during a turn-on event is also calculated,

as shown in Fig. 14 (c). To evaluate the loss in the damping resistor during turn-off of the IGBT, a similar analysis of the turn-off interval is carried out as well, and the calculated damping resistor loss during a turn-off event is shown in Fig. 14 (d).

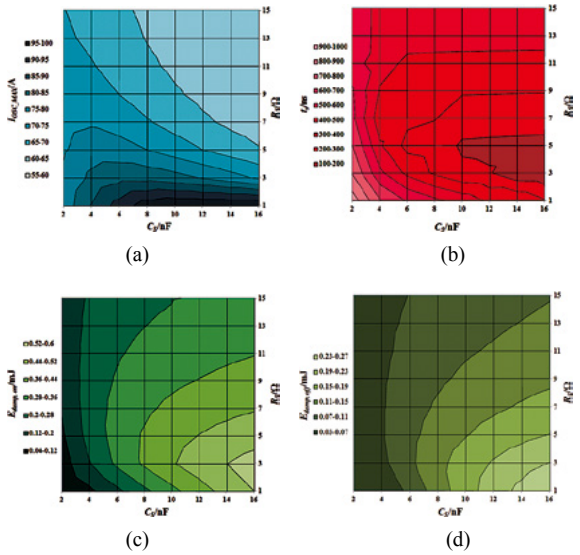


Fig. 14. Calculated results under different damping circuit parameters: (a) Maximum oscillation current; (b) Oscillation settling time; (c) Energy loss in the damping resistor during turn-on; (d) Energy loss in the damping resistor during turn-off.

It can be seen from the calculation results that the maximum oscillation current decreases with increasing C_S and R_S, however when R_S is larger than 5 Ω, the maximum oscillation current is only slightly influenced by C_S and R_S. The oscillation settling time represents the time for the damping circuit to attenuate the oscillation. The minimum value of oscillation settling time t_s occurs when C_S=10~16 nF, and R_S=3~5 Ω under the given conditions. The additional energy loss in the damping resistor increases with larger damping capacitor C_S, however both the additional energy losses during turn-on and turn-off remain small (<0.5 mJ) in the whole range of C_S and R_S.

If the damping resistor and capacitor are chosen as R_S=10 Ω and C_S=10 nF, the oscillation currents with and without damping circuit can be depicted by performing the analysis above, as shown in Fig. 15. Fig. 15 (a) presents the calculated results while Fig. 15 (b) shows the experimental results under the same conditions. It can be seen that by applying the damping circuit, the oscillation settling time is largely reduced, thus the attenuation of current oscillation can be accelerated by the damping circuit.

The calculated waveforms of gate-emitter voltages of the IGBT during the turn-on event with and without damping circuit are shown in Fig. 16. As shown in the figure, because of the transconductance and common emitter inductance L_{eE2}, the oscillations in collector current cause oscillation in the gate-emitter voltage. By introducing the damping circuit, the oscillation in gate-emitter voltage is mitigated as well.

The theoretical analysis of the damping circuit is helpful to

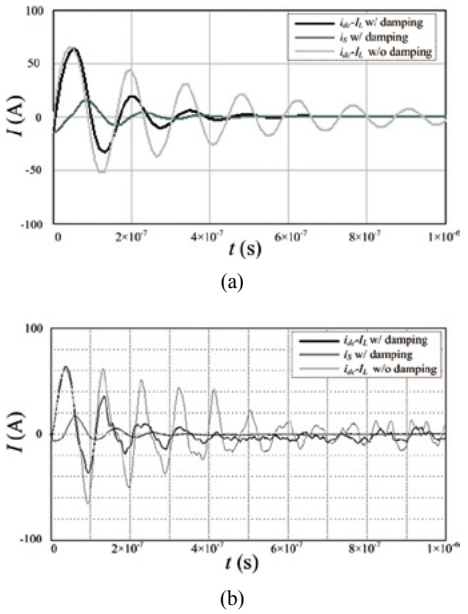


Fig. 15. Calculated (a) and tested (b) waveforms of current oscillation with and without damping.

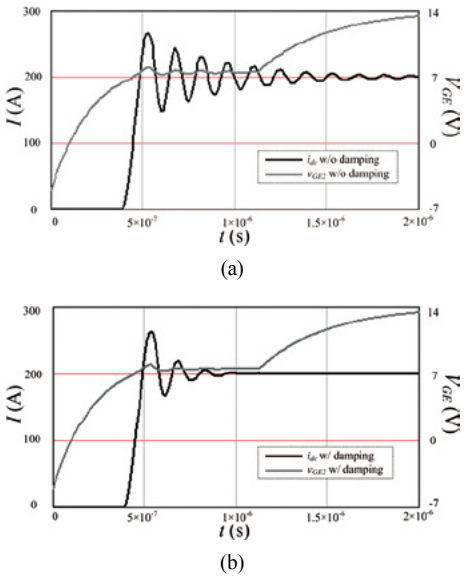


Fig. 16. Calculated waveforms of gate-emitter voltage and DC bus current: (a) without damping; (b) with damping.

determine the range of the resistance and capacitance for the damping circuit. It should be noted that the analytical model introduced in this paper is largely dependent on the parasitic elements of the module and the test circuit. The parasitic capacitances of the devices are especially critical because the variations in these capacitances may largely affect the calculation results. The parasitic capacitances are strongly non-linear components and sometimes may not be obtained from the device datasheet. Therefore, further experimental adjustment of the damping resistor and capacitor is still necessary since the values of parasitic components used in the theoretical estimation may differ from the actual values in the experiment system.

C. Difference between the Designs of Damping Circuit and Snubber Circuits

To overcome the turn-off over-voltage caused by the loop inductance, several variations of snubber circuits are investigated in the literature [32], [33]. The typical topologies of snubber circuits and the damping circuit are shown in Fig. 17, where LS is the stray inductance of the commutation loop, C_{CE1} and C_{CE2} are the parasitic capacitances of the switching devices. In the figures, the parastic components that each circuit is mainly dealing with are highlighted.

The discharge suppressing RCD snubber shown in Fig. 17 (c) and the decoupling capacitor (C snubber) shown in Fig. 17 (d) are the most commonly used snubber circuits for IGBT modules [32], [33]. The snubber circuit is aimed to suppress the turn-off voltage spike, thus the snubber capacitance C_{Sn} is designed to absorb the energy stored in the loop stray inductance LS during the conduction state of the IGBT. The snubber capacitor should be of high frequency type with low ESR and ESL. As reported in [23], the discharge suppressing RCD snubber shown in Fig. 17 (c) is also able to suppress the turn-on oscillations caused by the reverse recovery of the Si free-wheeling diode. However, since suppressing turn-on oscillation is not the primary purpose of snubber circuit, the designs of the capacitance and resistance are not optimized for turn-on oscillation suppression. While on the other hand, the damping circuit for Hybrid IGBT is dedicated to attenuating the turn-on current oscillation. During turn-on process, the damping circuit is used to damp the oscillation between the loop stray inductance LS and the parasitic capacitances of the switching devices C_{CE1} and C_{CE2}. The damping circuit provides a conducting path for high frequency currents. Part of the high frequency currents flowing through the parasitic capacitors of the switching devices are directed to the damping circuit and dampened by the damping resistor.

There are many references concerning the design of snubber circuits to mitigate the turn-off voltage spike and voltage oscillation [23],[30],[31]. The capacitance of the

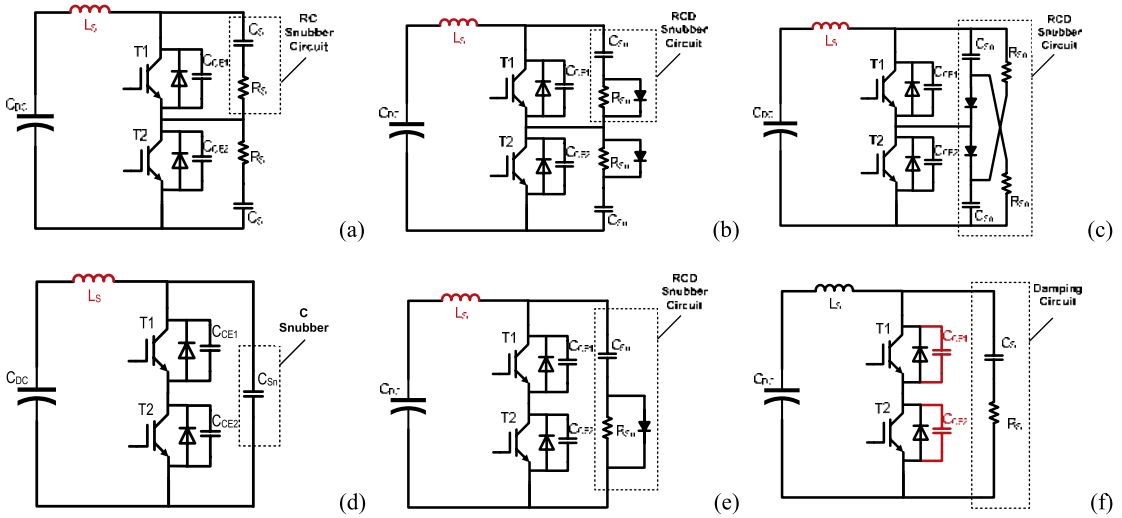


Fig. 17. Typical topologies of snubber circuits and the damping circuit

snubber capacitor CSn can be estimated by the following equation [23]:

$$C_{Sn} = L_S \cdot I_L^2 \Big/ \left(V_{pk} - V_{DC}\right)^2 \tag{21}$$

where V_{pk} is the desired peak voltage during turn-off. Applying the same conditions used in the analysis of damping circuit, i.e. L_S=75 nH, I_L=200 A, and the allowable voltage overshoot is set to 100 V, it can be estimated that the snubber capacitor is C_{Sn}=300 nF.

During turn-on interval of the IGBT, as the IGBT current rises with a slew rate of d*i*/d*t*, the voltage induced on the loop stray inductance L_S causes the voltage across the positive and negative terminals of the module to drop by L_S•di/dt while the snubber capacitors are charged to the DC bus voltage VDC, thus the diodes of the RCD snubber is reverse biased, yielding a turn-on equivalent circuit of the RCD snubber shown in Fig. 18 (a) which can be further simplified as Fig. 18 (b).

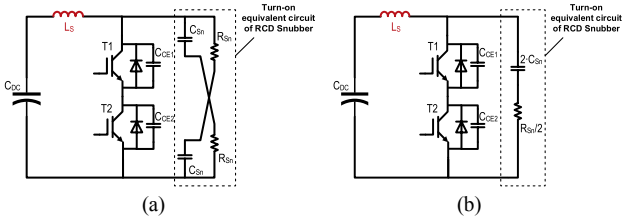
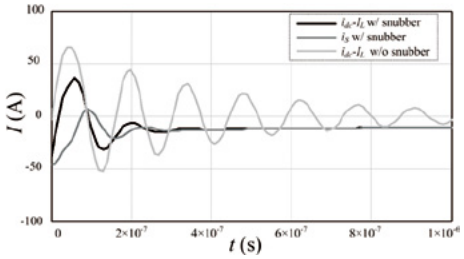


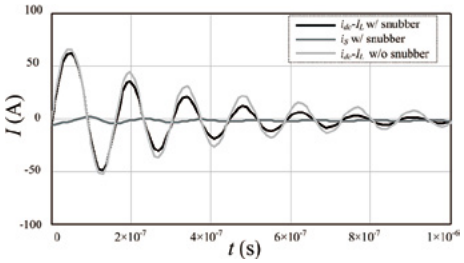
Fig. 18. The equivalent circuit of RCD snubber during IGBT turn-on.

As shown in Fig. 18 (b), the equivalent circuit of RCD snubber at turn-on has the same structure as the damping circuit. However, since the snubber circuit is used to mitigate voltage spikes, the capacitance is much larger than that of the damping circuit. In the turn-on equivalent circuit of RCD snubber, the capacitance is 2•C_{Sn}=600 nF which may largely increase the loss in the resistor. By performing the same analysis procedure of the damping circuits, the turn-

on current waveforms with snubber circuit can be derived as well. As shown in Fig. 19 (a), if a small value of 5 Ω is chosen for the snubber resistor, the snubber circuit has some ability of mitigating the turn-on oscillation, however the loss in the snubber resistor is 2.29 mJ for a turn-on event, much larger than the damping circuit (<0.5 mJ). If the snubber resistor uses a large value to reduce the losses, as shown in Fig. 19 (b) where the snubber resistor is set to 50 Ω, the loss in the snubber resistor is reduced to 0.71 mJ at the cost of losing the oscillation damping capability.



(a)



(b)

Fig. 19. Calculated turn-on waveforms with snubber circuit: (a) RSn=5 Ω; (b) RSn=50 Ω.

Therefore, by using the conventional snubber circuit design for turn-off over-voltage suppression, the features of effective turn-on oscillation damping and low loss in the snubber resistor cannot be achieved simultaneously. It might be a better solution to combine the decoupling capacitor (C snubber) and the damping circuit, as shown in Fig. 20. A large decoupling capacitor can be used to mitigate the turn-off voltage spike caused by loop stray inductance L_S, and the design of damping circuit can be implemented to mitigate the turn-on oscillation caused by the resonance between the loop stray inductance L_S and the parasitic capacitances of the switching devices C_{CE1} and C_{CE2}.

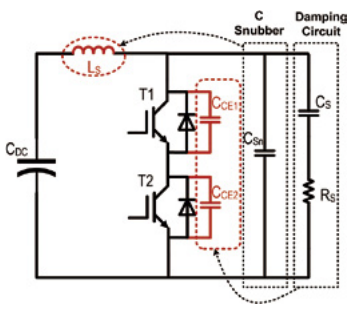


Fig. 20. Combining decoupling capacitor (C snubber) and RC damping circuit to suppress both the current oscillation at turn-on and voltage overshoot at turn-off

D. Experiment Results of Damping Circuit

The test setup for damping circuit 2 is the same as the test circuit shown in Fig. 2 where the RC damping circuit is connected across the phase leg. Different RC values for the damping circuit are tested to determine the optimized parameters for the suppression of turn-on oscillations. The tests are carried out under 550 V DC bus voltage and 200 A load current, the positive gate voltage provided by the voltage source gate driver is V_+=14 V, the external gate resistor is R_{G_ext}=10 Ω.

To minimize the parasitic inductance of the damping circuit and to simplify the mounting of damping circuit on the hybrid IGBT module, a damping circuit board is made as shown in Fig. 21. In this way, the connection between the damping circuit and the hybrid IGBT module can be minimized. In order not to affect the low inductance connection between the damping circuit and the hybrid module, only the DC bus current idc are measured in the experiments.

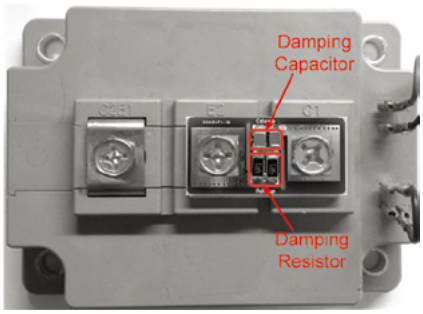


Fig. 21. The mounting of damping circuit on the hybrid IGBT module.

The first step is to keep the damping resistance at R_S=5 Ω, and the damping capacitance is set to C_S=2.2 nF, 4.4 nF, 6.6 nF, 8.8 nF, 11 nF and 13.2 nF respectively. The maximum oscillation current I_{OSC_MAX}, the oscillation settling time ts and the additional damping resistor energy losses during turn-on and turn-off ($E_{damp,\ on}$ and $E_{damp,\ off}$) with different damping capacitors are shown in Fig. 22. To evaluate the error between the calculations and the experimental results, the calculated and tested results are depicted in the same figures.

Fig. 22 illustrates that the damping circuit is effective in suppressing the turn-on oscillation. By using the damping circuit, the oscillation settling time is largely reduced while around 10 A over-current is added to the maximum oscillation current. The additional damping resistor loss increases with increasing damping capacitor, which is in good match with the theoretical analysis. The additional damping resistor loss is relatively small compared to the turn-on loss of the IGBT which is 24.1 mJ under the given conditions, thus no significant loss increase is introduced.

As can be seen from Fig. 22, when C_S=11 nF, the damping circuit has the best balance between oscillation suppression and unwanted side-effects.

The next step is to fix the damping capacitance at 11 nF, and the damping resistance is chosen as RS=0.8 Ω, 1.1

Ω, 1.7 Ω, 2.5 Ω, 3.3 Ω, 5 Ω, 6.8 Ω and 10 Ω respectively. Fig. 23 shows the maximum oscillation current I_{OSC_MAX}, the oscillation settling time ts and the additional damping resistor energy losses $E_{damp,\ on}$ and $E_{damp,\ off}$ with different damping resistors. Again, the calculated and experimental results are depicted in the same figures.

It can be seen from the test results that the best balance between oscillation suppression and side-effects is achieved when R_S=2.5~3.3 Ω. Finally, R_S=2.5 Ω is chosen. Therefore, the optimized parameters for the damping circuit are: C_S=11 nF and R_S=2.5 Ω.

Note that in Fig. 22 and Fig. 23, the tested and calculated results bare the same trends. The calculated maximum oscillation current and oscillation settling time are very close to the experimental values. Therefore, the theoretical analysis introduced in this paper is able to provide a good estimation of the turn-on oscillations.

The same experiment procedure is also performed for damping circuit 1, and the achieved optimal parameters of damping circuit 1 are C_S=5.2 nF and R_S=6.8 Ω.

The waveforms of the DC bus current i_{dc} and the collector-emitter voltage of the upper arm IGBT v_{CE1} in a turn-on event of the lower arm IGBT with and without the damping circuits are shown in Fig. 24. The performances of oscillation suppression and side-effects of the damping circuits are listed in Fig. 25 alongside each other. It should be noted that the turn-on energy losses E_{on} listed in Fig. 25 also include the additional energy loss of the damping resistor.

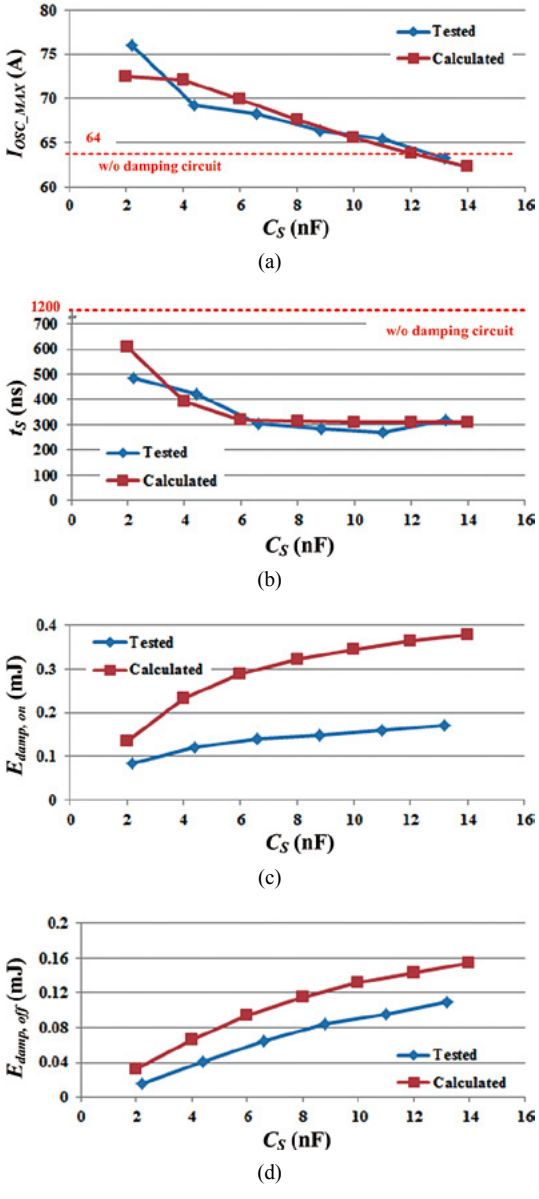


Fig. 22. Turn-on oscillation using damping circuit with different damping capacitors:
(a) Maximum oscillation current; (b) Oscillation settling time;
(c) Energy loss in the damping resistor during turn-on; (d) Energy loss in the damping resistor during turn-off.

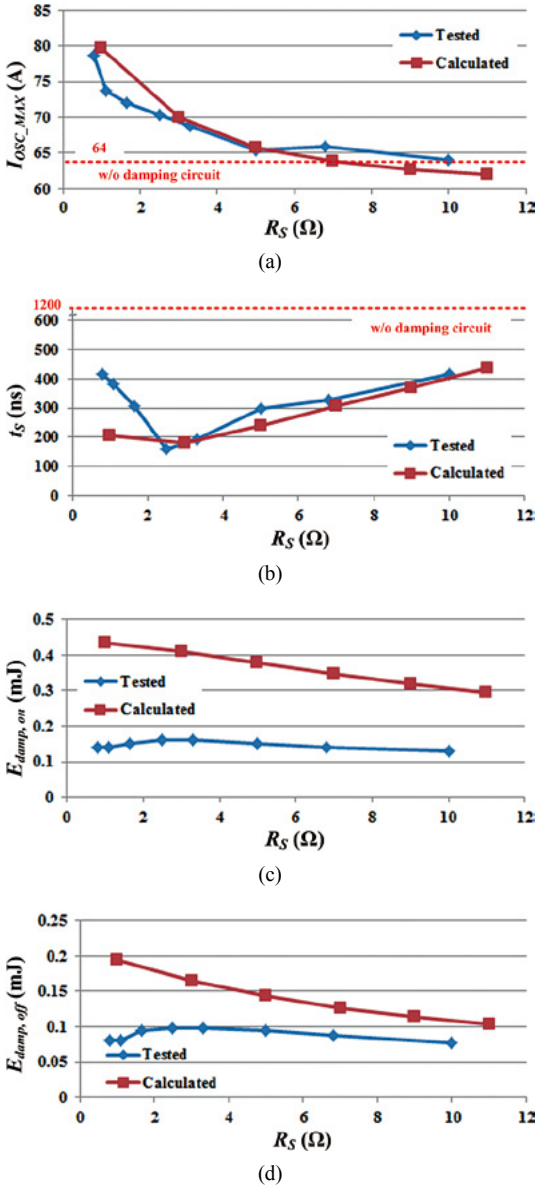


Fig. 23. Turn-on oscillation using damping circuit with different damping resistors:
(a) Maximum oscillation current; (b) Oscillation settling time;
(c) Energy loss in the damping resistor during turn-on; (d) Energy loss in the damping resistor during turn-off.

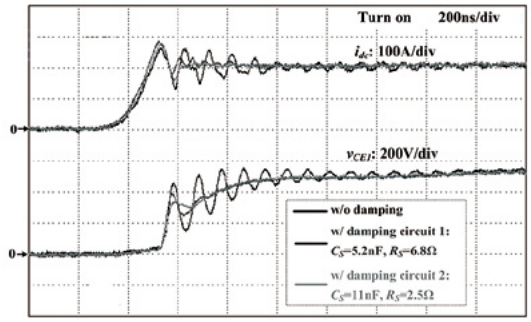


Fig. 24. The comparison of turn-on waveforms with and without the damping circuit.

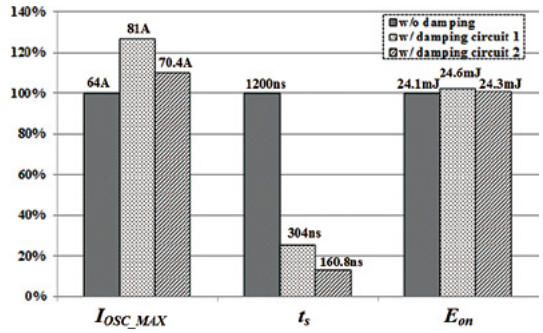


Fig. 25. The performance of oscillation suppression by the damping circuit.

According to the test results, the damping circuits are able to effectively suppress the turn-on current oscillation of the hybrid module. It should be noted that by applying the damping circuits, the maximum oscillation current I_{OSC_MAX} increases due to the discharging of damping capacitor, which is a disadvantage of this method. The oscillation settling time is reduced to 1/4~1/8 of the original value by attaching the damping circuit. Moreover, no significant turn-on energy loss increase (<1%) is caused by attaching the damping circuit. Comparing the two damping circuits, damping circuit 2 is able to achieve the lower turn-on current overshoot and the faster attenuation of oscillation. Damping circuit 1 is the RC circuit parallel connected to each device. Therefore, at each turn-on event, the capacitor is fully discharged, and at each turn-off event, the capacitor is charged to DC bus voltage. During the turn-on event, the discharging current of the damping capacitor flows through the IGBT causing a rise in the maximum oscillation current I_{OSC_MAX}. Also, the charging and discharging current flowing through the damping resistor cause a larger loss in the damping resistor. While for damping circuit 2, the voltage of the damping capacitor does not change much during turn-on and turn-off, only high frequency ripples are present, thus the added current and losses are lower than that of damping circuit 1.

To evaluate the influence of damping circuit on the turn-off characteristics, the turn-off voltage and current waveforms with and without damping circuit are shown in Fig. 26. The testing conditions are the same as those used to obtain the waveforms in Fig. 24. The damping circuit used is damping circuit 2 with the parameters of C_S=11 nF and R_S=2.5 Ω.

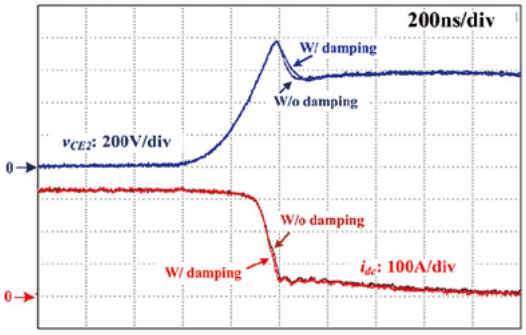


Fig. 26. The comparison of turn-off waveforms with and without the damping circuit.

As shown in Fig. 26, because of the turn-off tail current effect of the IGBT, no major oscillations in the current and voltage waveforms are observed during the turn-off process. Because of the relatively small capacitance of the damping circuit, the damping circuit has little effect on the turn-off voltage waveform. There are no significant changes in the voltage overshoot and current slew rate before and after attaching the damping circuit.

IV. Combining Damping Circuit with Active Gate Driver

In certain applications, besides the duration of current oscillation, the peak current overshoot may be restricted as well. From the studies introduced in the previous sections, it is found that by steering the gate voltage and gate current, active gate drivers are able to suppress the peak current overshoot during turn-on process of hybrid IGBT module. Therefore, by combining the active gate driver with the damping circuit method proposed above, both the suppression of current oscillation and current overshoot can be achieved simultaneously.

Since gate voltage and gate charging current both have large effects on the turn-on maximum oscillation current of the hybrid module, the function of current overshoot suppression can be achieved by adjusting the gate voltage or gate charging current during collector current rising stage in the turn-on process. On the other hand, since gate charging current has large effect on the turn-on delay time and the duration of miller plateau stage, to reduce the total turn-on time and turn-on energy loss, the duration of miller plateau can be reduced by injecting an extra current into the gate during the collector-emitter voltage falling stage. The schematic diagram of the active gate driver used in this paper is shown in Fig. 27.

As shown in Fig. 27, a gate current sink formed by a MOSFET and a diode is used to bypass part of the gate current during the collector current rising stage of the turn-on process, thus the current rising rate is decreased to suppress the current overshoot [6]-[9], [22]. The gate voltage v_{GE} is detected in the turn-on process for the determination of different switching stages. When v_{GE} reaches a preset

threshold voltage, the sink MOSFET will be turned on.

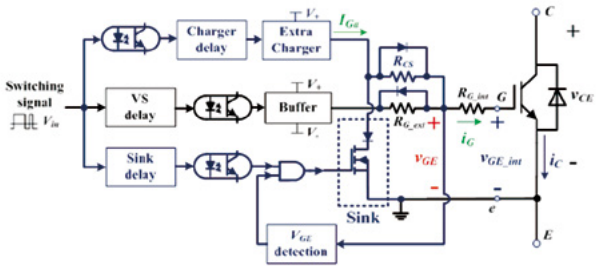


Fig. 27. Schematic diagram of active gate driver

A current source is used as an extra gate charger during the collector-emitter voltage dropping stage to accelerate the voltage drop. The conceptual turn-on waveforms of the active gate driver are shown in Fig. 28, where the dashed lines represent the waveforms achieved by traditional voltage source driver and the solid lines are the waveforms of the active gate driver.

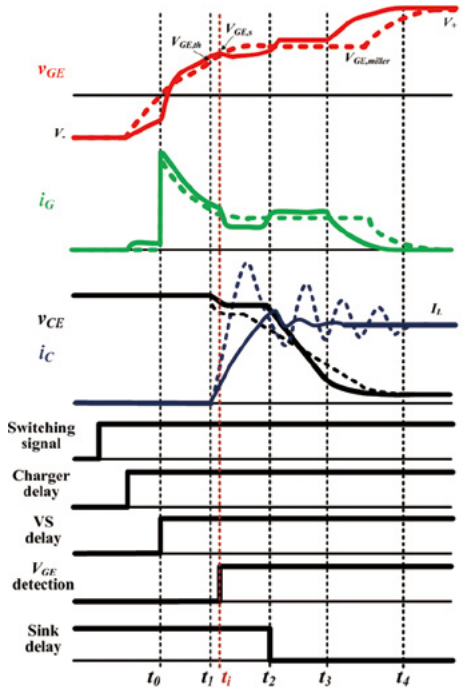


Fig. 28. Conceptual turn-on waveforms of active gate driver.

As shown in Fig. 28, when the turn-on signal comes, the extra gate charger turns on after a short delay. Before time point t_i, when v_{GE} has not reached the preset threshold value $V_{GE,s}$, the sink MOSFET is turned off, and the extra charger charges the gate, reducing the turn-on delay time. At time point t_i, v_{GE} reaches $V_{GE,s}$, the sink MOSFET turns on and bypasses part of the gate current, reducing the collector current rising rate of the IGBT. Then at time point t_2, when collector current reaches the maximum value, the sink MOSFET is turned-off, and the extra charger charges the gate again to reduce the time duration of miller plateau stage. It should be noted that the gate-emitter voltage v_{GE} during turn-on transient is largely dependent on the characteristics of the IGBT, such as input capacitance and transconductance. Therefore, the pre-set threshold value $V_{GE,s}$ of the active gate driver should be experimentally adjusted for the specific IGBT to reach the optimal performance.

To achieve the optimized turn-on performance, the values of R_{CS}, I_{Ga} and the sink delay time should be selected carefully. R_{CS} determines how much of the gate current is bypassed during the current rising stage, I_{Ga} is the extra gate charging current provided by the current source which determines the voltage dropping rate of the miller plateau stage, and the sink delay time should be carefully set so that the sink MOSFET turns off exactly at the time point when collector current reaches its peak value.

The experimental study of the active gate driver is done in the double-pulse test bed shown in Fig. 2. The positive gate voltage V_+ is 13 V and the external gate resistance R_{G_ext} is 3.3 Ω. Tests of turn-on characteristics have been done under 550 V DC bus voltage and 200 A load current. The achieved turn-on waveforms of the active gate driver when R_{CS}=12 Ω and I_{Ga}=300 mA are shown in Fig. 29 along with the turn-on waveforms of the conventional voltage source gate driver.

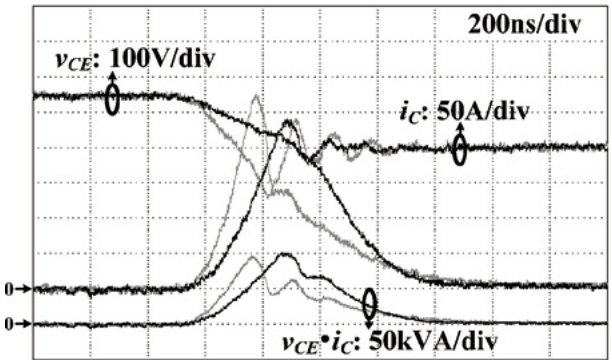


Fig. 29. Achieved turn-on waveforms of active gate driver

As shown in Fig. 29, the grey traces are the waveforms of the conventional voltage source gate driver and the black traces are those of the active gate driver. With the help of the active gate driver, the current rising rate is declined and the current overshoot reduces from 86.2 A to 44.6 A, a 50% reduction is achieved. On the other hand, the turn-on energy loss increases from 29.8 mJ to 34.3 mJ, 15% turn-on energy loss increase is introduced by the active gate driver.

The gate voltage waveforms of the active gate driver and the conventional voltage source driver are shown in Fig. 30. As shown in the waveforms, the gate voltage v_{GE} during the current rising stage is reduced while in the other stages v_{GE} is boosted by the extra gate charger, thus the current rising rate is reduced while the other stages are accelerated, achieving the desired turn-on performance.

Also can be noticed form Fig. 29 and Fig. 30 that since damping circuit is used, the turn-on oscillation is largely mitigated. Now the turn-on current waveform is approaching the ideal waveform with low overshoot and little oscillation.

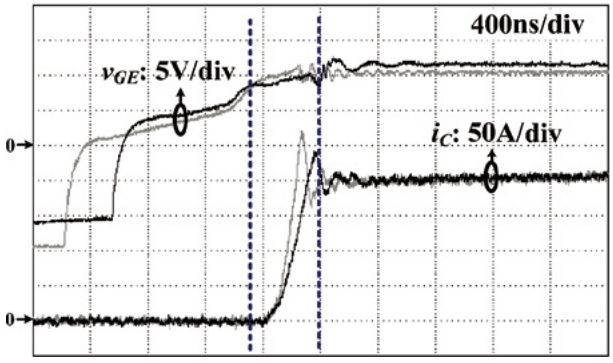


Fig. 30. Gate voltage waveform of the active gate driver

V. Conclusion

In this paper, methods to suppress the turn-on oscillation of hybrid IGBT module are studied. First, experimental analysis is used to evaluate the impacts of gate driver on the collector current oscillation during the turn-on interval of hybrid IGBT module. It is found that by decreasing gate drive voltage and gate charging current, the current overshoot can be suppressed. However, the active gate driver is not effective in reducing the settling time of oscillation. To mitigate the oscillation, a turn-on oscillation suppression method is proposed with combination of damping circuit and active gate driver. According to the analytical and experimental results, the damping circuit is able to effectively reduce the settling time of turn-on oscillation of hybrid IGBT module. Moreover, the damping circuit does not have much impact on the switching losses. The differences between the designs and working principles of snubber circuits and damping circuit are analyzed. It is shown that because the main purpose of snubber circuit is to suppress turn-off over-voltage, the designs and selection of capacitor types are different with damping circuit. By using the conventional snubber circuit design the features of effective turn-on oscillation damping and low loss cannot be achieved simultaneously. It is thus recommended to use the proposed damping circuit design to suppress the current oscillation at turn-on. Then an active gate driver is experimentally studied to illustrate its effectiveness in suppressing the turn-on current overshoot without largely increasing the turn-on energy loss. Combining the damping circuit with the active gate driver, both the suppression of current overshoot and the fast attenuation of current oscillation can be achieved without largely increasing the switching times and switching losses.

References

[1] H. Wang, O. Ikawa, S. Miyashivvta, T. Nishimura, and S. Igarashi, "1700V Si-IGBT and SiC-SBD hybrid module for AC690V inverter system," in Proc. *International Power Electronics Conf. (IPEC, ECCE-Asia)*, 2014, pp. 3702-3706.

[2] K. Ishikawa, K. Ogawa, S. Yukutake, N. Kameshiro, and Y. Kono, "Traction inverter that applies compact 3.3 kV / 1200 A SiC hybrid module," in *Proc. International Power Electronics Conf. (IPEC, ECCE-Asia)*, 2014, pp. 2140-2144.

[3] Erdman, W.L.; Grider, D.; VanBrunt, E., "4500 volt Si/SiC hybrid module qualification for modern megawatt scale wind energy inverters," in *Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2014, pp.1-6.

[4] O. Alatise, N. Parker-Allotey, D. Hamilton, and P. Mawby, "The impact of parasitic inductance on the performance of silicon–carbide schottky barrier diodes," *IEEE Transactions on Power Electronics*, vol. 27, pp. 3826-3833, 2012.

[5] T. Ibuchi and T. Funaki, "Conducted emission characteristics of CCM boost converter with SiC schottky barrier diode," in *Proc. IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, Dresden, pp. 1012-1017.

[6] Y. Sun, L. Sun, A. Esmaeli, and K. Zhao, "A Novel Three Stage Drive Circuit for IGBT," in *Proc. IEEE Conference on Industrial Electronics and Applications*, 2006, pp. 1-6.

[7] K. Onda, A. Konno and J. Sakano, "New concept high-voltage IGBT gate driver with self-adjusting active gate control function for SiC-SBD hybrid module," in *Proc. International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2013, pp. 343-346.

[8] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Transactions on Power Electronics*, vol. 29, pp. 3720-3732, July 2014.

[9] L. Shu, J. Zhang, F. Peng and Z. Chen, "A voltage controlled current source gate drive method for IGBT devices," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 5525-5530.

[10] N. Gao, Y. Wang, X. Cai and S. Igarashi, "Self-adaptive multi-stage IGBT driving method in medium voltage wind generation system," in *Proc. IEEE International Power Electronics and Motion Control Conference (IPEMC, ECCE-Asia)*, 2012, pp. 2287-2289.

[11] K. Fink and S. Bernet, "Advanced gate drive unit with closed-loop diC/dt control," *IEEE Transactions on Power Electronics*, vol. 28, pp. 2587-2595, May 2013.

[12] C. Gerster, P. Hofer and N. Karrer, "Gate-control strategies for snubberless operation of series connected IGBTs," in *Proc. IEEE Power Electronics Specialists Conference*, 1996, pp. 1739-1742 vol.2.

[13] L. Chen and F. Z. Peng, "Closed-Loop Gate Drive for High Power IGBTs," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 1331-1337.

[14] L. Chen, B. Ge and F. Z. Peng, "Modeling and analysis of closed-loop gate drive," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2010, pp. 1124-1130.

[15] Y.Lobsiger, J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT gate driver," *IEEE Transactions on Power Electronics*, vol. 30, pp. 3402-3417, June 2015.

[16] H. Kuhn, T. Koneke and A. Mertens, "Considerations for a digital gate unit in high power applications," in *Proc. IEEE Power Electronics Specialists Conference*, 2008, pp. 2784-2790.

[17] D. Lan, H. Kuhn and A. Mertens, "Digital adaptive driving strategies for high-voltage IGBTs," *IEEE Transactions on Industry Applications*, vol. 49, pp. 1628-1636, April 2013.

[18] P. J. Grbovic, "An IGBT gate driver for feed-forward control of turn-on losses and reverse recovery current," *IEEE Transactions on Power Electronics*, vol. 23, pp. 643-652, Feburary 2008.

[19] P. J. Grbovi, F. Gruson, N. Idir, and P. Le Moigne, "Turn-on performance of reverse blocking IGBT (RB IGBT) and optimization using advanced gate driver," *IEEE Transactions on Power Electronics*, vol. 25, pp. 970-980, April 2010.

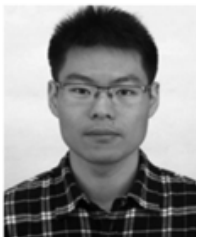
[20] Z. Chen and I. Amaro, "Optimizing low side gate resistance for damping phase node ringing of synchronous buck converter," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, Raleigh, NC, pp. 1827-1832.

[21] J. Makaran, "Gate charge control for MOSFET turn-off in PWM motor drives through empirical means," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1339-1350, 2010.

[22] S. Takizawa, S. Igarashi and K. Kuroki, "A new di/dt control gate drive circuit for IGBTs to reduce EMI noise and switching losses," in *Proc. IEEE Power Electronics Specialists Conference*, 1998, pp. 1443-1449 vol.2.

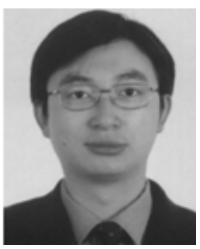
[23] Chokhawala, R.S. and S. Sobhani, "Switching voltage transient

protection schemes for high-current IGBT modules," *IEEE Transactions on Industry Applications*, vol. 33(6), pp. 1601-1610, 1997.
[24] Evaluation Board User's Manual, Cree, CRD8FF1217P-1/2, Oct. 2014.
[25] F. Filsecker, R. Alvarez and S. Bernet, "The Investigation of a 6.5-kV, 1-kA SiC Diode Module for Medium Voltage Converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2272-2280, 2014.
[26] I. Josifovic, J. Popovic-Gerber and J. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3843-3854, 2012.
[27] T. Liu, R. Ning, T. T. Y. Wong and Z. J. Shen, "Modeling and analysis of SiC MOSFET switching oscillations," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 747-756, Sept. 2016.
[28] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573–590, 2013.
[29] A. T. Bryant, L. Lu, E. Santi, J. L. Hudgins, and P. R. Palmer, "Modeling of IGBT Resistive and Inductive Turn-On Behavior," *IEEE Transactions on Industry Applications*, vol. 44, no. 3, pp. 904–914, 2008.
[30] *Designing RC snubbers*, NXP Semiconductors, AN11160, April, 2012.
[31] *Minimizing Ringing at the Switch Node of a Boost Converter*, Texas Instruments, SLVA255, Sept. 2006.
[32] J. Alnasseir, "Theoretical and experimental investigations on snubber circuits for high voltage valves of FACTS-Equipment for over-voltage protection," 2007, dissertation.
[33] Fuji IGBT Modules Application Manual, "Protection Circuit Design," Fuji Electric Device Technology Co., Ltd. February 2004.



Nan Zhu received the B.S. degree from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2011, where he is currently working toward the Ph.D. degree. His current research interests include intelligent power modules, semiconductor power device packaging, and application.

Xingyao Zhang received the B.S. and M.S. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2012 and 2016, respectively. From 2012 to 2013, he worked as an assistant R&D engineer at Delta Electronics (Shanghai) Co., Ltd. He is currently working as an RF engineer at TP-LINK Technologies Co., Ltd. His research interests include IGBT gate driver design and switch mode power supplies.



Min Chen was born in China in 1976. He received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China in 1998 and 2004, respectively. He is currently a Faculty Member at Zhejiang University. His research interests include power quality control, high-frequency high-power conversion, and new energy power conversion system.

Dr. Seiki Igarashi is Senior Manager for Device Application Technology Department Fuji Electric Co., Ltd., Japan. In 1984, he started working at Fuji Electric Corporate R&D Center. He was development of the high efficiency Fuel Cell Inverter, UPS and Industrial Power supplies. From 2003, he moved to the Semiconductor Group. Now he interests New Power Device Development planning and its application technologies. He is member of IEE Japan. He received an Excellent Paper Award from IEE Japan in 2000.

Dr. Tatsuhiko Fujihira is the CTO for Electronic Devices, Fuji Electric Co., Ltd., Japan. He has more than 30 years of experience in the research and development of power semiconductor devices, for example IGBT, power MOSFET, and high-voltage and/or -power ICs. He has authored more than 30 papers, including the world-first technical paper of superjunction devices, in which he named the device as "Superjunction", holds more than 100 patents, and is the receiver of three scientific awards.

Dehong Xu received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1983, 1986, and 1989, respectively. Since 1996, he has been with the College of Electrical Engineering, Zhejiang University, China, as a Full Professor. He was a Visiting Scholar in the University of Tokyo, Japan, from June 1995 to May 1996. From June to December 2000, he was a Visiting Professor in CPES of Virginia Tech, USA. From February 2006 to April 2006, he was a Visiting Professor in ETH, Switzerland. His current research interests include power electronics topology and control, power conversion for energy saving and renewable energy. He has authored or coauthored six books and more than 160 IEEE Journal or Conference papers. He owns more than 30 Chinese patents and 3 U.S. patents. Dr. Xu is the recipient of four IEEE journal or conference paper awards. From 2013, he is the President of the China Power Supply Society. He was an At-Large Adcom Member of the IEEE Power Electronics Society from 2006 to 2008. He is an Associate Editor of the IEEE TRANSACTION ON POWER ELECTRONICS and the IEEE TRANSACTION ON SUSTAINABLE ENERGY. He was the General Chair of the IEEE International Symposium on Industrial Electronics (ISIE2012, Hangzhou), the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG2013, Arkansas), and the IEEE Power Electronics and Applications (PEAC2014, Shanghai), and IFEC2015. He is the IEEE PELS Distinguish Lecturer in 2015.