99% Efficient Three-Phase Buck-Type SiC MOSFET PFC Rectifier Minimizing Life Cycle Cost in DC Data Centers

Lukas Schrittwieser, Johann W. Kolar, and Thiago Batista Soeiro

***Abstract*—Due to the increasing power consumption of data centers, efficient dc power distribution systems have become an important topic in research and industry over the last years and according standards have been adopted. Furthermore the power consumed by telecommunication equipment and data centers is an economic factor for the equipment operator, which implies that all parts of the distribution system should be designed to minimize the life cycle cost, i.e. the sum of first cost and the cost of the power conversion losses. This paper demonstrates how semiconductor technology, chip area, magnetic component volumes and switching frequency can be selected based on life cycle cost, using analytical and numerical optimizations. A three-phase buck-type PFC rectifier with integrated active filter for 380V dc distribution systems is used as an example system, which shows that a peak efficiency of 99% is technically and economically feasible with state-of-the-art SiC MOSFETs and nanocrystalline or ferrite cores. Measurements taken on an 8 kW, 4 kWdm^{-3} hardware prototype demonstrate the validity and feasibility of the design.**

***Index Terms*—Active third-harmonic current injection, buck-type power factor correction (PFC) converter, three-phase rectifier systems, integrated active filter rectifier.**

I. Introduction

INFORMATION and communication technology equipment has become a significant consumer of electric power in recent years. In 2007, for example, the related annual consumption in Germany alone was 55TWh which equaled approximately 10% of the countries total consumption. The annual power consumption of data centers located in Germany is approximately constant at ≈10TWh since 2008 [1]. For the US an annual data center power consumption of 60TWh was estimated in 2006 with a energy cost of $4.5 billion [2], for 2014 an increase to 70TWh has been reported [3]. Therefore the cost of electric energy is a significant economic factor for data center operators and should hence be considered in investment decisions.

In conventional data centers using ac distribution systems, as shown in Fig. 1(a), up to 50% of the total energy consumed is used for air conditioning, distribution and conversion losses [4]. Compared to this, distribution systems based on a dc bus with a nominal voltage of 380V offer significantly higher efficiency, improved reliability and reduced capital cost and floor space, cf. Fig. 1(b) [5]. Furthermore they allow a direct connection of lead acid batteries, consisting of 168 cells connected in series, with a typical floating cell voltage of ≈ 2.26 V, which results in a nominal bus voltage of 380 V. Accordingly, standards and components for dc distribution systems have been developed in recent years [6], [7].

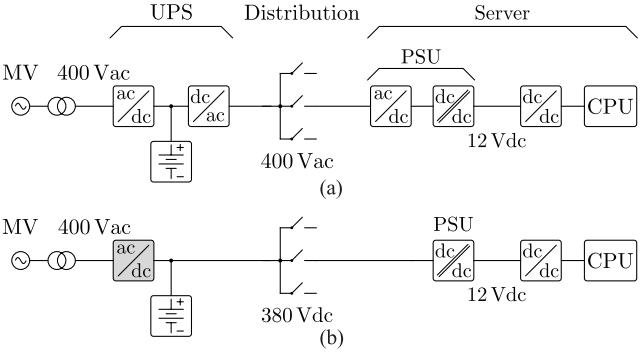

Fig. 1. Data center power distribution concepts: (a) Conventional 400 Vac distribution, using an ac output Uninterruptible Power Supply (UPS). Similar concepts can be used with 480 Vac. (b) Facility level dc distribution system based on a 380 Vdc bus which allows a direct connection of backup batteries [4].

Normally a boost-type power factor correction (PFC) stage is used to convert the 400 Vac mains into a dc voltage which is higher than the full-wave rectified ac input voltage, typically in the range of 700V to 800 V. A subsequent buck converter is then required to connect the PFC output to the dc distribution bus. (This configuration is also used for fast chargers of Electric Vehicle batteries which are powered from the three-phase ac mains [8].) As an alternative, a single-stage conversion between the three-phase mains and a dc bus with lower voltage can be achieved with buck-type PFC converters, like the SWISS Rectifier, the six-switch buck rectifier or the Integrated Active Filter rectifier [9]-[12].

The circuit topology of the Integrated Active Filter (IAF) buck-type PFC rectifier, shown in Fig. 2, was first introduced in [13] for three-phase solar inverters. A similar circuit was also proposed for drive systems with small dc-link capacitors [14]. Three major blocks can be identified in the IAF rectifier's schematic: an Input Voltage Selector (IVS) built of

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a linecommutated full-wave diode rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$2 and three four-quadrant switches $S_{\bar{k}y\bar{k}}$, a current injection circuit S_{xy}, S_{yz}, L_{inj} and a dc-dc buck converter S_x, D_z, L_o which provides the constant dc output voltage u_{pn}. Typically a small capacitor C_f' is required to ensure a valid conduction path during the commutation of S_{xy}, S_{yz} and S_x. Note that the IVS switches and diodes are commutated at mains frequency only which implies that almost no switching losses occur in the IVS, therefore rectifier diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ which are optimized for a low forward voltage drop can be used.

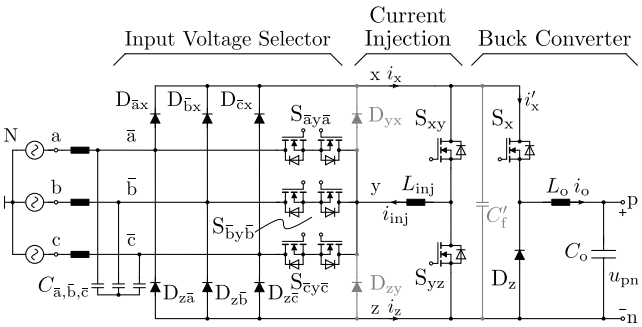


Fig. 2. Schematic of the Integrated Active Filter rectifier (IAF), using an Input Voltage Selector (IVS) commutated at mains frequency, combined with a buck converter providing the output current i_o and a current injection converter which serves as active harmonic filter for achieving sinusoidal ac input currents.

For this paper the IAF buck-type PFC rectifier was selected to demonstrate a cost-driven converter design approach, as only two line-commutated diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$, and one power transistor S_x are in its main conduction path [9], [15]. Based on a short review of the IAF rectifier's main properties in Section II and using the capital equivalent worth of energy together with component cost models, a non-isolated 8kW PFC rectifier is designed in Section III. This allows selecting cost optimal components such as semiconductors and inductors achieving an economically optimal converter which minimizes life cycle cost, i.e. the sum of first cost of the converter hardware and the cost of conversion losses during the service life. Measurements taken on a hardware prototype are presented in Section IV.

II. Integrated Active Filter PFC Rectifier

Simulation results for a 8kW IAF buck-type PFC rectifier (cf. Fig. 2) are shown in Fig. 3, for the system specifications given in Table I. For the IAF rectifier the current injection circuit and the buck converter can be analyzed, optimized and operated almost independently of each other. As the dc output is provided by the buck converter (S_x, D_z, L_o), the output current i_o and voltage u_{pn} can be controlled independently of the injection circuit. This can be seen from the simulation results in Fig. 3: During $\omega t < 180°$ the current injection circuit is turned off, i.e. $i_{inj} = 0$. As the buck converter creates a constant output current i_o it consumes constant power from the ac input. Hence non-sinusoidal ac input currents $i_{a,\,b,\,c}$ result and only two ac input phases $i_{a,\,b,\,c}$ conduct current at a time.

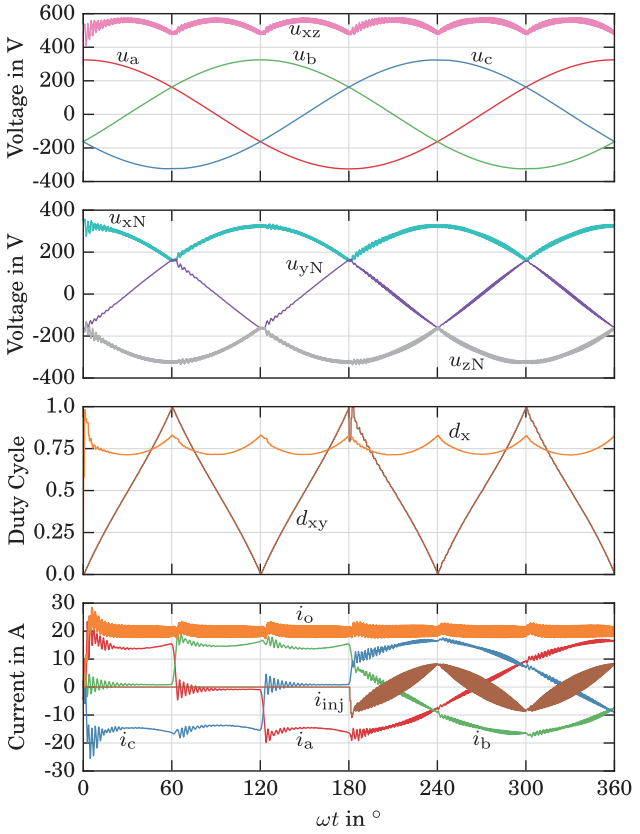


Fig. 3. Simulation results for an IAF buck-type PFC rectifier as shown in Fig. 2, plotted are the ac input voltages $u_{a,\,b,\,c}$, the IVS output voltages u_{xN}, u_{yN} and u_{zN}, the buck stage duty cycle d_x, the duty cycle d_{xy} of switch S_{xy}, the output current i_o, the injection current i_{inj} and the ac input currents $i_{a,\,b,\,c}$. During $\omega t < 180°$ the injection circuit is disabled (i.e. $i_{inj} = 0$) which results in non-sinusoidal mains currents $i_{a,\,b,\,c}$.

TABLE I
Converter Specifications

Input Voltage (Line-to-Neutral)	$U_1 = 230$ V rms
Input Frequency	$\omega_1 = 2\pi\ 50$ Hz
Switching Frequency	$f_s = 27$ kHz
Nominal Output Voltage	$U_{pn} = 400$ V
Nominal Output Power	$P_o = 8$ kW

For $\omega t > 180°$ the injection circuit is used to create a current i_{inj} which is proportional to the voltage u_{yN},

$$i_{inj}(\omega t) = -\hat{I}_1 \frac{u_{yN}(\omega t)}{\hat{U}_1} \quad \hat{I}_1 = \frac{2\,P_o}{3\,\hat{U}_1} \quad , \qquad (1)$$

where $\hat{I}_1$ is the peak value of the rectifier's ac input line current and $\hat{U}_1$ is the ac phase-to-neutral voltage amplitude. This results in sinusoidal ac input currents as shown in Fig. 3. A more detailed description of the modulation and control strategy can be found in [9], a brief description of the main

components is given in the following.

A. Input Voltage Selector

As described above, the IAF rectifier uses an IVS, which connects each ac input phase a, b, c to either node x, y or z. This implies that the voltages u_{xN}, u_{yN} and u_{zN} are piecewise sinusoidal, which allows to move the ac filter capacitors $C_{\bar{a},\bar{b},\bar{c}}$ from nodes $\bar{a}$, $\bar{b}$, $\bar{c}$ to nodes x, y, z as shown in Fig. 4. This shortens the commutation paths of the buck converter and the injection switches. Additionally the diode bridge currents i_x and i_z become continuous which reduces the conduction losses in the bridge diodes $D_{\bar{k}x}$ and $D_{z\bar{k}}$ and in the fourquadrant switches $S_{\bar{k}y\bar{k}}$. The resulting rms current values can be calculated as

$$I_{\mathrm{D}\bar{\mathrm{k}}\mathrm{x},\mathrm{rms}} = \hat{I}_1 \sqrt{\frac{\sqrt{3}}{8\pi} + \frac{1}{6}} \quad \text{and} \tag{2}$$

$$I_{\mathrm{S}\bar{\mathrm{k}}\mathrm{x},\mathrm{rms}} = \hat{I}_1 \sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}} \quad . \tag{3}$$

Assuming that MOSFETs are used as synchronous rectifiers, as shown in Fig. 4, the conduction losses are reduced by 31% in the rectifier bridge and by 78% in the four-quadrant switches compared to the original circuit shown in Fig. 2 [16].

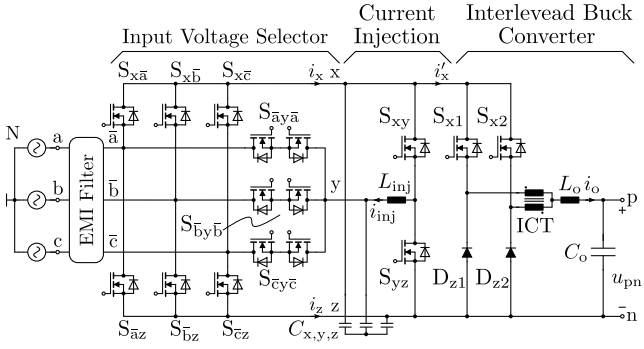


Fig. 4. Schematic of the IAF rectifier where the input filter capacitors have been moved from the ac side ($\bar{a}$, $\bar{b}$, $\bar{c}$) of the IVS to its output side (x, y, z), which reduces the conduction losses [16]. The diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ are replaced with SiC MOSFETs $S_{x\bar{k}}$, $S_{\bar{k}z}$ operating as synchronous rectifiers to further increase the efficiency. An interleaved buck converter with cells S_{x1}, D_{z1} and S_{x2}, D_{z2} is used where S_{x1} and S_{x2} are controlled with 180° phase shifted PWM signals. This lowers the current ripple in i'_x which leads to a lower voltage ripple at the input filter capacitors $C_{x,y,z}$. The buck converter output inductors are implemented as an inter-cell transformer (ICT) with closely coupled windings and a single output inductor L_o.

B. Buck Converter

It can be seen in Fig. 4 that the buck converter's input is connected to u_{xz} which is a six-pulse shaped voltage provided by the IVS' rectifier bridge, cf. Fig. 3. Neglecting any voltage drops across the semiconductors and inductors, the dc output voltage u_{pn} can be expressed as

$$u_{\mathrm{pn}} = \frac{3}{2}\hat{U}_1\, m \quad m \in [0,1] \quad , \tag{4}$$

where $\hat{U}_1$ is the ac phase-to-neutral voltage amplitude and m is the converter's modulation index. Note that a small distortion of the output current and the mains input currents occurs at every 60° sector of the ac input voltage, i.e. at the intersection of two phase voltages $u_{a,b,c}$. This is most likely due to the switching frequency ripple of the filter capacitor voltages u_{xN}, u_{yN}, u_{zN} as similar disturbances exist in the SWISS rectifier [16]. This voltage ripple is the result of the buck converter's discontinuous input current i'_x and could be reduced with larger $C_{x,y,z}$. However, as the capacitor voltages u_{xN}, u_{yN}, u_{zN} are piecewise sinusoidal they generate reactive power which is typically limited to 5% to 10% of the converter's active power rating.

C. Interleaved Buck Converter

In order to reduce the buck converter's input current ripple and hence the mains input current distortions and the electromagnetic noise emission of the rectifier, an interleaved buck converter can be used, as shown in Fig. 4. By modulating the switches S_{x1} and S_{x2} with 180° phase shifted PWM signals the peak-to-peak ripple in i'_x is reduced by approximately a factor of two and the ripple frequency is doubled due to cancellation of harmonics.

The dc output filter of the interleaved buck converter can be implemented by a combination of an inter-cell transformer (ICT) with closely coupled windings and a single inductor instead of two separate inductors. Using ICTs for interleaved dc-dc converters has been extensively described in literature and has been shown to result in a reduction of the magnetic component's volume, losses and weight [17]-[19].

In Fig. 5 the basic operating principle is shown for a duty cycle of $d_x = 0.75$ and 180° phase shifted PWM signals. The two cells S_{x1}/D_{z1} and S_{x2}/D_{z2} produce the output voltages u1 and u2 shown in Fig. 5(e). These can be transformed into the corresponding common-mode (cm) and differential-mode (dm) voltages u_{cm} and u_{dm}, cf. Figs. 5(f)-(g)

$$u_{\mathrm{cm}} = \frac{u_1 + u_2}{2} \quad , \tag{5}$$

$$u_{\mathrm{dm}} = \frac{u_1 - u_2}{2} \quad . \tag{6}$$

By replacing the ICT with the equivalent circuit shown in Fig. 5(b) the circuit diagram Fig. 5(c) results, which can be decomposed into two uncoupled circuits as shown in Fig. 5(d). It can be seen that the cm voltage u_{cm}, which is applied to the dc output inductor L_o and the ICT's leakage inductance L_σ, switches twice per switching frequency period and has a voltage step height of half the input voltage u_{xz}.

Note that unbalances in the system, such as unequal on-state resistances of the switches, duty cycle differences and mismatched PCB track resistances can lead to unbalanced ICT currents $i_{o1} \neq i_{o2}$. This results in a dc magnetization cur-

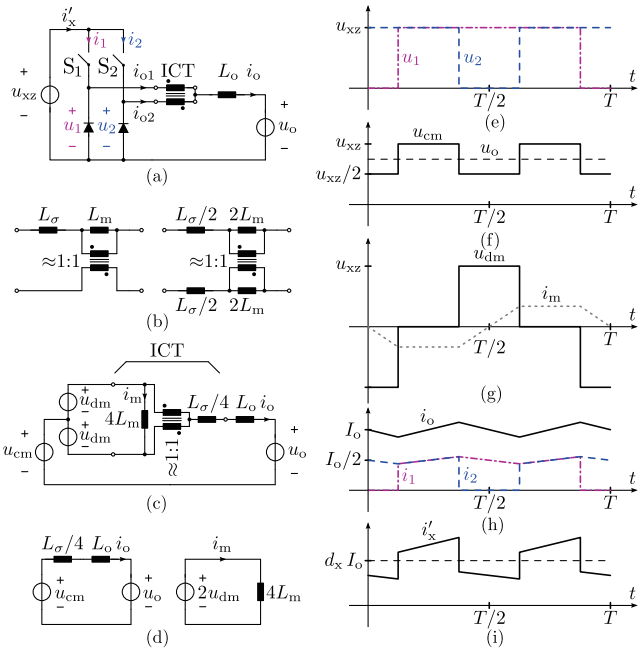


Fig. 5. Operating principle of an interleaved buck converter using a close-coupled inter-cell transformer (ICT). (a) shows the basic circuit diagram, the switches are controlled with 180° phase shifted PWM signals as shown in (e). Replacing the ICT with the equivalent circuit of an non-ideal transformer as shown in (b) and separating voltages u_1 and u_2 into common-mode (cm) and differential-mode (dm) voltages, u_{cm} and u_{dm}, yields the circuit shown in (c). It can be seen that u_{cm} is applied to L_σ and L_o and can be used to control the output current i_o, while udm controls the ICT's magnetizing current i_m as shown in (d).

rent of the ICT,

$$i_m = \frac{i_{o1} - i_{o2}}{2} \quad , \tag{7}$$

that could lead to a saturation of the core material. However, the dm voltage u_{dm} is applied to the ICT's magnetizing inductance L_m and can be used by an active control circuit to ensured an equal current sharing $i_{o1} \approx i_{o2}$ in the ICT windings. Strategies for active current balancing control in ICTs have been described in the literature [20]-[21].

III. Life Cycle Cost Based Converter Design

The design of any power electronic converter is essentially aiming for a best possible overall compromise of multiple trade-offs which result from couplings between different components concerning stresses and utilization. For example increasing the switching frequency reduces the peak-to-peak flux ripple of magnetic components which typically leads to smaller and/or more efficient components, but also increases the switching losses of the semiconductors. This in turn requires a larger heat sink and which could overcompensate the volume reduction achieved in the magnetic components. Similar trade-offs also exist on the component level, e.g. increasing the number of turns in an inductor decreases the core losses at the expense of increased winding losses. Furthermore even for a given fixed switching frequency multiple combinations of volumes or sizes of the different components can lead to similar power densities and efficiencies. Designing an optimal converter becomes even more challenging if more than a single circuit topology and/or several different core and winding materials are taken into account. Due to these tradeoffs a single optimal converter can typically not be found but rather a range of pareto optimal designs can be calculated which achieve e.g. the highest efficiency for a given power density and vice versa.

These trade-offs can be simplified by introducing a singlevalued objective function such as life cycle cost (LCC). As described in [22] the capital equivalent worth of one watt of continuous dissipation can be used to select components in order to minimize the LCC of that component. Combined with cost models, the switching frequency, semiconductors and magnetic components are selected to achieve minimal life cycle cost for a given service life time assuming continuous operation at rated power as will be shown in the following for the IAF rectifier [23].

Given some basic economic parameters, such as interest and inflation rates, the capital-equivalent worth of a continuously dissipated watt of ac power can be estimated. In 2008 the authors of [22] estimated an average value of $14 per watt for the US market and 15 years of service life, which implies that up to $14 could be invested now in order to reduce the equipment's power consumption by one watt over the next 15 years. Although the prices for electric power show a considerable geographical variation (approximately a factor of 5 in the US), the authors conclude that the cost of dissipation significantly overshadows the first cost for telecom power supplies.

A. Semiconductor Technology Comparison

An example calculation for the input voltage selector fullwave rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ / $S_{x\bar{k}}$, $S_{\bar{k}z}$ is shown in Fig. 6, where

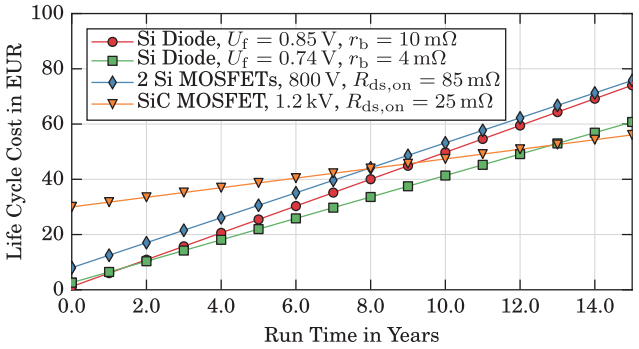


Fig. 6. Comparison of life cycle cost for different implementations of the diode bridge rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ of the IVS with $I_{rms} = 8.1$ A, $I_{avg} = 4.6$A (P_o = 8 kW) and a capital equivalent worth of EUR 0.12 per kWh [22]. Switching losses are neglected as the IVS commutates at twice the mains frequency only. It can be seen that the significantly higher first cost of a SiC MOSFET is compensated by the reduced conduction losses of the device achieving roughly the same life cycle cost as Si diodes and Si MOSFETs for run times of approximately ten years, assuming continuous operation at rated power.

a capital equivalent worth of γ = EUR 0.12 per kWh (approximately USD 0.13 at time of publication) is assumed. Neglecting switching losses in the IVS, the device losses can be directly determined from the rms and average currents found by numerical simulation, resulting in I_{rms} = 8.1A and I_{avg} = 4.6A for an 8kW system. Assuming a service life time of 10 years or more, a SiC MOSFET with a high initial cost of approximately EUR 30 and low on state resistance achieves the same or lower life cycle cost than conventional Si diodes with an initial cost of EUR 2.6. The same holds for a parallel connection of two Si MOSFETs with a first cost of approximately EUR 8. Note that all devices are operated far below their thermal limits, e.g. 1.7W of conduction losses result for the SiC MOSFTEs, ≈ 4W for the Si diodes and Si MOSFETs while all devices are rated for more than 100W of continuous power dissipation.

B. Semiconductors without Switching Losses

The calculation shown in Fig. 6 is based on a selection of standard semiconductor devices which might not achieve the lowest possible LCC. Using more than one device in parallel reduces the total on-state resistance $R_{ds,on}$ of MOSFETs or the (differential) bulk resistances r_b of diodes which lowers the conduction losses. This reduces the cost of dissipation during system operation, but increases the first cost as more devices are used, which implies that the resulting LCC is a function of the number n of devices used in parallel. For a MOSFET, continuously conducting the current I_{rms} for the run time t_r, without switching losses the corresponding LCC Λ can be expressed as

$$\Lambda_M(n) = \underbrace{\gamma\, t_r\, \frac{R_{ds,on}}{n}\, I_{rms}^2}_{\text{Cost of Dissipation, } \Gamma_M} + \underbrace{\sigma_M\, n}_{\text{First Cost, } \Sigma_M}\ , \tag{8}$$

where σ_M is the cost of a single MOSFET with an onstate resistance $R_{ds,on}$. A plot of the resulting values for t_r=10 years, $R_{ds,on}$=96mΩ and σ_M = EUR 7.14 is shown in Fig. 7. For a given t_r the optimal number of devices n_{opt}, which achieves minimal life cycle cost, can be derived by minimizing (8) with respect to n as

$$n_{opt} = \sqrt{\gamma\, t_r\, \frac{R_{ds,on}}{\sigma_M}}\, I_{rms}\ , \tag{9}$$

$$\Gamma_{M,opt} = \Sigma_{M,opt} = \sqrt{\gamma\, t_r\, R_{ds,on}\, \sigma_M}\, I_{rms}\ , \tag{10}$$

$$\Lambda_{M,opt} = \Gamma_{M,opt} + \Sigma_{M,opt} = 2\sqrt{\gamma\, t_r\, R_{ds,on}\, \sigma_M}\, I_{rms}\ . \tag{11}$$

Note that a certain minimum n_{min} exists due to the thermal limits of the device and the cooling system as indicated in Fig. 7. However, even for short run times of $t_r \approx 1$ year the optimal n is typically larger than n_{min}.

This optimization can be extended from MOSEFTs to diodes modeled by a constant forward voltage drop U_f connected in series with a (differential) bulk resistance r_b as

$$\Lambda_D(n) = \gamma\, t_r\, \frac{r_b}{n}\, I_{rms}^2 + \gamma\, t_r\, U_f\, I_{avg} + \sigma_M\, n\ . \tag{12}$$

In this case n_{opt} does not depend on Uf , however the losses and hence the cost of dissipation Γ increases. An example calculation for different run times is shown in Fig. 8 where a 96mΩ SiC MOSFET and Si diode with U_f = 0.74A and r_b = 4mΩ are considered as unit elements. For both, MOSFETs and diodes the optimal n increases proportional to $\sqrt{t_r}$, however for Si diodes the resulting losses show little variation due to U_f. As the first cost of the considered diode is ≈ 6

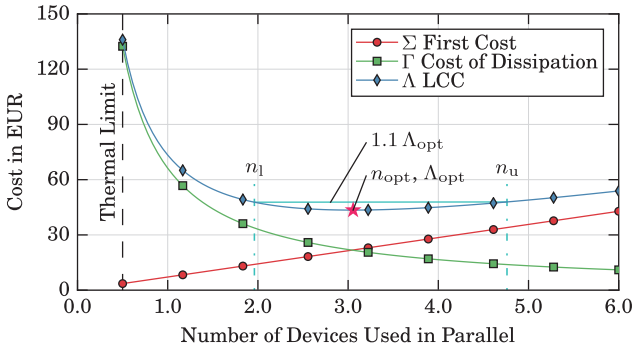


Fig. 7. First cost, cost of dissipated energy and life cycle cost (LCC) as a function of the number of devices connected in parallel for the rectifier bridge $S_{x\bar{k}}$, $S_{\bar{k}z}$ at nominal operation with I_{rms} = 8.1A (P_o = 8 kW). A SiC MOSFET with $R_{ds,on}$ = 96mΩ and a cost of EUR 7.14 is considered as unit device together with a capital equivalent worth of γ = EUR 0.12 per kWh and a run time of t_r = 10 years.

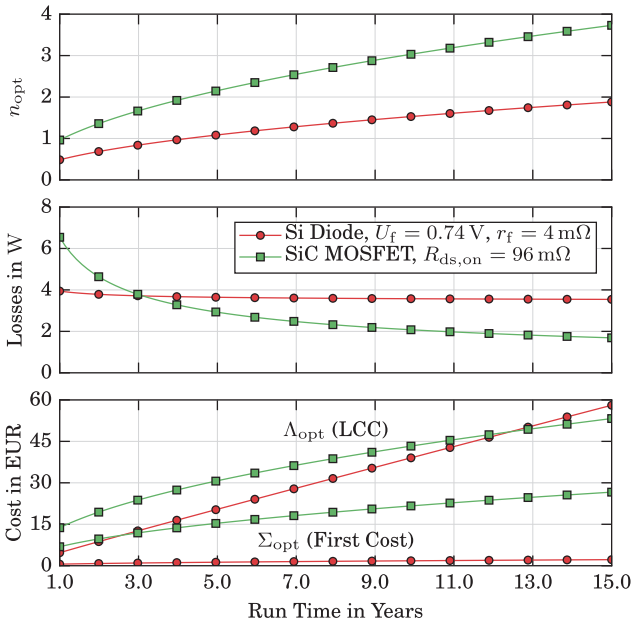


Fig. 8. Optimization results for Si Diodes and SiC MOSFETs showing the optimal (lowest LCC) number of parallel devices, resulting device losses, first and life cycle cost as a function of the run time t_r in years. The same parameters as in Fig. 7 are used.

times lower than the MOSFET's the Si diodes achieves lower LCC for small t_r while the SiC MOSFET achieves lower LCC for $t_r \geq 12.5$ years.

C. Device Selection

So far n has been assumed as a real number which has to be rounded to the next integer or to the next $R_{ds,on}$ value available from the device manufacturer. This leads to a suboptimal LCC, but it can seen in Fig. 7 that $\Lambda(n)$ is flat around the optimum. If a certain allowed increase α in LCC is assumed, a resulting lower and upper bound (n_l, n_u) for permissible values of n can be calculated using (8) as

$$n_l(\alpha) = n_{opt}\left(1+\alpha-\sqrt{(1+\alpha)^2-1}\right) . \quad (13)$$

$$n_u(\alpha) = n_{opt}\left(1+\alpha+\sqrt{(1+\alpha)^2-1}\right) . \quad (14)$$

To derive the required granularity of n the ratio r_n of n_u and n_l can be calculated,

$$r_n(\alpha) = \frac{n_u(\alpha)}{n_l(\alpha)} \quad r_n(0.1) = 2.43 \quad , \quad (15)$$

which does not depend on any device specific parameters in (8) and results in a value of 2.43 for $\alpha = 0.1$ (also shown in Fig. 7). This implies that the achievable LCC is at most 10% higher than the theoretical optimum if the ratio between two consecutive $R_{ds,on}$ values of the available devices is 2.4 or less.

D. Including Switching Losses

In the derivation (9), which gives the LCC optimal number of device, it was assumed that switching losses can be neglected which is typically not the case for the half bridge S_{xy}, S_{yz} used in the current injection circuit. The calculation can be extended by fitting a second order polynomial to measured hard switching losses (turn-on and turn-off) for the switched voltage,

$$E_{sw}(I_{sw}) \approx E_0 + E_1 I_{sw} + E_2 I_{sw}^2 , \quad (16)$$

where I_{sw} is the switched current. Switching losses measured in [23] for a half bridge of two *C2M0080120* SiC MOSFETs and 600V dc link voltage at various I_{sw} are shown in Fig. 9 together with a second order polynomial fitted by least squares regression. If n devices are used in parallel, equal current sharing is assumed and the switching frequency current ripple in the output current can be neglected the total switching losses can then be calculated as

$$E_{sw} \approx n\left[E_0 + E_1\frac{I_{sw,avg}}{n} + E_2\left(\frac{I_{sw,rms}}{n}\right)^2\right] , \quad (17)$$

where $I_{sw,avg}$ and $I_{sw,rms}$ are the average and rms values of the switched current over one mains voltage period. It can be seen that the terms in (17) have the same dependency on n as those in (8) which implies that the optimal number of devices which achieves minimal LCC for a given f_{sw} can be calculated as

$$n_{opt} = \sqrt{\gamma\, t_r \frac{R_{ds,on}\, I_{rms}^2 + f_{sw}\, E_2\, I_{sw,rms}^2}{\sigma_M + \gamma\, t_r\, f_{sw}\, E_0}} . \quad (18)$$

The resulting n_{opt}, first cost $\sum_{opt}$ and LCC Λ_{opt} for the injection switches S_{xy}, S_{yz} are shown as function of the switching frequency f_{sw} in Fig. 10. It can be seen that n_{opt} and therefore $\sum_{opt}$ decrease with f_{sw} while the cost of dissipation Γ increases, mainly due to the switching losses.

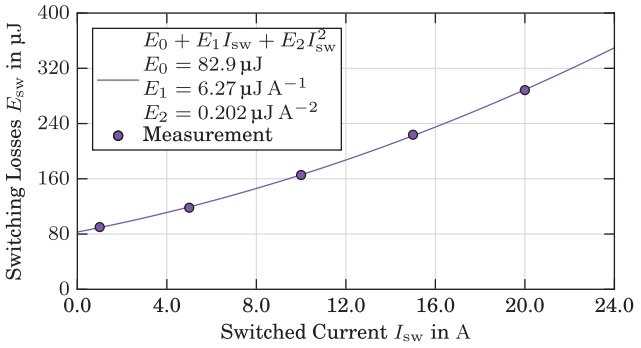


Fig. 9. Sum of turn-on and turn-off losses E_{sw} measured in [23] as a function of the switched current I_{sw} for a half bridge of *C2M0080120* SiC MOSFETs with 600V dc link voltage at 25 °C. Additionally a second order polynomial function fitted by least squares regression is shown and the fitted parameters are given in the legend.

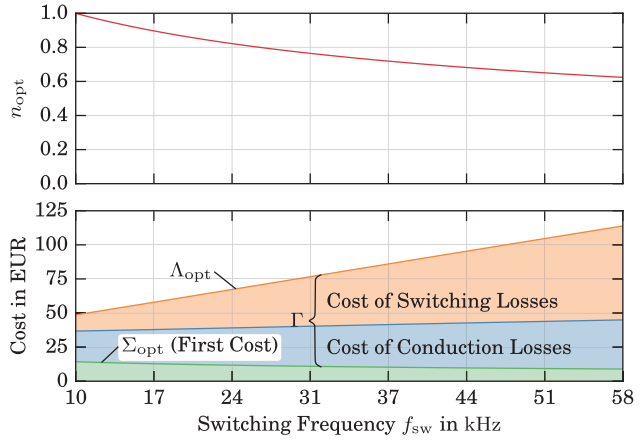


Fig. 10. Life cycle cost and optimal number of MOSFETs in parallel nopt for a half bridge built with *C2M0080120* devices for the injection Switches Sxy and Syz with an rms current $I_{rms} = I_{sw,rms} = 4.7$A and an average switched current of $I_{sw,avg} = 4.1$A as a function of the switching frequency for $t_r = 10$ years.

E. Magnetic Components

The dimensioning of magnetic components is performed

with a similar algorithm, but unlike for semiconductor devices analytical solutions can typically not be found. For a given f_{sw} the current and voltage stresses created by the converter can be determined and for a selected core material, shape and size the optimal number of turns, which minimizes the sum of core and winding losses, can be determined by numerical optimization methods. Using the losses and cost models for core and winding materials the inductor's LCC is calculated, which allows the selection of an optimal core size achieving minimal LCC for the given f_{sw} and t_r.

F. Optimal Switching Frequency Selection

Once the optimal LCC of semiconductors and magnetic components has been calculated as a function of f_{sw} these can be added in order to select a switching frequency which achieves the lowest total LCC. An example calculation for the injection circuit with the switches S_{xy}, S_{yz} and the inductor L_{inj} is shown in Fig. 11, where it can be seen that the inductor's first cost $\sum_{Linj}$ and cost of dissipation Γ_{Linj} and hence its LCC decrease with increasing f_{sw} as opposed to the increasing LCC of the semiconductors, resulting in an optimal f_{sw}. A total run time of t_r = 10 years is assumed in this example.

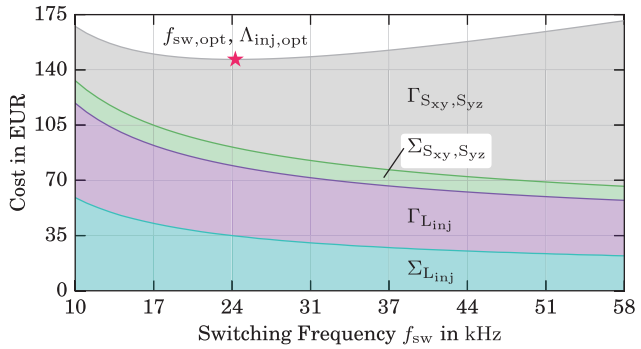


Fig. 11. Example showing the selection of a switching frequency f_{sw} which achieves the lowest sum of LCCs for the injection switches S_{xy}, S_{yz} and the corresponding inductor L_{inj} for t_r = 10 years, not considering any other components of the rectifier.

G. Global Optimization Algorithm

In a final step the algorithm outlined above can be extended to include the entire rectifier to determine the optimal f_{sw} and all optimal component sizes by minimizing the systems LCC

$$\Lambda_{\mathrm{sys,opt}}(t_r) = \min_{f_{sw}} \sum_{k} \Lambda_{k,\mathrm{opt}}(f_{sw}, t_r)\ . \qquad (19)$$

The design procedure sweeps over all relevant switching frequencies f_{sw} and considered run times t_r, where for each tupel (f_{sw}, t_r) and all components k (e.g. switches, inductors, etc.) of the system an optimal relative size $n_{k,opt}$ can be determined which achieves minimal LCC $\Lambda_{k,opt}$ for component k. This implies that all components can be designed independently of each other which simplifies the optimization procedure. Once all components have been selected, their life cycle costs can be summed up which yields the system's LCC for the considered (f_{sw}, t_r) : Once all designs have been calculated the switching frequency achieving lowest overall LCC is selected for each t_r considered in the analysis.

H. Auxiliary Components

The losses, volumes and costs of other components, such as gate drive circuits, DSP/FPGA, capacitors, PCBs, heat sinks, fans, EMI filter, etc have to be considered as well. While their contribution to the overall converter volume, and LCC can be significant, they are almost independent of the design point in the considered application. Therefore these auxiliary components have been considered in the design but were not part of the optimization.

I. Optimization Results

Fig. 12 shows the achievable minimal LCC $\Lambda_{sys,opt}(t_r)$ and the resulting first cost $\sum_{sys,opt}(t_r)$ as a function of run time calculated by the optimization outlined above. It can be seen that the first cost of the optimal systems is less than 30% of the total life cycle cost for a run time of 10 years or more. Furthermore, the LCC is comparable for all three core materials considered in the optimization. Designs using amorphous cores are expected to have slightly higher LCC than systems with nanocrystalline or ferrite cores, which is due to the higher core losses of amorphous materials.

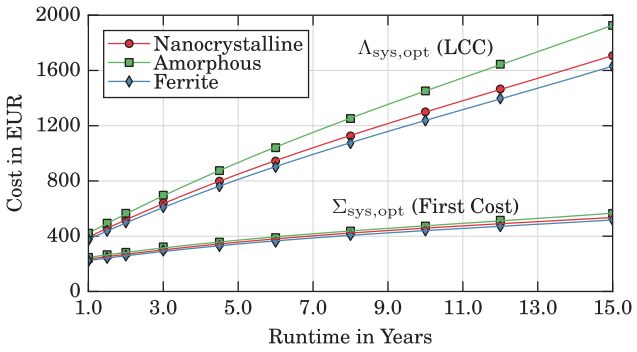


Fig. 12. Minimal achievable LCC and according first cost of optimal converter designs as a function of run time for different inductor core materials. It can be seen that for a run time of ten years, the first cost is < 30% of the total life cycle cost. The optimization results in similar first costs for all three core materials, however the life cycle cost of designs with ferrite and nanocrystalline inductors is slightly lower compared to solutions with amorphous cores.

However, the volumes and switching frequencies of the designed converters differ significantly as shown in Fig. 13; the resulting efficiency as function of t_r is shown in Fig. 14. For short run times ($\leq$ 2 years) converters with high switching frequencies and high power densities achieve minimal LCC as opposed to long run times ($\geq$10 years) where designs with approximately half the switching frequency, twice the volume and half the losses result. Furthermore, these results show that very high efficiencies of up to 99% are economically feasible with available state-of-the-art SiC

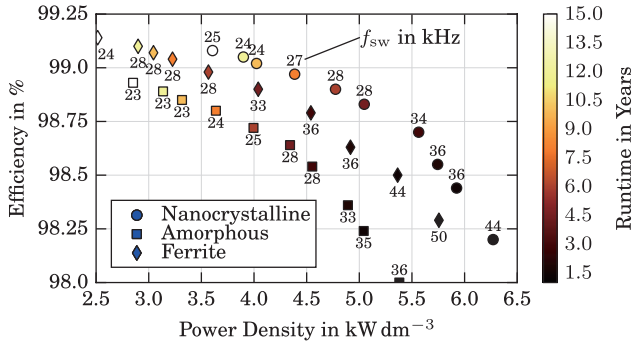


Fig. 13. Optimization results showing power density, efficiency and switching frequency f_{sw} of designs achieving minimal LCC for different run times and inductor core materials of ICT, L_{inj} and L_o.

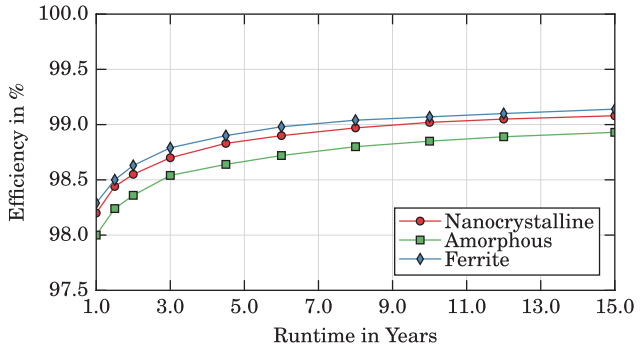


Fig. 14. Calculated efficiencies of life cycle cost optimal converter designs for different run times and core materials.

switches and core materials. Note that three-phase rectifiers based on Si and SiC MOSFETS with slightly lower efficiencies have been reported in the literature [24], [25], however without considering cost.

J. Selected Design

Based on the numerical optimization results the design point with t_r = 10 years, f_{sw} = 27 kHz, a power density of 4.0 kWdm^{-3} and an efficiency of 99% was selected to implement a hardware prototype. *FINEMET* nanocrystalline cores with helical windings (cf. Fig. 15) are used as they achieve considerably higher power density compared to designs based on ferrite. Detailed results of the optimization are shown in Fig. 16: for systems with a run time of 10 years or more, it can be seen that the semiconductors and heat sinks contribute about half of the first cost, life cycle cost and losses, but only about 10% to 20% of the total volume. Furthermore, the auxiliary components, such as PCBs, gate drivers, FPGA/DSP etc. have a significant contribution to both first cost and life cycle cost which implies that they cannot be neglected in the design process.

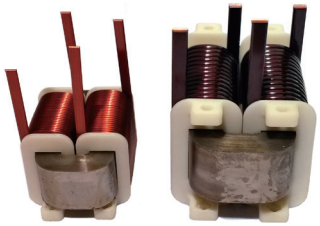


Fig. 15. Picture of L_{inj} and L_o, implemented using nanocrystalline C cores and helical windings. A boxed volume of 88 cm^3 and 249 cm^3 results for the two inductors. The specifications and parameters of the implemented inductors are given in Table II.

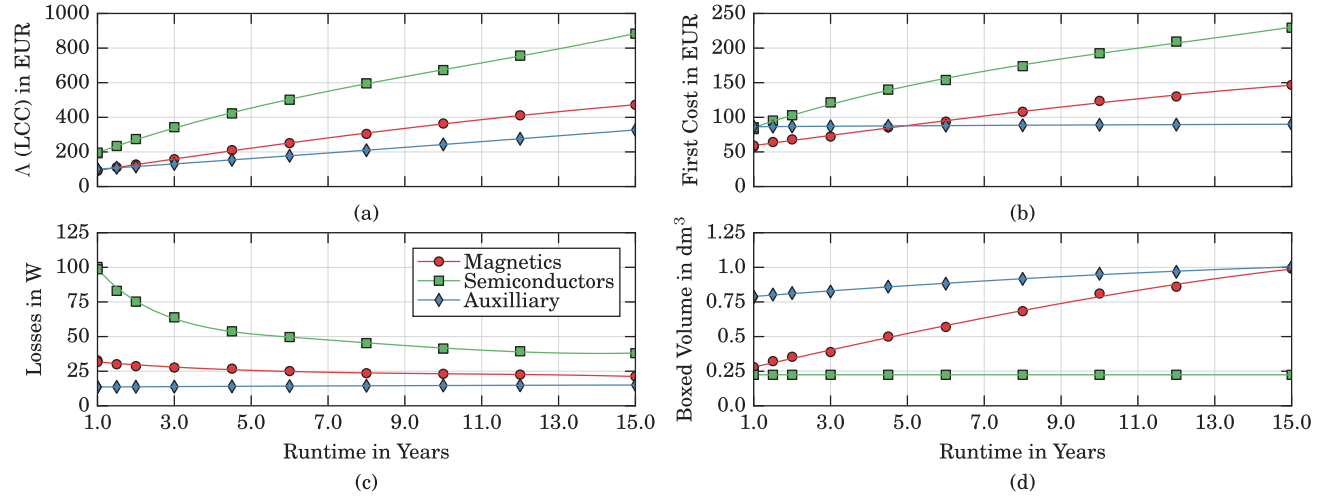


Fig. 16. Spline interpolated results of the numerical optimization (markers) for the semiconductors (incl. heatsinks), magnetics and remaining components (e.g. fans, gate drivers, PCBs, DSP/FPGA, capacitors, EMI filter) of the circuit shown in Fig. 4. Nanocrystalline cores with helical windings are used for all magnetic components as they offer the best performance in this case, cf. Fig. 13. Plot (a) shows the optimal LCC $\Lambda(t_r)$, (b) shows the corresponding optimal first cost $\sum(t_r)$, (c) the losses occurring in the components and (d) their boxed volume. It can be seen that the semiconductors contribute about half of the first cost and losses and hence the life cycle cost, but only ≈ 10% to 20% of the total converter volume.

IV. Hardware Prototype

Using the optimization results presented in the previous chapter, an 8 kW, prototype IAF rectifier with a switching frequency of f_{sw} = 27 kHz, according to the specifications given in Table I, was implemented. A picture of the hardware is shown in Fig. 17 and its main components are listed in Table II.

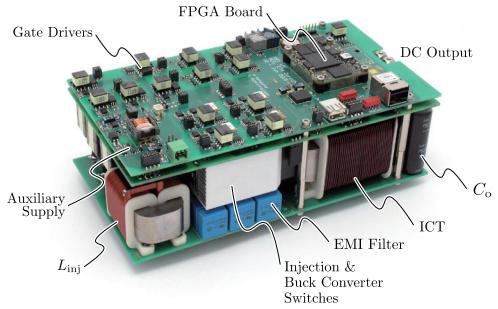
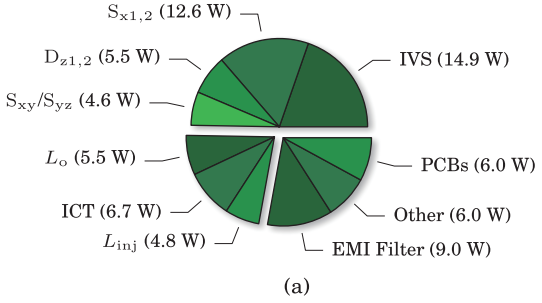


Fig. 17. Picture of the hardware prototype, measuring 220mm x 118mm x 77mm (8.66 in x 4.65 in x 3.03 in). This results in a power density of 4.0 kWdm^{-3} (65W in^{-3}).

TABLE II
Components Used in the Hardware Prototype

	L_{inj}	ICT	L_o
Core	F3CC-6.3	F3CC-25	F3CC25
Wire	1 x 4 mm	1 x 6 mm	2.4 x 6 mm
Turns	52	36:36	30
Inductance	750 µH	3 mH	300 µH
Volume	88 cm^3	245 cm^3	249 cm^3
Losses	4.8 W	6.7 W	5.5 W
$S_{x\bar{k}}$, $S_{\bar{k}x}$	C2M0025120		P_{loss} = 1.7 W
$S_{\bar{k}y\bar{k}}$	C2M0080120		P_{loss} = 0.8 W
S_{xy}, S_{yz}	C2M0080120		P_{loss} = 2.3 W
S_{x1}, S_{x2}	C2M0025120		P_{loss} = 6.3 W
D_{z1}, D_{z2}	C4D40120D		P_{loss} = 2.7 W

A more detailed distribution of the calculated component losses for the implemented prototype at nominal operating conditions and the corresponding component volumes are shown in Fig. 18. About 50% of the total losses occur in the semiconductors. Core and winding losses in the main magnetic components L_o, *ICT* and L_{inj} account for ≈ 22% of the total losses. The remaining 28% occur in the EMI filter, the PCB tracks, and other elements such as fans, gate drivers, FPGA, current sensors etc. Measurement results of the prototype converter are presented in the following.



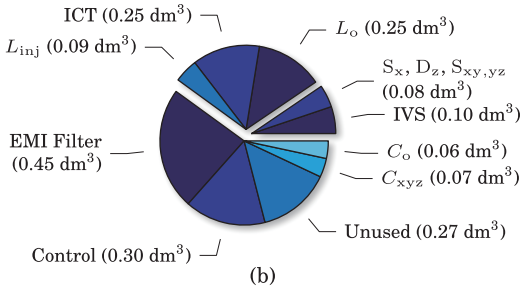


Fig. 18. The calculated distribution of losses for the selected design point at nominal operation is shown in (a), the corresponding component volumes are shown in (b). Category *other* includes fans, gate drivers, FPGA, ADCs, current sensors, auxiliary supply, etc.

A. AC Input Currents

In Fig. 19 measurement results of the prototype rectifier operated at full load and nominal input voltage are shown. Sinusoidal input currents with slight distortions at the mains voltage sector boundaries result as expected from simula-

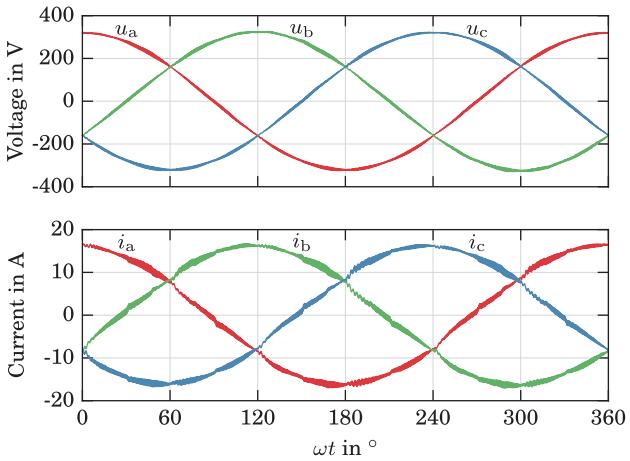


Fig. 19. Measurement results with the converter operating at nominal conditions and full output power, i.e. P = 8 kW, U_1 = 230 V$_{rms}$ and U_{pn} = 400 V. Note that phase quantities a and c were measured directly, phase b was recreated numerically as $u_b = -u_a - u_c$ and $i_b = -i_a - i_c$.

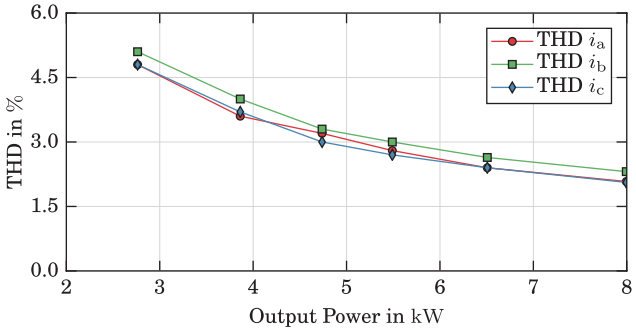


Fig. 20. Total harmonic distortion (THD) values of the rectifier's mains input line currents as a function of output power for nominal input and output voltages, measured using a *Yokogawa WT 3000* power analyzer.

tion. The measured total harmonic distortion of the mains input currents as a function of the dc output power is shown in Fig. 20.

B. Efficiency

A comparison of the rectifier's calculated and measured efficiency as a function of dc output power is shown in Fig. 21. The solid lines show the calculated efficiency for 400V and 380V output voltage, while the round and triangular markers show measurements taken with a *Yokogawa WT 3000* power analyzer. Additionally three efficiency measurements were taken based on a direct measurement of the converter's losses using a calorimeter which closely match the values obtained by the electrical measurement.

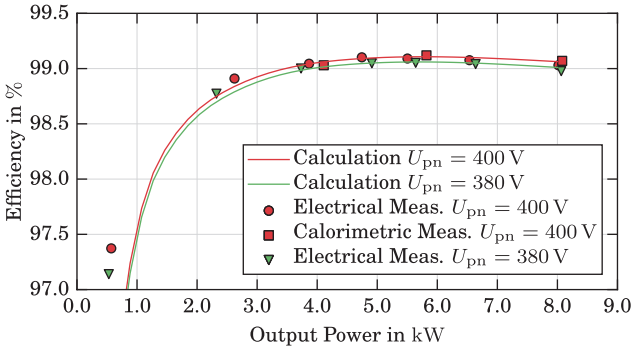


Fig. 21. Comparison of measured and calculated converter efficiencies for two different dc output voltages U_{pn}. The electrical efficiency measurements were performed with a *Yokogawa WT 3000* power analyzer. For U_{pn} = 400V additional measurements were done using a calorimeter. All measurements were taken at nominal ac input voltage U_l = 230V_{rms} and an ambient temperature of 30 degrees C.

C. ICT Current Balance

As written in Section II-C unsymmetries in the interleaved buck converter lead to an unbalance of the ICT currents i_{o1} and i_{o2} which create a dc offset in the ICT's magnetizing current i_m. Measurement results of the buck converter output voltages u_{Dz1}, u_{Dz2}, the ICT currents and the derived magnetizing current are shown in Fig. 22. Note that no active controller was used to balance i_{o1} and i_{o2}, resulting in a peak magnetizing current of 0.73A and average value of 0.42 A. This corresponds to a peak core flux density of ≈ 460mT which is far below the core material's saturation flux density of 1.2 T.

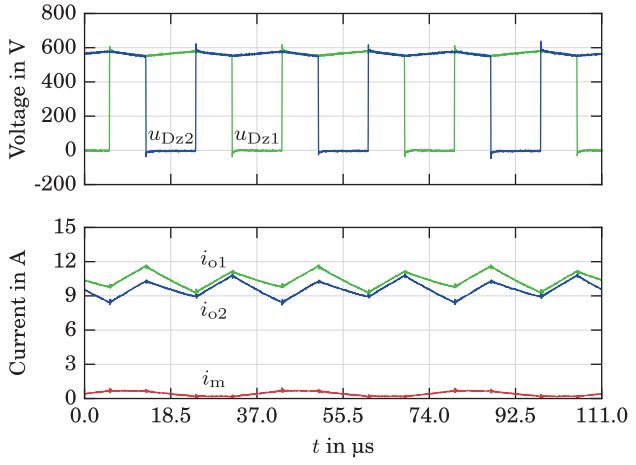


Fig. 22. Measurement of the interleaved buck converter output voltages u_{Dz1} and u_{Dz2}, the ICT currents i_{o1} and i_{o2} and the calculated ICT magnetizing current i_m for converter operation with nominal power at $\omega t \approx 0°$, i.e. at the peak of the six-pulse voltage u_{xz} (cf. Fig. 3) with a peak value of $i_{m,max}$ = 0.73 A.

D. Conducted EMI

A two stage EMI filter with a reactive power consumption of ≈ 4% of the rectifiers output power rating has been implemented. Its structure is shown in Fig. 23 and the values of all components are listed in Table III. However, a detailed analysis of the filter and of its design process is out of the scope

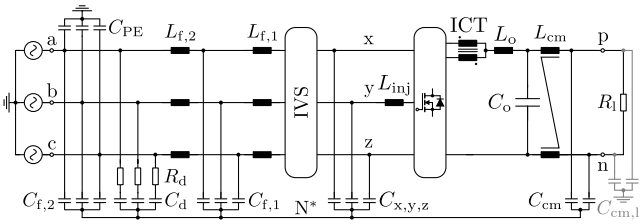


Fig. 23. Schematic of the implemented EMI filter with two combined CM/DM filter stages $L_{f,1}$, $C_{f,1}$ and $L_{f,2}$, $C_{f,2}$ at the ac input and an additional CM filter stage L_{cm}, C_{cm} at the dc output. The component values used in the prorotype are listed in Table III.

TABLE III
EMI FILTER COMPONENTS

C_{xyz}	4.4 µF	2 x 2.2 µF Epcos B32923, X2 in parallel
$L_{f,1}$	22 µH	PQ26/25, 10 turns, 1 x 4mm wire
$C_{f,1}$	2.3 µF	5 x 470 nF Epcos B32922, X2 in parallel
$L_{f,2}$	15 µH	Würth Elektronik 7443641500
$C_{f,2}$	1.4 µF	3 x 470 nF Epcos B32922, X2 in parallel
C_d	0.9 µF	2 x 470 nF Epcos B32922, X2 in parallel
R_d	4.7 Ω	4 x 1W 1218 SMD Thick Film resistors
C_{PE}	47 nF	Epcos B3202, Y2, connected to case
L_{cm}	≈ 200 µH	Vacuumschmelze W424, 5 turns, 2.5mm wire
C_{cm}	130 nF	4 x 33 nF MLCC in parallel

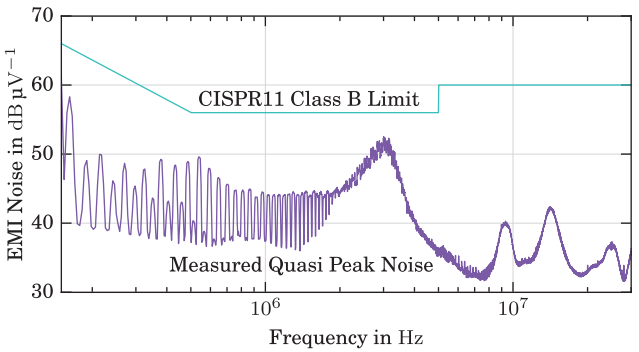


Fig. 24. Measured quasi-peak conducted EMI noise emission and corresponding CISPR11 class B limit for the 150 kHz to 30 MHz range with a bandwith of 9 kHz, measured in 4 kHz steps.

of this paper. Measurement results of the conducted EMI noise spectrum, using the quasi-peak detector, are shown in Fig. 24 together with the CISPR11 class B limit for the 150 kHz to 30MHz range.

V. Conclusion

This paper describes a life cycle cost driven optimization process were not only the first cost of a converter, but also the capital equivalent worth of the energy dissipated during the system's service life is considered. This allows the selection of optimal components, such as switches, inductors, transformers, etc., which achieve minimal cost for a given application, run time and switching frequency. By sweeping over a range of suitable switching frequencies a cost optimal converter system can then be found.

As an example an 8kW buck-type three-phase interleaved Integrated Active Filter rectifier for 380V dc distribution systems in data center and telecommunication applications is designed. Using state-of-the-art SiC MOSFETs and nanocrystalline cores a design with a power density of $4kWdm^{-3}$ and an efficiency of 99% results. Measurement results taken on a hardware prototype verify the validity of the employed models.

However, the cost driven optimization process is not only useful for data center applications with continuous operation, but could also be used in other applications were the system operates only for a relatively short period of time. For example in an on-board charger of a plug-in hybrid vehicle, which is used only once or twice a day for 1 to 2 hours, the first cost. Similarly the cost of weight and volume is expected to have significant impact on power electronic systems in aircraft, where weight has an impact on the vehicle's fuel consumption and hence on the life cycle cost. This is expected to lead to cost optimal systems with a higher switching frequency, higher power density and lower efficiency. In such cases an equivalent first cost, including weight and/or volume and the cost of conversion losses can still be used to compare, optimize and select components, circuit topologies and converter systems achieving minimal life cycle cost.

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