# Revisiting Stability Criteria for DC Power Distribution Systems Based on Power Balance

Zhicong Huang, Siu-Chung Wong, and Chi K. Tse

***Abstract*—Single-input-multiple-load converter systems sharing a common input DC voltage bus is becoming popular in DC power distribution. Due to the convenience of using conventional voltage-source systems for connecting a common bus voltage with multiple downstream loads, the same configuration is often adopted for current-source systems, where design optimization can be achieved without an intermediate (bus) voltage regulator. However, the stability of such cascaded current-source systems is still relatively unexplored or incomplete, though the associated basic circuit theory has been well established. In this paper, steady-state operating points are obtained by applying power balance between the current-source output converter and the downstream converters. The incremental change of the input power versus the input impedance of the downstream converters is derived. The stability of such current-source converter systems is re-visited using an impedance-based approach. A general set of impedance-based stability criteria is developed and experimentally verified by a DC bus system consisting of a current source output converter and two PWM power converters.**

***Index Terms*—DC bus system, DC current source converter, stability criterion.**

## I. Introduction

IMPEDANCE-BASED stability criterion [1] has been applied for the voltage-source converter system consisting a voltage-source converter and a load converter connected in cascade, with a regulated voltage being the interface between the source and load converters. Based on a small-signal model, the Middlebrook stability criterion states that the system is stable if the following conditions are satisfied:

V1 The source converter having an output voltage $V_o$ and output impedance $Z_s$ is stable under no load condition.

V2 The load converter having an input impedance $Z_l$ is stable when connected to an ideal voltage source $V_o$, and

V3 (a) aggressively, $T_v = Z_s / Z_l$ satisfies the Nyquist stability criterion, or

V3 (b) conservatively, $|T_v| \ll 1$.

Cascaded-converter systems with an inverter of highimpedance current source output connected to the lowimpedance input of a grid voltage have been studied by Sun [2] who identified the systems as current-source systems and presented a stability criterion as a dual to that given in [1]. Specifically, this current-source system is stable if the following conditions are satisffied:

C1 The source converter having an output current $I_o$ and impedance $Z_p$ is stable under no load condition.

C2 The load converter having an input impedance $Z_l$ is stable when connected to an ideal current source $I_o$, and

C3 (a) aggressively, $T_c = Z_l / Z_p$ satisfies the Nyquist stability criterion, or

C3 (b) conservatively, $|T_c| \ll 1$.

The above stability criteria have been applied to DC distributed power systems with multiple sources and loads where the numbers of sources and loads are changing dynamically [3]. Apart from verifying condition V1 or V2 as appropriate for each converter, the system's minor loop gain $T_v$ (referred to in V3) has been extended to include every impedance (or admittance) of the system given by

$$T_v = \frac{\text{parallel of all } m \text{ source impedances}}{\text{parallel of all } n \text{ load impedances}} \quad (1)$$

$$= \frac{\sum_{j=1}^{n} \frac{1}{Z_{lj}}}{\sum_{j=1}^{m} \frac{1}{Z_{sj}}}. \quad (2)$$

Likewise, similar modification has been proposed for the current-source system. However, only the usual voltage-source systems are studied in detail [3] due to the fact that such voltage-source systems, having a dominating regulated bus voltage, are the only systems considered in most DC distribution systems.

To see the potential of applications of current-source systems, we consider wireless power transfer systems here. Wireless power transfer systems are often designed with an inductive power transfer (IPT) converter cascaded with a downstream pulse-width modulation (PWM) converter to achieve a high overall system efficiency under line or load variation [4]-[8]. The series-series compensated IPT (SSIPT) converters [4]-[7] are among the most power efficient IPT converters [9], [10]. Operating at its power efficient point, the SSIPT converter can provide a constant output current which is independent of load variations [9], [10]. In this current-source system, no *voltage regulation* is needed at the interface of the cascaded power converters. Therefore, an equivalent source converter of the system has high output impedance which makes it difficult to meet the Middlebrook stability criterion applied to a voltage-source system that a stable cascaded converter should have its upstream power converter having a

Manuscript received March 16, 2017. This work was supported by Hong Kong Polytechnic University Grant G-YBKC.

The authors are with the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Kowloon, Hong Kong, China (e-mail: forward.huang@gmail.com, enscwong@polyu.edu.hk, encktse@polyu.edu.hk).

Digital Object Identifier 10.24295/CPSSTPEA.2017.00009

substantially lower output impedance compared to the input impedance of its downstream power converter [1], [11], [12]. However, the impedance-based stability criterion for current-source systems presented by [2], [3] is not general enough for applications with multiple loads, as shown in Fig. 1. In such a system, the converters can share either a common voltage bus or a common current loop. Additionally, as will be shown in Section III, the definition of either a voltage-source system or a current-source system is still unclear for the configurations shown in Figs. 1(b) and (c), making direct application of the Middlebrook stability criterion and its dual rather difficult.

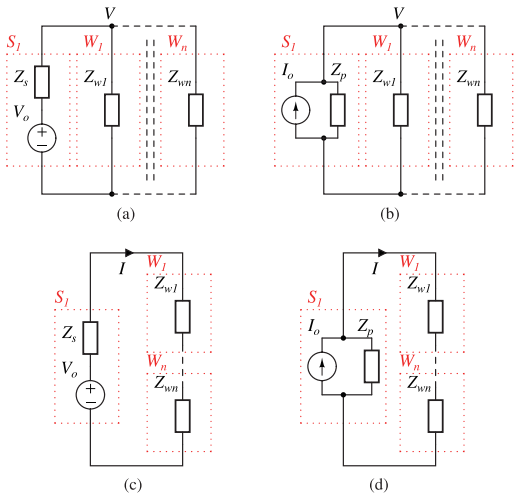



Fig. 1. Impedance-based models of a source converter $S_1$ and $n$ load converters $W_1,\cdots,W_n$. Components inside the dotted line blocks are the small-signal-equivalent circuits of the converters. (a) Voltage-source converter $S_1$ sharing a common voltage with $n$ load converters. (b) Current-source converter $S_1$ sharing a common voltage with $n$ load converters. (c) Voltage-source converter $S_1$ sharing a common current with $n$ load converters. (d) Current-source converter $S_1$ sharing a common current with $n$ load converters.

In this paper, we analyze the general cascaded converter system by considering an equivalent model as seen by one of the DC-DC converters and apply power balance to gain insights into the difference between a voltage-source system and a current-source system. A general set of impedance-based criteria of stability will be developed as a generalization of the criteria presented in [2], [3]. The set of stability criteria developed from this simple model will be verified experimentally by a cascaded SSIPT-PWM converter system. A stable prototype of independently controlled IPT and PWM converters will be demonstrated.

To differentiate a voltage-source system from a current-source system, we can consider the DC steady-state model of the system by referring to Fig. 1 with all small-signal variables being replaced by their DC counterparts. For brevity, we can start with $n = 1$, where Fig. 1(a) becomes identical to Fig. 1(c) and Fig. 1(b) becomes identical to Fig. 1(d). The DC operating circuit for $n = 1$ is shown in Fig. 2, where the source and load share the same voltage bus $V$ and current loop $I$.

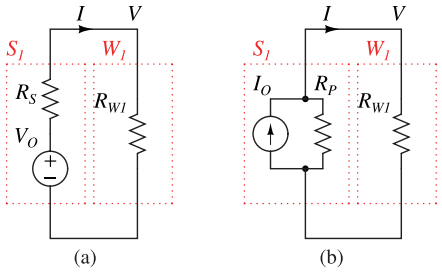



Fig. 2. DC operation models of a source converter $S_1$ and a load converter $L_1$. Components inside the dotted line blocks are the DC equivalent circuit of the converters. (a) Voltage source converter $S_1$ sharing a common voltage with a load converter. (b) Current-source converter $S_1$ sharing a common current with a load converter.

## II. Steady-State Operating Points from the Viewpoint of Power Balance

Fig. 1 shows equivalent small-signal models of closed-loop converters. We assume that the converters are stable, operating safely within their voltage, current and power ratings, and can be perfectly controlled to their DC operating points with a finite bandwidth $f_{BW}$. In this sense, the voltage-source converter $S_1$ has been stably *biased* to its DC operating point as an ideal voltage source $V_o$ with a small source resistance $R_S$, which represents the resistance of interconnection as well as the intentional output resistance from control algorithms such as the droop controller. The DC operating circuit shares the same circuit structure as shown in Fig. 1, with the corresponding DC variables being represented with uppercase letters and subscripts as appropriate. Likewise, we have an ideal DC current source $I_o$ and its large parallel output resistance $R_P$ for a current-source converter.

The $n$-load converters are normally regulated with a constant output voltage or current. When such near lossless converters are connected with resistive loads, their inputs will behave as a near perfect constant power sink $P_{Wi} = V_{Wi} I_{Wi}$, where $i = 1, \cdots, n$. Obviously, the same $P_{Wi}$ can be biased at different points on a constant power curve, such as points A, B or C, as shown in Fig. 3. It should be noted that point A has a DC resistance of $R_A = \dfrac{V_A}{I_A}$ while its incremental resistance on the constant power curve is $-R_A$, which should equal $Z_{wi}$ within $f_{BW}$. Obviously, to meet the output power requirement of $P_{Wi}$, the load converter $W_i$ can be biased anywhere on the power curve. The choice of biasing at a point on the power curve will be decided by the practical requirements of meeting the voltage and current ratings by designing a suitable $R_{Wi}$ and the regulation bandwidth dictates the associated $Z_{wi}(f) = -R_{Wi}$ with $f < f_{BW}$.

With reference to Fig. 2(a), the power output from $S_1$ should be identical to the power input to $W_1$. The power $P_1 = P_{W1}$ feeding to $R_L = R_{W1}$ can be plotted as shown in Fig. 4, which gives the expected maximum power transfer when $R_L$ is equal to $R_S$. Moreover, an intended input power $P_1$ can be biased at two load resistances $R_{Lx}$ and $R_{Ly}$ such that $R_{Lx} < R_S$

$< R_{Ly}$. For a native source resistance $R_S$, operating at $R_{Ly}$ will be more efficient than that at $R_{Lx}$. However, if $R_S$ is a virtual equivalent resistance as a result of application of some control algorithms which are common in some AC or DC voltage bus systems [16], there would not be much difference in efficiency between the operation points $R_{Lx}$ and $R_{Ly}$. It can be observed that a small increment of $R_L$ at $R_{Lx}$ acquires a higher $P_1$, while a small increment of $R_L$ at $R_{Ly}$ corresponds to a lower $P_1$. This gives an intuitive explanation on the requirement that the load $R_{Ly}$ is stable when it is connected to an ideal voltage source as the two systems give near identical $\frac{\delta P_1}{\delta R_L}$, especially when $R_L \gg R_S$. It can be observed in Fig. 4 that the load converter $W_1$ operating with $R_{Ly}$, i.e., $R_L > R_S$, will become unstable when it is operating near $R_S$ and even worse for $R_L \le R_S$ as $\frac{\delta P_1}{\delta R_L}$ will deviate significantly from that operating with $R_{Ly}$ [17]. It is obvious that converter $W_1$ switching operating points from $R_{Ly}$ to $R_{Lx}$ should have its feedback circuit redesigned.

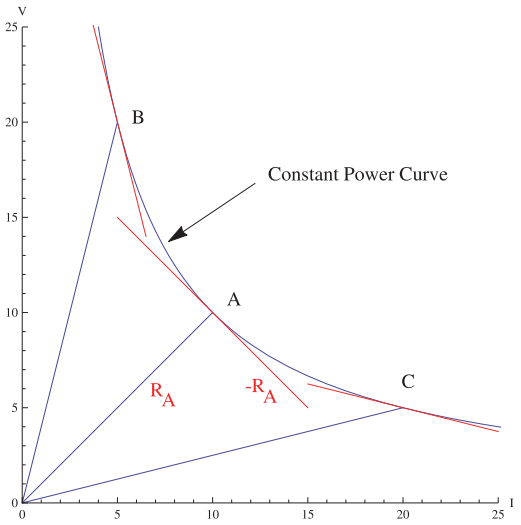



Fig. 3. Constant power curve with biasing points A, B and C.

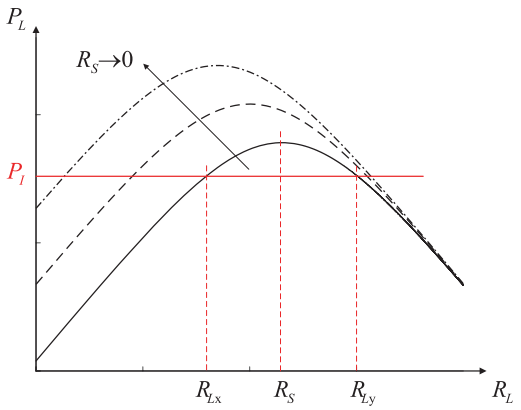



Fig. 4. Power transfer characteristic of a voltage-source system.

Likewise, with reference to Fig. 2(b), a current-source system has a power transfer characteristic as shown in Fig. 5. It is similar to Fig. 4 except that the current-source system is normally operating at $R_{Lx}$ while for a voltage-source system, it is normally operating at $R_{Ly}$. Based on our previous analysis on voltage-source systems, we can obtain a corresponding set of results using the *duality principle*. Specifically, for a voltage-source system, $\frac{\delta P_1}{\delta R_L}$ at $R_{Lx}$ is proportional to $R_{Lx}$, while for a current source system $\frac{\delta P_1}{\delta R_L}$ at $R_{Ly}$, it is inversely proportional to $R_{Ly}$. This again gives an intuitive explanation for the requirement that the load $R_{Lx}$ is stable when it is connected to an ideal current source as the two systems give near identical $\frac{\delta P_1}{\delta R_L}$, especially when $R_L \ll R_P$. Similarly, it can be observed from Fig. 5 that the load converter $W_1$ operating at $R_{Lx}$, i.e., $R_L < R_P$, will become unstable when it is operating near $R_P$ and even worse for $R_L \ge R_P$. It is also obvious that converter $W_1$ switching operation points from $R_{Lx}$ to $R_{Ly}$ should have its feedback circuit redesigned.

It can be concluded from Figs. 4 and 5 that for the source-converter having output resistance $R_O$ and the load converter having input resistance $R_L$, the system is considered as a voltage-source system if $R_L \gg R_O$, otherwise it must have $R_L \ll R_O$ and the system is regarded as a current-source system. Meanwhile, for $f < f_{BW}$, $R_L \gg R_O$ is equivalent to $|Z_l(f)| \gg |Z_o(f)|$ and $R_L \ll R_O$ is equivalent to $|Z_l(f)| \ll |Z_o(f)|$ that these two conditions are subsets of the conservative conditions V3(b) of the Middlebrook stability criterion and C3(b) of the dual of the Middlebrook stability criterion.

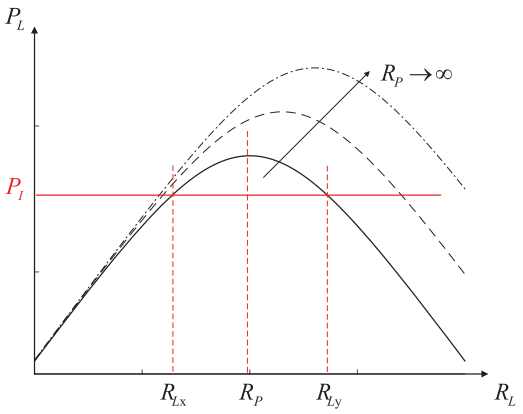



Fig. 5. Power transfer characteristic of a current-source system.

## III. Current-Source or Voltage-Source Driven Subsystem of Single-Source Multi-Load Systems

In Section II, the single-source single-load system is readily distinguished as being a voltage-source system or a current-system by considering the relative magnitude of the source and load resistances at DC operation. In Fig. 6, two loads $W_1$ and $W_2$ are assumed independently controlled, or otherwise, they can be combined into a single load such that the system

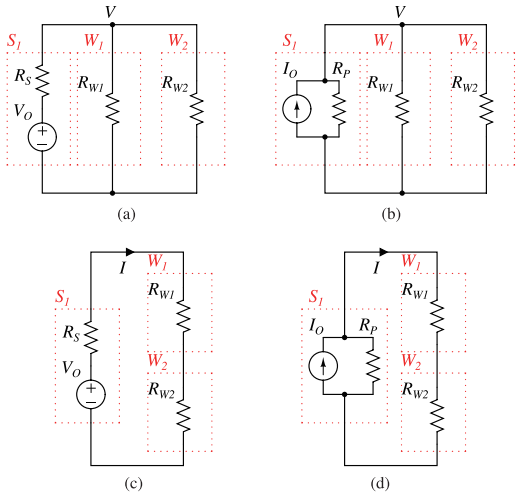



Fig. 6. DC circuit models of four possible configurations consisting of a source converter $S_1$ and two load converters $W_1$ and $W_2$.

is equivalent to a single-load system as shown in Fig. 2(a) or 2(b). To distinguish between a voltage-source system and a current-source system, we assess the converter subsystems individually. It can be readily observed from Fig. 6(a) that as long as

$$R_S \ll (R_{W1} || R_{W2}), \tag{3}$$

we have

$$(R_S || R_{W2}) \ll R_{W1}, \text{ and} \tag{4}$$

$$(R_S || R_{W1}) \ll R_{W2}. \tag{5}$$

For $S_1$, an equivalent resistance of $R_L = (R_{W1} || R_{W2})$ is being driven. Equation (3) identifies a voltagep-source system for $S_1$. Likewise, (4) and (5) identify a voltage-source system for $W_1$ and $W_2$. They can be designed stable by following the Middlebrook stability criterion [1] for their individual equivalent circuits. Similar arguments apply to Fig. 6(d) with respect to a current-source system with $R_P \gg (R_{W1} + R_{W2})$ and each load is designed to be stable when it is connected to an ideal current source. The results can be readily generalized to an $n$-load voltage-source system with $R_S \ll R_{W1} || R_{W2} || \cdots || R_{Wn}$ and an $n$-load current-source system with $R_P \gg (R_{W1} + R_{W2} + \cdots + R_{Wn})$. Common properties of systems represented by Fig. 6(a) and (d) are:

- there is a dominant source which regulates either the bus voltage or current of the system, and
- each load shares the s*ame* system defined by the source converter, i.e., a voltage- or a current-source system.

The stability of these well defined voltage-source or current-source systems can be easily assessed by applying either V1 to V3, or C1 to C3, to each of the source or load converters, or simply (2) or its dual [3].

The systems shown in Figs. 6(c) and (d) are less attractive than those shown in Figs. 6(a) and (b) which share a common voltage bus for easy connection or disconnection of loads. The identification and possible modification of the voltage- or current-source system shown in Fig. 6(b) will be developed as follows. For the current-driven system shown in Fig. 6(b), by applying Middlebrook stability criterion [1], [2] to each of the subsystem, the source $S_1$ is stable if C1 and the conservative condition C3(b) (solely needed for $f < f_{BW}$) are satisfied, which is equivalent to

$$R_P \gg (R_{W1} || R_{W2}), \tag{6}$$

the load $W_1$ should assume being driven by a current source. If so, we have

$$(R_P || R_{W2}) \gg R_{W1} \tag{7}$$

and the load $W_2$ should assume being driven by a current source. If so, we have

$$(R_P || R_{W1}) \gg R_{W2}, \tag{8}$$

It can be observed from Fig. 5 that (7) and (8) cannot be satisfied simultaneously if $R_{W1}$ and $R_{W2}$ are of similar order of magnitude and both $W_1$ and $W_2$ are stable when they are connected to an ideal current source. Without loss of generality, let us assume that

$$R_{W1} \ll R_{W2}, \tag{9}$$

such that (7) is satisfied, i.e., subsystem $W_1$ can be stable if it is stable when connected to an ideal current source. Now, for subsystem $W_2$, (8) can never be satisfied, i.e., subsystem $W_2$ cannot be stable when it is designed to be driven by a current source. Fortunately, from (9) we have

$$(R_P || R_{W1}) \ll R_{W2}, \tag{10}$$

which satisfies V2 of subsystem $W_2$, as given in Figs. 2(a) and 5, i.e., subsystem $W_2$ can be stable if it is stable when it is connected to an ideal *voltage* source [1], where the parallel connection of the current source and resistance $(R_P || R_{W1})$ are regarded as its Thevénin's voltage source equivalent. Since from the load's perspective, Thevénin's voltage source and Norton's current source are interchangeable, this result is important in several respects:

1) Load $W_1$ is driven by a *current source*, as shown in Fig. 5, with the source resistance $(R_P || R_{W2})$.
2) Load $W_2$ is driven by a *voltage source*, as shown in Fig. 4, with the source resistance $(R_P || R_{W1})$.
3) The systems in Fig. 4 and Fig. 5 are equivalent in terms of the load stability criteria.
4) For the single-source two-load system, the design of subsystem $W_1$ which is assumed stable when connected to an ideal current source is different from that of $W_2$ which is assumed stable when connected to an ideal voltage source.
5) For the stable single-source two-load system, the power

level of subsystem $W_1$ will be much higher than that of subsystem $W_2$ when they are controlled independently. To have the freedom of operating at any power level, the control of the subsystems must be well coordinated. In such a case, they reduce to a single-load system.

In summary, the lowest (highest) resistance of the system in Fig. 6(b) (Fig. 6(c)) acquires most of the power from the current (voltage) source and converts the current (voltage) source into an equivalent voltage (current) source for driving the other load.

The identification of current or voltage driven load subsystems can be readily generalized to an $n$-parallel-load current-source system with the condition that $R_P \gg (R_{W1}||\cdots||R_{Wn})$, $(R_P||R_{W2}||\cdots||R_{Wn}) \gg R_{W1}$ and $(R_P||R_{W1}) \ll R_{Wi}$ for $i = 2\cdots n$, where $W_1$ is stable when it is connected to an ideal current source, and $W_i$ ($i = 2\cdots n$) is stable when connected to an ideal voltage source. Similarly, it can be generalized to an $n$-series-load voltage-source system with the condition that $R_S \ll (R_{W1}+\cdots+R_{Wn})$, $(R_S+R_{W2}+\cdots+R_{Wn}) \ll R_{W1}$ and $(R_S+R_{W1}) \gg R_{Wi}$ for $i = 2\cdots n$, where $W_1$ is stable when connected to an ideal voltage source, and $W_i$ (i = $2\cdots n$) is stable when connected to an ideal current source.

The stability of each subsystem can thus be assessed by applying the source system identified. The system is stable when all subsystems satisfy the individually identified Middlebrook stability criterion or its dual.

Similarly, for the system shown in Fig. 7(b), $W_1$ should be designed for a current source system and satisfies C2 and C3 with

$$T_{cW_1} = \left(\sum_{j=1}^{n} \frac{1}{Z_{sj}}\right) Z_{w1}. \tag{11}$$

For each voltage-source converter $S_k$, conditions C1 and C3

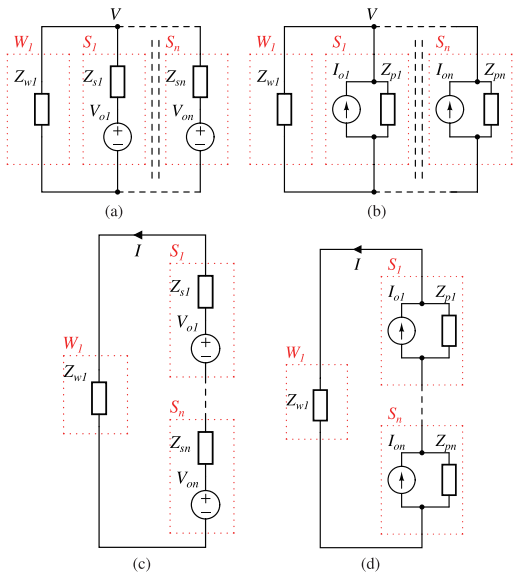



Fig. 7. Impedance-based models of a load converter $W_1$ and $n$ source converters $S_1,\cdots, S_n$.

should be satisfied with

$$T_{cS_k} = Z_{sk}^{-1}\left(\frac{1}{Z_{l1}} + \sum_{j=1,j\neq k}^{n} \frac{1}{Z_{sj}}\right)^{-1}. \tag{12}$$

## IV. Multi-Source Systems

The circuit for multi-source systems is represented in Fig. 7 by direct translation from Fig. 1, where the source $S_1$ is considered as load and the loads $W_1, \cdots, W_n$ are considered as sources $S_1, \cdots, S_n$. Since the circuits of Figs. 7(a) and (d) are dual, and so are the circuits of Figs. 7(b) and (c), it is suffice to consider the stability criteria for the circuits of Figs. 7(a) and (b).

In Fig. 7(a), if the voltage-source converters are active current-sharing converters [16], they are dependent converters and should be considered as a single voltage converter whose stability should be assessed according to the control algorithm used. The overall stable converter can be combined as a single voltage converter. If they are independent converters, the stability can be assessed using the approach described in Section III from the perspective of each converter and using the appropriate stability criterion of either V1 to V3, or C1 to C3. Specifically, $L_1$ should be designed for a voltage-source system, satisfying V2 and V3 with

$$T_{vW_1} = \frac{1}{\left(\sum_{j=1}^{n} \frac{1}{Z_{sj}}\right) Z_{w1}}. \tag{13}$$

For each voltage-source converter $S_k$, conditions V1 and V3 with

$$T_{vS_k} = Z_{sk}\left(\frac{1}{Z_{w1}} + \sum_{j=1,j\neq k}^{n} \frac{1}{Z_{sj}}\right). \tag{14}$$

should be satisfied. It should be noted that if the Nyquist stability criterion on $T_{vW}{}^{1}$ of (13) and that on $T_{vS}{}^{k}$ of (14) are satisfied, then the Nyquist stability criterion on $T_v$ of (2) is satisfied. However, the converse may not be true.

It is also noted that for $n = 2$ and the system not being loaded by $W_1$, we have $T_{vS_1} = \frac{Z_{s1}}{Z_{s2}}$ and $T_{vS_2} = T_{vS_1}^{-1}$. Hence, the conservative condition V3(b) cannot be satisfied for each converter. Moreover, for multiple parallel voltage-source system, the output impedance, apart from being a source impedance, is also a load impedance of other participating voltage sources. In terms of stability, the output impedance of a voltage-source converter in a single source system can be designed with sufficient stability margin without any righthalf-plane zero. However, for a stable multiple voltage-source system, the output impedances should be designed without any right-half-plane zero.

## V. Illustrative Example: Single-Current-Source Two-Load System

### A. Inductive Power Transfer Converter

In this section, the single-source two-load system shown in Fig. 6(b) is selected for design and verification. As shown in the block diagram of Fig. 8, an IPT converter will be selected as $S_1$ which can operate with its most efficient configuration and has a current output. Two independently controlled DC-DC PWM converters $W_1$ and $W_2$ will be designed as load converters of the system. The source converter $S_1$ and load converters $W_1$ and $W_2$ have internal DC operation models shown in Fig. 6(b). $S_1$ has an equivalent resistance $R_P$ which takes into account the losses due to the IPT transformer windings, magnetic cores and electronic devices. Such an IPT converter normally has a switching frequency current ripple filtering capacitor $C_O$ which may pose constraints on the design of load converters $W_1$ and $W_2$. Using the extra stability conditions developed in Section III, subsystem $W_1$ should be designed stable when it is connected with a current-source input, while subsystem $W_2$ should be designed stable when it is connected with a voltage-source input. Hence, a stable system has $R_{W1} \ll (R_P \| R_{W2})$ and $R_{W2} \gg (R_P \| R_{W1})$. Moreover, to be qualified as a current-source converter, $R_P \gg (R_{W1} \| R_{W2})$.

Existing PWM converters as shown in Fig. 9 are mostly designed with a voltage-source input. The current-source-input converter can be derived from the basic voltage-source converter based on duality principle [15], as shown in Fig. 10. However, converters in Figs. 10(a) and (c) are not compatible with the filtering capacitor $C_O$ without appropriate modification. In this example, a higher power dual-boost converter and a lower power buck converter will be chosen as the two parallel load converters $W_1$ and $W_2$ respectively.

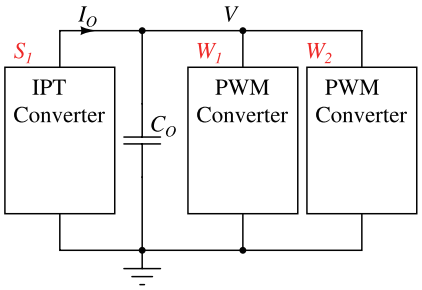



Fig. 8. Block diagram of the single-current-source two-load system.

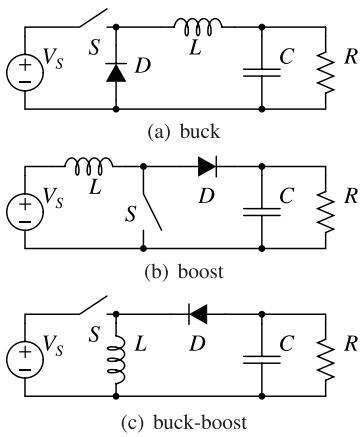



Fig. 9. Basic PWM voltage converters.

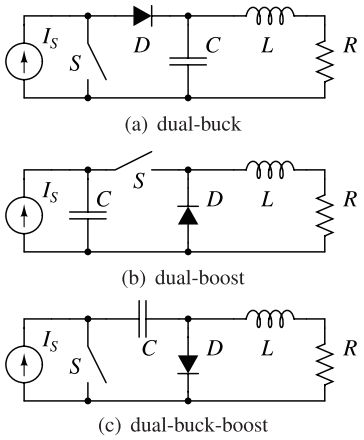



Fig. 10. Basic PWM current converters.

### B. Experimental Evaluation

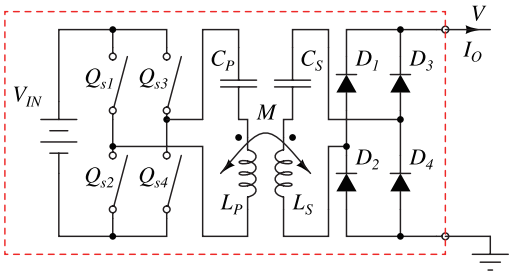
Fig. 11 shows the detailed schematics of subsystems $S_1$, $W_1$ and $W_2$ of the system shown in Fig. 8 with parameters given in TABLE I. The input voltage of $S_1$ is $V_{IN}$ = 30 V. Since the SSIPT converter operates at resonant frequency $f_S$, the output current is load-independent [4]-[7], [9]. The equivalent DC output current of the IPT converter can be estimated as $I_O = \frac{8}{\pi^2} V_{IN} \frac{1}{2\pi f_S M} = 2.05$ A.

In this system, $W_1$ regulates an output current of $I_{O1}$=3 A, driving a load $R_1$=3.75 Ω at a power of 33.75 W. Also, $W_2$ regulates an output voltage of $U_{O2}$ =15 V, driving a load $R_2$=35 Ω at a power of 6.43 W. Using the viewpoint of pow-

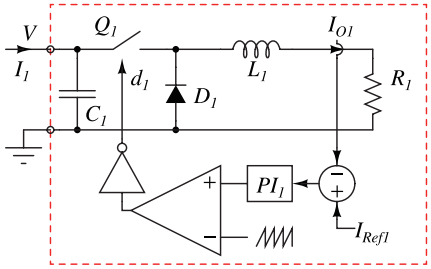
TABLE I
Parameters of Converters

| Parameters | Symbol | Value |
|---|---|---|
| Primary self inductance | $L_P$ | 31.46 $\mu$H |
| Secondary self inductance | $L_S$ | 33.02 $\mu$H |
| Mutual inductance | $M$ | 9.32 $\mu$H |
| Coupling coefficient | $k$ | 0.289 |
| Primary compensation capacitor | $C_P$ | 19.73 nF |
| Secondary compensation capacitor | $C_S$ | 18.8 nF |
| Switching frequency | $f_S$ | 202 kHz |
| Inductance | $L_1$ | 2 $m$H |
| Capacitance | $C_1$ | 470 $\mu$H |
| Proportion Constant | $K_{p1}$ | 0.04 |
| Integration Constant | $K_{i1}$ | 0.01 |
| Inductance | $L_2$ | 2 $m$H |
| Capacitance | $C_2$ | 470 $\mu$H |
| Proportion Constant | $K_{p2}$ | 0.04 |
| Integration Constant | $K_{i2}$ | 0.01 |

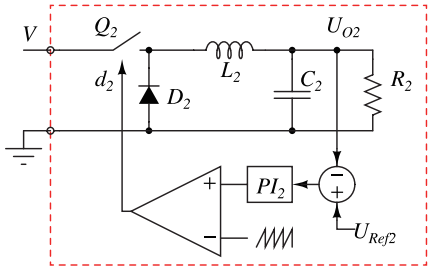
er balance and ignoring the power loss of the converters, the bus voltage can be estimated using $VI_O$=(33.75+6.43) W as $V$=19.6 V. The DC input equivalent resistances of the converters on the voltage bus $V$ are $R_{W1}$=11.4 Ω (21.1 dBΩ) and $R_{W2}$=59.8 Ω (35.5 dBΩ). These resistances should guarantee $R_{W1} \ll (R_P \parallel R_{W2})$ and $R_{W2} \gg (R_P \parallel R_{W1})$. The converters are built and their impedances are measured and given in the following subsections.




(a) IPT converter $S_1$




(b) dual-boost converter $W_1$




(c) buck converter $W_2$

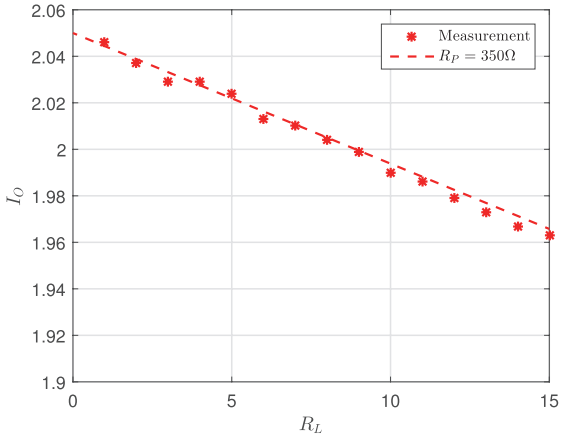
Fig. 11. Schematic of the single-current-source two-load subsystems.

### C. Output Resistance of the SSIPT Converter

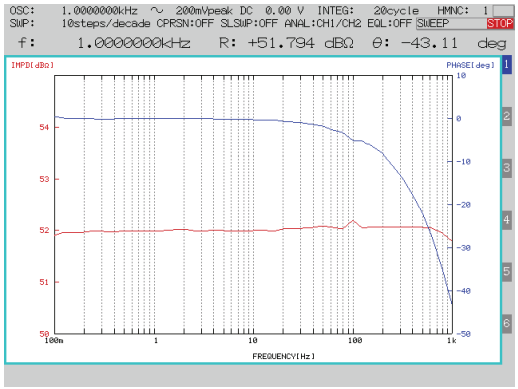
Fig. 12(a) shows measured steady-state output current $I_S$ versus load resistance $R_L$ of $S_1$. The low-frequency output transfer function can be represented by a Norton equivalent circuit with a parallel connection of current $I_O$=2.05 A and resistance $R_P$=350 Ω. Fig. 12(b) shows the small signal output impedance of $S_1$. With a bandwidth from 0 Hz to 1 kHz, $S_1$ should be stable driving an impedance lower than 50 dBΩ .

### D. Input Resistance of Load Converters

Measured bus voltage versus input current of the two PWM converters are shown as data points marked as '*'




(a)




(b)

Fig. 12. Output characteristics of $S_1$. (a) Steady-state output current $I_O$ versus load resistance $R_L$. (b) Small signal response of output impedance.

in Fig. 13. The dotted lines are constant power curves of the converters. Small-signal impedances of the converters are also measured and shown in Fig. 14, where $W_1$ is stable when it is driven by an ideal current source with infinite impedance, and $W_2$ is stable when it is driven by an ideal voltage source with zero output impedance.

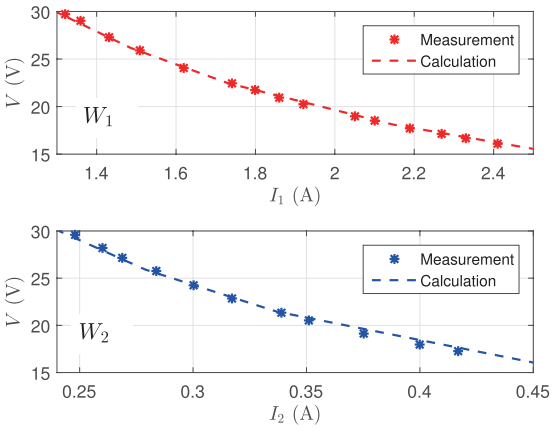
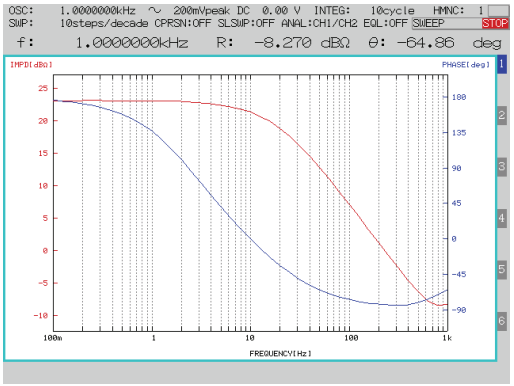
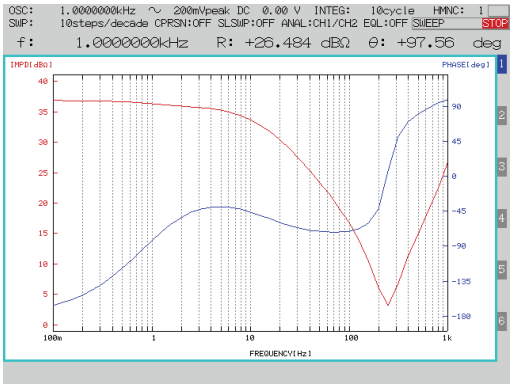



Fig. 13. Measured input VI steady-state characteristics of PWM converters $W_1$ and $W_2$. The dotted constant power curves fit well with the input powers 33.75 W of $W_1$ and 6.43 W of $W_2$.




(a) dual boost converter $W_1$




(b) buck converter $W_2$

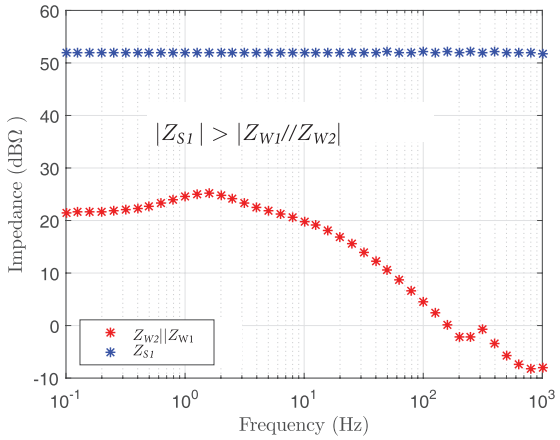
Fig. 14. Measured input impedances of PWM converters.

### *E. Stability Verification*

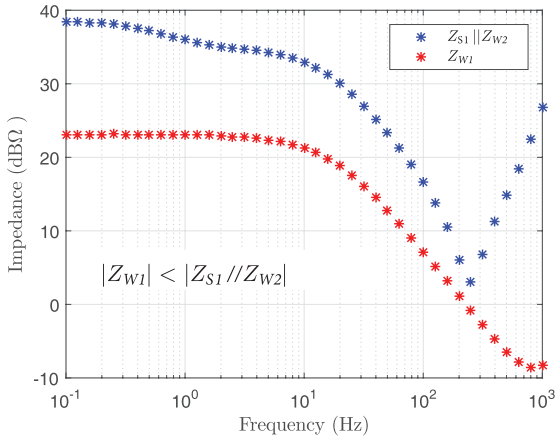
From the measurements taken in Section V-D, small-signal responses of the three converters are compared with emphasis of the local stability of each converter. Fig. 15 indicates that the converters are all locally stable within the measured bandwidth from 0 Hz to 1 kHz. To verify the system stability in general, step transient responses are measured.

The control of the subsystems are tested by maintaining power balance at steady state. Firstly, the control of $W_2$ is disabled by fixing $D_2$, such that it behaves as a resistor of $R_{L2}=\frac{R_2}{D_2^2}$. Then, $W_1$ is tested for its stability under closed-loop control. Fig. 16(a) shows the step response to a sudden reduction of the output reference current $I_{\text{Ref1}}$ of $W_1$. It shows that $R_{L1}$ decreases with decreasing output power, which coincides with the slope of the operating point $R_{L1}$ in Fig. 5.

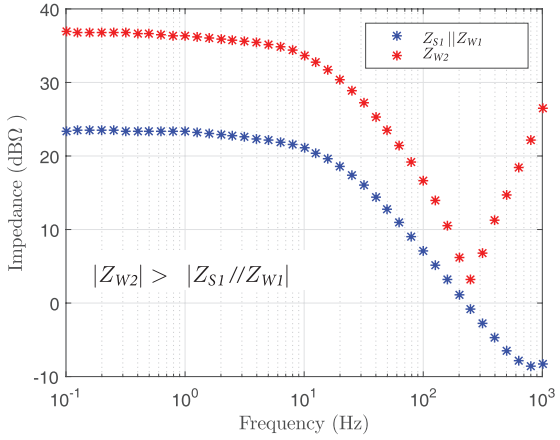
A similar experiment is done to test the stability of the control for $W_2$. The duty cycle of $W_1$ is disabled by fixing $D_1$, such that it behaves as a resistor of $R_{W1}=\frac{R_1}{D_1^2}$. $W_2$ is tested for its stability under closed-loop control. Fig. 16(b) shows the step response to a sudden reduction of the output voltage reference $U_{\text{Ref2}}$ of $W_2$. It shows that $R_{W2}$ increases with decreasing output power, which coincides with the slope of the operating point $R_{Ly}$ shown in Fig. 5.




(a) SSIPT converter $S_1$




(b) Dual boost converter $W_1$




(c) Buck converter $W_2$

Fig. 15. Measured magnitude of impedance ratio for verification of local stability within the bandwidth from 0 Hz to 1 kHz for (a) converter $S_1$ using C3(a), (b) converter $W_1$ using C3(a), and (c) converter $W_2$ using V3(a).

Finally, $W_1$ and $W_2$ are controlled independently. Fig. 17 shows the system in response to the cold start of $W_2$. It shows that the single-current-source-two-load system is stable, when the design is based on the generalized stability criteria developed in this paper.

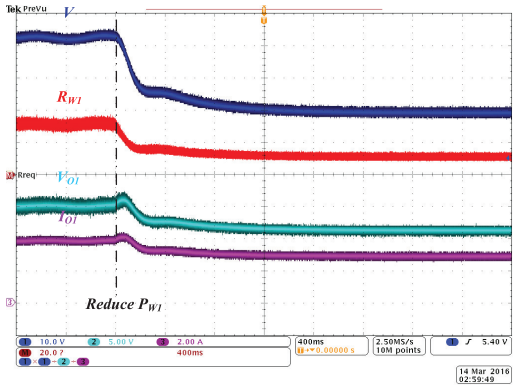



Fig. 16. Step response of the system. (a) Sudden reduction of the output reference current $I_{\text{Ref1}}$ of $W_1$ leading to a reduction of input voltage $V$, a characteristic of a current source system. Traces $U_{O1}$ and $I_{O1}$ are the output voltage and current of $W_1$. Trace $R_{W1}$, input resistance of $W_1$, is calculated based on measured data, using $R_{W1} = \dfrac{V^2}{U_{O1}I_{O1}}$, where the loss of the converter is ignored. (b) Sudden reduction of the output voltage reference $U_{\text{Ref2}}$ of $W_2$, leading to an increment of $V$, a characteristic of a voltage source system. Traces $U_{O2}$ and $I_{O2}$ are output voltage and current of $W_2$. Trace $R_{W2}$ is the input equivalent resistance of $W_2$, calculated using $R_{W2} = \dfrac{V^2}{U_{O2}I_{O2}}$, where the loss of the converter is ignored.

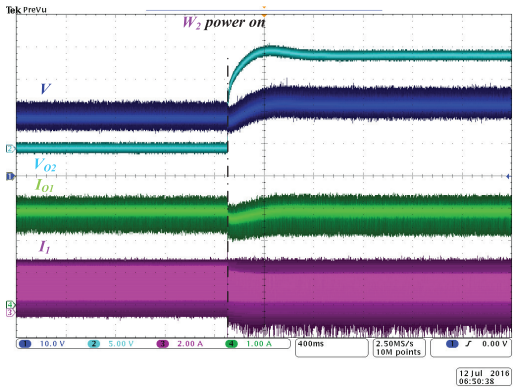



Fig. 17. System response to cold start of $W_2$. Traces $I_1$ and $I_{O1}$ are input and output currents of $W_1$. Traces $V$ and $U_{O2}$ are input and output voltages of $W_2$.

## VI. Conclusion

Impedance-based stability criteria for cascaded systems of converters is revisited in this paper. A more general set of criteria is presented here, which is suitable for the design of systems consisting of a single source cascaded with multiple load converters. This set of impedance-based stability criteria can be conveniently applied to a current output converter cascaded with multiple independently controlled current and voltage converters, such as those used in inductive power transfer systems.

## References

[1] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE IAS AnnualMeeting*, 1976, pp. 366-382.

[2] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Trans. Power Electron*., vol. 26, no. 11, pp. 3075-3078, Nov. 2011.

[3] X. Zhang, X. Ruan, and C. K. Tse, "Impedance-based local stability criterion for DC distributed power systems," *IEEE Trans. Circuit Syst. I, Reg. Papers*, vol. 62, no. 3, pp.916-925, Mar. 2015.

[4] O. Knecht, R. Bosshard, and J. W. Kolar, "High-efficiency transcutaneous energy transfer for implantable mechanical heart support systems," *IEEE Trans. Power Electron.,* vol. 30, no. 11, pp. 6221-6236, Nov. 2015.

[5] H. Li, J. Li, K. Wang, W. Chen, and X. Yang, "A maximum efficiency point tracking control scheme for wireless power transfer systems using magnetic resonant coupling," *IEEE Trans. Power Electron.,* vol. 30, no. 7, pp. 3998-4008, Jul. 2015.

[6] W. X. Zhong, and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4025-4034, Jul. 2015.

[7] M. Fu, C. Ma, and X. Zhu. Hui, "A cascaded boost-buck converter for high-efficiency wireless power transfer systems," *IEEE Trans. Industrial Informatics,* vol. 10, no. 3, pp. 1972-1980, Aug. 2014.

[8] H. H. Wu, A. Gilchrist, K. D. Sealy, and D. Bronson, "A high efficiency 5 kW inductive charger for EVs using dual side control," *IEEE Trans. Industrial Informatics,* vol. 8, no. 3, pp. 585-595, Aug. 2012.

[9] W. Zhang, S. C. Wong, C. K. Tse, and Q. Chen, "Load-independent duality of current and voltage outputs of a series- or parallel-compensated inductive power transfer converter with optimized efficiency," *IEEE J. Emer. Sel. Topics in Power Electron.*, vol. 3, no. 1, pp. 137-146, Mar. 2015.

[10] X. Qu, H. Han, S. C. Wong, C. K. Tse, and W. Chen, "Hybrid IPT topologies with constant current or constant voltage output for battery charging applications," *IEEE Trans. Power Electron*., vol. 30, no. 11, pp. 6329-6337, Nov. 2015.

[11] C. M. Wildrick, F. C. Lee, B. H. Cho, and B. Choi "A method of defining the load impedance specification for a stable distributed power system," *IEEE Trans. Power Electron*., vol. 10, no. 3, pp. 280-285, May 1995.

[12] A. Riccobono, and E. Santi, "Comprehensive review of stability criteria for DC power distribution systems," *IEEE Trans. Industry Applications*, vol. 50, no. 5, pp. 3525-3535, Sept. 2014.

[13] R. Ahmadi, D. Paschedag, and M. Ferdowsi, "Closed-loop input and output impedances of DC-DC switching converters operating in voltage and current mode control," in *Proc. IEEE IECON*, Nov. 2010, pp. 2311-2316.

[14] R. W. Erickson, and D. Maksimovic, *Fundamentals of Power Electronics,* 2nd ed., New York: Kluwer, 2001.

[15] C. K. Tse, Y. M. Lai, R. J. Xie, and M. H. L. Chow, "Application of duality principle to synthesis of single-stage power-factor-correction voltage regulators," *International Journal of Circuit Theory and Applications,* vol. 31, no. 6, pp. 555-570, Nov. 2003.

[16] S. G. Luo, Z. Ye, R. L. Lin, and F. C. Lee, "A classification and evaluation of paralleling methods for power supply modules," in *Proc. IEEE PESC,* 1999, pp. 901-908.

[17] M. Huang, S. C. Wong, C. K. Tse, and X. Ruan, "Catastrophic bifurcation in three-phase voltage-source converters," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 60, no. 4, pp. 1062-1071, 2013.

**Zhicong Huang** received the B.Sc. degree in electrical engineering and automation in 2010, and M.Sc. degree in mechanical and electronic engineering in 2013, both from Huazhong University of Science and Technology, Wuhan, China.

He is currently working toward the Ph.D. degree in power electronics at the Hong Kong Polytechnic University, Kowloon, Hong Kong. His research interests include power converter design, wireless power transfer systems and control.

**Siu-Chung Wong** received the BSc degree in Physics from the University of Hong Kong, Hong Kong, in 1986, the MPhil degree in electronics from the Chinese University of Hong Kong in 1989, and the PhD degree from the University of Southampton, U.K., in 1997.

Dr. Wong joined the Hong Kong Polytechnic in 1988 as an Assistant Lecturer. He is currently an Associate Professor of the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, where he conducts research in power electronics. Dr. Wong is a senior member of the IEEE and a member of the Electrical College, The Institution of Engineers, Australia. He is an editor of the *Energy and Power Engineering Journal*, Associate Editor of IEEE Transactions on Circuits and Systems II: Express Briefs, and a member of the Editorial Board of the *Journal of Electrical and Control Engineering*.

in 2012, Dr Wong was appointed as a Chutian Scholar Chair Professor by the Hubei Provincial Department of Education, China and the appointment was hosted by Wuhan University of Science and Technology, Wuhan, China. He was a visiting scholar at the Center for Power Electronics Systems, Virginia Tech, VA, USA on November 2008, Aero-Power Sci-tech Center, Nanjing University of Aeronautics and Astronautics, Nanjing, China on January 2009, and School of Electrical Engineering, Southeast University, Nanjing, China on March 2012.

**Chi K. Tse** received the BEng (Hons) degree with first class honors in electrical engineering and the PhD degree from the University of Melbourne, Australia, in 1987 and 1991, respectively.

He is presently Chair Professor at the Hong Kong Polytechnic University, Hong Kong, with which he served as Head of the Department of Electronic and Information Engineering from 2005 to 2012. He is author/co-author of 10 books, 20 book chapters and over 500 papers in research journals and conference proceedings, and holds 5 US patents. He was awarded a number of research and industry awards, including Best Paper Award by IEEE Transactions on Power Electronics in 2001, Best paper Award by International Journal of Circuit Theory and Applications in 2003, two Gold Medals at the International Inventions Exhibition in Geneva in 2009 and 2013, and a number of recognitions by the academic and research communities, including honorary professorship by several Chinese and Australian universities, Chang Jiang Scholar Chair Professorship, IEEE Distinguished Lectureship, Distinguished Research Fellowship by the University of Calgary, Gledden Fellowship and International Distinguished Professorshipat-Large by the University of Western Australia. While with the Hong Kong Polytechnic University, he received the President's Award for Outstanding Research Performance twice, Faculty Research Grant Achievement Award twice, Faculty Best Researcher Award, and several teaching awards.

Dr. Tse serves and has serevd as Editor-in-Chief for the IEEE Transactions on Circuits and Systems II (2016-2017), *IEEE Circuits and Systems Magazine* (2012-2015), Editor-in-Chief of *IEEE Circuits and Systems Society Newsletter* (since 2007), Associate Editor for three IEEE Journal/Transactions, Editor for *International Journal of Circuit Theory and Applications,* and is on the editorial boards of a few other journals. He also serves as panel member of Hong Kong Research Grants Council and NSFC, and member of several professional and government committees.