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ISSN 2475-742X

CPSS Transactions on Power Electronics and Applications

VOLUME 2 NUMBER 1 MARCH 2017

INAUGURAL SPECIAL ISSUE ON THE DEVELOPING TRENDS OF POWER ELECTRONICS: PART 2

A PUBLICATION OF THE CHINA POWER SUPPLY SOCIETY

CPSS TRANSACTIONS ON POWER ELECTRONICS AND APPLICATIONS

CPSS Transactions on Power Electronics and Applications (CPSS TPEA) is sponsored and published by China Power Supply Society and technically co-sponsored by IEEE Power Electronics Society. It publishes original and high quality peer reviewed papers in the field of power electronics and its applications. With the goal of promoting the technology of power electronics including concepts, theory, modeling and control, analysis and simulation, emerging technology and applications, CPSS TPEA is expected to be a favorable platform to strengthen information exchange in this area. Interested authors are welcome to submit your papers via the Manuscript Central (https://mc03.manuscriptcentral.com/tpea-cpss) online submission system. You can find more information on our website: http://tpea.cpss.org.cn.

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Editorial for the Inaugural Special Issue on the Developing Trends of Power Electronics: Part 2

WITH this editorial, we sincerely welcome our readers to the brand-new publication — CPSS Transactions on Power Electronics and Applications (CPSS TPEA). It is sponsored and published by China Power Supply Society (CPSS) and technically co-sponsored by IEEE Power Electronics Society (IEEE PELS).

CPSS was founded in 1983 and has been the only top-level national academic society in China that solely focuses on the power supply/power electronics area. In the past 30-plus years CPSS has dedicated to provide to its members, researchers, and industry engineers nationwide with high quality services including conferences, technical training, and various publications, and this in deed has helped the society build up its membership rapidly, which now totals up to more than 4000 individual members plus 500 enterprise members. The fast growth of membership in turn compels CPSS to always work out better services for its members, one of which being the open-up of this periodical — a new journal in English language as a publication platform for international academic exchanging. This of course needs to be done through international cooperation, and that's why IEEE PELS is tightly involved, being the premier international academic organization in power electronics area and one of the fastest growing technical societies of the Institute of Electrical and Electronics Engineers (IEEE).

To fulfill the publishing need of the fast-developing power electronics technology worldwide is a more important purpose of launching this new journal. So far there are only 3 or 4 existing journals which are concentrated on power electronics field and have global reputation. For quite a few years people in the international power electronics community have had the feeling that, the existing journals have not even come close to meeting the huge demand of global academic and technology exchanges. E.g., the two existing IEEE power electronics journals, i.e. IEEE Transactions on Power Electronics (IEEE TPEL) and IEEE Journal of Emerging and Selected Topics in Power Electronics (IEEE JESTPE), now publish about 1000 papers a year, which is under a very low paper acceptance rate of around 25%, but still have a back-log of about one year for the newly accepted papers to finally appear in printed form to the public. The addition of this new dedicated journal would be an ideal improvement to fulfill such a tremendous need.

The booming of publishing need really is an indicator of how fast power electronics has been developing in recent years. Innovations have been continuously coming up from component (both active device and passive device), module, circuit, converter, to system level, covering different technical aspects as topology or structure conceiving, modeling and analysis, control and design, and measurement and testing. New issues and corresponding solutions have been continuously presenting as the applications of power electronics prevail horizontally in almost every area and corner of human society, from industry, residence and commerce, to transportations, and penetrate vertically through every stage of electric energy flow from generation, transmission and distribution, to utilization, in either a public power grid or a stand-alone power system. I personally believe that we are entering a world with "more electronic" power systems. The prediction around 30 years ago, that power electronics one day will become one of the major poles supporting the human society, is coming into reality. And I also believe, that power electronics is going to last for long time as an important topic since it is one of the keys to answer a basic question for human society, which is how human can harness energy more effectively and in a manner friendlier to both the user and the environment.

Therefore, I assume that there is probably no better fitting as for CPSS TPEA to publish its first few issues under a special topic about the developing trends of power electronics. We have invited a group of leading experts in different areas of power electronics to write survey/review papers or special papers with review/overview nature to some extent. To publish in a timely and regular style, we organize this inaugural Special Issue into different parts. Part 1 was published in the December issue last year, Part 2 appears in this March issue, and the following parts are scheduled for the next issues.

In Part 2 we are honored to have 8 invited papers. For the first 3, each addresses one hot topic respectively in one of the 3 major application areas of power electronics: electric power grid, motor drives, and power supplies. The next 3 follow up with the state-of-the-arts in the structure or converters that are adopted in data center power systems, while the last 2 discuss specific issues for general power electronic circuits and systems.

We begin with a paper on the modernization of electric power grid. It is co-authored by Dr. Don Tan and Dr. Damir Novosel representing leadership of IEEE Power Electronics Society and IEEE Power and Energy Society respectively. It presents how power electronics & systems (PEAS) technology could possibly provide smart technology solutions for the power grid modernization to meet the grand energy challenge.

The second paper reviews the technology, research, and

Digital Object Identifier 10.24295/CPSSTPEA.2017.00001

applications of switched reluctance drives (SRD). It is written by Dr. Rik W. De Doncker and his research group from RWTH Aachen University, and presents a broad overview of the SRD taking into consideration all aspects such as machine modeling, design, control development, applications on the market and the focus of current research.

The third paper is about very high frequency (VHF) power converters. It is written by Dr. Dianguo Xu and his research group from Harbin Institute of Technology. It starts from the application background, introduces different topologies, and discusses resonant driving and control methods in a survey form.

The fourth paper is regarding data center challenges and their power electronics solutions. It is written by Dr. Philip T. Krein from the University of Illinois at Urbana-Champaign. The paper reviews the power hierarchy levels within modern data centers, and considers energy consumption and power electronics challenges across all levels of a data center, including building distribution, dc architectures, and conversion down to the board level.

The fifth paper is written by Dr. Johann W. Kolar and his research group from ETH Zurich, discussing techniques to realize highly efficient rectifier with minimized life cycle cost in DC data centers. It demonstrates how semiconductor technology, chip area, magnetic component volumes and switching frequency can be selected based on life cycle cost using analytical and numerical optimizations, and can be applied to three-phase buck-type PFC rectifier with integrated active filter for 380V DC distribution systems.

The sixth paper is written by Dr. Yan-Fei Liu and his research group from Queen's University, discussing LLC converter with possible application in data center, telecom, PV, and battery charging etc. It provides a comprehensive review on the latest advances of LLC converter from the perspective of topology and control with techniques range from high current, fast dynamic response to wide operational voltage range.

The seventh paper is written by Dr. Bo Zhang from the South China University of Technology, about sneak circuit — the unexpected path or operational status in an electric or electronic circuit due to the limitation or oversight in design. The paper briefly reviews sneak circuits in power converters and corresponding analyzing methods, with some interesting application examples.

Last but not least, the eighth paper is written by Dr. Chi K. Tse and his research group from Hong Kong Polytechnic University, revisiting stability criteria for DC power distribution systems. The paper focuses on the stability of current-source converter systems through an impedance-based approach, where a general set of stability criteria is developed and experimentally verified.

I'd like to thank the authors of all these 8 invited papers. It's their high-quality contributions that finally leads to the launching of this new journal. I'd like to thank Dehong Xu, President of CPSS, who in 2015 initiated the idea of publishing the new journal and since then has been persistently supporting my work as the founding Editor-in-Chief. I'd also like to thank Jiaxin Han, Secretary General of CPSS, Jan A. Ferreira, President of IEEE PELS, 2015-2016, Don F. D. Tan, President of IEEE PELS, 2013-2014, and Frede Blaabjerg, IEEE PELS Vice President for Products, 2015-2018, who form the CPSS and IEEE PELS Joint Advisory Committee for our new journal with Dehong Xu and myself. Other IEEE officers and leading staffs like Dushan Borojevich, PELS President, 2011-2012, Alan Mantooth, PELS President, 2017-2018, Mike Kelly, PELS Executive Director, and Frank Zhao, Director of China Operations, IEEE Beijing Office, just to name a few, also provided continuous support and constructive advices. My earnest thanks also go to the CPSS Editorial Office led by Lei Zhang, Deputy Secretary General of CPSS, for their wonderful editing work. It would not have been possible to create a new journal in such a short time without their efforts. I'd like to finally thank all the members of the Executive Council of CPSS and particularly the leaders of Chinese power electronics industry. They always firmly stand behind CPSS TPEA and ready to help whenever needed.

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Jinjun LIU received his B.S. and Ph.D. degrees in Electrical Engineering from Xi'an Jiaotong University (XJTU), China in 1992 and 1997 respectively. He currently holds the position of XJTU Distinguished Professor of Power Electronics, sponsored by Chang Jiang Scholars Program of Chinese Ministry of Education.

Dr. LIU coauthored 3 books (including a textbook), published over 200 technical papers in peer-reviewed journals and conference proceedings, and holds more than 30 invention patents (China/USA). He received for 7 times governmental awards at national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements. He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE Transactions on Power Electronics 2016 Prize Paper Award. His research interests are power quality control and utility applications of power electronics, micro-grids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu has served as the IEEE Power Electronics Society (PELS) Region 10 Liaison and then China Liaison for 9 years, an Associate Editor for the IEEE Transactions on Power Electronics for 9 years, and starting from 2015 the Vice President for membership of IEEE PELS. He is on Board of China Electrotechnical Society (CES) and was elected to a Vice President of the CES Power Electronics Society in 2013. He is the Vice President for International Affairs, China Power Supply Society (CPSS) and the inaugural Editor-in-Chief of CPSS Transactions on Power Electronics and Applications.

Energy Challenge, Power Electronics & Systems (PEAS) Technology and Grid Modernization

Don Tan and Damir Novosel

***Abstract*—Modern society has reached a point where virtually every crucial economic and social function depends on the secure and reliable operation of the electrical power and energy infrastructures. The energy consumption growth and the population growth are pushing world's total energy consumption to double by 2050. This represents grand challenges and opportunities for power electronics and electric power systems engineers to modernize the power grid. Power electronics & systems (PEAS) technology is increasingly important for smarter distributed systems, particularly for power grid modernization. This paper discussed smart technology solutions, such as PEAS, for the changing nature of the electric power system. Specific technical challenges that are facing the power electronics and electric power systems communities are then elaborated. It is shown that we can meet the grand energy challenge by leveraging the grid modernization efforts. To provide electric power to twice as many people does not have to increase the required environment footprint.**

***Index Terms*—Power electronics, electric power systems, grid modernization, energy challenges, energy solutions, large electronic power transformers, renewable energy, all things grid connected.**

I. Introduction

THE electrical grid is an amazing engineering achievement. The US National Academy of Engineering named it as number one among the top twenty engineering achievements for its "vast networks of electricity to provide power for the developed world" [1]. Over the last century, the grid has evolved into a system of systems. The technology is mature and electricity reliability (availability) is 99.99% or better. However, the basic technology of the electrical power grid was developed about a century ago and has been incrementally improved and its operation evolved [2], as new technologies, such as computing, sensors, and communications networking, became available. The electric power systems in the industrialized world, in addition to generally being quite old, particularly in large metropolitan areas, face challenges caused by new technology deployment trends, environmental concerns, new weather patterns, changing consumer needs, and regulatory requirements. New technology trends include development of more efficient, reliable, and cost-effective renewable generation and Distributed Energy Resources (DER), energy storage technologies, Electric Vehicles (EV), monitoring, protection, automation, and control devices, and communications that offer significant opportunities for realizing a sustainable energy future.

In the past, the distribution system was designed and built to serve peak demand (and comply with reliability and quality of service requirements) and was a passive delivery infrastructure with a radial "down and out" paradigm for the delivery of energy to consumers. Consumers used what they needed/wanted, the wholesale infrastructure provided the energy, and the T&D system delivered it with no need for real-time operation of the distribution system. Distribution operations consisted of construction, maintenance, and outage management — not of managing delivery per se. Today, customers are increasingly using the grid as a means to balance their own generation and demand and also as a supplier of last resource when their generation is unavailable. They expect to deliver excess generation back to the grid and to be paid for it, without restrictions on their production. And they still expect the grid to "be there" when they need it. In order to meet these needs, the very architecture of the distribution grid has to change and adopt new technologies, ways of planning, and ways of operating. Consumers are demanding changed business models and regulators and policy makers are striving to satisfy and even encourage them, sometimes running ahead of the grid's abilities to accommodate the new policies.

With the proliferation of smart devices, such as smart phones and other emerging wearable smart devices, a wave of industry systems are being digitized with computing power to be smart. It is safe to predict that all things that were industrialized will be digitized in order to make it smart. The future of our society will be revolutionized by the distributed smarter systems [3].

The grid that was originally developed in the last century requires addressing following issues due to integration of distributed energy resources (DER): 1) Bidirectional power flow; 2) Low fault currents and inadequate fault isolation; 3) Improved voltage management; 4) Low system inertia requiring improved frequency regulation; 5) Maintaining or improving reliability 6) Maintaining or improving safety 7) Transmission congestion; and 8) Efficient system operation and maintenance.

Power electronics & systems (PEAS) technology plays increasingly discriminatory role in grid modernization, electric vehicles, self-driving cars, and industrial drives, to name a few. Grid modernization represents a particular area where a significant growth has been happening in the utility indus-

Manuscript received March 10, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00002

try with many power electronics and electric power system related projects and technology development centers. However, a systematic understanding of issues and potential challenges and opportunities has not been fully explored. This paper is an attempt to address the missing pieces.

This paper is further organized as follows. Section II describes a grand challenge that is facing our society for the near future. Section III discusses the grid resilience and breadth and severity of the challenges related to aging power grid, physical and cyber security, and weather related issues. Section IV explains technologies to address the changing nature of the electric power system. Section V presents the grid challenges and opportunities the power electronics and electric power systems community face. Section VI points out that grid modernization will lay down a solid foundation for safe and reliable electrical energy delivery. Section VII summarizes recent development trends for PEAS technology. Section VIII describes the future options and recommendations to address grid transformation and possible solutions for meeting the grand energy challenge without having to increase the environmental foot print. And finally conclusions and references are presented at the end.

II. A Grand Energy Challenge

Refer to Fig. 1. According to a report released by the United Nations in 2000, the world's energy consumption will

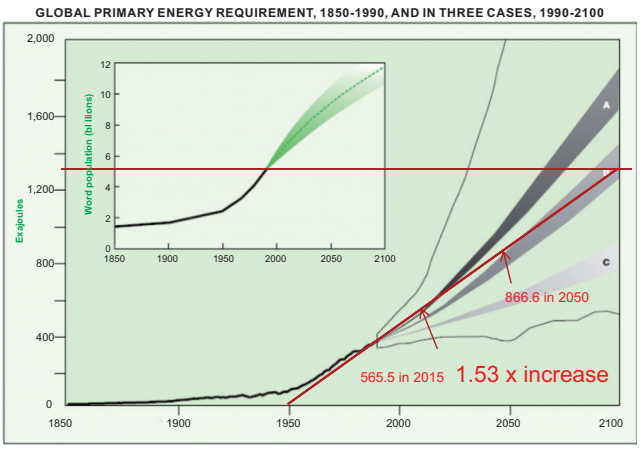

Fig. 1. World's energy consumption is projected to increase approximately by 1.53 times per year according to the United Nations.

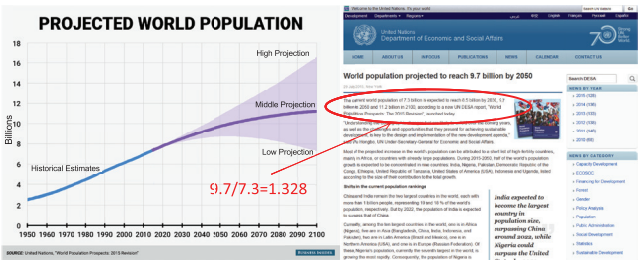

Fig. 2. World's population is projected to increase approximately by 1.328 times by the year of 2059 according to the United Nations.

grow by 53% from 2015 to 2050 [4]. In the meantime, the United Nation, in a dual report, also projected that world's population will increase by 32.8% from 2015 to 2050 [5] (Fig. 2). So the composite growth for energy consumption is projected to double from 2015 to 2050. The large increase of the energy consumption is expected to increase the energy environmental footprint significantly [6]. This represents a grand challenge for modern societies and their global citizens.

III. Grid Resilience

While the electrical power system is becoming and will continue to become more distributed, it is important to note that today's interconnected grid began as a distributed grid. Interconnected grids were created to improve grid cost-efficiency, reliability, service quality, and safety. As technology advancements made it easier to deploy renewable resources and, controllable, more efficient distributed grids, the fundamental benefits of a connected grid still hold and in fact, become more important. While the present grid is generally considered reliable, as dependency on the digital economy grows, users will demand even more reliability from the electric power delivery in the future, including resilience during major weather or security events. Transmission and distribution systems are an enabler to deployment of renewable resources, providing pathways for the transport of clean energy between production and consumption centers and a means for resource movement and delivery, while at the same time fortifying electric system efficiency, stability and reliability of supply. Integration of DER and distributed grids can increase efficiencies in the use of the existing grid, as well as become part of the overall development strategy to balance the supply and demand uncertainties and risks with a variety of different resources [7]-[10]. In cases where distributed grids become predominant (e.g. renewable intermittent DER plus energy storage), and grid usage becomes equally as variable, assuring a safe and reliable supply will require an intelligent, modern, resilient, flexible and safe grid.

Recently, grid resiliency is attracting more attention as weather events are becoming increasingly more frequent and damaging and as security threats external to the grid are increasing [11]. Changing weather patterns are leading to increased frequency of severe events and associated risks for electric utilities, such as extreme temperatures accompanied by abnormal peak demands, severe droughts accompanied by wildfires and infrastructure damage, etc. Average temperature rise stresses grid equipment (e.g. transformers and T&D lines), including reducing its life-time. In addition to adapting planning and operations practices to this "new normal", the above effects require updated equipment design, as well as different engineering and construction practices to counteract the impact of climate change and enable the adoption of new technologies.

In the meantime, the power grid infrastructure is aging with an alarming scale and at an alarming rate, according to a recent US Department of Energy report [12]. For instance,

large power transformers and much of power equipment are designed typically for 25 years' of life. But currently, a total of 70% of large transformers are 25 years or older, a total of 60% of circuit breakers are 30 years or older; and a total of 70% transmission lines are 25 years or older, to name a few.

More alarmingly, the impact of potential failure on the power grid is huge. A one-time loss of large power transformer can mean a temporary power outage for about 500,000 homes. A replacement of failed power transformer can take up to 2 years. A severe weather related event, such as Super Storm Sandy in the US, can inflict damage in the order of $28B to $168B [13].

Transmission lines are typically loaded to 50% in order to be able to deliver the peak power to the consumers during the peak usage time. Because of the environmental restrictions and costs associated with building new transmission lines, transmission system is often congested. Bottleneck is the weakest link in the transmission and is frequently the limiting factor for effective and efficient power flow. Congestion cost is estimated to be in the order of $1B to $2B in the last decade, according to a report from PJM based on data from its operations [14].

In summary, aging infrastructure should not be treated as an isolated concern; rather it should be viewed in the context of holistic asset management [15]. The entire equipment fleet must be managed to achieve system reliability and meet customer service needs through effective planning and operations. Holistic approach in support of business goals includes management of Aging Infrastructure (including condition monitoring and assessment tools), Grid Hardening (weather related response, physical vulnerability and cyber security), and System Capabilities (including reliability improvements). It also includes:

- Managing new Smart Grid assets such as advanced metering infrastructure and intelligent electronic devices.
- Investigate practical measures to shorten times to replace and commission equipment that failed due to extreme events, physical attacks, or other reasons.
- Better coordination of electricity and gas markets, including developing operational tools to more accurately forecast the availability of natural gas supply for generators and to improve unit commitment decisions.

IV. Smart Technologies for the Changing Nature of the Electric Power System

To address the grand energy challenges in the coming century, the US Department of Energy (DoE) launched the smart grid initiative under the Energy Independence and Security Act in 2007. Since then, the smart grid today has evolved to include the application of advanced communications and control technologies and practices to improve reliability, efficiency, and security. Specific technical areas include the following [16].

- **Advanced metering infrastructure** is comprised of smart meters, communication networks, and information management systems. It also includes customer-based technologies, such as programmable communicating thermostats for residential customers and building energy management systems for commercial and industrial customers. The architecture includes integration of sensing, communications, and control technologies with field devices in distribution systems to improve reliability and efficiency.
- **Advanced distribution and substation automation technologies** include digital relays, substation automation computers and data concentrators, and gateways to Distribution Management Systems (DMS), and Energy Management Systems (EMS) systems — are fully commercial and proven technologies. They need to be implemented in large scale with full utilization of their key capabilities. Distribution and Substation Automation promise enhanced grid flexibility as well as improved asset management that will increase asset lives, reduce costs, and improve reliability. However, only around 50% of US distribution substations are fully automated today.
- **Intelligent and adaptive reclosers and switches** isolate faults in smaller sections to support increased flexibility and improve reliability with both traditional and distributed grids.
- **Digital system protection** is adaptive to system conditions will need to be widely used. Distributed Energy Resources (DERs) with inverter technology create various operating scenarios which are not presently addressed by existing protection schemes. Circuit power flows and fault current levels will change based on DER size, output, and location on the circuit.
- **Advanced sensors and management systems** are required to provide cost-effective monitoring of key electric variables, including bi-directional power flows, voltages, currents, equipment and DER status, etc., as well as fault information to circuit breakers and other protection devices. The ability to control DER on a five-minute basis will require overall bandwidth beyond the typical AMI network capacity. It will be essential to have enough real-time monitoring of circuit conditions to provide situational awareness and to support applications such as distribution state estimation. Faster more intelligent and flexible volt-VAR schemes (such as distribution-class power electronics-based static compensators) that work in coordination with smart inverters are required. There is an increasing need for advanced sensors with higher resolution and GPS-based time-synchronization capabilities to accurately capture distribution system dynamics. The data provided by these devices may also help detect fault currents at a remote location or high impedance conditions not sufficient to trip the normal protection. Implementation of synchrophasor technology in distribution systems and applications based on such may be desirable as a means to address operational and power quality issues derived from DER variability.

As the renewable energy has come of age, the integration of renewable energy, especially wind and solar energy, reduces CO_2 gas emission and its impact on the environment. With the availability of energy balancing supported by storage technology and autonomous control, the concept of a structured microgrid was defined [17]. In general, microgrids serve two roles:

- It is a mechanism that enables resources, customer, and network to be islanded from the main power grid so as to allow continuity of service on some basis during contingencies with energy provided by local resources,
- In both islanded and grid connected operations, it can serve as a scheduling /dispatch /control entity responsible for balancing load and generation, and in grid connected operations possibly serving as a point of aggregation up to higher level operations and even to wholesale markets.

V. Challenges and Opportunities

As discussed above, grid faces real challenges but offers opportunities to address environmental concerns and improve efficiency and reliability of electrical power supply. Specific challenges can be divided into three categories: technology and integration, processes and standards, and regulation and business models.

For the technical aspects, we need to: 1) Provide more functionality and performance to break the cost barrier; 2) Obtain higher reliability and efficiency to complement traditional "dumb" hardware; 3) Promote the adiabatic technology [18] as a regular performance requirement; 4) Develop better dielectric materials and packaging for smaller size and foot print; 5) Reduce the cost to drive acceptance for wide applications; and 6) Make the performance to be location and load insensitive. In other words to obtain efficiency, cost and size goals simultaneously.

For policy and standards aspects, we need to: 1) Develop practical standards for better interoperability of various different types of devices and systems; 2) Drive regulatory requirements for pricing and for tariff to address resilience and environmental concerns through adaptation of renewables and related new electronics hardware and software technologies; and 3) Stipulate policies that support adaptation of new solutions for local and global economic, reliability, and safety benefits.

To illustrate the points, we can zero in on a case in point with further discussion — the large power transformers. The large distribution transformers are ubiquitous and cost $1,000 to $55,000 to procure. They are typically 10-60% loaded with increased total ownership cost for the consumer. For an electronic power transformer (EPT), the benefits are more compact, more efficient at light load with reduced ownership cost for the consumer and more functionality, especially with new and more capable SiC or GaN power devices coming on line every month.

But the electronic transformer still facing challenges in cost. Refer to Fig. 3. To the left is a comparison table electronics transformer relative to a traditional large power transformer [19]-[24]. According to the authors, the electronics transformer is still about 5 times more expensive than traditional designs. In order to reach its potential it needs to reach the target price of $10-$40/kVA. Another challenge is the losses are still 5 times larger than transitional transformers.

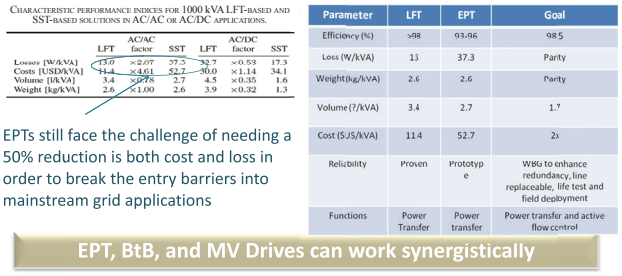

Fig. 3. Comparison of electronic transformer needs to consider its additional functionalities that any traditional power transformer cannot provide as shown in the table to the right.

Note that any comparison should include the additional functionalities that any traditional design simply cannot provide such as active control, fast response, flexibility, as it is illustrated in the right table of Fig. 3. EPTs, back-to-back converters and medium-voltage converters can work together synergistically to leverage the economy of scales, for both components production and hardware manufacturing, to bring the cost down to the desired level (a reduction of 3 to 5 times).

Electronic power transformer will continue to develop for more flexible electronic power transmission and distribution with more functionality such as those for transformer, for energy router, for electronic tab changers, and static VAR compensators.

Other opportunities for power electronic engineers are: 1) Invariant structure for fractal nature of the grid (radial or meshed); 2) Adiabatic, grid-scale, multilevel, multi-phase and multi-time-scale high-power conversion technology; 3) Grid-scale structure microgrids; 4) Reliability and fault management techniques for grids and microgrids; 5) Dynamic control of grids and microgrids; and 6) Substation retrofit and automation [25]-[28].

VI. Grid Modernization

To face the challenges presented by a rapidly aging grid, US DoE has recently initiated a multi-year program on grid modernization [13] (November, 2015). Some examples of those efforts are described in [26], [27]. Started from the smart grid initiative, the investment for grid modernization has reached $1.1 trillion, mostly for reliability and replacement purposes. The amount of investment cannot come from a single source. It has to be from multi sources such as government agencies at different levels, grid owners and operators, as well as consumers. So the grid modernization's first challenge is to enable the modernization drive to be a win-win-win situation for all parties involved [26].

The following are areas where further evolution and modernization is envisioned and needed to enable the T&D system of the future.

- **Integrated, holistic T&D planning and operations** — As the variability of distribution system net load increases, better coordination and information transfer is required. The ISO can no longer rely on simple load forecast bus allocation factors to forecast bus net loads but must be able to forecast PV production, as one example. More importantly, the use of DER to provide aggregated energy supply to the T&D system and ancillary services to the wholesale markets will be increasingly valuable.
- **Visibility and control of DER is vital to the electrical system of the future** — This will require more advanced monitoring on the distribution system (where sensors cost more to acquire and install) as opposed to simply obtaining it from the DER. If the utility of the future is to operate the distribution system in real-time to manage reliability and operational challenges derived from DER variability and load — and the system is to be engineered to allow for that management with associated savings — then visibility and controllability is a must. Hosting increased DER penetration levels and avoiding worst-case distribution investments absolutely requires a level of real-time DER visibility.
- **Improving flexibility, reliability, and DER hosting via advanced distribution system technologies** — It is necessary to leverage and modernize the existing infrastructure with electronic storage-supported distributed generation and active/dynamic control. The ideal scenario of the distribution system of the future of being able to monitor and control in real-time all key components of distribution circuits, is difficult to achieve in the short-term, given the monumental size and complexity of the distribution grid, and the large investments and required infrastructure (including communications systems) associated to this activity. However, a gradual transition toward this vision is possible and necessary to be able to provide a reliable, resilient, safe and secure service and operate the complex and highly dynamic distribution grid associated to high penetration of DER scenarios.
- **Work force development** — Well-trained workforce, capable of dealing with grid changes, is needed for the Grid of the Future.

In summary, building this intelligent grid is a monumental task (particularly on the distribution and grid-edge sides, which are vast and heterogeneous) that has led to the emergence of new concepts, technologies, and paradigms. Examples of this include debates regarding future grid architecture (a distributed, hybrid, or centralized grid); advances in grid modeling, simulation, and analysis; the introduction of the microgrid concept as an alternative to enhance resiliency and facilitate DER integration; and the convergence of information and operations technologies (IT/OT). As the power availability (frequently causally referred to as "grid reliability") is already 99.99%, it is important to note that the transition phase to potentially fully distributed systems will be long. During the transition phase, a hybrid grid will be in existence for long time to come.

The pace of the transition toward a modernized grid, particularly on the distribution side, is a function of the existing and expected system conditions and trends of every utility system and market. For instance, utilities operating in states such as California and Hawaii, where DER proliferation is already a reality and where aggressive DER adoption will continue to achieve Renewable Portfolio Standard (RPS) goals, must continue this evolution toward a modernized distribution grid at a faster pace than utilities operating in emerging DER markets. Otherwise, DER proliferation will lead not only to significant operations, planning and engineering challenges and inefficiencies, but also will prevent utilities (and ultimately customers and society in general) to attain the potential benefits derived from the adoption of these technologies. Furthermore, since even larger-scale adoption of DER is inevitable, given the imminent (or existing) achievement of grid parity by PV-DG in these markets, additions in grid modernization infrastructures and systems should largely be considered "required" rather than "optional" investments to enable the normal operation of modern and future distribution systems. It is worth noting that utilities operating in states with incipient penetration levels of DER, recognize the imminence and urgency of preparing for the transition to this new paradigm, and are actively working on modernizing their distribution grids and overall practices so that they are suitable for operation in this new reality.

We are at a crossroads of making business and technical decisions that will allow us to optimally and cost-effectively manage the electrical power delivery. As business models and technology are changing, traditional grids and distributed grids/microgrids should be purposefully integrated as hybrid grids to fulfill all the consumer needs (e.g. resilience and cost-efficiency), with transmission as an enabler to support integration of all available renewable resources [15]. In order for us to have clear goals for the modernization efforts, basic characteristics of a modern grid need to be understood first. The six (6) basic characteristics of a modern grid were first identified in [28]. They are: 1) Electronic, 2) Fractal, 3) Structured with microgrids, 4) Fault tolerant and fault isolating, 5) resilient, and 6) Asynchronous (Detailed discussion is the future subject for) These characteristics look simple on paper, but represent significant challenges (opportunities) for the power electronics and electric power systems communities.

VII. PEAS Technology

PEAS technology is experiencing profound changes. The top 10 trends in power electronics were presented in detail in [17]. Specifically, the top six (6) system-related trends are: 1) Renewables integration; 2) Structured microgrids (either dc-dominant or ac-dominant); 3) All things grid connected, 4) Transportation electrification; 5) Smart distributed systems (Smart grid, smart buildings, smart cities, etc.); and 6)

Energy harvesting. And the top four (4) technological trends are: 1) Power conversion goes adiabatic (Virtually no heat), 2) Low-power conversion goes monolithic, 3) High-power conversion goes multilevel, and 4) Wide-band-gap devices are going main stream.

Among all the emerging areas, the system applications and related issues are most prominent. It also represents a large departure from traditional power electronics technical scope. Traditionally, power electronics is simply defines as power conversion technologies (converters) with solid-state power devices. While this served the purpose of establishing power electronics as a technical discipline within electrical engineering, it is not adequate for today's endeavors of power electronics engineers. Among all the new systems applications as outlined in [17], the grid modernization represents most challenges and hence it represents many opportunities.

Fig. 4 illustrates basic constituent technical thrust for grid modernization. A modern grid has nine (9) major areas. They are: 1) Microgrids; 2) Physical grid, interconnects, and power flow control; 3) All things grid connected (ATGC); 4) Command, control, compatibility, interoperability, standards and codes; 5) Sensor network, command, and telemetry; 6) Communication network and security; 7) System integration and resiliency; 8) System analytics and big data; and 9) Policy, economics, and market. The dark green areas represent the technical areas where the PEAS is directly involved. It is clearly seen that six out of nine areas are involved with PEAS. PEAS technology is playing an increasingly important role in the drive for grid modernization. Among all the desired characteristics for a modern grid, the electronictization is the very first step, since it lays the foundation for the modern and electronic grid.

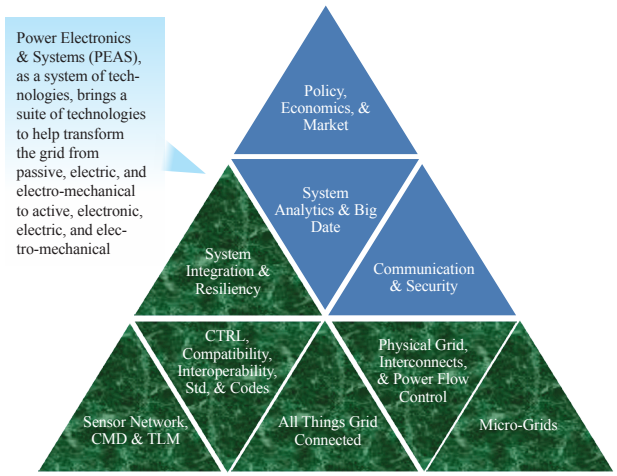

Fig. 4. PEAS technology occupies six (6) out of nine (9) main technical thrust areas for grid modernization.

VIII. Grid Transformation to Meet the Grand Challenge

Looking at the top level of grid modernization, we can summarize the task of modernization simply as: to transform

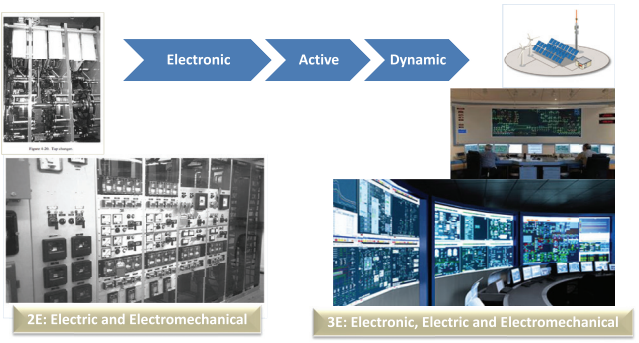

Fig. 5. Grid modernization is largely a task to transform the grid from currently (by and large) electrical and electromechanical (EE) to electronic, electrical and electromechanical (EEE).

the power grid from current (by and large) passive/static control to active/dynamic control. Fig. 5 illustrates the concept in a pictorial fashion, where a wireless communication symbol is used to indicate layers of communication infrastructure for grid data. (Aspects of communication network are not pursued in this paper because of space limit.)

A vast amount of work related to the grid modernization is to lay the electronic foundation, upon which the active control (and then smartness) can be inserted. Since the computer related smart technologies are relative mature, the real challenges then lie with their deployment, including measurement, protection and control devices.

Relative to grid applications, the challenges can be categorized into six (6) major equipment and apparatus areas known as "all things grid connected (ATGC)," as first introduced in [17] and discussed in detail in [17], [18]. Fig. 6 presents a pictorial summary of all the six (6) categories and typical hardware types under each category. (Because of the limited space, detailed discussion is not presented in this article, except the main challenges. Interested readers are referred to [18] and its listed references.)

The main challenges in ATGC are: 1) Limited availability of solid-state devices for high voltage and high current applications; 2) Limited availability of high voltage dielectric materials and packaging techniques that can take extremely high voltage and high dv/dt values; and 3) Limited availability of high-efficiency, high reliability, low-power, and small

Fig. 6. Electronictization lays a foundation for grid modernization – four (4) out of six (6) 6 main thrust areas are synergistic.

sized voltage, current, voltage and power sensors and limiters.

Furthermore, the retirement of conventional generation and reliance on more DG without appropriate back-up will also threaten the system's restoration/black-start capability. Many new generators do not include this capability due to complexity and cost. Renewable DG can inherently have this capability with the transition to grid-forming voltage source inverters and the addition of energy storage, however, creating opportunity for distributed, resilient, low cost black-start capability. The development of monitoring and control schemes to enable this is needed, including further applications of distribution GPS-based synchronized measurements and advanced substation and distribution automation.

Let's discuss how we can meet the Grand Challenge. Refer to Fig. 7, where a typical daily grid loading scenario is presented together with the typical terms associated with defining a grid capacity [29]. It is clear that a grid capacity is typically sized to meet the peak power demand during a year. But the peak power demand usually happens only about a few days out of a year, or about 1%. During the vast majority of the year the grid is underutilized and hence inefficient. A sensible way of achieving a better utilization is to devise a power flow and control scheme to leverage fully a grid's full installed capability.

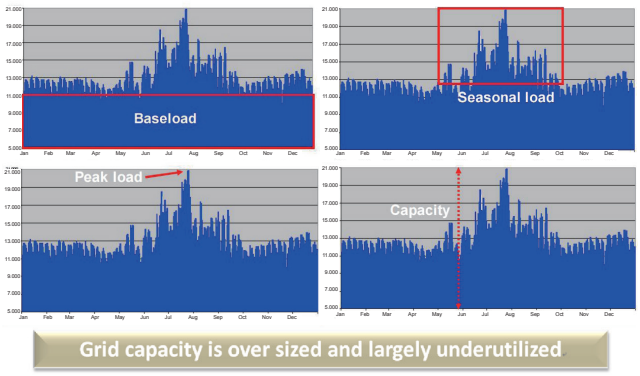

Fig. 7. Typical load conditions for a power grid and definition of frequently used terms for grid capacity.

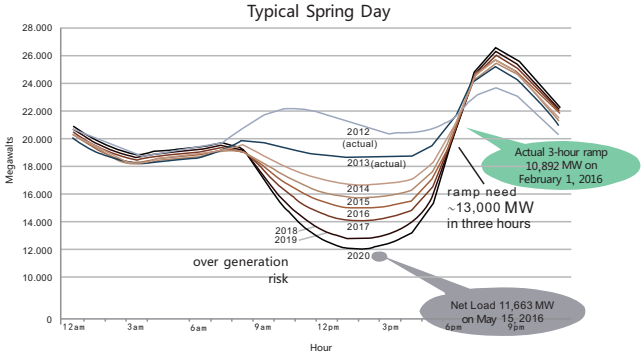

Fig. 8. 2016 update on the duck curve by California ISO (CASIO).

With the ever-increasing integration of solar power into the grid, the power demand seen by utilities typically resembles that of duck body profile during the day and hence the nickname "the duck curve" by CAISO. The 2016 update by CASIO is available in [30], as illustrated in Fig. 8. The duck curve shows steep ramping needs for utilities when sun does not shine and potential overproduction risk during the day when the sun shines in California. The fast ramping needs and the overproduction risk could both be handled effectively with PEAS technology together with sufficient storage capacity. PEAS-based equipment can be fast brought on line to provide the power needed during the day to meet peak demand, provided sufficient storage capacity is present.

The well-known peak shaving techniques [31] can then be used to store the over-produced solar power during the day and then release to power the peak demand during the evening (See [17], for a detailed discussion). If we assume that the peak power is typically 100% above the average load and that the amount of energy can be stored during the day is equal approximately to the additional power demanded by the load during the peak hours of the evening, then the real power can be "shaved" off to fill the valley of the duck curve. And then the load demand curve becomes effective a flat line, rather than a duck shaped. The flatness of the load profile has significant implication: It means that we can power twice as many customers (100% growth) without having to increase the capacity.

In summary, energy storage (empowered by power electronics technology) promises the ability to mitigate renewable DER variability and improve T&D utilization and economics. Technical, regulatory and economic barriers still impede its adoption even in states with aggressive programs for deployment. As storage is still fairly expensive, it is widely understood that "shared applications" — meaning multiple use of the same energy storage device, is a key to realizing the best economic potential from the technology. However, regulatory barriers and legacy paradigms are major obstacles to the rapid adoption of these technologies and their most effective uses. Energy storage is forced to fit into one of the generation, transmission, distribution or customer "buckets" and follow rules established for that asset class. Energy storage is in many viewpoints a new asset class of its own.

Furthermore, electric transportation holds significant promise for reducing dependence on oil and carbon footprint. Electrical systems can help improve the livability, workability and sustainability of "Smart Cities". Specifically addressing EVs, the first purchase of an EV is likely to inspire more in the same neighborhood, which can lead to the emergence of "clusters" and the overload of system components. Distribution system capacity upgrades in combination with solutions based on DER and intelligent load control using power electronics could address these issues [32].

That is, we can meet the grand energy challenge without having to increasing the environmental footprint of carbon-based energy generation and reliance on fossil fuel. The discriminator is PEAS and energy storage technology and system

engineering to integrate them together with any given local environmental predictions for sunshine and weather forecast and accompanying advanced distribution energy management systems [33], [34].

Conclusions

The following are overarching recommendations to achieve reliable, resilient and cost-effective delivery of electrical energy while supporting environmental targets for years to come:

- There is a need for grid modernization, with the speed of modernization adjusted to the pace of integration of clean DER and environmental and other regulatory targets.
- The architecture and design of the grid will have to be updated to accommodate very high penetration of DER and customer driven operations and planning.
- Enabling the transition to a modern grid requires changes in business models and regulatory policies, as well identification of the technical needs and development of new technologies.
- Continuous focus on improving reliability, resilience, safety, cost-efficiency, and customer flexibility to choose.

The six (6) basic characteristics of a modern grid are: 1) Electronic, 2) Fractal, 3) Structured with microgrids, 4) Fault tolerant and fault isolating, 5) Resilient, and 6) Asynchronous. Furthermore, the electronic power transformer will continue to develop for more flexible electronic power transmission and distribution with more functionality such as those for transformer, for energy router, for electronic tab changers, and static VAR compensators.

Other opportunities for power electronic engineers are: 1) Invariant structure for fractal nature of the grid (radial or meshed); 2) Adiabatic, grid-scale, multilevel, multi-phase and multi-time-scale high-power conversion technology; 3) Grid-scale structure microgrids; 4) Reliability and fault management techniques; 5) Dynamic control; and 6) Substation retrofit and automation.

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Technology, Research and Applications of Switched Reluctance Drives

Bernhard Burkhart, Annegret Klein-Hessling, Iliya Ralev, Claude P. Weiss, and Rik W. De Doncker

***Abstract*—Electrical drives are one of the major consumers of electrical energy and their penetration in the market is still growing. Hence, for many drive applications efficient, reliable and cost effective solutions have to be found. Switched reluctance drives (SRD) offer a potential solution when focus is mainly on cost and robustness. However, to benefit from the unique advantages of this machine type a deep understanding of its strongly non-linear behavior is required. After discussing some major differences to classic rotating field machines, this paper presents a broad overview of the state of the art of SRD taking into consideration all aspects relevant to machine modeling, design and control development process. Finally, applications on the market utilizing SRDs and the focus of current research is presented. After reading this paper the reader will be able to assess if this modern drive technology could be advantagous in a given application.**

***Index Terms*—Switched reluctance drives, switched reluctance machine, design, modeling, analysis, control, acoustics.**

I. Introduction

ALTHOUGH the switched reluctance machine (SRM) is one of the oldest rotating machine concepts (proposed first by Taylor in 1840 [1]), its practical implementation and market introduction came to fruition in the mid-1980's thanks to the development of modern power electronic components and control circuitry [2]. The SRM has always been of interest to drive designers due to its simple working principle and robust mechanical construction. Especially, for high-speed applications with low-to-medium torque requirements, or when a high overload capability is necessary, the SRM has unique advantages over classic rotating field machines. However, due to the SRM's highly non-linear characteristics, the design of a switched reluctance drive (SRD) requires an integrated, often iterative, design process in which the converter, its controls and the design of the SRM itself are intertwined. Hence, a global system perspective of the SRD technology is essential to reach an appropriate solution for the target application. To achieve this task a fundamental understanding of the entire SRD, i.e. the machine, its inverter (including control) and the target system are required.

Within this paper state-of-the-art and current research on SRD will be covered. Section II compares the SRD to itsrivals, the synchronous and induction machines. Thereafter, design approaches are presented in section III, followed in section IV and V by SRD modeling and analysis techniques. The technological discussion closes with the inverter and its control in section VI and VII. In section VIII some examples of SRDs available on the market are presented and discussed. Finally, an overview on current application research is given.

Manuscript received March 24, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00003

II. Pros and Cons of SRDs

The outcome of selecting the optimal drive for a given application depends strongly on the application's requirements, i.e. torque and speed, and the design goals. Selecting a certain machine or designing an electrical drive is generally a compromise between technologically conflicting requirements, such as power density, efficiency (in a single operating point or over an entire load cycle), field-weakening potential, cost, employed materials, machine or drive volume, fault tolerance and maintenance cost. This section highlights some major differences between various machine types with respect to these requirements.

Beside machines with permanent magnets, all electrical machines have in common, that the primary flux has to be supplied by an external source. Thereby, as long as no field-weakening is required, permanent magnet synchronous machines (PMSM) tend to have the lowest ohmic and inverter losses, and therefore the highest overall system efficiency in the so-called base speed region. However, when using surface mounted permanent magnets (SPMSM), only a very small field-weakening operation, similar to synchronous reluctance machines (SynRM), is possible. A common figure of merit is the field-weakening (maximum speed compared to the corner speed) of the machine. In case of SynRMs this ratio is about 2.5 [3]. Switching to interior permanent magnet machines (IPMSM) and adding a certain amount of reluctance torque, the field-weakening ratio can be pushed up to 5-7 times its corner speed. In contrast to the variable flux machines, this operation however forces the inverter to supply reactive current to actively weaken the magnet flux and hence reduce the efficiency. Induction machines (IM) have higher rotor losses when compared to SynRM and hence generally a lower efficiency region. However, the IM has a larger field-weakening area with 3.5 to 5 times its corner speed [4]. A major disadvantage for applications with special sizing requirements is the fact that the IM is the only

machine which can not be effectively built with concentrated windings that have shorter end-turns compared to distributed windings.

For SRMs an extensive field-weakening area, up to 10 times, is claimed [5]. This wide speed range capability originates from the possibility to operate the SRM in deep magnetic saturation. Furthermore, single-pulse operation enables exciting the SRM far above the designed corner speed point. Both features combined offer even an additional overload reserve above base speed when the machine is operated in continuous conduction mode (CCM). The efficiency of SRMs is similar to that of a SynRM in the designed operating region, however the rotor losses are expected to be higher due to the pulsating magnetic fields. In contrast to IPMSMs, the efficiency of SRMs is the highest in the region just above base speed and at high torque. Hence, SRMs are especially suited for applications with a broad field-weakening region. On the other hand, at partial load some penalty has to be expected.

SRMs are operated with pulsating voltage or current waveforms. These block waveforms cause significant pulsating forces between rotor and stator. Particularly the radial forces, which are much larger than the tangential forces, cause vibrations and therefore also acoustic noise [6]. The steeper flanks of the force waveforms in SRMs (compared to rotating field machines) are disadvantageous to reduce noise, which can only be reduced to a certain extent by proper machine design, housing construction or force control measures [7], [8]. Similarly, the inherent torque ripple has to be tackled during the design stage and can be reduced further with appropriate torque control methods. Possible solutions to reduces these disadvantages are presented in sections III and VII in this paper.

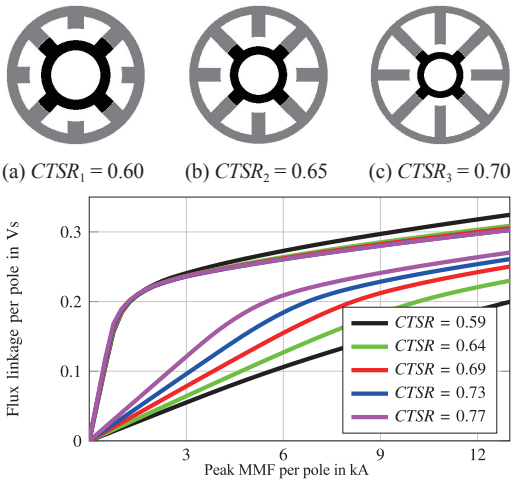
Regarding thermal design of electrical machines, e.g. for temperature critical applications, the SRM as well as the SynRM are particularly suitable for high temperature applications. The maximum operating temperature of these machines is only limited by the thermal insulation class used for their windings. In contrast to this, in IPMSM and SPMSM the employed magnet material, as well as eddy current losses in the rotor place serious constraints on the maximum temperature at which these machines can be operated. In IMs the thermal expansion coefficient of the rotor cage and electric sheet materials have to be considered for lifetime estimations due to mechanical stress during thermal cycling.

The low rotor inertia, high torque dynamics as well as the lack of drag torque in freewheeling are further benefits of the SRM compared to rotating field machines. The high torque dynamics are based on the fact that within each voltage period the entire coil is magnetized and demagnetized. Hence, for each electrical period the magnetic flux can be freely set. The time constant associated with this magnetization process is much lower than the reacting magnetizing time constant common in rotating field machines. Furthermore, the fact that the stator phases are magnetically decoupled in SRMs, makes the SRM attractive, e.g. for aerospace applications that require very high reliability [9]. Indeed, SRMs can continue operation, albeit with reduced power, when one or more phases drop out. This “limb home” capability can be of great value in traction and electrical propulsion drives for electric vehicles.

III. Design

A long list of publications can be found, e.g. [2], [10]-[13], which present torque production equations similar to those of classic rotating field machines and analytical sizing rules for SRMs. All this work directly and indirectly contributed to a design tool developed by a team under guidance of Prof. T. Miller [14], which is till today the reference in analytical SRM design.

With the increased use of finite element analysis (FEA) other approaches, such as in [15], focus more on the physical working principal of SRMs for the design methodology. This work, based on a generalized SRM model, is further developed into a comprehensive design procedure in [16], [17]. To make the design process dependent only on physical and geometric parameters rather than empirical tuning factors a solution space based design approach is prefered in [18]. In this approach the application dependent design parameters are decoupled from the basic torque production capability of a specific SRM cross section. The underlying solution space is subdivided by the machine configuration, diameter and the coil-to-slot-ratio *CTSR* ([16]), which unambiguously describes the shape of stator teeth and yoke (see Fig. 1). The torque production capability is then pre-calculated by FEA and stored in a database. The design comparison can be performed with a small amount of physical parameters. As a result, the designer has a fast, yet accurate evaluation tool, based on FEA validated machine characteristics, to assess the potential and limitations of different machine configurations before entering a detailed iterative optimization process. It is shown in [18] that even in this early design stage it is essential to consider the thermal behavior and the losses,



(a) $CTSR_1 = 0.60$ (b) $CTSR_2 = 0.65$ (c) $CTSR_3 = 0.70$

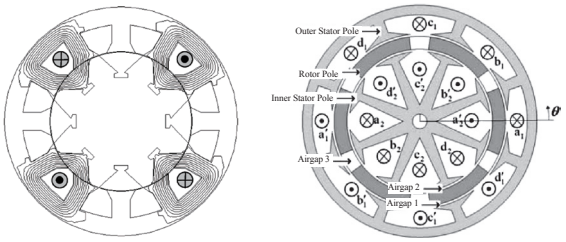
(d) Flux-linkage curves for aligned and unaligned position

Fig. 1. Influence of the *CTSR* on SRM cross section and flux linkage with constant outer diameter [18].

as the heat transfer characteristic from coil to cooling sleeve strongly depends on the SRM cross section.

Optimizing an SRM for a certain driving-cycle is a quite challenging task and strongly depends on the optimization criteria [19], [20]. If focus is mainly on efficiency, iron and eddy current losses in the coils are the main challenge. Low loss electrical steel [21] or special winding schemes and placements [22] should be considered for improvement. When focus is on acoustics, the positioning of the eigenfrequencies and the structural stiffness of the stator are of special interest. Many publications investigate the possibilities to reduce stator surface vibrations [20], [23], however interactions with control algorithms always need to be considered (see section VII).

Recent publications divert from the classic SRM structure to adopt the SRM for special applications. References [24], [25] propose a segmental rotor structure to improve the magnetic utilization and hence increase torque output. A 40% increase of power density is claimed. In [26] a double stator structure is proposed, where basically a outer- and inner-rotor SRM is combined in one machine. Beside the immense increase in torque density, an improved acoustic behavior is achieved. For the same torque, the radial forces on the outer stator are strongly reduced. In [17] an axial segmentation of a threephase machine is proposed for applications with an extremely low machine diameter requirement. These examples illustrate that the SRM concept lends itself to be adopted to new applications, thereby outperforming other machine types.



(a) Segmental rotor [25] (b) Double stator [26]

Fig. 2. Special machine cross sections derived from the basic SRM functionality.

IV. Modeling

Models for switched reluctance machines are needed for motor design and control algorithm development. To reduce development costs, system simulations nowadays are crucial in gathering and analyzing data on entire drive trains before building the actual prototype. Coupling the machine model with inverter and load models allows fast and efficient programming of control algorithms. Such simulation models are referred to as offline models and should portray reality accurately.

The second category of models are real-time online models for motor control units. Over the last decades online model complexity and accuracy has greatly increased thanks to the progress in microelectronics and its computational power.

Nevertheless, due to the strong non-linear behavior of SRMs a trade-off between simulation accuracy and simulation speed still has to be made. Some modeling techniques are very accurate but time consuming, such as the coupled finite element analysis (FEA). On the other hand, models based on analytical formulae and look-up-tables (LUTs) are very fast but tend to have reduced accuracy.

SRM models can further be divided into inductance (current fed) and flux-linkage (voltage fed) based models, depending on the main state variable. Commonly the machine's phase voltage equation, integrating the terminal voltage, is used to calculate the flux linkage per phase. The non-linear transformation of the phase flux linkage at a certain rotor position to the produced torque (radial forces and phase current) can be modeled by a number of different approaches in an attempt to combine simulation accuracy and speed. These techniques are described in the next sections..

A. Offline: SRM Models for System Simulations

Today, look-up tables (LUT) are most common to model SRMs, as they are directly transferable to the controller of the machine. Thereby, the relationship between flux linkage, rotor position, current and torque is stored in 2D LUTs. As switched reluctance machines are operated in saturation, it is important to consider their non-linear magnetic characteristics. This is achieved by non-linear FEA simulations [22] or testbench measurement of the actual machine [27]-[29].

Depending on the winding configuration an inductance (Fig. 3) or flux based (Fig. 4) machine model can be more suitable. When series windings are considered, the inductance based modeling approach is more suitable. In case parallel windings are considered, a flux-linkage based modeling approach is more suitable. Normally phase based LUT models are used. However, if machine asymmetries, for example rotor eccentricities, are simulated, the models should be pole based so that each stator pole has its own LUT.

The computationally fastest models are analytical formulas describing the electro-magnetic SRM behavior as in [27], [30]-[33]. Thereby, the analytical equations describe the

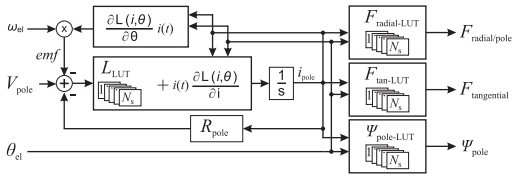


Fig. 3. Per pole inductance (current) based look-up table SRM model.

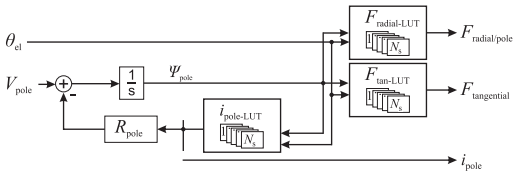


Fig. 4. Per pole flux-linkage based look-up table SRM model.

machine geometry, to determine the flux path through the machine, with focus on the air gap. From the magnetic flux distribution the tangential- and radial forces are determined. Alternatively, equations can be expressed to fit the non-linear phase inductance of the SRM. The model thus becomes an inductance based model, describing the change of the inductance in dependence of rotor position and current.

Similar to analytical equations describing the flux path, magnetic lumped parameter models known as magnetic equivalent circuits (MECs) can be used. In contrast to the analyticaland LUT models, MEC models are more commonly used when phase coupling [34], [35] or geometric asymmetry effects in the machine are described [36], [37]. MEC-based models offer a more sophisticated machine model, with more accuracy compared to analytical models, without the computational complexity of a FEA. MEC networks can either be formulated as meshes or nodes, resulting in different matrices to be solved. A comparison is investigated in [38].

With the advances of computer aided design FEA software tools specifically for electrical machines have become available. Not only are non-linear machine characteristics being calculated to support the design process of electrical machines, also in-depth electromagnetic and multi-physics analysis has become possible. Calculating the flux distribution, eigenfrequencies and forces acting on the machine during the design process has become state-of-the-art. A further method to analyze SRMs are circuit coupled FEA models. Thereby, a time-stepping simulation is executed modeling the inverter and control circuit with a circuit simulator, while the actual crosssection of the machine is modeled in great detail with FEA, and the control algorithms are executed for example in MATLAB/Simulink. This allows loss distribution analysis (eddy current, iron loss) at a specific operating point determined by its specific current trajectory. The disadvantage of coupled-FEA is the computational complexity and considerably longer computational time [39]. In pancake shaped machines the effects of end windings can be considerable. Calculating stray flux due to end effects is only possible with 3D FEA. However, the meshing complexity increases manifold compared to a 2D analysis, leading to even longer computation times.

The challenge to reduce computation complexity while maintaining the most realistic model has sparked the search for different kinds of machine modeling approaches. Nakamura models iron loss within a MEC model by incorporating additional inductances next to the reluctances [40]. Another approach for offline and online modeling to calculate instantaneous torque are gage curves [30], [32]. Thereby, the flux-linkage versus rotor position and current characteristic is stored as normalized flux-linkage curves in relation to the rotor position in a LUT. This allows instantaneous torque calculation at a constant current from differentiation of the stored flux linkage values.

B. Online: SRM Models for Real-Time

When designing online models the main challenge is to create algorithms with high accuracy that are able to run in real-time on (low-cost) motor control units. Today, often a LUT-based approach is used, whereby the tables are provided by either FEA or measurements. To reduce the initialization effort and to account for production uncertainties, the amount of auto-parameterizing [41], genetic algorithms, self-learning and neural network tuning algorithms, that adjust the characteristic stored in the LUT to the actual machine, has increased steadily.

Alternatively, to model saturation and phase coupling in an SRM, Fleming proposes to use MEC-based models [42], [43]. However, the network needs to be reduced to enable realtime capability, leading to a strongly reduced analytical phase model.

V. Analysis Techniques

A. Losses

To predict efficiency of a particular SRM design or a control strategy, the machine losses need to be determined already at an early development stage. Machine losses in general are divided into copper losses, iron losses and mechanical friction losses.

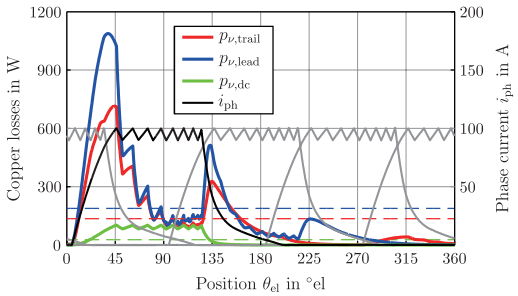
Copper losses consist of ohmic losses and additional eddy current losses caused by the skin and proximity effects. Contrary to conventional rotating field machines, the windings of SRMs are penetrated by a high amount of stray flux at the stator tips. Therefore, for an accurate efficiency analysis eddy currents in the windings have to be considered [22], [39], [44]. The amount of stray flux depends on the saturation of the stator teeth. The saturation leads to nonlinear magnetic behavior. Additionally, the stray field is two-dimensional and varies depending on the position of the rotor [22]. In most cases analytical approaches are not sufficient for copper loss calculations of SRMs. In [39], [44] an automated copper loss analysis based on FEA is presented.

The approach from [39] considers the actual phase current trajectory to determine the instantaneous losses (p_v) depending on the electrical position of the rotor. Fig. 5(a) displays the copper losses of a four-phase SRM operated with hysteresis current control. During motoring operation, the winding losses on the leading side of the stator teeth are higher than the losses on the trailing side. This is due to the fact that the magnetization of the phase before the aligned position causes a higher amount of stray flux penetrating the leading side windings.

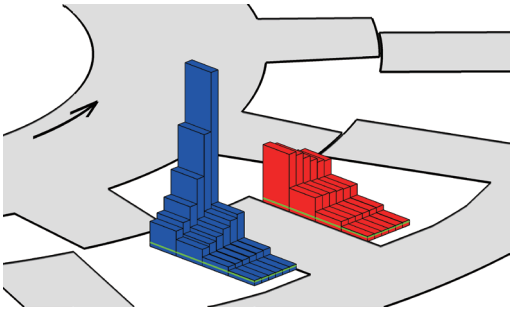
The instantaneous ohmic losses ($p_{v,\mathrm{dc}}$) depend quadratic on the phase current and account in the observed case only for a small amount of the copper losses. Eddy current losses occur also due to magnetization of the neighboring phases. Fig. 5(b) shows the loss distribution depending on the position of each winding in the coil. In windings closer to the air gap higher eddy currents are induced.

For the iron loss estimation in electrical machines various methods and models are presented in literature. Two

groups can be distinguished: empirical models and physics based models [45]-[47]. Empirical models base on equations deduced from measurements as e.g. the original Steinmetz equation (OGE) [48]. The Jiles-Atherton model [49] is an example for a physics based approach. The model describes the losses based on the molecular behavior of the material.



(a) Losses depending on the electrical position



(b) Loss distribution depending on the position of the winding

Fig. 5. Finite-element based winding loss calculation [22].

The flux in SRMs is non-sinusoidal. Therefore, approaches considering the time-depending gradient of the flux density instead of the peak flux density are more applicable for SRMs, e.g. modified Steinmetz equation (MSE) [50] and the improved generalized Steinmetz equation (iGSE) [51]. For the loss calculation with analytical approaches the SRM is divided into parts (e.g. stator teeth and stator yoke sections) assuming a homogeneous flux density in each of this part [52]. However, especially at the tips of the teeth this assumption is not fulfilled due to deep saturation. The choice between an analytical approach and an FEA is a trade-off between accuracy and calculation effort.

Fig. 6 exemplifies a loss distribution of a two-phase SRM based on an FEA [47]. Due to the symmetry of the machine only a quarter of the machine is investigated. The dissimilar distribution of the losses along the stator yoke (points a and b) can be observed. The reason for this is that some yoke segments experience an alternating magnetic flux, while others segments experience only an unidirectional flux. The effect is typical for SRMs. Furthermore, the loss density is higher at the tips of the teeth (points d and g) as in middle of the teeth (points c and f) as shown in Fig. 6.

Mechanical friction losses occur in every machine. However, due to the doubly salient structure of the rotor and the stator, SRMs are prone to higher windage losses. Especially at high rotational speeds, the windage losses in the air gap should be minimized. These losses can be estimated with the formulas proposed in [53], which are also implemented in [14]. References [54], [55] confirm the losses with some experimental results.

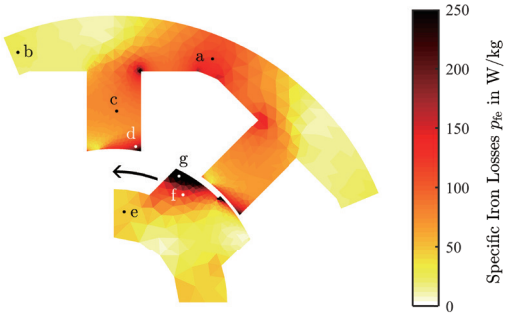


Fig. 6. Loss distribution of an two-phase 8/4 SRM [47].

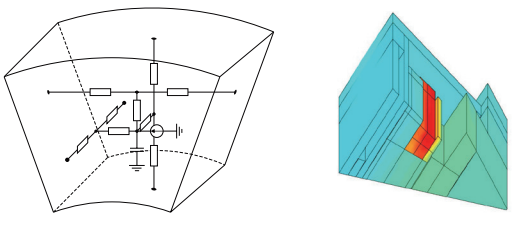
B. Thermal Behavior

Improved power density of electrical machines is achieved by downsizing and pushing the machines towards their thermal limits. However, overheating reduces the life span of the machines and might cause premature failures [56]. Therefore, it is important to analyze the thermal behavior of the machine and the effect of the occurring losses on the machine regarding the resulting temperature distribution.

To model the thermal behavior of SRMs, lumped parameter thermal networks (LPTNs) [57] or computational fluid dynamics (CFDs) and FEAs [58] are used. Space-resolved lumped parameter thermal networks have been proposed to predict the hot-spot temperature as well as the temperature at any userspecified spot within the machine [59]-[62]. They represent a trade-off between accuracy and calculation effort.

The space-resolved LPTNs of electrical machines are based on 3D cylindrical elements. Each element consists of three 1D T-structure thermal circuits connected at their central points (Fig. 7(a)). The resistances represent the thermal contacts and conductivity while the capacitor represents the thermal capacity of the object. The losses of the element are fed into the element by the current source. The potential of the central node represents the average temperature of the element. The potential of the outer nodes represents the temperatures on the boundary surfaces [60].

The LPTN can often be simplified using the angular symmetry of the machine. The minimum symmetry of SRMs is



(a) Cylindrical element (b) Discretization

Fig. 7. Space-resolved lumped parameter thermal network [56].

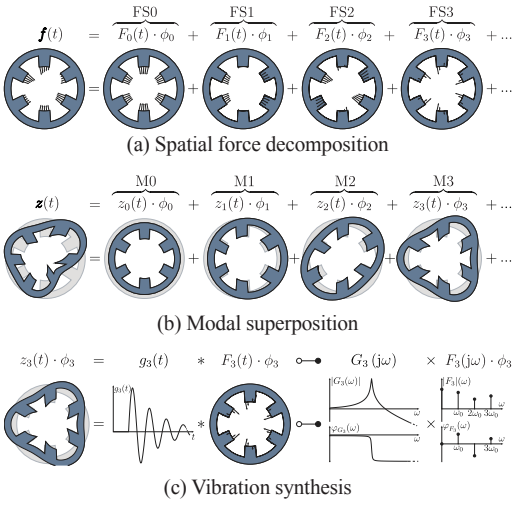
one half of a stator tooth and one half of a rotor tooth [56]. Fig. 7(b) shows the discretization of an 18/12 SRM. Implemented on a controller the space-resolved LPTN can be used to estimate the temperatures of the machine online. This information can be used for model predictive overload control of electrical machines [63].

C. Acoustic Excitation

Noise in electrical machines is of electromechanical (radial force ripple, torque ripple, inverter switching), mechanical (bearings, friction), combined electrical and mechanical (eccentricity) or aerodynamic (fan, rotor) origin [6], [64], [65]. For SRMs the acoustic noise of electromagnetic origin dominates the aerodynamic noise except in case of high-speed SRMs with open rotors [66]. The most relevant source is the airgap force [6], which is hard to measure directly but can be determined via simulations of the electromagnetic domain from its excitation (current, magnets). The air-gap force is transformed via the structure domain to vibrations which are transmitted via the acoustic domain to airborne sound [65]. Classical acoustic machine models simulate this causal path as a three-domain approach [67].

As shown in Fig. 8(a), the time-dependent radial air-gap force can be decomposed to spatial Fourier series components, socalled force shapes (FSs). The Fourier series can eventually be truncated based on the observation that with increasing spatial order ν the vibration response of the machine to a force excitation shape decreases [67]. Due to the symmetry of SRMs along the axial direction only the forces in 2D need to be considered [65].

Analog to the spatial force decomposition, the timedependent deflection of the SRM can be described by a superposition of modes [69] (Fig. 8(b)). The modal superposition approach is based on the fact that the dynamic behavior of a structure for a given frequency range can be separately modeled as a set of individual modes of vibration [65]. Modes are almost exclusively excited by force shapes with the same order [70]. The excitation of a mode due to a force shape is quantized by the structural vibration response g_ν. A transformation of the vibration response and the force shape to the frequency domain simplifies the calculation (Fig. 8(c)). Additionally, the eigenfrequency of the vibration response becomes visible.



(a) Spatial force decomposition

(b) Modal superposition

(c) Vibration synthesis

Fig. 8. Acoustic modeling [68].

A universal acoustic modeling framework for electrical machines is introduced in [65], [71]. The structure of the framework is shown in Fig. 9. The normalized structural responses and the electromagnetic characterizations including the air-gap force model are pre-calculated with two independent FEAs. The data is saved and can be used afterwards. For each operating point or torque-speed trajectory a system simulation calculates, with help of the stored FEA-data, the occurring force shapes. With these force shapes and the stored vibration responses the vibration synthesis determines the resulting machine vibrations.

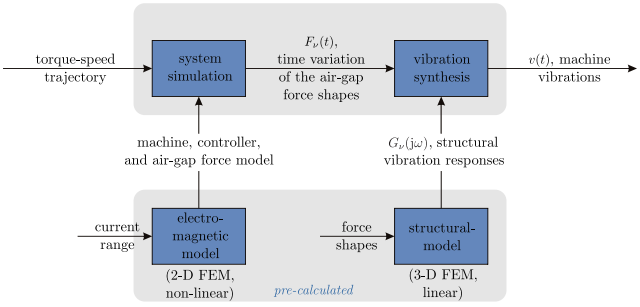
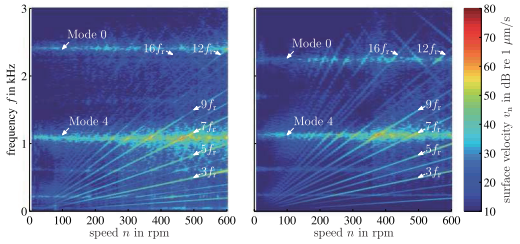


Fig. 9. Acoustic modeling framework [65].

The advantage of this approach is that the two FEAs with high calculation effort have to be carried out only once per machine design. This results in high accuracy and low calculation effort. In comparison, for the classic threedomain approach [67] for each operating point all three models have to be solved. This creates a trade-off between fast and therefore often inaccurate analytical models and accurate but time consuming FEAs [65].

Fig. 10 compares exemplary the measured and the acoustic modeling framework synthesized run-up spectrograms of a four-phase SRM. The eigenfrequency of the structural vibration response of mode 0 and mode 4 are clearly visible. The harmonics of the electric rotor frequency f_r can also be identified. The observed machine has a shape 0 excitation at multiples of $4f_\mathrm{r}$ and a shape 4 excitation at all odd multiples of f_r [65]. Measurement and simulation show a high degree



(a) Measured (b) Synthesized

Fig. 10. Validation of modeling framework with run-up spectrograms [65].

of accordance.

D. Eccentricity

The radial forces acting on the teeth surfaces of SRMs is known to cause vibrational and acoustic noise, as discussed before. However, in case of a rotor eccentricity, these radial forces are superposed by an additional unbalanced magnetic pull (UMP). Such an eccentricity can occur during fault operation or in normal operation caused by manufacturing tolerances.

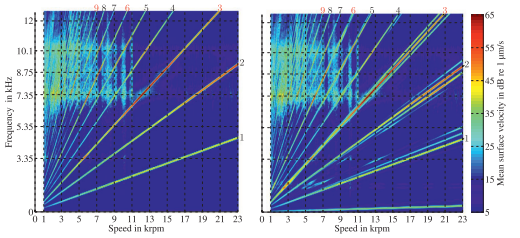
Eccentricities are divided into static, dynamic and mixed eccentricities [72]. Thereby, a static eccentricity implies that the rotor's axis is not placed entirely in the center of the stator i.e. a shorter air-gap length on one side. With a dynamic or rotating eccentricity the rotor axis is not entirely in the center of the rotor, but is placed in the center of the stator. This creates a variable air-gap length which rotates with the rotor, i.e. is dependent on the rotor position and therefore also on machine speed [73].

To what extent eccentricity influences normal operation is discussed in [74]. The results show that the effect of possible eccentricity due to manufacturing tolerances should be considered during the drive design process by proper choice of rotor- and stator tooth width (tooth overlap during rotation). The air-gap length has a direct influence on the unbalanced magnetic pull. The smaller the air-gap length, the larger the effect which UMP has on the overall drive performance with respect to additional vibration.

Furthermore, different winding configuration can either worsen or mitigate the eccentricity effects on the drive. Connecting the machines phases in series causes much larger UMP compared to a machine with parallel connected phase windings. A parallel connection of opposite teeth windings causes a flux (current) balancing between the rotor teeth, resulting in a strongly reduced UMP acting on the bearings [73]. Therefore, with parallel windings the influence of manufacturing related asymmetries can be reduced.

The asymmetric force distribution due to an eccentricity causes an unbalanced force which excites secondary modes in addition to the initial vibration shapes which are discussed before. Investigations in [75], [76] show that the mode orders 1 and 2 are excited by UMP forces, regardless of the machine tooth configuration. In [76] a mathematical description for the excitation forces resulting from an eccentricity is derived. Thereby, eccentricity is described by a multiplication of two 2D Fourier series in space and time. From the mathematical representation it can be determined that a static eccentricity excites additional modes with the electrical harmonics, while in case of a rotating eccentricity mechanical-frequency side bands arise besides the initial electrical harmonics in the vibration spectrum of the machine.

Fig. 11 shows a simulated vibration spectrogram of an 18/12 automotive SRM without (Fig. 11(a)) and with a dynamic eccentricity (Fig. 11(b)). The additional frequency side bands from the dynamic eccentricity are well visible in Fig. 11(b).



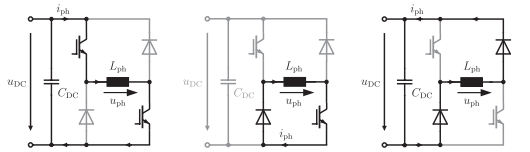
(a) Without eccentricity (b) With a dynamic eccentricity

Fig. 11. Simulated spectrograms with eccentricity from [76].

VI. Power Electronics

A. SRM Inverter

The SRM inverter has to supply a positive voltage across the phase to magnetize this phase and a negative phase voltage for the demagnetization. A third state, which supplies zero voltage across the phase and, therefore, keeps the flux at a nearly constant level, is optional but important in terms of inverter efficiency and noise reduction. The commonly used inverter topology for SRMs is the asymmetric half bridge [77]. The switching states of the asymmetric half bridge and the resulting voltage loops are shown in Fig. 12. One asymmetric half bridge per phase is necessary to control each phase independently from the other phases. To reduce the number of semiconductors and/or wires between inverter and machine different topologies are discussed in literature [77], [78], e.g. the Miller topology and C-dump converter.



(a) Magnetization (b) Freewheeling (c) Demagnetization

Fig. 12. Switching states of an asymmetric half bridge inverter.

B. DC-Link Capacitor

Switched reluctance machines need a comparatively large dc-link capacitor to smoothen the dc-link voltage due to the high amount of magnetization energy that oscillates between the dc-link and the machine [79]. A large dc-link capacitor increases the size, weight and price of the SRM inverter compared to inverters for conventional rotating field machines.

Recent publications recommend phase switching techniques to minimize the size of the dc-link capacitor [79]-[81]. These switching techniques aim at commutating the magnetization energy stored in one phase to the next active phase without buffering it in the dc-link capacitor. Additionally, in [81] a passive input filter is proposed to reduce the ripple on the source current. In [82] an active filter consisting of a bidirectional boost dc-dc converter is introduced (Fig. 13). The converter switches actively control the current between the

dc-link and the voltage source.

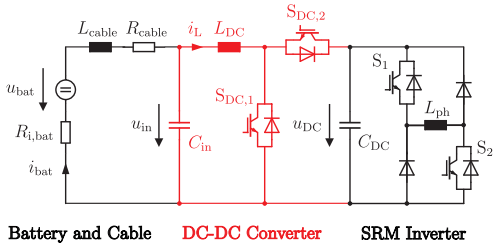


Fig. 13. Equivalent circuit of SRM with active filter [82].

VII. Control

For SRM control two main aspects are of interest: firstly, the position of the current pulse in each phase, which is controlled by the up to three parameter θ_{on}, θ_{free} and θ_{off}. Secondly, the shape of the current which is, at low speeds, controlled by a hysteresis or a PWM based switching scheme. The current shape strongly influences the instantaneous torque of the machine and is focus of many publications. At higher speeds, when the back-emf of the machine is in the range of the supply voltage, no switching is required to limit the phase current in single-pulse control (SPC). Many publications, such as [83], suggest ways to combine the control schemes for a smooth 4-quadrant operation of SRM in the full torque and speed operating range.

A. Current Control

The position dependent block-wise excitation of the sequential phases with a hysteresis current controller (HCC) is the most simple way to operate SRMs when smooth torque is not of interest (see Fig. 14). One potential to improve torque or acoustics is then to apply pre-calculated optimal current waveforms [84]. However a fast current acquisition and control device is required as for example proposed in [85]. If such a device is available, basically any desired current shape can be applied to the phase (see Fig. 15).

For efficiency reasons, above base speed most SRMs are operated in single-pulse control (SPC). In this operation mode, the current (and consequently torque) is controlled by the three switching angles mentioned before. With the position of the current pulses the behavior of the machine can be strongly influenced [8], [86], [87]. Output power control is mostly performed with a fixed θ_{off} (optimized for a specific design goal such as efficiency or acoustics) and by varying θ_{on} [87], [88].

In recent years, an additional focus has been laid on the potential to influence the system behavior by the third control parameter θ_{free} [89]-[91]. Especially at low speed operation this optimization offers significant efficiency improvement for inverter and machine as it reduces the iron losses in the machine by reducing ψ_{peak} [89], [91]. In [90] it is additionally found that even at nominal operation a short zero voltage period has a positive effect on the ac-losses caused by proximity effect in the machine windings. All optimizations have in common, that torque ripple is generally increased, hence are only applicable were this is not a major requirement.

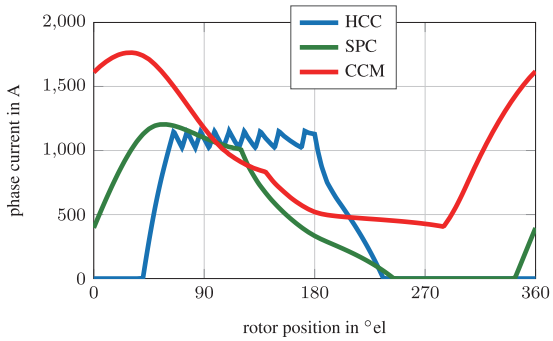


Fig. 14. Exemplary current shapes for different control modes.

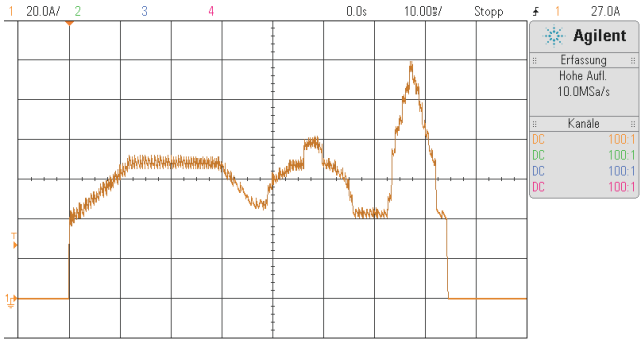


Fig. 15. Illustrating high dynamic current control in a 6-phase SRM. In this example the current waveform follows the outline of the cathedral in Aachen.

A significant torque boost at high speeds is offered by the so-called CCM [92] where the phase current does not reach zero any more. However, as it also increases the machine losses tremendously it is only applicable for short overload operation.

B. Torque Control

Pulsating torque is inherent to current controlled SRMs due to their doubly-salient structure and torque production principle. It is still considered as one of the main drawbacks of this drive technology. However, advances in power electronics and control hardware over the recent years have enabled the development of sophisticated control strategies that enable smooth torque output. The algorithms differ in their structure, implementation effort and operating range. The general goal of torque control schemes is to induce phase current waveforms such that the torque proportions of the single phases add up to constant torque output on the shaft. The different techniques can be roughly divided in several categories:

- indirect methods or current profiling methods
- direct torque control

Current profiling methods rely on offline or online computation of current profiles [94]-[96]. The profiles are derived by evaluation of experimental data or simulation and then

stored as a mathematical function or a look-up table (LUT). Based on the stored profile a torque sharing function delivers torque minimizing control parameters for a cascaded current controller and initiates a suitable phase commutation.

Most of the current profiling algorithms suffer from a limited operating range and do not consider the machine dynamics at higher speed. More advanced torque sharing functions consider further important criteria besides torque ripple minimization. Since different current waveforms can deliver constant torque for the same operating point, additional requirements can be considered, e.g. minimized rms current, which is similar to maximum-torque-per-ampere (MTPA) techniques for rotating field machines, or minimized flux and accordingly minimized iron losses (maximum-torque-per-flux- MTPF) [97], [98].

In contrast to indirect methods, direct instantaneous torque control (DITC) demonstrated in [99], [100] and predictive DITC [101], [102], a PWM version of DITC meant for microprocessor based hardware platforms, offer full flexibility and do not rely on predefined current profiles and commutation waveforms. Torque is estimated online, from a torque observer that uses the measured machine terminal quantities and a machine model (Fig. 17).

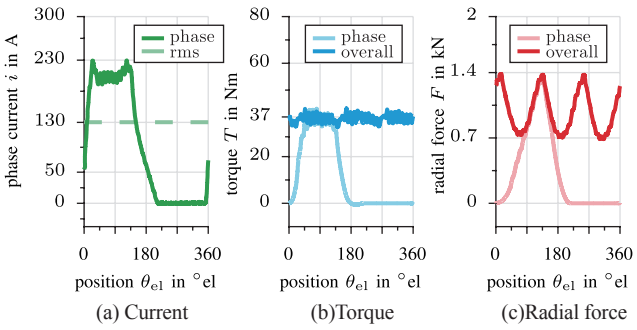


Fig. 16. Resulting trajectories applying DITC [93].

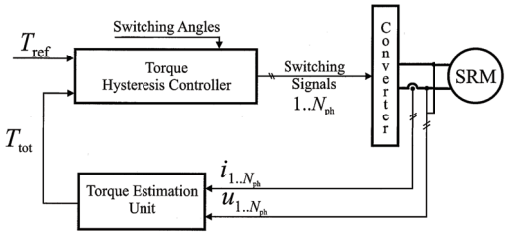


Fig. 17. Control diagram of DITC [100].

By controlling θ_{on} the current waveforms can be adapted to meet different secondary requirements like MTPA and MTPF optimization. The turn-on angle θ_{on} is varied depending on speed to ensure constant torque at higher speed. However, torque minimization techniques may reduce the system efficiency of reluctance drives [103].

Estimation of average torque, however, does not require pre-knowledge of the phase characteristics. This property of switched reluctance machines is used in [104] to develop direct average torque control (DATC) (Fig. 18). The estimated torque is compared to a reference value. The error is fed to a PIblock that adapts the control parameters of a cascaded current controller.

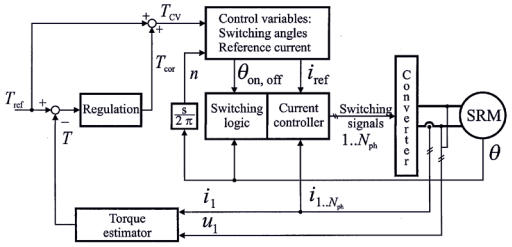


Fig. 18. Control diagram of DATC [104].

C. Acoustic Control

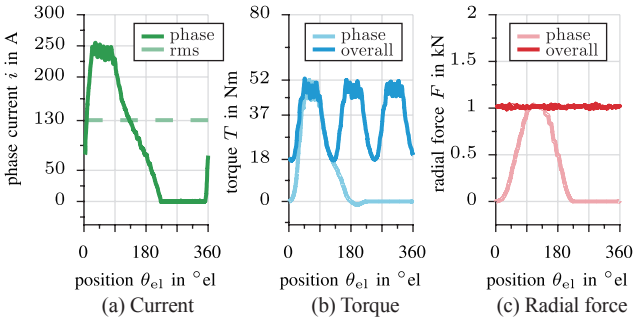
SRMs are prone to acoustic noise caused by stator vibrations due to high radial forces. Some research focuses on reducing actively the radial forces to overcome the noise issue [86], [87]. In [8] the influence of a switching angle dithering in singlepulse operation on the acoustics is investigated. However, recent publications [105]-[107] show that the vibration mode shape zero (M0), which is excited by a ripple on the overall radial force, is likely to be the predominant noise source in automotive-sized machines.

Therefore, recent approaches propose to keep the instantaneous overall radial force on a constant level. In [106]-[108] current profiles to fulfill this requirement are determined. Analog to DITC, in [7] Hofmann introduces the so-called direct instantaneous force control (DIFC), which calculates the required switching signals online to guarantee constant overall force. This approach can be implemented with PWM as well as hysteresis control [68].

Fig. 19 shows the resulting machine current, torque and radial force trajectories for a sample operating point applying DIFC. The brighter trajectories represent the phase torque and the phase radial force while the darker trajectories represent the overall torque and the overall radial force, respectively. The overall radial force is kept constant throughout the complete electrical period (Fig. 19(c)). A comparison of the synthesized run-up spectrogram for HCC and DIFC is shown in Fig. 20. Using HCC leads to increased surface velocity at the intersections of the eigenfrequency of mode shape zero (f_{M0}) with the 3rd and 6th harmonic of the electrical frequency (marked with white circles). DIFC is able to eliminate those peaks in the surface velocity.

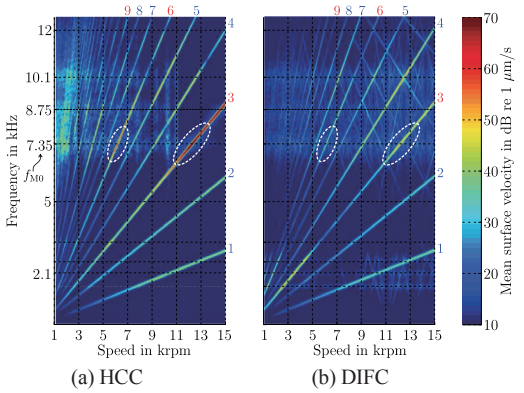
DIFC and the indirect approach for constant overall radial force have in common, that both increase the ripple on the overall torque (Fig. 19(b)). Torque ripple has also an effect on the acoustic behavior as well as on drive-train oscillations. In [109], an approach is presented that defines a current profile to reduce the peak value of the produced radial force per pole and simultaneously tries to reduce the torque ripple during commutation. However, it only aims at decreasing the radialforce ripple rather than eliminate it completely.

Direct instantaneous force and torque control (DIT&FC)



(a) Current (b) Torque (c) Radial force

Fig. 19. Resulting trajectories when applying DIFC [93].

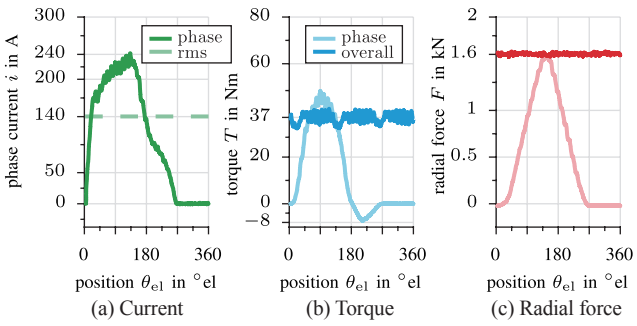


(a) HCC (b) DIFC

Fig. 20. Simulated run-up spectrograms of a three-phase 18/12 SRM [68].

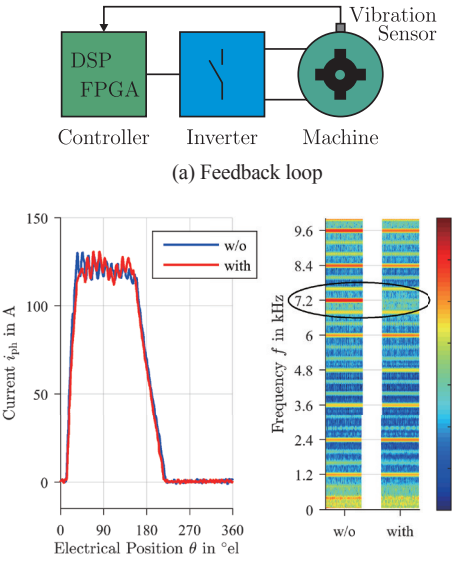
unifies DITC and DIFC to simultaneously eliminate torque and force ripple [93]. An online search algorithm determines the appropriate phase flux-linkages and switching signals to fulfill both requirements: constant overall torque and constant overall radial force. Sample current, torque and radial force trajectories are shown in Fig. 21. However, the two-fold control objective inherently reduces the drive efficiency due to an increased rms current [93].

All previously presented approaches have the drawback that they depend on predetermined machine characteristics or an offline post-processed parameter optimization. The proposed control optimization in [110] uses a vibration sensor feedback in the control loop to improve the acoustic behavior of the machine online during operation (Fig. 22(a)). Investigations have shown that the modulation of harmonic content on a control reference signal affects the acoustic behavior of the SRM. An online search algorithm determines the optimal modulation parameter. Fig. 22(b) shows a proof of concept. The increased surface velocity at the mode-zero eigenfrequency (7.2 kHz) is totally eliminated while the overall torque and overall radial force trajectories are barely affected by the modulation. The approach is independent of the used control method and can also be applied with, e.g. DITC.



(a) Current (b) Torque (c) Radial force

Fig. 21. Resulting trajectories when applying DIT&FC [93].



(a) Feedback loop

(b) Current control with and without vibration sensor feedback

Fig. 22. Vibration sensor feedback to the controller [110].

D. Self-Sensing of SRMs

A number of methods for position sensorless operation of SRMs have been studied in literature. Most techniques take advantage of the doubly salient geometry of SRMs which results in strongly position dependent flux characteristic. The flux characteristic (though nonlinear) is a defined function between phase current, flux linkage and rotor position (Fig. 23). The knowledge of two quantities is sufficient to estimate the third, provided that the characteristic is available. Methods for deriving the motor characteristics are discussed in Chapter IV.

Various approaches to extract the rotor position from the phase characteristic have been presented in literature. Comprehensive studies giving an overview over sensorless techniques are presented in [111]-[113]. The main classification

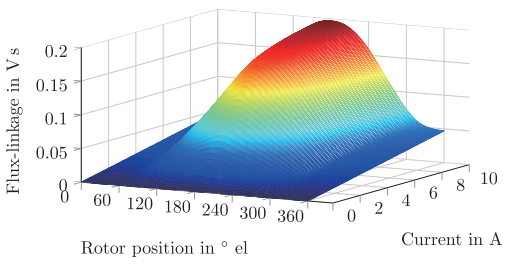


Fig. 23. Typical phase characteristic of a switched reluctance motor.

criteria can be listed as follows:

- **Phase state:** active or passive phase methods depending on whether the phase is also used for torque production or not
- **Hardware effort:** depending on how much computational power is necessary and whether additional sensing hardware is used
- **Speed range:** defining the range in which the algorithms are applicable
- **Periodicity of measurement:** Continuous detection of rotor position or detection at certain defined rotor position
- **Signal injection:** direct methods, that apply signal injection to detect the rotor position and indirect methods that make use of the terminal quantities only.

A commonly applied active phase approach is the flux-linkage method [114]. It does not require additional hardware and estimates the rotor position from the measured phase current and applied flux linkage. However, a machine model must be available, usually derived from finite element simulations or static measurements and stored as a LUT. Since flux linkage is derived by integration of the phase votlage the algorithm is not suitable for near zero speed. Further modifications and improvements of the flux-linkage method are suggested in [115], [116]. Another approach to improve the position detection is to employ additional filters and self-calibration routines [117]. Other common active phase methods employ current monitoring, current gradient measurements and various model observer [118], [119]. One of the first approaches for stepper application of SRMs without position sensor is presented in [120].

Sensorless operation over the complete speed range can be achieved by combining the flux-linkage method with signal injection methods in the low speed and low torque area. Current signals with small magnitude, typically a fraction of the rated value [118], are injected in one of the idle phases to estimate the phase inductance and derive the rotor position. However, signal injection methods can lead to undesired torque production in the machine and worsened acoustic behavior.

E. Control Hardware

Switched reluctance machines cannot be fed directly from the power grid or be applied as generators without dedicated power electronic converters and active switching strategies implemented in digital or analog electronic circuits. When SRDs were introduced, digital computation devices were not available or not powerful enough to accommodate the sophisticated control strategies, that minimized torque ripple or acoustic noise. This is one of main reasons why switched reluctance drives have been disregarded for a long time.

Nowadays state-of-the-art control platforms for SRMs are based on digital signal processors (DSPs), similar to rotating field machines. They allow fast computation, storage of machine characteristics and tracking of terminal quantities. Lately field programmable gate arrays (FPGAs) are getting attractive as a control hardware for SRDs due to their oversampling capability and high parallelization grade. The rapid development and the steadily decreasing cost of FPGAs makes them a viable option to DSPs. In mass production FPGAs can be replaced by custom chips called ASICs (application-specific integrated circuit) to reduce the hardware cost. An example for a commercially available chip enabling sensorless control of SRMs is given in [121]. Modern chips containing both DSP and FPGA blocks gain attention for motor control due to their flexibility. Timely critical control tasks can be assigned to the FPGA while the microprocessor takes over more complex high level control (Fig. 24).

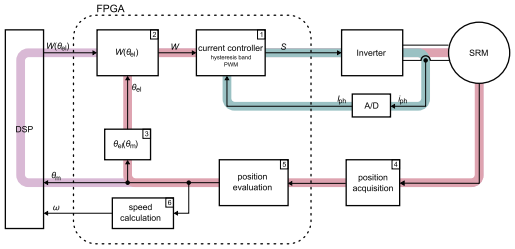


Fig. 24. Controller structure in a combined DSP-FPGA platform [85].

Depending on the target hardware different implementation techniques need to be applied. DSPs execute their program sequentially and usually have fixed interrupts. Depending on the complexity of the control algorithm and the processor performance control of electrical frequencies of up to several kHz are possible. Due to the limited signal tracking capability compared to FPGAs, DSPs are usually the target hardware for PWM based algorithms.

Hysteresis based algorithms however, where the switching action directly depends on values of the terminal quantities, are generally more suited for FPGA target hardware. Conventional hysteresis current control as well as torque and force controllers like DITC, hysteresis based DIFC [20] and various current profiling techniques benefit from an FPGA implementation. A fully FPGA-based current controller including both PWM and hysteresis band modulation was demonstrated in [85]. The FPGA implementation of state of the art predictive DITC is discussed in [122]. The advantages of FPGAs can be exploited for high-grade position detection techniques as in [117].

In particular the choice of hardware depends mainly on the system dynamics. Especially highly dynamic SRMs and highspeed drives require fast signal tracking. Devices operating with fixed switching frequency as most DSPs can switch only at discrete time steps. At high speed, this leads to a turnon angle uncertainty, i.e. the exact turn on angle cannot be met and phase commutation takes place earlier or later than desired (Fig. 25). This effect can lead to power oscillations and consequently to a limitation of the operating range.

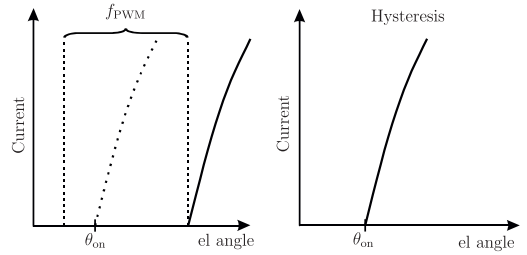


Fig. 25. Turn-on uncertainty of PWM algorithms at high speed.

VIII. SRM in Application

Today, SRMs are found in a number of niche products throughout the industry, some of which are discussed in this section. Furthermore, the section highlights the current research landscape dealing with SRMs followed by an outlook on open research topics to be tackled in the near future.

A. Available Solutions

For household applications the best-known companies using switched reluctance machines are Vorwerk and Dyson. The first and second generations of Vorwerk's Thermomix use a 500W SRM with a speed range of 40 rpm up to 10 700 rpm [123]. Furthermore, the Kobold 140/150 vacuum cleaner by Vorwerk has a 900W SRM with speeds of up to 60 krpm [124]. A further industrial vacuum cleaner with SRMs is constructed by Ametek [125]. Even higher speeds and therefore an even higher power density is used by Dyson in their vacuum cleaners and hand dryers. The hand dryers use a one pole-pair SRM with speed up to 90 krpm and 1600W nominal power [126].

Other high-speed applications such as weaving machines or centrifuges use SRMs as well. The company Picanol uses reluctance machines from the company Nidec SR-Drives for weaving machines [127], while the company Beckman Coulter exploits the benefit of low rotor inertia and the resulting fast acceleration of SRMs in their centrifuges. The centrifuges are operated between 10 krpm and 30 krpm [128]. The airconditioning compressor unit of German ICE3 high-speed passenger train is powered by an SRD with up to 40 kW at 23 krpm also from Nidec SR-Drives [129]. A further application benefiting from the low rotor inertia and resulting small time constants are electric compressors, e.g. electric turbo chargers. The company Valeo proposes a near future entry into the automotive market. The proposed SRM, on 12 V and 48 V basis is designed to accelerate up to 70 krpm within 350 ms and 200 ms respectively [130], [131].

Another application designated for SRM are power tools. The company Hilti uses a special form of one phase SRM with magnets in the stator for demolition hammers and diamond grinders up to 1800 W and 22 krpm e.g. TE 1000-AVR or DG150 [132]. In these applications torque ripple and vibration (acoustic noise) are not an issue, highlighting the SRM's advantages in respect to cost and robustness. Robustness and low maintenance is also a crucial advantage in the highpower application of wheel-loaders. LeTourneau (since 2002) and more recently John Deere (since 2013) employ Nidec SR-Drives technology in one of their biggest hybrid electric systems [133].

B. Research and Development

Giving a complete overview on the SRM application research landscape is quite impossible. However, some applications have received increased attention from researchers all over the world. One topic are high-speed turbo machines and generators due to their robust rotor structure. A wide overview can be found in [134]. Especially aircraft starter-generators and fuel pumps in the range of several ten kW have already been investigated by many working groups [135]. Another focus is the automotive industry searching for magnet-free traction drive alternatives for the roll out of millions of electric cars [136]. The cost advantage of SRDs also plays an important role in range extender (and backup power) systems presented in [137].

IX. Conclusions

Over the past decades, all major issues of SRDs have been addressed. Hence, SRDs are ready to be implemented in applications, if the requirements necessitate its main advantages. Compared to common rotating field machines, these advantages are large speed-range, the possibility for a high torque overload, high torque dynamics, a simple and robust mechanical construction (e.g. one phase machines), low-cost production and the exclusion of rare-earth materials. In lowspeed applications, with regard to the SRD's acoustic behavior, power density and efficiency, the SRM cannot outperform rotation field machines, despite the advances in control and design that are shown within this paper.

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Topologies and Control Strategies of Very High Frequency Converters: A Survey

Dianguo Xu, Yueshi Guan, Yijie Wang, and Wei Wang

***Abstract*—with the fast development of power electronics, very high frequency (VHF) power converters (30–300 MHz) gradually become research focus, which can greatly reduce the value, volume of passive components and help to improve the system power density. However, at such high operating frequency, many challenges have been proposed, such as switching characteristics, topologies characteristics and control methods. This paper starts from the development background of VHF power converters, and an overview of VHF development is described. Different topologies adopted in VHF condition are introduced and compared. At the same time, the resonant driving strategies and control methods for very high frequency converters are discussed and analyzed, which can provide guidance for further research of VHF converters.**

***Index Terms*—Very high frequency power converters, topologies, resonant driving, control strategies.**

I. Introduction

WITH the development of power electronics technique, very high frequency (VHF, 30~300 MHz) power converters have gradually become a hot field of research directions. By increasing the working frequency of the system, the VHF power converters can effectively reduce the volume of the passive components, and improve the power density. Meanwhile, the transmitted and stored energy of components during each operating period can be significantly decreased due to the increase of the frequency. Thus the speed of the transient response can be accelerated. The decrease of the value and volume of passive components is beneficial to the integration and manufacture of the system.

The topologies of VHF converters are proposed through a combination of RF power amplifier technology and power electronic technology [1]-[8]. The power amplifier can transform DC components into high frequency AC components, which is similar to the inverter stage of Switching Mode Power Supplies (SMPS). Nowadays, many researchers have focused on the research of VHF power converters based on the existing topologies. Combining the inverters with the corresponding rectifiers, different topologies of the VHF power converter have been proposed [9]-[64], which own excellent characteristics, such as small volume, high power density and fast response speed. Although the VHF system has such merits, the high switching frequency puts forward strict requirements on the selection of semiconductor devices [21]-[28], the utilization of parasitic parameters [29]-[36], the design of the circuit [37]-[42] and the design of passive components [43]-[49].

In the VHF power converters, with the increasement of system switching frequency, switching losses also increase rapidly. Thus, the losses of the switch and the driving circuit must be reduced to ensure a high system efficiency. In the existing VHF power converters, scholars mainly adopt zero voltage switching (ZVS) technology to reduce the power losses caused by the overlap of voltage and current at the instant of switching. Besides, to reduce the driving circuit losses, the resonant driving circuit is also proposed which can utilize the energy stored in the switch input capacitor.

Apart from the topologies and the driving methods, another important aspect of VHF converters is the control method. For traditional converters, pulse width modulation (PWM) or pulse frequency modulation (PFM) is used to adjust the drive signal of the system in close-loop control. However, both methods are not available to be adopted in VHF situations. Because in such a high frequency condition, it is difficult to sample and adjust the duty cycle or the operating frequency of driving signals. At the same time, the change of period or duty cycle will affect the operating modes of switches. Thus some suitable control methods have been researched to regulate the output voltage and keep the switch operating in soft-switching modes when the input voltage or load change.

In this paper, introduction and detailed analysis of advanced technologies in VHF power converters are presented. Based on existing VHF power converter topologies, the design principle of VHF topology is introduced. The characteristics of different inverter stages, rectifier stages and matching networks are analyzed in Section II. The driving methods of the VHF system are explored in Section III. An overall analysis and comparison of the self-resonant driving circuit and multi-resonant driving circuit are given. The control strategies of VHF power converter are discussed in Section IV. Section V elaborates the opportunities and chal-

Manuscript received March 20, 2017.This work was supported in part by Lite-On Power Electronics Technology Research Fund, in part by the National Natural Science Foundation of China under Grant 51407044, in part by the Research and Development of Applied Technology Projects in Heilongjiang Province under Grant GA13A403, in part by the Fundamental Research Funds for the Central Universities under Grant HIT.BRETIII.201510, and in part by the China Post-Doctoral Science Foundation under Grant 2014M550187 and Grant 2015T80348.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00004

lenges in the field of VHF power converters.

II. Topologies of VHF Power Converters

A. Overview of Topologies

As shown in Fig. 1, the circuit topology of VHF DC-DC converter is usually composed of three parts: inverter stage, matching network and rectifier stage. The inverter stage transforms DC voltage into AC voltage. The rectifier stage regulates AC voltage into constant DC output voltage. Resonant and soft-switching technologies are adopted in the inverter and rectifier in order to reduce the system switching losses. Between inverter and rectifier stage, the matching network is used to adjust the equivalent load of the rectifier, so that the converter can achieve the required output power.

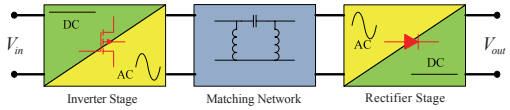

Fig. 1. The diagram of VHF power converters.

In the VHF conditions, the switching losses of the switch and diode increase rapidly. To ensure the efficiency of the system, the switch and diode should achieve soft-switching to decrease losses. In the present researches, most of the VHF circuits are based on the single switch structure to avoid floating drive. Combining with different structures of VHF power amplifiers, Class E topology [50], [51] and Class Φ_2 topology [52]-[55] are used to constitute the inverter and rectifier stage. The following sections will introduce these three parts in detail.

B. The Analysis of Inverter Stage

Fig. 2 shows the diagram of Class E resonant inverter circuit. The inductor L_F, capacitor C_F and the corresponding resonant tank constitute Class E inverter network. It should be noted that C_F is the sum of the output parasitic capacitor of the switch and the parallel discrete capacitor. When the switch is off, inductor L_F and capacitor C_F resonate. To reduce the switching losses under VHF conditions, the switch should operate at ZVS state. Through comprehensive design of the resonant frequency, operating frequency and duty cycle, the voltage across the switch can exactly be zero when the drive signal comes, therefore the soft switching characteristic is achieved. In ideal situations, the parasitic capacitor

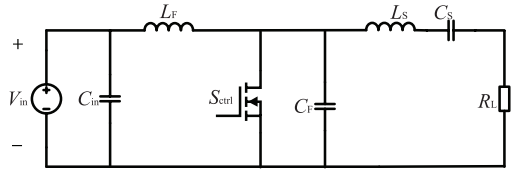

Fig. 2. Circuit of Class E type resonant inverter stage.

of the switch can exactly act as the resonant capacitor in the inverter stage, so there is no need to add extra capacitor. However, the parasitic output capacitance of the switch varies with its type, and the value of the parasitic capacitor changes nonlinearly while the drain-source voltage changes. So a parallel discrete capacitor is generally necessary.

Although the topology of the Class E inverter stage is simple, and the switch can work in soft-switching state, the major defect is that the switch's drain-source voltage stress is very high. When the duty ratio of the switch is 50%, the drain-source voltage stress is about 3.6 times of the input voltage, which means that the switch with high rated voltage has to be adopted. Also the cost of this system increases. With high voltage stress, the application area of this topology is greatly restricted.

According to these problems, scholars expect the introduction of higher harmonics to reduce the peak voltage across the switch. Fig. 3 shows the peak voltage across the switch is effectively reduced by superimposing the fundamental and third harmonic voltages. Based on above method, the Class Φ_2 inverter, as shown in Fig. 4, is proposed and is widely used in VHF power converters [52]-[57]. The topology can meet the soft switch requirement and effectively reduce the voltage stress across the switch.

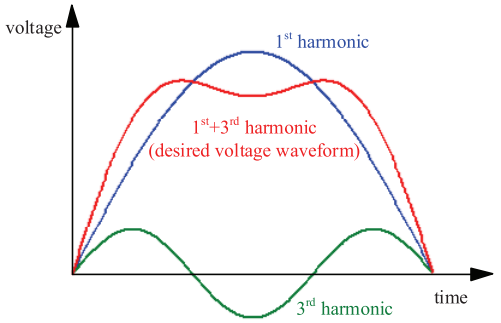

Fig. 3. The desired voltage waveform with the addition of third harmonic.

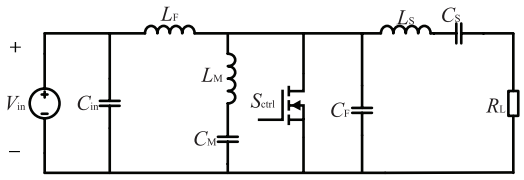

Fig. 4. The circuit of Class Φ_2 type resonant inverter stage.

The Class Φ_2 inverter is derived from Class E circuit. The input resonant network consists of L_F, C_F, L_M and C_M. In parameter design process, to make the switch drain-source waveform presenting a low impedance at the second harmonic frequency, the resonant frequency of L_M and C_M is set to be close to twice of the switching frequency. Then the resonant tank should be adjust to exhibit high impedance at the fundamental and three harmonic frequency with proper L_F and C_F. Since the superposition of one and third harmonic, the voltage waveform across switch is in approximately trap-

ezoidal form. The voltage stress of switch can be reduced to twice of the input voltage, thus the topology can be adopted in wide application fields. Meanwhile the switch is still able to maintain an excellent ZVS characteristic. However compared with Class E resonant rectifier topology, the introduction of L_M and C_M increases the size and cost of the system, also improves the complexity of circuit design. Therefore, the inverter topologies of VHF power converters should be selected considering different system requirements.

C. The Analysis of Rectifier Stage

In VHF DC-DC power converters, the inverter stage converts the DC signal into a high frequency AC component, and the rectifier converts the AC signal into a DC output signal with the desired amplitude. Meanwhile in VHF power converter the rectifier circuit also decides the impedance across the switch. For the design of the resonant rectifier circuit, the ideal working state is that the input fundamental voltage and current are in the same phase. Thus it can reduce the circulating current and improve the rectifier efficiency. In this condition, the rectifier can be replaced with a resistor. In very high frequency conditions, the ZCS characteristic of the diode can also be realized by the resonance of the inductor and capacitor, which can reduce the switching losses of the diode.

Fig. 5 and Fig. 6 show two commonly used resonant rectifier circuits respectively, they can be deduced from the Class E inverter according to duality characteristics [58], [59]. Each resonant rectifier circuit consists of a resonant inductor L_R, a resonant capacitance C_R and a diode D_1, C_R includes the parasitic capacitance of the diode. When the diode is turned on, the diode anode voltage is clamped by the output voltage. In contrast, when the diode is turned off, the inductor and capacitor begin to resonate in order to achieve the ZCS characteristic of diode. According to the different types of input source, the circuit shown in Fig. 5 is called the voltage-driven rectifier circuit and the circuit shown in Fig. 6 is called the current-driven rectifier. They all provide a DC path from the input side to the output side. The advantage is that the DC component can be used to deliver part of the required energy, reduce system losses and improve efficiency. However the disadvantage is that the output voltage must be higher than the input voltage, it means the converter can only be used in step-up condition. A DC blocking capacitor is necessary when to achieve step-down conversion.

Although the diode operating in ZCS state can effectively reduce the switching losses. In the resonant rectifier, the

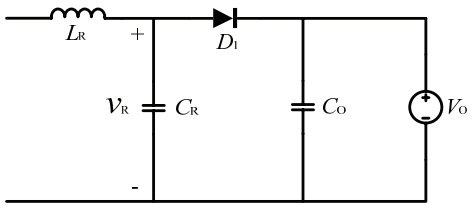

Fig. 5. Voltage-driven Class E resonant rectifier stage.

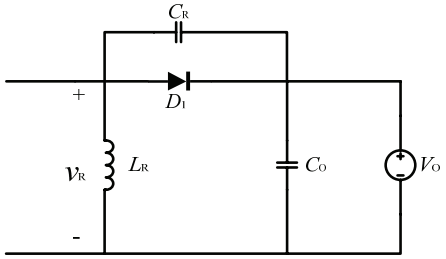

Fig. 6. Current-driven Class E resonant rectifier stage.

diode conduction voltage drop will also cause great losses. Especially in the low output voltage conditions, the system efficiency will be greatly compromised. To solve above problems, a new method based on synchronous rectification is put forward, in which the diode is replaced by a switch. The switch is driven by proper signal to achieve the required rectifier characteristics. With low conduction voltage drop, the method can effectively reduce the conduction losses. However an extra driving circuit must be added which increases the driving losses. Besides, the driving signal of synchronous rectifier switch and inverter switch need to meet a specific time relationship which is very difficult in VHF situation. Therefore, the proper rectifier stage of the VHF power converter should be decided according to the specific requirements of the system.

D.The Analysis of Matching Network

As the diagram of VHF DC-DC power converter shown, a matching network is usually added between the inverter and the rectifier, which can play the role of impedance conversion. As mentioned above, the input voltage and current of rectifier are usually designed to be in the same phase. Then the rectifier circuit can be represented by an equivalent impedance, which can be transformed by the matching network to meet the requirement of the impedance value under the required output power. There are two kinds of matching networks: isolated type [11], [24], [60] and non-isolated type [56]. The isolated type matching network adopts the transformer as the impedance conversion element which can realize the electrical isolation between the system input and output side. In a wide frequency variation range, the transformer owns a constant impedance conversion characteristic. However, in VHF condition, the transformer will introduce more non-ideal parameters, such as parasitic capacitance, leakage inductance, magnetizing inductance. Based on optimization design, the transformer leakage inductance and magnetizing inductance can be effectively absorbed and utilized. However, the parasitic capacitance cannot be eliminated because of the facing area between adjacent windings, which affects the performance and operating mode of the system. So in the applications without the requirement of electrical isolation, the non-isolated matching networks are widely adopted.

Fig. 7 shows the topologies of some commonly used non-isolated matching networks. From the point of frequency domain characteristics, these matching networks can

be divided into low-pass matching network and high-pass matching network. In VHF power converters, the high-pass matching network is more suitable because it can transfer the energy of the fundamental waveform and other high harmonics to the load. It means the energy of the inverter can be fully utilized compared with low-pass ones. Fig. 7(b) is the simplest structure of high-pass matching network, which is called L type. It contains only one inductor L_S and a capacitor C_S. Meanwhile the capacitor C_S is connected in series with the load which can play a role of DC blocking capacitor. With this matching network, the converter can achieve step-up and down conversion. At the same time, combining the L type matching network with the current-driven rectifier, the inductor L_S of matching network and the inductor L_R of rectifier can be merged to one inductor, which effectively reduces the component number and the corresponding losses. Fig. 7(d) and Fig. 7(f) show the π type and T type matching network. With optimal design, these two circuits can ensure constant impedance angle conversion under load variation conditions, which is conductive to ensure the soft switching characteristics of the switch at different output power. The non-isolated matching network can only achieve the required impedance transferring ratio at a certain frequency. When the operating frequency of the matching network changes, the impedance transferring ratio will change, which affects the switch operating mode. Therefore considering the advantages and disadvantages of different matching networks, the topology of matching network should be selected according to the system specific requirement.

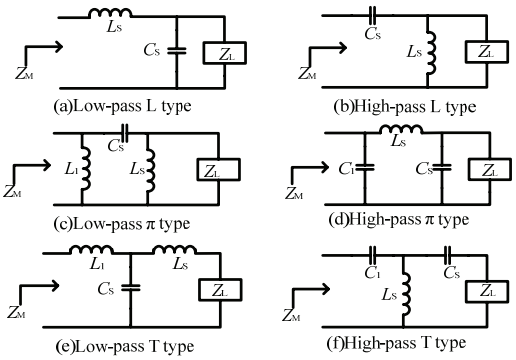

Fig. 7. The diagrams of different non-isolated matching networks.

E. Typical Topologies of VHF Converters

Based on the different types of the inverter stage, the rectifier stage and the matching network, many VHF power converters with different characteristics are gradually proposed. Fig. 8 shows the circuit of the SEPIC VHF power converter proposed in article [56], the inverter stage is Class E topology, the rectifier stage is current-driven resonant topology, and the matching network is L type high-pass network. As mentioned above, the inductance L_R is the equivalent inductance of the matching network and the rectifier stage. Here C_T also plays the role of DC blocking capacitor, thus this converter owns both step-up or down voltage transferring ability.

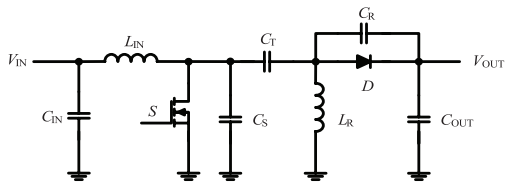

Fig. 8. Schematic diagram of a SEPIC VHF converter proposed in [56].

Fig. 9 shows the circuit diagram of the Boost VHF power converter proposed in article [54], [57]. The inverter stage is ClassΦ_2 topology; the rectifier stage is voltage-driven resonant topology. In this prototype, the equivalent impedance of the rectifier meets the inverter requirement. Thus the matching network is not added in this circuit. As can be noticed from the schematic, because of the absence of the DC blocking capacitor, this converter can only provide stet-up power conversion. Fig. 10 shows the circuit diagram of the isolated VHF power converter proposed in [11]. The inverter stage is still ClassΦ_2 topology. Here the rectifier stage adopts synchronous rectifier resonant topology, which can reduce the conduction losses. Meanwhile, a transformer is adopted here to be the matching network, so the electrical isolation between the input side and output side is achieved. The leakage inductances in primary side and secondary side are both absorbed by the resonant inductor of rectifier stage, which can reduce the magnetic components in the high frequency converter. Meanwhile, the effect of parasitic inductances can be reduced by the optimal design.

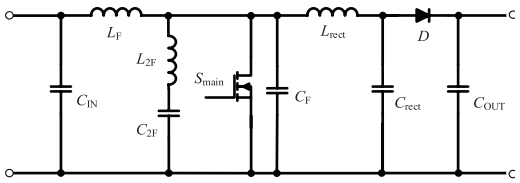

Fig. 9. Schematic diagram of a Class Φ_2 based Boost VHF converter.

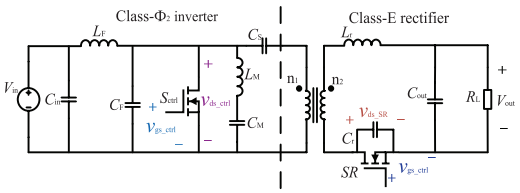

Fig. 10. Isolated Class Φ_2 resonant converter.

F. Novel Topologies of VHF Converters

Based on the aforementioned typical topologies, some scholars begin to propose some new topologies, such as the interleaved VHF converters, the bidirectional VHF converters and the half-bridge VHF converters.

Similar to the application of the interleaved technology in low frequency condition, the input current ripple of VHF power converter can be reduced when two complementary signals are applied to drive the two interleaved circuit mod-

ules. The schematic of the interleaved VHF converter based on Class E topology is shown in Fig. 11. In article [61], this prototype is used as the LED driver operating at 120 MHz. The output power is 3-9 W, and the efficiency is 80%~89%. The application of the interleaved technology can effectively reduce the input and output ripple, so that this converter can be applied in high power fields. However, the tiny deviations of the two circuit modules may result in the offset of the system's optimal operating point. In such high frequency condition, the differences of two modules will greatly affect the system nominal operating mode.

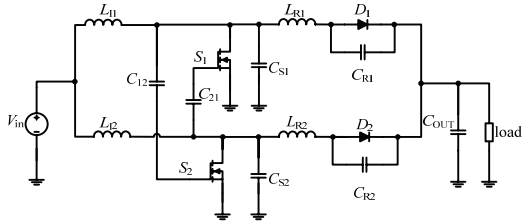

Fig. 11. Schematic view of the interleaved class E converter from [61].

As seen in Fig. 12, the diode in the rectifier stage is replaced by a switch, then a bidirectional VHF converter is obtained [62]. This converter is composed of Class E inverter and Class E synchronous rectifier. When the circuit operates in forward transferring mode, S_1 acts as the power switch, S_2 acts as the synchronous rectifier diode. When the circuit runs in reverse transferring mode, the roles of the switches are opposite to the former. Besides having the ability to conduct bi-directionally, this converter can also effectively reduce the conduction losses of the rectifier stage by introducing the synchronous rectifier switch. However, as mentioned above, this topology requires an extra driving circuit, and the two driving signals must satisfy a specific logical relationship at high frequency, which is a great challenge for the design of driving circuits. As mentioned in the former section, the

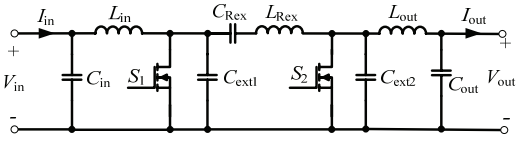

Fig. 12. Schematic diagram of a VHF converter with class-E inverter and synchronous class-E rectifier.

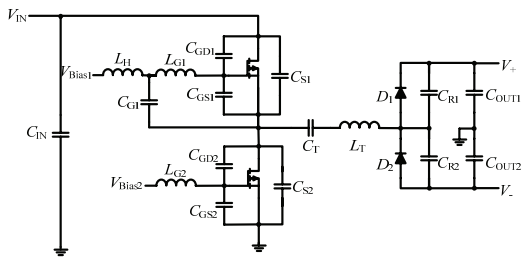

Fig. 13. Schematic diagram of a VHF converter with class-DE inverter and rectifier.

scholars try to avoiding the applications of half-bridge topology in VHF converters. The floating driving method of the top switch is difficult to solve in half-bridge structure. But a natural advantage of this topology is that the voltage stress across the switch is very low, for the switch is directly connected with the input voltage, the stress is equal to input voltage. Based on Class DE half-bridge inverter topology [64] and Class DE rectifier topology, a VHF converter is presented in [63], as shown in Fig. 13. Self-resonant driving method is proposed in this paper. The half bridge circuit is very suitable for the applications where high input voltage or output voltage is required. In addition, compared with the other topologies mentioned above, the power circuit of the converter presented in Fig. 13 only contains one inductor, which is beneficial to improving the power density of the system.

III. Driving Methods of VHF Power Converters

In VHF power converters, with the increasement of operating frequency, the losses of the driving circuit also increase rapidly. In the low frequency power converters, the most commonly used driving circuit is square wave driving circuit in which the switch driving signals are square waveforms. In this case, the driving losses are caused by the charging and discharging energy dissipation of the parasitic capacitance C_{gs}. The losses of the driving method can be calculated by $C_{gs}V_g^2f$, where V_g is the amplitude of driving voltage and f is the driving frequency. As can be seen, the power losses are proportional to the operating frequency, the high driving losses in VHF converter greatly restricts the improvement of high frequency system efficiency.

A. Analysis of VHF Resonant Driving Circuit

In order to solve the above problems, the concept of resonant driving circuit has been proposed in recent years [65]-[70]. Compared with the square wave driving circuit, the most obvious difference of the resonant driving circuit is that the driving voltage is in sinusoidal or approximately sinusoidal form, which can use the energy of switch parasitic capacitance. Thus, the driving losses can be reduced. Fig. 14 shows diagram of the simplest resonant driving circuit. A series resonant inductor L_{res} is added in the circuit. In Fig. 14, R_g is the gate resistance of switch, R_l is the equivalent resistance introduced by other components in the driving circuit.

In the traditional square wave driving circuit, the energy

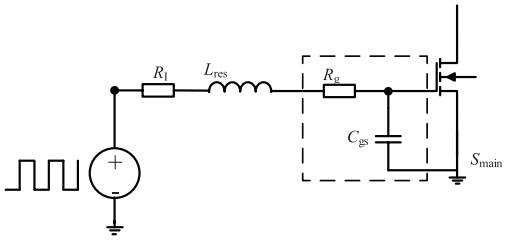

Fig. 14. Schematic diagram of resonant circuit.

stored in the input capacitor C_{gs} is completely consumed during each switching cycle. However in the resonant driving circuit, the energy is converted between the capacitor and the series resonant inductor in the form of electromagnetic energy. Ignoring the small equivalent resistance R_I in the driving circuit, the losses are only caused by the gate parasitic resistance R_g. The losses can be calculated by $2R_g\pi^2 f^2 C_{gs}^2 V_{g,ac}^2$, where V_{gac} is sinusoidal driving voltage amplitude. For the switch of MRF6S9060, comparing the power losses of the above two driving methods, the losses of the resonant driving circuit are much less than that of the square wave driving circuit [70].

Fig. 15 shows a typical VHF sinusoidal resonant drive circuit based on the external oscillator signal, in which the control method will be introduced in the next section. This circuit reduces the current flowing through the equivalent resistance R_I by introducing a parallel branch which consists of an resonant inductor L_p and a resonant capacitor C_B. So the losses of equivalent resistance R_I can be reduced and the efficiency of the resonant driving circuit can be further improved. In the driving circuit, U_3 is a CMOS inverter and S_1 is an auxiliary switch. When the control signal is in low level, the output signal of U_3 is high, and the auxiliary switch turns on. The additional circuit can accelerate the shutdown process.

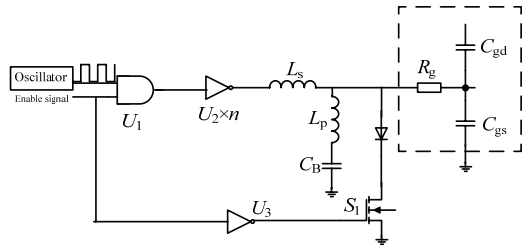

Fig. 15. The typical VHF resonant circuit based on external oscillating signal.

The aforementioned resonant driving circuit owns many advantages, such as simple structure, high reliability, and high efficiency. However, the rising and falling edge slopes of the sinusoidal driving signals are slow which increases the average on-resistance of the switch during the switching period. To solve the above problems, some scholars have proposed trapezoidal wave driving method which can speed up the rise and fall edge of driving signal. Also there is no negative voltage in this trapezoidal driving signal. But the structure of trapezoidal wave driving circuit is complex. There are many components in the circuit which is not conducive to the improvement of power density.

B. Analysis of Self-Resonant Driving Circuit

The above mentioned resonant driving circuits have been widely used in VHF power converters. However, these methods require many components, such as oscillator, AND gate, CMOS inverter, auxiliary switch, etc. These components will increase system cost and reduce system reliability. To solve above problems, the self-resonant driving circuits have been adopted in VHF condition.

Within the above mentioned VHF power converters, the switch drain-source voltage waveform is always in approximate half-wave sine form. When the switch is turned on, the drain-source voltage is in low level, and the driving voltage is in high level. When the switch is turned off, the situation is just the opposite. From the perspective of phase, there is an almost 180 degree phase difference between the driving voltage and the drain-source voltage. According to above analysis, a passive network is expected to be designed, which can feed back the drain-source voltage to the gate with an almost 180 degree phase difference. Meanwhile with the adjustment of the feed-back voltage amplitude, a self-resonant driving system can be built with a proper feed-back network.

Fig. 16 shows a VHF self-resonant driving circuit based on series resonant inductor [71]. In the circuit, L_G is the resonant inductor and V_{bias} represents the bias DC voltage. Based on the inductor and the switch parasitic capacitors, a high-pass filter with the capacitive load is formed. The transfer function V_{ds}/V_{gs} needs to be carefully designed to satisfy the requirements. Fig. 17 shows the Bode diagram of the feed-back network with different series inductance parameters. As can be seen from the figure, the network can achieve about 180 degree phase difference within certain frequency range. By changing the value of inductances, the voltage gain at the operating frequency can be adjusted to meet the amplitude

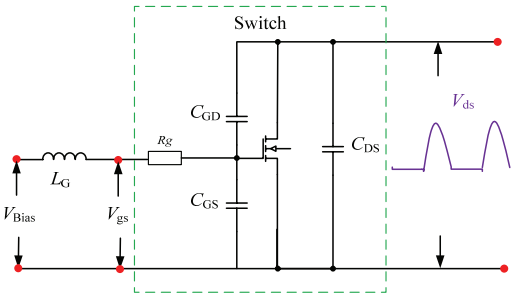

Fig. 16. Circuit of a self-resonant VHF driving circuit.

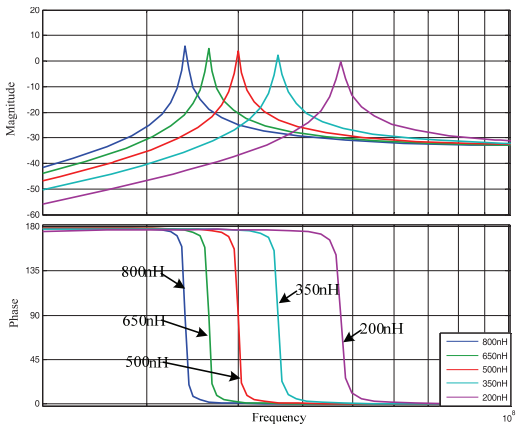

Fig. 17. The bode plots of self-resonant circuit with different inductor values.

requirement of different switches. The bias voltage V_{bias} can be adjusted to change the switch duty cycle with different threshold voltages.

Although the above mentioned self-resonant driving circuit has a simple structure, the network performance mainly depends on the parasitic parameters of the selected switch. For many switches, the feed-back network cannot achieve 180 degree phase difference. Meanwhile the amplitude of the driving voltage is proportional to the input voltage. With the increasement of input voltage, the driving voltage may exceed the switch allowable voltage, which restricts the application fields of the self-resonant circuit.

To solve the above problems, paper [72] proposes a VHF self-resonant driving circuit based on the auxiliary switch as shown in Fig. 18. The driving circuit adopts Class E resonant circuit. Based on the proper feed-back network, the auxiliary switch is driven by the self-resonant signal. Then the drain-source voltage of the auxiliary switch is used as the driving voltage of the main switch. With proper DC bias voltage, the driving signal is independent of the input voltage of the power circuit. Meanwhile an inductor L_{start} is added between the gate of the auxiliary switch and the DC voltage source, which can fasten the switch transition. Although the structure solves the problem of self-resonant driving circuit based on series inductor, the driving method is more complicated and needs many components.

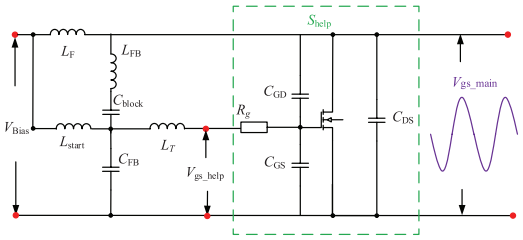

Fig. 18. The VHF self-resonant circuit based on an auxiliary switch.

IV. Control Strategies of VHF Power Converters

Apart from the topology structures and the driving methods, another important factor of VHF converters is the control method. For traditional converters, pulse width modulation (PWM) or pulse frequency modulation (PFM) is used to adjust the system driving signal, and finally the system's closed-loop control can be achieved. However, both methods are difficult to realize in VHF situations. As for PWM, the ZVS characteristic of the switch in the VHF system is realized at a certain duty ratio. Once the duty ratio changes, the switch will lose the ZVS characteristic, thus the system losses will greatly increase. And if PFM is utilized in the VHF topology, the frequency range of the system will be too wide, the elements and control system will be difficult to design and operate. Of course, PWM and PFM can be combined to control the system collectively, but this will increase the complexity of the control circuit and still cause the system to withstand a wide frequency range.

In VHF converters, on-off control method is widely used, Fig. 19 shows the control block diagram [56], [60], [72]-[75]. The driving signal is obtained after the low frequency control signal and high frequency oscillator signal passing the AND gate. The final driving signal is shown in Fig. 20. With this method, the output voltage can be regulated. The advantage of this control method is that the switch keeps working at its optimal operating point once it turns on. Thus with a constant output voltage, this control method can also ensure high efficiency in a wide input range. However the drawback of this approach is that it causes low-frequency harmonic interference, so it is necessary to increase the values of the filter elements. Besides, as the switch state constantly converting between working and non-working, this method puts forward higher requirements for the transition speed of the power circuit. On the basis of on-off control method, the improved hysteresis control method and the phase-shift control method also have been used in VHF converters.

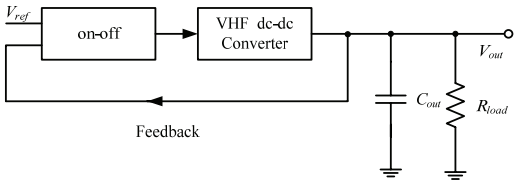

Fig. 19. The diagram of VHF DC-DC converter controlled by on-off method.

In [76], the outphasing control technology is applied to VHF power converters, Fig. 21 is the schematic diagram of this control method. This method is to adjust the phase difference between the two or more inverters to control the output voltage amplitude of the rectifier. Fig. 22 is a VHF power converter based on outphasing control, it has fast response speed, wide adjustment range and small input output filters. However the system losses are roughly the same

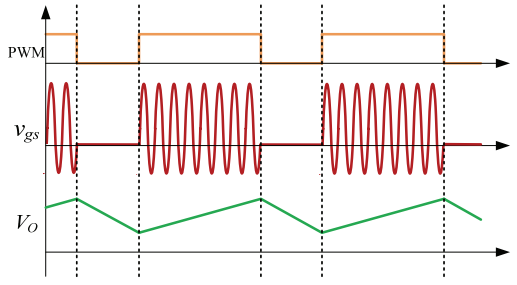

Fig. 20. The waveforms of control signal and gate voltage.

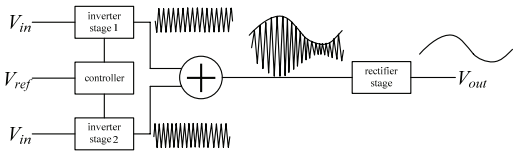

Fig. 21. System diagram of VHF converters based on outphasing modulation.

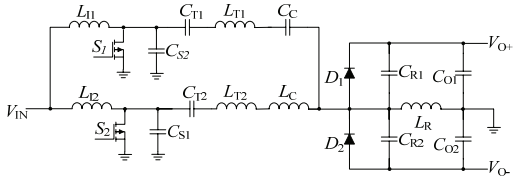

Fig. 22. The circuit of VHF resonant circuit based on outphasing control method.

when the circuit is under light load and full load conditions, which will cause lower efficiency in the light load situation. Another defect is that the control circuit is complex and not easy to design.

V. Opportunities and Challenges of VHF Power Converters

With the continuous improvement of the working frequency, the VHF converters can effectively reduce the value and volume of passive components and increase the power density [77]-[82]. In the future, the integrated VHF converters will become the development trend of the VHF converters. In order to achieve the integrated system, the design and integration method of the magnetic components, such as inductors and transformers, becomes one of the hottest and most difficult subjects. In VHF situations, planar magnetic components can effectively reduce the volume of the inductors and transformers, especially their height in the vertical direction. Generally speaking, air core structure can be adopted to design magnetic components when the frequency is tens of megahertz. The copper tracks in the PCB board can act as the windings of the inductors and transformers. However, the ac resistance, parasitic capacitance, the primary and secondary leakage inductances under high frequency conditions are all needed to be studed thoroughly and designed optimally.

At the same time, with the rapid development of the wide band gap semiconductors, such as GaN, the development of VHF power converters is correspondingly promoted. GaN FETs own lower on-resistance and smaller parasitic capacitance, and can effectively reduce the conduction losses and the driving losses. Although GaN FETs have many advantages when applied in VHF converters, there are many problems that need to be addressed. Compared with Si switch, the threshold voltage of GaN FET is lower, so GaN FET is more sensitive to the driving voltage amplitude, the spikes contained in the driving signal may cause malfunctions or even damage to the GaN FETs. In addition, the reverse conduction voltage of this switch is relatively high, in order to reduce the losses caused by this aspect, the opening time of the switch is required to be calculated and designed precisely.

Nowadays, most of the available VHF converters are only suitable for the applications where the input and output voltage are low. This is mainly constrained by the high voltage stress of the switches and diodes in the inverter stage and rectifier stage. Even if the Class Φ_2 topology is used, the stress is twice of the input voltage. Thus, investigating new inverter and rectifier topologies with low voltage stress can widen the input and output voltage range of the VHF converters. For the application of high power conditions, the design of optimal system structure is another urgent problem to study and settle.

The non-ideal parasitic parameters created by the pins of the components and the layout of the PCB board will also greatly affect the performance of the VHF power converters. In the further study, the characteristics of parasitic parameters and the suppression methods need to be studied deeply under the VHF conditions. And the optimal layout of elements in VHF converters should be proposed with the help of 3D simulation software. Meanwhile, the sensitivity of the system to parasitic parameters can be restrained by exploring the new topologies. Also the compensation method of non-ideal parasitic parameters should be deeply researched.

VI. Conclusion

High frequency and high power density have become the developing trend of power electronics technology, the VHF converter can effectively reduce the system volume, improve the system power density and other performance. However, it also brings many challenging problems. In this paper, from the perspective of the topology, the inverter stage, rectifier stage and matching network are introduced respectively, and their merits and demerits are analyzed in detail. Then in the respect of driving technology, the resonant and self-resonant driving mode have taken place of the traditional hard drive mode, which can take advantage of the energy stored in parasitic capacitance. Besides, the control methods of VHF converters are described and compared in this paper. In the end, the development trends and challenges of VHF converters are introduced, and the promotion in components and topologies is expected.

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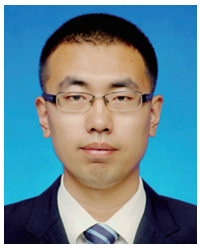

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Data Center Challenges and Their Power Electronics

Philip T. Krein

***Abstract*—Data centers use more than 1.5% of all electricity in China and the U.S., with continuing growth. This paper reviews the power hierarchy levels within modern data centers. It considers energy consumption and power electronics challenges across all levels of a data center, including building distribution, dc architectures, and conversion down to the board level. Power electronics plays a central role throughout the hierarchy, and emerging approaches are described. Strategies that enhance center energy efficiency, both in terms of overall center operation and in terms of computation performance, are discussed.**

***Index Terms*—Data centers, dc distribution, dc-dc converters, server racks, power utilization factor, dc power architecture, digital power.**

I. Introduction

MODERN data centers are superficially similar to mainframe computer rooms from the 1960s, but have grown in scale and in number. They represent a fast-growing load component within the electric power grid. In [1], it is reported that in 2015, more than 400,000 data centers in China alone were consuming about 1.5% of national electricity supply. In the U.S., consumption in 2014 reached 70 TWh, about 1.8% of total supply [2]. Life-cycle costs of data centers today are often dominated by energy expense [3].

Although there is vast literature about overall data center performance, and large-scale industry efforts to enhance high-level efficiency [3], [4], the attributes associated with power architecture and power electronics across the layers in a data center are less widely discussed. This paper draws on [5], with updates across the hierarchy. Opportunities for improvements across the layers are summarized, and work in these areas is reviewed. The impact of power electronics is emphasized.

Based on the recommendation to "follow the power" [6], it is important to track energy flow in a data center from the external utility substation through building distribution to the individual racks, and then on to the server blades, memory and computing boards, and finally to the low-level information technology (IT) loads. Each level in this hierarchy brings its own challenges and opportunities for energy savings.

Manuscript received March 27, 2017. The work was supported in part by the Grainger Center for Electric Machinery and Electromechanics at the University of Illinois.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00005

II. The Hierarchy Levels in a Data Center

Data center power can be treated according to levels of function:

- Utility level. Independent feeds, cogeneration, and external renewables are a few examples of challenges outside a data center itself.
- Building level. This is the level at which the primary utility feed enters the facility. Challenges include the choices between low voltage (e.g. 480 V or 600 V) input and medium voltage input, and whether the main building feed should be converted immediately to dc.
- Backup level. Many architectures have uninterruptible power supplies (UPS) and fuel-driven generators to provide power at the building level. Some distribute backup at lower levels.
- Rack level. Groups of racks are likely to use broader thermal management, but power delivery to individual racks is typical.
- Board level. Within a blade, power may be managed for memory boards, computing motherboards, and other local IT equipment.
- Chip level. Within a board, individual point-of-load (PoL) dc-dc converters provide low-voltage power for chips or chipsets. It is typical to see three to five different voltage values at this level of power management.
- Internal level. Some ICs, especially multi-core processors have on board energy management.

Each level involves particular power requirements and opportunities. Although an optimized system might couple attributes at several levels to achieve the best results, this paper will emphasize the individual levels and the challenges that each one entails.

A. Utility Level

At the utility level, many of the design aspects are linked to reliability. Reliability is linked to tiers [7], and at the highest Tier IV level, multiple independent utility feeds are typical. A data center might also be part of a microgrid. Some of the system architecture opportunities for power electronics include active switch management of multiple feeds [8] and integration into microgrids [9].

From a thermal perspective, the "energy" in the form of information leaving a data center is insignificant, and IT equipment ultimately converts 100% of incoming energy

into heat. This implies opportunities for combined heat and power (CHP or co-gen) utility-level architectures [10]. However, CHP has only been explored in a limited way for data centers. One issue is that the waste heat from IT devices is at relatively low temperature (rarely above 50°C) and therefore is not useful for steam generation. It can be used in district heat systems [11]. Following some early work [12], the trend has been to emphasize co-gen based on other devices such as microturbines [13]. A more practical situation locates a data center near a power plant that can also supply steam for absorption chillers.

As data center energy use continues to grow, numbers of data centers climb, and reliability demands increase, utilities are likely to have a larger role in siting and planning [14]. This has been typical in the past for large manufacturers, and data centers are approaching similar load levels.

B. Building Level

At the building level, there have been extensive studies that address the *power usage effectiveness* (PUE), defined as the ratio of total energy into a facility to total energy consumed by IT equipment within the facility. PUE must be greater than one under any circumstances and can readily exceed two given conventional heating, ventilation, and air-conditioning (HVAC) systems operating in hot environments. Realistically, PUE will exceed one substantially even if HVAC requirements are minimal, since a useful data center has lighting, security systems, and other non-IT functional loads.

An extreme low in PUE can be achieved with liquid immersion cooling in unstaffed data centers. In [15], a PUE value of 1.02 is reported for an insulating boiling immersion cooling approach. However, such a low number strongly suggests incomplete computation. For example, the power into a data center is delivered to power electronics, and only indirectly to IT equipment. The loss in power conversion is not really energy delivered to IT loads. Given an overall power conversion efficiency as high as 95% (unlikely), a PUE below 1.05 is not physically valid unless power supplies are considered to be IT load. This also ignores any energy consumed within uninterruptible supplies and even building switchgear and wiring.

Google reports a much more realistic company-wide PUE of 1.12 [16], and also reports there that

> "When measuring our IT equipment power, we include only the servers, storage, and networking equipment. We consider everything else overhead power. … Similarly, we measure total utility power at the utility side of the substation, and therefore include substation transformer losses in our PUE."

The distinction between IT and non-IT equipment is important when PUE values are used to incentivize system improvements.

Liquid immersion in data centers can take at least two forms. As in [15], the individual boards or blades can be immersed in coolant. Advanced hydrofluorocarbon liquids and mineral oils have been used for this [17] (claiming PUE values in the range of 1.02 to 1.03). The alternative is to immerse a complete rack or data center itself, possibly with conventional air-based heat transfer into the surrounding liquid. An undersea approach based on this has been announced by Microsoft [18].

Building-level emphasis on PUE has encouraged advanced HVAC work. Just a few examples include [19], in which enthalpy wheels are evaluated for data center benefits, and [20], in which rack-based cooling is proposed. In [21], a comprehensive overview of power architectures and interconnections to renewables is presented. The work also discusses power electronics architectures and cooling alternatives. Much of the discussion addresses UPS efficiency and operation.

In the context of power electronics, the discussion and use of direct dc distribution within data centers is a key trend. By the time of the workshop [6] held in February 2007, there were already some demonstration projects and active industry engagement. In [22], architectures are compared in depth across conventional ac distribution with conversion at the rack level, building-level 48 V dc distribution, building-level 400 V dc distribution, and others. The work identifies 400 V building-level dc distribution as advantageous. Several studies, including [23], [24] have reported that dc distribution at the building level enhances efficiency and also raises reliability and availability. It is important to recognize, however, that efficiency improvements are on the order of one percentage point or so with best-practice present designs.

Results from related areas, including mainframe computer systems, supercomputers, and mobile power systems have bearing on questions of dc distribution. A broad discussion of the issues and the power conversion requirements can be found in [25]. This work suggests that dc distribution was reported to have advantages even as early as the ENIAC mainframe system. In [26], architectures and power electronics designed for electric ship applications are suggested as a basis for dc applications in data centers. In [27], a supercomputer powered directly from a 380 V dc solar energy bus is described.

One important advantage of building-level dc distribution is that megawatt-scale rectifiers can be designed with much higher efficiency that rack-level kilowatt-scale devices [28]. Building-level conversion also simplifies reliability design. Redundancy at the building level is relatively straightforward, and it is generally accepted that single points of failure need to be avoided.

The trend toward dc distribution in data centers is part of a larger discussion of dc distribution within low-energy buildings [29]. Early efforts related to data centers and more broadly to buildings were conducted by Lawrence Berkeley National Lab. These activities have culminated in an international industry group, the Emerge Alliance [30]. The energy savings are one aspect, even if the amounts are not large [31]. At present, dc distribution in a data center is not confined to research. Commercial systems are in place [32].

It is important to notice that PUE in particular, and also dc distribution practices, do not by themselves drive power in-

novation in data centers. Even though PUE is a limited metric, it does give linkage to some efficiency improvements, particularly those associated with HVAC. Starting from relatively high PUE numbers (above 1.5), several strategies for energy savings have been suggested by Pouchet [33]:

- Optimize air flow throughout the building.
- Optimize air flow within each rack.
- Extra attention to building outer envelope and room sealing.
- Economizers in the heating, ventilation, and air-conditioning (HVAC) system.

A combination of cooling from ambient air and inexpensive energy has driven many data center locations [34].

C. Backup Level

In conventional practice, a UPS is provided at the building level, and represents an important element in overall efficiency. The basic electrical distribution scheme in a typical ac data center is shown in Fig. 1. Notice in particular the stack-up of power electronics. Just behind the building feeder, an online UPS (also termed a "double conversion" UPS) provides back-to-back conversion, with an input-side rectifier, regulated battery bus, and output-side inverter. This provides high-quality power conditioning and backup. At the rack level, ac may be connected to individual server blades, or an active rectifier supports a dc bus for the complete rack, usually at 48 V. At the board level, a relatively low voltage is used to send power across board traces. The final point-of-load (POL) converters supply the digital chip sets. Other POL converters produce supplies for communication links, disk drives, diagnostic devices, sensors, and other IT infrastructure. Building-level HVAC and lighting are not shown.

The advantage of an online UPS in this context is high power quality and excellent immunity to short-term changes on the grid side. Not shown is a transfer switch that can connect in local fuel-driven generation if the utility feed or feeds are lost. The disadvantages are that the UPS must have inherently high reliability, and that the multiple conversion stages involve power loss.

Offline or "standby" UPS circuits are also in wide use in data centers. Various hybrid configurations are employed to speed the process of transferring the energy source from the grid to a battery set [35]. Recent innovations include smaller intermediate converters that support the load during the transfer interval [36]. This can also be supported with passive filters combined with small converters [37]. Grid-interactive standby architectures allow fast source transfer without having the UPS in the continuous energy conversion path [38].

Notice that in the online UPS case, power is converted at least four times from the ac mains to the IC level. Given estimates such as a 97% efficient UPS process, a 95% efficient rack-level rectifier, and POL converters at typically 93% or less, overall about 85% of energy, at best, reaches the final IT loads. This would limit the PUE to more than 1.17 even without considering HVAC – provided IT power does not include power supply input.

A direct dc architecture, in which the "dc UPS" could be as simple as a master regulated dc bus, is shown in Fig. 2. In this case, the building rectifier efficiency exceeds 98%, the rack level might reach 97%, and the POL efficiency is still 93%. The total is about 88%, and the PUE will be more than 1.13.

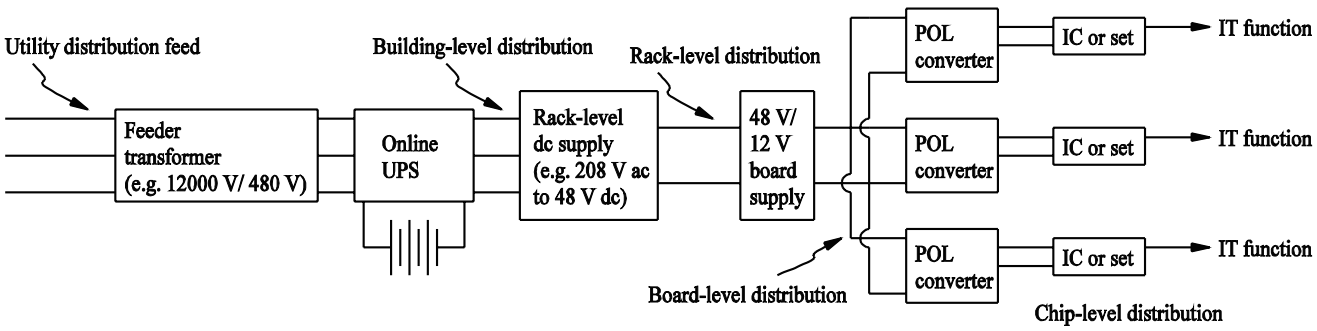

Fig. 1. Typical conversion sequence in an ac data center architecture [5].

Given these limitations on power loss and performance, how, for example, does Google achieve system-wide PUE of 1.12 [16]? Part of the answer is a *distributed UPS* architecture [38]-[40]. In the initial 2009 announcement [38], Google reported the use of small 12 V batteries directly within each individual server. The result has higher backup performance than a building-level online UPS, since it is distributed among all computing loads, but avoids power conversion layers built into conventional UPS architectures. Strictly speaking, the overall system efficiency is the same as in Fig. 2 because there is still conversion at the building level, rack level, and POL level, but the system is simpler and adapts better over a wide load range. The effective PUE improves by a few points. Many other users have adopted the distributed approach.

D. Rack Level

Servers in a data center are organized into conventional rack mounts, or in high-density blade configurations. A 42-unit (42U) rack is typical. In an ac data center, each rack might be provisioned with three or four three-phase circuit sets, provid-

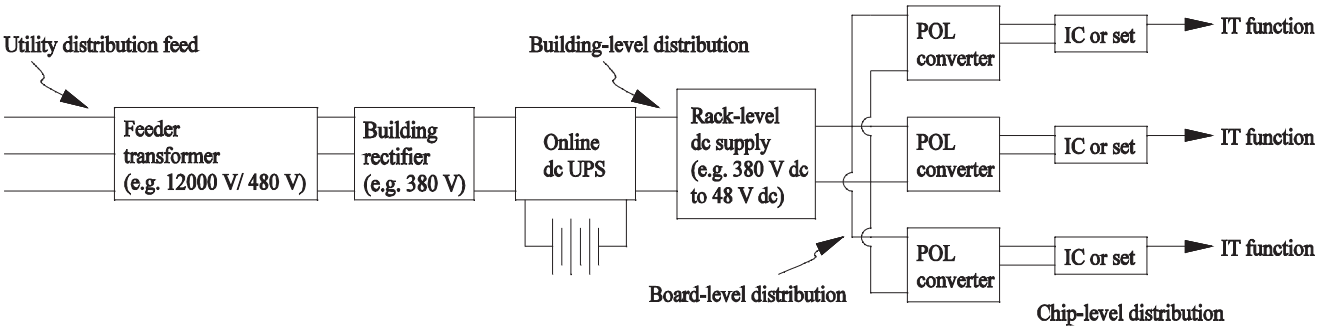

Fig. 2. Typical conversion sequence in a dc data center architecture.

ing up to 25 kW per rack. In a dc data center, nominal dc voltage such as 380 V is delivered directly to each rack, providing up to about 30 kW. In each case, power is often delivered directly to server-level power supplies.

An important challenge in rack provisioning is to manage various rating stackups. Standards and codes limit the loading level of any circuit. Servers are likely to have dual redundant supplies. The supplies themselves are oversized, and servers do not always operate close to 100% power. The combination generates considerable confusion when rack-level power provisioning is designed [42]. Worst-case design leads to extreme over-provisioning [43].

Rack distribution offers several opportunities for advanced power electronics. For example, supplies within a rack should be sequenced to avoid combined inrush peaks or other short-term system stresses. Faults should be managed to avoid propagation. Protection at the rack level is especially challenging with dc distribution [44]. Supplies must be efficient over a wide load range, given the limited full power operation of servers. Several approaches have been proposed to broaden the range of high efficiency [45]-[47], but rack-level power considerations are not quite the same as board-level issues discussed below.

The ongoing discussion about 48 V power for data centers [48] mainly considers board-level innovations. However, 48 V rack distribution is discussed [22], and direct board 48 V power would eliminate one power conversion level in the chain.

A more radical rack-level approach is to connect individual servers in *series* [49]-[51]. Because communications links are electrically isolated, alternative electrical connections can be supported. A series stack of server boards or blades eliminates a layer of conversion and substantially increases system efficiency [52], [53]. An oversimplified version of the approach would connect 32 servers in series, and connect them directly from a 380 V bus. This requires diligent load balancing, but avoids a conversion step and enhances system efficiency. In [54], it is shown that the approach can raise this part of the power conversion process from a state-of-the-art 96% efficiency to more than 99.8% efficiency. Some of the ideas appeared earlier [55], but the architectures have much in common with older battery balancing techniques [56]-[58].

Better integration of power and thermal management at the rack level has been discussed as a power saving tool [59], [60]. In [59], local rack cooling is linked to computing loads. The intention is to make total system power track the computational load. In [60], methods for server power interconnection within a rack, to reduce redundancy but maintain power reliability, are presented. The gains in energy performance from interconnection do not approach those of a complete series connection, but linkages between system power and computing power are important. This is linked to the concept of *energy proportional computing*, as described by Google [61].

E. Board Level

Individual server boards often employ one or two power supplies, known in the data center industry as *power supply units* (PSUs), within the server enclosure. Two are used when direct "1+1" redundancy is required. As in [38], many modern designs use battery backup directly at this level. As in [48], there is continuing discussion of 48 V supplies at the board level. Recent results [62] deliver 48 V directly to end-use POL converters.

At the board level, power supplies previously had various designations such as "silver," "gold," or "platinum," and there have been various industry initiatives for improvement [63], [64]. Wide ranges for high efficiency are more important than full-load efficiency [45], especially in redundant supply architectures in which the maximum output is 50% unless a failure occurs. In fact, dual redundancy benefits from high efficiency in the load range below 50% rather than higher.

Most innovations at this level have come from incremental improvements in power supplies. This is particularly true because most architectures employ a supply that delivers 12 V, 5 V, 3.3 V, and other voltages similar to those in a desktop computer. It draws power either from a single-phase ac input or a direct 380 V dc bus. Some of the work applies to rack-level power or to multiple boards (as in a blade enclosure) [65].

F. Chip Level

At the "chip level," the power province of POL convert-

ers, high efficiency is challenging. This is because voltages are low, currents are high, and additional requirements such as fast transient response trade off against low losses. Typical solutions use two-stage dc-dc converters with an initial 12 V to 5 V stage followed by a multi-phase 5 V to 1 V stage [66]. Other configurations can take advantage of high voltage conversion ratios [67]. Some broader concepts are addressed in [68], [69], in which the hierarchy issues are considered.

Some of the earliest work on POL converters considered 48 V input [70]-[72], even though implementation is much more recent [62]. In [70], the concept of multi-phase dc-dc converters is introduced. In [72], this is extended to a four-phase two-stage converter for 2 V output. Comprehensive work on design based on 48 V POL applications was presented in [73], [74]. The two-stage concept is presented in depth in [75]. Recent designs, such as [76], are mature and ready for applications.

In POL circuits and at the chip level, droop control methods can be employed for enhanced power management. Voltage droop (termed *adaptive voltage positioning*) seeks to keep POL output impedance resistive, such that increasing load drops the supply voltage linearly. This is a helpful innovation since finite output impedance is unavoidable, and resistive characteristics have advantages given dynamic disturbances. In digital loads, the effective load is resistive, since energy proportional to an internal capacitance C_{int} is lost during each digital clock cycle. This means the load power is

$$P_{load}=f_{clock}\,C_{int}\,V^2, \tag{1}$$

the same as replacing the digital load with an effective resistance R_{eff}. Voltage droop helps the stabilize operation against disturbances.

Adaptive voltage positioning or scaling can also refer to an adaptive process by which the supply voltage at the chip level is decreased as much as computational performance allows [77]. In an idealized version, a computational load runs a test protocol, and requests step-by-step reduction in supply voltage until excessive error rates are encountered. The chip itself might store a map of voltage vs. load to deliver error-free performance at the lowest possible power.

Frequency droop for digital loads is not a power supply strategy, but clock frequency adjustment or droop, as in (1), can manage load requirements in a dynamic manner. This is part of the industry concept of *dynamic voltage and frequency scaling* (DVFS) to rapidly adjust the power requirements of digital loads at the chip level [78]. The term DVFS appears in more than 1000 papers on IEEExplore. Summaries can be found in [79], [80].

G. Internal Level

At the internal level, within a chip, a recent trend is to bring dc-dc conversion into the chip itself. The general power-system-on-chip approach has been explored for a long time [81], [82], but commercial implementation is recent. The Intel "Haswell" processor concept was one of the first large-scale digital loads to incorporate internal power management [83], [84]. As digital supply voltages drop below 1 V, on-chip management becomes increasingly important.

Modern digital chips are likely to comprise many computation cores or internal modules. If these can be connected in other ways, such as in series [49], [55], large voltage savings become possible. For instance, a chip with 61 cores, connected in series, can operate directly from a 48 V bus at a nominal 0.79 V per core, eliminating all layers of point of load conversion. Such a connection does not eliminate benefits of DVFS, even though it involves more comprehensive system-level approaches to power conversion and management [85]. The series concept applies across many levels, with the highest benefits for core interconnections [86]. However, since electrical isolation is rare below the board level, series connected racks are likely to have more impact in the short-term than series connected cores.

The internal level is well-suited to certain types of software-based data center energy management. Individual cores can be switches on and off, or computing loads can be actively balanced among cores to best spread thermal stresses. A potential innovation is cores that report or even predict their power requirements back to on-chip power converters. The converters can anticipate requirements and make dynamic adjustments to deliver the best possible performance.

III. System-Level Management

Even though power distribution and conversion in a data center are inherently hierarchical processes, in the end the power is consumed by IT loads and combined management of hardware and software provides the greatest possible benefits. The PUE metric is less useful at this level. There are two aspects to consider:

1) Is a data center dynamically managed to keep its energy requirements as low as possible?
2) What about reduction of energy used per unit of computation?

For the first item, energy proportionality is important, but the complete system architecture also matters. For the second, the linkage between power electronics and digital design is important.

Strategies for keeping energy requirements as low as possible at the system level tend to be unique to an implementation. For example, for the highest-performing thermal designs, low energy consumption means good balance. A center operating at 10% of maximum design load in this case functions best if all internal elements also function at 10%. For power electronics, this is not typical, since there are overhead requirements that begin to affect efficiency as power decreases. For point-based thermal designs, typical practice is to run racks as close to 100% power as possible, setting other equipment to an idle state. This works well in systems designed for high full-load efficiency, but the high loading can diminish reliability and leads to hot spots and other potential failure mechanisms.

For reduced energy per computational unit, voltage reduction reduces this value in a nonlinear manner, but there are limits. Computation cores operating at near-threshold or sub-threshold conditions use much less power than cores running at conventional supply levels. However, power conversion down to 0.3 V to 0.5 V levels associated with this reduction are extremely hard to produce; series connections become important, even though they bring more complicated management issues. The clock rates also must be reduced, trading off performance in a multi-dimensional space. As pointed out in [87], the linkages between digital-side "low-power design" and system-level considerations in data centers are complicated.

In the large-scale computing literature, there is a growing body of work on system-level data center energy management. In [88], an early summary of management approaches is presented. In [89], [90], high-level simulation is used in an energy management process.

A critical observation is that energy saved at the point of end use, especially via reduction in energy required per unit of computation, provides extra dividends throughout a data center. Even if PUE is defined all the way at the point of final chip connection, with a value as low as 1.12, reduced consumption at the end offers extra benefits. In more conventional scenarios, in which PUE does not include power supply losses and impacts, reduced computation energy has much larger impact at the input. Dynamic optimization has a key role to play in long-term data center operation [91].

IV. Conclusion

Data centers are large energy consumers, analogous to heavy manufacturing industries. Both are key economic drivers, and energy costs are crucial in both arenas. Energy reduction in data centers requires attention to power distribution and conversion across all hierarchy levels. A challenging requirement is to combine hardware and software in operation to achieve system-level optimization. Power electronics plays a vital role in enabling intelligent system-level power management.

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99% Efficient Three-Phase Buck-Type SiC MOSFET PFC Rectifier Minimizing Life Cycle Cost in DC Data Centers

Lukas Schrittwieser, Johann W. Kolar, and Thiago Batista Soeiro

***Abstract*—Due to the increasing power consumption of data centers, efficient dc power distribution systems have become an important topic in research and industry over the last years and according standards have been adopted. Furthermore the power consumed by telecommunication equipment and data centers is an economic factor for the equipment operator, which implies that all parts of the distribution system should be designed to minimize the life cycle cost, i.e. the sum of first cost and the cost of the power conversion losses. This paper demonstrates how semiconductor technology, chip area, magnetic component volumes and switching frequency can be selected based on life cycle cost, using analytical and numerical optimizations. A three-phase buck-type PFC rectifier with integrated active filter for 380V dc distribution systems is used as an example system, which shows that a peak efficiency of 99% is technically and economically feasible with state-of-the-art SiC MOSFETs and nanocrystalline or ferrite cores. Measurements taken on an 8 kW, 4 kWdm^{-3} hardware prototype demonstrate the validity and feasibility of the design.**

***Index Terms*—Active third-harmonic current injection, buck-type power factor correction (PFC) converter, three-phase rectifier systems, integrated active filter rectifier.**

I. Introduction

INFORMATION and communication technology equipment has become a significant consumer of electric power in recent years. In 2007, for example, the related annual consumption in Germany alone was 55TWh which equaled approximately 10% of the countries total consumption. The annual power consumption of data centers located in Germany is approximately constant at ≈10TWh since 2008 [1]. For the US an annual data center power consumption of 60TWh was estimated in 2006 with a energy cost of $4.5 billion [2], for 2014 an increase to 70TWh has been reported [3]. Therefore the cost of electric energy is a significant economic factor for data center operators and should hence be considered in investment decisions.

In conventional data centers using ac distribution systems, as shown in Fig. 1(a), up to 50% of the total energy consumed is used for air conditioning, distribution and conversion losses [4]. Compared to this, distribution systems based on a dc bus with a nominal voltage of 380V offer significantly higher efficiency, improved reliability and reduced capital cost and floor space, cf. Fig. 1(b) [5]. Furthermore they allow a direct connection of lead acid batteries, consisting of 168 cells connected in series, with a typical floating cell voltage of ≈ 2.26 V, which results in a nominal bus voltage of 380 V. Accordingly, standards and components for dc distribution systems have been developed in recent years [6], [7].

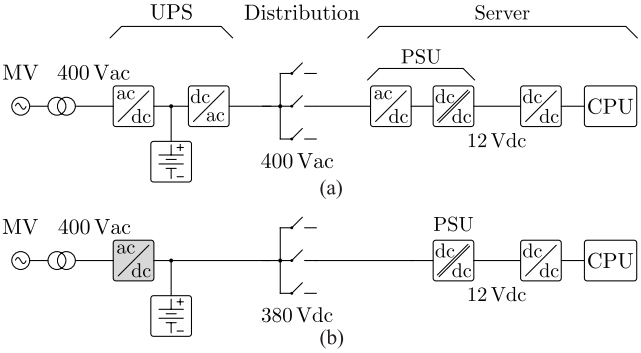

Fig. 1. Data center power distribution concepts: (a) Conventional 400 Vac distribution, using an ac output Uninterruptible Power Supply (UPS). Similar concepts can be used with 480 Vac. (b) Facility level dc distribution system based on a 380 Vdc bus which allows a direct connection of backup batteries [4].

Normally a boost-type power factor correction (PFC) stage is used to convert the 400 Vac mains into a dc voltage which is higher than the full-wave rectified ac input voltage, typically in the range of 700V to 800 V. A subsequent buck converter is then required to connect the PFC output to the dc distribution bus. (This configuration is also used for fast chargers of Electric Vehicle batteries which are powered from the three-phase ac mains [8].) As an alternative, a single-stage conversion between the three-phase mains and a dc bus with lower voltage can be achieved with buck-type PFC converters, like the SWISS Rectifier, the six-switch buck rectifier or the Integrated Active Filter rectifier [9]-[12].

The circuit topology of the Integrated Active Filter (IAF) buck-type PFC rectifier, shown in Fig. 2, was first introduced in [13] for three-phase solar inverters. A similar circuit was also proposed for drive systems with small dc-link capacitors [14]. Three major blocks can be identified in the IAF rectifier's schematic: an Input Voltage Selector (IVS) built of

Manuscript received March 27, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00006

a linecommutated full-wave diode rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ $\bar{k} \in \{\bar{a}, \bar{b}, \bar{c}\}$2 and three four-quadrant switches $S_{\bar{k}y\bar{k}}$, a current injection circuit S_{xy}, S_{yz}, L_{inj} and a dc-dc buck converter S_x, D_z, L_o which provides the constant dc output voltage u_{pn}. Typically a small capacitor C_f' is required to ensure a valid conduction path during the commutation of S_{xy}, S_{yz} and S_x. Note that the IVS switches and diodes are commutated at mains frequency only which implies that almost no switching losses occur in the IVS, therefore rectifier diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ which are optimized for a low forward voltage drop can be used.

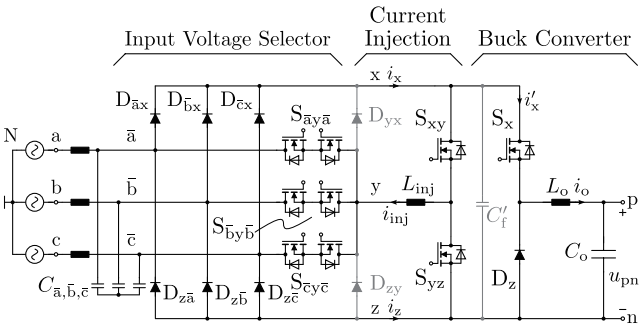


Fig. 2. Schematic of the Integrated Active Filter rectifier (IAF), using an Input Voltage Selector (IVS) commutated at mains frequency, combined with a buck converter providing the output current i_o and a current injection converter which serves as active harmonic filter for achieving sinusoidal ac input currents.

For this paper the IAF buck-type PFC rectifier was selected to demonstrate a cost-driven converter design approach, as only two line-commutated diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$, and one power transistor S_x are in its main conduction path [9], [15]. Based on a short review of the IAF rectifier's main properties in Section II and using the capital equivalent worth of energy together with component cost models, a non-isolated 8kW PFC rectifier is designed in Section III. This allows selecting cost optimal components such as semiconductors and inductors achieving an economically optimal converter which minimizes life cycle cost, i.e. the sum of first cost of the converter hardware and the cost of conversion losses during the service life. Measurements taken on a hardware prototype are presented in Section IV.

II. Integrated Active Filter PFC Rectifier

Simulation results for a 8kW IAF buck-type PFC rectifier (cf. Fig. 2) are shown in Fig. 3, for the system specifications given in Table I. For the IAF rectifier the current injection circuit and the buck converter can be analyzed, optimized and operated almost independently of each other. As the dc output is provided by the buck converter (S_x, D_z, L_o), the output current i_o and voltage u_{pn} can be controlled independently of the injection circuit. This can be seen from the simulation results in Fig. 3: During $\omega t < 180°$ the current injection circuit is turned off, i.e. $i_{inj} = 0$. As the buck converter creates a constant output current i_o it consumes constant power from the ac input. Hence non-sinusoidal ac input currents $i_{a,\,b,\,c}$ result and only two ac input phases $i_{a,\,b,\,c}$ conduct current at a time.

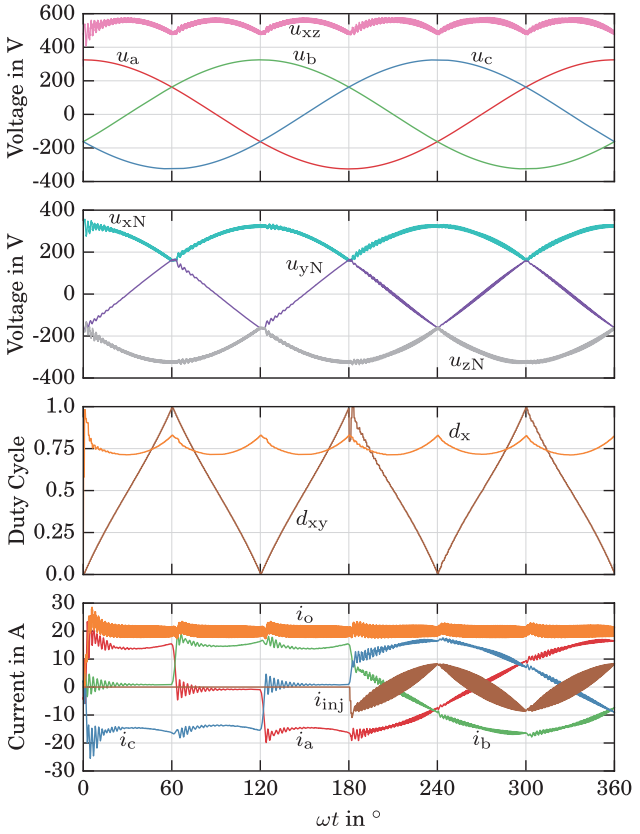


Fig. 3. Simulation results for an IAF buck-type PFC rectifier as shown in Fig. 2, plotted are the ac input voltages $u_{a,\,b,\,c}$, the IVS output voltages u_{xN}, u_{yN} and u_{zN}, the buck stage duty cycle d_x, the duty cycle d_{xy} of switch S_{xy}, the output current i_o, the injection current i_{inj} and the ac input currents $i_{a,\,b,\,c}$. During $\omega t < 180°$ the injection circuit is disabled (i.e. $i_{inj} = 0$) which results in non-sinusoidal mains currents $i_{a,\,b,\,c}$.

TABLE I
Converter Specifications

Input Voltage (Line-to-Neutral)	$U_1 = 230$ V rms
Input Frequency	$\omega_1 = 2\pi\ 50$ Hz
Switching Frequency	$f_s = 27$ kHz
Nominal Output Voltage	$U_{pn} = 400$ V
Nominal Output Power	$P_o = 8$ kW

For $\omega t > 180°$ the injection circuit is used to create a current i_{inj} which is proportional to the voltage u_{yN},

$$i_{inj}(\omega t) = -\hat{I}_1 \frac{u_{yN}(\omega t)}{\hat{U}_1} \quad \hat{I}_1 = \frac{2\,P_o}{3\,\hat{U}_1} \quad , \qquad (1)$$

where $\hat{I}_1$ is the peak value of the rectifier's ac input line current and $\hat{U}_1$ is the ac phase-to-neutral voltage amplitude. This results in sinusoidal ac input currents as shown in Fig. 3. A more detailed description of the modulation and control strategy can be found in [9], a brief description of the main

components is given in the following.

A. Input Voltage Selector

As described above, the IAF rectifier uses an IVS, which connects each ac input phase a, b, c to either node x, y or z. This implies that the voltages u_{xN}, u_{yN} and u_{zN} are piecewise sinusoidal, which allows to move the ac filter capacitors $C_{\bar{a},\bar{b},\bar{c}}$ from nodes $\bar{a}$, $\bar{b}$, $\bar{c}$ to nodes x, y, z as shown in Fig. 4. This shortens the commutation paths of the buck converter and the injection switches. Additionally the diode bridge currents i_x and i_z become continuous which reduces the conduction losses in the bridge diodes $D_{\bar{k}x}$ and $D_{z\bar{k}}$ and in the fourquadrant switches $S_{\bar{k}y\bar{k}}$. The resulting rms current values can be calculated as

$$I_{\mathrm{D}\bar{\mathrm{k}}\mathrm{x},\mathrm{rms}} = \hat{I}_1 \sqrt{\frac{\sqrt{3}}{8\pi} + \frac{1}{6}} \quad \text{and} \tag{2}$$

$$I_{\mathrm{S}\bar{\mathrm{k}}\mathrm{x},\mathrm{rms}} = \hat{I}_1 \sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}} \quad . \tag{3}$$

Assuming that MOSFETs are used as synchronous rectifiers, as shown in Fig. 4, the conduction losses are reduced by 31% in the rectifier bridge and by 78% in the four-quadrant switches compared to the original circuit shown in Fig. 2 [16].

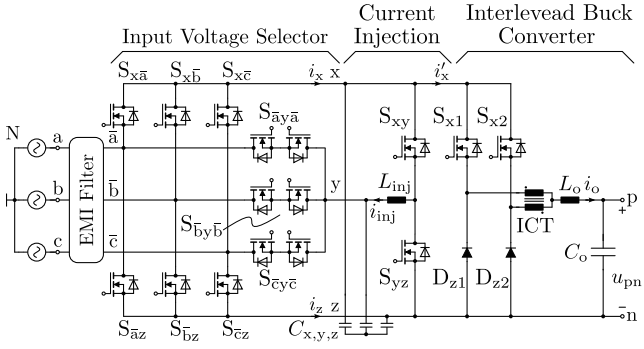


Fig. 4. Schematic of the IAF rectifier where the input filter capacitors have been moved from the ac side ($\bar{a}$, $\bar{b}$, $\bar{c}$) of the IVS to its output side (x, y, z), which reduces the conduction losses [16]. The diodes $D_{\bar{k}x}$, $D_{z\bar{k}}$ are replaced with SiC MOSFETs $S_{x\bar{k}}$, $S_{\bar{k}z}$ operating as synchronous rectifiers to further increase the efficiency. An interleaved buck converter with cells S_{x1}, D_{z1} and S_{x2}, D_{z2} is used where S_{x1} and S_{x2} are controlled with 180° phase shifted PWM signals. This lowers the current ripple in i'_x which leads to a lower voltage ripple at the input filter capacitors $C_{x,y,z}$. The buck converter output inductors are implemented as an inter-cell transformer (ICT) with closely coupled windings and a single output inductor L_o.

B. Buck Converter

It can be seen in Fig. 4 that the buck converter's input is connected to u_{xz} which is a six-pulse shaped voltage provided by the IVS' rectifier bridge, cf. Fig. 3. Neglecting any voltage drops across the semiconductors and inductors, the dc output voltage u_{pn} can be expressed as

$$u_{\mathrm{pn}} = \frac{3}{2}\hat{U}_1\, m \quad m \in [0,1] \quad , \tag{4}$$

where $\hat{U}_1$ is the ac phase-to-neutral voltage amplitude and m is the converter's modulation index. Note that a small distortion of the output current and the mains input currents occurs at every 60° sector of the ac input voltage, i.e. at the intersection of two phase voltages $u_{a,b,c}$. This is most likely due to the switching frequency ripple of the filter capacitor voltages u_{xN}, u_{yN}, u_{zN} as similar disturbances exist in the SWISS rectifier [16]. This voltage ripple is the result of the buck converter's discontinuous input current i'_x and could be reduced with larger $C_{x,y,z}$. However, as the capacitor voltages u_{xN}, u_{yN}, u_{zN} are piecewise sinusoidal they generate reactive power which is typically limited to 5% to 10% of the converter's active power rating.

C. Interleaved Buck Converter

In order to reduce the buck converter's input current ripple and hence the mains input current distortions and the electromagnetic noise emission of the rectifier, an interleaved buck converter can be used, as shown in Fig. 4. By modulating the switches S_{x1} and S_{x2} with 180° phase shifted PWM signals the peak-to-peak ripple in i'_x is reduced by approximately a factor of two and the ripple frequency is doubled due to cancellation of harmonics.

The dc output filter of the interleaved buck converter can be implemented by a combination of an inter-cell transformer (ICT) with closely coupled windings and a single inductor instead of two separate inductors. Using ICTs for interleaved dc-dc converters has been extensively described in literature and has been shown to result in a reduction of the magnetic component's volume, losses and weight [17]-[19].

In Fig. 5 the basic operating principle is shown for a duty cycle of $d_x = 0.75$ and 180° phase shifted PWM signals. The two cells S_{x1}/D_{z1} and S_{x2}/D_{z2} produce the output voltages u1 and u2 shown in Fig. 5(e). These can be transformed into the corresponding common-mode (cm) and differential-mode (dm) voltages u_{cm} and u_{dm}, cf. Figs. 5(f)-(g)

$$u_{\mathrm{cm}} = \frac{u_1 + u_2}{2} \quad , \tag{5}$$

$$u_{\mathrm{dm}} = \frac{u_1 - u_2}{2} \quad . \tag{6}$$

By replacing the ICT with the equivalent circuit shown in Fig. 5(b) the circuit diagram Fig. 5(c) results, which can be decomposed into two uncoupled circuits as shown in Fig. 5(d). It can be seen that the cm voltage u_{cm}, which is applied to the dc output inductor L_o and the ICT's leakage inductance L_σ, switches twice per switching frequency period and has a voltage step height of half the input voltage u_{xz}.

Note that unbalances in the system, such as unequal on-state resistances of the switches, duty cycle differences and mismatched PCB track resistances can lead to unbalanced ICT currents $i_{o1} \neq i_{o2}$. This results in a dc magnetization cur-

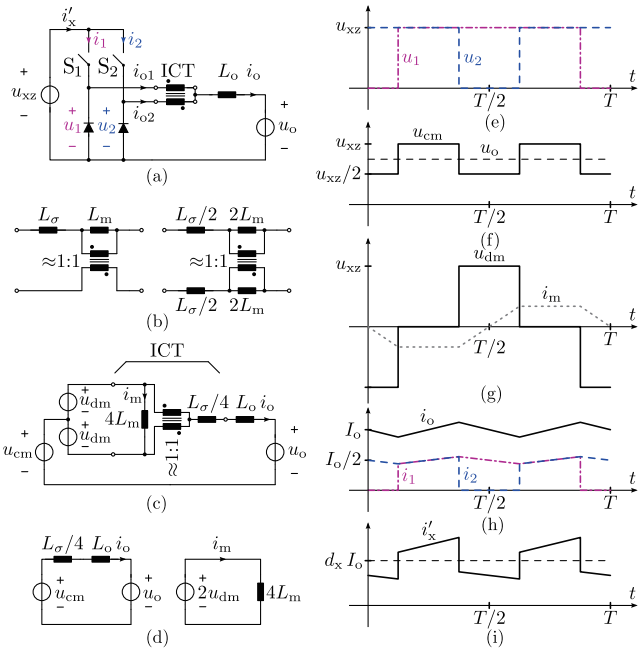


Fig. 5. Operating principle of an interleaved buck converter using a close-coupled inter-cell transformer (ICT). (a) shows the basic circuit diagram, the switches are controlled with 180° phase shifted PWM signals as shown in (e). Replacing the ICT with the equivalent circuit of an non-ideal transformer as shown in (b) and separating voltages u_1 and u_2 into common-mode (cm) and differential-mode (dm) voltages, u_{cm} and u_{dm}, yields the circuit shown in (c). It can be seen that u_{cm} is applied to L_σ and L_o and can be used to control the output current i_o, while udm controls the ICT's magnetizing current i_m as shown in (d).

rent of the ICT,

$$i_m = \frac{i_{o1} - i_{o2}}{2} \quad , \tag{7}$$

that could lead to a saturation of the core material. However, the dm voltage u_{dm} is applied to the ICT's magnetizing inductance L_m and can be used by an active control circuit to ensured an equal current sharing $i_{o1} \approx i_{o2}$ in the ICT windings. Strategies for active current balancing control in ICTs have been described in the literature [20]-[21].

III. Life Cycle Cost Based Converter Design

The design of any power electronic converter is essentially aiming for a best possible overall compromise of multiple trade-offs which result from couplings between different components concerning stresses and utilization. For example increasing the switching frequency reduces the peak-to-peak flux ripple of magnetic components which typically leads to smaller and/or more efficient components, but also increases the switching losses of the semiconductors. This in turn requires a larger heat sink and which could overcompensate the volume reduction achieved in the magnetic components. Similar trade-offs also exist on the component level, e.g. increasing the number of turns in an inductor decreases the core losses at the expense of increased winding losses. Furthermore even for a given fixed switching frequency multiple combinations of volumes or sizes of the different components can lead to similar power densities and efficiencies. Designing an optimal converter becomes even more challenging if more than a single circuit topology and/or several different core and winding materials are taken into account. Due to these tradeoffs a single optimal converter can typically not be found but rather a range of pareto optimal designs can be calculated which achieve e.g. the highest efficiency for a given power density and vice versa.

These trade-offs can be simplified by introducing a singlevalued objective function such as life cycle cost (LCC). As described in [22] the capital equivalent worth of one watt of continuous dissipation can be used to select components in order to minimize the LCC of that component. Combined with cost models, the switching frequency, semiconductors and magnetic components are selected to achieve minimal life cycle cost for a given service life time assuming continuous operation at rated power as will be shown in the following for the IAF rectifier [23].

Given some basic economic parameters, such as interest and inflation rates, the capital-equivalent worth of a continuously dissipated watt of ac power can be estimated. In 2008 the authors of [22] estimated an average value of $14 per watt for the US market and 15 years of service life, which implies that up to $14 could be invested now in order to reduce the equipment's power consumption by one watt over the next 15 years. Although the prices for electric power show a considerable geographical variation (approximately a factor of 5 in the US), the authors conclude that the cost of dissipation significantly overshadows the first cost for telecom power supplies.

A. Semiconductor Technology Comparison

An example calculation for the input voltage selector fullwave rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ / $S_{x\bar{k}}$, $S_{\bar{k}z}$ is shown in Fig. 6, where

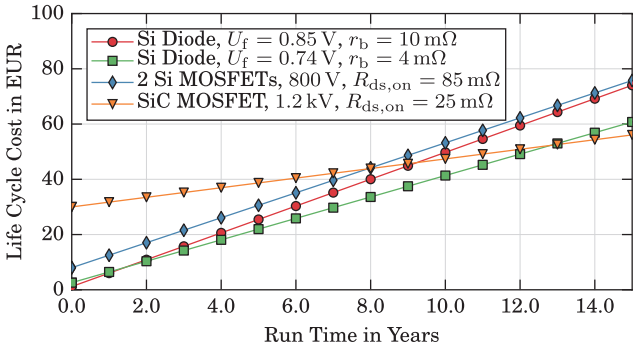


Fig. 6. Comparison of life cycle cost for different implementations of the diode bridge rectifier $D_{\bar{k}x}$, $D_{z\bar{k}}$ of the IVS with $I_{rms} = 8.1$ A, $I_{avg} = 4.6$A (P_o = 8 kW) and a capital equivalent worth of EUR 0.12 per kWh [22]. Switching losses are neglected as the IVS commutates at twice the mains frequency only. It can be seen that the significantly higher first cost of a SiC MOSFET is compensated by the reduced conduction losses of the device achieving roughly the same life cycle cost as Si diodes and Si MOSFETs for run times of approximately ten years, assuming continuous operation at rated power.

a capital equivalent worth of γ = EUR 0.12 per kWh (approximately USD 0.13 at time of publication) is assumed. Neglecting switching losses in the IVS, the device losses can be directly determined from the rms and average currents found by numerical simulation, resulting in I_{rms} = 8.1A and I_{avg} = 4.6A for an 8kW system. Assuming a service life time of 10 years or more, a SiC MOSFET with a high initial cost of approximately EUR 30 and low on state resistance achieves the same or lower life cycle cost than conventional Si diodes with an initial cost of EUR 2.6. The same holds for a parallel connection of two Si MOSFETs with a first cost of approximately EUR 8. Note that all devices are operated far below their thermal limits, e.g. 1.7W of conduction losses result for the SiC MOSFTEs, ≈ 4W for the Si diodes and Si MOSFETs while all devices are rated for more than 100W of continuous power dissipation.

B. Semiconductors without Switching Losses

The calculation shown in Fig. 6 is based on a selection of standard semiconductor devices which might not achieve the lowest possible LCC. Using more than one device in parallel reduces the total on-state resistance $R_{ds,on}$ of MOSFETs or the (differential) bulk resistances r_b of diodes which lowers the conduction losses. This reduces the cost of dissipation during system operation, but increases the first cost as more devices are used, which implies that the resulting LCC is a function of the number n of devices used in parallel. For a MOSFET, continuously conducting the current I_{rms} for the run time t_r, without switching losses the corresponding LCC Λ can be expressed as

$$\Lambda_M(n) = \underbrace{\gamma\, t_r\, \frac{R_{ds,on}}{n}\, I_{rms}^2}_{\text{Cost of Dissipation, } \Gamma_M} + \underbrace{\sigma_M\, n}_{\text{First Cost, } \Sigma_M}\ , \tag{8}$$

where σ_M is the cost of a single MOSFET with an onstate resistance $R_{ds,on}$. A plot of the resulting values for t_r=10 years, $R_{ds,on}$=96mΩ and σ_M = EUR 7.14 is shown in Fig. 7. For a given t_r the optimal number of devices n_{opt}, which achieves minimal life cycle cost, can be derived by minimizing (8) with respect to n as

$$n_{opt} = \sqrt{\gamma\, t_r\, \frac{R_{ds,on}}{\sigma_M}}\, I_{rms}\ , \tag{9}$$

$$\Gamma_{M,opt} = \Sigma_{M,opt} = \sqrt{\gamma\, t_r\, R_{ds,on}\, \sigma_M}\, I_{rms}\ , \tag{10}$$

$$\Lambda_{M,opt} = \Gamma_{M,opt} + \Sigma_{M,opt} = 2\sqrt{\gamma\, t_r\, R_{ds,on}\, \sigma_M}\, I_{rms}\ . \tag{11}$$

Note that a certain minimum n_{min} exists due to the thermal limits of the device and the cooling system as indicated in Fig. 7. However, even for short run times of $t_r \approx 1$ year the optimal n is typically larger than n_{min}.

This optimization can be extended from MOSEFTs to diodes modeled by a constant forward voltage drop U_f connected in series with a (differential) bulk resistance r_b as

$$\Lambda_D(n) = \gamma\, t_r\, \frac{r_b}{n}\, I_{rms}^2 + \gamma\, t_r\, U_f\, I_{avg} + \sigma_M\, n\ . \tag{12}$$

In this case n_{opt} does not depend on Uf , however the losses and hence the cost of dissipation Γ increases. An example calculation for different run times is shown in Fig. 8 where a 96mΩ SiC MOSFET and Si diode with U_f = 0.74A and r_b = 4mΩ are considered as unit elements. For both, MOSFETs and diodes the optimal n increases proportional to $\sqrt{t_r}$, however for Si diodes the resulting losses show little variation due to U_f. As the first cost of the considered diode is ≈ 6

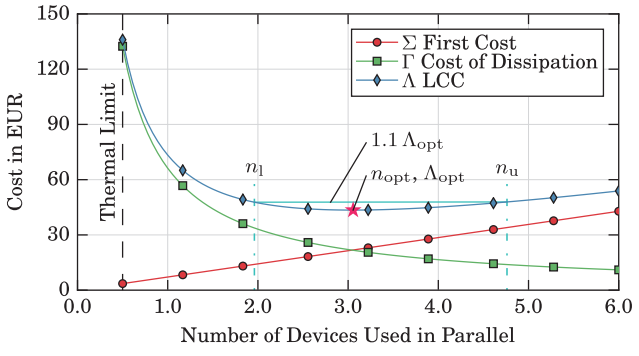


Fig. 7. First cost, cost of dissipated energy and life cycle cost (LCC) as a function of the number of devices connected in parallel for the rectifier bridge $S_{x\bar{k}}$, $S_{\bar{k}z}$ at nominal operation with I_{rms} = 8.1A (P_o = 8 kW). A SiC MOSFET with $R_{ds,on}$ = 96mΩ and a cost of EUR 7.14 is considered as unit device together with a capital equivalent worth of γ = EUR 0.12 per kWh and a run time of t_r = 10 years.

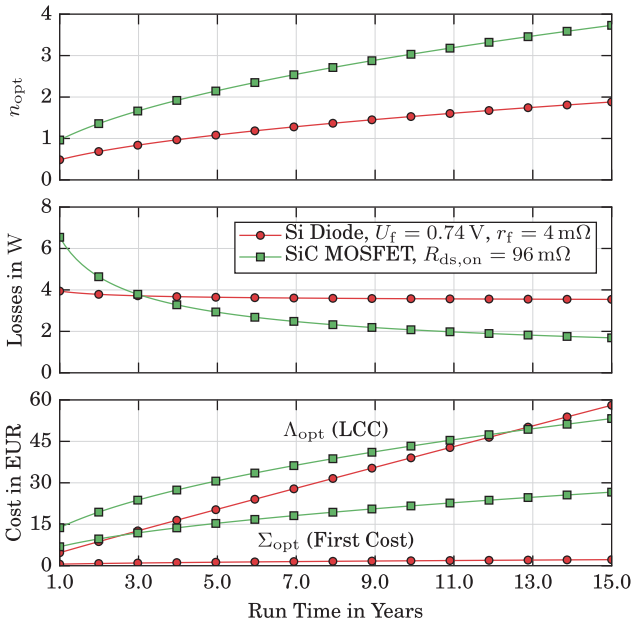


Fig. 8. Optimization results for Si Diodes and SiC MOSFETs showing the optimal (lowest LCC) number of parallel devices, resulting device losses, first and life cycle cost as a function of the run time t_r in years. The same parameters as in Fig. 7 are used.

times lower than the MOSFET's the Si diodes achieves lower LCC for small t_r while the SiC MOSFET achieves lower LCC for $t_r \geq 12.5$ years.

C. Device Selection

So far n has been assumed as a real number which has to be rounded to the next integer or to the next $R_{ds,on}$ value available from the device manufacturer. This leads to a suboptimal LCC, but it can seen in Fig. 7 that $\Lambda(n)$ is flat around the optimum. If a certain allowed increase α in LCC is assumed, a resulting lower and upper bound (n_l, n_u) for permissible values of n can be calculated using (8) as

$$n_l(\alpha) = n_{opt}\left(1+\alpha-\sqrt{(1+\alpha)^2-1}\right) . \quad (13)$$

$$n_u(\alpha) = n_{opt}\left(1+\alpha+\sqrt{(1+\alpha)^2-1}\right) . \quad (14)$$

To derive the required granularity of n the ratio r_n of n_u and n_l can be calculated,

$$r_n(\alpha) = \frac{n_u(\alpha)}{n_l(\alpha)} \quad r_n(0.1) = 2.43 \quad , \quad (15)$$

which does not depend on any device specific parameters in (8) and results in a value of 2.43 for $\alpha = 0.1$ (also shown in Fig. 7). This implies that the achievable LCC is at most 10% higher than the theoretical optimum if the ratio between two consecutive $R_{ds,on}$ values of the available devices is 2.4 or less.

D. Including Switching Losses

In the derivation (9), which gives the LCC optimal number of device, it was assumed that switching losses can be neglected which is typically not the case for the half bridge S_{xy}, S_{yz} used in the current injection circuit. The calculation can be extended by fitting a second order polynomial to measured hard switching losses (turn-on and turn-off) for the switched voltage,

$$E_{sw}(I_{sw}) \approx E_0 + E_1 I_{sw} + E_2 I_{sw}^2 , \quad (16)$$

where I_{sw} is the switched current. Switching losses measured in [23] for a half bridge of two *C2M0080120* SiC MOSFETs and 600V dc link voltage at various I_{sw} are shown in Fig. 9 together with a second order polynomial fitted by least squares regression. If n devices are used in parallel, equal current sharing is assumed and the switching frequency current ripple in the output current can be neglected the total switching losses can then be calculated as

$$E_{sw} \approx n\left[E_0 + E_1\frac{I_{sw,avg}}{n} + E_2\left(\frac{I_{sw,rms}}{n}\right)^2\right] , \quad (17)$$

where $I_{sw,avg}$ and $I_{sw,rms}$ are the average and rms values of the switched current over one mains voltage period. It can be seen that the terms in (17) have the same dependency on n as those in (8) which implies that the optimal number of devices which achieves minimal LCC for a given f_{sw} can be calculated as

$$n_{opt} = \sqrt{\gamma\, t_r \frac{R_{ds,on}\, I_{rms}^2 + f_{sw}\, E_2\, I_{sw,rms}^2}{\sigma_M + \gamma\, t_r\, f_{sw}\, E_0}} . \quad (18)$$

The resulting n_{opt}, first cost $\sum_{opt}$ and LCC Λ_{opt} for the injection switches S_{xy}, S_{yz} are shown as function of the switching frequency f_{sw} in Fig. 10. It can be seen that n_{opt} and therefore $\sum_{opt}$ decrease with f_{sw} while the cost of dissipation Γ increases, mainly due to the switching losses.

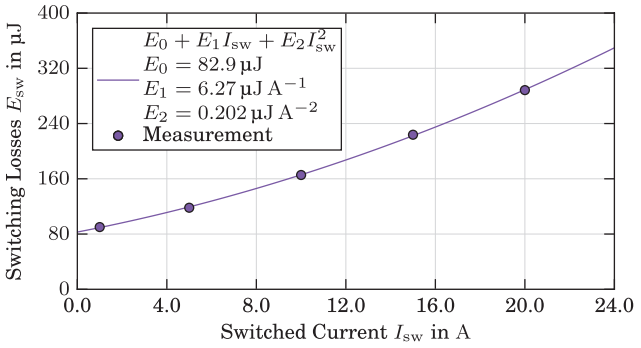


Fig. 9. Sum of turn-on and turn-off losses E_{sw} measured in [23] as a function of the switched current I_{sw} for a half bridge of *C2M0080120* SiC MOSFETs with 600V dc link voltage at 25 °C. Additionally a second order polynomial function fitted by least squares regression is shown and the fitted parameters are given in the legend.

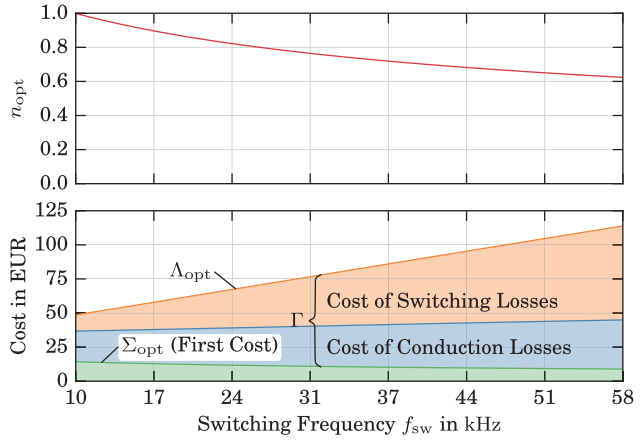


Fig. 10. Life cycle cost and optimal number of MOSFETs in parallel nopt for a half bridge built with *C2M0080120* devices for the injection Switches Sxy and Syz with an rms current $I_{rms} = I_{sw,rms} = 4.7$A and an average switched current of $I_{sw,avg} = 4.1$A as a function of the switching frequency for $t_r = 10$ years.

E. Magnetic Components

The dimensioning of magnetic components is performed

with a similar algorithm, but unlike for semiconductor devices analytical solutions can typically not be found. For a given f_{sw} the current and voltage stresses created by the converter can be determined and for a selected core material, shape and size the optimal number of turns, which minimizes the sum of core and winding losses, can be determined by numerical optimization methods. Using the losses and cost models for core and winding materials the inductor's LCC is calculated, which allows the selection of an optimal core size achieving minimal LCC for the given f_{sw} and t_r.

F. Optimal Switching Frequency Selection

Once the optimal LCC of semiconductors and magnetic components has been calculated as a function of f_{sw} these can be added in order to select a switching frequency which achieves the lowest total LCC. An example calculation for the injection circuit with the switches S_{xy}, S_{yz} and the inductor L_{inj} is shown in Fig. 11, where it can be seen that the inductor's first cost $\sum_{Linj}$ and cost of dissipation Γ_{Linj} and hence its LCC decrease with increasing f_{sw} as opposed to the increasing LCC of the semiconductors, resulting in an optimal f_{sw}. A total run time of t_r = 10 years is assumed in this example.

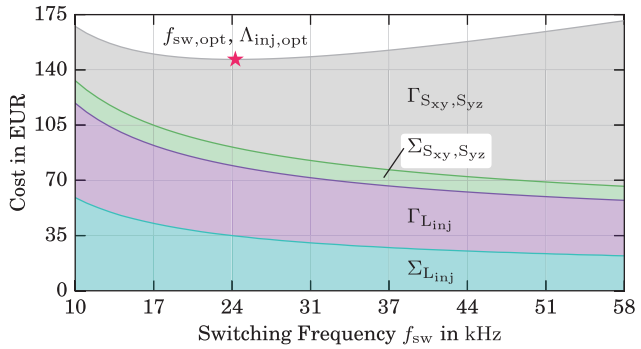


Fig. 11. Example showing the selection of a switching frequency f_{sw} which achieves the lowest sum of LCCs for the injection switches S_{xy}, S_{yz} and the corresponding inductor L_{inj} for t_r = 10 years, not considering any other components of the rectifier.

G. Global Optimization Algorithm

In a final step the algorithm outlined above can be extended to include the entire rectifier to determine the optimal f_{sw} and all optimal component sizes by minimizing the systems LCC

$$\Lambda_{\mathrm{sys,opt}}(t_r) = \min_{f_{sw}} \sum_{k} \Lambda_{k,\mathrm{opt}}(f_{sw}, t_r)\ . \qquad (19)$$

The design procedure sweeps over all relevant switching frequencies f_{sw} and considered run times t_r, where for each tupel (f_{sw}, t_r) and all components k (e.g. switches, inductors, etc.) of the system an optimal relative size $n_{k,opt}$ can be determined which achieves minimal LCC $\Lambda_{k,opt}$ for component k. This implies that all components can be designed independently of each other which simplifies the optimization procedure. Once all components have been selected, their life cycle costs can be summed up which yields the system's LCC for the considered (f_{sw}, t_r) : Once all designs have been calculated the switching frequency achieving lowest overall LCC is selected for each t_r considered in the analysis.

H. Auxiliary Components

The losses, volumes and costs of other components, such as gate drive circuits, DSP/FPGA, capacitors, PCBs, heat sinks, fans, EMI filter, etc have to be considered as well. While their contribution to the overall converter volume, and LCC can be significant, they are almost independent of the design point in the considered application. Therefore these auxiliary components have been considered in the design but were not part of the optimization.

I. Optimization Results

Fig. 12 shows the achievable minimal LCC $\Lambda_{sys,opt}(t_r)$ and the resulting first cost $\sum_{sys,opt}(t_r)$ as a function of run time calculated by the optimization outlined above. It can be seen that the first cost of the optimal systems is less than 30% of the total life cycle cost for a run time of 10 years or more. Furthermore, the LCC is comparable for all three core materials considered in the optimization. Designs using amorphous cores are expected to have slightly higher LCC than systems with nanocrystalline or ferrite cores, which is due to the higher core losses of amorphous materials.

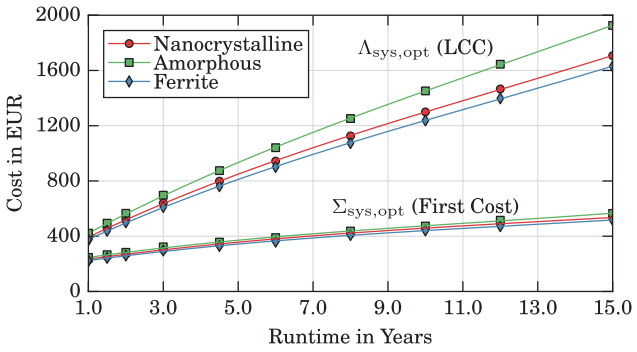


Fig. 12. Minimal achievable LCC and according first cost of optimal converter designs as a function of run time for different inductor core materials. It can be seen that for a run time of ten years, the first cost is < 30% of the total life cycle cost. The optimization results in similar first costs for all three core materials, however the life cycle cost of designs with ferrite and nanocrystalline inductors is slightly lower compared to solutions with amorphous cores.

However, the volumes and switching frequencies of the designed converters differ significantly as shown in Fig. 13; the resulting efficiency as function of t_r is shown in Fig. 14. For short run times ($\leq$ 2 years) converters with high switching frequencies and high power densities achieve minimal LCC as opposed to long run times ($\geq$10 years) where designs with approximately half the switching frequency, twice the volume and half the losses result. Furthermore, these results show that very high efficiencies of up to 99% are economically feasible with available state-of-the-art SiC

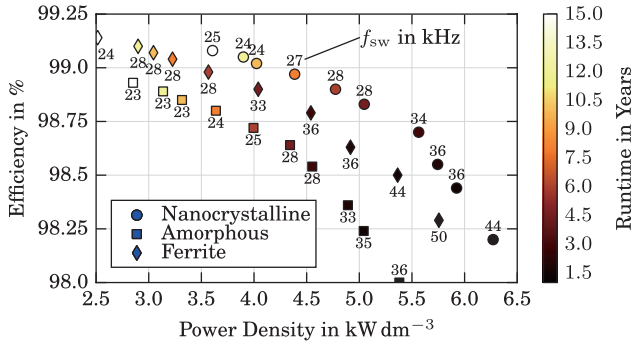


Fig. 13. Optimization results showing power density, efficiency and switching frequency f_{sw} of designs achieving minimal LCC for different run times and inductor core materials of ICT, L_{inj} and L_o.

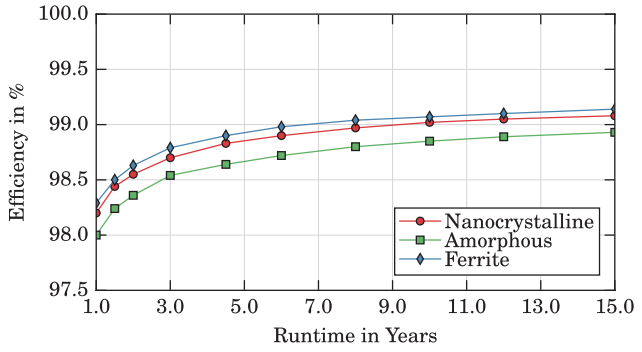


Fig. 14. Calculated efficiencies of life cycle cost optimal converter designs for different run times and core materials.

switches and core materials. Note that three-phase rectifiers based on Si and SiC MOSFETS with slightly lower efficiencies have been reported in the literature [24], [25], however without considering cost.

J. Selected Design

Based on the numerical optimization results the design point with t_r = 10 years, f_{sw} = 27 kHz, a power density of 4.0 kWdm^{-3} and an efficiency of 99% was selected to implement a hardware prototype. *FINEMET* nanocrystalline cores with helical windings (cf. Fig. 15) are used as they achieve considerably higher power density compared to designs based on ferrite. Detailed results of the optimization are shown in Fig. 16: for systems with a run time of 10 years or more, it can be seen that the semiconductors and heat sinks contribute about half of the first cost, life cycle cost and losses, but only about 10% to 20% of the total volume. Furthermore, the auxiliary components, such as PCBs, gate drivers, FPGA/DSP etc. have a significant contribution to both first cost and life cycle cost which implies that they cannot be neglected in the design process.

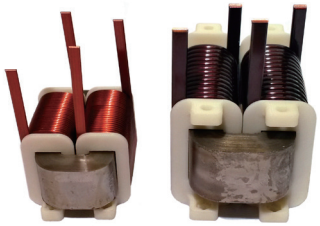


Fig. 15. Picture of L_{inj} and L_o, implemented using nanocrystalline C cores and helical windings. A boxed volume of 88 cm^3 and 249 cm^3 results for the two inductors. The specifications and parameters of the implemented inductors are given in Table II.

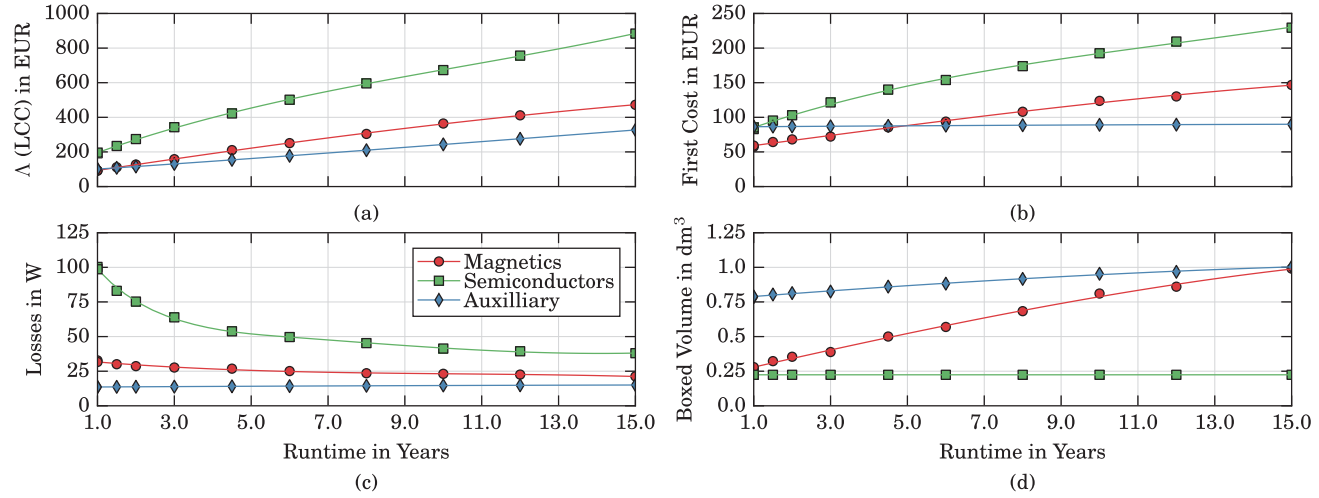


Fig. 16. Spline interpolated results of the numerical optimization (markers) for the semiconductors (incl. heatsinks), magnetics and remaining components (e.g. fans, gate drivers, PCBs, DSP/FPGA, capacitors, EMI filter) of the circuit shown in Fig. 4. Nanocrystalline cores with helical windings are used for all magnetic components as they offer the best performance in this case, cf. Fig. 13. Plot (a) shows the optimal LCC $\Lambda(t_r)$, (b) shows the corresponding optimal first cost $\sum(t_r)$, (c) the losses occurring in the components and (d) their boxed volume. It can be seen that the semiconductors contribute about half of the first cost and losses and hence the life cycle cost, but only ≈ 10% to 20% of the total converter volume.

IV. Hardware Prototype

Using the optimization results presented in the previous chapter, an 8 kW, prototype IAF rectifier with a switching frequency of f_{sw} = 27 kHz, according to the specifications given in Table I, was implemented. A picture of the hardware is shown in Fig. 17 and its main components are listed in Table II.

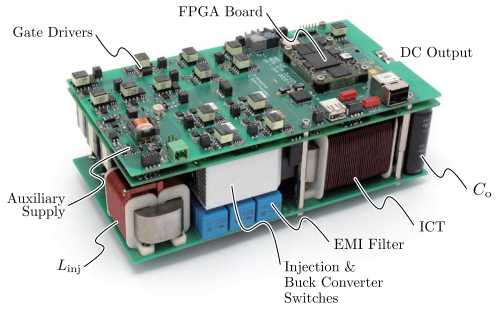
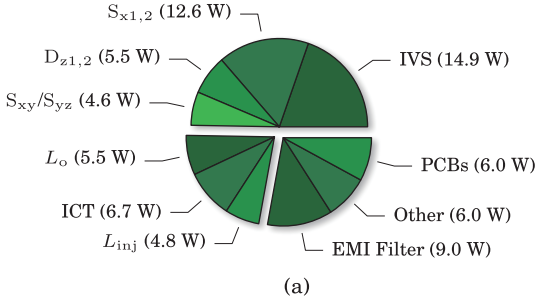


Fig. 17. Picture of the hardware prototype, measuring 220mm x 118mm x 77mm (8.66 in x 4.65 in x 3.03 in). This results in a power density of 4.0 kWdm^{-3} (65W in^{-3}).

TABLE II
Components Used in the Hardware Prototype

	L_{inj}	ICT	L_o
Core	F3CC-6.3	F3CC-25	F3CC25
Wire	1 x 4 mm	1 x 6 mm	2.4 x 6 mm
Turns	52	36:36	30
Inductance	750 µH	3 mH	300 µH
Volume	88 cm^3	245 cm^3	249 cm^3
Losses	4.8 W	6.7 W	5.5 W
$S_{x\bar{k}}$, $S_{\bar{k}x}$	C2M0025120		P_{loss} = 1.7 W
$S_{\bar{k}y\bar{k}}$	C2M0080120		P_{loss} = 0.8 W
S_{xy}, S_{yz}	C2M0080120		P_{loss} = 2.3 W
S_{x1}, S_{x2}	C2M0025120		P_{loss} = 6.3 W
D_{z1}, D_{z2}	C4D40120D		P_{loss} = 2.7 W

A more detailed distribution of the calculated component losses for the implemented prototype at nominal operating conditions and the corresponding component volumes are shown in Fig. 18. About 50% of the total losses occur in the semiconductors. Core and winding losses in the main magnetic components L_o, *ICT* and L_{inj} account for ≈ 22% of the total losses. The remaining 28% occur in the EMI filter, the PCB tracks, and other elements such as fans, gate drivers, FPGA, current sensors etc. Measurement results of the prototype converter are presented in the following.



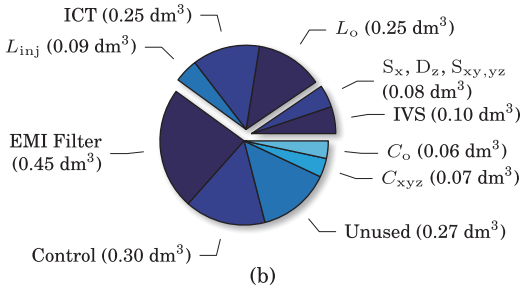


Fig. 18. The calculated distribution of losses for the selected design point at nominal operation is shown in (a), the corresponding component volumes are shown in (b). Category *other* includes fans, gate drivers, FPGA, ADCs, current sensors, auxiliary supply, etc.

A. AC Input Currents

In Fig. 19 measurement results of the prototype rectifier operated at full load and nominal input voltage are shown. Sinusoidal input currents with slight distortions at the mains voltage sector boundaries result as expected from simula-

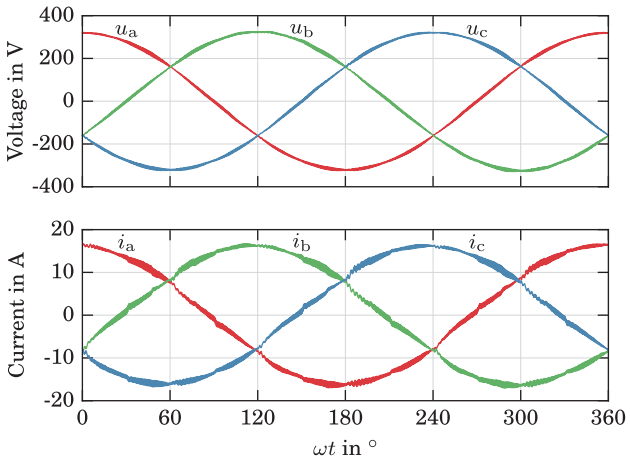


Fig. 19. Measurement results with the converter operating at nominal conditions and full output power, i.e. P = 8 kW, U_1 = 230 V$_{rms}$ and U_{pn} = 400 V. Note that phase quantities a and c were measured directly, phase b was recreated numerically as $u_b = -u_a - u_c$ and $i_b = -i_a - i_c$.

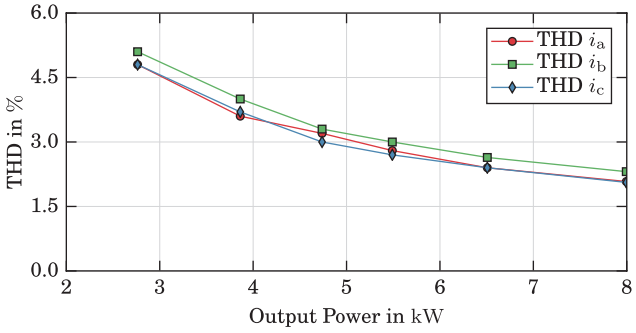


Fig. 20. Total harmonic distortion (THD) values of the rectifier's mains input line currents as a function of output power for nominal input and output voltages, measured using a *Yokogawa WT 3000* power analyzer.

tion. The measured total harmonic distortion of the mains input currents as a function of the dc output power is shown in Fig. 20.

B. Efficiency

A comparison of the rectifier's calculated and measured efficiency as a function of dc output power is shown in Fig. 21. The solid lines show the calculated efficiency for 400V and 380V output voltage, while the round and triangular markers show measurements taken with a *Yokogawa WT 3000* power analyzer. Additionally three efficiency measurements were taken based on a direct measurement of the converter's losses using a calorimeter which closely match the values obtained by the electrical measurement.

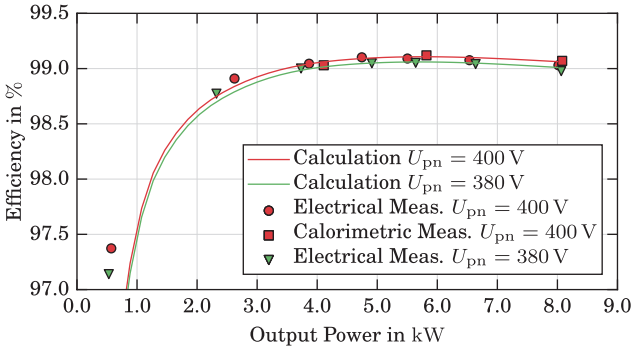


Fig. 21. Comparison of measured and calculated converter efficiencies for two different dc output voltages U_{pn}. The electrical efficiency measurements were performed with a *Yokogawa WT 3000* power analyzer. For U_{pn} = 400V additional measurements were done using a calorimeter. All measurements were taken at nominal ac input voltage U_l = 230V_{rms} and an ambient temperature of 30 degrees C.

C. ICT Current Balance

As written in Section II-C unsymmetries in the interleaved buck converter lead to an unbalance of the ICT currents i_{o1} and i_{o2} which create a dc offset in the ICT's magnetizing current i_m. Measurement results of the buck converter output voltages u_{Dz1}, u_{Dz2}, the ICT currents and the derived magnetizing current are shown in Fig. 22. Note that no active controller was used to balance i_{o1} and i_{o2}, resulting in a peak magnetizing current of 0.73A and average value of 0.42 A. This corresponds to a peak core flux density of ≈ 460mT which is far below the core material's saturation flux density of 1.2 T.

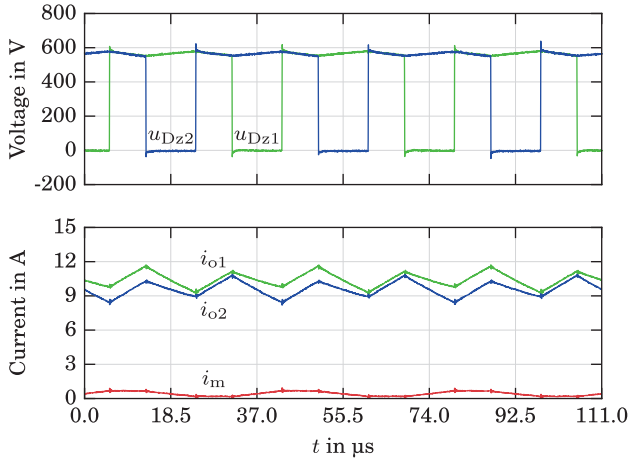


Fig. 22. Measurement of the interleaved buck converter output voltages u_{Dz1} and u_{Dz2}, the ICT currents i_{o1} and i_{o2} and the calculated ICT magnetizing current i_m for converter operation with nominal power at $\omega t \approx 0°$, i.e. at the peak of the six-pulse voltage u_{xz} (cf. Fig. 3) with a peak value of $i_{m,max}$ = 0.73 A.

D. Conducted EMI

A two stage EMI filter with a reactive power consumption of ≈ 4% of the rectifiers output power rating has been implemented. Its structure is shown in Fig. 23 and the values of all components are listed in Table III. However, a detailed analysis of the filter and of its design process is out of the scope

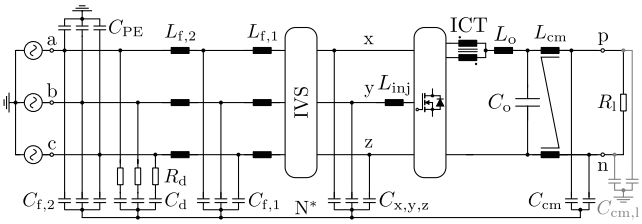


Fig. 23. Schematic of the implemented EMI filter with two combined CM/DM filter stages $L_{f,1}$, $C_{f,1}$ and $L_{f,2}$, $C_{f,2}$ at the ac input and an additional CM filter stage L_{cm}, C_{cm} at the dc output. The component values used in the prorotype are listed in Table III.

TABLE III
EMI FILTER COMPONENTS

C_{xyz}	4.4 µF	2 x 2.2 µF Epcos B32923, X2 in parallel
$L_{f,1}$	22 µH	PQ26/25, 10 turns, 1 x 4mm wire
$C_{f,1}$	2.3 µF	5 x 470 nF Epcos B32922, X2 in parallel
$L_{f,2}$	15 µH	Würth Elektronik 7443641500
$C_{f,2}$	1.4 µF	3 x 470 nF Epcos B32922, X2 in parallel
C_d	0.9 µF	2 x 470 nF Epcos B32922, X2 in parallel
R_d	4.7 Ω	4 x 1W 1218 SMD Thick Film resistors
C_{PE}	47 nF	Epcos B3202, Y2, connected to case
L_{cm}	≈ 200 µH	Vacuumschmelze W424, 5 turns, 2.5mm wire
C_{cm}	130 nF	4 x 33 nF MLCC in parallel

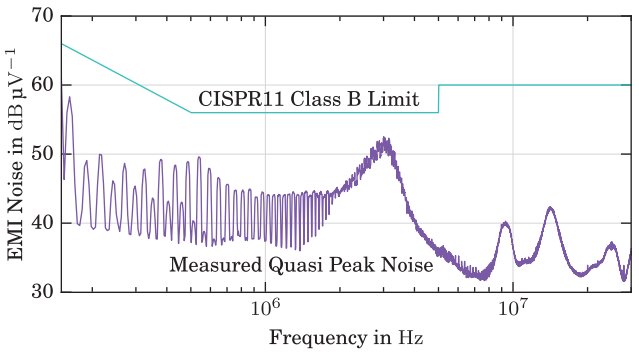


Fig. 24. Measured quasi-peak conducted EMI noise emission and corresponding CISPR11 class B limit for the 150 kHz to 30 MHz range with a bandwith of 9 kHz, measured in 4 kHz steps.

of this paper. Measurement results of the conducted EMI noise spectrum, using the quasi-peak detector, are shown in Fig. 24 together with the CISPR11 class B limit for the 150 kHz to 30MHz range.

V. Conclusion

This paper describes a life cycle cost driven optimization process were not only the first cost of a converter, but also the capital equivalent worth of the energy dissipated during the system's service life is considered. This allows the selection of optimal components, such as switches, inductors, transformers, etc., which achieve minimal cost for a given application, run time and switching frequency. By sweeping over a range of suitable switching frequencies a cost optimal converter system can then be found.

As an example an 8kW buck-type three-phase interleaved Integrated Active Filter rectifier for 380V dc distribution systems in data center and telecommunication applications is designed. Using state-of-the-art SiC MOSFETs and nanocrystalline cores a design with a power density of $4kWdm^{-3}$ and an efficiency of 99% results. Measurement results taken on a hardware prototype verify the validity of the employed models.

However, the cost driven optimization process is not only useful for data center applications with continuous operation, but could also be used in other applications were the system operates only for a relatively short period of time. For example in an on-board charger of a plug-in hybrid vehicle, which is used only once or twice a day for 1 to 2 hours, the first cost. Similarly the cost of weight and volume is expected to have significant impact on power electronic systems in aircraft, where weight has an impact on the vehicle's fuel consumption and hence on the life cycle cost. This is expected to lead to cost optimal systems with a higher switching frequency, higher power density and lower efficiency. In such cases an equivalent first cost, including weight and/or volume and the cost of conversion losses can still be used to compare, optimize and select components, circuit topologies and converter systems achieving minimal life cycle cost.

Acknowledgment

The authors would like to thank ABB Switzerland Ltd. for the funding and for their support regarding many aspects of this research project. Furthermore we would like to thank Ms. A. Kengunte for her help in the design, assembling and commissioning of the hardware prototype.

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Latest Advances of LLC Converters in High Current, Fast Dynamic Response, and Wide Voltage Range Applications

Yang Chen and Yan-Fei Liu

***Abstract*—LLC converter has been the simplest topology since long to achieve soft switching and overall the highest performance within small form factor at converter level. This paper discusses the latest advances of LLC converter from the perspective of topology and control. The technology ranges from high current, fast dynamic response to wide operational voltage range. The application mainly falls in the scope of server and data center, and may also cover telecom, PV, battery charging, etc.**

***Index Terms*—LLC, review, survey, current sharing, multiphase, interleave, phase shedding, passive impedance match, SR drive, fast dynamic, current mode control, current sensing, wide voltage range, hold up, high voltage gain.**

I. Introduction

AFTER being invented for decades, LLC converter is proved as an excellent vehicle of power conversion. From the perspective of both topology and design, LLC converter is perhaps the simplest way to achieve ZVS on the primary switches (mostly MOSFETs) and ZCS on the rectifiers (eventually diodes), which respectively removes the turn on loss and the reverse recovery loss – two most urgent losses related to switching frequency. Thus, the gap ahead of the hard switching topologies is widened when the switching frequency gets higher. Yet the improvement and development is still undergoing to reform LLC converter to best fit the industry and consumer needs in different applications.

Among the various applications that LLC converter has significantly impacted, including the server and data center, telecom, PV, battery charging, etc., data center power system raises the most concern and research interest due to the existing scale of power assumption as well as the ever-increasing demand [1]. The latest survey has found that data centers consumed around 1.5% of the 270 terawatt-hours electricity usage in 2012, globally [2]. The percentage is even higher for the US at 2.2%. Additionally, the energy cost of powering a typical data centers is doubled every five years [3]. It is estimated that the data center alone will consume 10% of the total electricity by 2020 [4]. Thus, large savings of electricity bill can be made by improving the efficiency and performance of the power conversion inside the data center power system.

Wide band gap devices have made undeniable contribution to the advances of power converters in achieving high efficiency, high power density and potentially low cost when the technology becomes mature. The evolving topology and control is another propulsive force on the other wing. In this paper, the latest technologies of LLC converters in high current, fast dynamic response and wide voltage range applications will be discussed from the perspective of improving the topology and control.

The organization of this paper is as follows. Section II will discuss the performance of multiphase LLC converters and accurate driving for synchronous rectifiers. Section III will discuss technologies related to current mode control and other high level control of LLC converters to achieve fast dynamic response. Section IV will discuss the improving methods of LLC converter to meet the demands of holdup and wide voltage range operations. The paper will be concluded in Section V.

II. Technologies for High Current Application

It is generally believed that 100 W to 1 kW is the preferred power range for LLC converter. For lower power, which further emphasizes the simple structure and low cost, topologies like Flyback is dominant. For high power/current applications, the design becomes difficult for LLC converter. High current ripple causes high loss on the capacitor filter. And large capacitor value is needed to meet the voltage ripple requirement. Besides, the package inductance of the synchronous rectifiers (SR) introduces volt-level voltage deviation at 50 A, 500 kHz level, which could easily trick the voltage-based gate drivers with improper timing. The layout of SRs is also difficult to achieve balanced loops and thermal performance.

A. Multiphase and Current Sharing

The issues come with the high output current could be solved by either splitting the single power train into multiple paralleled phases inside the module, or paralleling multiple phases/modules. Either way will reduce the power that each LLC phase should deal with. It should be noted that this conclusion is drawn with the assumption that current sharing

Manuscript received Mar. 24, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00007

among phases is achieved.

As an example of the split phases within single converter, [5] demonstrates a 1 kW 1MHz LLC converter with four phases. The conventional single transformer is separated into four small transformers. So, on the secondary side, the power train is split into four phases in parallel, with each phase dealing with a quarter of the total load power. As the primary windings are connected in series, the load current of the four phases are naturally balanced. Another highlight of this structure is that the connection point of the multiple phases could be designed at the DC side, so that the terminal loss/winding loss generated by the high frequency AC current is reduced. Similarly, 1.5% of efficiency increase is achieved by using eight phases [6].

B. Interleaving

Interleaving between phases is a desired feature on top of current sharing. The output capacitor currents stress as well as the capacitor value could be reduced at the same time. Such techniques that improve the performance and reduce the cost are most welcome to the industry. To achieve interleaving, the switching frequency of each phases must be same so to avoid beat frequency components. The primary switches must operate with 90° (180°/2) phase shift for two phases interleaving, and 60° (180°/3) for three phases interleaving, and so on.

The topology introduced in [7] is a straightforward demonstration of an interleaved two phase LLC converter. The input voltage is split by two capacitors and fed to the two phases in series. The output side of the two phases are connected in parallel. With this simple structure, if one phase has higher voltage gain, then that phase will provide more power to compensate the gain difference. Thus, the input capacitor of that phase will discharge more, so the input voltage of that phase will reduce, and the power transferred by that phase will also reduce. This intrinsic negative feedback generally provides good current sharing, but cannot fully remove the load current difference.

The source of the unbalanced load current is the different voltage gains between phases at given quiescent point, which is caused by the resonant components' tolerances. By employing the switch controlled capacitor (SCC), the equivalent resonant capacitor value can be controlled so to compensate the component tolerances, and thus the voltage gain difference [8], [9]. Besides, the switches always achieve ZVS, which maintains the attractiveness at high frequency applications. Fig. 1 shows the structure and waveform of a half wave SCC circuit. The equivalent capacitor value could be found as in (1).

$$C_{SC,HW} = \frac{2C_a}{2-(2\alpha-\sin 2\alpha)/\pi} \tag{1}$$

Fig. 2 shows the topology of the two-phase SCC LLC converter. The primary switches operate with same switching frequency while out of phase for interleaving, by which the

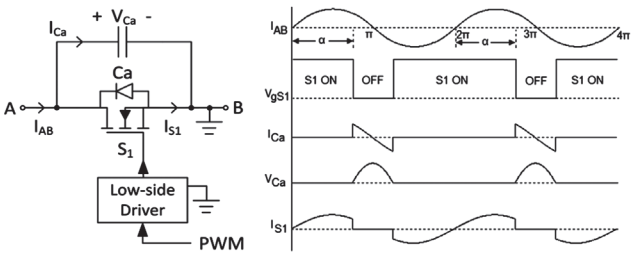

Fig. 1. Structure and waveforms of half-wave SCC circuit.

output voltage ripple is reduced by 4 times. The SCCs can actively compensate voltage gains at different frequencies, which enables accurate current sharing performance throughout the load range. It is worth mentioning that the switches of SCC are ground referenced, and of small footprint. 60 V/2 A MOSFETs could be used in 600 W application. Besides, the SCC LLC converter is able to achieve phase shedding. Thus, the light load efficiency is significantly higher than its counterparts.

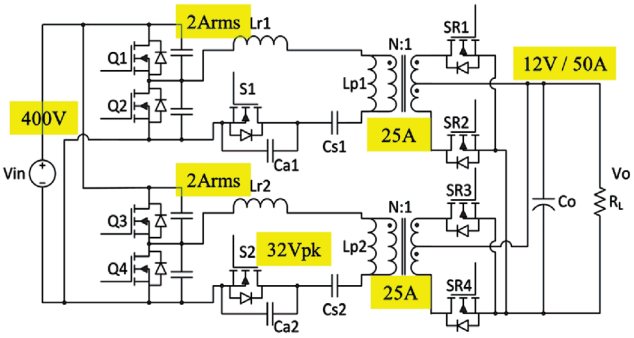

Fig. 2. Two-phase SCC LLC converter.

C. Current Sharing with Passive Impedance Matching

Paralleling multiple modules/phases directly at both the input side and output side are more common and practical in centralized load applications. During installation and fault, power modules could be easily cut in and out with hot swap setup. Conventional multiphase LLC converter regulates the output voltage and phase current with a current loop. The different frequencies for different phases would inevitably introduce the beat frequency ripple, and force great duty on the EMI filter. Improved methods like [7]-[13] remove most of the drawbacks but still needs the sensing and control. Comparing with these active current sharing methods, passive current sharing topologies benefits both the end user and the designer with low cost and extreme simplicity.

Fig. 3 shows the common inductor two-phase LLC converter as an example of the passive current sharing method [14], [15]. As compared to the conventional two-phase LLC converter, only a wire is added at no cost. The primary switches of the two phase operate at the same frequency to regulate the output voltage and total load current, just like conventional single phase LLC converter.

The current sharing ability is achieved by the common

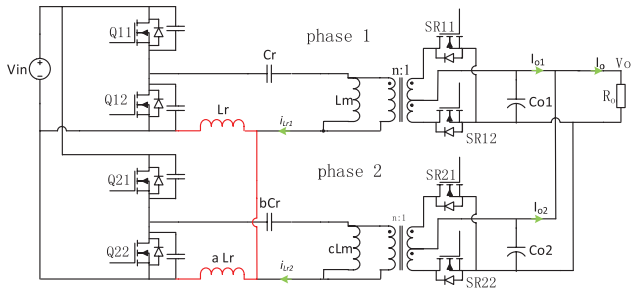

Fig. 3. Common inductor two-phase LLC converter.

inductor of the two phases, thus no additional phase current sensing or control. In conventional two-phase LLC converter without the current loop, the input square wave voltage is the same, and the transformer primary side could be viewed as a constant voltage source, which is also same for the two phases. Thus, the phase current is determined by the combined impedance of the resonant inductor and the resonant capacitor, which is close to zero around resonant frequency. Thus, a small tolerance on the components will cause very large difference. For the common inductor LLC converter, however, the phase current is determined by the resonant capacitor alone, as the inductor is shared by both phases. Consequently, the current of respective phase is nearly proportional to the capacitors' tolerance, which usually under 5%. This is a perceptual understanding of the current sharing mechanism for common inductor LLC converters.

A more detailed explanation of the current sharing mechanism could be found in Fig. 4, in which the common inductor is equivalent to four components – one virtual inductor plus one virtual resistor for each phase [16]-[18].

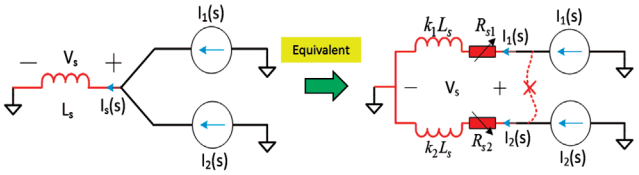

Fig. 4. Common inductor and the its equivalent model with virtual open and virtual short.

In the equivalent model, the virtual inductor and virtual resistor tanks of respective phases are independent (virtual open), which means there is no current commutation between phases. Also, the voltage cross each virtual inductor and virtual resistor tank is the same as that of the common inductor, thus the tanks are also virtual short.

At given switching frequency, (2) must hold true. Solving (2), one can find that the two virtual resistors are always of opposite sign. Whichever phase bears heavier load will have a positive virtual resistor, and the phase with lighter load will have a negative resistor. These two virtual resistors are the key to current sharing performance, as they enable a natural negative feedback – the positive resistor will decrease the power of the phase with heavy load, while the negative resistor will increase the power of the other phase with lighter load.

$$\frac{(sk_1L_s + R_{s1})(sk_2L_s + R_{s2})}{(k_1 + k_2)sL_s + (R_{s1} + R_{s2})} = sL_s \tag{2}$$

Fig. 5 shows the current sharing performance of the common inductor LLC converter. The two phases' current have less than 1% difference at heavy load. At light load, although phase shedding will be used in practice, the current sharing performance maintain as high.

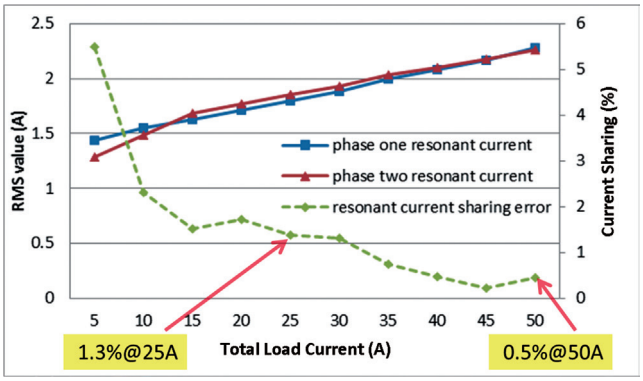

Fig. 5. Resonant current RMS value and the current sharing error.

Common capacitor LLC converter has also been verified to achieve good current sharing performance [19], [20]. In addition to LLC converter, the passive impedance matching methods can also be applied to other resonant converters. More research can be done in this area.

TABLE I summarizes the features of different multiphase technologies in the high current applications.

D. Accurate Synchronous Rectifier Driving

The driving of synchronous rectifier is a well-known difficulty for not only LLC converters but also many other topologies, such as Flyback. Historically, many methods have been tried. Current-based methods which need current sensing transformers gradually lose the attractiveness due to the complexity and extra loss [21]-[25]. Currently, the mainstream is the voltage-based methods that detect the voltage across the drain and source of the SR to generate the driving signal.

The basic idea of the voltage-based method is to turn on the SR when v_{DS} equals to the body diode conducting voltage, and turn off the SR when v_{DS} comes back to zero. This holds true if only R_{dson} is considered. However, in practice, the package and PCB track inductances will also introduce a voltage of same scale if not larger, which makes the v_{DS} no longer an accurate trigger, more specifically an early trigger for turn off [26]-[28].

To obtain the accurate current information in the SR, several methods borrowed the knowledge from the conventional DCR meter, which is used to measure the DC resistor of an inductor. An elegant example of this method is the zero-crossing noise (ZCN) filter which added three passive components to achieve accurate turn on/off timing as well as diode switching

TABLE I
COMPARISON OF DIFFERENT MULTIPHASE TECHNOLOGIES

Technology	Current Sharing	Cost	Complexity	Interleaving	Phase Shedding
in-module multiphase	Good	Low	High	No	No
split capacitor multiphase	Modest	Modest	Low	Yes	No
SCC multiphase	Excellent	Modest	High	Yes	Yes
conventional with current loop	Excellent	Modest	High	No	Yes
passive impedance matching	Good	Low	Low	No	Yes

noise filtering [29], [30]. Fig. 6 shows the circuit of the ZCN filter.

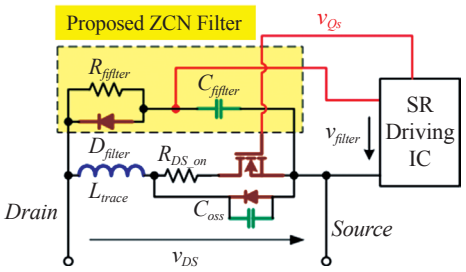

Fig. 6. The ZCN filter for SR accurate driving.

During turn on, C_{filter} discharges through D_{filter} together with C_{oss}, thus there is not delay at turn on. Besides, the ringing of the parasitic inductors and C_{oss} can be filtered during the diode switching, which avoids false turn on. During turn off, C_{filter} will be charged through R_{filter}, so that a delay is created to compensate the early zero-crossing voltage created by the parasitic inductors. Very accurate timing could be achieved if the filter is designed so that (3) holds.

$$\tau_{filter} = R_{filter} \cdot C_{filter} = \frac{L_{trace}}{R_{dson}} \tag{3}$$

The ZCN filter can capture accurate switching time for SR in both transient and steady state, despite of the load current. The efficiency of a 600 W LLC converter could be improved by 0.8% as compared to conventional SR driving at basically no cost. This ZCN filter can also be applied to Flyback converter.

III. TECHNOLOGIES FOR FAST DYNAMIC RESPONSE

At different operation points, the LLC open-loop transfer functions vary between first order system and secondary order system, which makes the compensation difficult to optimize, hence a slow dynamic response in general.

From the experience with Buck converters, current-mode control is expected to improve the dynamic response. Different from Buck converters' current sensing, LLC converter has non-linear current shape, which is a time-domain superposition of trigonometric and triangular waveforms. Thus, the instantaneous input power cannot be easily extracted from the peak current or other instantaneous current values.

A. Cycle-by-Cycle Average Current Sensing

The average current-mode control senses the average resonant current using a current transformer and low pass filter. The compensator design is simplified as compared to voltage-mode control. However, the bandwidth is cannot be improved due to the low pass filter in the current sensing circuit. Besides, the conventional sensing method is not suitable for multiphase LLC converters that requires current sharing, because shared average current in the primary side does not necessarily guarantee good load current sharing.

Inspired by trajectory control, which reveals the relationship between resonant capacitor voltage and output current at the resonant frequency, cycle-by-cycle average current sensing method can accurately calculate the input charge at arbitrary switching frequency, based on the capacitor voltage at the turn off instant of the primary switches [31]. The relationship of the input charge and capacitor voltage is illustrated in Fig. 7.

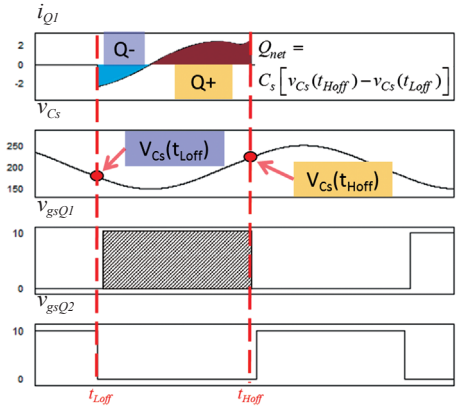

Fig. 7. Relationship of input charge and resonant capacitor voltage.

Taking advantage of the symmetry of resonant capacitor voltage, only one sensing is needed for each cycle to obtain the average current value. For half bridge LLC converter, the equation of the input average current is shown as in (4). Similar equation could be developed for full bridge LLC converter.

$$I_{in\_ave} = f_s C_s \left[2v_{Cs}(t_{Hoff}) - V_{in}\right] + 2C_j f_s V_{in} \tag{4}$$

TABLE II shows the comparison of the calculated input power and the measured data. As can be observed, the cycle-by-cycle current sensing method is very accurate, despite

TABLE II
COMPARISON OF MEASURED AND CALCULATED INPUT POWER

Load current	5A	10A	15A	20A
Actual P_{in}	71.6 W	136.1 W	199 W	263.6 W
$v_{Cs}(t_{Loff})$	199.2 V	188.8 V	178.4 V	166.4 V
$v_{Cs}(t_{Hoff})$	199.2 V	211.2 V	221.6 V	233.6 V
f_s	199.5 kHz	197.3 kHz	197.0 kHz	195.5 kHz
Calculated P_{in}	71.6 W	135.9 W	196.0 W	263.6 W
Error	0.00%	-0.13%	-1.50%	-0.02%

the load current value.

Other than current-mode control, the cycle-by-cycle average current sensing method can also be used to achieve current sharing for multiphase LLC converter. As the reference is the input charge/power rather than the resonant tank current, the current sharing performance is significantly better than the conventional current sensing method with current transformer. Fig. 8 shows the simulation comparison of the conventional method and the cycle-by-cycle average current sensing method.

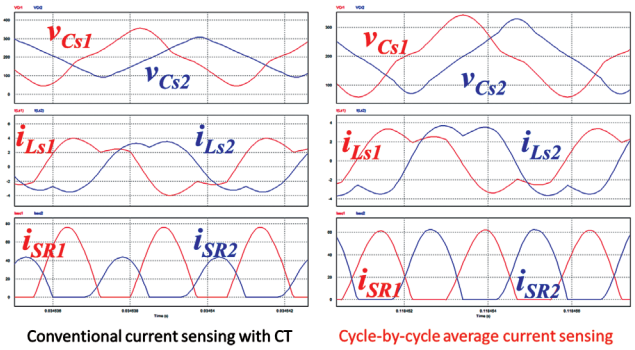

Fig. 8. Current sharing performance comparsion of conventional and cycle-by-cycle average current sensing.

B. Bang Bang Charge Control for Fast Dynamic Response

As commented previously, both voltage-mode control and conventional average current-mode control suffers from poor dynamic response performance.

The optimal trajectory control based on state-plane analysis can achieve very fast dynamic performance for series resonant converter [32]. However, when it comes to LLC converter, the extra state variable greatly increase the complexity. If fixed at resonant frequency, the simplified trajectory control can still achieve very fast dynamic performance [33]. In general, the trajectory based control requires inductor current and load current sensing, which could be complicated and lossy.

Bang Bang Charge Control (BBCC) only need to sense the resonant capacitor voltage, based on which the turn off timing of the primary switches is determined. The input power of each cycle can be then controlled directly. Thus, very fast dynamic response is achieved without complicated sensing or performance degradation [34].

The operation of LLC converter with Bang Bang Charge Control is shown in Fig. 9. The high threshold controls the turn off timing of the high side switch, and the low threshold controls the turn off timing of the low side switch. Only one of the two thresholds serve as the control variable, and the other one could be calculated based on the symmetrical waveform.

The transfer functions of both open loop and close loop are plotted in Fig. 10. As can be observed, the open loop ap-

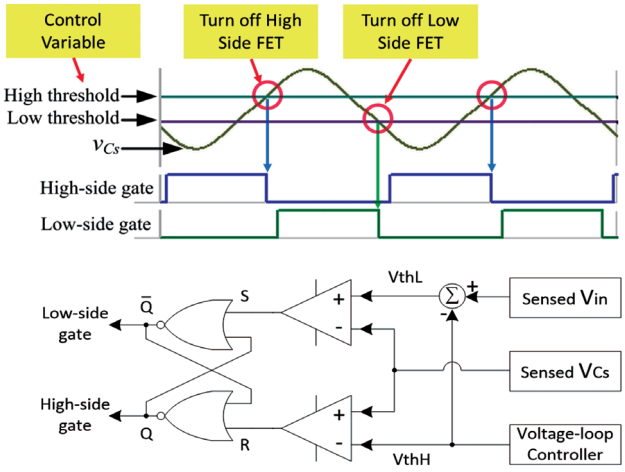

Fig. 9. Principle and operation of LLC with BBCC and the implementation.

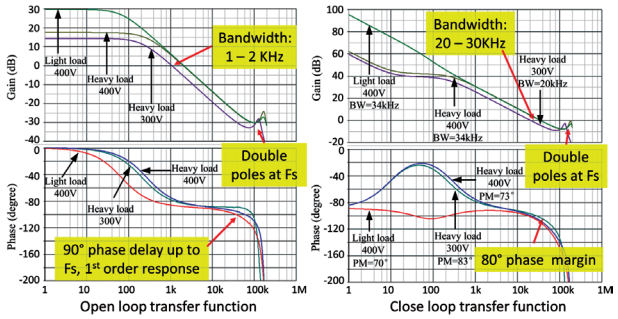

Fig. 10. Openloop and closeloop bode plot of Bang Bang Charge Control.

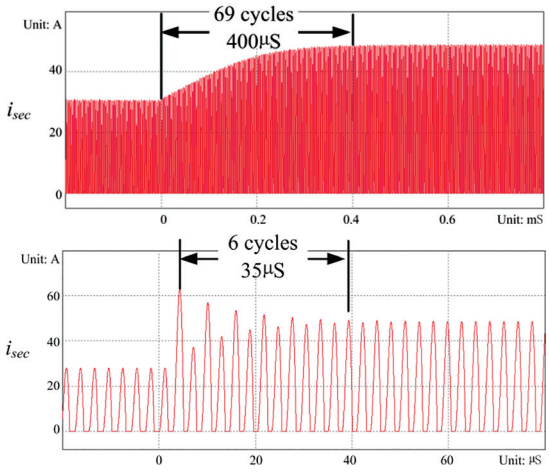

Fig. 11. 10 A to 20 A step load change of frequency control (up) and Bang Bang Charge Control (down) at 400 V input.

pears as first order system, which can be easily compensated. With simple PI control, the bandwidth is improved from 1-2 kHz to 20-30 kHz for different input and load conditions, which is approximately 1/6 – 1/5 of the switching frequency.

Fig. 11 shows the load step response at 400 V input. With conventional frequency control, it takes 70 cycles or 400 µs to reach steady state. While the Bang Bang Charge Control reduce it to 6 cycles, which is less than 40 µs.

IV. Technologies for Wide Voltage Range Application

There are generally two types of requirement in the wide voltage range field – holdup requirement and the wide voltage range requirement itself. Although both require the LLC converter to achieve high voltage gain, the holdup application and wide voltage range application still have subtle difference in terms of requirements and solutions.

In holdup application, normally, the converter operates for long time at high input voltage. The converter only occasionally operates at low input voltage for short period, such as less than 1 second. Thus, the converter design should emphasize on the optimization at high input voltage. Design considerations for the low input voltage, e.g. thermal design, could be de-rated.

For wide voltage range application, the converter should be able to operate at the entire input voltage range for extended time. Therefore, the entire range should be optimized from both efficiency and cost point of view. The wide voltage range requirement is mandatory in many applications, such as photovoltaic and battery charging. Even in the server and data center power systems, it is becoming a more solid requirement.

A. Holdup Operation

The holdup operation is introduced and originally solved by the range winding technique [35]. The transformer has two sets of secondary windings. At normal operation, the transformer operates with the winding of small turns ratio, which is optimized. During holdup period, the winding with high turns ratio is used, such that the voltage gain is increased.

By driving the half-bridge MOSFETs with asymmetric pulse-width modulation (APWM) rather than conventional frequency modulation, LLC converter can improve voltage gain without any additional components [36]. However, the improvement relies on the parameter design.

A critical insight was revealed in [37] that if the resonant tank can be charged with more energy during one switching cycle, LLC converter achieves higher voltage gain. To charge the resonant tank more, the secondary windings are short circuit for a certain period in every switching cycle. Based on [37], a few improving methods have been proposed to adopt either Boost PWM discontinuous current mode (DCM) control [38] or phase shift control on LLC topology [39], [40]. These methods share the similar intrinsic principle with [37], but optimize the LLC converter for different specifications with respective topologies, circuits and control.

Fig. 12 shows an example of the six topologies in the sLLC converter family [41], [42]. The sLLC converter still uses center tapped transformer with synchronous rectifiers, which are commonly seen in the 12 V output applications.

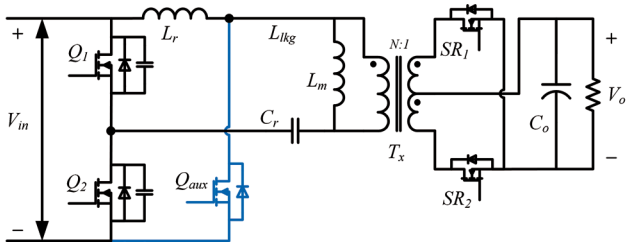

Fig. 12. sLLC converter with center-tapped transformer and SR.

The auxiliary switch remains idle at normal operation, thus the efficiency for 400 V operation can be optimized. During holdup period, the ground referenced auxiliary switch operates in PWM mode to energize the resonant inductor with the input voltage directly. The inductor then can store more energy in each cycle, and the converter achieves higher voltage gain. The detailed operation for 400 V input and 250 V input are illustrated in Fig. 13.

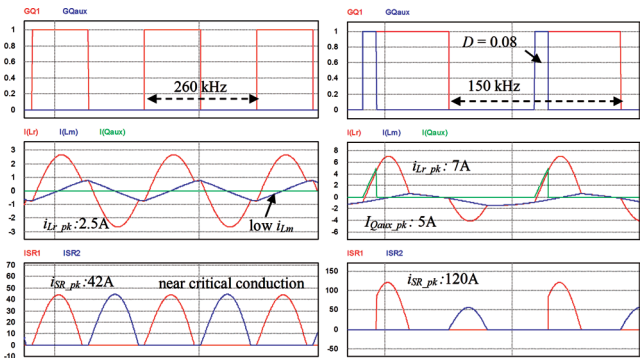

Fig. 13. sLLC converter operation with 12 V/25 A load at normal input 400 V (left) and during holdup at 250 V (right).

B. Wide Input Voltage Range Application

For operation with wide input voltage range, the converter's performance and stability cannot be compromised. The methods used in the holdup application are generally not suitable due to weakened robustness.

Conventionally, a boost converter is used between the AC and the LLC stage in data center application. DC applications could also use this structure to deal with the wide input range. The method is straightforward and the control is well established [43], [44]. The downside is the complexity and cost.

By using full bridge instead of half bridge, the voltage gain of LLC converter is doubled without changing the design. Using three level branch to replace the half bridge achieves similar effect [45]. For example, if the peak voltage gain is 2 for the half bridge configuration, then the peak volt-

age achieved by switching to full bridge is 4. This means the allowed maximum input voltage is four times the minimum. By using two phases, the voltage range could be increased to 8 times [46]. However, with conventional frequency control, the converter operates with either half bridge or full bridge (three level) at a time, and there is no middle ground. Thus, to make use of the ZVS + ZCS region, the peak voltage gain of the resonant tank must be at least 2 times of the resonant point, which might constrain the design and efficiency in some cases.

A few improving methods use similar idea of switching between full bridge and half bridge, but make the mode switching inside each switching period [47]. Consequently, the equivalent input square wave voltage can be smoothly changed by controlling the conduction time of half bridge mode and full bridge mode (three level mode). The control can be implemented with frequency modulation, PWM, phase shift, individually or jointly, depending on the actual circuit.

Similar idea could be transferred to the secondary side. The counterparts of the half bridge and full bridge inverter are the rectifiers including the center tapped, full bridge, voltage doubler and voltage quadrupler. By switching the operation modes between them, one can achieve wide output voltage range for LLC converters [48], [49].

Another way is inspired by the LLC design requirement. From LLC converter optimal operation point of view, a large magnetizing inductor L_m should be used at high input voltage, to limit the circulating current. While a small L_m should be used at low input voltage, to achieve high voltage gain. This contradictory magnetizing inductor design is the limitation for LLC converter, which also implies the desired feature – an adjustable L_m changing with the input voltage. LCLC converter can meet this requirement if designed properly [50]. The topology is shown as in Fig. 14. On the parallel branch of the resonant tank, an inductor and a capacitor is used to replace the conventional magnetizing inductor. The inductor L_p must be external. Thus, it is more suitable for high power applications, in which integrated magnetics suffer from high conduction loss and limited window size.

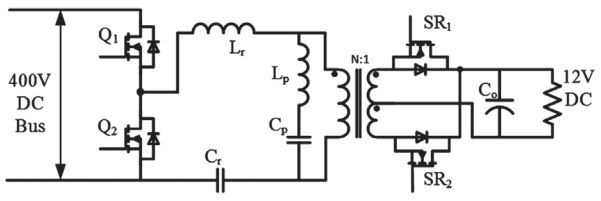

Fig. 14. LCLC converter with wide input voltage range.

By designing the total impedance of L_p and C_p as inductive, the LCLC converter can always be equivalent to an LLC converter for different input voltage and switching frequency. The voltage gain of LCLC converter and its equivalent LLC converter at different operation points are shown in Fig. 15.

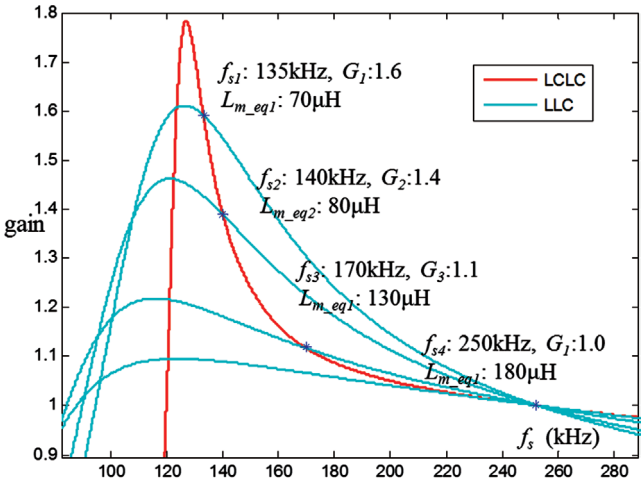

Fig. 15. Voltage gain of LCLC converter and its equivalent LLC converters .

From the bench test, LCLC converter achieves 1-2% improvements of efficiency for different loads, as compared to an LLC converter with same 250 V-400 V voltage range. If compared to an LLC converter that is optimized for 400 V, the efficiency has a 0.1-0.2% sacrifice in exchange for the much wider voltage operation range.

V. Conclusion

Three applications with significant industry value are discussed in the paper. The existing technologies are introduced and categorized. The popular technologies are explained in terms of the principle, the deriving process, and the advantages.

More in details, for high current application, SCC LLC and common inductor LLC converter are discussed and compared with existing multiphase LLC converters from the point view of current sharing performance, complexity and cost, interleaving ability, and phase shedding. The zero-crossing-noise filter is also introduced as an enabler of accurate SR driving for high current applications.

For fast dynamic application, cycle-by-cycle average current sensing reduces the complexity to the minimum, and enables both current mode control without delay and accurate current sharing for multiphase LLC converter. With bang bang charge control, the input power is controlled by turning off the primary switches at specified capacitor voltage, and achieve up to 1/5 bandwidth of switching frequency.

Both holdup operation and wide voltage range applications requires high voltage gain. The subtle difference is explained and exampled. Existing methods are summarized and categorized by intrinsic principle for both applications. New topologies including sLLC for holdup operation and LCLC for wide input voltage range application are explained in details.

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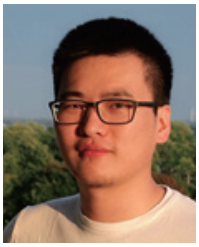

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Sneak Circuits in Power Converters: Concept, Principle and Application

Bo Zhang and Dongyuan Qiu

***Abstract*—"Sneak Circuit" is defined as the unexpected path or operational status in an electric or electronic circuit due to the limitation or oversight in design by human. The sneak circuit can be triggered to operate under certain conditions, which results in an unwanted or unintended action. As power converter is an artificially designed system, it is undoubted that sneak circuits exist in power converters, while sneak circuit phenomena have been proved in some typical power converters. In order to improve safety and reliability of a power electronic system, it is necessary to understand thoroughly the sneak circuit in power converters under all possible practical conditions. Thus, this paper aims at providing a brief review of sneak circuits in power converters, and summarizes the sneak circuit analysis (SCA) methods based on the graph theory. Finally, some applications on power converters by making use of the SCA principle of sneak circuit analysis are included.**

***Index Terms*—Sneak circuit, power converter, graph theory, sneak circuit analysis (SCA).**

I. Introduction

POWER converter is an important part in most of electrical and electromechanical systems, because it can realize energy transfer between different electrical forms and meet the requirement of high efficiency [1], [2]. As the need of power converters grow rapidly in many areas, the reliability of power converter should be concerned according to its fundamental place in energy conversion and management.

Normally, preventing part failure or component failure is an effective method to improve system reliability [3]. However, not all systems failures are caused by component failure. In some situations, no part has failed, yet the system performs improperly or initiates an undesired function. A significant cause of such unintended events is named as "sneak circuit", which is the unexpected electrical path or logic flow that can produce an undesired result under certain conditions [4]. Opposing to the component failure, sneak circuit happens without any physical failure in the system, an undesired effect is obtained although all parts are working within design specifications.

It has been concluded that the main factor causing sneak circuit is lacking of a complete view of the detailed interrelationship between components and functions in a system [5]. Similar to the other systems, it has been proven that sneak circuits exist in the power converter, which may affect the performance of the whole system [6]-[8]. Therefore, the sneak circuit situations in power converters should be investigated and identified, which will have a positive impact on the reliability of power electronic system.

In order to identify sneak circuits systematically, sneak circuit analysis (SCA) is a safety analytical technique which was developed firstly by Boeing in the late 1960s [9]. However, different from other electric or electronic systems, power converter is a typical switched-mode system which operates based on the alternate switching of the semiconductor switches. Obviously, sneak circuit conditions of power converters will relate not only to the variation of parameters, such as the step change of input voltage or load resistance, but also to the control schemes applied for the power switches. Thus, the conventional SCA methods are not suitable for analyzing the sneak circuits in power converters, SCA for power converter should consider both circuit paths and control schemes.

The remainder of this paper is organized in the following sections. Section II gives a comprehensive description of sneak circuit in power converter by using a common Boost DC-DC converter as an example. Section III reviews several available SCA methods for power converters. And then the applications of SCA methods on sneak circuit elimination, topology design and performance improvement are provided in Section IV. Finally, some concluding remarks in the sneak circuit of power converter are drawn in Section V.

II. Concept of Sneak Circuit

Sneak circuit is a designed-in current path or signal flow within a system which inhibits wanted functions or causes unwanted functions to occur without a component having failed. Sneak circuits are not the result of component failures, electrostatic, electromagnetic or leakage factors, marginal parametric factors or slightly out-of-tolerance conditions, they are present but not always active conditions inadvertently designed into the system, coded into the software program, or triggered by human error [5]. Consequently, the sneak circuit phenomena are controllable or reversible if the condition of sneak circuit occurrence are known.

A. Sneak circuit definition in power converter

Power converter is usually composed of power diodes, controllable power switches, inductors, capacitors and resistors. As inductor and capacitor belong to the energy storage components, some unintended electrical current paths can

Manuscript received March 27, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00008

be established by inductor and/or capacitor independently. If this kind of current path affects the performance of power converter, they can be considered as the sneak circuit path in power converter, according to the definition of sneak circuit.

In fact, sneak circuit in power converters is not strange. For example, the basic Boost converter shown in Fig. 1(a) has two distinct operating modes based on the status of inductor current, one is continuous conduction mode (CCM) and the other is discontinuous conduction mode (DCM). Generally, Boost converter is designed to operate in CCM or DCM to meet certain control functions by selecting the converter parameters (for example the inductance) in advance. However, CCM will switch to DCM and vice versa, when some operating conditions change, such as input voltage, load or duty ratio. Comparing Fig. 1(b) with Fig. 1(c), if CCM is regarded as the normal operation mode, then the current path only consisting of the output capacitor and the load when both D and S are OFF in DCM can be considered as the sneak circuit path. It is well known that the voltage gain in DCM is different from that in CCM, thus DCM can be considered as the sneak circuit mode.

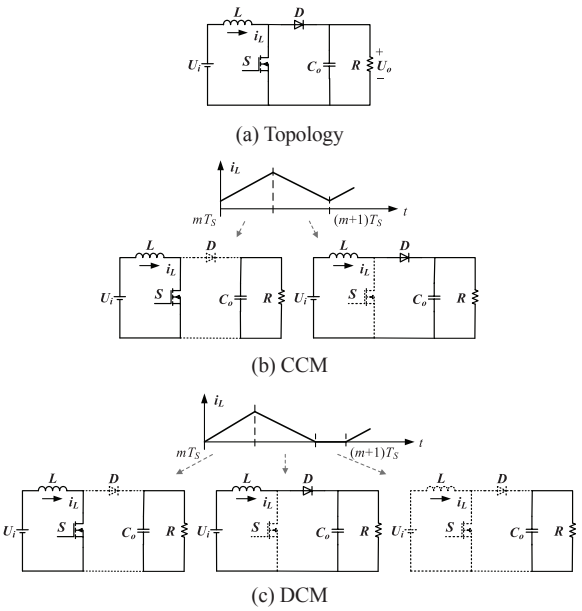


Fig. 1. Boost converter and its operating modes.

B. Sneak circuit considering parasitic parameter

The components in power converter are always considered as the ideal ones in order to simplify the analysis, however, all components in power converter have parasitic parameters in fact. It is obviously that the current flows in power converter will be more complicated when all parasitic components are considered, and the probability of overlooking potentially undesirable conditions will increase proportionately as a result.

Take Boost converter as the example again, if Power MOSFET is selected as the power switch *S*, the equivalent circuit of Boost converter is shown in Fig. 2(a) when some critical parasitic elements are taken into account [10]. The actual model of Power MOSFET is composed of a N-channel MOSFET, a gate-drain capacitor C_{gd}, a gate-source capacitor C_{gs}, a drain-source capacitor C_{ds}, and a body diode D_S. And power diode D is represented by a freewheel diode in paralleled with a junction capacitor C_D.

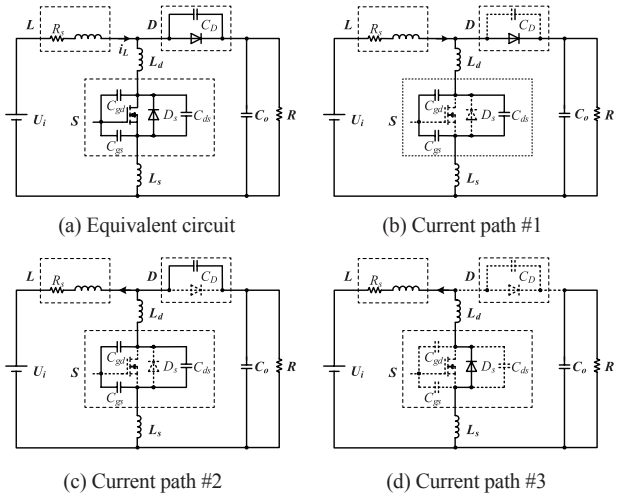
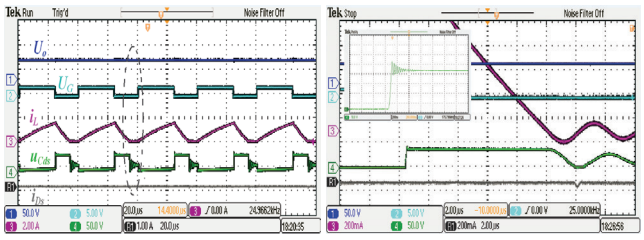
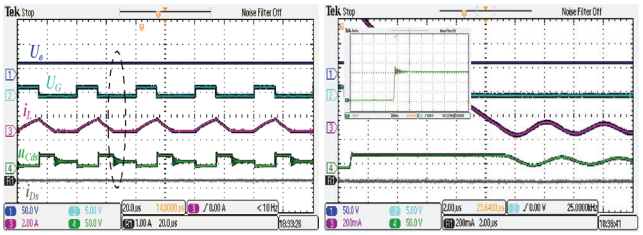


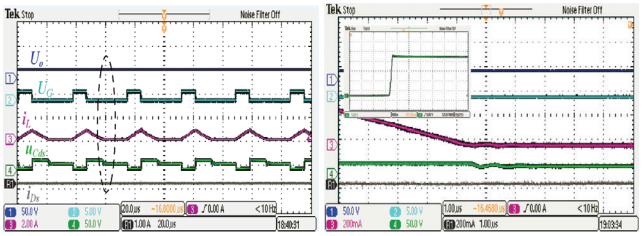
Fig. 2. Boost converter with parasitic parameters.

When Boost converter operates in DCM, except for the conventional current paths in Fig.1 (c), it is found that there exist another three current paths caused by the parasitic components, which are illustrated in Fig.2 (b) to Fig.2 (d), respectively. The experimental waveforms of a Boost prototype shown in Fig. 3 are provided to prove the existence of the above three current paths [10]. In Case I or Fig. 3(a), current paths #1, #2 and #3 appear, because the voltage on the drain-source capacitor resonates, the inductor current i_L is negative and the body diode current i_{Ds} is not equal to zero during the switch is turned off. However, i_{Ds} keeps at zero in Fig. 3(b), which means that current path #3 disappears in Case II. By changing some operating conditions of the prototype, the ideal DCM waveform similar to Fig. 1(c) is obtained in Fig. 3(c), it can be concluded that current paths #1, #2 and #3 have not been established in Case III. Therefore, the appearance of these three paths are controllable, there will be currents flowing through these paths during the operating process of Boost converter if certain operating conditions are satisfied. In addition, the influence of different cases as well as each parasitic component on the voltage gain have been summarized in literature [10]. It is demon-





(b) Case II



(c) Case III

Fig. 3. Experimental waveforms of Boost converter under different conditions.

strated that current paths caused by parasitic parameters in power converter are coincident with the definition of sneak circuit.

III. Principle of Sneak Circuit Analysis

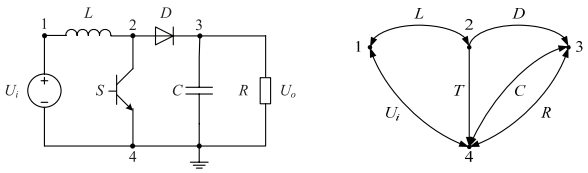
As sneak circuit have been found and proven in a variety of power electronic converters [11], it is necessary to understand thoroughly the sneak circuits in power converter under all possible practical conditions. According to the definition of sneak circuit in power converter, sneak circuit phenomenon belongs to one of the operating modes of power converter. It is known that the operating mode of power converters consists of several operating stages in one switching period, different operating stages are switched in a fixed order according to the applied control strategy. Since each operating stage refers to a sub-circuit or equivalent circuit, there is current flowing through the sneak circuit path when sneak circuit phenomenon appears. Therefore, the sneak circuit analysis of power converter should have two functions: one is sneak circuit path analysis, which is used to identify the sneak circuits paths existed in the converter; the other is sneak circuit mode analysis, which can predict the sneak circuit phenomena.

A. Sneak Circuit Path Analysis

The precondition to find out the sneak circuit path is to obtain all possible circuit paths or current loops existed in the power converter. If a current path is neither an invalid current path nor a normal current path, then it belongs to the sneak circuit one. Obviously, searching for circuit paths in power converter is the first step in sneak circuit path analysis. If power converter is considered as a graph, some concepts in graph theory, such as adjacency matrix, connection matrix, and mesh, will be useful for path or loop searching [12]-[14].

When a directed graph $G=(V, E)$ with two finite sets V and E is used to describe the power converter, the element of vertex set V represents the intersection of components in the power converter, which is named by number; the element of edge set E is the branch in the converter, which is named by the component symbol of the branch; and the direction of the edge is determined by the current direction of the component on the edge. The edge whose current can flow in bi-direction is indicated by a bidirectional or two-way arrow, while the edge with diode or the switching component without inverse conduction property is indicated by a single-way arrow, which points to the possible flowing direction of the component current.

Boost converter is taken as an example again to explain how to establish the directed graph of power converter. As shown in Fig. 4(a), the branch in the converter is defined as edge, the intersection of the branches is defined as vertex and there are 4 vertices in Boost converter. Considering the symbol of the component on the branch as the edge name, the component current direction as the edge direction, the directed graph of Boost converter can be obtained in Fig. 4(b).



(a) Vertex definition (b) Directed graph

Fig. 4. Boost converter and its directed graph.

According to the definition of adjacency matrix [12], the adjacency matrix of Boost converter is

$$\mathbf{A}=\begin{bmatrix}0&1&0&1\\1&0&1&1\\0&0&0&1\\1&0&1&0\end{bmatrix} \tag{1}$$

Based on (1), the vertex sequence 1-2-3-4 is on behalf of one current path in the Boost converter, because a_{12}=1, a_{23}=1, a_{34}=1, a_{41}=1. But the vertex sequence 4-3-2-1 is an invalid current path, because a_{32}=0. Therefore, all the current paths in power converter can be described by a group of vertex sequences and obtained by some searching algorithms [11].

If the matrix element of the connection matrix is defined by

$$c_{ij}=\begin{cases}1, \text{for } i=j\\ 0, \text{for } i\neq j \text{ and no current path from } i \text{ to } j\\ \text{Element symbol, for } i\neq j\end{cases} \tag{2}$$

then the generalized connection matrix of Boost converter is

$$\mathbf{C}=\begin{bmatrix} 1 & L & 0 & U_i \\ L & 1 & D & S \\ 0 & 0 & 1 & R+C_o \\ U_i & 0 & R+C_o & 1 \end{bmatrix} \tag{3}$$

As the current path must be a loop in the circuit, all possible current loops in power converter can be found by calculating the determinant of the generalized connection matrix **C** [15], [16]. Thus, base on (3), the calculation result of loop is

$$f_{loop}=\left|\det \mathbf{C}\right| \Rightarrow RC_o+U_iLDR+U_iLDC_o+U_iLS \tag{4}$$

From (4), it is concluded that there are 4 current loops in Boost converter, which are *R*-C_o, U_i-*L*-*D*-*R*, U_i-*L*-*D*-C_o and U_i-*L*-*S*, respectively.

Since an operating stage of power converter is normally consisted of more than one circuit path or current loop, circuit paths or current loops should be combined to a sub-circuit which refers to an operating stage. By defining mesh as the loop that does not contain internal loop with edge [14], mesh combination algorithm can be used to find out all of the possible sub-circuits in power converter.

According to the mesh definition, Boost converter in Fig. 1(a) is made up of 3 meshes, which are expressed by the following sets:

$$\begin{aligned} G_1&=\{U_i,L,S\} \\ G_2&=\{S,D,C_o\} \\ G_3&=\{C_o,R\} \end{aligned} \tag{5}$$

By applying AND ($\cup$) and RING SUM ($\oplus$) operations of graph, meshes can be composed into connected pieces [14], for example,

$$\begin{aligned} G_1\cup G_3&=\{U_i,L,S,C_o,R\} \\ G_1\oplus G_3&=\{U_i,L,S,C_o,R\} \end{aligned} \tag{6}$$

$$G_1\cup G_2\oplus G_3=\{U_i,L,D,C_o,R\} \tag{7}$$

It can be found that G1($\cup$ or $\oplus$) G3, G1$\cup$G2$\oplus$G3 and G3 represent for three operating stages in DCM shown in Fig. 1 (c), respectively.

Thus, all possible circuit paths, circuit loops and sub-circuits in power converter can be obtained by the above methods, and they can be divided into groups according to the circuit principle and the operating principle of power converter:

1) The invalid path, loop or sub-circuit, which will not be allowed in the power converter. For example, both *S* and *D* are "ON" at the same time in Boost converter. After eliminating the invalid path, the rest of possible paths are the effective ones.
2) The desired path, loop or sub-circuit, which will show up as designed during normal operation of the converter.
3) The sneak circuit path, which is the effective circuit path different from any normal circuit path.

As a result, the sneak circuit path can be identified by comparing the effective circuit paths with the normal ones.

B. Sneak Circuit Mode Analysis

Even the sneak circuit paths have been obtained, the behavior of the converter when the sneak circuit paths appear during the operating process is still unknown, thus sneak circuit mode analysis should be carried out. It is known that the switching components in the power converter are turned on or off in a fixed order based on the control strategy, so the sub-circuits corresponding to different switching states will constitute the operating mode of power converter.

As shown in Fig. 5, there are two switching components in Cúk converter, one is the controllable switch *S* and the other is the uncontrollable diode *D*. If "1" indicates the state of the switching component when it is on, and "0" indicates off, then the available switching states for Cúk converter are expressed by SD=10, SD=01 and SD=00, while SD=11 is invalid. These three switching states can compose two switch control sequences, 10-01-10-01-… (Control sequence I) and 10-01-00-10-01-00-… (Control sequence II).

The equivalent circuits corresponding to switch states SD=10 and SD=01 are shown in Figs. 6(a) and (b), respectively. But both circuits in Figs. 6(c) and (d) refer to the same switch state SD=00. Thus, the operating mode under control sequence I is unique, and there are two operating modes under control sequence II. It is common to define the operating mode under control sequence I (i.e. CCM) as the normal operation mode of Cúk converter, while those under control sequence II should be considered as sneak operating modes, which are shown in Figs. 7(a) and (b).

In order to describe the sneak circuit phenomena of Cúk converter, the waveforms of inductor currents i_{L1} and i_{L2} are selected. It is noted that inductors L_1 and L_2 are connected in

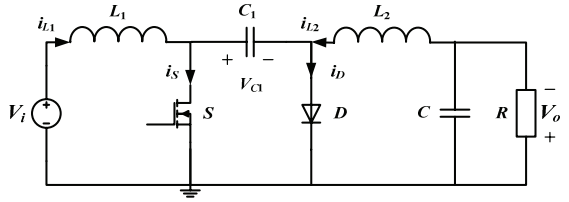


Fig. 5. Schematic of Cúk converter.

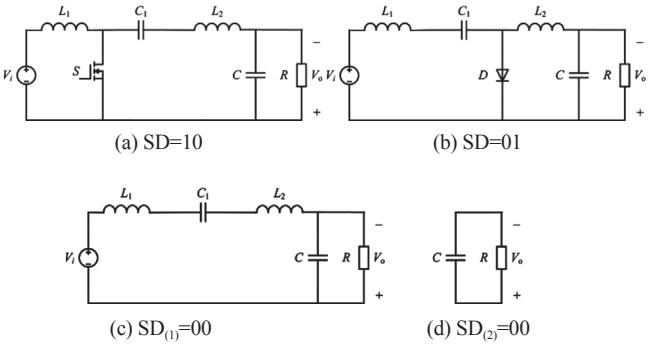
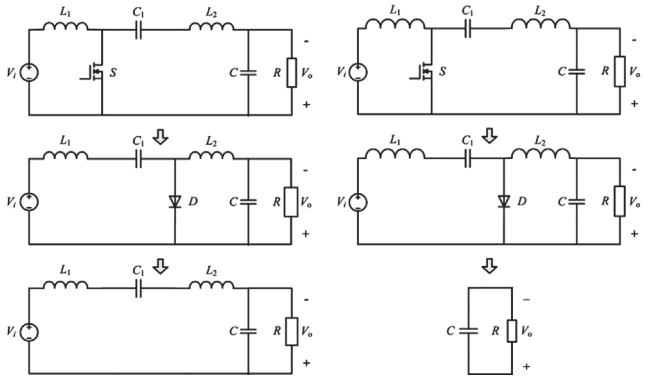


Fig. 6. Equivalent circuits of Cúk converter.

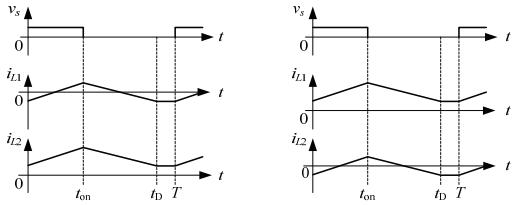


(a) Sneak operating mode 1 (b) Sneak operating mode 2

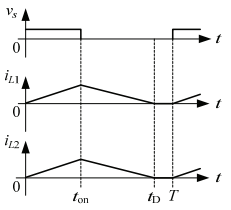
Fig. 7. Sneak operating modes of Cúk converter.

series in Fig. 6(c), then $i_{L1}+i_{L2}=0$ should be satisfied, and the inductor currents will have the following two forms: (i) $i_{L1}<0$ and $i_{L2}>0$; (ii) $i_{L1}>0$ and $i_{L2}<0$. When Cúk converter operates in Fig. 6(d), both of the inductor currents i_{L1} and i_{L2} are equal to zero, i.e. $i_{L1}=i_{L2}=0$. Therefore, based on the possible current forms of the equivalent circuits, the typical inductor waveforms corresponding to sneak operating modes can be predicted and shown in Fig. 8.

A Cúk prototype has been built to verify different kinds of phenomena [17]. By reducing the duty cycle d, the Cúk prototype will work in different operating modes, and the experimental waveforms of driving signal v_s, output voltage V_o, inductor currents i_{L1} and i_{L2} are shown in Fig. 9, which have good agreement with the predicted waveforms in Fig. 8.

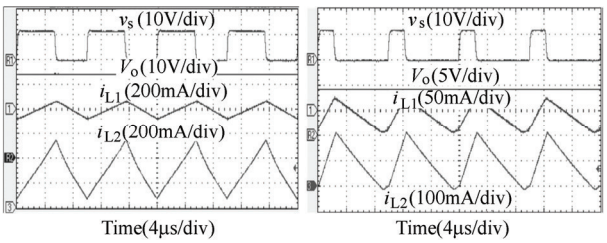


(a) Typical waveforms of sneak operating mode 1

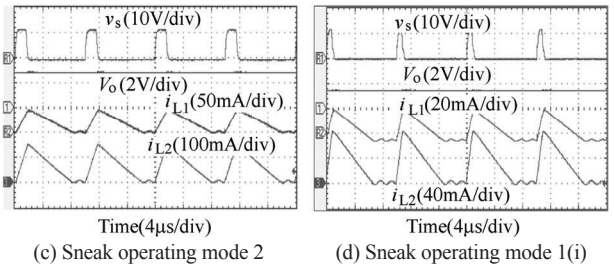


(b) Typical waveforms of sneak operating mode 2

Fig. 8. Sneak circuit phenomena of Cúk converter.



(a) Normal operating mode (or CCM) (b) Sneak operating mode 1(ii)



(c) Sneak operating mode 2 (d) Sneak operating mode 1(i)

Fig. 9. Experimental waveforms of different operating mode.

Therefore, the feasibility of the proposed sneak circuit mode analysis method has been verified.

IV. Application of Sneak Circuits

With the help of sneak circuit analysis method proposed in section III to power converter, the operating principle and the characteristics of power converter can be understood comprehensively, thus SCA for power converter is useful to modify the topology and improve the performance of the power converter.

A. Sneak Circuit Elimination

Based on the definition of sneak circuit, the sneak circuit of power converter is a path hided in the converter, which would appear when specific parameter condition is satisfied. As a result, the operating stages increase and the energy balance under normal operating mode is destroyed, which will lead to some changes of converter characteristics and the desired performance of the converter cannot be achieved. Thus the sneak circuits should be eliminated in the power converter.

Apparently, the emergence of sneak circuits should satisfy two conditions: firstly, there must be some sneak circuit paths existed in the power converter; secondly, sneak circuits will appear if the converter parameters are not designed appropriately or the converter operating conditions are out of the normal range. Therefore, in order to eliminate sneak circuits in power converters, there are two methods:

1) Proper parameter design, which is suitable for the converter which has specific sneak circuit condition, because the emergence of sneak circuit can be avoided through reasonable parameter design.
2) Topology modification, which can cut off the sneak circuit paths by changing the converter topology based on the characteristic of sneak circuit path.

The three-phase Z-source inverter [18] shown in Fig. 10 is taken as an example to demonstrate how to eliminate the sneak circuit by parameter design and topology modification. Normally, the diode D conducts when the three-phase inverter is at the active or traditional zero state, D is blocked when the inverter operates at the shoot-through state. However, when the diode current is discontinuous during the period of active states, the input dc voltage of the inverter bridge drops, which will affect the quality of the output ac voltage seriously. It has been proven that this sneak circuit phenom-

ena will occur if a small inductance or low load power factor is selected [19].

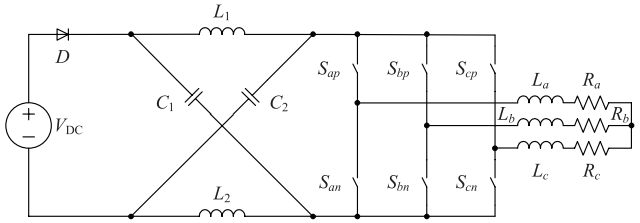


Fig. 10. The classic three phase Z-source inverter.

As the Z-source inverter has a specific sneak circuit condition, if the operating conditions of Z-source inverter are set to satisfy with the following equation, the sneak circuit phenomenon of Z-source inverter will not appear.

$$\frac{3}{2}MB\cos\phi - 1 \geq 0 \tag{8}$$

where M is modulation ratio, B is step-up factor and $\cos\phi$ is the load power factor.

On the other hand, the sneak circuit phenomenon will appear in the Z-source inverter when the link between the DC voltage source V_{DC} and impedance network is open during the inverter's active state. Therefore, if there is a circuit path that connects V_{DC} with Z-network at any state, the sneak circuit phenomenon will disappear. Substituting diode D by a fully controlled power switch S_m which has the reverse conducting property (i.e. Power MOSFET), the improved Z-source inverter is illustrated in Fig. 11.

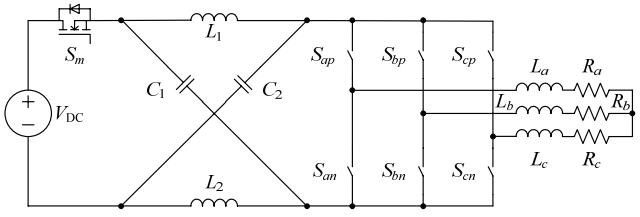


Fig. 11. The improved Z-source inverter.

As the input current or the switch current can flow bi-directionally, the switch can provide a backward path for the current by its control signal or anti-parallel diode even when the input current decreases to zero and becomes reversed. Therefore, the sneak circuit phenomenon of the classic Z-source inverter will not happen forever.

B. Performance Improvement

In fact, as the existed circuit paths in power converter, sneak circuits may have positive effect in power converter if it can be made good use of. The synchronous Buck converter can be used as an example to discuss how to improve the converter performance without adding any component but by making use of the sneak circuit.

The synchronous Buck converter can be obtained by replacing the diode in Buck converter with a controllable power switch. As shown in Fig. 12, S_1 is the main switch and S_2 is the synchronous switch. In general, the conduction of S_1 and S_2 are complementary, and certain dead time is inserted between the two driving signals to prevent simultaneous conduction of the two switches.

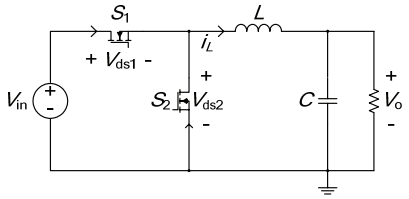
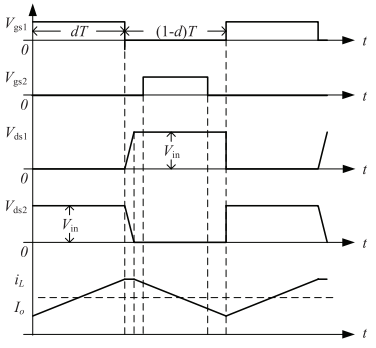
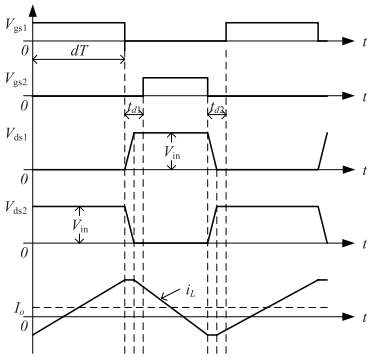


Fig. 12. Synchronous Buck converter.

When the inductor current is continuous and positive, typical waveforms of the synchronous Buck converter in normal operating mode are shown in Fig. 13(a). It is obvious that the synchronous switch S_2 can achieve ZVS before it is switched on. However, the main switch S_1 is still operating in hard-switching state. As the switch such as Power MOSFET can flow through bidirectional current, the body diode of S_1 will conduct when the inductor current i_L drops to zero and becomes negative during the on-state of S_2, then the zero-voltage turn-on condition of the main switch S_1 can be created. The typical waveforms that both the main switch and the synchronous switch can achieve ZVS are shown in Fig. 13(b).



(a) Normal waveforms



(b) Sneak circuit mode

Fig. 13. Typical waveforms of Synchronous Buck converter under different modes.

It has been proven that this situation only happen when the inductance of the synchronous Buck converter is designed relatively small [20], thus Fig. 13(b) can be regarded as the sneak circuit phenomenon of the synchronous Buck converter according to the definition of sneak circuit. Obviously, it is a significant reward to achieve ZVS by using the sneak circuit paths that exist in synchronous DC-DC converter.

C. Topology Reconstruction

Topology is one of the key techniques in power electronics, because it determines the basic performance and operating characteristics of power converter. A large number of power converter topologies have been proposed, such as Cúk converter [21], resonant converter [22], soft-switching converter [23], multilevel converter [24], modular multilevel converter (MMC) [25], etc., which have greatly improved the level and quality of electric energy transformation.

However, it is found that the invention of the novel power converter largely depends on the inventors' academic attainments and practical experiences. Furthermore, many typical power converters also need further improvement and optimization in practical application and the process of topology reconstruction is still based on the "try and test" method. As the sneak circuit analysis method can provide a thoroughly understanding of power converter, it is possible to be applied in reconstructing the topology of power converter.

For example, the original Boost ZCT PWM converter and an improved Boost ZCT PWM converter are shown in Fig. 14 and Fig. 15, respectively.

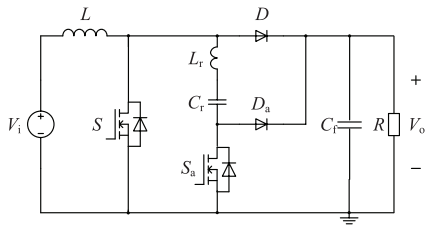


Fig. 14. The original Boost ZCT PWM converter.

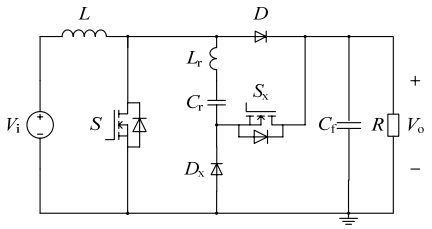


Fig. 15. An improved Boost ZCT PWM converter.

Comparing Fig. 15 with Fig. 14, diode D_x substitutes for the original auxiliary switch S_a and the conducting direction of D_x is consistent with the anti-parallel diode of S_a; switch S_x substitutes for the original auxiliary diode D_a and the anti-parallel diode of S_x keeps the same conducting direction of D_a. Therefore, the switching states of both converters are the same, the original functions of Boost ZCT PWM converter can be kept in the modified one. Furthermore, the modified Boost ZCT PWM converter is proven to have other advantages, such as ZCS of the main switch as well as auxiliary switch can be realized, the peak current of auxiliary switch is relatively small and the switch time of auxiliary switch is easy to control [26]. Therefore, topology reconstruction method by making use of the sneak circuit path analysis method is feasible, and the good performance of the original converter can be kept.

V. Conclusions

In this paper, the work on sneak circuits and related sneak circuit analysis methods for power converters have been reviewed, how to eliminate and make use of sneak circuit have been proposed as well. The research on sneak circuit in power converters offers guidelines in the design of power electronic system and enable early detection of potential problems, which will contribute to the reliability of power electronic system.

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Revisiting Stability Criteria for DC Power Distribution Systems Based on Power Balance

Zhicong Huang, Siu-Chung Wong, and Chi K. Tse

***Abstract*—Single-input-multiple-load converter systems sharing a common input DC voltage bus is becoming popular in DC power distribution. Due to the convenience of using conventional voltage-source systems for connecting a common bus voltage with multiple downstream loads, the same configuration is often adopted for current-source systems, where design optimization can be achieved without an intermediate (bus) voltage regulator. However, the stability of such cascaded current-source systems is still relatively unexplored or incomplete, though the associated basic circuit theory has been well established. In this paper, steady-state operating points are obtained by applying power balance between the current-source output converter and the downstream converters. The incremental change of the input power versus the input impedance of the downstream converters is derived. The stability of such current-source converter systems is re-visited using an impedance-based approach. A general set of impedance-based stability criteria is developed and experimentally verified by a DC bus system consisting of a current source output converter and two PWM power converters.**

***Index Terms*—DC bus system, DC current source converter, stability criterion.**

I. Introduction

IMPEDANCE-BASED stability criterion [1] has been applied for the voltage-source converter system consisting a voltage-source converter and a load converter connected in cascade, with a regulated voltage being the interface between the source and load converters. Based on a small-signal model, the Middlebrook stability criterion states that the system is stable if the following conditions are satisfied:

V1 The source converter having an output voltage V_o and output impedance Z_s is stable under no load condition.

V2 The load converter having an input impedance Z_l is stable when connected to an ideal voltage source V_o, and

V3 (a) aggressively, $T_v = Z_s / Z_l$ satisfies the Nyquist stability criterion, or

V3 (b) conservatively, $|T_v| \ll 1$.

Cascaded-converter systems with an inverter of highimpedance current source output connected to the lowimpedance input of a grid voltage have been studied by Sun [2] who identified the systems as current-source systems and presented a stability criterion as a dual to that given in [1]. Specifically, this current-source system is stable if the following conditions are satisffied:

C1 The source converter having an output current I_o and impedance Z_p is stable under no load condition.

C2 The load converter having an input impedance Z_l is stable when connected to an ideal current source I_o, and

C3 (a) aggressively, $T_c = Z_l / Z_p$ satisfies the Nyquist stability criterion, or

C3 (b) conservatively, $|T_c| \ll 1$.

The above stability criteria have been applied to DC distributed power systems with multiple sources and loads where the numbers of sources and loads are changing dynamically [3]. Apart from verifying condition V1 or V2 as appropriate for each converter, the system's minor loop gain T_v (referred to in V3) has been extended to include every impedance (or admittance) of the system given by

$$T_v = \frac{\text{parallel of all } m \text{ source impedances}}{\text{parallel of all } n \text{ load impedances}} \quad (1)$$

$$= \frac{\sum_{j=1}^{n} \frac{1}{Z_{lj}}}{\sum_{j=1}^{m} \frac{1}{Z_{sj}}}. \quad (2)$$

Likewise, similar modification has been proposed for the current-source system. However, only the usual voltage-source systems are studied in detail [3] due to the fact that such voltage-source systems, having a dominating regulated bus voltage, are the only systems considered in most DC distribution systems.

To see the potential of applications of current-source systems, we consider wireless power transfer systems here. Wireless power transfer systems are often designed with an inductive power transfer (IPT) converter cascaded with a downstream pulse-width modulation (PWM) converter to achieve a high overall system efficiency under line or load variation [4]-[8]. The series-series compensated IPT (SSIPT) converters [4]-[7] are among the most power efficient IPT converters [9], [10]. Operating at its power efficient point, the SSIPT converter can provide a constant output current which is independent of load variations [9], [10]. In this current-source system, no *voltage regulation* is needed at the interface of the cascaded power converters. Therefore, an equivalent source converter of the system has high output impedance which makes it difficult to meet the Middlebrook stability criterion applied to a voltage-source system that a stable cascaded converter should have its upstream power converter having a

Manuscript received March 16, 2017. This work was supported by Hong Kong Polytechnic University Grant G-YBKC.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00009

substantially lower output impedance compared to the input impedance of its downstream power converter [1], [11], [12]. However, the impedance-based stability criterion for current-source systems presented by [2], [3] is not general enough for applications with multiple loads, as shown in Fig. 1. In such a system, the converters can share either a common voltage bus or a common current loop. Additionally, as will be shown in Section III, the definition of either a voltage-source system or a current-source system is still unclear for the configurations shown in Figs. 1(b) and (c), making direct application of the Middlebrook stability criterion and its dual rather difficult.

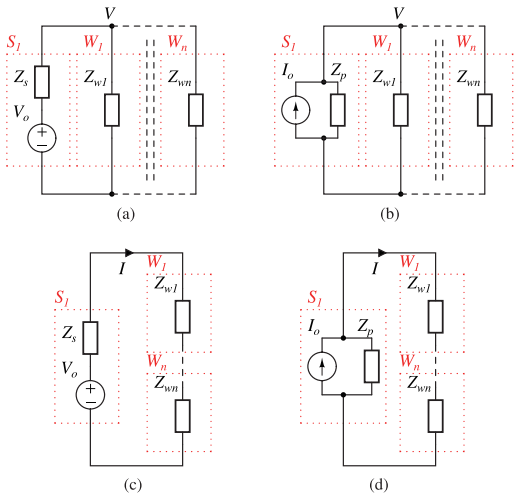


Fig. 1. Impedance-based models of a source converter S_1 and n load converters $W_1,\cdots,W_n$. Components inside the dotted line blocks are the small-signal-equivalent circuits of the converters. (a) Voltage-source converter S_1 sharing a common voltage with n load converters. (b) Current-source converter S_1 sharing a common voltage with n load converters. (c) Voltage-source converter S_1 sharing a common current with n load converters. (d) Current-source converter S_1 sharing a common current with n load converters.

In this paper, we analyze the general cascaded converter system by considering an equivalent model as seen by one of the DC-DC converters and apply power balance to gain insights into the difference between a voltage-source system and a current-source system. A general set of impedance-based criteria of stability will be developed as a generalization of the criteria presented in [2], [3]. The set of stability criteria developed from this simple model will be verified experimentally by a cascaded SSIPT-PWM converter system. A stable prototype of independently controlled IPT and PWM converters will be demonstrated.

To differentiate a voltage-source system from a current-source system, we can consider the DC steady-state model of the system by referring to Fig. 1 with all small-signal variables being replaced by their DC counterparts. For brevity, we can start with $n = 1$, where Fig. 1(a) becomes identical to Fig. 1(c) and Fig. 1(b) becomes identical to Fig. 1(d). The DC operating circuit for $n = 1$ is shown in Fig. 2, where the source and load share the same voltage bus V and current loop I.

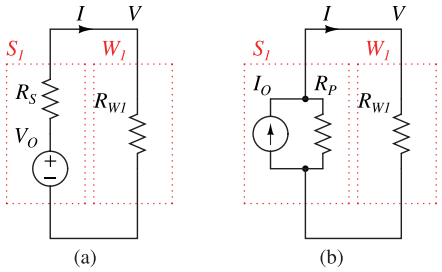


Fig. 2. DC operation models of a source converter S_1 and a load converter L_1. Components inside the dotted line blocks are the DC equivalent circuit of the converters. (a) Voltage source converter S_1 sharing a common voltage with a load converter. (b) Current-source converter S_1 sharing a common current with a load converter.

II. Steady-State Operating Points from the Viewpoint of Power Balance

Fig. 1 shows equivalent small-signal models of closed-loop converters. We assume that the converters are stable, operating safely within their voltage, current and power ratings, and can be perfectly controlled to their DC operating points with a finite bandwidth f_{BW}. In this sense, the voltage-source converter S_1 has been stably *biased* to its DC operating point as an ideal voltage source V_o with a small source resistance R_S, which represents the resistance of interconnection as well as the intentional output resistance from control algorithms such as the droop controller. The DC operating circuit shares the same circuit structure as shown in Fig. 1, with the corresponding DC variables being represented with uppercase letters and subscripts as appropriate. Likewise, we have an ideal DC current source I_o and its large parallel output resistance R_P for a current-source converter.

The n-load converters are normally regulated with a constant output voltage or current. When such near lossless converters are connected with resistive loads, their inputs will behave as a near perfect constant power sink $P_{Wi} = V_{Wi} I_{Wi}$, where $i = 1, \cdots, n$. Obviously, the same P_{Wi} can be biased at different points on a constant power curve, such as points A, B or C, as shown in Fig. 3. It should be noted that point A has a DC resistance of $R_A = \dfrac{V_A}{I_A}$ while its incremental resistance on the constant power curve is $-R_A$, which should equal Z_{wi} within f_{BW}. Obviously, to meet the output power requirement of P_{Wi}, the load converter W_i can be biased anywhere on the power curve. The choice of biasing at a point on the power curve will be decided by the practical requirements of meeting the voltage and current ratings by designing a suitable R_{Wi} and the regulation bandwidth dictates the associated $Z_{wi}(f) = -R_{Wi}$ with $f < f_{BW}$.

With reference to Fig. 2(a), the power output from S_1 should be identical to the power input to W_1. The power $P_1 = P_{W1}$ feeding to $R_L = R_{W1}$ can be plotted as shown in Fig. 4, which gives the expected maximum power transfer when R_L is equal to R_S. Moreover, an intended input power P_1 can be biased at two load resistances R_{Lx} and R_{Ly} such that $R_{Lx} < R_S$

$< R_{Ly}$. For a native source resistance R_S, operating at R_{Ly} will be more efficient than that at R_{Lx}. However, if R_S is a virtual equivalent resistance as a result of application of some control algorithms which are common in some AC or DC voltage bus systems [16], there would not be much difference in efficiency between the operation points R_{Lx} and R_{Ly}. It can be observed that a small increment of R_L at R_{Lx} acquires a higher P_1, while a small increment of R_L at R_{Ly} corresponds to a lower P_1. This gives an intuitive explanation on the requirement that the load R_{Ly} is stable when it is connected to an ideal voltage source as the two systems give near identical $\frac{\delta P_1}{\delta R_L}$, especially when $R_L \gg R_S$. It can be observed in Fig. 4 that the load converter W_1 operating with R_{Ly}, i.e., $R_L > R_S$, will become unstable when it is operating near R_S and even worse for $R_L \le R_S$ as $\frac{\delta P_1}{\delta R_L}$ will deviate significantly from that operating with R_{Ly} [17]. It is obvious that converter W_1 switching operating points from R_{Ly} to R_{Lx} should have its feedback circuit redesigned.

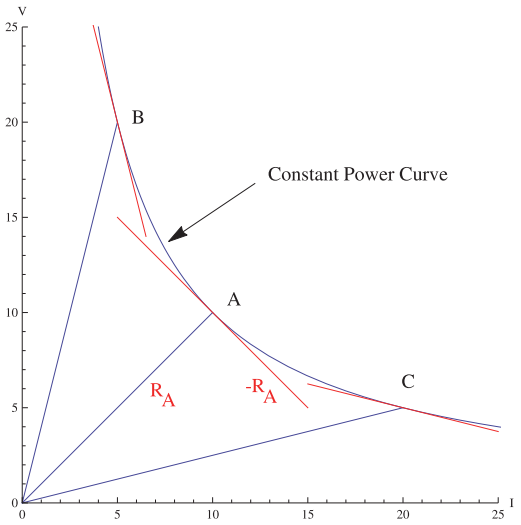


Fig. 3. Constant power curve with biasing points A, B and C.

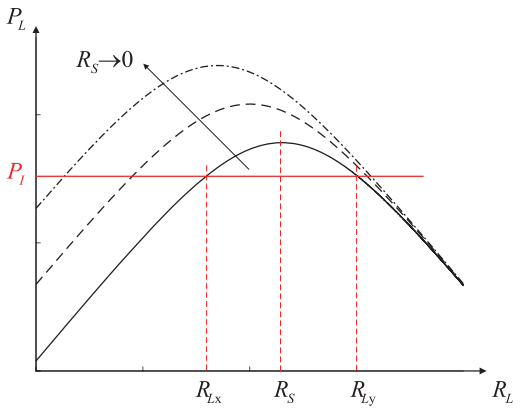


Fig. 4. Power transfer characteristic of a voltage-source system.

Likewise, with reference to Fig. 2(b), a current-source system has a power transfer characteristic as shown in Fig. 5. It is similar to Fig. 4 except that the current-source system is normally operating at R_{Lx} while for a voltage-source system, it is normally operating at R_{Ly}. Based on our previous analysis on voltage-source systems, we can obtain a corresponding set of results using the *duality principle*. Specifically, for a voltage-source system, $\frac{\delta P_1}{\delta R_L}$ at R_{Lx} is proportional to R_{Lx}, while for a current source system $\frac{\delta P_1}{\delta R_L}$ at R_{Ly}, it is inversely proportional to R_{Ly}. This again gives an intuitive explanation for the requirement that the load R_{Lx} is stable when it is connected to an ideal current source as the two systems give near identical $\frac{\delta P_1}{\delta R_L}$, especially when $R_L \ll R_P$. Similarly, it can be observed from Fig. 5 that the load converter W_1 operating at R_{Lx}, i.e., $R_L < R_P$, will become unstable when it is operating near R_P and even worse for $R_L \ge R_P$. It is also obvious that converter W_1 switching operation points from R_{Lx} to R_{Ly} should have its feedback circuit redesigned.

It can be concluded from Figs. 4 and 5 that for the source-converter having output resistance R_O and the load converter having input resistance R_L, the system is considered as a voltage-source system if $R_L \gg R_O$, otherwise it must have $R_L \ll R_O$ and the system is regarded as a current-source system. Meanwhile, for $f < f_{BW}$, $R_L \gg R_O$ is equivalent to $|Z_l(f)| \gg |Z_o(f)|$ and $R_L \ll R_O$ is equivalent to $|Z_l(f)| \ll |Z_o(f)|$ that these two conditions are subsets of the conservative conditions V3(b) of the Middlebrook stability criterion and C3(b) of the dual of the Middlebrook stability criterion.

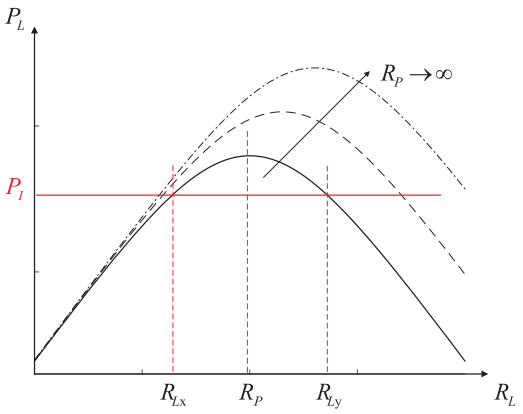


Fig. 5. Power transfer characteristic of a current-source system.

III. Current-Source or Voltage-Source Driven Subsystem of Single-Source Multi-Load Systems

In Section II, the single-source single-load system is readily distinguished as being a voltage-source system or a current-system by considering the relative magnitude of the source and load resistances at DC operation. In Fig. 6, two loads W_1 and W_2 are assumed independently controlled, or otherwise, they can be combined into a single load such that the system

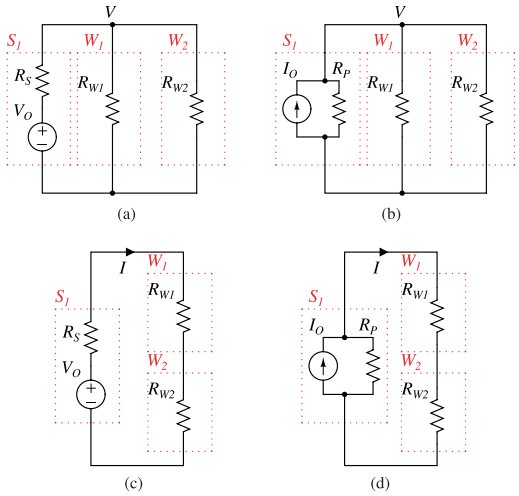


Fig. 6. DC circuit models of four possible configurations consisting of a source converter S_1 and two load converters W_1 and W_2.

is equivalent to a single-load system as shown in Fig. 2(a) or 2(b). To distinguish between a voltage-source system and a current-source system, we assess the converter subsystems individually. It can be readily observed from Fig. 6(a) that as long as

$$R_S \ll (R_{W1} || R_{W2}), \tag{3}$$

we have

$$(R_S || R_{W2}) \ll R_{W1}, \text{ and} \tag{4}$$

$$(R_S || R_{W1}) \ll R_{W2}. \tag{5}$$

For S_1, an equivalent resistance of $R_L = (R_{W1} || R_{W2})$ is being driven. Equation (3) identifies a voltagep-source system for S_1. Likewise, (4) and (5) identify a voltage-source system for W_1 and W_2. They can be designed stable by following the Middlebrook stability criterion [1] for their individual equivalent circuits. Similar arguments apply to Fig. 6(d) with respect to a current-source system with $R_P \gg (R_{W1} + R_{W2})$ and each load is designed to be stable when it is connected to an ideal current source. The results can be readily generalized to an n-load voltage-source system with $R_S \ll R_{W1} || R_{W2} || \cdots || R_{Wn}$ and an n-load current-source system with $R_P \gg (R_{W1} + R_{W2} + \cdots + R_{Wn})$. Common properties of systems represented by Fig. 6(a) and (d) are:

- there is a dominant source which regulates either the bus voltage or current of the system, and
- each load shares the s*ame* system defined by the source converter, i.e., a voltage- or a current-source system.

The stability of these well defined voltage-source or current-source systems can be easily assessed by applying either V1 to V3, or C1 to C3, to each of the source or load converters, or simply (2) or its dual [3].

The systems shown in Figs. 6(c) and (d) are less attractive than those shown in Figs. 6(a) and (b) which share a common voltage bus for easy connection or disconnection of loads. The identification and possible modification of the voltage- or current-source system shown in Fig. 6(b) will be developed as follows. For the current-driven system shown in Fig. 6(b), by applying Middlebrook stability criterion [1], [2] to each of the subsystem, the source S_1 is stable if C1 and the conservative condition C3(b) (solely needed for $f < f_{BW}$) are satisfied, which is equivalent to

$$R_P \gg (R_{W1} || R_{W2}), \tag{6}$$

the load W_1 should assume being driven by a current source. If so, we have

$$(R_P || R_{W2}) \gg R_{W1} \tag{7}$$

and the load W_2 should assume being driven by a current source. If so, we have

$$(R_P || R_{W1}) \gg R_{W2}, \tag{8}$$

It can be observed from Fig. 5 that (7) and (8) cannot be satisfied simultaneously if R_{W1} and R_{W2} are of similar order of magnitude and both W_1 and W_2 are stable when they are connected to an ideal current source. Without loss of generality, let us assume that

$$R_{W1} \ll R_{W2}, \tag{9}$$

such that (7) is satisfied, i.e., subsystem W_1 can be stable if it is stable when connected to an ideal current source. Now, for subsystem W_2, (8) can never be satisfied, i.e., subsystem W_2 cannot be stable when it is designed to be driven by a current source. Fortunately, from (9) we have

$$(R_P || R_{W1}) \ll R_{W2}, \tag{10}$$

which satisfies V2 of subsystem W_2, as given in Figs. 2(a) and 5, i.e., subsystem W_2 can be stable if it is stable when it is connected to an ideal *voltage* source [1], where the parallel connection of the current source and resistance $(R_P || R_{W1})$ are regarded as its Thevénin's voltage source equivalent. Since from the load's perspective, Thevénin's voltage source and Norton's current source are interchangeable, this result is important in several respects:

1) Load W_1 is driven by a *current source*, as shown in Fig. 5, with the source resistance $(R_P || R_{W2})$.
2) Load W_2 is driven by a *voltage source*, as shown in Fig. 4, with the source resistance $(R_P || R_{W1})$.
3) The systems in Fig. 4 and Fig. 5 are equivalent in terms of the load stability criteria.
4) For the single-source two-load system, the design of subsystem W_1 which is assumed stable when connected to an ideal current source is different from that of W_2 which is assumed stable when connected to an ideal voltage source.
5) For the stable single-source two-load system, the power

level of subsystem W_1 will be much higher than that of subsystem W_2 when they are controlled independently. To have the freedom of operating at any power level, the control of the subsystems must be well coordinated. In such a case, they reduce to a single-load system.

In summary, the lowest (highest) resistance of the system in Fig. 6(b) (Fig. 6(c)) acquires most of the power from the current (voltage) source and converts the current (voltage) source into an equivalent voltage (current) source for driving the other load.

The identification of current or voltage driven load subsystems can be readily generalized to an n-parallel-load current-source system with the condition that $R_P \gg (R_{W1}||\cdots||R_{Wn})$, $(R_P||R_{W2}||\cdots||R_{Wn}) \gg R_{W1}$ and $(R_P||R_{W1}) \ll R_{Wi}$ for $i = 2\cdots n$, where W_1 is stable when it is connected to an ideal current source, and W_i ($i = 2\cdots n$) is stable when connected to an ideal voltage source. Similarly, it can be generalized to an n-series-load voltage-source system with the condition that $R_S \ll (R_{W1}+\cdots+R_{Wn})$, $(R_S+R_{W2}+\cdots+R_{Wn}) \ll R_{W1}$ and $(R_S+R_{W1}) \gg R_{Wi}$ for $i = 2\cdots n$, where W_1 is stable when connected to an ideal voltage source, and W_i (i = $2\cdots n$) is stable when connected to an ideal current source.

The stability of each subsystem can thus be assessed by applying the source system identified. The system is stable when all subsystems satisfy the individually identified Middlebrook stability criterion or its dual.

Similarly, for the system shown in Fig. 7(b), W_1 should be designed for a current source system and satisfies C2 and C3 with

$$T_{cW_1} = \left(\sum_{j=1}^{n} \frac{1}{Z_{sj}}\right) Z_{w1}. \tag{11}$$

For each voltage-source converter S_k, conditions C1 and C3

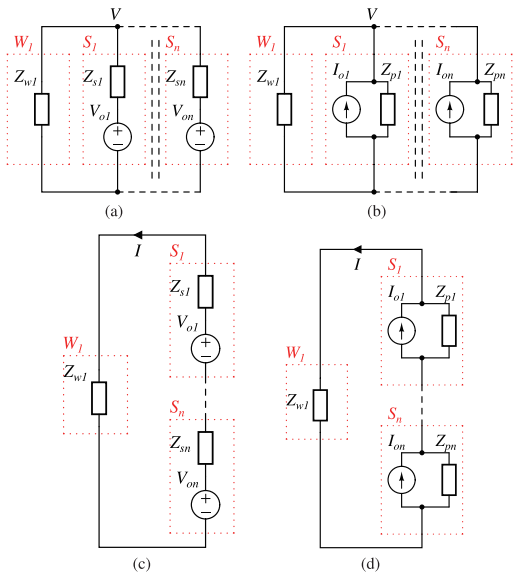


Fig. 7. Impedance-based models of a load converter W_1 and n source converters $S_1,\cdots, S_n$.

should be satisfied with

$$T_{cS_k} = Z_{sk}^{-1}\left(\frac{1}{Z_{l1}} + \sum_{j=1,j\neq k}^{n} \frac{1}{Z_{sj}}\right)^{-1}. \tag{12}$$

IV. Multi-Source Systems

The circuit for multi-source systems is represented in Fig. 7 by direct translation from Fig. 1, where the source S_1 is considered as load and the loads $W_1, \cdots, W_n$ are considered as sources $S_1, \cdots, S_n$. Since the circuits of Figs. 7(a) and (d) are dual, and so are the circuits of Figs. 7(b) and (c), it is suffice to consider the stability criteria for the circuits of Figs. 7(a) and (b).

In Fig. 7(a), if the voltage-source converters are active current-sharing converters [16], they are dependent converters and should be considered as a single voltage converter whose stability should be assessed according to the control algorithm used. The overall stable converter can be combined as a single voltage converter. If they are independent converters, the stability can be assessed using the approach described in Section III from the perspective of each converter and using the appropriate stability criterion of either V1 to V3, or C1 to C3. Specifically, L_1 should be designed for a voltage-source system, satisfying V2 and V3 with

$$T_{vW_1} = \frac{1}{\left(\sum_{j=1}^{n} \frac{1}{Z_{sj}}\right) Z_{w1}}. \tag{13}$$

For each voltage-source converter S_k, conditions V1 and V3 with

$$T_{vS_k} = Z_{sk}\left(\frac{1}{Z_{w1}} + \sum_{j=1,j\neq k}^{n} \frac{1}{Z_{sj}}\right). \tag{14}$$

should be satisfied. It should be noted that if the Nyquist stability criterion on $T_{vW}{}^{1}$ of (13) and that on $T_{vS}{}^{k}$ of (14) are satisfied, then the Nyquist stability criterion on T_v of (2) is satisfied. However, the converse may not be true.

It is also noted that for $n = 2$ and the system not being loaded by W_1, we have $T_{vS_1} = \frac{Z_{s1}}{Z_{s2}}$ and $T_{vS_2} = T_{vS_1}^{-1}$. Hence, the conservative condition V3(b) cannot be satisfied for each converter. Moreover, for multiple parallel voltage-source system, the output impedance, apart from being a source impedance, is also a load impedance of other participating voltage sources. In terms of stability, the output impedance of a voltage-source converter in a single source system can be designed with sufficient stability margin without any righthalf-plane zero. However, for a stable multiple voltage-source system, the output impedances should be designed without any right-half-plane zero.

V. Illustrative Example: Single-Current-Source Two-Load System

A. Inductive Power Transfer Converter

In this section, the single-source two-load system shown in Fig. 6(b) is selected for design and verification. As shown in the block diagram of Fig. 8, an IPT converter will be selected as S_1 which can operate with its most efficient configuration and has a current output. Two independently controlled DC-DC PWM converters W_1 and W_2 will be designed as load converters of the system. The source converter S_1 and load converters W_1 and W_2 have internal DC operation models shown in Fig. 6(b). S_1 has an equivalent resistance R_P which takes into account the losses due to the IPT transformer windings, magnetic cores and electronic devices. Such an IPT converter normally has a switching frequency current ripple filtering capacitor C_O which may pose constraints on the design of load converters W_1 and W_2. Using the extra stability conditions developed in Section III, subsystem W_1 should be designed stable when it is connected with a current-source input, while subsystem W_2 should be designed stable when it is connected with a voltage-source input. Hence, a stable system has $R_{W1} \ll (R_P \| R_{W2})$ and $R_{W2} \gg (R_P \| R_{W1})$. Moreover, to be qualified as a current-source converter, $R_P \gg (R_{W1} \| R_{W2})$.

Existing PWM converters as shown in Fig. 9 are mostly designed with a voltage-source input. The current-source-input converter can be derived from the basic voltage-source converter based on duality principle [15], as shown in Fig. 10. However, converters in Figs. 10(a) and (c) are not compatible with the filtering capacitor C_O without appropriate modification. In this example, a higher power dual-boost converter and a lower power buck converter will be chosen as the two parallel load converters W_1 and W_2 respectively.

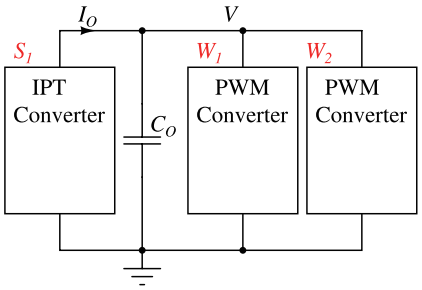


Fig. 8. Block diagram of the single-current-source two-load system.

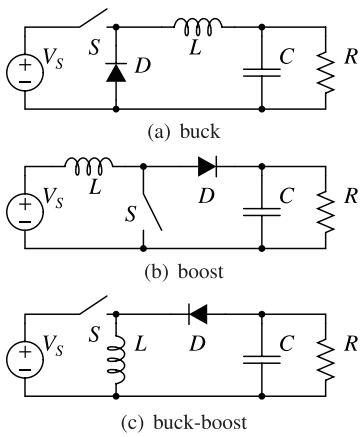


Fig. 9. Basic PWM voltage converters.

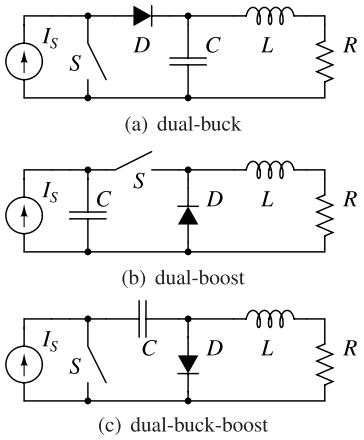


Fig. 10. Basic PWM current converters.

B. Experimental Evaluation

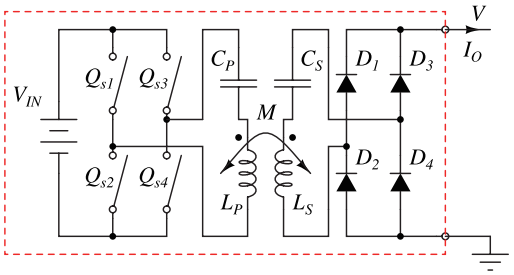
Fig. 11 shows the detailed schematics of subsystems S_1, W_1 and W_2 of the system shown in Fig. 8 with parameters given in TABLE I. The input voltage of S_1 is V_{IN} = 30 V. Since the SSIPT converter operates at resonant frequency f_S, the output current is load-independent [4]-[7], [9]. The equivalent DC output current of the IPT converter can be estimated as $I_O = \frac{8}{\pi^2} V_{IN} \frac{1}{2\pi f_S M} = 2.05$ A.

In this system, W_1 regulates an output current of I_{O1}=3 A, driving a load R_1=3.75 Ω at a power of 33.75 W. Also, W_2 regulates an output voltage of U_{O2} =15 V, driving a load R_2=35 Ω at a power of 6.43 W. Using the viewpoint of pow-

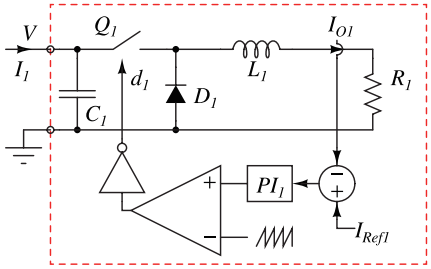
TABLE I
Parameters of Converters

Parameters	Symbol	Value
Primary self inductance	L_P	31.46 μH
Secondary self inductance	L_S	33.02 μH
Mutual inductance	M	9.32 μH
Coupling coefficient	k	0.289
Primary compensation capacitor	C_P	19.73 nF
Secondary compensation capacitor	C_S	18.8 nF
Switching frequency	f_S	202 kHz
Inductance	L_1	2 mH
Capacitance	C_1	470 μH
Proportion Constant	K_{p1}	0.04
Integration Constant	K_{i1}	0.01
Inductance	L_2	2 mH
Capacitance	C_2	470 μH
Proportion Constant	K_{p2}	0.04
Integration Constant	K_{i2}	0.01

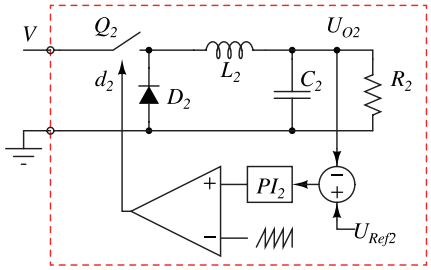
er balance and ignoring the power loss of the converters, the bus voltage can be estimated using VI_O=(33.75+6.43) W as V=19.6 V. The DC input equivalent resistances of the converters on the voltage bus V are R_{W1}=11.4 Ω (21.1 dBΩ) and R_{W2}=59.8 Ω (35.5 dBΩ). These resistances should guarantee $R_{W1} \ll (R_P \parallel R_{W2})$ and $R_{W2} \gg (R_P \parallel R_{W1})$. The converters are built and their impedances are measured and given in the following subsections.



(a) IPT converter S_1



(b) dual-boost converter W_1



(c) buck converter W_2

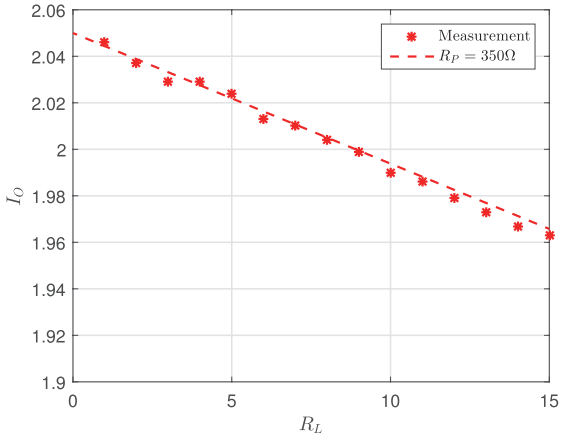
Fig. 11. Schematic of the single-current-source two-load subsystems.

C. Output Resistance of the SSIPT Converter

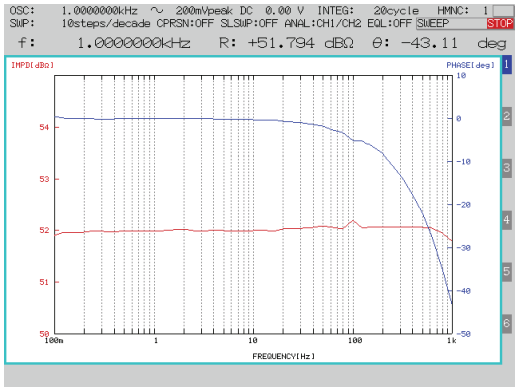
Fig. 12(a) shows measured steady-state output current I_S versus load resistance R_L of S_1. The low-frequency output transfer function can be represented by a Norton equivalent circuit with a parallel connection of current I_O=2.05 A and resistance R_P=350 Ω. Fig. 12(b) shows the small signal output impedance of S_1. With a bandwidth from 0 Hz to 1 kHz, S_1 should be stable driving an impedance lower than 50 dBΩ .

D. Input Resistance of Load Converters

Measured bus voltage versus input current of the two PWM converters are shown as data points marked as '*'



(a)



(b)

Fig. 12. Output characteristics of S_1. (a) Steady-state output current I_O versus load resistance R_L. (b) Small signal response of output impedance.

in Fig. 13. The dotted lines are constant power curves of the converters. Small-signal impedances of the converters are also measured and shown in Fig. 14, where W_1 is stable when it is driven by an ideal current source with infinite impedance, and W_2 is stable when it is driven by an ideal voltage source with zero output impedance.

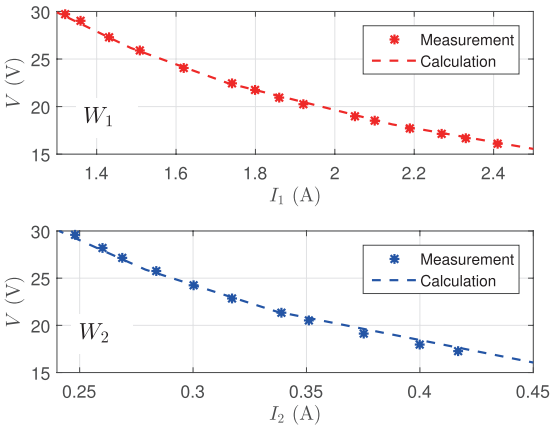
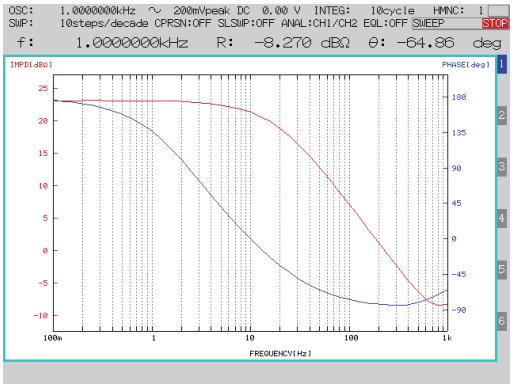
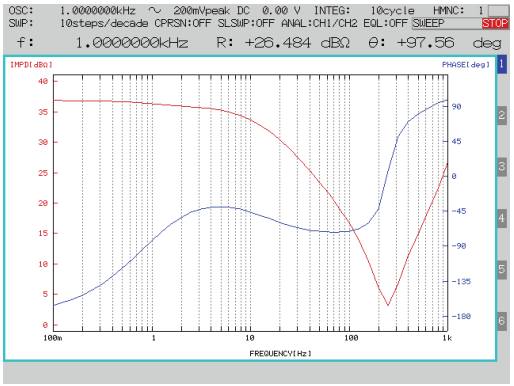


Fig. 13. Measured input VI steady-state characteristics of PWM converters W_1 and W_2. The dotted constant power curves fit well with the input powers 33.75 W of W_1 and 6.43 W of W_2.



(a) dual boost converter W_1



(b) buck converter W_2

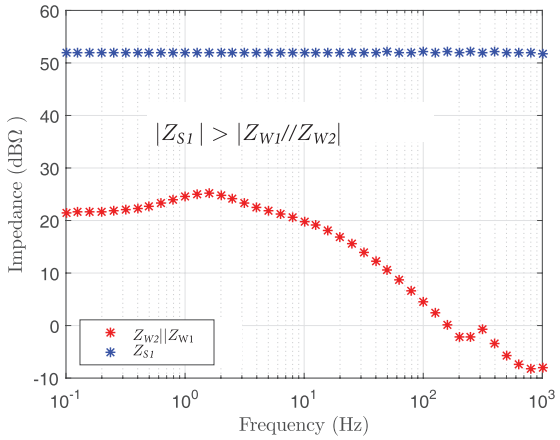
Fig. 14. Measured input impedances of PWM converters.

E. Stability Verification

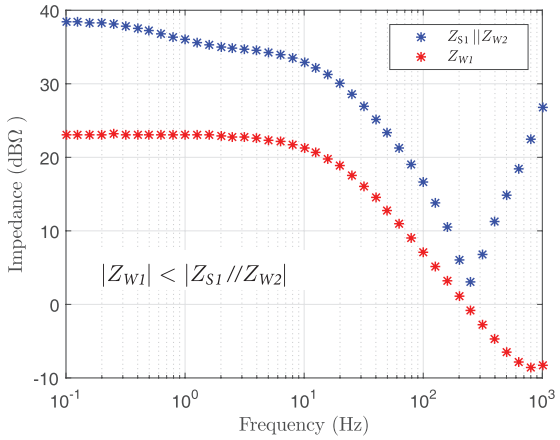
From the measurements taken in Section V-D, small-signal responses of the three converters are compared with emphasis of the local stability of each converter. Fig. 15 indicates that the converters are all locally stable within the measured bandwidth from 0 Hz to 1 kHz. To verify the system stability in general, step transient responses are measured.

The control of the subsystems are tested by maintaining power balance at steady state. Firstly, the control of W_2 is disabled by fixing D_2, such that it behaves as a resistor of $R_{L2}=\frac{R_2}{D_2^2}$. Then, W_1 is tested for its stability under closed-loop control. Fig. 16(a) shows the step response to a sudden reduction of the output reference current I_{Ref1} of W_1. It shows that R_{L1} decreases with decreasing output power, which coincides with the slope of the operating point R_{L1} in Fig. 5.

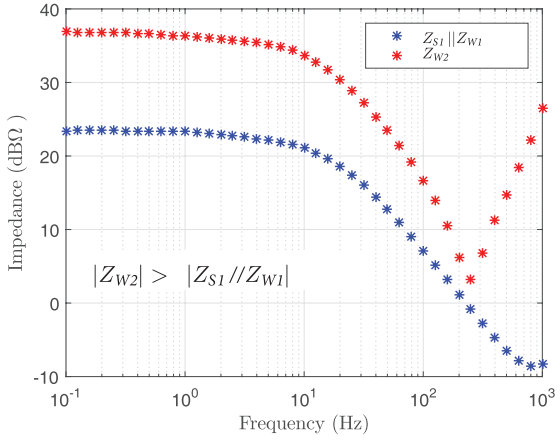
A similar experiment is done to test the stability of the control for W_2. The duty cycle of W_1 is disabled by fixing D_1, such that it behaves as a resistor of $R_{W1}=\frac{R_1}{D_1^2}$. W_2 is tested for its stability under closed-loop control. Fig. 16(b) shows the step response to a sudden reduction of the output voltage reference U_{Ref2} of W_2. It shows that R_{W2} increases with decreasing output power, which coincides with the slope of the operating point R_{Ly} shown in Fig. 5.



(a) SSIPT converter S_1



(b) Dual boost converter W_1



(c) Buck converter W_2

Fig. 15. Measured magnitude of impedance ratio for verification of local stability within the bandwidth from 0 Hz to 1 kHz for (a) converter S_1 using C3(a), (b) converter W_1 using C3(a), and (c) converter W_2 using V3(a).

Finally, W_1 and W_2 are controlled independently. Fig. 17 shows the system in response to the cold start of W_2. It shows that the single-current-source-two-load system is stable, when the design is based on the generalized stability criteria developed in this paper.

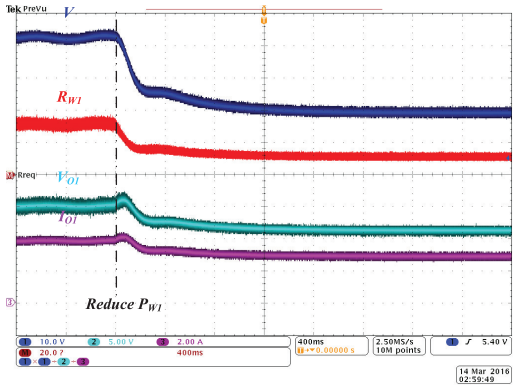


Fig. 16. Step response of the system. (a) Sudden reduction of the output reference current I_{Ref1} of W_1 leading to a reduction of input voltage V, a characteristic of a current source system. Traces U_{O1} and I_{O1} are the output voltage and current of W_1. Trace R_{W1}, input resistance of W_1, is calculated based on measured data, using $R_{W1} = \dfrac{V^2}{U_{O1}I_{O1}}$, where the loss of the converter is ignored. (b) Sudden reduction of the output voltage reference U_{Ref2} of W_2, leading to an increment of V, a characteristic of a voltage source system. Traces U_{O2} and I_{O2} are output voltage and current of W_2. Trace R_{W2} is the input equivalent resistance of W_2, calculated using $R_{W2} = \dfrac{V^2}{U_{O2}I_{O2}}$, where the loss of the converter is ignored.

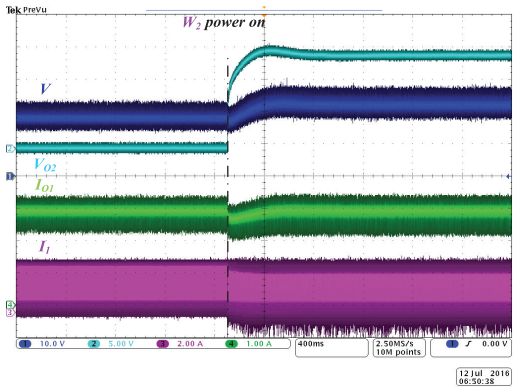


Fig. 17. System response to cold start of W_2. Traces I_1 and I_{O1} are input and output currents of W_1. Traces V and U_{O2} are input and output voltages of W_2.

VI. Conclusion

Impedance-based stability criteria for cascaded systems of converters is revisited in this paper. A more general set of criteria is presented here, which is suitable for the design of systems consisting of a single source cascaded with multiple load converters. This set of impedance-based stability criteria can be conveniently applied to a current output converter cascaded with multiple independently controlled current and voltage converters, such as those used in inductive power transfer systems.

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Published by: Editorial Office of CPSS TPEA

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