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CPSS Transactions on Power Electronics and Applications (CPSS TPEA) is sponsored and published by China Power Supply Society and technically co-sponsored by IEEE Power Electronics Society. It publishes original and high quality peer reviewed papers in the field of power electronics and its applications. With the goal of promoting the technology of power electronics including concepts, theory, modeling and control, analysis and simulation, emerging technology and applications, CPSS TPEA is expected to be a favorable platform to strengthen information exchange in this area. Interested authors are welcome to submit your papers via the Manuscript Central (https://mc03.manuscriptcentral.com/tpea-cpss) online submission system. You can find more information on our website: http://tpea.cpss.org.cn.

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Editorial for the Inaugural Special Issue on the Developing Trends of Power Electronics: Part 3

WITH this editorial, we sincerely welcome our readers to the brand-new publication — CPSS Transactions on Power Electronics and Applications (CPSS TPEA). It is sponsored and published by China Power Supply Society (CPSS) and technically co-sponsored by IEEE Power Electronics Society (IEEE PELS).

CPSS was founded in 1983 and has been the only top-level national academic society in China that solely focuses on the power supply/power electronics area. In the past 30-plus years CPSS has dedicated to provide to its members, researchers, and industry engineers nationwide with high quality services including conferences, technical training, and various publications, and this in deed has helped the society build up its membership rapidly, which now totals up to more than 4000 individual members plus 500 enterprise members. The fast growth of membership in turn compels CPSS to always work out better services for its members, one of which being the open-up of this periodical — a new journal in English language as a publication platform for international academic exchanging. This of course needs to be done through international cooperation, and that's why IEEE PELS is tightly involved, being the premier international academic organization in power electronics area and one of the fastest growing technical societies of the Institute of Electrical and Electronics Engineers (IEEE).

To fulfill the publishing need of the fast-developing power electronics technology worldwide is a more important purpose of launching this new journal. So far there are only 3 or 4 existing journals which are concentrated on power electronics field and have global reputation. For quite a few years people in the international power electronics community have had the feeling that, the existing journals have not even come close to meeting the huge demand of global academic and technology exchanges. E.g., the two existing IEEE power electronics journals, i.e. IEEE Transactions on Power Electronics (IEEE TPEL) and IEEE Journal of Emerging and Selected Topics in Power Electronics (IEEE JESTPE), now publish about 1000 papers a year, which is under a very low paper acceptance rate of around 25%, but still have a back-log of about one year for the newly accepted papers to finally appear in printed form to the public. The addition of this new dedicated journal would be an ideal improvement to fulfill such a tremendous need.

The booming of publishing need really is an indicator of how fast power electronics has been developing in recent years. Innovations have been continuously coming up from component (both active device and passive device), module, circuit, converter, to system level, covering different technical aspects as topology or structure conceiving, modeling and analysis, control and design, and measurement and testing. New issues and corresponding solutions have been continuously presenting as the applications of power electronics prevail horizontally in almost every area and corner of human society, from industry, residence and commerce, to transportations, and penetrate vertically through every stage of electric energy flow from generation, transmission and distribution, to utilization, in either a public power grid or a stand-alone power system. I personally believe that we are entering a world with "more electronic" power systems. The prediction around 30 years ago, that power electronics one day will become one of the major poles supporting the human society, is coming into reality. And I also believe, that power electronics is going to last for long time as an important topic since it is one of the keys to answer a basic question for human society, which is how human can harness energy more effectively and in a manner friendlier to both the user and the environment.

Therefore, I assume that there is probably no better fitting as for CPSS TPEA to publish its first few issues under a special topic about the developing trends of power electronics. We have invited a group of leading experts in different areas of power electronics to write survey/review papers or special papers with review/overview nature to some extent. To publish in a timely and regular style, we organize this inaugural Special Issue into different parts. Part 1 and 2 were published in the December issue last year and the March issue this year respectively, Part 3 appears in this June issue, and the following part is scheduled for the September issue.

In Part 3 we are honored to have 4 invited papers. For the first two, each addresses one hot topic in the area of power semiconductor devices: power loss mechanism and reliability. The next two follow up with the state-of-the-arts in the applications of new power semiconductor devices, one application being solid state transformers and the other being single-phase inverters.

We begin with a paper on the power loss mechanisms for silicon and wide band-gap power semiconductor devices. It is co-authored by Dr. Gerald Deboy and his team from Infineon Technologies. It presents a detailed comparison between the latest generation Super Junction power transistors and e-mode GaN HEMTs and SiC MOSFETs in terms of semiconductor power losses and their potential for further improvement, with a short application section showing the best matching circuits for each device.

The second paper provides a review on the reliability of power semiconductor devices used in power converters.

It is written by Prof. Luowei Zhou and his research group from Chongqing University, and presents a broad overview of reliability researches for power semiconductor devices, including failure mechanisms, condition monitoring, lifetime evaluation and active thermal control. The current issues and future challenges on the reliability of power semiconductor devices are also provided.

The third paper is about the application of a new power semiconductor device in medium voltage (MV) solid state transformers. It is written by Dr. Alex Q. Huang and his research group from North Carolina State University. It reviews the characteristics of 15 kV SiC MOSFET and offers a comprehensive guideline of implementing this device in solid state transformers and other possible MV power conversion scenarios in terms of topology selection, loss optimization and thermal management.

Last but not least, the fourth paper is written by Dr. Huang-Jen Chiu and his research group from National Taiwan University of Science and Technology in cooperation with Dr. Katherine A. Kim from Ulsan National Institute of Science and Technology. The paper focuses on the Little Box Challenge (LBC) — a competition sponsored by Google and the IEEE Power Electronics Society in 2014-2015, where participants were challenged to design a high power-density single-phase 2-kVA inverter. The paper surveys the designs from eight different participating teams, shares experimental results from the Taiwan Tech team, and highlights some interesting innovations from the teams that participated in the LBC.

I'd like to thank the authors of all these 4 invited papers. It's their high-quality contributions that finally leads to the launching of this new journal. I'd like to thank Dehong Xu, President of CPSS, who in 2015 initiated the idea of publishing the new journal and since then has been persistently supporting my work as the founding Editor-in-Chief. I'd also like to thank Jiaxin Han, Secretary General of CPSS, Jan A. Ferreira, President of IEEE PELS, 2015-2016, Don F. D. Tan, President of IEEE PELS, 2013-2014, and Frede Blaabjerg, IEEE PELS Vice President for Products, 2015-2018, who form the CPSS and IEEE PELS Joint Advisory Committee for our new journal with Dehong Xu and myself. Other IEEE officers and leading staffs like Dushan Borojevich, PELS President, 2011-2012, Alan Mantooth, PELS President, 2017-2018, Mike Kelly, PELS Executive Director, and Frank Zhao, Director of China Operations, IEEE Beijing Office, just to name a few, also provided continuous support and constructive advices. My earnest thanks also go to the CPSS Editorial Office led by Lei Zhang, Deputy Secretary General of CPSS, for their wonderful editing work. It would not have been possible to create a new journal in such a short time without their efforts. I'd like to finally thank all the members of the Executive Council of CPSS and particularly the leaders of Chinese power electronics industry. They always firmly stand behind CPSS TPEA and ready to help whenever needed.

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Jinjun LIU received his B.S. and Ph.D. degrees in Electrical Engineering from Xi'an Jiaotong University (XJTU), China in 1992 and 1997 respectively. He currently holds the position of XJTU Distinguished Professor of Power Electronics, sponsored by Chang Jiang Scholars Program of Chinese Ministry of Education.

Dr. LIU coauthored 3 books (including a textbook), published over 200 technical papers in peer-reviewed journals and conference proceedings, and holds more than 30 invention patents (China/USA).He received for 7 times governmental awards at national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements.He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE Transactions on Power Electronics 2016 Prize Paper Award.His research interests are power quality control and utility applications of power electronics, micro-grids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu has served as the IEEE Power Electronics Society (PELS) Region 10 Liaison and then China Liaison for 9 years, an Associate Editor for the IEEE Transactions on Power Electronics for 9 years, and starting from 2015 the Vice President for membership of IEEE PELS.He is on Board of China Electrotechnical Society (CES) and was elected to a Vice President of the CES Power Electronics Society in 2013.He is the Vice President for International Affairs, China Power Supply Society (CPSS) and the inaugural Editor-in-Chief of CPSS Transactions on Power Electronics and Applications.

Perspective of Loss Mechanisms for Silicon and Wide Band-Gap Power Devices

Gerald Deboy, Oliver Haeberlen, and Michael Treu

***Abstract*—With the commercial availability of GaN and SiC-based power semiconductor devices having significantly improved material characteristics, there is a need to discuss the perspective of the underlying physical loss mechanisms of these devices versus their silicon counterparts. This article will compare latest generation Superjunction power transistors versus e-mode GaN HEMTs and SiC MOSFETs in terms of semiconductor losses and their potential for further improvement. A short application section will give practical information on best matching circuits for each device concept.**

***Index Terms*—GaN HEMT, loss mechanisms, power semiconductor devices, Superjunction, wide bandgap devices.**

I. Introduction

THROUGH the introduction of the Superjunction principle [1]-[3], the characteristics of silicon based power MOSFETs could be greatly improved extending the life cycle of this technology up to now and potentially far into the future. Continuous improvement of the technology and major cost-down steps in the fabrication have made Superjunction transistors the first choice for high voltage power devices in the 500 V to 800 V domain. AC to DC power converters in a wide variety of applications such as lighting, adapter, server and telecom power supplies, and EV charging are based on Superjunction transistors as the prevailing technology utilizing a number of well-established power circuits and control methods.

With the arrival of GaN High Electron Mobility Transistors (HEMT) as a potentially game-changing technology [4] new topologies and control methods are challenging classic power supply architectures.

As it is rarely meaningful to put entirely new devices into existing sockets, it is worthwhile to analyze the underlying physical loss mechanisms both for wide band-gap devices and Superjunction transistors. Based on this loss analysis best matches in terms of circuits and control methods are identified. Starting from today's achievements we will give an outlook into further improvement potential with respect to semiconductor losses.

Section II will introduce the limit line of silicon and ways to overcome it with various device concepts. Perspectives are given to further lower the on-state resistance.

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In Section III, switching losses are derived from a physical understanding of the mechanisms inside the device. The influence of control and application circuit is discussed. Experimentally measured values are given both for e-mode GaN HEMTs and latest generation of Superjunction devices.

Based on the loss analysis Section IV suggests best matching circuits and control methods for each power device concept.

A short summary will conclude the article.

II. Device Concepts and Their Potential Towards Lowering the On-State Resistance

A. The Limit Line of Silicon

The optimization of the specific on-state resistance has always been a strong driving factor for the semiconductor industry as it allows differentiation from competition through lower $R_{DS(on)}$ in a given package as well as to lower costs through fabricating more dies on the same wafer.

In the simplest case, the dependency of the on-state resistance can be derived from the Poisson equation in a one-dimensional way as:

$$R_{on} = \frac{4BV^2}{\mu\varepsilon E_C^3}. \tag{1}$$

Modeling silicon's dependency of the critical electric field on doping concentration in an empirical way leads to the well-known formula:

$$R_{on} \approx 8.3\times10^{-9} BV^{2.5}\Omega\cdot cm^2. \tag{2}$$

This relation is known as the "silicon limit". It describes the best specific on-state resistance, which can theoretically be achieved for a given breakdown voltage in case of a one-dimensional p-n junction. It is noteworthy that the optimum doping profile is not constant as function of depth, but shows an increase towards the drain electrode [5] following a hyperbolic sine function. Practically, margins need to be considered both for voltage and $R_{DS(on)}$. Commercial products are therefore typically 20% or more above the limit line [6].

Improvements beyond this barrier have been the subject for research for many decades. In principle there are three fundamental concepts:

1) Changing the material system towards wide band-gap. SiC MOSFETs and JFETs follow this path.

2) Breaking away from the limitations of the one-dimensional Poisson equation by introducing two- or three-dimensional structures. Superjunction devices and field plate (or shielded gate) concepts are classic representatives.
3) Overcoming the relationship between doping and conductivity as expressed in the Poisson equation through doping-independent conduction. The two-dimensional electron gas of GaN lateral high electron mobility transistors proves this concept.

B. Wide Band-Gap Devices

(1) highlights, with its strong dependency on the critical electric field, the motivation to move into wide band-gap materials. The energy required for band-to-band electron-hole generation through impact ionization is much higher; the breakdown field e.g. in SiC with triple the band-gap (3.26 eV vs. 1.12 eV) is hence nearly a factor of 10 higher compared to silicon (2 MV/cm vs. 0.25 MV/cm). Taking further into account mobility and dielectric constant as expressed in the Baliga Figure-of-Merit (FoM), the limit line for SiC is 231 times below the silicon limit. The same rational applies for one-dimensional vertical GaN devices with a FoM advantage of 2097 [7]. Practically, the channel contribution, contact and substrate resistances, the re-distribution of current (especially in planar gate concepts), and last-but-not-least the ruggedness requirements such as short circuit operation [8] are barriers on the way towards the theoretical limits.

C. Two-dimensional Devices (2D)

Two-dimensional devices introduce an electric field component perpendicular to the direction of current flow. Conductivity in the on-state and blocking characteristic are hence no longer coupled through the Poisson equation.

As shown in Fig. 1, Superjunction transistors lower the specific on-state resistance through a compensation structure formed by p-doped pillars placed adjacent to the n-type current conducting regions, thus allowing much higher doping levels in the n-regions.

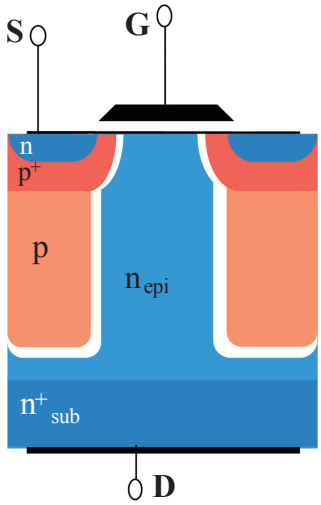

Fig. 1. Vertical Superjunction transistor with planar gate structure.

The p-pillars do not contribute to current conduction in the on-state, but help to maintain the blocking voltage during the off-state by compensating the donor charges in the n-columns. The blocking characteristic depends on the effective doping level, that is, donor charges minus acceptor charges, while the on-state resistance depends on the n-doping level alone. The concept allows therefore an optimization of the area-specific on-state resistance far below the silicon limit. As the adjacent p- and n-columns create a horizontal component of the electric field, an increase of doping level needs to be accompanied by reduction of the cell pitch to stay within the limits of the critical electrical field. The overall electric field is given by a superposition of horizontal and vertical field vectors. The relationship between blocking voltage and $R_{DS(on)}$ [3] can now be expressed as:

$$R_{on} \cdot A_V = 4 \cdot w \cdot \frac{V_B}{\mu \cdot \varepsilon \cdot E_C^{\,2}}. \tag{3}$$

This formula shows a significantly more favorable dependency between on-state resistance and breakdown voltage. Modelling the doping dependence of the critical electrical field in a similar way as described above gives $R_{on} \cdot A_V \approx V_B^{1.3}$ instead of $R_{on} \cdot A_V \approx V_B^{2.5}$ as expressed in (2). The direct proportionality to the cell pitch w, enables a continuous path towards ever lower on-state resistance. Fig. 2 shows this race towards lower R_{on} and the hitherto achieved results.

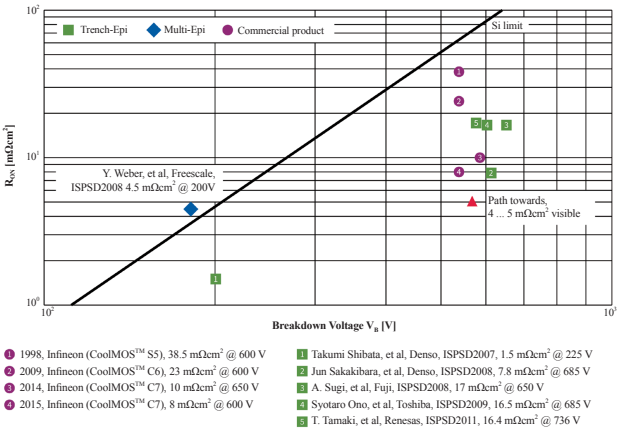

Fig. 2. Specific on-state resistance for different Superjunction devices using Trench Epi and Multi-Epi processes against the limit of silicon.

As the blocking capability of the device depends crucially on the local difference of charges, an elaborate scheme is required to control doping levels both in the p- and n-column precisely during mass production. In order to reduce the on-state resistance below the silicon limit, doping levels in the n-column in the upper 10^{15} cm^{-3} to lower 10^{16} cm^{-3} range are necessary, whereas a high blocking capability such as 600 V, mandates an effective doping level below 1 to $2 \cdot 10^{14}$ cm^{-3}. The relative difference of charges must be balanced within few percent of their absolute doping levels. A surplus of donor charges turns

the drift layer into a lightly n-doped area, a surplus of acceptor charges into a lightly p-doped area. Consequently, with constant doping profiles, the gradient of the vertical electric field changes its sign, moving the point of highest electric field from the top side to the bottom side of the device. Such a characteristic may create instabilities and must be avoided. Hence, constant doping profiles for p-and n-columns are not favorable [9].

In terms of manufacturing technology the subsequent deposition of epitaxial layers with intermediate implantation steps has proven to be compliant both with these needs and has paved a way towards an area specific on-state resistance below 10 $m\Omega \cdot cm^2$. Alternative concepts comprise trench etching and epitaxial re-fill of trenches. In this case grading of doping profiles need to be controlled through the taper angle of the trench.

From our view point refining production technology and device concept will allow further improvements down to an area specific on-state resistance in the range of 4 to 5 $m\Omega \cdot cm^2$. Besides production tolerances, early depletion of the current-conducting n-columns may pose a final limit to the Superjunction principle as pointed out by Disney and Dolny [10]. For more background on the history and further use cases of the Superjunction principle, we refer the reader to a recently published article by Udrea *et al.* [11].

The field plate concept is another representative of two-dimensional device concepts. The horizontal field component is created between a metal or quasi-metallic electrode being isolated from the drift region through a thick oxide. Being typically connected to the source electrode, the field plate helps to deplete the n-doped mesa region. Similar to Superjunction transistors, the n-doped region can be significantly higher doped than possible under the limitations of the one-dimensional Poisson equation. Another advantage of the concept is that the field plate shields the gate electrode, which is typically being fabricated within the same trench. The overlap between gate and drain electrode is therefore minimized. The concept is therefore not only beneficial for the on-state resistance, but also for the gate-to-drain capacitance. This makes this structure the preferred technology for power MOSFETs with low to medium breakdown voltages such as 25 V to few hundred volts. Since its introduction the area-specific on-state resistance has been lowered a factor of 50 versus planar silicon power MOSFETs and roughly one order of magnitude versus early implementations of the concept.

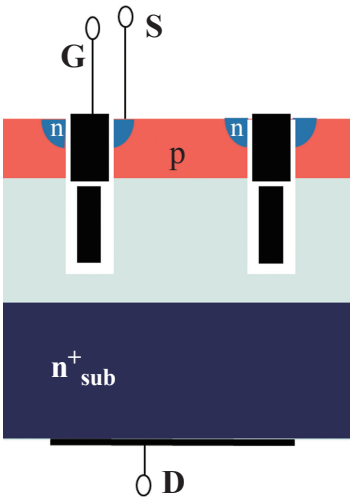

Fig. 3. Vertical power MOSFET with field plate.

Towards higher breakdown voltages the structure is limited by the thickness of the oxide around the field plate, which poses a barrier towards reduction of the pitch and technological challenges. Recent technology analysis has shown that the cross-over point in terms of on-state resistance between field plate and Superjunction concept is located between 300 V and 400 V. Fig. 3 shows the basic structure.

D. GaN High Electron Mobility Transistor

The third way to break the limit line of silicon is one of the most challenging but also the most rewarding. Stacking AlGaN on GaN forms a spontaneous charge layer at the interface due to the differences in polarization between the two materials. The charge is confined in the third dimension on the one hand by the bandgap difference at the hetero junction and on the other hand by the band curvature. Hence a two-dimensional charge sheet is created at the interface without any doping in which electrons can move freely. This so-called two dimensional electron gas (2DEG) is the basis for GaN High Electron Mobility Transistors (GaN HEMT). The concentration of the electrons is defined by the mismatch in polarization and can be adjusted through concentration and thickness of the AlGaN barrier.

Contacting this electron gas and controlling the current flow through a gate electrode forms high performance lateral transistors with very high electron mobility and the potential towards unrivalled low area-specific on-state resistance. As the electron gas conducts at zero gate bias, GaN HEMTs yield naturally normally-on transistors. Consequently, effort is required to turn transistors into normally-off or enhancement mode (e-mode) devices as the majority of power electronic applications are voltage source converters. Two major concepts have been commercially introduced to the market: MISFETs, where the AlGaN barrier is locally thinned and the gate electrode is insulated from the 2DEG through a very thin dielectric layer and p-GaN gate transistors having a p-n junction between gate and the 2DEG. The latter concept exists in two variants: the p-GaN gate injection transistor used by Panasonic and Infineon operates with an ohmic contact to the p-GaN gate. It requires a low bipolar current to clamp the gate to a positive forward bias during the on-state of the transistor, but has the unique advantage, that it can tolerate several amperes of forward current thus limiting effectively any voltage spikes on the gate [12]. The second variant of the p-GaN gate concept operates with a Schottky contact to the gate, which yields a low gate current but has issues with a high susceptibility to gate rupture through voltage spikes.

Besides devices showing a normally-off characteristic on

die, also normally-on or depletion mode transistors are commercially available. In this case the transistors are turned into normally-off through a cascode circuit, where a series low voltage MOSFET switches the source of the HEMT with the gate electrode of the HEMT being connected to the source of the LV FET. Even though driving the cascode is easy, we believe that the bigger potential is with e-mode devices. First, the series low voltage MOSFET adds capacitance and complexity deteriorating especially FoMs for charge of the output capacitance; second, power devices require essentially slew rate control. Hence, direct gate access as provided by the e-mode concept is preferred to the indirect switching of the cascode.

Fig. 4 shows an e-mode GaN HEMT and its electric symbol, Fig. 5 shows the cascode circuit.

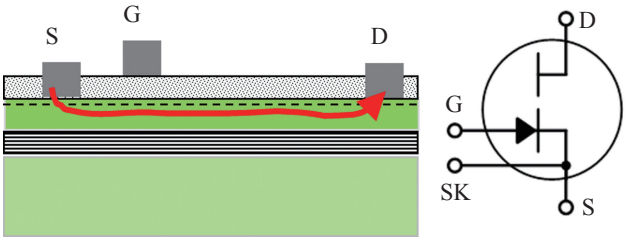

Fig. 4. Structure of lateral GaN HEMT and electrical symbol of the e-mode GaN HEMT.

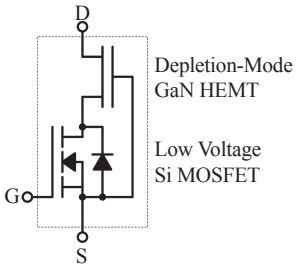

Fig. 5. Electric circuit for depletion mode GaN HEMT (cascode).

The relationship between on-state resistance and breakdown voltage does not follow the theory for vertical power devices but is much closer to the theory for silicon-on-insulator devices as formulated by Zingg [13]. In case of constant density of the 2DEG, the field distribution along the drift zone can be compared to one-dimensional RESURF devices. Characteristic are two distinct peaks of the electric field at the gate electrode and the drain contact. Further device optimization can therefore follow the ideas developed for lateral RESURF devices [14]. Fitting a curve to published experimental values of R_{DS}(on) and breakdown voltage suggests a dependency $R_{ON} \cdot A_V \approx V_B^{1.3}$ similar to the relationship derived for Superjunction transistors. Fig. 6 shows the corresponding graph in comparison to the vertical limit lines of silicon, SiC and GaN, where data points are taken from [7].

Obviously, there is large improvement potential from today's state-of-the-art towards fundamental limit lines making GaN HEMTs a very interesting candidate for significant

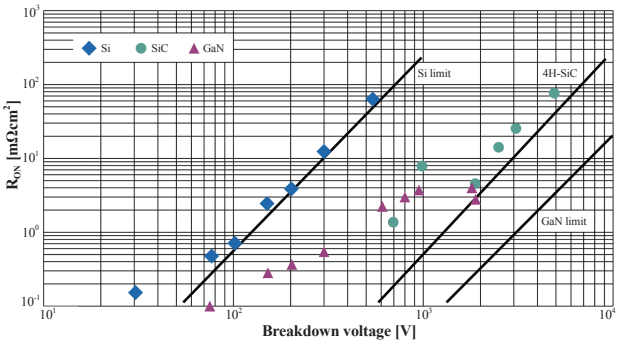

Fig. 6. Reported values for area specific on-state resistance for GaN HEMTs and SiC in comparison to material specific limit lines for vertical devices [7].

reduction in terms of $R_{on} \cdot A$ and cost.

III. Switching Losses With Special Emphasis on Wide Bandgap and Superjunction Power Devices

We will group switching losses into three distinct categories: turn-off losses, turn-on losses, and soft switching losses. We will not consider gate drive losses, as these losses are comparatively small for high voltage devices, being the main scope for this article.

A. Turn-off Losses

Fast switching power devices, such as Superjunction, GaN HEMT, or SiC devices, are able to come at least close to the theoretical limit of switching losses during turn-off. The minimum turn-off loss being recorded at the terminals as overlap of current and voltage is the energy stored in the output capacitance [15]. In this case, the channel - be it a MOS channel or a bipolar Gate-injection structure such as in e-mode GaN HEMTs - is turned off before the voltage across drain to source rises. The load current commutates into the output capacitance charging it from zero Volts up to the DC link voltage. If this mechanism is lossless - we will see later that this is not entirely true - the energy, observed on the oscilloscope as overlap between voltage and current, equals the energy E_{oss}, a value which is typically given in the datasheet. It is noteworthy that the energy stored in the output capacitance should be derived from large signal analysis not from small signal due to hysteresis effects especially in Superjunction devices [16], [17].

If we turn-off in this way, physically speaking, no energy is yet dissipated. The current inside the device flows as a capacitive displacement current not as a drift current. That means that the space charge layer inside the device structure builds up by carriers moving away from the boundary of the space charge layer towards the contacts. In case of a Superjunction transistor, electrons will move within the n-columns to the drain, holes will move within the p-columns to the source contact leaving a depleted zone behind. The key point is that these carriers are not crossing any space charge layer. They should always flow as majority carriers within unde-

pleted areas. The turn-off mechanism is hence in the ideal case entirely lossless. The energy stored in the output capacitance is dissipated when the device is turned on under voltage unless an external circuit provides zero voltage switching conditions. The energy stored in the output capacitance is therefore a good indicator on the strength of a power device to achieve low overall switching losses. Especially for hard switching circuits such as Continuous Current Modulation (CCM) for e.g. Power Factor Correction (PFC) applications, improvements in the energy stored in the output capacitance lead directly to corresponding lower overall losses and better efficiency.

Even though fast turn-off is desirable from an efficiency perspective, there are several drawbacks to this concept. There is basically no slew rate control as the voltage rise dv/dt (4) is defined by the load current and the shape of the output capacitance.

$$dv/dt = \frac{I_l}{C_{oss}} \tag{4}$$

Reducing the output capacitance especially on the high voltage end helps to reduce the energy stored in the output capacitance, but makes the device inevitably faster switching. This is especially true for Superjunction devices and GaN HEMTs. Both devices have the capability to switch at a speed of far greater than 100 V/ns.

In abnormal conditions such as an AC cycle drop in a PFC stage or a secondary side short circuit on a LLC converter, very high currents may occur, leading to excessive high dv/dt. These high slew rates may create issues with EMI or induce parasitic oscillations, which may potentially destroy the power device.

In many cases, the switching speed must be limited. The most effective and most common way is to use a gate resistor, which limits the current for charging and discharging the gate capacitance of the device. Turning off the MOS channel takes a little bit longer. The control is now implemented through the reverse capacitance C_{gd}. The slew rate is expressed as (5) with gate current I_g, gate resistor R_g, and Miller plateau voltage V_{MP}. By varying R_g the slew rate can be controlled accordingly. During the Miller plateau phase, the voltage across drain to source V_{DS} rises; the entire gate current flows through the reverse capacitance C_{gd}, the gate voltage V_{GS} does not change. After this plateau, the voltage has reached the DC link voltage and the current starts to fall. The device is controlled in this period by the discharging of the input capacitance below the Miller plateau voltage and the corresponding transconductance of the power device.

$$dv/dt = \frac{I_g}{C_{gd}} = \frac{V_{MP}}{R_g \cdot C_{gd}} \tag{5}$$

Fig. 7 shows these behaviors in an ideal manner without any parasitics.

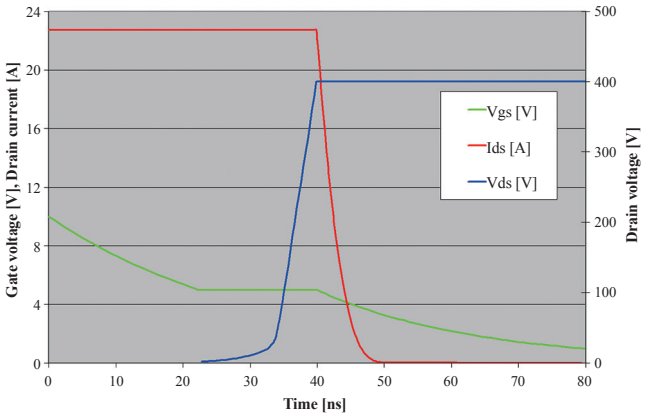

Fig. 7. Ideal turn-off of a power device by controlling the turn-off speed by the gate current flowing through the reverse capacitance C_{gd}.

Ideally, the gate resistor is chosen in such a way, that in normal operation conditions, optimum lossless turn-off is maintained, but at high peak currents both dv/dt and di/dt is controlled. In this way, both safe operation and best efficiency is achieved.

Fig. 8 shows resulting di/dt and dv/dt slew rates as a function of load current and gate resistor for a 190 mΩ Superjunction device (CoolMOS™ CP). Limiting, for example, di/dt below 2000 A/µs and dv/dt below 60 V/ns requires a gate resistor of around 20 Ω. For load currents below 5 A di/dt and dv/dt is still linearly increasing with load current. Control follows hence the lossless charging of the output capacitance. At higher currents, however, the control is shifted into C_{gd} control with corresponding limitations on dv/dt and di/dt.

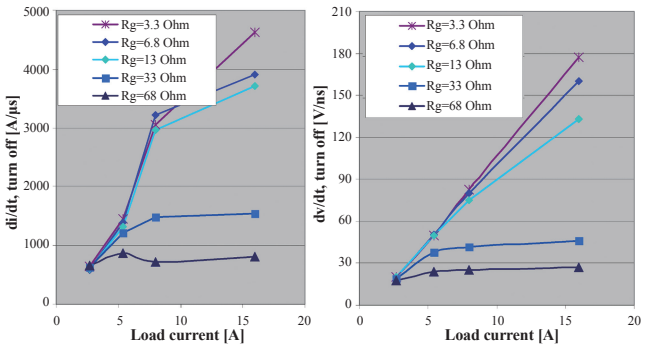

Fig. 8. Slew rated di/dt (left) and dv/dt (right) as function of load current and gate resistor during turn-off, Superjunction device 600 V / 190 mΩ.

Recent Superjunction generations have been optimized to allow this combined control seamlessly with minimum effect on efficiency. Fig. 9 shows the turn-off losses as function of load current for the latest generation of Superjunction devices (CoolMOS™ C7).

As shown in Fig. 9 using, for example, a gate resistor in the range of 10 Ω allows minimum turn-off losses close to the theoretical limit for a current range up to 15 A.

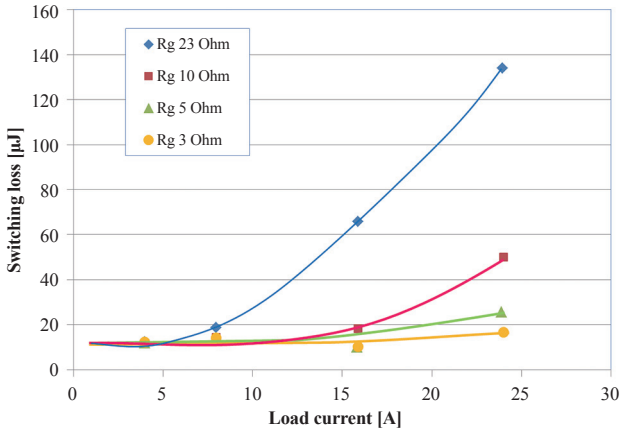

Fig. 9. Turn-off loss of a 60 mΩ / 600 V rated Superjunction device as function of current and gate resistor switching against a 6 A SiC Schottky barrier diode.

B. Turn-on Losses

Turn-on losses can be divided into two major contributions: one loss source arises from parasitic capacitances of the switching cell circuit, and a second loss source comes from shortening the output capacitance of the power device itself. A switching cell consists fundamentally of the switch, a freewheeling element, and at least an input capacitor. In case of a boost converter the freewheeling element is a diode, preferably a SiC Schottky barrier diode, or in case of a synchronous boost, a power MOSFET such as Superjunction or GaN HEMT. In case of a flyback, the freewheeling element is a synchronous MOSFET or a diode on the secondary side of the transformer.

In hard switching conditions the charge of the freewheeling element is added to the load current causing a characteristic current peak. Fig. 10 shows an example of a 70 mΩ GaN HEMT half bridge device arranged in a symmetric half bridge. Both turn-on and turn-off show very linear di/dt and dv/dt slopes. The turn-off waveform demonstrates perfect shut-off of the channel before the voltage rises, thus bringing

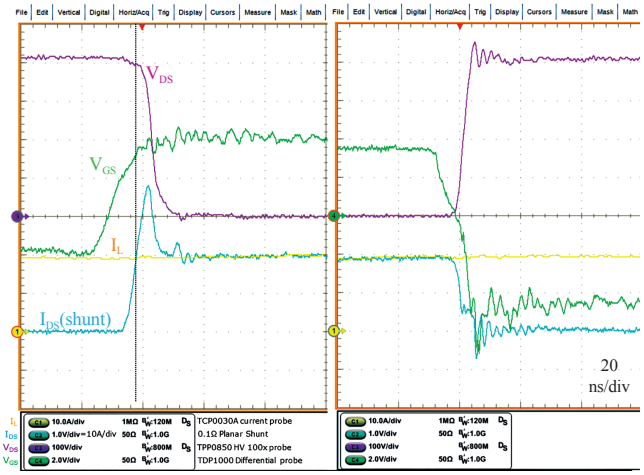

Fig. 10. Turn-on and turn-off waveform of a 70 mΩ / 600 V rated e-mode GaN HEMT arranged in a symmetric half bridge.

the turn-off loss very close to its theoretical minimum. It is noteworthy, that GaN offers such loss-less turn-off at a time scale of just a few ns.

The losses from the freewheeling element amount in total to $Q_{oss} \cdot V_{DC}$ as a minimum with Q_{oss} being the charge stored in the output capacitance of the freewheeling element. The distribution of this loss into the device turning on and the freewheeling element respectively is given by the voltage dependency of Q_{oss}. Whereas Superjunction devices basically deliver the entire Q_{oss} at very low voltage, GaN HEMTs show a more favorable dependency with losses roughly evenly split between both devices in the half bridge. Fig. 11 shows the Q_{oss} curves of advanced Superjunction versus an e-mode GaN HEMT.

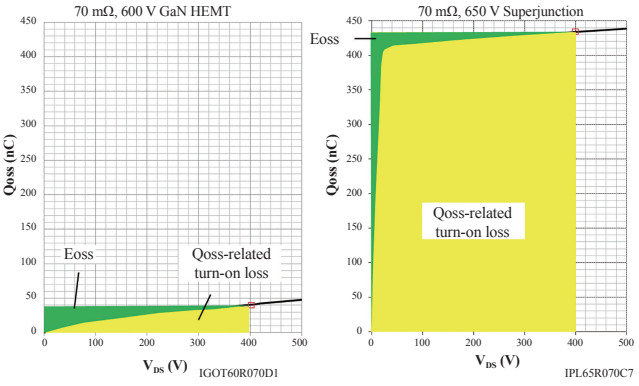

Fig. 11. Comparison of Q_{oss} versus voltage for an e-mode GaN HEMT (left) to an advanced Superjunction device (right).

The Q_{oss} curve represents the losses associated from the freewheeling element as yellow shaded area. These losses can be expressed as:

$$E_{Qoss} = \int_0^{V_{DC}} Q_{oss}(V) \cdot dV \,. \tag{6}$$

Similarly, the losses associated with short-circuiting the output capacitance E_{oss} can be seen as green shaded area in the same graph [18]. Despite GaN HEMTs having nearly a factor 10 lower Q_{oss} in comparison to Superjunction, the energy E_{oss} is in the same order of magnitude. The losses originating from E_{oss} can be expressed as:

$$E_{Eoss} = \int_0^{V_{DC}} C_{oss}(V) \cdot V \cdot dV \,. \tag{7}$$

The output capacitance should be derived from large signal analysis. The strong non-linear shape of the output capacitance of Superjunction devices leads to a very good optimization of E_{oss}-associated losses, which is a prerequisite for hard-switching circuits with SiC Schottky barrier diodes or silicon-based ultra-fast diodes as freewheeling elements. GaN HEMTs will in addition also perform perfectly well in symmetrical half bridges, where Superjunction devices can only be used with external circuitry providing zero voltage conditions.

A third contribution of turn-on losses comes from the inevitable overlap of load current with voltage. Assuming constant dv/dt and di/dt slopes these losses can be modeled as:

$$E_{I-V} = \frac{1}{2} \cdot \left(V_{DC} \cdot \frac{I_L^2}{dI/dt} + I_L \cdot \frac{V_{DC}^{\ 2}}{dV/dt} \right). \qquad (8)$$

This formula gives an interesting insight into the necessity for fast switching to optimize losses. As long as both di/dt and dv/dt increase linearly with load current, turn-on losses from the overlap of current and voltage will increase only linearly with load current. The efficiency of a power converter with losses only linearly increasing with load is constant. If, however, di/dt or dv/dt needs to be limited, losses will increase parabolically; the converter efficiency will correspondingly decrease as function of load.

It is hence of utmost importance to optimize layout and parasitic inductances of the switching cell to take the maximum benefit of modern power devices with their intrinsic capabilities to reduce switching losses. SMD packages such as TO-leadless or at least packages with separate source bond wire (Kelvin contact) such as 4-pin TO 247 will be mandatory to tap into the performance advantages of modern power devices.

Fig. 12 shows turn-on, turn-off, and sum of switching losses for an e-mode GaN HEMT arranged in a symmetric half bridge.

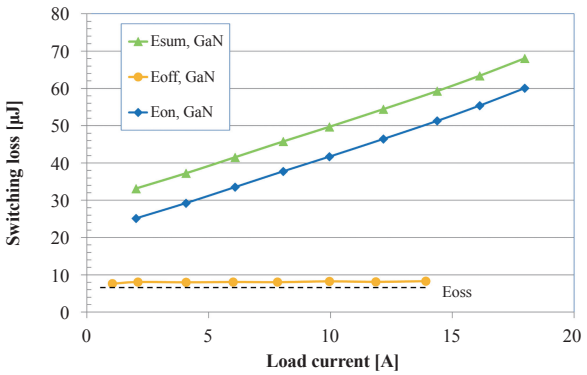

Fig. 12. Turn-on, turn-off, and sum of switching losses of a 70 mΩ / 600 V rated e-mode GaN HEMT arranged in a symmetric half bridge.

In the considerations above we assumed unipolar current transport in the freewheeling element. This is both true for GaN HEMTs and for SiC Schottky barrier diodes, however false for Superjunction devices. In reverse direction the intrinsic body diode of the device (see Fig. 1) will conduct and will flood the voltage supporting zone with electron hole plasma. In hard switching symmetric half bridges, there will be hard commutation of this conducting body diode. Due to the device structure of Superjunction devices with its deep p-columns, the electron-hole plasma needs to be entirely removed before the device blocks voltage. This effect leads to a very high reverse recovery peak and a snappy discontinuation of the reverse recovery current with very high di/dt values. Fig. 13 shows a comparison of the hard commutation behavior of a Superjunction device in comparison to an e-mode GaN switch.

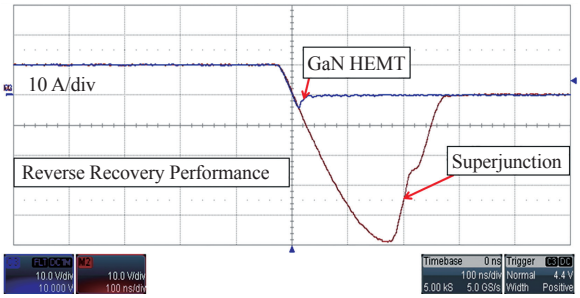

Fig. 13. Comparison of the reverse recovery behavior of an e-mode GaN HEMT in comparison to a Superjunction device.

The amount of reverse recovery charge can be reduced through reduction of the ambipolar carrier life time leading to overall lower losses. The device can be made rugged to ensure survival during hard commutation events (e.g. CoolMOS™ P7); the snappiness of the body diode however will always remain.

Taking these additional Q_{rr} losses into account, Superjunction devices are ruled out for symmetric half bridge circuits unless external circuitry is provided for zero voltage switching. We will discuss examples of these circuits in Section IV.

C. Perspective of Switching Losses

All power devices discussed in this article, be it based on silicon using field plate, on the Superjunction concept, or on wide bandgap materials, have the possibility to switch at several thousand amperes per microsecond and at dv/dts beyond 100V/ns. Losses arising from the overlap of current and voltage can hence be minimized to limits given by EMI and layout parasitics.

With GaN HEMTs, and to some extent with SiC MOSFETs, (near) Q_{rr}-free devices exist.

The energy stored in the output capacitance, E_{oss}, can be reduced further with every technology step. Fig. 14 shows a comparison of the output capacitance of three consecutive technology nodes of Superjunction devices versus an e-mode GaN HEMT.

The continuous race for lower area specific on-state resistance shifts the output capacitance into more pronounced non-linearity with every generation. This trend helps to reduce the energy stored in the output capacitance, yielding lower switching losses and better efficiency in hard switching applications. However, the devices inherently switch faster at the same load current. Furthermore the turn-off delay time, an important feature for resonant applications, increases.

GaN HEMTs show, in comparison, a near linear shape of the output capacitance which is reflected in and extremely linear switching waveform with near constant dv/dt as

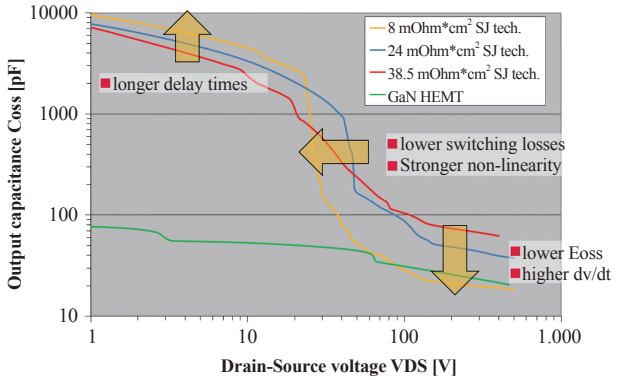

Fig. 14. Development of the characteristic output capacitance of three consecutive technology nodes of Superjunction device in comparison to an e-mode GaN HEMT.

shown in Fig. 10. The comparison of the energy stored in the output capacitance is given in Fig. 15.

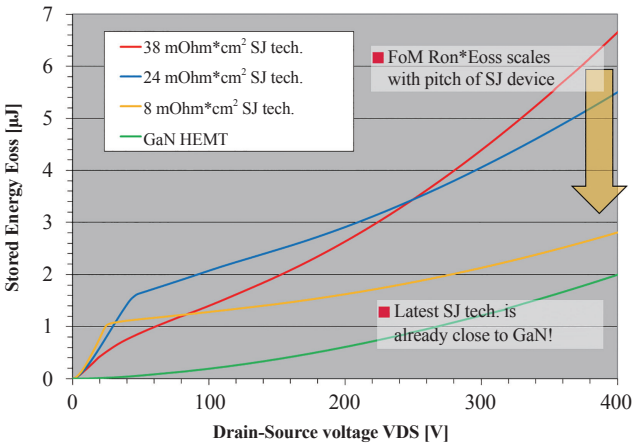

Fig. 15. Trend for the energy stored in the output capacitance across three consecutive generations of Superjunction devices in comparison to GaN HEMTs.

The latest generations of Superjunction devices are already reaching the E_{oss} levels of GaN HEMT devices. With every generation E_{oss} will further decrease. The path down towards 4 to 5 mΩ·cm^2 will hence coincide with a reduction of the E_{oss} of another factor of 2. Obviously, improvements in GaN device concept and technology will also result in a lowering of the energy stored in the output capacitance.

The outlook into the primary intrinsic loss mechanism for power device is hence bright both for Superjunction and wide bandgap devices.

All device concepts allow, in hard switching applications, superior performance. Superjunction devices are best when switched against SiC Schottky barrier diodes. Wide bandgap devices, GaN HEMTs and SiC MOSFETs, can be switched in a symmetric half bridge configuration.

In soft switching applications, where an external circuit ensures zero voltage transition, the sum of turn-on and turn-off losses can be significantly below the E_{oss} limit. As the turn-off mechanism is, physically speaking, lossless and the voltage is reduced to zero volts prior to turn on of the device, the only remaining losses are arising from secondary effects such as charging and discharging of internal capacitances and from lumped resistances e.g. in the device contact areas. Fig. 16 shows the sum of hard switching losses versus soft switching losses and the theoretical limit line of E_{oss} for the latest generation of Superjunction devices.

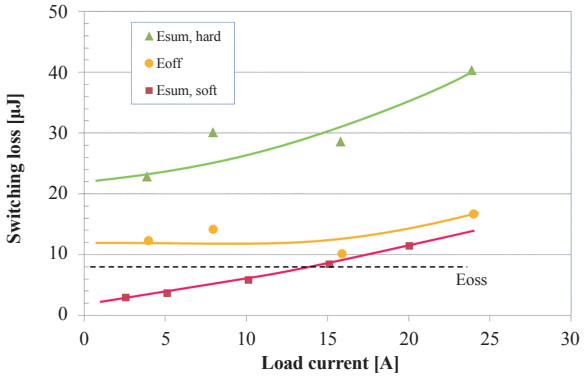

Fig. 16. Comparison of the sum of soft switching losses versus hard switching losses and the energy stored in the output capacitance, E_{oss}. 600 V rated device, 60 mΩ, switching against 6 A SiC Schottky barrier diode.

As long as turn-off losses are constant (up to around 15 A for the 60 mΩ / 600 V rated device) the sum of soft switching turn-on and turn-off losses stays clearly below the E_{oss} limit line. The linear increase of losses in this range can be attributed to charging and discharging the output capacitance and reflects increasing losses due to an increasing dv/dt slew rate. Beyond 15 A additional losses from turn-off are added as the channel is now not completely turned off before the voltage across the device rises.

Fig. 17 shows a comparison of round-cycle soft switching losses of Superjunction, GaN HEMT and SiC MOSFET measured with a novel calorimetric approach [19]. The level of loss energies of all device concepts is with a few µJ quite similar. The GaN HEMT not only shows the lowest losses but will offer the greatest improvement potential for the future with respect to soft switching losses.

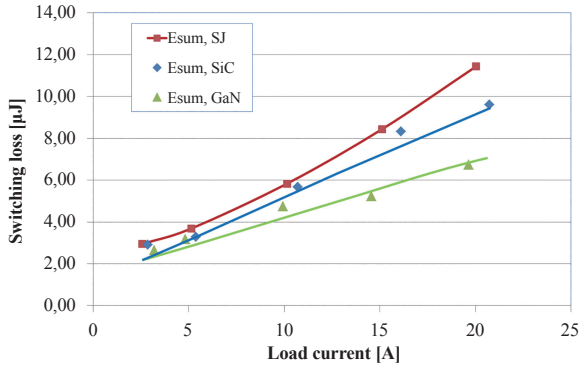

Fig. 17. Comparison of soft switching losses for Superjunction, GaN HEMT and SiC MOSFET, taken from [19].

IV. Device Concepts and Their Best Matching Application Circuit

The key for a true comparison of devices in the application is to choose appropriate circuits and control methods, which bring out the best performance of the individual device concept. As we discussed in the previous sections, Superjunction performs best when switching versus a SiC Schottky barrier diode as freewheeling element. Alternatively, good results are found in zero voltage switching applications at low to medium high switching frequency (30 to 300 kHz). GaN HEMTs can be used in hard switching applications due to their true zero reverse recovery charge. SiC MOSFETs still show some reverse recovery charge even though the ambipolar carrier life time is extremely short. Nevertheless, even for a GaN HEMT the Q_{oss} related charge is roughly a factor 5 higher than the corresponding charge of a SiC Schottky barrier diode. Switching frequencies for hard switching half bridges need hence to be chosen appropriate to keep Q_{oss} related switching losses comparatively low.

Fig. 18 shows the classic Continuous Current-Mode (CCM) boost stage, which is the prevailing topology for many switch mode power supply applications. As a result, as shown in Fig. 19, a peak efficiency of 98.5% and full load efficiency above 98% is achieved when this circuit is used with the latest generation of Superjunction devices and SiC Schottky barrier diodes.

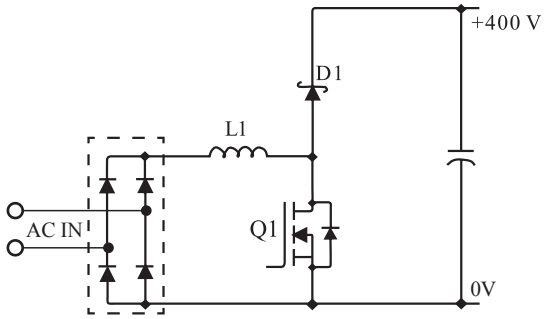

Fig. 18. Classic continuous current-mode boost stage.

This type of power factor correction stage achieves Platinum or Platinum + level if combined with a well-designed LLC stage including synchronous rectification. If Titanium level needs to be reached, the losses of the bridge rectifier become a major hurdle. Two conducting diodes create at high line (230 V AC) an efficiency drop of around 0.7%. This issue can be overcome with bridgeless topologies, having only one or even no conducting diode in the power flow path.

Fig. 20 shows two alternative circuits for bridgeless topologies with only one remaining conducting diode.

Both topologies have only one inductor and two switches. The totem pole has, in the minimum configuration, two slow diodes (D1, D2), but should use another two slow diodes for surge protection. The H4 topology uses two fast diodes (SiC

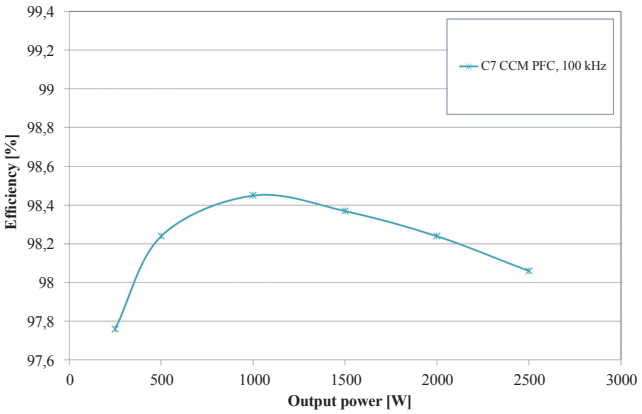

Fig. 19. Measured efficiency of a CCM PFC stage using a 65 mΩ Superjunction device in a 4-pin Kelvin contact TO package switching at 100 kHz versus a 16 A rated SiC Schottky barrier diode.

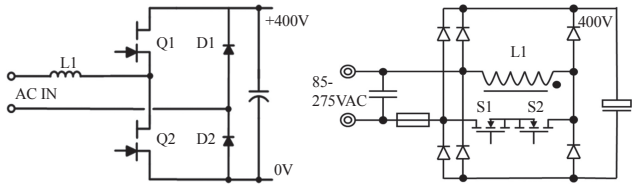

Fig. 20. Bridgeless topologies with only one conducting diode in the power flow path: totem pole (left) and H4 topology (right).

Schottky barrier diodes or ultrafast silicon diodes) and four slow diodes [20]. In the totem pole there is only one diode conducting in the power path. The H4 topology has, during the on-phase of switches S1 and S2, no conducting diode in the power path; during the off-phase of the anti-serial switches, one fast diode and one slow diode conducts. This topology is therefore versatile for low line conditions where the modulation index of switches S1/S2 is high.

When operating in continuous current mode, the totem pole requires switches with very low Q_{oss} and ideally zero reverse recovery charge. The totem pole therefore works best with GaN HEMTs. The H4 topology can be equipped with Superjunction and SiC Schottky barrier diodes for equally good performance. Forward looking, a bidirectionally blocking and conducting GaN HEMT is an interesting alternative for this topology.

Fig. 21 shows an analysis of the loss contribution from bridge rectifier, freewheeling element, and switches for both topologies.

The loss contribution from the freewheeling element is

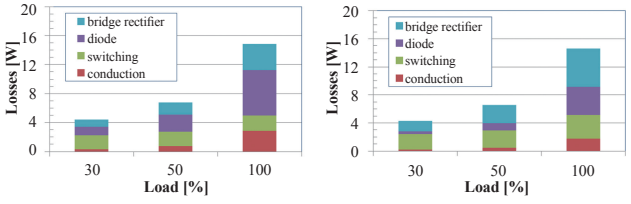

Fig. 21. Loss analysis of totem pole (left) and H4 topology (right), 1600 W, 230 V AC in, 65 kHz.

higher in the H4 topology due to higher forward voltage V_f of the SiC Schottky barrier diode in comparison to the losses of the GaN HEMT conducting in reverse direction in synchronous rectification mode. However, as the slow diode only conducts when switches S1/S2 are off, the contribution from the bridge rectifier is lower in comparison to the totem pole topology. Furthermore, the switching losses in the H4 circuit are lower as the switching losses of a Superjunction device switching against a SiC Schottky barrier diode is lower than of a GaN half bridge circuit operating at the same switching frequency. In total, the efficiency of both topologies is very similar across the entire load range with peak efficiency around 98.8% when operating at 65 kHz.

The totem pole topology can be further improved by replacing slow diodes D1 and D2 with power MOSFETs. This circuit is often referred to as full bridge totem pole. In this case no diode is left in the power flow path. GaN HEMTs are the best choice when operating in continuous current mode. Due to hard switching transients, the losses from both Q_{oss} and reverse recovery charge do not allow the use of Superjunction devices in this circuit. Therefore, we need to change the control strategy if Superjunction devices should be used in this circuit.

We need to ensure full removal of the reverse recovery charge and ideally discharge the output capacitance before turning on the device to eliminate all associated switching losses. This can be achieved by changing from Continuous Current Mode (CCM) into Triangular Current Mode (TCM) [21] as shown in Fig. 22.

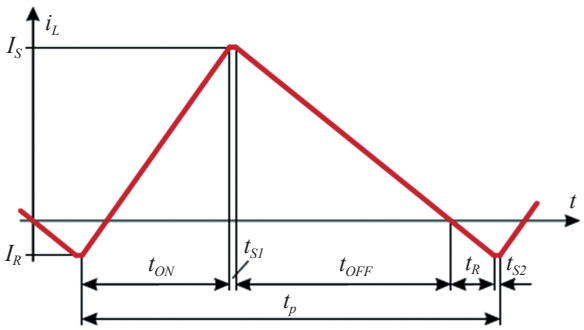

Fig. 22. Triangular current modulation scheme allowing zero voltage switching in half-bridge circuits.

Due to higher peak current from this modulation scheme it is advised to interleave two or more high frequency legs. The resulting circuits for continuous current and triangular current mode are shown in Fig. 23.

In, for example, positive line voltage, a positive current in inductor L1 is built up by turning on switch Q4 (vice versa in inductor L2 by turning on switch Q6). At the desired peak current Q4 is turned off with the current now freewheeling through the body diode of switch Q3, charging the DC link capacitor and returning through Q2. Switch Q3 can now be turned on at any time in a zero voltage condition parallel to the conducting body diode to allow synchronous rectification. After time interval t_{off}, the current reaches zero. Keeping Q3 further in the on-state will result in a change of the direction of current flow. Now the current in switch Q3 is positive. Keeping the device on for an interval t_R with:

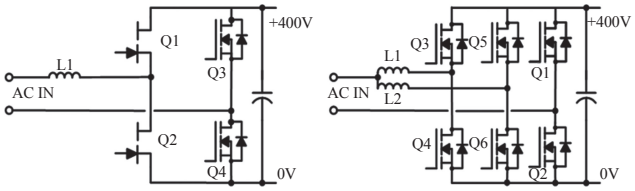

Fig. 23. Full bridge totem pole circuits using one high frequency leg with GaN HEMT devices in continuous current modulation (left) or two interleaved high frequency legs with Superjunction devices in triangular current modulation (right).

$$\frac{1}{2} \cdot I_R \cdot t_R > Q_{rr}(I) \tag{9}$$

ensures complete removal of the reverse recovery charge Qrr from switch Q3. The negative current I_R furthermore stores energy in inductor L1, which can be used to discharge the half bridge switching node between switches Q3 and Q4 prior to turning on Q4. Zero voltage switching can be achieved, if

$$\frac{1}{2} \cdot L \cdot {I_R}^2 > Q_{oss}(V) \cdot V_{DC} \cdot \tag{10}$$

It is noteworthy, that for zero voltage switching conditions in half bridge circuits the term $Q_{oss}*V_{DC}$ needs to be considered and not the energy term E_{oss} [22]. Referring to Fig. 11 the sum of the yellow and green coloured area needs to be taken into account.

Thus, when both equations are fulfilled, all switching losses related to Q_{rr} and Q_{oss} are removed. The devices are now achieving the extremely low soft switching losses as shown in Fig. 16 and Fig. 17 respectively. A peak efficiency above 99.2% has been demonstrated with this type of modulation scheme [23].

Due to the nature of the control scheme, the switching frequency varies strongly with load and across the AC sine wave; between full load / peak AC voltage and light load / zero voltage crossing, the frequency may change up to one order of magnitude. This strong frequency variation may create issues for the control. Furthermore, residual switching losses as shown in Fig. 17, are posing upper limits to the switching frequency.

The frequency swing can be limited by increasing the reverse current time, t_R, thus trading off switching losses versus additional conduction losses. A combination of partially hard switching and soft switching, thus combining the best aspects of both control schemes, has been proposed to overcome the limits of continuous and triangular current modulation, respectively [24].

The full bridge totem pole achieves in contrast same or better peak efficiency with great simplicity of control. Fig. 24 shows the measured efficiencies of half bridge and full

bridge totem pole configurations.

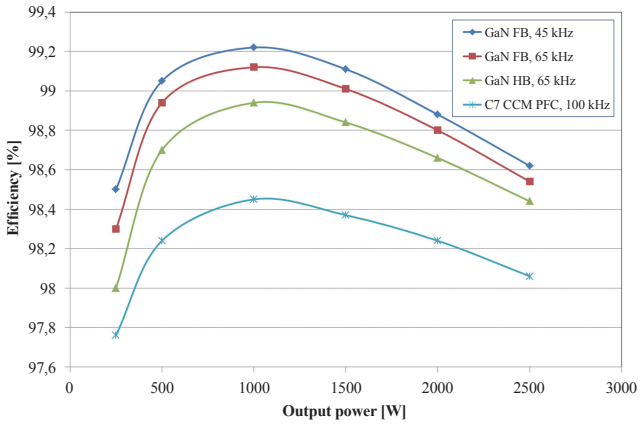

Fig. 24. Measured efficiencies for various totem pole configurations (half bridge, full bridge) using e-mode GaN HEMTs in comparison to the "classic" CCM PFC stage based on Superjunction and SiC Schottky barrier diode.

With just two 70 mΩ GaN HEMTs, a peak efficiency above 99% can be achieved in the full bridge totem pole circuit using two additional 35 mΩ Superjunction devices as low frequency switches. Lowering the switching frequency to 45 kHz allows greater than 99% efficiency from a load range of 20 to 70% of the full load.

Even though we discussed only power factor correction in this section, the underlying concept can be transferred to many applications in power electronics.

V. Conclusion

The comparison of different power device concepts is only meaningful in combination with their best matching circuits. We showed that both the latest generation of Superjunction devices as well as wide bandgap devices can achieve peak efficiencies above 99% in, for example, non-isolating power factor correction applications. While the control concept for silicon based power devices is more challenging, circuit and control for wide bandgap power devices is relatively simple and straight forward.

Both silicon and wide bandgap power devices have significant potential to further lower on-state resistance and correspondingly the cost of the fabricated die. We showed that Superjunction devices achieve best performance with SiC Schottky diodes as freewheeling element, while wide bandgap devices are very efficient in hard switching half bridge circuits, too.

In soft switching applications, GaN HEMTs with their unique device properties, have the potential towards very high switching frequencies, while silicon-based counterparts are limited to low and moderate switching frequencies.

VI. Acknowledgment

I would like to express my gratitude to many colleagues who contributed to aspects of this article. Without their knowhow and support this article would not exist. Special thanks go to Eric Persson and Matteo Kutschak for discussions on the e-mode GaN HEMT and application circuits and to Dr. Oliver Blank for discussions on the field plate concept.

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Review of Power Semiconductor Device Reliability for Power Converters

Bo Wang, Jie Cai, Xiong Du, and Luowei Zhou

***Abstract*—The investigation shows that power semiconductor devices are the most fragile components of power electronic systems.Improving the reliability of power devices is the basis of a reliable power electronic system, and in recent years, many studies have focused on power device reliability.This paper describes the current state of the art in reliability research for power semiconductor devices, mainly includes failure mechanisms,condition monitoring, lifetime evaluation and active thermal control.Among them,condition monitoring technology are classified and summarized by the failure mechanism and the change rules of characteristic quantities; The method of lifetime estimation isillustrated from the practical point of view;Methods of active thermal control are classified and summarized from the two ideas of reducing loss and loss compensation which are refined by the principle of realization. At last, this paper draws the existing problems and challenges of power devices reliability studies.**

***Index Terms*—Active thermal control, condition monitoring, failure mechanism, lifetime evaluation, power device, reliability.**

I. Introduction

POWER electronic system has high energy conversion efficiency and controllability[1],it has been widely used in aerospace, industrial automation, transportation, renewable energy power generation and other fields which require the highly reliability [2]-[5]. In these fields, the power will fluctuate in a large range [6]-[8], the reliability of power electronic systems with the harsh operating conditions are far less than traditional power equipment. Power semiconductor devices are the core component of power electronic system, and it is also one of the most fragile components in power electronic system [9], so that power device has a significant effect on the reliability of the power electronics system.Thereby, improving the reliability of power devices is one of the focus of power electronics studies. At present, the research on the reliability of power devices mainly includes failure mechanisms, condition monitoring, life estimation and active thermal control etc. As shown in Fig. 1, the study of failure mechanism is the basis of power device reliability research; Condition monitoring and active thermal control are the implementation means to improve the reliability of power devices; Accelerated aging test and lifetime estimation are the verification methods.

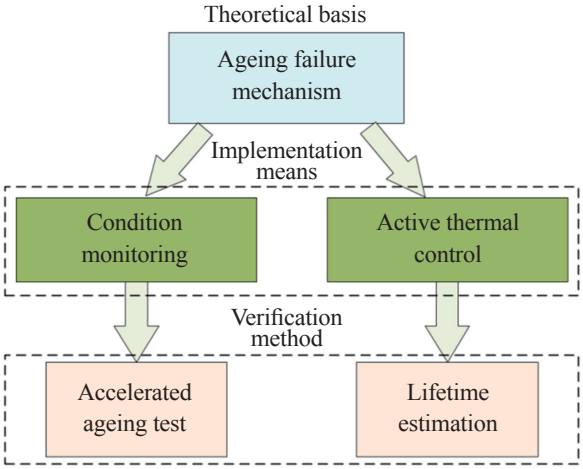

Fig. 1. The main research contents of the reliability of power devices.

Condition monitoring is one of the implementation means to improve the reliability of power devices, it means the health status of power devices is monitored by characteristic quantities in real-time,it enables timely maintenance to prevent the accident shutdown.The studies of condition monitoring are based on the failure mechanism which can be used to find the characteristic quantities and their change rules, and the change rules can beverified by accelerated aging test. Due to Insulated Gate Bipolar Transistor (IGBT) module is the most widely used in power devices, many studies of converter condition monitoring are mainly around IGBT [10]-[12], a great variety characteristic quantities of IGBT are proposed, the results of these studies are discussed in this paper. Active thermal control is another way to improve the reliability of power devices. The main factors causing aging failure of power devices are thermal stresses which are caused by the means temperature and temperature fluctuations.Active thermal control reduces the means temperature or temperature fluctuations by controlling the loss-related variables, thus reducing the thermal stress of power devices.Although the purpose of active thermal control is to improve the power devices lifetime, active thermal control should take account to the costs involved and make a trade-off between them.Due to the longer service time of power devices, the feedback of active thermal control from the practical application also longer. Therefore, life estimation is generally used to design active thermal control and verify

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the effect of active thermal control. What's more,customers can obtain the lifetime information by lifetime estimation to proper maintenance; manufacturers can make a new design to increase the lifetime of the power devices by lifetime estimation. The method of lifetime estimation is illustrated from the practical point of view in this paper.

In summary,the studies offailure mechanisms, condition monitoring, lifetime estimationand active thermal control have great significance for improving the reliability of power devices. This paper reviews these studies, Section II summarizes the main failure mechanism and failure modes of IGBT modules; Section III summarizes the current condition monitoring method from different point of view; Section IV summarizes the methods of life estimation and the usage method is illustrated; Section V summarizes active thermal control,refines the basic ideas of active thermal control methods and classifies them accordingly; And section VI draws the conclusions and challenges.

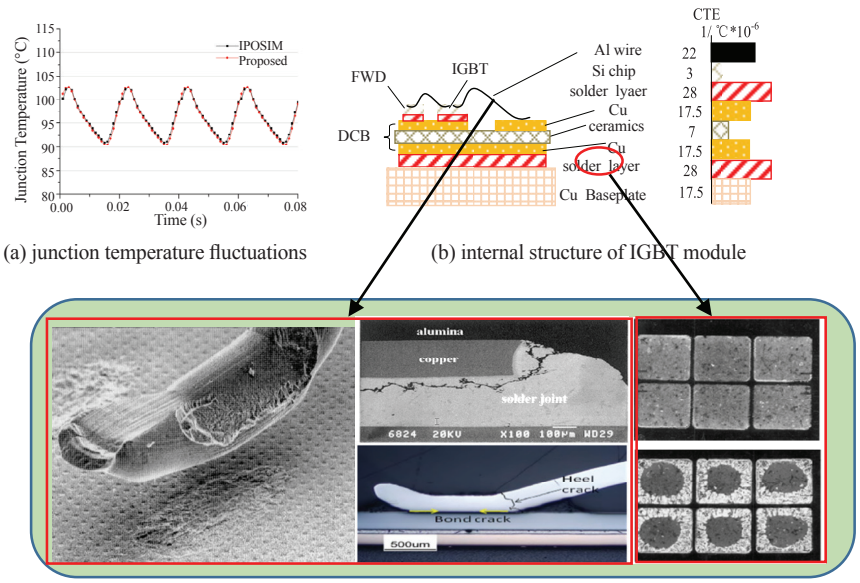
II. Failure Modes and Mechanism of IGBT Modules

At present, IGBT modules are widely used in high-power occasions. Its relatively low reliability is mainly attributed to its operation feature of dealing with a wide-range random power fluctuations during a long period.Statistics have shown that power converter is one of the most fragile part of the new energy equipment[2]-[5], among them the IGBT modules are also the most fragile part. The failure modes of it can generally be separated into two categories: chip-related failure and packaging-related failure. The chip-related failure can mainly attributed to the catastrophic failures. In the operation of IGBT modules, transient over-voltage, over-current, electrical-over-stress etc. such causal factors could cause catastrophic failures. However, due to their short transient process, these failures are include in the protection category and excluded from the focus of reliability research.

For silicon chip modules, the current research of the reliability research focus more on the package-related failure. The package structure of IGBT module can also be separated into categories: bonding wire structure and press-packaging structure. Between them, the press pack high-power devices, which have a higher reliability than wire-bond devices, are not discussed in this paper.

For the typical multi-layers wire-bond module package device as Fig. 2 shown, when the converter deals with a wide range of random fluctuating power, the power fluctuation causes the power device to withstand the shock of thermal cycle for a long time. The temperature fluctuates repeatedly during the thermal cycle. Due to the differences of mechanical and electrical characteristics of multi-layers, most heat loss transfer vertically downward and the temperature gradient arises from top to bottom within the modules resulting in alternating thermal and electrical stress. The alternating thermal and electrical stress and the bending stress of the bond wire itself, resulting in the crack between the aluminum lead and the silicon chip and gradually spread, and eventually lead to bond wire lift off and solder layer fatigue. Therefore, the IGBT internal temperature fluctuations and the unmatched CTE (thermal expansion coefficient) of different materials leading to alternating thermal and electrical stress, is the root cause of ageing failure. Research shows that the fast power cycling (time period is tens of seconds) and higher temperature swing ($\Delta T > 100$ K) leads to wire-bond failure, while the slow power cycling (time periodis several minutes) and lower temperature swing ($\Delta T < 80$ K) leads to solder fatigue related failures [9].

The failure mechanism of the IGBT modules in the converter mainly includes: bond wire fatigue, aluminum recon-



(a) junction temperature fluctuations

(b) internal structure of IGBT module

(c) main failure mechanism

Fig. 2. The internal structure of wire-bond package IGBT modules and main failure mechanism.

struction, solder fatigue and gate oxide degradation [10]. Among them, the aluminum bond fatigue [10], [20] and solder fatigue [21] are the two main failure mechanism of IGBT modules. The aluminum bond wire fatigue including bond wire lift off and heel cracking is caused by the temperature fluctuation and unmatched CTE at the lead-to-chip connection point [12], [22]. The solder layer fatigue refers to the phenomenon of solder cracks and holes under long-term work due to CTE mismatch of the solder connection between the silicon chip and the baseplate [21]. Failures such as solder layer fatigue cracks, cavity and bond wires lifting off or breaking lead to the changes of IGBT thermal, electrical characteristics as well as the degradation of reliability. Thus, failure mechanism is the basis of reliability research of power device.

III. Condition Montitoring Methods of IGBT Modules

A. General Idea of Condition Monitoring Method

Condition monitoring of IGBT modules refers to the process of extracting the information reflecting the health status but without interrupting its normal operation simultaneously. In fact, this process can be achieved by monitoring the operating status, and then determine the health level of the device, and finally evaluate the health condition. Thus, systematic maintenance and optimization repair based on condition monitoring can be achieved.

The failure modes of the IGBT modules can be separated into two aspects: sudden failure and aging failure. The sudden failure is instantaneous and unpredictable, belonging to the scope of protection [13]-[15], is not in the discussion of this paper. The ageing failure of IGBT modules are due to long-term work in harsh environment which leading to bear the continuous impact of thermal mechanical stress. Finally, due to the thermal fatigue cumulative damage, the working performance of the module will degrade leading the module parameters or signal shift [16]-[17]. This failure mode is slow and inevitable, if not found in time, will eventually evolve into a catastrophic failure, especially for some high reliability applications will cause incalculable significant losses. Thus, health condition monitoring of the power converter and power devices is of great significance.

At present, a large amount of ageing precursor and monitoring methods has been put forward to monitor the health status of IGBT modules [18]. Some correlation evaluation of these method combined with the practical use is also carried out from serval aspects such as: the intrusion of converter, identification accuracy and on-line application. From the perspective of online application,it can be divided into three parts: on-line monitoring, quasi-on-line monitoring and off-line monitoring. It can also be divided into classical ageing-precursor, new ageing precursor, global variable and other precurso raccording to its different characteristics. However, few literatures indicate the general idea of converter condition monitoring. Based on the existing research, this paper concludes the general idea of condition monitoring method of IGBT modules. The basic idea is shown in Fig. 3.

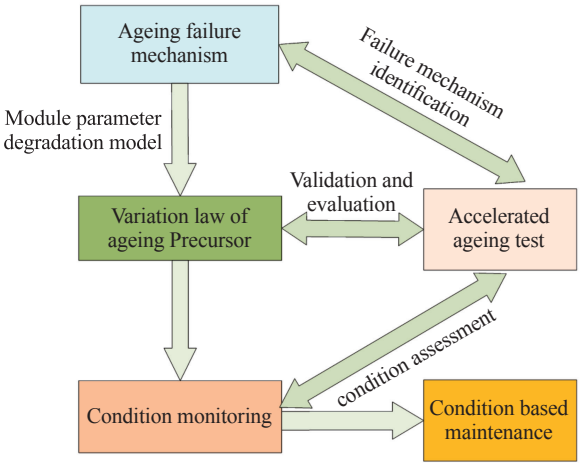


Fig. 3. General idea of condition monitoring.

From Fig. 3, the condition monitoring of the IGBT modules can be divided into three steps: the aging failure mechanism, the change characteristic of ageing precursor and the realization of the condition monitoring. The general idea can be described as follows:

1) Making a deep analysis of the aging failure mechanism and conducting the accelerated aging test based on the operating conditions and fatigue theory;
2) Modeling the IGBT module considering the degradation of parasitic parameters in the aging process and determining whether the feature can reflect the health condition and its changing trend based on the failure mechanism of IGBT module;
3) Verifying the changing characteristics of the module and making a comprehensive evaluation through the accelerated aging test;
4) Finally, based on a large number of aging test data, determine the certain correspondence between the precursor and the aging level of the device, determine the evaluation index of the health status of the module and finally use it for the health monitoring of the module.

Among them, the failure mechanism is the basis for the realization of converter condition monitoring. Accelerated aging test is an important means to reveal the physical failure mechanism and characteristic variation of the module, and the condition monitoring is the final means based on the terminal characteristics of the converter and power device. These three aspects will be described in detail below.

B. Condition Monitoring Indicators of IGBT Module

The health status of the IGBT module is closely related to its terminal characteristics. With the increase of power cycling of IGBT module, the thermal stress caused by the CTE mismatch will lead to the bond wire fatigue and the solder fatigue. The two main different failure mechanism will lead

to some changes in its terminal electro thermal characteristics, providing the reference and basisfor the IGBT condition monitoring. The key of IGBT health monitoring is to find the ageing precursor that reflects the health condition of IGBT module.With the aging process, the most significant change in the terminal characteristic is the increase in the on-state voltage drop and the thermal resistance. In order to analyze the variation rule of the terminal characteristic, the equivalent circuit model considering the packaging parameters are shown in Fig. 4, where R_{EW} and L_{EW} are the parasitic resistance and inductance of the bond wire respectively. R_{GW} and L_{GW} are the gate parasitic resistance and inductance respectively. C_{GC} and C_{GE} are parasitic capacitance. The aging of the module will lead the change of the bond wire parasitic parameters and gate parasitic parameters, resulting in the change of its terminal electrical characteristics.

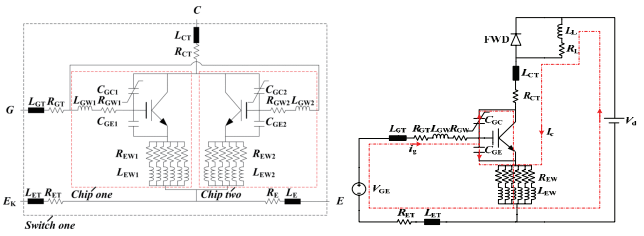


Fig. 4. The equivalent circuit model considering the ageing parasitic parameters.

$$
\begin{aligned}
I_{SC} &= \frac{\mu_{ni}\left(T_j\right)C_{OX}z}{2L_{CH}\left(1-\alpha_{PNP}\left(T_j\right)\right)}\left(V_G - R_{EW}I_{SC} - V_{TH}\left(T_j\right)\right)^2 \\
V_{ce\_sat} &= V_{ce\_0}\left(T_j\right) + I_C R_{EW} \\
\Delta V_{GE} &= L_{EW}\frac{dI_C}{dt} + I_C R_{EW}
\end{aligned}
\tag{1}
$$

Through the equivalent circuit model shown in Fig. 4, we can get some simple expression of partial ageing precursor (short circuit current I_{SC}, saturation voltage drop V_{ce_sat} and gate voltage change ΔV_{GE}) shown in the (1). It can be seen from the formula that the aging of the module will have an impact on the change of bond wire parameters which leading to the change of these precursors. Meanwhile, the aging of the solder layer will lead to the increase of the equivalent thermal resistance and the degradation of heat dissipation performance. Moreover, the increased thermal resistance also lead to the increased junction temperature(T_j) and thus affect the external characteristics of the module.Therefore, the aging of the solder layer not only leads to the increase of the thermal resistance directly but also leads to the increase of the junction temperature and the changing of the external electro-thermal properties in a certain degree. So it's significant to identify the variation law of the ageing precursor.

However, due to the complex packaging structure and physical structure of IGBT modules, it's hard to model the IGBT consider the ageing degradation parameters correctly and comprehensively. From the above partial precursors' formula and equivalent circuit, it can be seen that the precursors are often affected by multi-factors and have the characteristics of nonlinearity and strong coupling effects. Therefore,It is difficult to reveal its specific change rule and determine the certain failure level by direct theoretical analysis, but it is useful to identify whether the precursor are affected by ageing failure and its changing trend. Thus, after the simple theoretical analysis, it is still necessary to further evaluate the changing trends and validate the failure level through the accelerated aging test.

At present, a large amount of studies has been carried out on the characteristics of IGBT modules. The theoretical analysis and experimental results show that the saturation voltage drop (V_{ce_sat}), threshold voltage (V_{th}), transconductance (K_p), short circuit current (I_{SC}), *I-V*characteristics, switch transient signal (t_{on}、 t_{off}、 V_{GE}), gate parasitic parameters, case temperature (T_c), junction temperature (T_j) et al. can all be used as the indicators [12], [18], [22]. Part of the variation law of the ageing precursor with the ageing process is shown in Fig. 5.

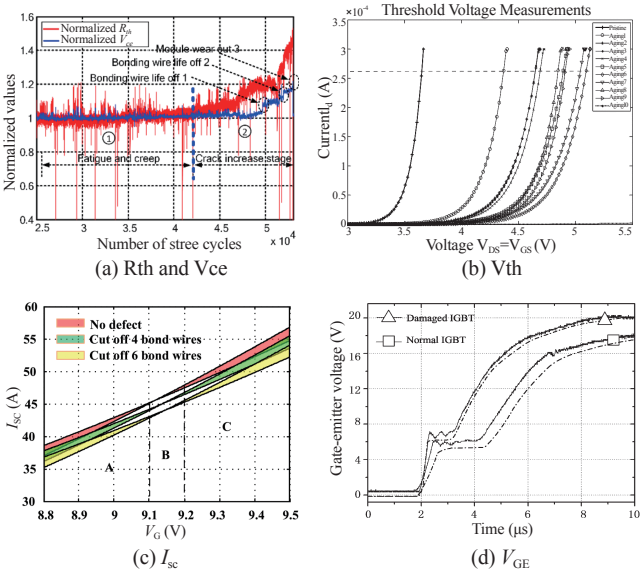


Fig. 5. Partial ageing precursors and it's variation law [23]-[26].

C. Analysis of Condition Monitoring Method of IGBT Module

As discussed above, different failure mechanism of IGBT module will lead to some changes in its terminal characteristics.Among them, the aging of the bonding wire will lead to changes in the electrical parasitic parameters within the module, the terminal electricalcharacteristics changes can be separated into two categories: steady characteristics and transient characteristics.Besides, the aging of the solder layer will mainly leads to the significant change of the thermal resistance and thermal characteristic of the module. These two categories will be described below separately.

1) Condition Monitoring of Bond Wire Fatigue

Because the bond wire is enclosed in the IGBT module, it

is difficult to observe its variation. In addition, the bond wire related parameters are extremely small, making it difficult to measure. Therefore, the study of aging failure of the bonding wire is still difficult. At present, the health status monitoring of IGBT module based on the bond wire fatigue can be mainly divided into two aspects: steady-state monitoring and transient monitoring. The steady-state characteristic quantity mainly includes V_{ce_sat} [23], [30], V_{th}, K_p, I_{SC} [25], R_{on} et al. [18], and the transient electrical characteristic mainly includes switching transient time (t_{on}, t_{off}) [12], [18], gate voltage current variation [26], [27] and so on.

In the field of steady-state condition monitoring, most research currently use V_{ce_sat} of IGBT module to achieve on-line monitoring [28], [29]. The V_{ce_sat} of the IGBT module increases with the aging process, so the health level of the IGBT can be monitored by monitoring the saturation voltage drop [6], [31]-[35]. However, V_{ce_sat} is nonlinear with the collector current I_c and the junction temperature. Therefore, it is necessary to test the IGBT module under specific conditions, which increases the difficulty of on-line application. Meanwhile, the variation of V_{ce} caused by ageing effects is generally only tens of millivolts, but the bus voltage is up to 100 volts or even kilovolt, which needs higher requirement of measurement equipment.Choi et al.[32], [33] proposes an on-line measurement method of the V_{ce_sat}, and the saturation voltage drop near the inflection point in the output characteristic curves is not affected by the junction temperature(-shown in the Fig. 6)[34], [35]. Therefore, the V_{ce_sat} near the inflection point measured at a specific current can accurately achieve bonding wire health monitoring, the V_{ce_sat} online measurement circuit and identification results are shown in Fig. 6.

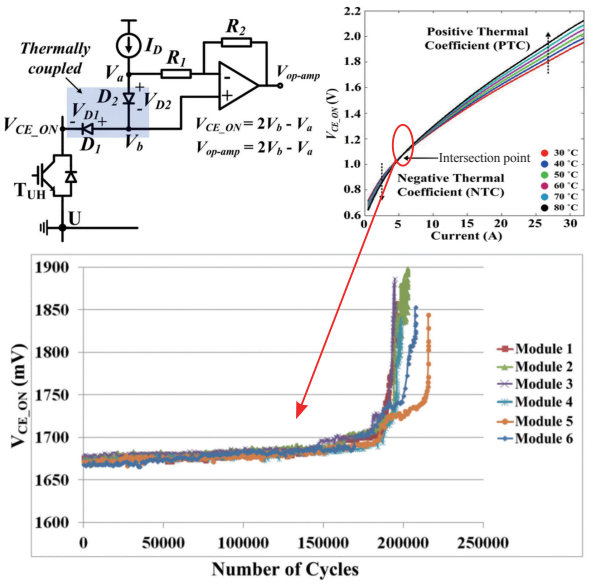


Fig. 6. On line Vce measurement circuit and Vce monitoring results at the infection point [34].

In the same way, Sun et al. [25], [36] propose the short-circuit current can be used as a precursor of the IGBT modules. The theoretical analysis and the experimental results shows that the short-circuit current near the inflection point of the transmission characteristic curves is not affected by junction temperature, bus voltage and complex working conditions. Thus, the short-circuit current under the specific driver voltage can directly reflect the health condition of IGBT module. The corresponding experimental resultsare shown in Fig. 7.

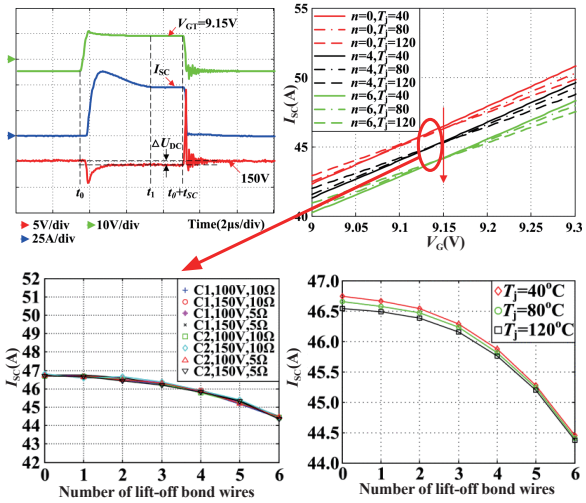


Fig. 7. Short circuit current measurement waveform and measurement results under different condition [36].

The two steady state monitoring method under specific measurement condition discussed above can both avoid the coupling influence of junction temperature and other parameters can reflect the health status of the bond wire well. Besides, the transconductance and threshold voltage of the IGBT module also change with the aging of the module [24], [37], [38], and the transconductance-based condition monitoring method is difficult to achieve on-line application due to the limitations of its specific measurement requirement. The monitoring method based on threshold voltage is divided into two types: static threshold voltage and dynamic threshold voltage [39], [40]. The static threshold voltage measurement requires the converter to be in the shutdown state, it is also difficult to achieve on-line measurement. The dynamic threshold voltage measurement needs to detect sudden change moment of I_c and V_{ce}, the measuring process can easily be affected by the noise factors. Besides, these two parameters are both affected by temperature, so the effect of junction temperature could not be ignored.

The condition monitoring of the IGBT module based on the transient characteristic is mainly based on the gate voltage or current signal, the gate parasitic parameter, the switching transient time and so on. Du and Zhou et al. [26], [27], [41] investigate the relationship between the gate signal and the health level of IGBT module. The relationship between the change of the gate signal and the aging state of the module is shown in Fig. 8. The study shows that the gate signal shows little difference unless a chip is damaged or all the bond wire on the chip lifting off in the multi-chip paralleled modules. Therefore, accurate identification of the

bond wire based on the gate signal could not be achieved,the identification accuracy is low.

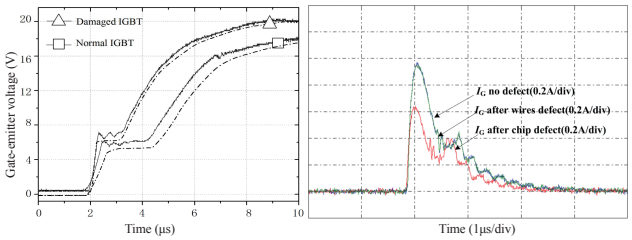


Fig. 8. The varies of gate signal at bond wire liftoff station [26], [27].

The switching transient time of the power device also changes with the aging of the power device [12], [18], [42], Brown et al. [43] proposed turn-off time(t_{off}) can effectively reflect the power device condition due to latching effect caused by ageing, the experimental results are shown in Fig. 9. Condition monitoring based on the switching transient time needs higher requirements for the measuring equipment, and it is easy to be affected by the complex factors such as junction temperature and complex working condition, the practical application is difficult.Besides, the condition monitoring based on the main circuit switching precursor is more invasive to the normal operation of the converter.

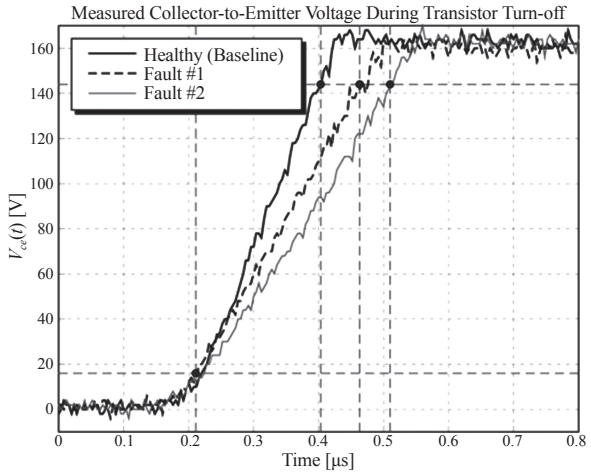


Fig. 9. Collector-Emitter voltage waveform before and after IGBT aging [43].

2) Condition Monitoring of Solder Layer Fatigue

The aging of the solder layer leads to the degradation of the module's thermal performance, directly causes the increase in the thermal resistance of the IGBT module, result in abnormal changes in the junction temperature and case temperature of the IGBT modules [44], [45]. So the thermal resistance, junction temperature, case temperature can be used as monitoring indicators.

The type of thermal resistance monitoring is generally divided into static thermal resistance and dynamic thermal resistance, the two measurements are basically the same. Generally, the static thermal resistance increases by 20% relative to the initial value is regarded as the failure criteria of IGB modules [46], and the dynamic thermal resistance curve will drifts after aging [47]. Therefore, monitoring of IGBT module thermal resistance can determine the health state of the IGBT module. Ji et al. [48] present an on board method to test the thermal resistance of IGBT module in off-line condition. The method requires the addition of measurement program and measuring equipment to realize the extraction of thermal impedance parameters after the converters completely shut down. Du. X et al. [49] propose a quasi-on-line thermal network parameter identification method of IGBT module based on the cooling curve of junction temperature. This method does not require additional heating current source, the measuring process can be conducted in the process of converter shut down without intrusion of the converter normal operation.

The junction temperature can also be used as an indicator for condition monitoring [10], [18]. However, due to encapsulation of IGBT module, it is difficult to achieve a direct measurement of junction temperature without modifying the package. On the other hand, indirect measurement of the junction temperature is possible. The junction temperature can be extracted through the terminal thermo-sensitive electrical parameters. Part of the typical thermo-sensitive electrical parameters are shown in TABLE I.

TABLE I
JUNCTION TEMPERATURE SENSITIVE PARAMETERS

Parameter	Definition
t_{diff}[50], [51]	Miller platform time
V_{eE}[52], [53]	voltage between the main emitter and the auxiliary emitter
$V_{ce.on}$[36]	saturation voltage
$V_{ge.th}$[40]	threshold voltage

Rodriguez-Blanco and Sundaramoorthy et al. [50], [51] point out that the Miller platform delay can be used as the characteristic of the junction temperature measurement, and the temperature sensitivity is 1.1 ns/°C-3.5 ns/°C.Luo et al. [52], [53] propose that the amplitude and turn-off delay time of the voltage V_{Ee} induced by the parasitic inductance between the main emitter and the auxiliary emitter of the IGBT module can also be taken as the characteristic of the junction temperature estimation of the IGBT module.

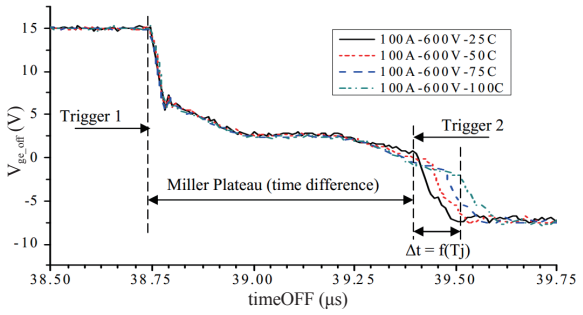


Fig. 10. Gate voltage turn-off signals at different temperatures [51].

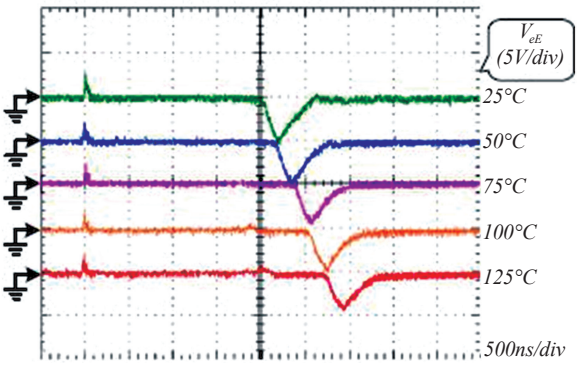


Fig. 11. VeE waveform at different temperature [52].

The case temperature can also reflect the health condition and junction temperature after dexterously treatment [54]-[56]. The change of the case temperature can reflect the aging state of the device [54], it's temperature distribution of at different location can both reflect the bond wire fatigue and solder layer fatigue of the device [55]. Besides, the mean values of the different chip case temperatures in the same module can be used to estimate junction temperature [56].

Finally, it is worth noting that the ageing parameters of the IGBT module are often affected by the coupling of multiple factors. Generally, almost all the precursor are affected by the junction temperature. In the actual converter operation, the solder layer of the aging will lead to abnormal changes in junction temperature, which has a significant effect on the bond wire monitoring parameters. At the same time, the aging of the bonding wire, aluminum reconstruction and other failure mechanism, will lead to increased loss of the module and thus lead to junction temperature and case temperature changes. Therefore, there are strong coupling effects among mutli-indicators. It is still unrealistic to rely on a single ageing precursor to realize the condition monitoring of the IGBT module and even the whole converter. Besides, how to avoid the influence of other factors when using the condition monitoring parameters and find characteristics that can reflect health condition of IGBT module more comprehensively is still of great importance. It is also the focus of future research to realize the more comprehensive monitoring of the health status of from the power device to the converter based a large amount of test data analysis and data fusion from actual converter operation.

IV. Lifetime Estimation

Junction temperature fluctuation is the main factor leads to power device failure, according to the failure mechanism. In the actual conditions of the junction temperature fluctuations can generally be divided into long, medium and short time scales. Among them, the long time scale means ambient changes which are slow changes; the medium time scale means low frequency junction temperature fluctuations caused by input and output power fluctuations of converters, such as random variation of wind speed in the wind power converter; the short time scale means fundamental frequency junction temperature fluctuations followed by the output frequency of converter. All of the junction temperature fluctuations at different time scales will consume the life of the power device, and the lifetime expectancy of the power device should be considered for multiple-time scales [57]. Usually the power device manufacturers provides the lifetime expectancy only under a single thermal load condition in the application manual[58], [59]. So the lifetime expectancy of power device in the actual conditions can not be obtained directly from the application manual, it is necessary to be estimated by lifetime estimation technique.

Customers and manufacturers of power devices want to estimate the lifetime of power devices under certain operating conditions. On the one hand, customers hope lifetime estimation can help to reduce the expense of conservative maintenance.On the other hand, lifetime estimation can also help manufacturers to design new devices, which can have a longer service life.What's more, life estimation is generally used to design active thermal control and verify the effect of active thermal control.This section reviews the present situation of lifetime estimation.

A. Junction Temperature Evaluation

The junction temperature evaluation is the fundamental of lifetime estimation of power devices. The methods of junction temperature evaluation are mainly classified into two categories: the junction temperature measurement and the junction temperature estimation.The junction temperature measurement is divided into direct measurement method and indirect measurement method, in which optical method and physical contact method belong to direct measurement, and thermo-sensitive electrical parameters(TSEP) belongs to indirect measurement. The optical method is non-contact,which measures the chip temperature of opened module by Infrared Radiation camera (IR) [60]; physical contact requires the installation of temperature sensors on chip surfaces, such as the thermocouple or the fiber [61]. These two methods are generally used in labs. The TSEP such as saturation voltage, gate voltage, threshold voltage, short circuit current, etc. can be used to monitor the junction temperature [62]-[67]. It can be applied online, but there are still some issues such as accuracy, expensive, vulnerable to interference, so that it has not ready to wide application.

At present, the most widely used method of online junction temperature evaluation is the junction temperature estimation based on the thermal network [68]-[74].This method is implemented by two steps, firstly, the loss of power devices is calculated according to the operating conditions, and then the junction temperature is calculated by the case temperature and the thermal network.The thermal network parameters can be extracted by finite element method, analytic model method, extended description function method, polynomial fitting, equivalent RC thermal network etc. [75]-[77]. The accuracy of the estimation is mainly limited by accuracy of the loss calculation. In addition, the thermal network parameters will change with power devices ageing, it also has

a great influence on the accuracy of junction temperature estimation [78]. Some other methods for junction temperature estimation have been reported.The temperature field distribution of the chip is calculated by the finite element modeling method [79]; in [80], the transient junction temperature is calculated by Fourier series; literature [81] uses finite difference method to solve the 3-D heat distribution of devices etc. The above three methods are only suitable for simulations and are not suitable for the online calculation.

B. Lifetime Model

Existing life models can be divided into two categories: analytic models and physical models. Physical models combine material strain analysis and aging data, it can deeply reflect the physical mechanism of lifetime, but the expression is complex and the parameters are difficult to obtain. Analytical models are established only by fitting the aging data. It does not reflect the physical relation of the aging process, but it is simple for application.The analytical model is the most widely used in life estimation, the studies of analytical models are shown as follows.

The main factors affecting the lifetime of power devices are the means junction temperature and junction temperature fluctuations according to the failure mechanism. In the manual of the SEMIKRON semiconductor, the relationship among the means junction temperature, junction temperature fluctuations and the number of IGBT thermal cycles is shown in Fig. 12 [57]. Analytical models based on the two factors, and the common analytic models are as follows: Coffin-Manson Model, Lesit Model, Norris-Landzberg Model and the most widely used Bayerer Model.

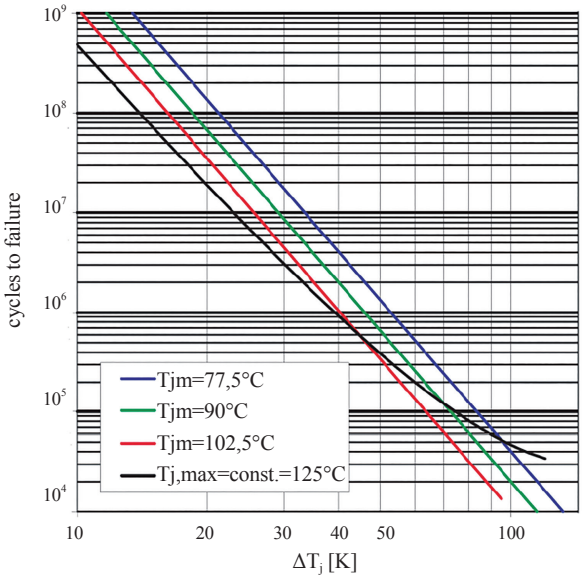


Fig. 12. Temperature cycle capability characteristic Nf for Standard SEMIKRON IGBT modules [57].

Coffin-Manson model only takes account of the fluctuation of the junction temperature ΔT_j, it can be expressed as follow [82]:

$$N_f = \alpha(\Delta T_j)^{-n} \tag{2}$$

Here α,n can be fitted by simulation or cyclic experiment. The model only suits to the condition what is the temperature fluctuations less than 120 °C, and there is only one factor is taken into consideration that results the low accuracy.

Another mathematical formulation of the Coffin-Manson model which besides the temperature variation ΔT_j takes also into consideration the medium temperature Tm is shown in (3) [83].

$$N_f = a(\Delta T_j)^{-n} e^{E\alpha/(kTm)} \tag{3}$$

Here k the Boltzmann constant and E_a the activation energy parameter.

On the basis of Coffin-Manson model, the influence of cycle frequency on the life is considered in Norris-Landzberg model [84], it can be written as:

$$N_f = Af^{-n_2}(\Delta T_j)^{-n} e^{E_\alpha/(kT_m)} \tag{4}$$

Here f is the thermal cycle frequency; n_1 and n_2 are constant fitted by experimental data.

In addition to the medium temperature and temperature fluctuations, the the Bayerer model also takes into account the heating time ton, the load current I, the bonding wire diameter D and the module block voltage V [85], it can be written as follow:

$$N_f = K(\Delta T_j)^{-\beta_1} e^{-\beta_2/(T_{jmax}+274K)} t_{ton}^{\beta_3} + I^{-\beta_4} + V^{-\beta_5} + D^{-\beta_6} \tag{5}$$

Here T_{jmax} the maximum value of junction temperature, K and β are constant fitted by experimental data.

C. Miner Linear Accumulation Damage Theory and Rainflow Counting Algorithm

The junction temperature of the power devices varies with the load variations, which leads to the cyclic thermal stress within the power devices, and fatigue failure of the power devices is the result what is a damage caused by accumulation of the thermal stress. Thereby, estimating the lifetime should consider the accumulation of damage. Miner linear accumulation damage theory is very simple, and has been widely used in lifetime estimation of power devices [86]. Lifetime estimation formula based on Miner linear cumulative damage theory can be written as:

$$T = \frac{1}{D} \tag{6}$$

Here T is the number of cycles, D is the cumulative damage for the n power cycles which is defined as follow:

$$D = \sum_{i=1}^{n} \frac{n_i}{N_i} \tag{7}$$

Here D is the cumulative damage, n_i the number of cycles in the stress range i and N_i the number of cycles to failure. When $D = 1$, the device fails.

In order to count the number of cycles, the Rainflow Counting Algorithm is employed [87]. The Rainflow Counting Algorithm is a statistical method for analyzing the process of random load,the principle of counting is carried out on the basis of the stress-strain behavior of the material as shown in Fig. 13. It combines load reversals in a manner that defines a cycle as a closed hysteresis loop. Each closed hysteresis loop has a strain range and mean stress associated with it that can be compared with the constant amplitude [88].

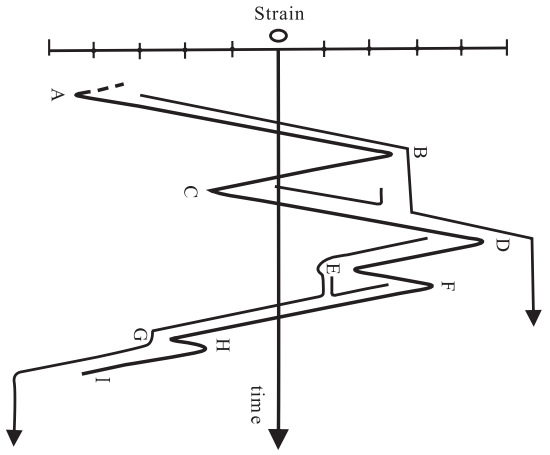


Fig. 13. Stress-strain cycles [88].

The flow of lifetime estimation is shown in Fig. 14. Firstly,extracting the junction temperature curve of the power device through converter mission profile.Secondly, gathering statistics of the types of thermal cycle and the number of each thermal cycle by Rainflow counting algorithm.Thirdly, calculating the total number of cycles that the power device can withstand for each thermal cycle through the life model. At last, the lifetime expectancy of the power device can be estimated based on Miner linear accumulation damage theory. In order to verify the effect of active thermal control, the lifetime expectancy can be calculated with and without active thermal control respectively by lifetime estimation technique, under the same operating condition.

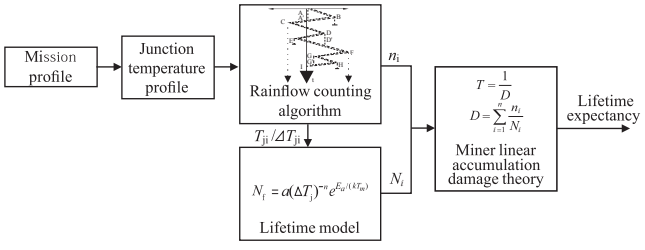


Fig. 14. The flow chart of lifetime estimation.

V. Active Thermal Control

In recent years, reports of active thermal control for power devices gradually increased, which is in order to reduce the thermal stress on the power devices,active thermal control is another way to improve the reliability of power devices. In those reports, methods of active thermal control can be divided into two categories by the basic ideas, which are refined by the principle of realization.The first kind of active thermal control method is based on the loss compensation, this kind of method is mainly for the junction temperature fluctuations caused by the converter input and output power changes, i.e. low frequency junction temperature fluctuations. Its basic idea is that when the power of converter is reduced, the loss of the power device can be compensated in real-time by controlling the loss-related variables, such as increase switch frequency, thus the magnitude of the junction temperature fluctuation is reduced.The mainly problem of the loss compensation is that it will increase the total loss of power devices and improves the average junction temperature of power devices.The second kind of active thermal control method is based on the loss reduction. Its basic idea is that according to the thermal load distribution of power devices divides the work interval of converter, when power devices work into the serious thermal load interval, the total loss can be reduced by decreasing the switching times,such as reducing the switching frequency etc. to reducing the thermal stress of power devices.This kind of method can reduce both the average junction temperature and junction temperature fluctuation at the same time.The mainly problem of the loss reduction is that the quality of the converter output will be reduced with decreasing the switching times, such as the converter output ripple current will increase with reducing the switching frequency. And if the converter is designed with minimum loss, this method cannot be applied. The latest researches progress of active thermal control are respectively outlined by the two basic concepts as follow.

A. Loss Compensation

Loss compensation is mainly for smoothing low frequency junction temperature fluctuations. The basic idea of loss compensation is that the loss-related variables such as switching frequency are usedto compensate for the internal loss fluctuations of power devices which is caused by the fluctuations of converter input and output power. As a result, loss compensation will increase the total loss of power devices, but the overall fluctuation of junction temperature can be significantly reduced with slightly increased mean temperature level. According to the lifetime models in Fig. 12, this is a more optimal loading condition with regard to lifetime extension. Loss compensation does not affect the fundamental frequency temperature fluctuation. There is no current flows through the power devices in the half-sinusoidal period, so that the base frequency junction temperature fluctuation is difficult to smooth by loss compensation. The methods of junction temperature on-line measurement are not yet ready wide application, the junction temperature estimation with the thermal network is used to loss compensation, and the quasi-close loop control such as look-up table is applied.

A control scheme based on the junction temperature estimation is proposed as shown in Fig. 15 [89]. In the scheme the resulting junction temperature are calculated by the thermal network with the P_{loss}. Information such as load current i_c, the DC-link voltage V_{dc} and the case temperature T_c are measured in the physical system, they are taken to determine the collector to emitter voltage drop V_{ce} and the switching energies E_{on} and E_{off} by the characteristic curves of power devices. They can be used to achieve an estimation of the conduction losses P_{cond} and the switching losses P_{sw}. The thermal controller sets the switching frequency independent from the calculation result of T_j. To filter the junction temperature's fluctuation of the fundamental frequency f is used as an input.

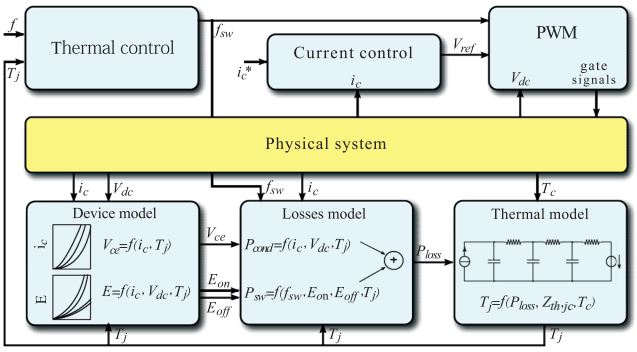
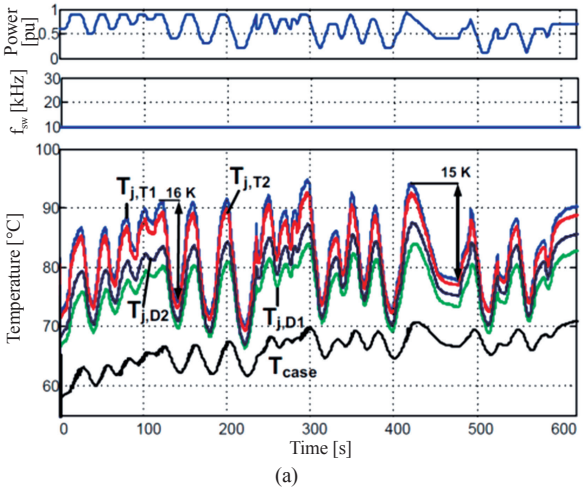


Fig. 15. Block scheme of the thermal control system [89].

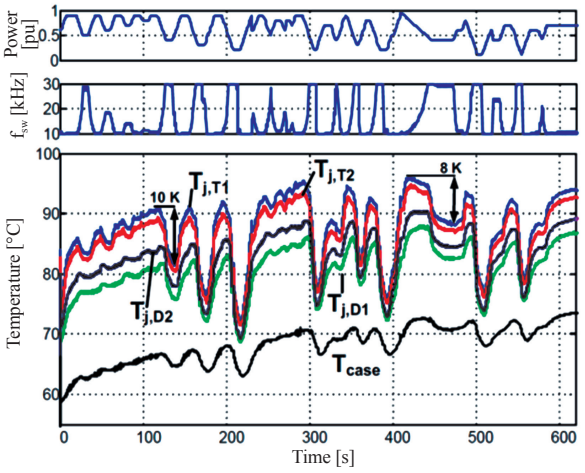
1) Switching Frequency Control

The switching frequency is a loss dependent variable, which mainly affects the switching losses of power devices. The junction temperature of power devices reduces with the decreasing of load, then the switching losses are adjusted by increasing the switching frequency, so that the junction temperature fluctuation can be smoothed.This method does not need additional hardware [89]-[91].

A loss compensation method with controlling the switching frequency is proposed [90], and the control method of Fig. 14 is employed.The junction temperature with fixed switching frequency and with the active thermal control are shown in Fig. 16, they are acquired by a single-phase inverter. It can be seen that the maximum junction temperature fluctuation of the power device is reduced from 15 K to 8 K.



(a)



(b)

Fig. 16. Experimental result of the switching frequency control [90]:(a) Constant switching frequency. (b) Active thermal control using switching frequency variation between 10 kHz and 30 kHz.

2) Gate Control

Gate control is also a method of switching losses control. Gate voltage and the driving resistance have an effect on loss, the relationship among the gate voltage, resister and power devices lifetime has been estimated according to a real field mission profile [92]. Gate control does not affect the current ripple of the converter output, but gate control requires additional circuit.

Gate drive voltage affects switching loss and the saturation voltage, consequently the loss of power devices can be controlled. A temperature dependent driving strategy for power transistors is proposed which aimed at counterbalancing temperature related increases in their on-state resistance and power losses by a corresponding increase of the amplitude of the applied driving level [93]. But this method requires a precise control of the voltage level, which is too difficult to implement. This problem has been improved by [94]. The two-step gate drive unit is employed in [94], which divides the gate voltage into two levels. The switching loss and conduction loss of GaN can be adjusted by controlling the low level of time, at the same time the junction temperature is smoothed as shown in Fig. 17.

3) Reactive Power Circulated

In the parallel converter, the reactive power delivered can significantly influence the loading of components, and it is not restricted to the available mechanical/electrical power processed by the converter system, so that it is suitable to achieve active thermal control [95]. The reactive power will not only modify the phase angle between the output voltage and current of converter, but also modify the current amplitude flowing in the power devices, which are all related to the power loss and thermal loading of power devices. By introducing certain amount of underexcited reactive power

to heat up the device during the low power period, the overall fluctuation of device temperature can be significantly reduced.Compared to switching frequency control or gate control, the disadvantage of reactive power cycling is that it can only be applied in the parallel converter system and the thermal load of the diode is increased.

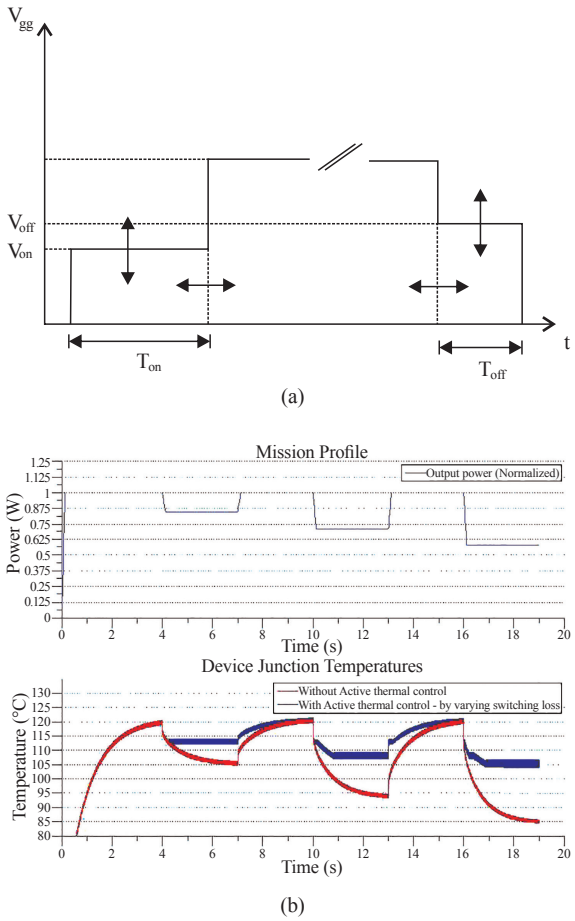


Fig. 17. Gate driver for the active thermal control of a DC/DC GaN-based converter [94]: (a) Waveform of the two-step gate driver; (b) Simulation results of active thermal control strategies.

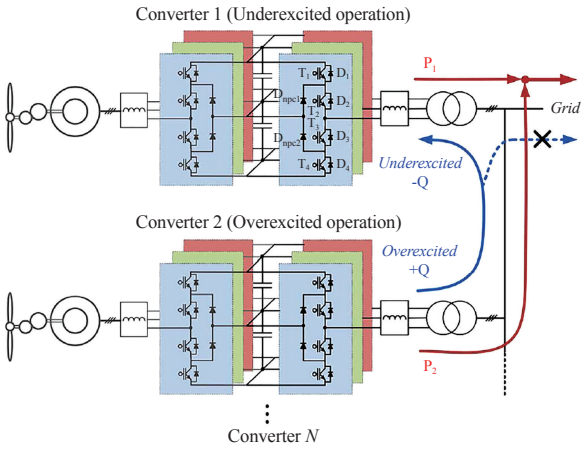


Fig. 18. Reactive power circulated in paralleled wind power converters [95].

4) Power Sharing

The existing solutions for paralleled converter operation focus on equal current sharing among the converters. Reference [96] provides a method of various publications for equal power distribution in the paralleled power electronics building blocks. The power distributions among paralleled power electronics building blocks can be adjusted by the junction temperature to improve the efficiency and the lifetime of semiconductor. The disadvantage of power sharing is as same of reactive power cycling, it also can only be applied in the parallel converter system.

B. Loss Reduction

The basic idea of loss reduction active thermal control is that the losses of power devices will be reduced by decreasing the switching times in the worst working environment. It can be achieved by adjusting some operating conditions, as dc-link voltage, modulation strategy and switching frequency, as a result the thermal stress on power electronic devices is reduced, the control flow chart of loss reduction is proposed as shown in Fig. 19 [97].

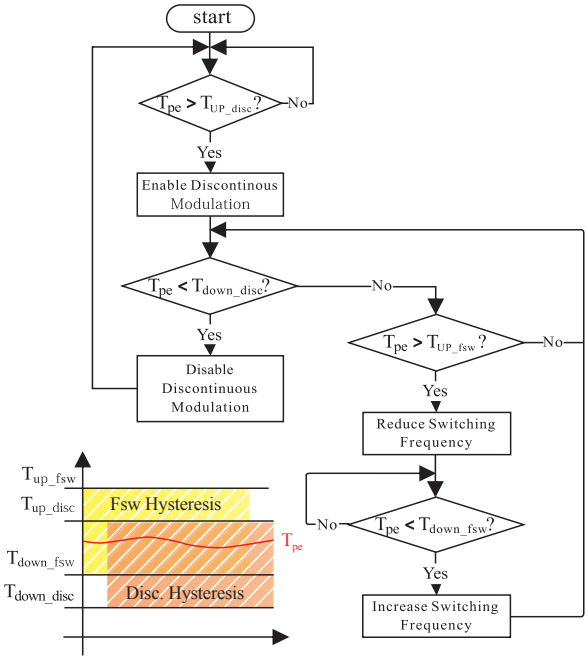


Fig. 19. State diagram for the hysteretic control[97].

1) Switching Frequency and Current Limit

Switching frequency hysteresis control is one method of loss reduction, the switching frequency is reduced to limit the junction temperature, in addition the load current is limited to prevent the junction temperature overheating [98]-[101]. In [102], a new approach for junction temperature estimation is investigated using an enhanced-Luenberger-style closed-loop observer. This technology can then be used as a sensor replacement technique for estimating junction tem-

perature using a baseplate temperature sensor in the module, and also perform the active thermal control by switching frequency and current limit regulation as show in Fig. 20.

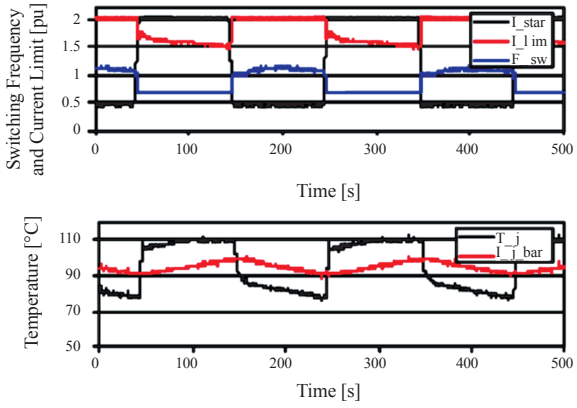


Fig. 20. Comparison of junction temperature with and without switching frequency control [102].

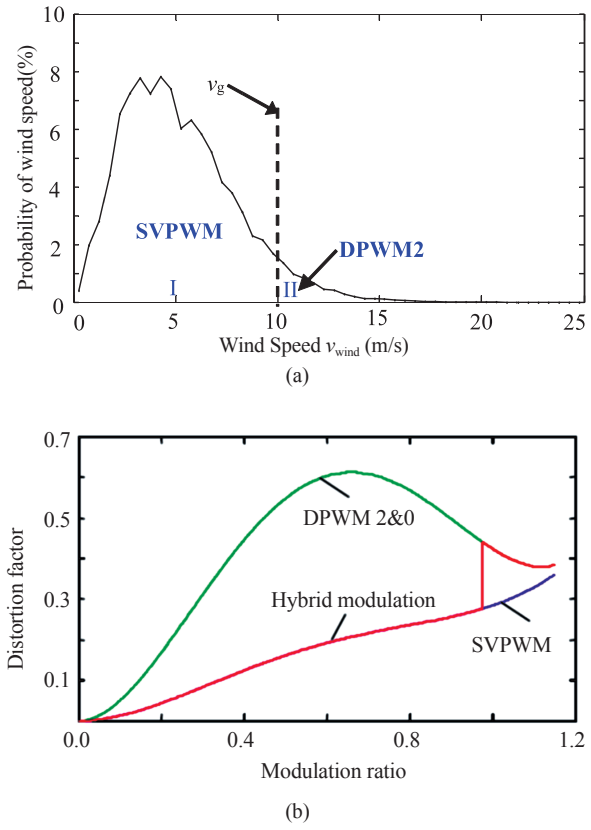


Fig. 21. The hybrid modulation method [105]:(a) the control strategy;(b) the influence of the power quality.

2) Modulation Strategy

Space vector modulation can be divided into continuous pulse width modulation (CPWM) and discontinuous pulse width modulation (DPWM). Compared with CPWM, the switching loss of the device is low if the DPWM is adopted, so that the junction temperature fluctuation is low. The 60° discontinuous pulse width-modulation strategies allow better thermal performance and increase the estimated lifetime of the converter compared with SPWM modulation, when FT60 modulation is adopted, the average junction temperature of the device is lower, thereby improving the converter energy conversion efficiency [103], [104]. Although DPWM can improve the lifetime of power devices, it will reduce the

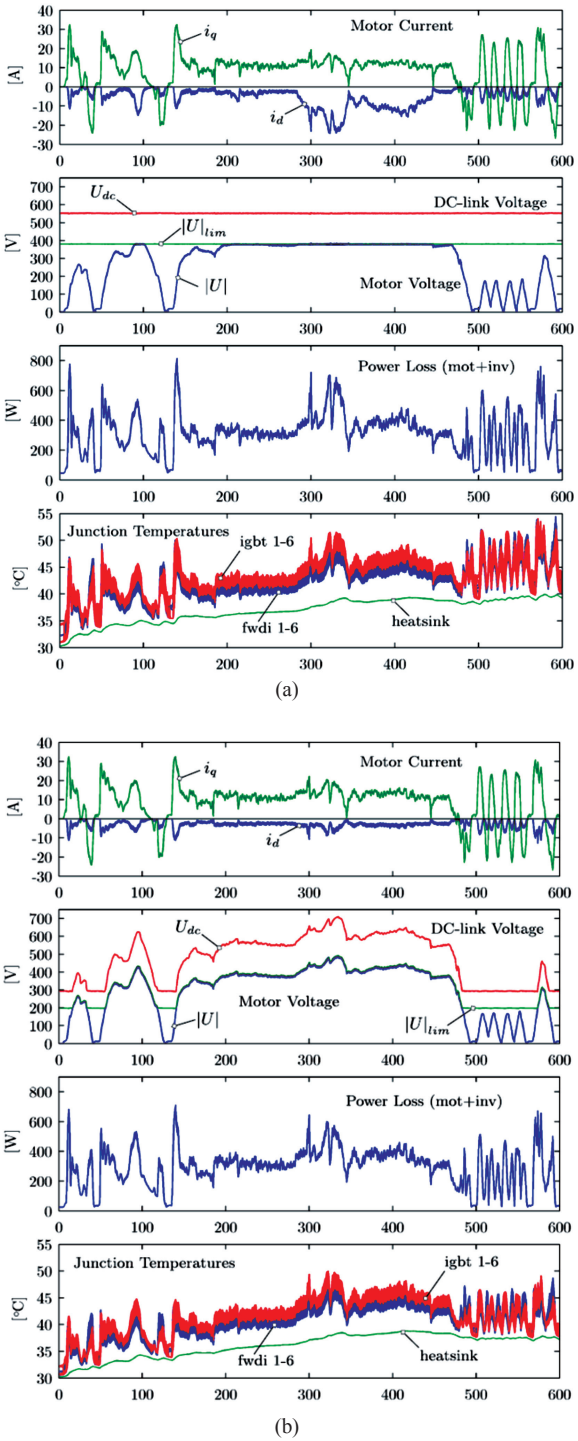


Fig. 22. Dynamic DC-link voltage adaptation for thermal management of traction drives [106]: (a) Fixed DC-link voltage: Udc = 550 V; (b) Variable DC-link voltage: Udc = [290...750] V.

power quality of converter.In order to maximization reduction the impact of DPWM on the power quality, in the wind turbine system, a hybrid modulation method based on the wind speed distribution probability is proposed. This method makes the converter working mainly with the CPWM modulation, and the DPWM will be employed if the operating condition is worst, the control strategy and the influence are shown in Fig. 21 [105].

3) DC-link Voltage Regulation

In the traction drives with PMSM, the DC bus voltage is adjusted dynamically to reduce the loss [106]. The bus voltage level is adjusted to the required PMSM terminal voltage in each operating point. Consequently, switching losses can be reduced at low speed by lowering the bus voltage. At high speed, the voltage level is boosted and field-weakening operation and the associated additional losses are avoided. The junction temperature with the fixed DC-link voltage and with the variable DC-link voltageare shown in Fig. 22. It can be seen that the average junction temperature and junction temperature fluctuations are significantly reduced.

C. Others

In addition to the above categories, there are other methods of active thermal control have been reported, and all of their purpose is to reduce the junction temperature fluctuations.In the three-level neutral-point-clamped converter, the inner hexagon of the space vector diagram have switching redundancies which can be adopted to active thermal control. These switching redundancies provide the control flexibility to modify the current paths flowing in the power devices, and thereby modifying the conduction losses of the device. This feature is especially interesting for the ride-through operation during the grid faults for grid-tied converters, or the start-up operation of motor drives, where the voltage reference vector is normally low in amplitude and it is located in the inner hexagon [107], [108].The algorithm of a DC/DC converter for photovoltaic system was actively modified in order to limit the maximum junction temperature derivative in the presence of irradiation changes where the algorithm modifies the Maximum Power Point Tracking embedded in this kind of converters [109]. In fast varying irradiance environments, it is demonstrated in Fig. 23 to reduce the thermal cycling by not tracking very fast irradiance variations, which only slightly increase the harvested energy, but cause damage to the components. If there are no fast variations, the maximum power point is normally tracked by harvesting the maximum energy, as it is commonly done. To mitigate the effects of the ambient temperature variations, a regulation strategy of cooling is reportedin [110], which the speed of the fan is controlled.

The above approaches for active thermal control are summarized in Fig. 24 and their references are attached.This figure classifies the existing active thermal control methods from the perspective of the basic ideas and the means of implementation.Loss compensation methods can significantly

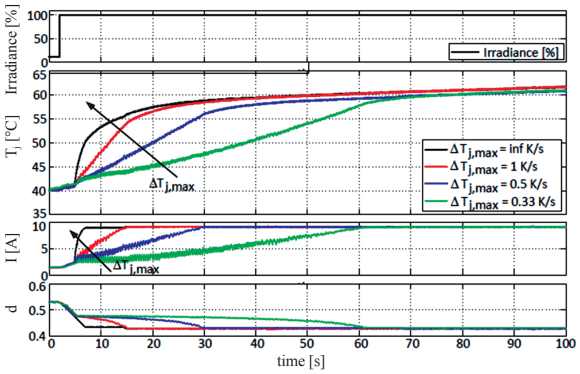


Fig. 23. Behavior of the MPPT for a step in the irradiance PPV,rel=10%≥P-PV,rel=100% for different temperature gradients and normalized starting temperature in one IGBT. Irradiance, junction temperature, input current and duty cycle of the boost converter are shown [109].

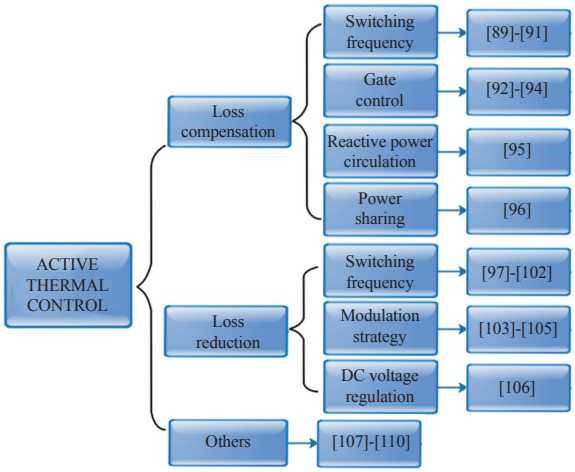


Fig. 24. Classification of active thermal control methods.

reduce the thermal stress caused by low frequency junction temperature fluctuations, but the main drawbacks include: 1) have no effect on the base frequency junction temperature fluctuations; 2) it will increase the average loss of power devices.Loss reduction methods can reduce thermal stress caused by both the fundamental frequency junction temperature fluctuations and low frequency junction temperature fluctuations,but the main drawbacks include: 1) it will reduce the output quality of the converter; 2) if the converter is designed with minimum loss, it will not be applied. Other active thermal control methods are mainly for specific applications and can effectively reduce the thermal stress under the specific condition, but they can not be promoted.

VI. Conclusion and Challenge

Current studies of conditions monitoring generally revolve around IGBT modules, the conditions monitoring of the IGBT module can provide reference and basis for the optimization maintenance of power converter systems. On the basis of existing research, it is still necessary to find out more indicators that can reflect the health condition more comprehensively and understand the precursors' variation

law more deeply. Meanwhile, the comprehensive health condition assessment based on multiple precursors is still of great importance. Furthermore, how to achieve the condition monitoring of power converters from the device level to the system-level is significant important.

Lifetime of power devices is estimated on the basis of the accelerated aging test, the junction temperature evaluation and the method of accumulation damage calculation. The existing IGBT lifetime models have their limitations due to the diversity of materials, the complexity of operating condition and the imperfection of accumulation damage theories. Consequently, it is too difficult to establish an accurate, universal IGBT life model, so that the material of the module and the operating conditions should be taken into account when building or using a lifetime model.Damage accumulation theory also needs to be developed so that lifetime models can get more accurate predictions, customers and manufacturers can be acquired more valid reference to do so.

In active thermal control, junction temperatures general are estimated by the case temperature and the thermal network, so that its control is quasi-closed loop and the actual junction temperature is ambiguous before or after active thermal control. The potential costs for higher losses or expense of control device etc.are must to be considered, if the potential costs are too high,active thermal control is of little significance. There is a trade-off between active thermal control and the potential costs. In addition, the effectiveness of active thermal control is verified by lifetime estimation at present, the real result of active thermal control is missing, and it is should to be verified with practical applications or accelerated tests.

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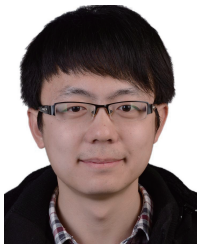

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15 kV SiC MOSFET: An Enabling Technology for Medium Voltage Solid State Transformers

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***Abstract*—Due to much higher achievable blocking voltage and faster switching speed, power devices based on wide bandgap (WBG) silicon carbide (SiC) material are ideal for medium voltage (MV) power electronics applications. For example, a 15 kV SiC MOSFET allows a simple and efficient two-level converter configuration for a 7.2 kV solid state transformer (SST) for smart grid applications. Compared with multilevel input series and output parallel (ISOP) solution, this approach offers higher efficiency and reliability, reduced system weight and cost by operating at medium to high switching frequency. However, the main concern is how to precisely implement this device in different MV applications, achieving highest switching frequency while maintaining good thermal performance. This paper reviews the characteristics of 15 kV SiC MOSFET and offers a comprehensive guideline of implementing this device in practical MV power conversion scenarios such as AC-DC, DC-DC and AC-AC in terms of topology selection, loss optimization and thermal management.**

***Index Terms*—15 kV SiC MOSFET, efficiency, medium voltage, medium voltage power electronics, reliability, solid state transformer, smart transformer.**

I. Introduction

As a new and emerging application of medium voltage (MV, 2 kV-35 kV) power electronics, the Solid State Transformer (SST) is very attractive in smart grid, traction drive and renewable energy systems [1]-[4] due to its benefits in size and weight reductions, as well as a number of smart functionalities such as reactive power compensation. The basic concept of the SST is to use a Medium Frequency (MF) (several kHz to tens of kHz) power converter to replace a traditional Line Frequency (LF) power transformers (LFT). Comparing to LFTs, SSTs can achieve higher power density while potentially offering many smart features such as Var compensations, voltage regulation, fault isolation and DC link [1]-[4].

The basic operational principle of the SST is as follows:

1) Change the 50/60 Hz MV ac voltage to a MF voltage.

2) Step up/down this MF voltage through a MF transformer.

3) Reshape the MF waveform back to 50/60 Hz voltage.

One grand challenge for the SST is to achieve MV input voltage such as 7.2 kVac in single phase smart grid application in United States. No commercial power devices are currently available to handle the associated peak voltage stress. Modular multilevel configurations based on input series and output parallel (ISOP) are widely used to address this issue in which low voltage converters are connected in series to share the voltage and power [5]-[13]. To avoid power and voltage balancing problems, additional balancing circuits and control strategies are needed [14]. The resulting SST is therefore typically very complex due to the complex system configuration, protection and control schemes, numerous gate drivers and isolated power supplies. System reliability is low if redundancy is not carefully considered.

Ultimate solutions for MV power electronics can be more elegantly achieved if MV power devices can be developed to cover the wide spectrum of MV voltages (2 kV-35 kV). Up to now, silicon power devices such as Si IGBT are the only available device for MV applications but the maximum blocking voltage of the IGBT is limited to 6.5 kV due to substantially increased losses if designed for even higher voltages. On the other hand, due to the significantly increased peak electric field strength in WBG materials such as SiC, SiC power devices with much higher blocking voltage have been developed and demonstrated. The blocking voltage demonstrated ranges from 10 kV to 24 kV with three terminal device concepts based on unipolar (i.e. SiC MOSFET) and bipolar (i.e. SiC IGBT/ETO) conduction mechanisms [15]-[18]. Although not yet commercially available, they can enable a simpler and robust two-level SST in 7.2 kV applications where the peak voltage stress is less than 12 kV. SST based on high voltage SiC power devices is therefore a very attractive technical approach. With two-level configuration, the system complexity and control scheme can be much simplified. Therefore, higher reliability and efficiency can be obtained. In addition to the improvements in voltage ratings, the switching speed of these devices is also significantly faster than commercially available 6.5 kV Si IGBTs hence allowing the SST to operate at higher switching frequency. Higher operation frequency enables volume reduction of the MF transformers, inductors and capacitors so that higher power density and light weight can be obtained.

Varies power conversion topologies and applications of the SST have been discussed in literatures [5]-[13]. Many well-known MV SST designs are depicted in Fig. 1, including designs by Alstom [5], Bombardier [6], UNIFLEX [7], ABB PETT [8], GE Global Research [10], EPRI [9], ETH [11] and the FREEDM System Center [12], [13], [19].

From power conversion point of view, there are basically

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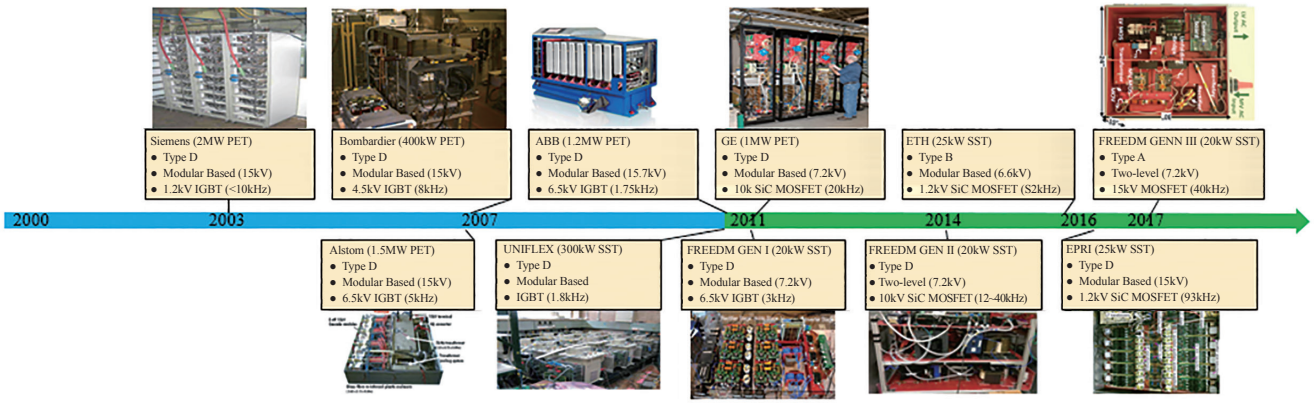

Fig. 1. MV prototypes developed by leading research groups.

four topology approaches to form a SST as shown in Fig. 2. Type D is the most widely used approach since it can achieve most of the smart features that a smart transformer desires. It contains three conversion stages: a rectifier stage that offers power factor correction and reactive power capability; a second DC-DC stage with galvanic isolation and voltage step-down and a third low voltage (LV) inverter stage that reshapes the DC voltage back into a desired AC voltage. The efficiency of Type D SSTs is lower because of the three stages of power conversion, and two of them are MV converters.

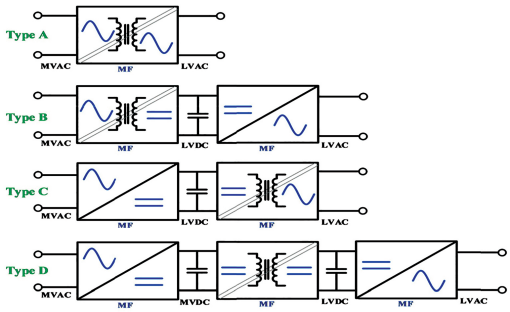

Fig. 2. SST topology classification.

Type A topology is very attractive since the power conversion stages are reduced, which enables better efficiency and higher reliability. Due to these benefits, several efforts on Type A SST have been carried out [11], [29], [34]. In Type A SST, the MV device will experience a wide voltage range, from 0 to 10 kV during one line frequency cycle in case of a 7.2 kVac input. Achieving ZVS under such wide voltage range and load conditions becomes very difficult.

In the SSTs, the MV devices may encounter totally different operation conditions. The AC-DC stage of the Type D SST normally operates under hard switching condition, which limits the switching frequency under 10 kHz due to the large amount of switching losses even if SiC MOSFET is used [13], [28]. While in the DC-DC stage, ZVS can be easily achieved and it enables a substantial reduction of the switching loss. Hence the switching frequency can be much higher [19], [20]. Type A SST is basically an isolated direct AC-AC converter and the MV devices may operate under hard switching condition. In this case, both switching and conduction losses exist, an optimal design that achieves minimum overall loss is needed. Transformer loss optimization must also be part of this optimization process. On the other hand, Type A SST with ZVS capability will be very desirable to reduce or eliminate the switching loss hence the switching frequency can be substantially increased.

Many previous papers focus on topology, passive components and control design. Only a few papers focus on the MV device utilization issue in MV and MF applications. This paper provides a comprehensive review of the 15 kV SiC MOSFET characteristics as well as a comprehensive design guideline for utilizing its full switching frequency and power potential in MV AC-DC, DC-DC, AC-AC applications.

The paper is structured into five sections. Section II gives a comprehensive overview of the salient characteristics of 15 kV SiC MOSFET. In the Section III, the frequency vs. power handling capability of the 15 kV SiC MOSFET in AC-DC, DC-DC and AC-AC are fully investigated. Some of the experimental results from the author's group are presented to verify the design. Some conclusions will be drawn in the final section.

II. 15 kV SiC MOSFETs

Due to almost ten times higher peak electric field strength in SiC when compared to Si, SiC power devices with much higher blocking voltages such as the 15 kV SiC MOSFETs have been developed and demonstrated [13], [14]. Since the device operates as a unipolar conduction device, its switching speed is also very fast. As a comparison, Si power MOSFETs are typically designed with a blocking voltage less than 1200 V. So achieving ultra high blocking voltage is a direct benefit of SiC power devices.

The 15 kV SiC MOSFET prototype developed by Wolfspeed uses a DMOS device structure and the device is packaged with a single side cooling capability as shown in Fig. 3 [35]. The chip size has a dimension of 8.1 mm×8.1 mm in which 5.95 mm×5.95 mm is the active area that conducts current. To Implement this device in MV applications, ac-

curate device conduction loss, switching loss and thermal models need to be developed.

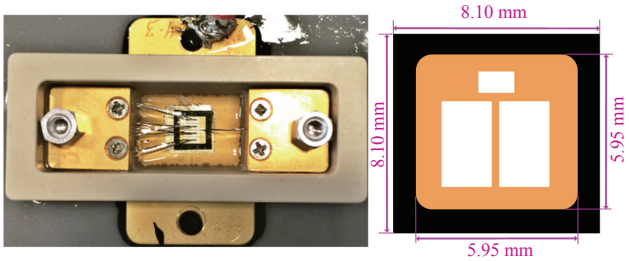

Fig. 3. 15 kV SiC MOSFET (a) packaged module (b) die dimension [35].

A. On-Resistance Model

The measured and modeled conduction resistance of the device at 20V gate to source voltage are shown in Fig. 4. The room temperature on-resistance is around 0.875 Ω, and the corresponding specific on-resistance is 309 mohm-cm^2. This value is very close to the theoretical capability of 15 kV SiC MOSFET. In the future, superjunction SiC MOSFET can be developed that can lower this resistance substantially.

SiC MOSFET on-resistance increases quickly with the increase of the junction temperature as shown in Fig. 4. The measured result can be represent by a Ron model [19]

$$R_{on} = R_0(\frac{T_j}{T_0})^{3.5} \tag{1}$$

where R_0=0.875 Ω, T_0=348.16 K.

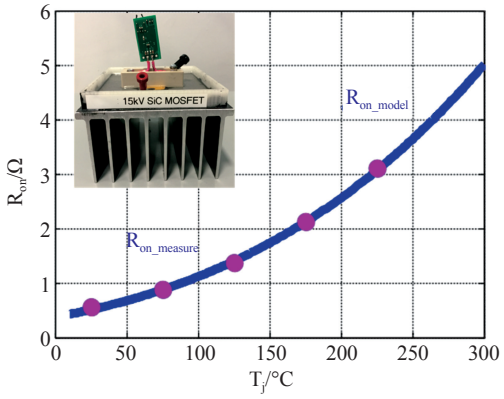

Fig. 4. On-state resistance of the 15 kV SiC MOSFET modules [19].

Increased Ron at high temperature is a typical behavior of all unipolar power devices such as the MOSFET, but the rate of increase for the 15 kV device is substantially higher than 1200 V SiC MOSFET. This is due to the fact that the 15 kV device on resistance is dominated by the drift layer resistance. Due to the large on resistance, a single chip MOSFET is only capable to operate under relative low current conditions due to the high conduction loss. Ideal applications will be those requiring high voltage and low current, such as a single phase SST in the range of 10 to 50 kVA. For high power applications, many MOSFET chips can be paralleled to form a MOSFET module. In paper [10], 12 dies of 10 kV/10 A MOSFETs are paralleled to form a single 10 kV 120 A switch.

B. Switching Loss Model

The SiC MOSFET has very fast switching speed because it is a unipolar switch with no current tail. The switching time is determined by load condition and the device parasitic capacitance. The switching time is typically less than 500 ns as shown in Fig. 6, in which the dynamic turn-on and turn-off waveforms under 8 kV/8 A conditions are shown. However, this high switching speed does not directly translate to high switching frequency. In MV applications, the energies stored in the output capacitance of the devices is extremely high, which will result in large turn-on loss if the stored energies are not carefully recovered. An accurate Q_{oss} and E_{oss} model is critical for converter design.

Turn-on Loss: In a typical bridge configuration, the minimum turn on energy under hard switching condition is the energy stored in the output capacitance of the device as well as that in the freewheeling diode. Additional turn-on loss occurs due to the controlled dI/dt and dV/dt which results in a large voltage and current overlap during the turn-on, as shown in Fig. 5.

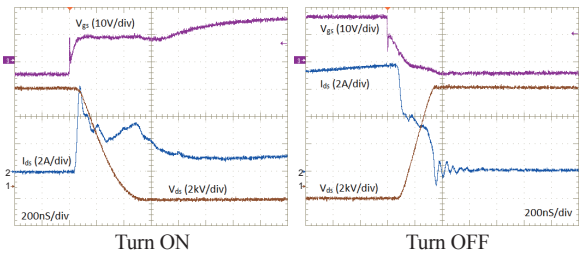

Fig. 5. Turn on and turn off waveforms under 8 kV /8 A condition.

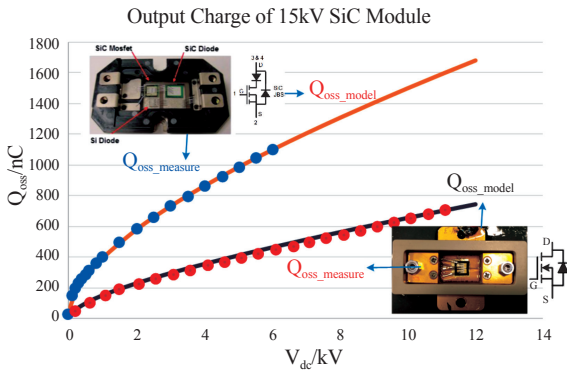

Fig. 6. Output charge of 15 kV SiC MOSFET modules.

The output charge Q_{oss} of the 15 kV MOSFET, hence the associated loss E_{oss}, can be accurately measured with a novel method proposed in [23]. The measured and modeled output charge of the 15 kV MOSFET in two different package are plotted in Fig. 6.

The Q_{oss} model equation is expressed as

$$Q_{oss\_single}(V_{ds}) = 4.08\sqrt{V_{ds}} + 24.8 \cdot V_{ds} \quad (2)$$

for the packaged 15 kV SiC MOSFET prototype device. If the associated energy E_{oss} is directly released to the device during the hard turn on, it will result in a substantial turn on loss. The measured E_{on} loss, which include E_{oss} as well as the voltage and current overlap loss, is shown in Fig. 7.

Turn-off Loss: Since the load current for the 15 kV MOSFET is low, the turn-off process is dominated by the charging of the output capacitance of the MOSFET as well as the discharge of the associated freewheeling diode and load parasitic capacitance. This is clearly shown in Fig. 5. This process is almost lossless (E_{off}=0) since the energy is simply stored in the output capacitance and stored energy is E_{oss}. Hence the turn-off loss of the 15 kV SiC MOSFET can be modeled as zero. Similar situation can also happen in lower voltage SiC MOSFETs if the turn-off process is dominated by the load current determined charging of C_{oss} of the switch, the freewheeling diode and the load parasitic capacitance [38].

The measured E_{on} and E_{off} at 4 kV condition are shown in Fig. 7 when compared with a 6.5 kV Si IGBT under similar test condition. The E_{on} loss shown includes the E_{oss} loss as well as the voltage and current overlap loss which has a strong dependence on the gate driving condition or R_g value.

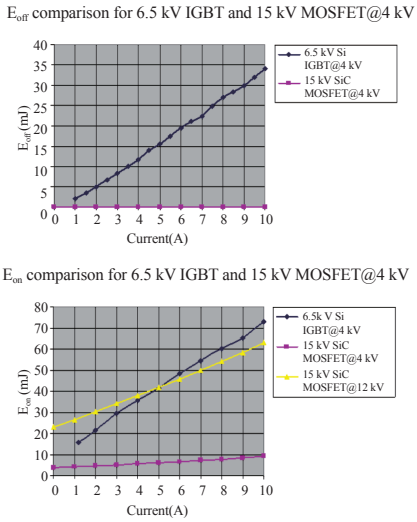

Fig. 7. The E_{on} and E_{off} of the 15 kV SiC MOSFET [22].

Compared with the IGBT, the SiC MOSFET shows a much lower total loss. This overall lower switching loss enables higher switching frequency in MV converters under hard switching conditions, leading to smaller system volume and higher power density. Hard switching based AC-DC converter based the 15 kV MOSFET has been reported in [28] which has a switching frequency of 6 kHz and a DC link voltage of 6 kV.

If the DC link voltage increases to 12 kV, the E_{off} loss remains close to zero while the E_{on} loss increases substantially, as shown in Fig. 7. This will limit the maximum switching frequency if the MOSFET operates in hard switching condition.

ZVS Turn-on: The switching frequency can be increased by recycling the output charge energy E_{oss} back to the load and/or source through the well-known zero voltage switching (ZVS) technique. The basic idea is to use the inductive energy stored in an inductor to discharge the C_{oss} of the device during the deadtime. A minimum amount of current is needed in the inductor and a typical ZVS criteria is shown in (3) where $Q_{oss}(V_{ds})$ corresponds to the charge in the C_{oss} of the device prior to the discharge.

$$I_{off}(V_{ds})t_{dead} \geq Q_{oss}(V_{ds}) \quad (3)$$

If ZVS can be achieved, then the total switching loss of the device is almost zero. Theoretically then no switching frequency limitation exists. In practice, the switching frequency will be limited by the performance of the magnetic components, as well as the timing required to discharge the C_{oss}. In summary, with a combination of intrinsic capability (unipolar device vs. bipolar device) and circuit technique (ZVS vs. hard switching), the unique opportunity with the 15 SiC MOSFET can be summarized as a significantly increased operational Voltage×Frequency figure of merit (FOM) when compared with Si IGBT. This FOM is directly related to the MV converter performance. The higher the FOM, the better. The 15 kV SiC MOSFET device can achieve a FOM several hundred times higher than MV Si IGBT power devices. For example, the author's group have already achieved steady operation of the 15 kV SiC MOSFET at 40 kHz under 10 kV/ 20 kW condition [39] hence the FOM number is 400 MHz-Volt. Additional analysis shown in this paper (see Fig. 23) suggest that operation beyond 100 kHz is also feasible hence the FOM can reach more than 1 GHz-Volt, which is 200 times higher than the typical 5 MHz-Volt capability of a Si IGBT device. Fig. 8 shows the achieved FOMs for a number of power devices.

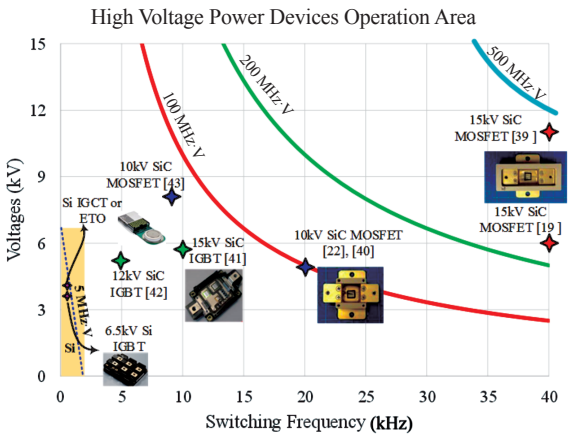

Fig. 8. The MV SiC MOSFET's Voltage×Frequency capability in comparison with Si high power devices such as IGBT/IGCT/ETO.

C. Paralleled JBS Diode

The 15 kV SiC MOSFET has an integrated body diode

that can be used as the freewheeling diode in converter applications. Applying a positive gate voltage will enable the MOSFET to operate as a synchronous rectifier. This capability is a directly advantage of the MOSFET when compared with an IGBT which must have a paralleled freewheeling diode.

However, there may be a need to connect a separate SiC JBS diode with the 15 kV SiC MOSFET for several reasons. The body diode of the 15 kV SiC MOSFET does not turn on until a forward voltage higher than 3.2 V. This higher forward drop will result in higher conduction loss. Applying a gate voltage to operate it as a synchronous rectifier can lower the conduction loss to the same level as that of the forward direction with a resistance shown in Fig. 4. This strategy can only happen after the deadtime period. Another important reason is the poorer diode reverse recovery performance associated with the SiC PN junction diode if substantial carriers are injected by the PN junction. The forward conduction of the PN junction may also cause significantly device degradation (loss of the forward blocking capability and/or increase of the R_{on}) [24], [25]. Many research on this degradation has been conducted with several literatures indicate that the issue has been largely solved in 1200V SiC MOSFET. For the tested 15 kV SiC MOSFET, however, there is a significantly degradation observed if the body diode conducts.

For above reasons, the 15 kV SiC MOSFET prototype device should be used without the body diode conduction. One strategy is to have low voltage silicon diode connected in series with the MOSFET to prevent the body diode from conducting, while a 15 kV SiC JBS diode is placed in parallel to conduct the reverse current (see Fig. 9). These two add-on devices may affect the device performance as well as system designs. The upper curve in Fig. 6 shows the output charge of the device up to 12 kV with a paralleled JBS diode, which has a significantly higher Q_{oss} than the MOSFET alone (lower curve). The Q_{oss} model for the MOSFET+JBS is derived as

$$Q_{oss\_combine}(V_{ds}) = 11.43\sqrt{V_{ds}} + 36 \cdot V_{ds} \qquad (4)$$

At 11 kV, the Q_{oss} of the SiC MOSFET alone is around 700 nC, while the output charge of the JBS diode is around 900 nC at this point. The test result indicates that the output charge in the JBS diode is even larger than that in MOSFET. In hard switching conditions, the added output charge will increase the hard switching E_{on} loss. In ZVS converter, larger output charge requires higher turn off current or longer deadtime, either way it will result in higher conduction loss for the system.

However, in a well-designed ZVS DC-DC or AC-AC converter, as will be mentioned in this paper, body diode conduction of the MOSFET can be avoided. So that the anti-paralleled SiC JBS diode can be eliminated. This will lower the semiconductor cost and improve the system power density.

D. Thermal Model

In this paper, the 15 kV SiC module is mounted on a heatsink without fan (see Fig. 4), which has a measured junction to air thermal resistance of 1.5 °C/W. Junction temperature is calculated based on this thermal resistance to predict the converter capability. If a better cooling system such as forced air or forced water is adopted, the thermal resistance will be much lower and even higher power handling capability can be obtained in the discussed converters.

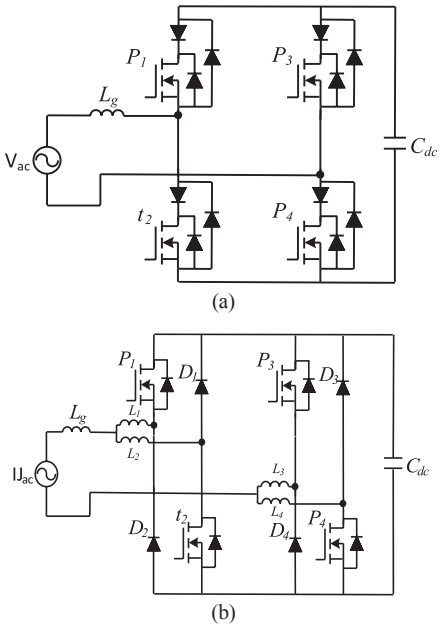

Fig. 9. AC-DC topologies: (a) Full bridge based (b) Dual buck based.

III. MV Converter Implementation Using 15 kV SiC MOSFETs

In different implementations, the MV devices may encounter totally different operation scenarios. Therefore it is important to understand the MV device's capability in terms of power handling capability in practical MV applications according to the unique applications features and requirements. AC-DC, DC-DC and AC-AC are the three main conditions the 15 kV SiC MOSFETs will encounter in MV applications.

A. AC-DC Applications

AC-DC stage normally acts as the input stage for a Type D SST and offers power factor correction and reactive power functionalities. Fig. 9(a) shows a typical bridge type AC-DC circuit that is widely adopted in MV applications. The MV devices operate under hard switching condition in this stage. As mentioned previously, a series connected Si diode and a SiC JBS diode are used with the MOSFET to prevent the body diode conduction [21], [22]. In hard switching conditions, the output charge of the device is directly released to the device during turn on. These amount of energy is large in MV applications, which will therefore limit the switching frequency of this stage. A design example of a MV AC-DC converter based on the 15 kV SiC MOSFET is shown in

[13] and the switching frequency is 6 kHz at 3.6 kV input voltage/V_{dc}=6 kV. The measured efficiency and calculated efficiency are shown in Fig. 10. Loss breakdown at V_{dc}= 6 kVdc and 12 kVdc are also shown in Fig. 10 to highlight the significantly increased switching loss at higher DC link voltages. Fig. 11 shows the predicted junction temperature of the 15 kV SiC MOSFET versus dc voltage and switching frequency in hard switching AC-DC converters. The results indicate that the switching frequency and power handling capability of the device in hard switching conditions. The results show that switching loss dominant the total loss and increases significantly as DC link voltages increases. At V_{dc}=12 kV, the switching frequency has to be lowered to keep the junction temperature below 150 ℃.

To reduce the switching loss of the AC-DC stage, critical conduction mode (CRM) is normally implemented in LV PFC applications [39] to achieve ZVS turn-on at the expense of increased control complexity and large conduction loss. However, there is currently no publications that discussed the CRM mode operation of a MV AC-DC converter. The main concerns may include: 1) a current zero crossing detection circuit is required in CRM, which is not easy to implement in MV applications. 2) Switching frequency varies in CRM, which makes it difficult to design input filter and create additional EMI problems. 3) The current ripple is two times of the average current, resulting in larger input filters. Nevertheless, CRM based MV AC-DC is worth exploring since it will completely eliminate the switching loss (E_{on}=0, E_{off}=0) and the conduction loss can always be reduced by paralleling more devices. Multiphase CRM AC-DC can be used to reduce the input side current ripples.

The integrated silicon diode in Fig. 9(a) may experience an abnormal avalanche breakdown in every switching cycle and the circuit has potential shoot-through problem [28]. An improved AC-DC as shown in Fig. 9(b) is presented in [28] to solve the shoot-through and avalanche of silicon diode problems. In the improved topology, the SiC MOSFET body diode never conducts and there is no shoot through problem that threatens the safe operation of the circuit.

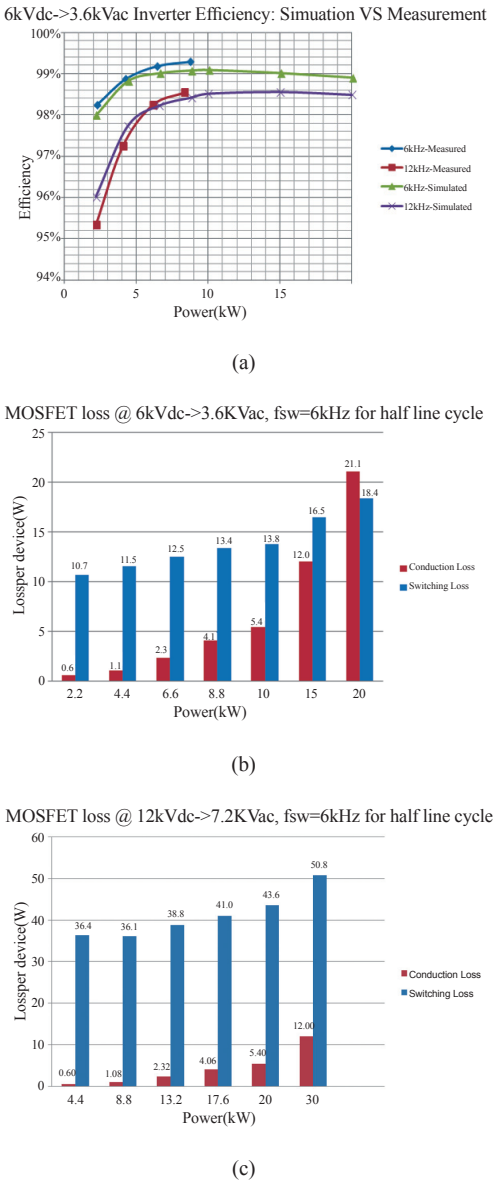

Fig. 10. (a) Measured and calculated AC-DC converter efficiency at V_{dc} =6kV and f_s=6 kHz and 12 kHz. (b) Loss breakdown at V_{dc}=6 kV, f_s=6 kHz; (c) Loss breakdown at V_{dc} =12 kV and f_s=6 kHz.

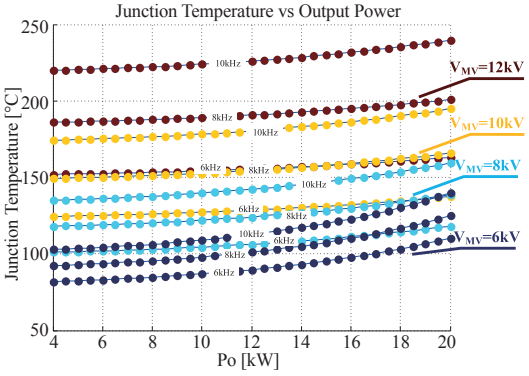

Fig. 11. Minimum 15 kV SiC MOSFET junction temperature versus processed power with different f_s and V_{MV} in AC-DC application. Natural cooling.

B. DC-DC Applications

MV MF isolated DC-DC converter is an essential device functioning as a DC transformer in future MV DC grid as well as a key stage in a Type D SST. Its conversion efficiency is crucial to the overall system power efficiency. In addition, it needs to step down the MV DC to LV DC and provides system galvanic insulation. Its operation frequency directly determines the MF transformer's size. SiC MOSFETs with fast switching speed enables the realization of MV MF transformation. However, due to the significant amount of energy store in the output capacitance, even with zero load current, hard turn-on loss is still high enough to limit the operation frequency below 10 kHz [13], [28]. To increase the switching frequency and conversion efficiency, full ZVS DC-DC converter is therefore required.

Dual Active Bridge (DAB) or Dual Half Bridge (DHB, Fig. 12) are classical solutions for MV isolated DC-DC converter with ZVS capability. Only two MV switches are needed in the DHB. It has simple and symmetrical structure, easy to start up and to implement over current protection. With the 15 kV SiC MOSFETs, a 6 kV-400 V, 10 kW DHB DC-DC converter running at 20 kHz has been developed and reported [19]. The steady state waveforms at 6 kV/ 6.5 kW is shown in Fig. 14(a). ZVS of the switch is obtained in this condition. However, ZVS may be lost under light load condition and the high turn off current may result in non-zero turn-off loss (introduce additional voltage-current overlap during device turn-off) hence deteriorates the overall efficiency [13], [20]. Additional control methods such as extended-phase-shift (EPS) and dual-phase-shift (DPS) can be applied to extend the ZVS operation range of this converter [36], [37].

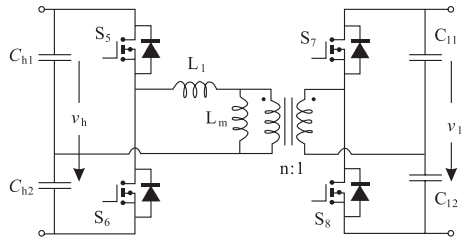

Fig. 12. DHB based DC/DC converter circuit used in [13] .

Novel MV DC-DC converter (see Fig. 13) that combines a DAB and a series resonant converter has been demonstrated by the authors in [19]. Operating at 40 kHz, it can realize ZVS at any load condition [19]. From zero to full load, the converter is designed to operate at the resonant frequency. Magnetizing current charges and discharges the MOSFETs' output capacitors during the switching interlock time. According to (5), complete soft turn-on is realized by carefully chosen magnetizing inductance and dead-time t_d. Fig. 14(b) and (c) shows the steady state waveforms of the converter with a V_{dc}=10 kV at light and heavy loads. V_{ds} waveforms in orange indicate that ZVS is fully achieved in both load conditions.

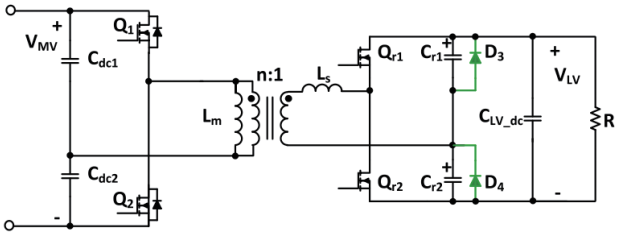

Fig. 13. Novel resonant and DAB hybrid DC-DC converter in [19].

$$Q_{oss}(V_{ds}) \le V_{MV} T_r t_d / 8 L_m \quad (5)$$

In order to have an optimized L_m and t_d, understanding the MOSFETs' output charge is crucial. [23] proposed a new test circuit that not only reflects the realistic ZVS scenario, but also achieves high accuracy (<1% error). High voltage measurement of the MOSFETs' output charge was measured up to 12 kV without resorting to special equipment or complex configuration. The result is shown in Fig. 6.

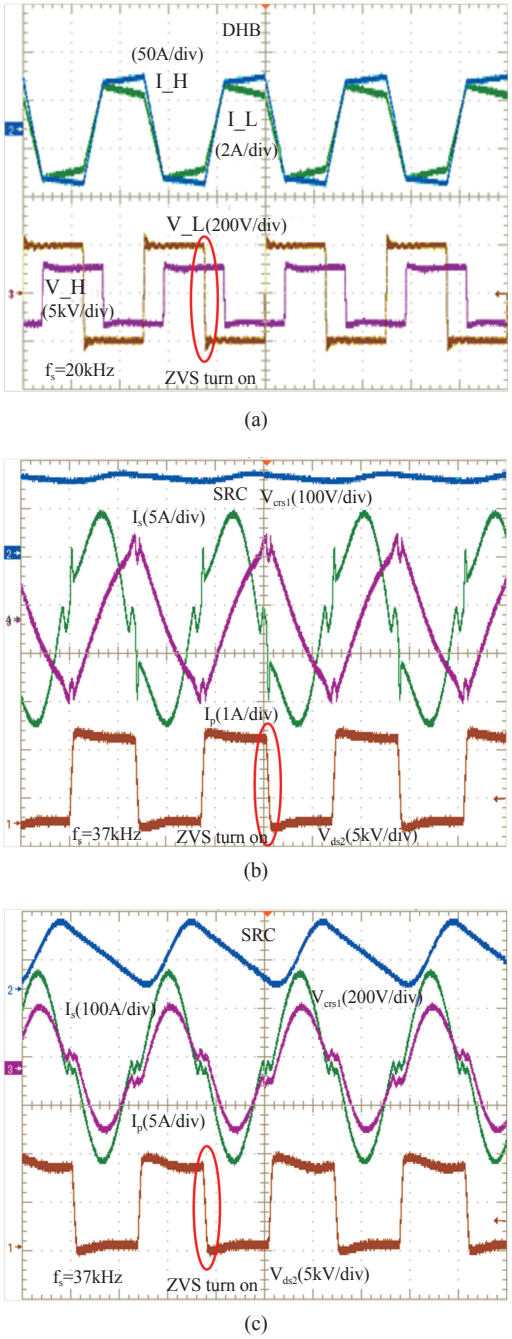

Fig. 14. DC-DC Operation waveforms (a) DHB at 6 kV/ 6.5 kW/20 kHz (b) SRC at 10 kV /1 kW/ 40 kHz (b) SRC at 10 kV /17 kW/ 40 kHz.

The Q_{oss} model, together with the on-resistance model as well as the thermal model, is used to calculate the maximum power handling capability of the 15 kV SiC MOSFET in the Fig. 13 DC-DC topology. The results are summarized in Fig. 15. The results indicate the amazing capability of the 15 kV

SiC MOSFET if soft switching is achieved. With less than 2 cm^2 total chip area for the two MV switches, the converter can deliver greater than 30 kW when operates at 12 kV with 100 kHz switching frequency. In a well-designed ZVS DC-DC converter, body diode conduction of MOSFET can also be avoided. The anti-paralleled SiC JBS diode is not necessary, which further lowers the semiconductor cost.

Fig. 16 provides the measured efficiency curves at both 6 kV and 10 kV conditions over a wide load range. The achieved efficiency is higher than 97% at most load conditions and the peak efficiency is up to 98%.

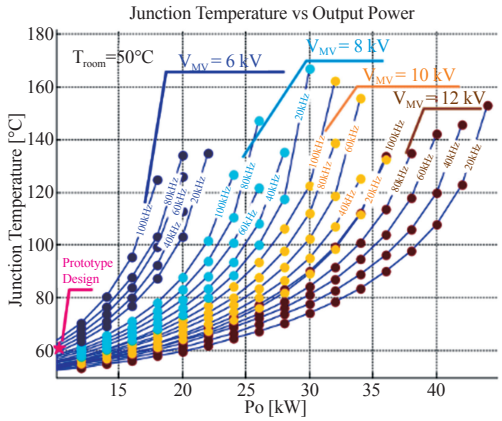

Fig. 15. Optimized (minimum)15 kV SiC MOSFET junction temperature versus processed power with different f_s and V_{MV} in DC-DC application. Natural convection cooling [19].

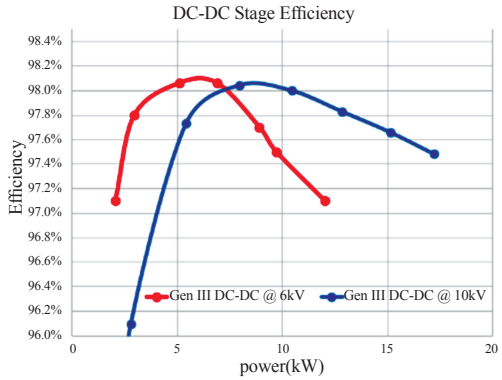

Fig. 16. Efficiency curves of the MV DC-DC converter at 6 kV and 10 kV.

C. AC-AC Applications

Type A SST shown in Fig. 2 is also attractive since the power conversion stages are reduced. The reduced power stages and simplified system configuration enables higher efficiency and reliability. The main challenges to implement MV Type A SST is the ZVS design under wide input voltage range. The input voltage changes from 0 to 10 kV every line frequency cycle. Achieving ZVS under such wide voltage range and load conditions is very difficult. The ZVS constraint is still represented by equation (6).

$$I_{off}(V_{ds}, P_o)t_{dead} \geq Q_{oss}(V_{ds}) \tag{6}$$

However, The Q_{oss} of the MOSFET is nonlinear with the V_{ds} voltage, while turn off current at left hand side of the equation has a linear relatioship with voltage, which makes the ZVS design more complicated.

Fig. 17 shows a Type A topology based on DAB and four-quadrant switch cells [34]. The converter can operate at high frequency and efficiency due to its ZVS capability. This circuit also shows a good capability in bidirectional power flow and voltage regulation. The turn off current of a normal SPS controlled DAB can be expressed in as [31]

$$I_{off} = \frac{T_S}{4L}[nV_{in}(2d-1) + V_o] \tag{7}$$

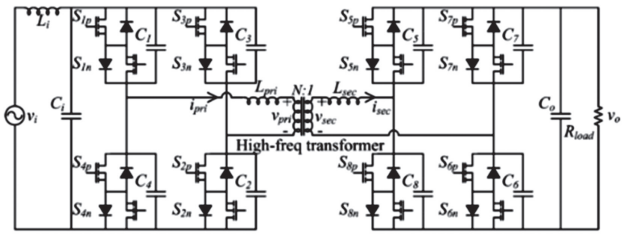

Fig. 17. Direct AC-AC converter based on DAB in [34].

The turn-off current in (7) not only depends on the load condition but also on the input voltage. If not well designed, ZVS may be lost at light load and low voltage conditions due to insufficient turn off current [31]. Additional control methods such as extended-phase-shift (EPS) and dual-phase-shift (DPS) can be applied to extend the ZVS operation range [36]-[37]. The converter in [34] also contains eight MF MV device, which is not cost effective.

Fig. 18 shows another Type-A SST configuration which uses an ISOP configuration of low voltage AC-AC converters [11]. Series resonant converter (SRC) is used as the AC-AC topology that operates in half cycle discontinuous conduction mode. [11] provides an analysis of the ZVS behavior under wide input voltage range. A time-dependent variation of deadtime control is adopted to achieve ZVS over the entire grid period. The SST is based on modular structure with voltage on each module less than 1200 V. Many modules are needed to achieve MV and there are no experimental results reported so far.

The authors of the paper have proposed a Type-A SST using a two-level SRC circuit based on the 15 kV SiC MOSFETs, as shown in Fig. 19 [39]. The circuit is proposed to operate at constant resonant switching frequency for high efficiency. The achieved gain is unity and is independent of load conditions. Only two MV switches are used.

In Fig. 19 circuit, the turn off current can be derived as

$$I_{Lm}(V_{ds}) = \frac{V_{ds}T_s}{8L_m} \tag{8}$$

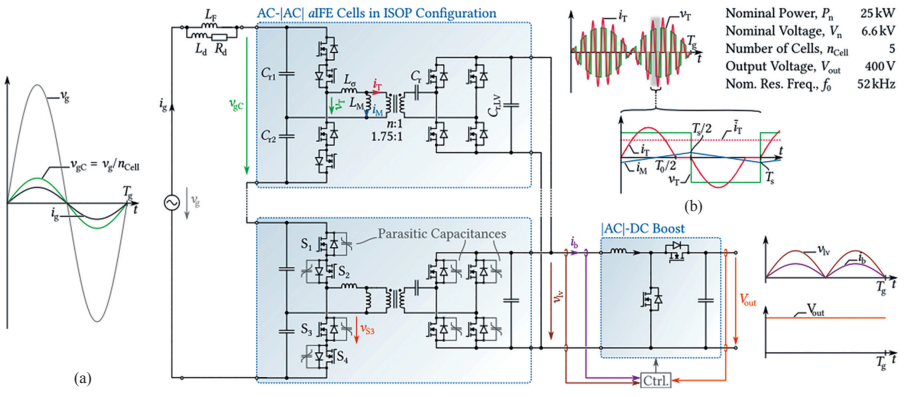

Fig. 18. Type A SST based on the ISOP Configuration of AC-AC converters [11].

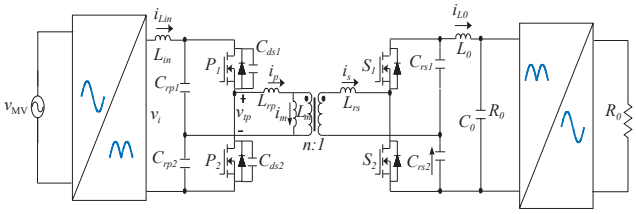

Fig. 19. Direct AC-AC converter based on SRC proposed by the author's group [39].

This turn off current is only associated with the input voltage, the magnetizing current and the deadtime and is idependent of the load condition, which means that if ZVS is obtained at a certain voltage level, this ZVS is maintained over wide load range. The ZVS constraint is still same as shown equation (5). The orange and blue curves in Fig. 20 shows the minimum deadtime required to realize ZVS over the half line cycle for two different L_m cases. These curves represent the adaptive deadtime strategy that is also mentioned in paper [11]. Long deadtime is needed at low input voltage range to maintain ZVS operation.

On the other hand, the turn-on loss of the SiC MOSFET decreases rapidly as V_{ds} decreases even if it has partial hard switching. In practical design, it is possible for the MOSFETs to experience hard switching at low voltage conditions if the turn on loss is controlled within a low level.

To simplify the deadtime control complexity, a constant deadtime scheme can be used and is drawn in pink curve in Fig. 20. The value of this deadtime is designed to guarantee

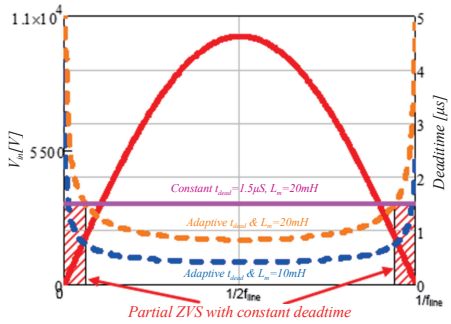

Fig. 20. Required and proposed deadtime versus input voltage.

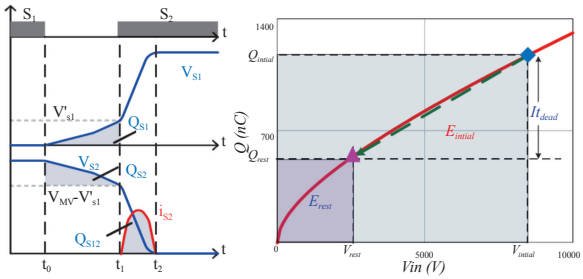

Fig. 21. Partial discharge theory.

the ZVS operation of the MOSFETs under most high voltage conditions. At low voltage conditions, the deadtime is not long enough to fully discharge the Q_{oss} of the devices and some turn on loss is generated. Such a partial discharge condition is shown in Fig. 21. When partial discharge happens, the residual Q_{oss} can be calculated as Q_{res}=Q_{oss}-It_{dead}.

The corresponding residual voltage at that moment can be derived based on equation (9)

$$V_{res} = \left(\frac{-4.08 + \sqrt{4.08^2 + 4 \cdot 0.0248 \frac{Q_{rest}}{2} 10^9}}{2 \cdot 0.0248}\right)^2 \tag{9}$$

The turn on power loss can be obtained with (10)

$$P_{on} = f_{sw}{}^2 \cdot f_{line} \int_0^{\frac{1}{2 \cdot f_{line}}} V_{res} Q_{res} \tag{10}$$

Fig. 22(a) shows the residual charge Q_{res} and voltage V_{res} versus the input voltage under different deadtime conditions. Fig. 22(b) shows the results of turn on loss versus deadtime under different L_m conditions with a switching frequency of 40 kHz. The curves indicate that the turn on loss decreases dramatically as the deadtime increases or L_m decreases. If the deadtime and L_m values are properly selected, the turn on loss will be small even if partial discharge happens.

Increasing deadtime or decreasing magnetizing inductance both help reduce the turn on loss. However, smaller magnetizing inductance leads to larger circulating and RMS current in the circuit. Longer deadtime also leads to higher RMS current and more distortion. Both methods will cause larger

conduction loss in the circuit. The L_m and t_{dead} selection is actually a trade-off between switching loss and conduction loss.

RMS current on MV side can be calculated with equations from (11) to (13) [32], [33].

$$i_{r\_p}(t) = \sqrt{2} I_{RMS\_P} \sin(\omega_0 t + \varphi) \tag{11}$$

$$i_{Lm\_p}(t) = -\frac{V_{in} T_0}{8 L_m} + \frac{V_{in}}{2 L_m} T \tag{12}$$

$$I_{RMS\_P} = \sqrt{\frac{\pi^2 I_o^2}{2n^2} \left(\frac{T_s}{T_s - 2t_d}\right)^2 + \frac{\left(\frac{V_{in} T_0}{8 L_m}\right)^2}{2}} \tag{13}$$

Using the on-state resistance R_{on} and thermal models of the 15 kV SiC MOSFET, the overall semiconductor loss versus magnetizing inductance and deadtime in the proposed AC-AC converter are calculated and shown in Fig. 23. This figure is based on 7.2 kV, 13 kW and 40 kHz switching frequency conditions. When t_{dead} is short and L_m is large, overall loss increases as turn on loss increases. While when t_{dead} is long and L_m is small, overall loss is also high due to the increasing of conduction loss. Optimized parameters can be chosen based on Fig. 22 and Fig. 23. L_m and t_{dead} values are chosen as 20 mH and 1.5 μs in actual hardware implementation.

Fig. 24(a) and (b) show the system operation waveforms at 7.2 kVac, 12 kW condition, with an output voltage of 230 Vac. Fig. 24(b) is the zoom-in switching cycle waveforms

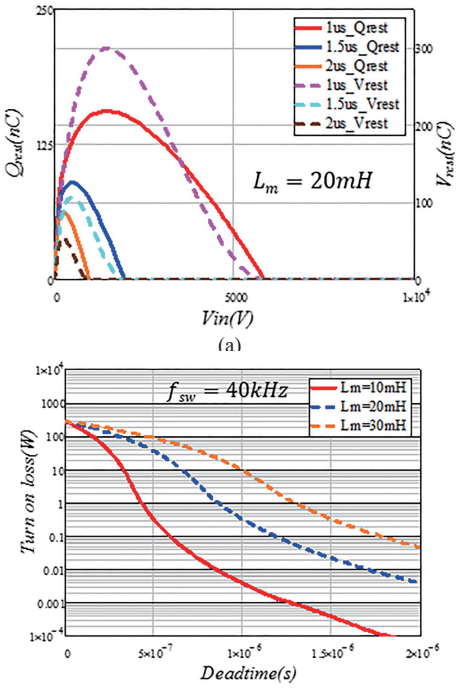

Fig. 22. (a) Residual output charge Q_{oss} and voltage vs input voltage (b) turn on loss vs deadtime.

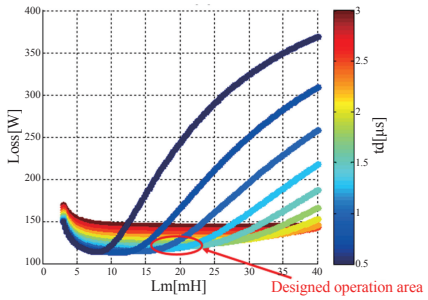

Fig. 23. Total semiconductor loss vs magnetizing inductance and deadtime. Vin=7.2kV, P=13 kW, f=40 kHz.

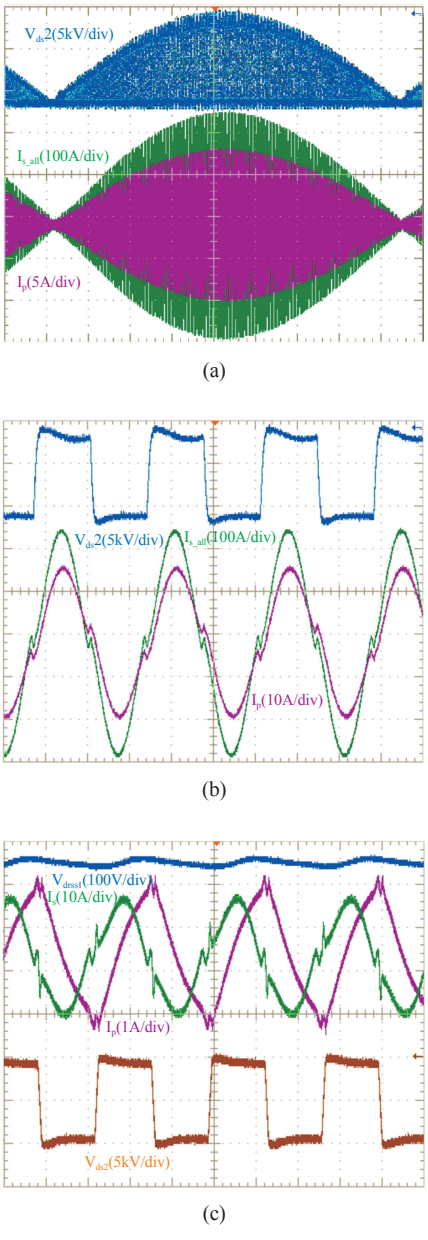

Fig. 24. Steady operation waveforms (a) and (b) V_{MV}=7.2 kV, P_o=12 kW; (c) V_{MV}=7.2 kV, P_o=600 W.

with a switching frequency of 37 kHz. The blue waveform is

the V_{ds} voltage of the MOSFET, which verifies the ZVS operation at 7.2 kV. Fig. 24(c) shows the operation waveforms at 7.2 kV / 600 W condition, which verifies the ZVS operation under at light load.

Efficiency of the developed prototype tested under 3.6 kV and 7.2 kV input voltage conditions are shown in Fig. 25. An efficiency curve of a Type D SST using the same MOSFETs is also added for comparison [13]. The efficiency for the developed Type A SST at 7.2 kV is shown in red curve and is higher than 97% under most load conditions. This figure shows an obvious improvement in efficiency compared with a Type D SST.

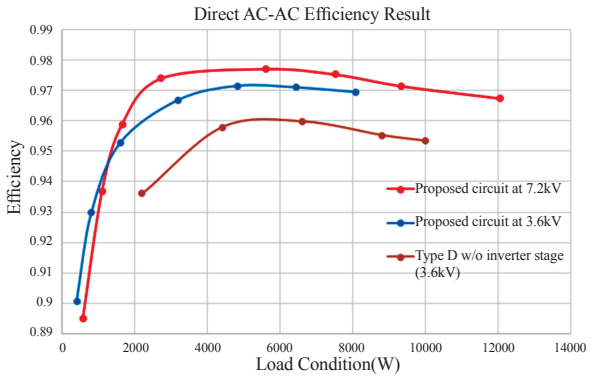

Fig. 25. Measured MV TLSS-SST efficiency, V_{MV}=3.6 & 7.2 kV, P_o from 600 W to 12 kW.

To fully utilize the 15 kV SiC MOSFETs in the direct AC-AC application, a series of optimized designs are presented in Fig. 26 with V_{MV} ranging from 3.6 to 7.2 kVac and switching frequency f_s from 20 to 100 kHz. One can observe from the results that if ZVS is well secured, a potential switching frequency of 100kHz and power over 20 kW can be achieved based on this device at 7.2 kV condition. Since the chip area of the MV switch is less than 2 cm^2, this resprents a remarkable power handling capability of more than 10 kW/cm^2 for the 15 kV SiC power MOSFET in natural convection condition. This can be increased further if forced air and water coolings are used.

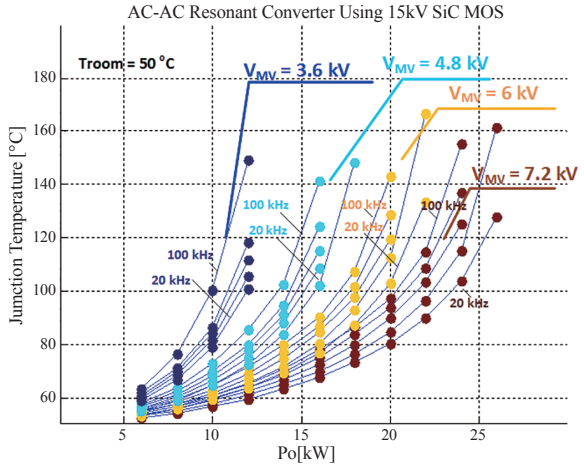

Fig. 26. 15kV SiC MOSFET junction temperature versus power with different f_s and V_{MV} in AC-AC application. Cooling=Natural convection.

IV. Conclusions

This paper reviews the characteristics of 15 kV SiC MOSFET in terms of conduction, switching and thermal performance. Comprehensive guidelines of implementing this device in practical MV applications such as AC-DC, DC-DC, AC-AC are elaborated in detail with an emphasis on device power and frequency handling capability. In hard switching MV AC-DC converters, switching loss dominates which limits the switching frequency to less than 10 kHz or even lower if DC link voltage reaches 12 kV. CRM AC-DC can be used to expand the switching frequency range. In isolated DC-DC and AC-AC applications, ZVS is extremely important and there are well studied topologies to achieve this. With the ZVS technique, the 15 kV SiC MOSFET can operate at frequencies up to 100 kHz and process an amazing amount of power in a small chip area. These results clearly demonstrate that the 15 kV SiC MOSFET is a disruptive and enabling device for a wide range of MV applications.

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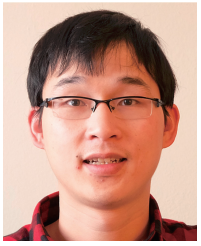

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Opening the Box: Survey of High Power Density Inverter Techniques From the Little Box Challenge

Katherine A. Kim, Yu-Chen Liu, Ming-Cheng Chen, and Huang-Jen Chiu

Abstract—**The Little Box Challenge (LBC) was a competition sponsored by Google and the IEEE Power Electronics Society in 2014-2015, where participants were challenged to design a high power-density single-phase 2 kVA inverter. This paper surveys the designs from eight different participating teams, including academic grant awardees, finalists, and the winners. Inverter topologies, power decoupling circuits, and thermal management strategies are overviewed for each team. Wide bandgap switches were heavily utilized in both the inverter and power decoupling circuits, particularly GaN switches. Most teams utilized a full-bridge inverter with some variations and the most common power decoupling strategy was the use of a synchronous buck converter and a power buffering capacitor. One team used a multi-level inverter approach and a number of teams proposed innovative power decoupling topologies. Heat sinks and active cooling systems, many of which were custom made, were crucial for teams to stay within the 50 °C case temperature limit. The resulting power density of the surveyed teams ranged from 55.8 to 216 W/in^3, all of which exceed the 50 W/in^3 LBC requirement. This paper surveys the approaches for various teams, shares experimental results from the Taiwan Tech team, and highlights some innovations from the teams that participated in the LBC.**

Index Terms—**Higher power density, Little Box Challenge, single-phase inverter, wide bandgap switches.**

I. Introduction

HIGH power density converters are an important trend in power electronics for many modern applications, including electric vehicles and renewable energy. In light of this trend, Google and IEEE Power Electronics Society announced the Little Box Challenge (LBC) in July 22, 2014 to incite innovation and developments for high power density inverters. Specifically, the LBC called for designs and testable prototypes of a single-phase inverter rated at 2 kVA with a power density of at least 50 W/in^3. The LBC provided detailed specifications and testing requirements, detailed in [1]. A grand prize of 1 million USD would be awarded to the team that developed a single-phase inverter with the highest power density that met the requirements.

Google Research also announced that it would provide academic research grants to institutions to support research on high power density converters for the LBC. The academic research grants were awarded in December 2014 [2]. The list of awardees is provided in Table I. Competitors were required to submit a Technical Approach and Testing Application document for their proposed inverter designs by July 22, 2015. Based on those documents, 18 finalists were selected to submit prototypes for testing. The list of finalists is also listed in Table I, however three teams dropped out of the competition before final testing. The prototypes were submitted by October 21, 2015 and subject to testing at the Renewable Energy Laboratory (NREL). In February 2016, the CE+T Power's Red Electrical Devils team from industry was announced as the winner with 142.9 W/in^3 power density, with the Schneider Electric team in second with 96.2 W/in^3, and Virginia Tech's Future Energy Electronics Center in third with 68.7 W/in^3 [3].

The competition results were exciting news that generated positive public attention for the power electronics community [4], but the more significant results are in the innovations and technological advances that came from various teams participating in the LBC. The purpose of this paper is to survey the design approaches and techniques utilized by various teams to achieve the target high power density inverter. Although the Technical Approach documents were shared for all the finalists, they do not generally contain deep technical detail. Fortunately, a number of teams that participated in the LBC have published their designs and results [5]-[12].

This paper summarizes and compares the final LBC designs for the following teams: National Taiwan University of Science and Technology (Taiwan Tech), Texas A&M University (Texas A&M), ETH Zürich !verter (ETH !verter), University of Illinois Urbana-Champaign UIUC Pilawa Group (UIUC), Virginia Tech Future Energy Electronics Center (VT FEEC), Red Electrical Devils, Schneider Electric, and the University of Tennessee (Univ. Tennessee). In Section II, general challenges for high power density inverter designs are discussed. Comparisons of the dc-ac inverter stage, power decoupling design, and thermal management design are given in Section III. A general discussion of the overall approach is provided in Section IV, followed by concluding remarks in Section V.

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TABLE I
PARTICIPANTS IN THE LITTLE BOX CHALLENGE

Academic Grant Awardees	Finalist Teams	Country
University of Colorado Boulder	-	USA
National Taiwan Univerity of Science and Technology	-	Taiwan
Universidad Politécnica de Madrid	-	Spain
Texas A&M University	-	USA
ETH Zürich	!verter	Switzerland & Germany
University of Bristol	-	UK
Case Western Reserve University	-	USA
University of Illinois Urbana-Champaign	UIUC Pilawa Group	USA
University of Stuttgart	-	Germany
Queensland University of Technology	-	Australia
-	Adiabatic Logic*	UK
-	AHED	Germany
-	AMR	Argentina
-	Cambridge Active Magnetics	UK
-	Energylayer	Ukraine
-	Fraunhofer IISB	Germany
-	Future Energy Electronics Center (3rd)	USA
-	Helios*	USA
-	LBC1*	Slovakia
-	OKE-Services	Netherlands
-	Red Electrical Devils (1st)	Belgium
-	Rompower	USA & Romania
-	Schneider Electric Team (2nd)	France
-	The University of Tennessee	USA
-	Tommasi-Bailly	France
-	Venderbosch	Netherlands

*Team dropped out of the competition before final testing.

II. CHALLENGES FOR HIGH POWER DENSITY INVERTERS

A. Magnetics Size Reduction

One major challenge in achieving high power density for any power converters are the size of the magnetics. Magnetic components in power converters are used for basic power conversion, filtering, and galvanic isolation. While these components are difficult to design out of power converters, their physical size is often reduced by increasing operating frequencies [13]. Recently, wide-bandgap (WBG) semiconductor switches have come to market, which have significantly higher switching speeds than traditional Si switches. These WBG switches have allowed for much higher switching frequencies in power converters, which allows the size of the magnetics to be reduced.

B. Thermal Management

Another general challenge in designing high power density converters is thermal management. As the converter size is reduced, losses are dissipated over a smaller volume, which can result in very high temperatures. If the heat is not properly, managed, higher temperatures can reduce component performance or, in extreme conditions, damage components. Thus, thermal management is important at all levels of the design, from the PCB layout to the case enclosure. Fortunately, using WBG switches reduces switching losses compared to Si switches. For this reason, WBG switches are crucial for high power density converters and were heavily utilized in the LBC prototypes.

C. Single-Phase Inverter Power Ripple

While three-phase inverters have steady output power attributed to the power balance between the phases, single-phase inverters have a substantial power ripple at twice the line frequency [14]. Generally, large electrolytic capacitors can be used to store bulk energy to reduce the voltage ripple, but these bulky capacitors limit the power density and reliability of the converter [15]. To address the power ripple problem, a number of passive and active techniques were utilized in the LBC prototypes. This topic attracted a significant amount of research attention that will be further discussed in Section III. B.

III. LBC INVERTER DESIGNS

This paper focuses on three major aspects of single-phase inverters: dc-ac inverter, power decoupling, and thermal management. The different approaches for various LBC teams are outlined and compared in the following sections. Table II summarizes the design aspects for each team.

A. Inverter Power Stage

For the dc-ac inverter power stage, the topology, type of switches, and operating frequencies are examined. For the inverter topology, the standard topology is to use a full-bridge inverter. Most teams used the full-bridge inverter approach with some modifications in the control or how the decoupling circuit interacts with the inverter.

1) Taiwan Tech

The Taiwan Tech team used the standard full-bridge topology, as shown in Fig. 1. However, an asymmetric control scheme was implemented, where the first leg switches at higher frequencies and the second leg switches at a low frequency, carrying out the unfolding operation. The high-frequency leg switched at a range of 25 to 800 kHz and the low-frequency leg switched at 120 Hz, twice the line frequency. The switch used in the inverter stage was the GaN Systems GS66516T,

TABLE II
INVERTER DESIGN ASPECTS

Team	Topology	Switches	Switching Frequency	Power Decoupling	Thermal Management
Taiwan Tech	Full-bridge, asymmetric control	GaN Systems, GS66516T, 650 V, 60 A	DC-AC: 25-800 kHz DC-DC: 200-680 kHz	Active, synchronous buck to buffer capacitor	Six fans, heat sink connected to aluminum case
Texas A&M	Full-bridge, 3rd leg decoupling circuit	GaN Systems, GS66508P, 650 V, 30 A	100 kHz	Active, decoupling circuit similar to inverter 3rd phase, as in [5]	Unspecified cooling system with heat sink
ETH !verter	Full-bridge, interleaved paralleled legs	Infineon, CoolGaN, 600 V	200 kHz-1 MHz	Active, synchronous buck to buffer capacitor	forced air cooling by utilizing high fin-number heat sinks and six ultra-flat blowers
UIUC	Multilevel, 7-level flying capacitor inverter	EPC, GaN EPC2003, 150 V, 48 A	Switch: 120 kHz Effective: 720 kHz	Active, series-stacked buffer architecture	Copper enclosure, 2 mm tall heat sink fins, 6 radial fans
VT FEEC	HERIC	DC-DC: Transphorm TPH3002LD, GaN, 600 V, 9 A DC-AC: GaN Systems, GS66516T, 650 V, 60 A	DC-AC: 60 kHz DC-DC: 400 kHz	Active, interleaved buck as first power stage	Copper enclosure, 10 micro-fans on side wall
Red Electrical Devils	Full-bridge, paralleled legs	GaN Transistors	35-240 kHz	Active, synchronous buck to buffer capacitor	Copper enclosure, with gap-pad
Schneider Electric	Full-bridge	SiC MOSFETs, TO247 package	45 kHz	Active, ripple filter full-bridge to buffer capacitor	Heat sink over power switches with small fan, two air inlets on case
Univ. Tennessee	Full-bridge	GaN Systems, GS66508T, 650 V, 30 A	100 kHz	Passive, notch filter	Heat sink over power switches, two small fans, air inlets on top and side

rated at 650 V and 60 A. The main choice for employing an asymmetric control strategy is to reduce the total switching losses compared to standard PWM control, which both increases efficiency and reduces heat generation.

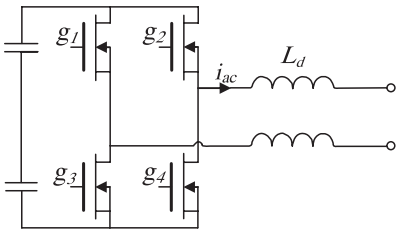
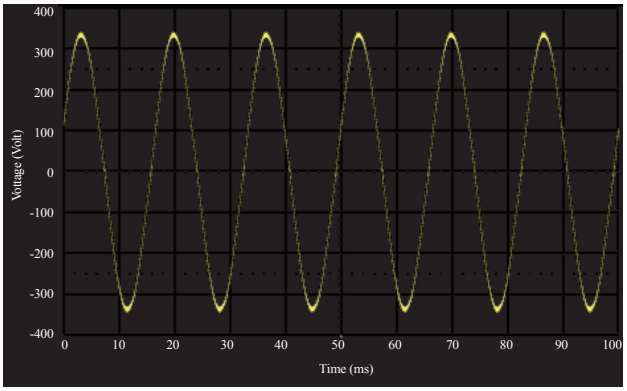


Fig. 1. Basic full-bridge inverter topology.

As an example of the inverter output performance achieved with this topology, Fig. 2 shows the experimental waveforms at the full 2 kW power rating. Fig. 2(a) shows the ac output voltage at 231.7 V rms with 1.29% THD, and Fig. 2(b) shows the ac output current at 8.6 A rms with 1.30% THD. The output shows very little distortion and meets the LBC requirements.

2) Texas A&M

The Texas A&M Team also uses a full-bridge topology for the inverter stage. The decoupling circuit is connected in parallel to the inverter input, such that it looks similar to a 3rd leg of the inverter, but the decoupling circuit will be discussed in the following power decoupling section. After a number of different wide bandgap switches were compared in [5], the GaN Systems GS66508P, rated at 650 V and 30 A, was selected for the inverter design. The switches operate at a switching frequency of 100 kHz [5].



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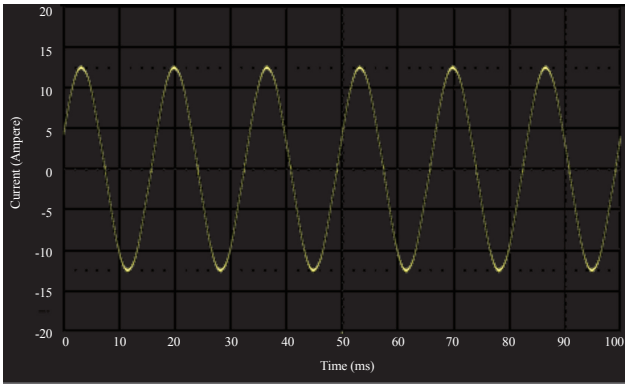


(b)

Fig. 2. Ac output voltage (a) and current (b) for the Taiwan Tech team's full-bridge inverter at full power.

3) ETH !verter

The ETH !verter team used an interleaved full-bridge inverter with four inverter legs, as shown in Fig. 3, where the power for each phase is split over two legs. The inverter is controlled in triangular current mode (TCM), such that soft switching is achieved to reduce switching losses. The switches used are Infineon CoolGaN^{TM} transistors, rated at 600 V, switching at a frequency range of 200 kHz to 1 MHz, depending on the output voltage [6], [7].

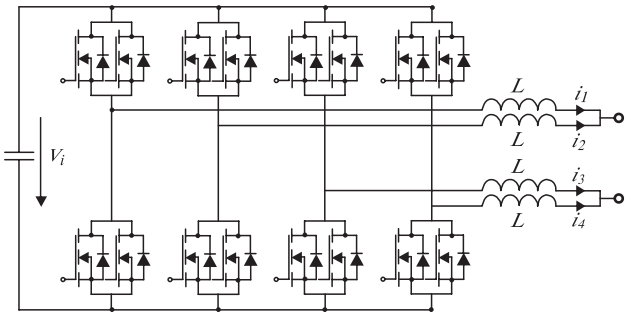


Fig. 3. Parallel full-bridge inverter topology.

4) UIUC

Different from other teams, the UIUC team chose a multi-level topology rather than the standard full-bridge topology. The main motivation for using a multilevel inverter is its lower inherent THD, which means that the EMI filter size can be reduced, leading to higher overall power density. The design used for the LBC was a 7-level flying capacitor topology, which consists of 5 flying capacitors, an inductor, an output capacitor and four switches, is shown in Fig. 4. The switches used were the EPC EPC2003, rated at 150 V and 48 A. Compared to the full-bridge topology, this approach has significantly more switches, which requires more complex control. The transistors switch at 120 kHz, but the effective frequency of the multilevel converter is 720 kHz [8].

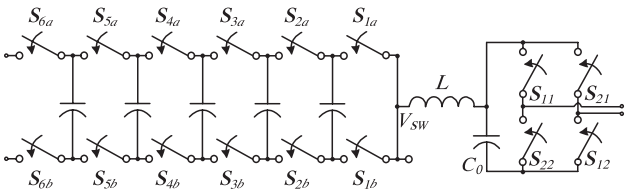


Fig. 4. 7-level flying capacitor inverter topology.

5) VT FEEC

The VT FEEC team used an inverter topology with the trade name HERIC, which stands for highly efficient and reliable inverter concept. The inverter topology is shown in Fig. 5 and utilizes two series-connected switches across the inverter output. For switches, the team used the GaN Systems GS66516T, rated at 650 V and 60 A. The switching frequency for the inverter was 60 kHz [9].

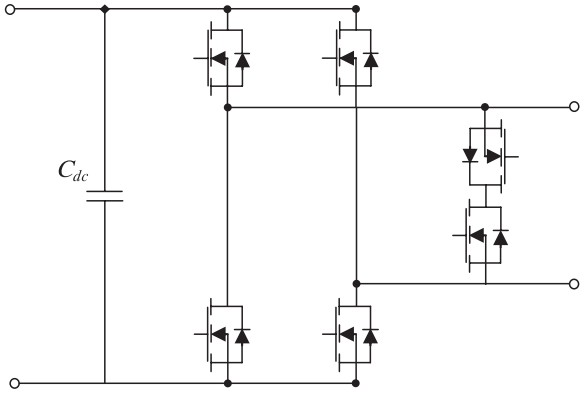


Fig. 5. HERIC inverter topology.

6) Red Electrical Devils

The Red Electrical Devils team used the a full-bridge inverter, with four inverter legs (two legs for each side of the output. The technical document [10] states a five-legs topology, but this is simply four legs for the parallel full bridge and one leg for decoupling. The approach is essentially the same as the ETH !verter team, shown in Fig. 3. Although GaN transistors were used for all bridge legs, neither the part number nor the manufacturer were stated [10]. The switching frequency ranged between 35 and 240 kHz to achieve soft switching, which helped in reducing losses.

7) Schneider Electric

The Schneider Electric team used a full-bridge inverter operating in PWM mode, but details about the control strategy are not given in their technical approach document [11]. For the four switches in the inverter, SiC MOSFETs in a TO247 package were used (exact part number is not given in [11]) and the switching frequency was 45 kHz. This is one of the few teams that used SiC switches rather than GaN switches.

8) Univ. Tennessee

The Univ. Tennessee team used the standard full-bridge inverter where the switches are hard-switched rather than soft-switched. The switches used were the GaN Systems GS66508T, rated at 650 V and 30 A. The switching frequency was 100 kHz and the inverter operation is controlled using unipolar continuous sinusoidal pulse-width modulation [12].

B. Power Decoupling Designs

The approaches for power decoupling in the single-phase inverter varied greatly among the teams and was an area of innovation for many teams. While the traditional approach is to use passive, bulky components, almost all teams took active decoupling approaches in order to reduce the volume. The decoupling circuits are overviewed for each team.

1) Taiwan Tech

The Taiwan Tech team utilized a synchronous buck converter that transfers power to and from a buffer capacitor to decouple the power, as shown in Fig. 6. This allows power to

vary at double-line frequency without causing voltage swings in the inverter input voltage. The switches used in the decoupling buck converter are also GaN Systems GS66516T. The switching frequencies varies from 200 to 680 kHz according to the current level. The buck converter operates in this way to achieve ZVS mode to reduce losses and heat generation.

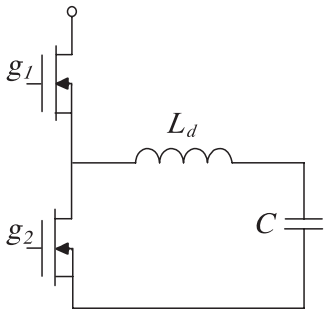
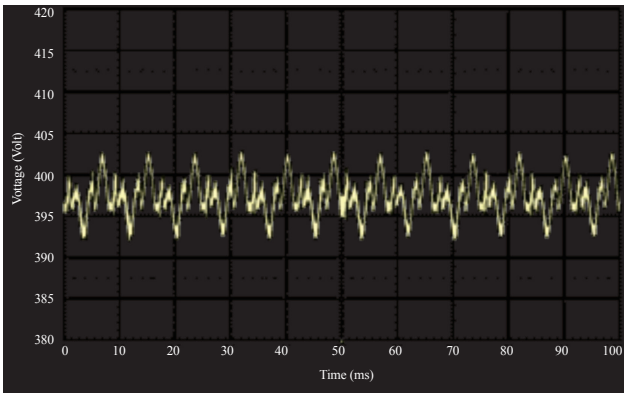


Fig. 6. Synchronous buck power decoupling topology.

The effectiveness of the synchronous buck power decoupling circuit to reduce the ripple at the dc input for the Taiwan Tech team is shown in Fig. 7. Experimental results were taken at full power. Fig. 7(a) shows the voltage ripple of the dc input and Fig. 7(b) shows the current ripple of the dc input. As shown, the voltage ripple is 10.8 V peak-to-peak and the current ripple is 0.86 A peak-to-peak, which shows good performance of the synchronous buck power decoupling circuit.



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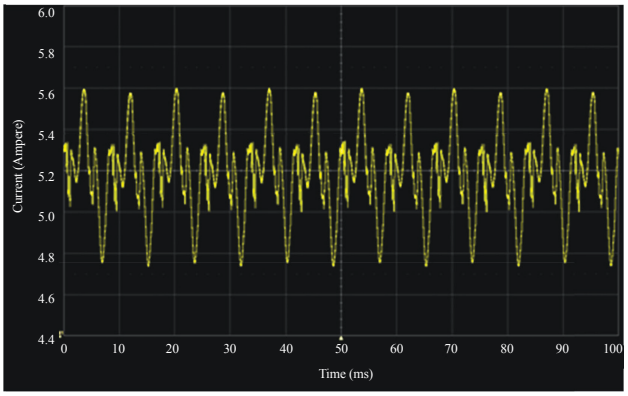


(b)

Fig. 7. Input voltage (a) and current (b) for dc input to the inverter for the Taiwan Tech team's design at full power.

2) Texas A&M

The Texas A&M team focused mainly on the power decoupling circuit and proposed a circuit that connects from the dc input to one line of the ac output. The proposed decoupling circuit, shown in Fig. 8, is a kind of half-bridge power decoupling topology that is fully detailed in [5]. The advantages of this topology are that the decoupling capacitor carries the ac voltage such the capacitor is fully utilized and its size is minimized. Further, compared to a full-bridge inverter decoupling circuit, which uses four switches, this solution uses only two switches. The decoupling circuit can also be thought of as a third leg of the inverter, such that it helps to balance out the power, which also distributes power dissipation in the inductors [5]. This decoupling approach was developed specifically for the LBC, and was a unique approach.

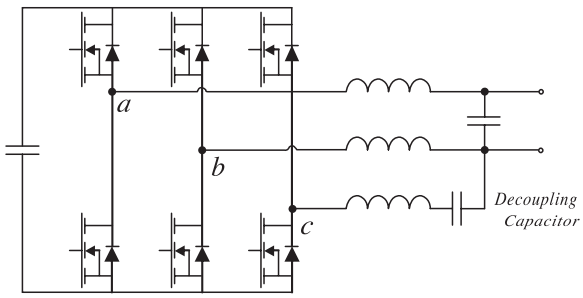


Fig. 8. Half-bridge power decoupling topology, as in [5].

3) ETH !verter

For power decoupling the ETH !verter team also used a synchronous buck converter to buffer power to and from a capacitor, as shown in Fig. 6. Although his method does not fully utilize the capacitor's capacity, the team employs high energy-density ceramic capacitor to reduce overall size [6], [7].

4) UIUC

The UIUC team utilized a unique active power decoupling

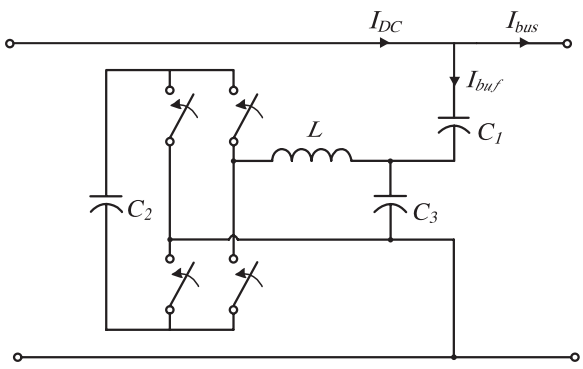


Fig. 9. Series-stacked power decoupling circuit topology.

technique that utilizes a series-stacked type of differential power processing architecture, as shown in Fig. 9. The advantage of this topology is that the energy storage capacitor's capacity is fully utilized such that the capacitor's size can be minimized and power losses can be minimized by reducing the amount of power processed in transferring power to and from the storage capacitor. One tradeoff is that there are four switches rather than two used in many of the other power decoupling circuits [8]. However, the UIUC team's overall design did not shy away from complex switching circuits, which resulted in a small overall converter volume.

5) VT FEEC

The VT FEEC team utilized a 2-phase interleaved buck converter as a first dc-dc stage before the dc-ac stage. The switch for the buck converter was Transform TPH3002LD, a GaN switch rated at 600 V and 9 A, and the diode was a SiC diode, Cree C3D1P7060Q. The converter switched at 400 kHz, which helps reduce the inductor size [9].

6) Red Electrical Devils

Similar to other teams, the Red Electrical Devils used a synchronous buck converter for power decoupling, as shown in Fig. 6. Ceramic capacitors were used as the buffer capacitor to maintain a small size. Although not clearly specified in the [10], the same GaN switches and switching frequency range as the inverter stage was likely utilized for the buck converter as well.

7) Schneider Electric

The Schneider Electric team used a low-voltage full-bridge inverter in series with the inverter input voltage, which they called an active ripple filter. This circuit requires four switches, rather than two, as shown in Fig. 10. Silicon MOSFETS were used rather than wide-bandgap switches [11].

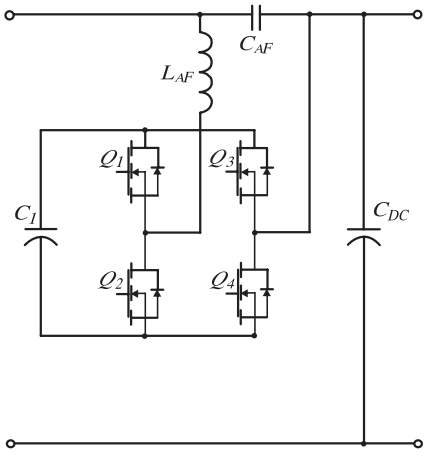


Fig. 10. Active ripple filter in series with the inverter input capacitor.

8) Univ. Tennessee

Different that the other teams, the Univ. Tennessee team was the only team to choose a passive power decoupling method, rather than an active method. A resonant notch filter tuned to 120 Hz was used. This filter allowed for high attenuation at the target frequency but can be implemented with a relatively small capacitor size [12].

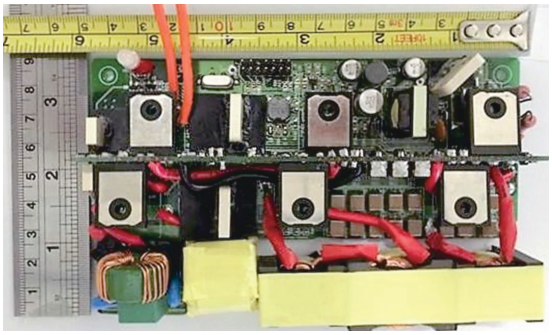
C. Thermal Management

Most teams assumed that their inverter operated at an efficiency of around 97%, such that at least 60 W of heat would need to be dissipated. In general, all teams concluded that forced air flow, using fans, was necessary and conducted detailed thermal modeling for their LBC designs.

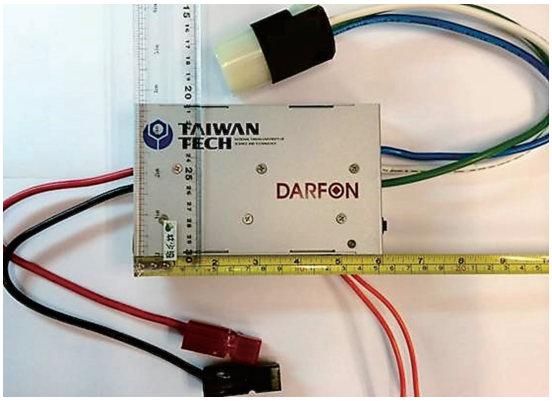
1) Taiwan Tech

For heat dissipation, Taiwan Tech used multiple fans at the air inlet and outlet of the enclosure. A fan was also used near the GaN switches to ensure sufficient airflow around them. In total six fans were utilized. A heat sink was also utilized near the switches, which was thermally linked to the aluminum case to further improve heat dissipation.

The prototype of the LBC inverter prototype for the Taiwan Tech team is shown in Fig. 11. The circuit board is shown in Fig. 11(a), along with the top-view of the prototype in Fig. 11(b), and the side-view in Fig. 11(c). As shown, the dimensions of the enclosure are 5.985 in by 3.685 in x 1.000 in, which is a volume of 22.055 in^3. In experimental testing at full load with an ambient temperature of 29 °C, the maximum enclosure temperature was 57 °C, which is below the 60 °C requirement for the LBC.



(a)



(b)

Fig. 11. The internal circuit board (a), case top-view (b), the Taiwan Tech team's LBC prototype.

(c)

Fig. 11. (*Continued*..) Case side-view (c) the Taiwan Tech team's LBC prototype.

2) Texas A&M

The cooling system for the Texas A&M team is only generally described in [5]. A heat sink of dimensions 60 mm by 25 mm by 24 mm is utilized. The use of fans is not explicitly stated, but are likely incorporated in the cooling system as the cooling system and auxiliary circuits were cited as contributing to the inverter's size.

3) ETH !verter

For thermal management, for the ETH !verter team also utilizes forced air cooling by utilizing high fin-number heat sinks and six ultra-flat blowers. The relatively flat cooling system in placed on the top of the enclosure to facilitate the natural convection flow [6], [7].

4) UIUC

The cooling system for the UIUC team incorporates an enclosure that is milled out of copper with heat-sink fins on the exterior. Six small blower fans are also integrated on the outside of the enclosure. Testing results in [8] state a maximum case temperature of 57 °C.

5) VT FEEC

The VT FEEC team managed the heat by using forced-air cooling and the case as a heat sink. The case was made out of copper to act as a heat sink and ten 0.1 W micro-fans forced air across fins mounted on one side wall of the case. Testing results in [9] shows the maximum case temperature as 53.6 °C.

6) Red Electrical Devils

The Red Electrical Devils team put a significant amount of attention into the thermal management design. Heat sinks were custom made by electrical discharge machining and were connected to an 0.012-in-thickness PCB using micro-spring contacts. Silicone foam was used to spread the GaN contact pressure evenly over the heatsink. The heat sink was made of copper in a honeycomb pattern that is layered between other component layers. The team also employed a gap-pad between the external copper enclosure and the internal copper shielding. The purpose is to extract heat from the hottest components without creating local hot spots in the external enclosure. An axial fan was placed in the middle of the front plate to facilitate forced air flow through the various converter layers [10].

7) Schneider Electric

The Schneider Electric team used heat sink mounted on the power switches with a small fan directly above the heat sink [11]. Two outlets on opposite faces of the enclosure to allow airflow.

8) Univ. Tennessee

For thermal management, the Univ. Tennessee team utilized a heat sink above the GaN switches with thermal interface materials between the switches and heat sink. There are two main fans above the heat sinks with air inlets on the top and side of the enclosure. Results in [12] show that the maximum case temperature is just below the 60 °C requirement for the LBC.

IV. Discussion

Performance of the various designs is summarized in Table III for the efficiency, dimensions, volume, and power density. Note that because the performance of all the final prototypes tested for the LBC were not all made public, the values are based on either technical documents or papers published about the inverter.

From the inverter designs outlined in Table II, most teams utilized a full-bridge topology, with some variations, like the HERIC or using parallel legs. Only the UIUC team utilized a multi-level converter, which had the most number of switches by far. WBG semiconductor switches were a fundamental part of all designs due to achieve high density. All but one team used GaN switches and only the Schneider Electric team used SiC switches. The switching frequencies for fixed-frequency approaches ranged from 45 to 120 kHz while the variable frequency strategies ranged from 25 kHz up to 1 MHz. The ranges are relatively reasonable and did not push the present-day limits for switching, mainly to reduce heat generation from switching loss. Further, many teams employed soft switching methods to further reduce switching losses.

The power decoupling methods showed a wider variety and a number of innovative solutions. Only the Univ. Tennessee team used a passive solution and the rest utilized active circuits to reduce the size of the passives and magnetics. The synchronous buck converter connected to a buffer capacitor was the most common active power decoupling solution, but the half-bridge power decoupling topology used by the Texas A&M team, the series-stacked power decoupling circuit used by the UIUC team, and active ripple buffer used by the Schneider Electric team were unique approaches that fully utilized the buffer capacitor. These approaches are worth further analysis and investigation for future high power density designs.

For the surveyed designs, the thermal management normally involved detailed modeling, analysis, and a customized cooling system. Based on the expected power losses, forced-air cooling using fan and heat sinks was the standard approach. Three of the teams used copper enclosures, utilizing the case itself as a heat sink. For the fans, many of the teams used multiple small fans that directed airflow evenly across the enclosed converter.

TABLE III
INVERTER PERFORMANCE

Team	Efficiency	Inverter Dimensions (in)	Volume (in^3)	Power Density (W/in^3)	Source
Taiwan Tech	96.5% (CEC)	6.00 x 3.69 x 1.00	22.06	90.68	reported here
Texas A&M	98% (conditions unspecified)	5.3 x 5.2 x 1.3	35.8	55.8	[5]
ETH !verter	95.07% (CEC)	-	14.8	134	[6], [7]
UIUC	97.0 %(CEC)	4.02 x 2.42 x 0.95	9.24	216	[8]
VT FEEC	98.59% (peak)	-	29.1	68.7	[9], [3]
Red Electrical Devils	not provided	2.5 x 1.615 x 3.41	13.77	145.2	[10], [3]
Schneider Electric	not provided	-	20.8	96.2	[11]
Univ. Tennessee	96.9% (CEC)	4.38 x 3.47 x1.29	19.6	102	[12]

Although the first, second, and third winners of the LBC were the Red Electrical Devils, Schneider Electric, and VT FEEC teams, respectively, a number of other teams showed power densities higher than the winners. Because the prototype testing for the LBC was not public, it is not clear which specifications the teams that claimed higher power density failed to meet. Based on this survey, the winning teams all seemed to use straight-forward inverter topologies and had robust thermal designs with extra margin from the 60 °C case limit, which may have been an advantage during on-site testing in a new environment.

Based on the power densities in Table III, the highest power density was the UIUC team, which used the 7-level flying capacitor inverter and series-stacked power decoupling circuit. That design made a clear trade-off of using more switches in order to reduce magnetics, even if it meant more complicated control. Based on the results of the LBC and the survey provided here, the first step towards higher power density inverter seems to be through the standard full-bridge topology and more well-established power decoupling techniques, but the future steps may move towards multi-level inverters and newer power decoupling topologies to reach the next level of high power density inverters.

V. CONCLUSION

This paper surveyed the designs for eight teams that participated in the LBC including: Taiwan Tech, Texas A&M, ETH !verter, UIUC, VT FEEC, Red Electrical Devils, Schneider Electric and University of Tennessee. The information surveyed here was based on the technical approach documents from the LBC and from papers published by participating teams. WBG switches, especially GaN, were widely used in both the inverter and power decoupling stages. Soft-switching approaches were also heavily utilized to reduce switching losses and associated heat generation. Various active power decoupling topologies, including a number of newly proposed circuits, were used to decrease the size of passive components used in traditional single-phase inverters. Thermal management was a crucial challenge for high power density and teams utilized custom heat sink solutions with forced cooling using small fans. Although the LBC officially had only one official winner, the contribution of the competition was not just the design of the winning team, but the various approaches and design from the many teams that participated in the LBC.

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Analysis and Cell-Level Experimental Verification of a 25 kW All-SiC Isolated Front End 6.6 kV/400 V AC-DC Solid-State Transformer

Jonas E. Huber, Julian Böhler, Daniel Rothmund, and Johann W. Kolar

***Abstract*—Solid-state transformers (SSTs) could serve as interfaces between a medium-voltage (MV) AC grid and a low-voltage (LV) DC load or source, i. e., could be employed in applications with power supply character such as traction auxiliary supplies or rack-level power supplies in future datacenters. For handling the high input-side AC voltage and output side current, SSTs are typically realized as input-series output-parallel (ISOP) arrangements of multiple converter cells, whereby each cell comprises a medium-frequency isolation stage. This paper presents such a multi-cell 25 kW all-SiC MVAC-LVDC SST (6.6 kV AC to 400 V DC) based on the isolated front end (IFE) approach, which is an interesting alternative to the isolated back end (IBE) configuration mainly discussed in literature so far. The IFE concept is briefly explained, the main component stresses are derived, and a converter cell prototype is designed and tested. The 5 kW prototype cell features a power density of 1.5 kW/l (24.6 W/in3) and a measured peak efficiency of 97.5%. This is significantly higher than previously published data for IFE-based SSTs, and in the same range as what has been reported recently for industrial IBE-based SSTs. Thus, this paper confirms that the IFE approach can be a feasible and interesting alternative for realizing MVAC-LVDC SST systems with low complexity.**

***Index Terms*—Isolated AC-DC converters, isolated front end, isolated power factor correction, solid-state transformer.**

I. Introduction

VARIOUS low-voltage (LV) DC loads or sources with higher power ratings could benefit from a direct connection to the medium-voltage (MV) AC grid. Such applications with power supply character are, e. g., future rack-level power supplies for datacenters with power flow from the AC to the DC side, larger PV installations with power flow from the DC to the AC side, or battery storage systems requiring bidirectional power flow. Especially for cases where the available space and/or weight for the power conversion equipment is constrained (e. g., datacenters [1], [2], traction applications [3], future shipboard power systems [4], or possibly future all-electric aircraft [5]), solid-state transformers (SSTs) that realize the galvanic separation by means of medium-frequency (MF) transformers are a highly interesting option [6]. In addition, such systems could operate with a power factor close to unity at the MV grid and/or minimize the effects on the mains.

A. Isolated PFC Functionality Partitioning

Realizing galvanic isolation of input and output, (single-phase) power factor correction (PFC) functionality, and output voltage control requires four distinct tasks [7]: folding (rectification) of the AC grid voltage into a |AC| voltage, shaping of the input current (current shaping, CS), galvanic isolation (I), and output voltage regulation (VR). As shown in Fig. 1, there are different variants of how these functional blocks can be arranged and/or combined.

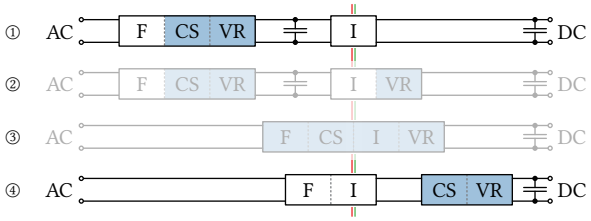

Fig. 1. Partitioning of the tasks required to perform isolation, PFC, and output voltage control: folding (F), current shaping (CS), isolation (I), and output voltage regulation (VR); blue stages are controllable.

Variant ① interfaces the AC grid with a folding (rectifier) stage with boost functionality that draws an appropriately shaped current from the grid to generate a regulated DC link voltage, which is then processed by a unregulated isolated DC-DC converter stage, e. g., by a half-cycle discontinuousconduction-mode (HC-DCM) series-resonant converter (SRC) [8], [9]. The isolation stage is positioned after the main controlling stage. Hence, the concept can be referred to as an isolated back end (IBE) system. Alternatively, the isolation stage can be controllable as well (variant ②), thereby facilitating a directly regulated output voltage, however, at the price of increased system complexity. Fig. 2(a) shows a realization example of such an IBE system.

Variant ③ is a fully integrated isolated AC-DC dual-active bridge converter (cf., e. g., [10]). Whereas such single-stage power conversion potentially achieves low losses, the complexity is high, especially considering a multi-cell arrangement.

Finally, variant ④ features an inverted sequence of the functional blocks compared to variant ① : a folding and iso-

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lation stage is directly connected to the MV AC grid, but the current shaping and the voltage regulation are performed by a controlled |AC|-DC conversion stage on the LV side. Thus, this arrangement is referred to as an *isolated front end* (IFE) system. Fig. 2(b) shows a realization example of such an IFE system.

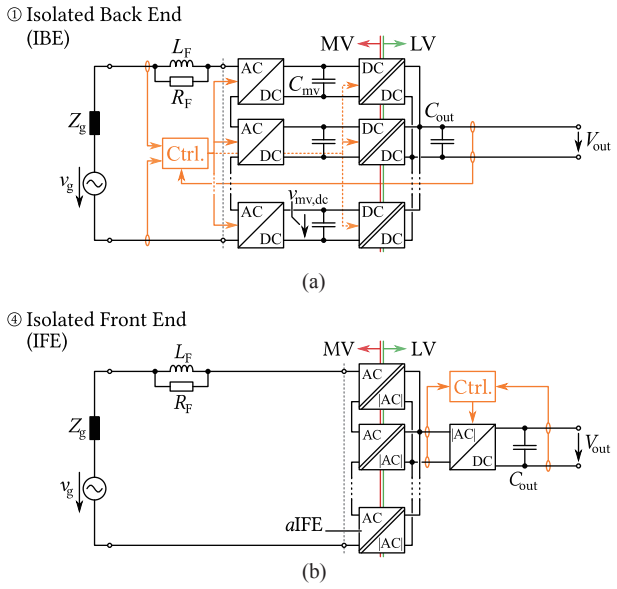

Fig. 2. Realization examples (a) of an IBE AC-DC SST, and (b) of an IFE AC-DC SST, both in multi-cell ISOP configuration.

B. Isolated Back End Multi-Cell SSTs

Fig. 2(a) shows a typical realization example of a multicell IBE SST, whereby an input-series output-parallel (ISOP) arrangement of converter cells is employed in order to handle the high voltage at the MV AC side and the high currents at the LV DC side. Such an IBE SST using an ISOP configuration has been first patented in 1996 [11], and since then been employed in various applications ranging from a 1.2 MVA SST for a locomotive achieving an AC-DC efficiency of 96% [3] to a 25 kW MVAC-LVDC power supply for datacenters with a peak AC-DC efficiency of 96.5% [1].

C. Isolated Front End Multi-Cell SSTs

In contrast, even though the IFE approach has first been proposed in 1985 for a traction application [12], it has so far not been given much attention in the engineering community. There are only recent publications discussing IFE-based multicell converter concepts with hard-switched isolation stages (i. e., non-resonant isolation stages), considering cascaded converter cells [13] and/or multi-winding transformers [14]. On the other hand, the application of an isolated HC-DCM SRC in AC-AC configuration, which allows for soft-switching operation of the power semiconductors, dates back to 1969 [8]. An ISOP configuration of such AC-AC conversion cells to realize a low-complexity AC-AC SST has been patented recently by GE [15]. The combination of these two ideas, i. e., the IFE approach and the AC-AC (or, specifically, AC-|AC|) operation of the soft-switched HC-DCM SRC converter has finally been proposed in 2013 by Han et al. [16], [17] to realize a multicell AC-DC SST, thereby demonstrating the feasibility of an IFE-based multicell SST in ISOP configuration. However, the corresponding IGBT-based small-scale (2 kVA) prototype achieved only a comparably low efficiency of 83.6%. Fig. 2(b) shows a typical realization of a multi-cell IFE SST. It should be noted that the entire control is handled on the LV side, which is in stark contrast to the IBE SST, whose control is hence more complex [7].

D. Scope of the Paper

In the scope of a research program funded by the Swiss government [18], an all-SiC realization of a 25 kW IFE SST (6.6 kV AC to 400 V DC)—the Swiss SST (S^3T)—is investigated, whereby a slightly simplified topology (no individual filter elements on the cells' AC sides as in [16], [17]) is considered [19]. TABLE I gives detailed specifications of the system. Continuing the research on IFE-based SST systems described in [7] and in [20], this paper first briefly describes the IFE concept in Section II. Then, Section III discusses the design and testing of one of the S^3T's five converter cells realized with latest silicon carbide (SiC) power semiconductors. Based on the measurement results, the IFE SST is finally evaluated against an IBE SST with same rated power [1]. Therefore, this paper contributes first a condensed overview on the IFE concept and its comparative evaluation against the well-known IBE approach. Second, the experimental part demonstrates that IFE-based AC-DC SST systems can achieve similar peformance as their counterparts employing the IBE approach. Finally, Section IV concludes the paper and gives an outlook on future research.

II. IFE Operation Principle

As indicated in Fig. 2(b), the S^3T features an ISOP configuration of converter cells, i. e., autonomous AC-|AC| isolation (front end) stages (*a*IFE), and a |AC|-DC boost converter stage. This boost converter stage can also be realized using several paralleled converters, e. g., with one boost converter per *a*IFE cell, as is considered in the following. Fig. 3 shows the detailed topology of one such converter cell consisting of an AC-|AC| *a*IFE and a |AC|-DC boost stage. Fig. 4 shows the corresponding key waveforms. The operating principle of the IFE is briefly explained in the following based on these figures; for a more detailed description please refer to [7].

The *a*IFE stage is realized as an SRC operated in HC-DCM, which has the property of tightly coupling its terminal voltages in open-loop operation (cf. [8], [9], [21] for details). On its MV side, the *a*IFE cell features a half-bridge with bidirectional switches to enable an AC input voltage, i. e., direct connection to the AC grid, by combining the folding of the grid voltage and the high-frequency switching for the

SRC operation. The second, capacitive AC-side leg consists of two (small) resonant capacitors, C_{r1} and C_{r2}. Hence, the envelope of the switched transformer voltage, v_T, is proportional to the grid voltage, and a scaled and rectified version of the grid voltage, v_{lv}, is obtained after rectification on the secondary side (active rectification is employed in order to reduce conduction losses). Accordingly, the *a*IFE is essentially acting as an isolated AC-|AC| converter.

The magnetizing current of the transformer, i_M, can be utilized for zero-voltage switching (ZVS) in order to reduce the switching losses and improve the EMI signature. However, since the switched voltage is varying over the grid period, the current available for ZVS varies, and so does the effective output capacitance of the MOSFETs. As comprehensively discussed in [20], it is nevertheless possible to realize ZVS during most of the grid period by properly designing the magnetizing inductance and the interlock time of the bridges; if a variable interlock time is employed, ZVS can be realized for the entire grid period (cf. also Section III and Fig. 5).

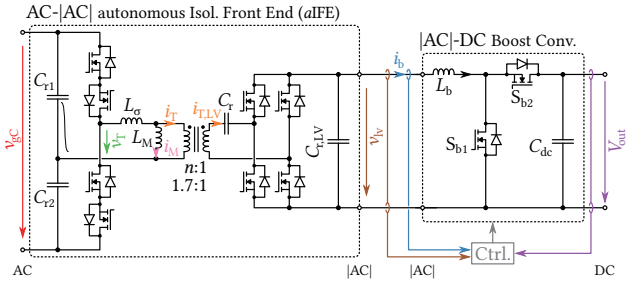

Fig. 3. Circuit schematic of one IFE converter cell. Note that C_{r1}, C_{r2} and $C_{r,LV}$ are resonant capacitors, not constant-voltage DC link capacitors. Fig. 4 shows corresponding waveforms.

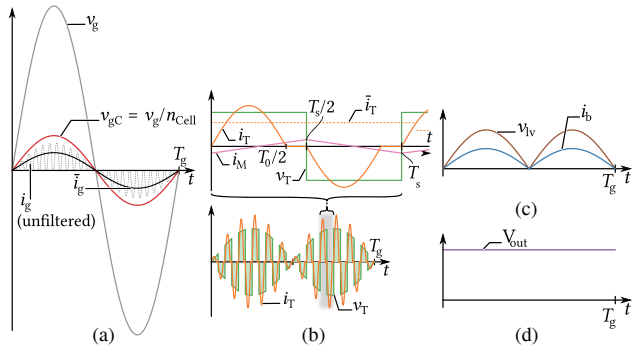

Fig. 4. Qualitative key waveforms of the IFE cell depicted in Fig. 3. (a) Cell AC input voltage v_{gC}, which is a fraction of the grid voltage due to the input-series connection of five cells; (b) HF transformer waveforms; (c) boost converter |AC|-side waveforms; (d) DC output voltage.

The input current, i_b, of the non-isolated |AC|-DC boost converter connected to the *a*IFE stage's LV |AC| terminals can be controlled such as to be in phase with v_{lv} and of appropriate magnitude to maintain the output DC voltage at a given value. Note again that thereby the entire control, including measurements, can be realized solely on the LV side of the converter. Since the *a*IFE only contains switching frequency energy storage elements, the power flow impressed by the |AC|-DC converter is directly translated to the grid. The local average value of the resonant current pulses, $\bar{i}_T$, is proportional to the boost inductor current, i_b (and hence also to the grid current, i_g), which can be assumed to be constant during a switching period. Neglecting the minor reactive power consumption of the capacitive leg, this results in unity power factor operation.

III. Prototype and Experimental Results

Based on these considerations and the specifications given in TABLE I, a prototype of a single converter cell of the S^{3}T IFE SST has been designed, constructed and tested.

A. Key Component Stresses

The stresses of the main components can be calculated analytically, which provides a basis for the system design [7].

TABLE I
Specifications of the S^{3}T and of the Converter Cell Prototype

Nom. powr, P	25 kW	Output volt., V_{out}	400 V
MV AC volt., V_N	6.6 kV	Number of cells, n_{Cell}	5
Cell power, P_{cell}	5 kW	Cell AC volt. (ampl.)	1.08 kV
SRC res. freq., f_0	52 kHz	SRC sw. freq., f_s	50 kHz
Turns ratio, n	1.7	Boost sw. freq., $f_{s,b}$	75 kHz

In a cascaded cells system, the number of required cells follows from the peak phase voltage, $\sqrt{2}V_{ph} = \sqrt{2/3}V_N$, the semiconductor blocking voltage capability, $V_{b,MV}$, and its utilization, u, as

$$n_{cell} = \frac{\sqrt{2}V_{ph}}{uV_{b,MV}}. \quad (1)$$

With $n_{cell} = 5$, the considered 1700 V SiC MOSFETs are utilized to about 65%, which is feasible regarding reliability [22].

1) Transformer: Assuming unity power factor operation, the instantaneous power of the single-phase system at the SST's AC side is

$$p_g(t) = 2P\sin(2\pi f_g t)^2. \quad (2)$$

Hence, the transformer RMS current of the IFE converter cell can be derived starting with the relation

$$\bar{i}_T(t)\cdot\bar{v}_T(t) \stackrel{!}{=} \frac{\bar{p}_g(t)}{n_{cell}}, \quad (3)$$

where $\bar{x}$ denotes a local average value over half a switching cycle of the SRC. In the case of a half-bridge configuration (factor 1/2),

$$\overline{v}_{\mathrm{T}}(t) = \frac{\sqrt{2}}{2n_{\mathrm{cell}}} V_{\mathrm{ph}} \sin(2\pi f_{\mathrm{g}} t) \tag{4}$$

holds, and thus the local average value of the MV side transformer current in a single cell becomes

$$\overline{i}_{\mathrm{T}}(t) = \frac{2\sqrt{2}P}{V_{\mathrm{ph}}} \sin(2\pi f_{\mathrm{g}} t). \tag{5}$$

Assuming piecewise sinusoidal transformer current pulses, the relation between local average and local RMS values is given by (cf. [9])

$$\tilde{i}_{\mathrm{T}}(t) = \frac{\pi}{2\sqrt{2}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}} \cdot \overline{i}_{\mathrm{T}}(t), \tag{6}$$

where f_0 and f_s are the resonant and the switching frequency of the SRC stage, respectively. The transformer RMS current over a grid period follows then as

$$\tilde{I}_{\mathrm{T}} = \sqrt{2f_{\mathrm{g}} \int_0^{\frac{1}{2f_{\mathrm{g}}}} \tilde{i}_{\mathrm{T}}(t)^2 dt} = \frac{\sqrt{2}}{2} \cdot \frac{\pi P}{V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}}. \tag{7}$$

Core loss densities can be estimated using the Steinmetz equation, $p_c = k f^{\alpha} \hat{B}^{\beta}$, where $\beta \approx 2...2.5$ for typical core materials suitable for MF transformers. In an IFE system, $\hat{B}$ varies with the grid voltage, i. e., $\hat{B}(t) = B_{\max} \sin(2\pi f_{\mathrm{g}} t)$, where $B_{\max}$ denotes the allowable peak flux density. Therefore, the core loss density can be found by averaging over a grid period as

$$p_{\mathrm{c}} = \frac{2}{T_{\mathrm{g}}} \int_0^{T_{\mathrm{g}}/2} k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta} \sin(2\pi f_{\mathrm{g}} t)^{\beta} dt. \tag{8}$$

For $\beta = 2$, this integral can be solved analytically, resulting in $p_{\mathrm{c}}{=}1/2 \cdot k f_{\mathrm{s}}^{\alpha} B_{\max}^{\beta}$, i. e., the core loss density is lower than that of a transformer that would be operated with a constant voltage magnitude and the same $B_{\max}$.

2) aIFE Power Semiconductors: The RMS currents of the power semiconductors in the SRC bridges follow directly from the transformer current, and are given as

$$\tilde{I}_{\mathrm{SRC,MV}} = \frac{\pi P}{2V_{\mathrm{ph}}} \cdot \sqrt{\frac{f_0}{f_{\mathrm{s}}}} \tag{9}$$

and

$$\tilde{I}_{\mathrm{SRC,LV}} = n \cdot \tilde{I}_{\mathrm{SRC,MV}}. \tag{10}$$

If an appropriate magnetizing inductance and interlock time, t_{il}, are selected, ZVS can be guaranteed over a certain range of the grid period as is shown in Fig. 5(a). Note that residual switching losses from partial ZVS in the vicinity of the grid voltage zero cross are typically neglible, if the maximum switched voltage is low. Full-range ZVS, e. g., in order to reduce EMI, would require a large magnetizing current and/or a long interlock time, which both would increase conduction losses, if a constant interlock time is used (Fig. 5(b)). Alternatively, a variable interlock time can be employed to achieve full-range ZVS without the mentioned drawbacks. Please refer to [20] for an in-depth discussion and theoretical analysis of ZVS in IFE converter cells.

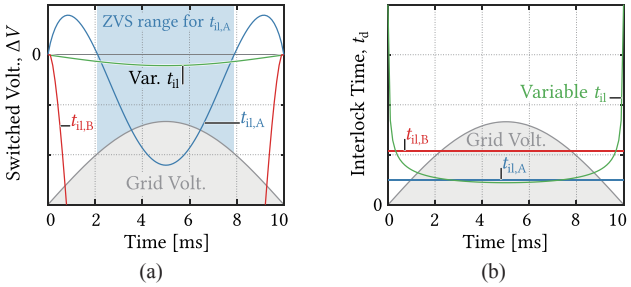

Fig. 5. *a*IFE ZVS (qualitative): (a) shows the switched voltage over half a grid period for two different constant interlock times, $t_{\mathrm{il,A}}$ and $t_{\mathrm{il,B}}$, as well as for a variable interlock time; (b) shows these interlock times over the grid period.

3) Boost Converter Power Semiconductors: The RMS currents (over one grid period) of the boost converter switches can be analytically calculated as

$$\tilde{I}_{\mathrm{Sb1}} = \frac{2\sqrt{3}Pn}{3V_{\mathrm{ph}}} \cdot \sqrt{3 - \frac{4\sqrt{2}V_{\mathrm{ph}}}{\pi n_{\mathrm{cell}} n V_{\mathrm{LV}}}} \tag{11}$$

for the shunt switch and as

$$\tilde{I}_{\mathrm{Sb2}} = \frac{4\sqrt{3}P}{3} \cdot \sqrt{\frac{\sqrt{2}n}{\pi V_{\mathrm{ph}} n_{\mathrm{cell}} V_{\mathrm{LV}}}} \tag{12}$$

for the series switch. Switching losses for hard-switching conditions can be obtained from the devices' datasheets.

4) Boost Inductor: The rms current of the boost inductor (neglecting the switching frequency ripple) is given by

$$\tilde{I}_{\mathrm{B}} = \frac{2Pn}{V_{\mathrm{ph}}} \quad \left(= \sqrt{\tilde{I}_{\mathrm{B,Shunt}}^2 + \tilde{I}_{\mathrm{B,Series}}^2} \right). \tag{13}$$

Its core losses can be estimated from the peak-to-peak current ripple, $\Delta I_{\mathrm{b\,,\,pp}}$, the number of turns, N_{b}, and the core cross section area, A_{Fe}, according to

$$\Delta B_{\mathrm{pp}} = \frac{L_{\mathrm{b}} \Delta I_{\mathrm{b,pp}}}{N_{\mathrm{b}} A_{\mathrm{Fe}}} \tag{14}$$

and

$$p_{\mathrm{c,b}} = k f_{\mathrm{s,b}}^{\alpha} \left(\frac{\Delta B_{\mathrm{pp}}}{2} \right)^{\beta}. \tag{15}$$

For typical current ripples, the resulting core losses are small compared to the winding losses.

B. Key Components of the Realized Prototype

Using the above considerations, a prototype of a converter cell with the topology given in Fig. 3 has been designed and constructed. Fig. 6 shows a photograph of the realized 5 kW prototype, which features an AC input voltage of 760 V (rms) and 1080 V (peak), and a DC output voltage of 400 V. The power density is about 1.5 kW/l (24.6 W/in^3).

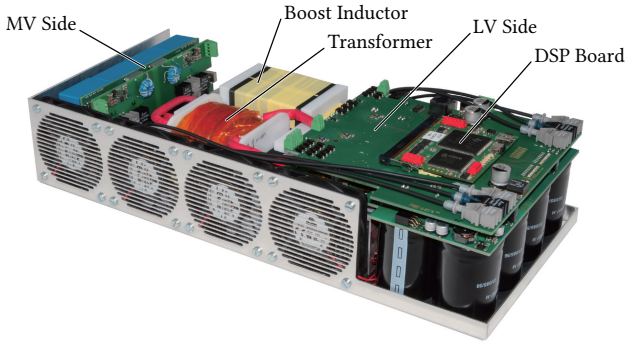

Fig. 6. Photograph of the constructed IFE cell prototype with a rated power of 5 kW The dimensions are 323 mm × 148 mm × 70 mm, corresponding to a power density of 1.5 kW/l (24.6 W/in^3). The measured peak efficiency is 97.5%, and the full efficiency curve is shown in Fig. 11.

The cell prototype employs latest SiC MOSFETS by Wolfspeed [23]: the bidirectional switches on the MV side are realized with 1700 V/45 mΩ (25 °C) devices (C2M0045170D), whereas the LV side switches (for both, active rectification in the *a*IFE and the boost stage) are realized with 900 V/13 mΩ (25 °C) devices (X3M0010090X-ES). The latter are available in a TO-247-4 package, i. e., they feature a Kelvin source that helps improving the switching behavior and reducing switching losses.

The transformer is based on an E80 core (Epcos N87 ferrite) and litz wire windings (22 turns of 900 × 0.1 mm litz wire on the MV side, 13 turns of 1400 × 0.1 mm litz wire on the LV side), with 3 mm of isolation material between the primary and secondary side windings. Note that no detailed isolation coordination such as in [2] is carried out, because the focus lies on evaluation of the IFE topology, not on the transformer design, which is covered by corresponding literature [2], [24]-[27].

In order to constrain the size of the boost inductor, a comparably high switching frequency of 75 kHz is used. The boost inductor can then be realized from three stacked E56 cores (Epcos N87 ferrite), and again using 14 turns of a litz wire winding (900 × 0.1 mm) and a 2.4 mm air gap. Please refer to TABLE II for more details on the main components of the prototype as well as their respective current and/or voltage stresses.

The control software is implemented on a custom control board that features a TMS320F28335 DSP from TI and a LFXP2-5E-T144 FPGA from Lattice. Optical fibers are used to transmit the gate signals from the control on the LV side to the gate drives of the switches on the MV side, and to transmit status signals from those gate drives back to the control board.

TABLE II
MAIN COMPONENTS AND THEIR KEY STRESSES.

MV res. cap., $C_{r1,2}$	2.7 µF, 8.7 A (rms), 565 V (peak)
Series res. cap., C_r	4.6 µF, 26.9 A (rms), 37 V (peak)
LV res. cap., $C_{r,LV}$	3 µF, 13.6 A (rms), 321 V (peak)
MV FETs	C2M0045170D (1700 V/45 mΩ)
MV *a*IFE FET cur.	11 A (rms)
LV FETs	X3M0010090X-ES (900 V/13 mΩ)
LV *a*IFE FET cur.	19 A (rms)
LV Boost low-side cur.	13.8 A (rms)
LV Boost high-side cur.	19 A (rms)
Transf. core.	E80/38/20, N87 ferrite
MV winding	22 turns, 15.5 A (rms), 900 × 0.1 mm litz
LV winding	13 turns, 26.4 A (rms), 1400 × 0.1 mm litz
Stray ind., L_σ	10 µH
Magn. ind., L_M	733 µH (0.2 mm air gap)
Boost. ind., L_b	140 µH (30% peak-peak cur. ripple)
Boost. ind. core	3 × E56/24/19 N87 ferrite
Winding	14 turns, 23 A (rms), 900 × 0.1 mm litz
Air gap	2.4 mm
LV DC cap., C_{dc}	5.45 mF, 13.1 A (rms), 400 V (DC)

C. Measurements

As no MV AC source was available, the converter cell has been tested with power flow from the DC to the AC side, i. e., a 400V DC power supply is connected to the LV DC terminals, and a resistive load is attached to the MV AC side terminals. The system is then operated in open-loop, i. e., by using a $|\sin 2\pi f_g|$-shaped reference for the PWM of the boost converter stage, and by gating the bidirecitional switches on the MV side such as to realize both, active recitification of the

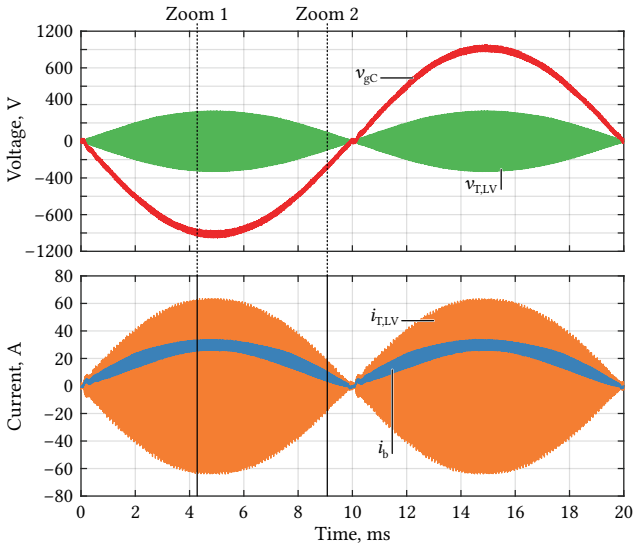

Fig. 7. Measured key waveforms at rated load in DC-AC operating mode, i. e., with power flow from the DC to the AC side. Fig. 8 shows zoomed views covering a few switching periods at the indicated locations.

HF voltage and unfolding of the resulting $|\sin 2\pi f_g|$-shaped waveform into an AC voltage at the MV terminals.

Fig. 7 shows the corresponding key waveforms over one fundamental period (50 Hz) at nominal load. The AC output voltage, v_{gC}, is sinusoidal and in phase with the boost inductor current, i_b, on the LV side, which, as discussed above, corresponds to unity power factor operation. Fig. 8 shows zoomed views of these key waveforms at two different points in time within the grid period. These measurements clearly verify the description of the IFE converter's operating principle described in Section II.

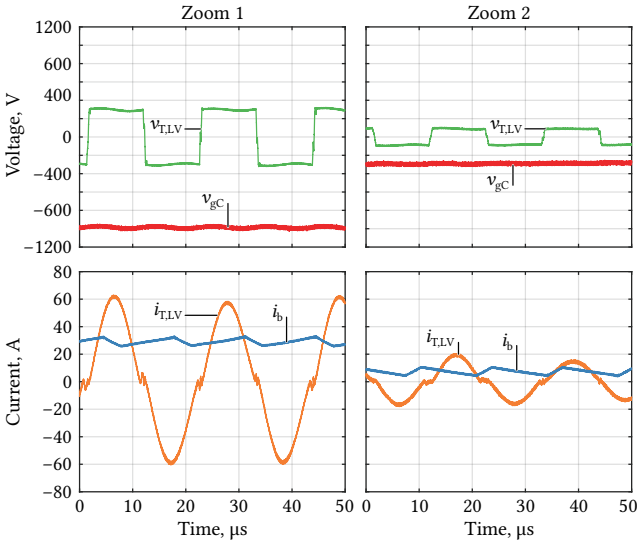

Fig. 8. Measured key waveforms at rated load in DC-AC operating mode at two different instants during the grid period as indicated in Fig. 4.

Fig. 9 shows two transitions of the transformer voltage at two different instants of the grid period, once at 50 V and once at 220 V. In both cases, an interlock time of 700ns is used—this is clearly too short to achieve ZVS in the first case, and clearly too long in the second, which confirms the theoretical considerations from [20] and the qualitative analysis in Fig. 5. Thus, the required interlock time has been measured for different switched voltages, which is an alternative to the simulation-based approach described in [20]. The results are

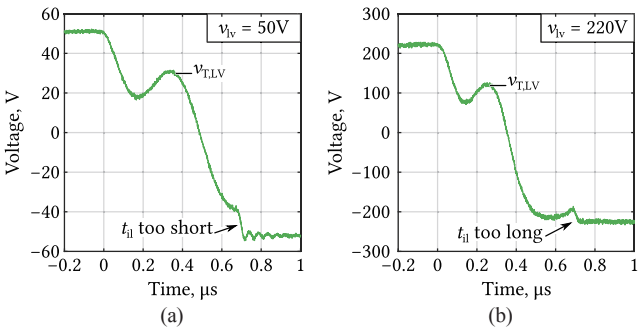

Fig. 9. Detailed view of transitions at different switched voltages of (a) 50 V and (b) 220 V. A constant interlock time of 700ns is employed, which is too short in case (a) but too long in case (b).

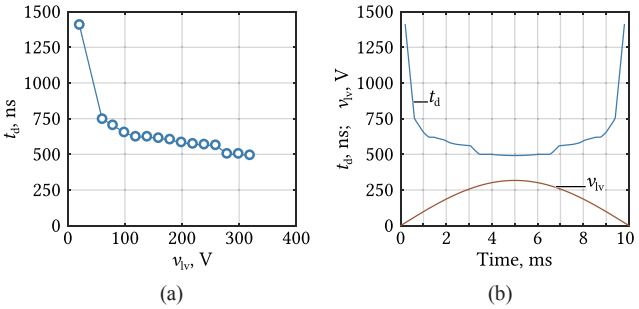

Fig. 10. (a) Required interlock time to ensure ZVS (measured); (b) required interlock time plotted versus time during one half grid period.

shown in Fig. 10(a) and match the qualitative curve shown in Fig. 5(b). The data is then stored in a lookuptable in order to adapt the interlock time of the *a*IFE bridge during the grid period as indicated in Fig. 10(b). The impact on losses is low, however, full-range ZVS may help in improving the EMI signature of the converter by limiting the appearing dv/dt during the transients.

Finally, the efficiency of the converter cell has been measured using a Yokogawa WT3000 power analyzer. The resulting dependeny of the efficiency on the supplied power for DC-AC operation with resistive loads is given in Fig. 11. The full-load efficiency is about 97%, and the peak efficiency observed between 50%...60% of rated load is 97.5%. Note that the efficiency for power flow from the AC to the DC side is expected to be similar, because active rectification is used.

Fig. 12 shows a calculated loss breakdown for nominal

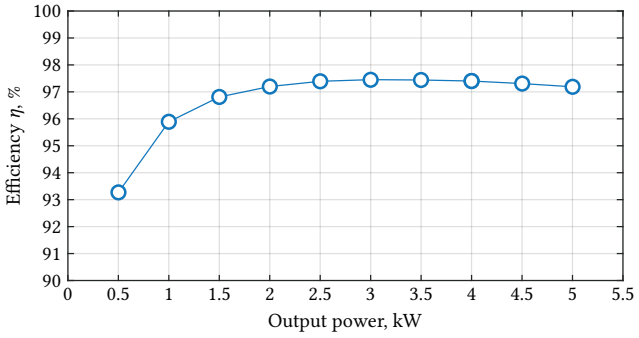

Fig. 11. Measured efficiency in DC-AC operation with V_{dc} = 400 V and a resistor load on the AC side.

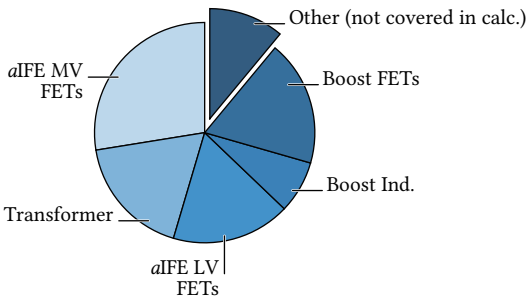

Fig. 12. Loss breakdown (calculated) at nominal power. The separated slice represents the losses not covered by the calculation, i. e., the difference between calculated and measured losses at rated power, corresponding to the calculations underestimating the losses by roughly 11%.

power transfer from the DC to the AC side. The loss share denoted as "Other" corresponds to the deviation between calculated and measured losses, and may be related to losses in the PCB traces, additional switching losses due to additional parasitic capacitance, and other effects not captured by the modeling of the main components. The efficiency could thus possibly be further increased by reducing the switching frequency of the boost converter stage, however, at the cost of lower power density. Also, since the *a*IFE MV MOSFET losses are only conduction losses, paralleling of two devices could contribute to a higher efficiency; the same is true, although to a lesser extent, for the *a*IFE LV MOSFETs.

D. Discussion

In [7], a generic theoretical comparison between equally rated IFE and IBE systems is given. The main findings are summarized in Fig. 13: considering the same specifications, an IFE system requires less cascaded converter cells than an IBE system, because the boost functionality is realized on the LV side in case of the IFE system. As a consequence, the IFE system also uses fewer individual switches and hence gate drive units. The overall transformer volume is similar. However, the relative VA rating of the power semiconductors, i. e.,

$$\mathrm{VA}_{\mathrm{rel}} \stackrel{\mathrm{def}}{=} \frac{1}{P} \cdot \sum i_{\mathrm{x,max}} v_{\mathrm{x,max}}, \tag{16}$$

is higher in case of the IFE, because of the higher peak current in the transformer resulting from the sinusoidal envelope of the transformer voltage. Similarly, considering equal cooling conditions, i. e., equal permissible loss densities, the required total semiconductor chip area is also slightly higher for the IFE system.

The considerations and the experimental results presented in this paper confirm that indeed an IFE-based SST can achieve similar performance as an IBE SST: The measured efficiency of the converter cell is significantly higher than previously reported efficiencies of IFE-based MVAC-LVDC SSTs (83.6% for a 2 kVA demonstrator [16], [17]), and similar to the efficiency published for a similarly rated IBE-based MVAC-LVDC SSTs (25 kW, 96.5% peak efficiency [1]). Considering that the complete IFE SST would contain also additional hardware for protection, measurements, etc., the overall efficiency would likely be slightly lower than the measured efficiency of the converter cell at hand, and hence similar to that of the IBE-based SST system.

The power density of converters connected to MV levels is influenced strongly by clearance and creepage distances required by corresponding standards. The isolation coordination for such systems, e. g., for the HF transformer itself, is a complex task that is similar for all MV-connected power electronic converters, i. e., not specific for IFE-based systems. Therefore, and for the sake of conciseness, these issues have not been considered here in detail. Instead, the interested reader is referred to the corresponding literature [2], [24]-[28]. Thus, the power density of the industrial IBE prototype

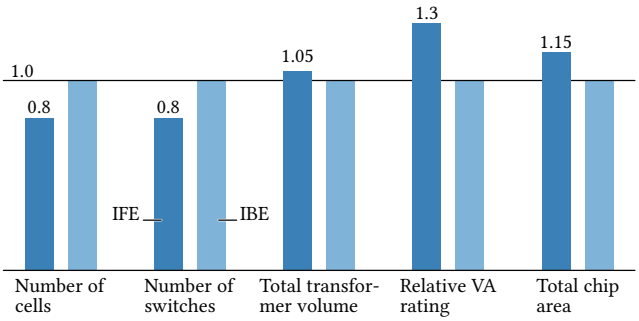

Fig. 13. Generic comparison of the realization offort of the IFE and the IBE concepts according to [7].

discussed above is only about 0.4 kW/l (6.6 W/in^3) (overall) and 0.83 kW/l (13.6 W/in^3) for one of its converter cells [1], i. e., only about half the power density achieved with the presented IFE converter cell. It is thus reasonable to expected that an inudstrialized version of the IFE SST could achieve similar power density as its IBE-based counterparts.

All in all, the IFE converter cell prototype design and the measurements show that it is possible to achieve decent efficiencies and power densities also with MVAC-LVDC SSTs based on the IFE approach.

IV. Conclusion and Outlook

This paper discusses the isolated front end (IFE) concept for realizing an MVAC-LVDC SST. First, the different options to partition the functionality requried for isolated AC-DC conversion with PFC are briefly discussed, before then the operating principle of IFE-based SSTs is explained in detail. In order to clarify the achievable performance of IFE-based SSTs, one converter cell of a 25 kW 6.6 kV AC to 400 V DC MVAC-LVDC IFE SST, denominated as Swiss SST (S^{3}T), is designed, constructed and tested. The 5 kVA converter cell prototype features a power density of 1.5 kW/l (24.6 W/in^3) and a peak efficiency of 97.5% for power flow from the DC to the AC side. This efficiency is significantly higher than previously published results for IFE-based SSTs, and comparable to reported efficiencies of IBE-based SSTs. Therefore, this paper demonstrates the competitiveness of the IFE approach for realizing MVAC-LVDC SST systems. Especially in case low complexity is desirable as, e. g., in applications where the focus is on weight and space reduction, not on controllability, i. e., in applications where the SST essentially acts as a MVAC-LVDC power supply, the IFE concept may be an interesting alternative approach worth considering. Such applications could be, among others, auxiliary power supplies in future trains to supply air conditioning units, lighting, etc. of individual coaches, or rack-level power supplies in future datacenters.

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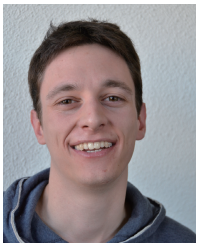

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Improved Control Strategy of Interlinking Converters With Synchronous Generator Characteristic in Islanded Hybrid AC/DC Microgrid

Gongxin Qi, Alian Chen, and Jie Chen

***Abstract*—In this paper, an improved control strategy of interlinking converters for hybrid AC/DC microgrid operated in islanding mode is proposed, which applies synchronous generator model to the converters. This enhanced scheme adopts direct frequency control method to realize active power sharing and improves the transient frequency stability by using synchronverter technology. Unlike existing droop control methods of interlinking converters that mostly just focus on power sharing, this scheme can not only maintain proportional power distributed between DC and AC subgrid, but also regulate the AC subgrid voltage directly to improve its poor frequency stability during AC-side loading transitions in autonomous operation. It's noteworthy that this scheme can also keep the AC-side loads working uninterruptedly during AC subgrid faults events by using voltage-controlled method. Moreover, any additional energy storage or inverters are not required to assist interlinking converters for microgrid frequency regulation. The effectiveness of this modified control method is verified by offline time-domain simulation and real-time experiment in MATLAB/Simulink and OPAL-RT digital platform respectively.**

***Index Terms*—Frequency transient stability, hybrid AC/DC microgrid, interlinking converter, proportional power sharing, sychronverter.**

I. Introduction

NOWADAYS, with the rapid increase of photovoltaic, fuel cells, energy storages and many other DC energy power systems in microgrids as well as modern DC loads such as electric vehicles, and considering the existing century-long AC power systems, hybrid AC/DC microgrids have obtained more and more attention [1]. In a hybrid microgrid, as shown in Fig. 1, AC and DC microgrids are interconnected together via interlinking converters (ILCs), making it possible to exchange power among all distributed generations (DGs). Many types of distributed resources are connected to DC and AC buses by different power converters. Once there are some faults in utility grid, the static switch at point of common coupling (PCC) will be kept open and the hybrid microgrid works in an islanded mode. It is noteworthy that ILCs control method plays an important part in the hybrid microgrids especially without the support of utility grid, coordinating the dual subsystems to regulate AC and DC bus voltages and exchange power proportionally between DC subgrid and AC subgrid [2].

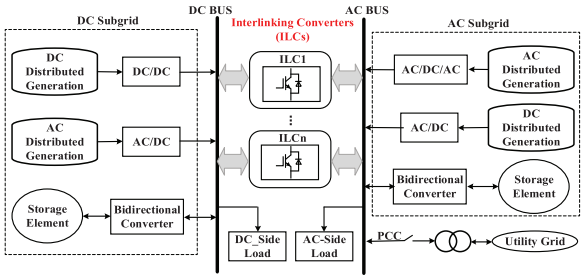

Fig. 1. Structure of hybrid AC/DC microgrid.

All of the ILCs control methods can be classified into communication-based and communication-less strategies. References [3]-[5] present centralized control schemes based on energy management system to manage power flows of a hybrid microgrid and regulate the AC and DC bus voltages on their reference values. However, these methods highly depend on fast and accurate communication system. But any link malfunctions or communication interference would likely lead to instability of the whole system. So communication-based control methods are usually viewed as less reliable and they are also not suitable to be applied to multiple parallel ILCs due to many wire links [6]. Therefore, communication-less control based on the classical droop operating principles is preferred.

Many wireless control methods based on normalized droop control have been proposed in recent literatures. In [7]-[11], it has been suggested to just measure per-unit values of the AC subgrid frequency and DC subgrid voltage to determine the reference power for ILCs and consequently balance supply-demand between two subgrids. Besides, multiple ILCs could be used in parallel to enhance capacity and reliability without wire links. However, these schemes employed in ILCs usually use frequency variation and current-controlled method. Large frequency variation has bad effects on AC-side frequency stability and would lead to poor power quality. Besides, the current-controlled method doesn't offer voltage support for AC bus and even deteriorates AC-side frequency stability while transferring

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exchanged power. Especially during the AC-side loads transients, microgrid frequency could oscillate heavily and even beyond allowable limits.

Motivated by aforementioned problems, this paper proposes a modified method to optimize AC subgrid frequency stability based on normalized droop control method. The direct frequency control scheme is adopted to manage proportional power flows and enhance frequency dynamic response meanwhile. Furthermore, synchronverter technology is applied to ILCs control system to improve poor dynamic frequency stability by mimicking a synchronous generator. Virtual inertia can make ILCs appear as high inertia so as to avoid AC bus high-frequency oscillation during loading transients. It's noteworthy that suitable virtual damp could availably suppress active power and frequency fluctuation and regulate AC-side frequency extremely smoothly.

This paper is organized as follows. Section II overviews droop control methods of DGs within DC and AC subgrids. Section III explains the improved ILCs control scheme including proportional power sharing and application of synchronverter technology. Simulation results are given in Section IV and experimental results are presented in Section V with conclusions in Section VI.

II. Autonomous Control Within Subgrids

A. Droop Control of DGs within AC Subgrid

DGs linking to the AC bus have widely adopt droop control scheme [12]. As shown in Fig. 2, active and reactive power within AC subsystem are relevant to the references of voltage frequency and amplitude, respectively. The distributed sources can automatically share the total active power and reactive power demand in proportion to their rated power and maitain the stable operation of the AC subgrid.The droop equations for obtaining voltage frequency and amplitude of xth DG unit are presented as in

$$f_{\text{ac\_H}} = f_{\text{x}}' + m_{\text{x}} P_{\text{a,x}};\ U_{\text{ac\_H}} = U_{\text{ac,x}}' + n_{\text{x}} Q_{\text{a,x}} \tag{1}$$

where $f_{\text{ac\_H}}$ and $U_{\text{ac\_H}}$ are the maximum allowable voltage frequency and amplitude respectively; m_x and n_x are the droop coefficients.

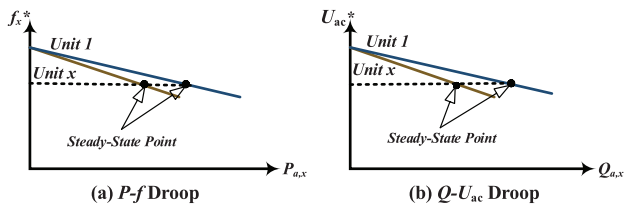


Fig. 2. P-f and Q-U_{ac}droop characteristic in AC subgrid.

Upon reaching steady state, these parallel DG*s* come to be one prevailing frequency autonomously as presented by the single dashed horizontal line. Similarly, we will also get one voltage amplitude ignoring line impedance at the steady working point. Consequently, the AC subsystem will nicely meet such P-f and Q-U_{ac} droop characteristics as follows

$$\begin{cases} f_{\text{ac\_H}} = f_{\text{ac}}' + m_{\text{ac}} P_{\text{ac}} \\ U_{\text{ac\_H}} = U_{\text{ac}}' + n_{\text{ac}} Q_{\text{ac}} \end{cases} \tag{2}$$

$$\begin{cases} m_{\text{ac}} = (f_{\text{ac\_H}} - f_{\text{ac\_L}}) / P_{\text{ac\_max}} \\ n_{\text{ac}} = (U_{\text{ac\_H}} - U_{\text{ac\_L}}) / Q_{\text{ac\_max}} \end{cases} \tag{3}$$

where m_{ac} and n_{ac} are the combined droop coefficients of the AC bus; $f_{\text{ac\_L}}$ and $U_{\text{ac\_L}}$ are the minimum allowable voltage frequency and amplitude respectively; $P_{\text{ac\_max}}$ and $Q_{\text{ac\_max}}$ are the rated active and reactive power capacity of AC subgrid respectively.

B. Droop Control of DGs within DC Subgrid

Comparing to AC subgrid, the DC subgrid is a little easier without considering reactive power, frequency, and phase issues. As shown in Fig. 3, DC bus voltage will fall down linearly with the output active power increasing [13]. Without taking line impedance into consideration, DGs remain the same voltage in the steady-state point. The droop equation of yth DG connected to the DC bus is given by

$$U_{\text{dc\_H}} = U_{\text{dc,y}}' + k_{\text{y}} P_{\text{dc,y}} \tag{4}$$

where $U_{\text{dc\_H}}$ is the maximum output voltage at no load condition, k_{y} is the droop coefficient of the yth DG unit. Similarly, mathematic model of the total DC subsystem can be expressed as follows

$$U_{\text{dc\_H}} = U_{\text{dc}}' + k_{\text{dc}} P_{\text{dc}} \tag{5}$$

$$k_{\text{dc}} = (U_{\text{dc\_H}} - U_{\text{dc\_L}}) / P_{\text{dc\_max}} \tag{6}$$

where k_{dc} is the DC bus droop coefficient and $P_{\text{dc\_max}}$ is the maximum output active power of the DC subgrid.

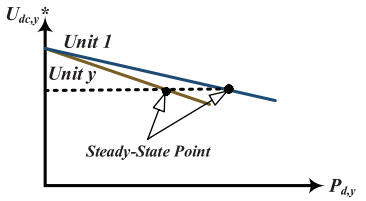


Fig. 3. P-U_{dc} droop characteristic in DC subgrid.

III. Improved ILCs Control Strategy

ILCs are aimed to properly manage the power flows between AC and DC subgrids such that proportional power sharing throughout hybrid microgrids is guaranteed. Besides, due to inertia-less feature of converters, microgrids with high penetration rate of inverter-interfaced DGs usually suffer

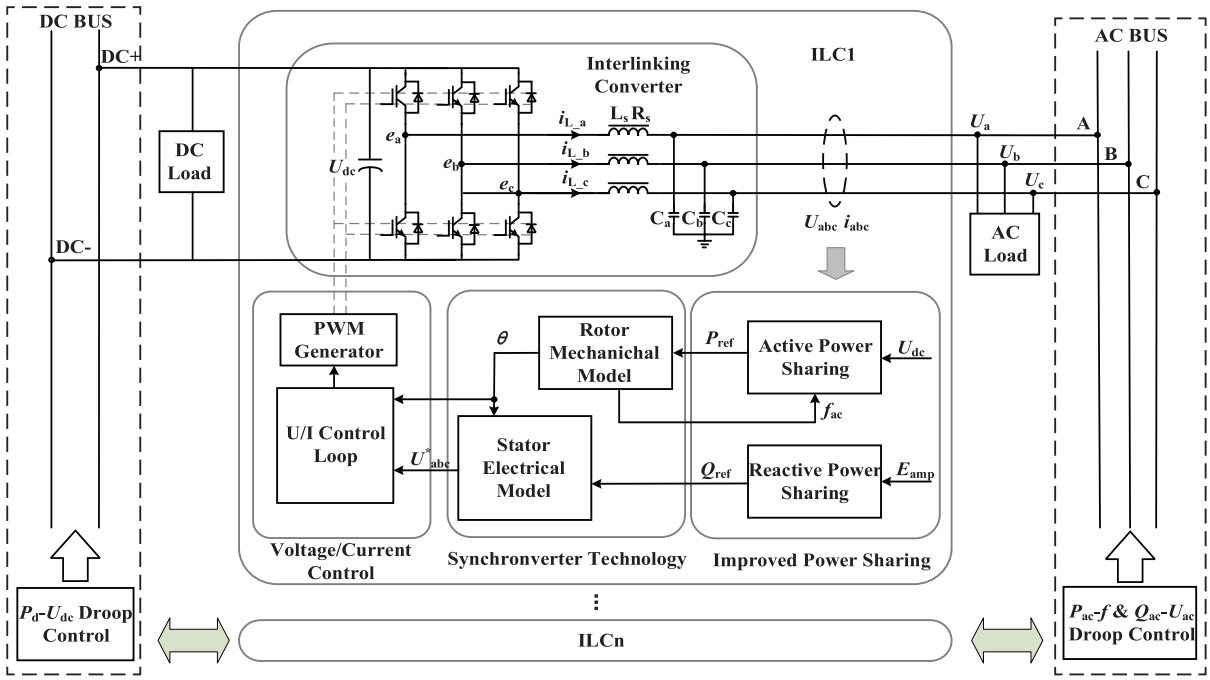


Fig. 4. Control block diagram of hybrid AC/DC microgrids.

from heavy power issues such as poor dynamic frequency stability. And large frequency variation again aggravates this matter. To solve this problem, ILCs should be also responsible for the regulation of AC subgrid frequency stability instead of only depending on the DGs inside of the AC subsystem. What's more, it's also considerable for ILCs to provide uninterruptable power supply for AC-side extreme loads during AC subgrid faults events in an islanded mode.

As a consequence, the improved ILCs control strategy is proposed to exchange proportional power flows, improve the AC-side frequency dynamic stability, and offer voltage support to the AC subsystem during faults events. Based on such control objectives,the ILC is connected to the AC bus via a LC filter so that it can be served as a voltage-controlled source with proper control method and offer voltage support to the AC subgrid shown in Fig. 4. The ILCs control strategy adopts direct frequency control to ensure proportional active power sharing and makes the microgrid appear as high inertia and damp with the application of synchronverter technology. The complex voltage command U^*_{abc} is tracked by a traditional double PI voltage and current control of an inverter. The double control loop is well known, and hence no further clarification here.

A. Proportional Power Sharing Control

Rational power sharing is the main task for ILCs in the island mode, which includes active power and reactive power [2]. AC-side frequency is a global parameter and is the same throughout AC subgrid. On the basis of (2), any increase in power demand in the AC subsystem will follow by a decrease in AC bus frequency. Therefore, the relative amount of frequency variation range is anavailable reflection of the relative output active power of the AC subgrid. Similarly, the relative amount of DC subgrid voltage variation is a reliable indication of the relative active power of DC subsystem. However, AC frequency and DC terminal voltage are two different types of droop variables corresponding to AC-side and DC-side active power. To address this problem, these variations can be brought to a common per unit range by [6]

$$\begin{cases} f_{pu} = \dfrac{f_{ac} - 0.5(f_{ac\_H} + f_{ac\_L})}{0.5(f_{ac\_H} - f_{ac\_L})} \\ U_{dc,pu} = \dfrac{U_{dc} - 0.5(U_{dc\_H} + U_{dc\_L})}{0.5(U_{dc\_H} - U_{dc\_L})} \end{cases} \tag{7}$$

Setting the per-unit frequency and per-unit DC voltage equal in the hybrid microgrid, the total active power demanded by both AC and DC subgrids are shared among all DGs proportional to their rated power. Traditional methods employed in ILCs use the error of the normalized variations (f_{pu} - $U_{dc,pu}$) to calculate the reference active power and usually realized by current-controlled method [6-8]. Such control methods only ensure rating active power distribution but can't offer voltage support to AC bus and even deteriorate the AC subgrid voltage quality to a degree. As a consequence, this scheme adopts direct frequency control method to improve frequency response meanwhile maintaining the function of conventional control scheme. According to (2) (3) (5) (6) and setting AC and DC instantaneous active power to be equal, real-time dynamic reference frequency is obtained as

$$f_{ref} = f_{ac\_H} - \frac{(f_{ac\_H} - f_{ac\_L})P_{dc\_max}}{(U_{dc\_H} - U_{dc\_L})P_{ac\_max}}(U_{dc\_H} - U'_{dc}) \tag{8}$$

As long as controlling instantaneous AC-side frequency f_{ac} and reference frequency f_{ref} to be equal, the output active power of AC and DC subgrids will naturally be proportional to each rated power upon reaching steady state. According to (8) and droop control within subgrids, ILC droop characteristic can be described as Fig. 5, where e_f is the error of reference frequency f_{ref} and feedback value f_{ac}.

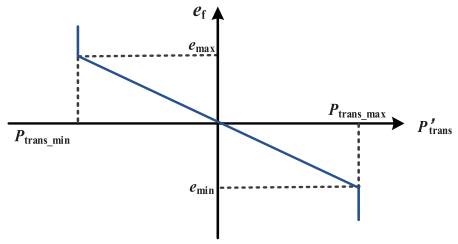


Fig. 5. *P-f* droop characteristic of ILCs.

Specific direct frequency control method is shown in Fig. 6, DC-side voltage is measured and plugged into (8) to get real-time reference frequency corresponding to the DC-side voltage variation. Then f_{ref} is sent to a low-pass filter (LPF) so as to avoid high frequency harmonics resulting in the fluctuation of frequency and active power. K_f is the droop coefficient of ILCs used to calculate exchanged active power according to Fig. 5. Integration element $1/J_{fS}$ is applied to realize non-error adjustment regulation for frequency corresponding to power sharing and increase frequency inertia interrelated to the virtual damp of synchronverter meanwhile. By controlling AC-side frequency to regulate transferred active power, it can not only manage proportional power sharing between the dual subgrids but also improve dynamic frequency stability to a degree with the application of frequency integration element. As for negative transferred power control part shown in Fig. 6, the ILC is regarded as a distributed source connected to the AC bus and adopt a Q-U_{ac} droop control so as to enable the DC subgrid share proportional reactive power with the AC subsystem.

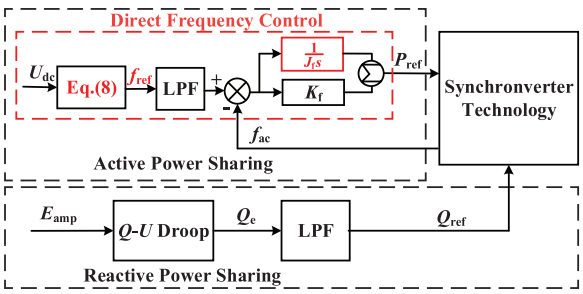


Fig. 6. Power sharing control block.

B. Application of Synchronverter Technology in ILCs

In order to enable ILC appear as high inertia and damp to enhance the dynamic frequency stability during AC-side load transients, this part applies the synchronverter technology to the ILC control scheme. The DC subgrid contains of various DGs with storage elements shown in Fig. 1. And thus there's no extra energy storages demanded for ILCs.

Synchronverter is to apply the mathematic model of synchronous generator into converters to mimic good characteristics of a synchronous generator [14]. The simplified mathematic model of synchronous generator can be summarized by rotor mechanical model and stator electrical model shown respectively as [15]

$$\begin{cases} J\dot{\omega} = T_m - T_e + D_p(\omega_n - \omega) \\ Te = M_f i_f \left\langle i_L, \widetilde{\sin\theta} \right\rangle \end{cases} \tag{9}$$

$$\begin{cases} e = \omega M_f i_f \widetilde{\sin\theta} \\ Q = -\omega M_f i_f \left\langle i_L, \widetilde{\cos\theta} \right\rangle \end{cases} \tag{10}$$

where J and D_p are imaginary inertia and damp of all the parts rotating with the rotor. ω, T_m, T_e, e, and Q are the respectively synchronverter angular frequency, virtual mechanical torque, the electromagnetic torture, the converter potential voltage, and the reactive power of the synchronverter respectively. I_f is the field-excitation current and M_f is the maximum mutual inductance between the stator windings and the field winding. i_L is the output inductor current. Denote

$$\widetilde{\cos\theta} = \begin{bmatrix} \cos\theta \\ \cos(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) \end{bmatrix}, \quad \widetilde{\sin\theta} = \begin{bmatrix} \sin\theta \\ \sin(\theta - 2\pi/3) \\ \sin(\theta + 2\pi/3) \end{bmatrix}. \tag{11}$$

The synchronverter technology control part is shown in Fig. 7. Reference active and inactive power are all calculated by the power sharing partshown in Fig. 6 and they can be regulated separately by synchronverter relying on the mathematic model presented in (9) and (10).

In the mechanical control part, J and D_p represent the associated ILC's virtual inertia and damp coefficients, respectively. According to (9), dynmics of the system frequency ω can be optimized and appear as high inertia by using proper inertia coefficient. It does help to ease the problem of severe frequency oscillations during AC-side load transients. Damp factor D_p can suppress the oscillation of active power [16]. It is a key factor to completely damp frequency fluctuation making it possible to regulate AC-side frequency extremely smoothly, which is not available just relying on virtual inertia. During the process of damping coefficient debugging, there's still once oscillation in frequency and active power while D_p is too small during transient regulation process. Only until virtual damp coefficient is large enough can the AC-side frequency regulate absolutely smoothly without any fluctuation. And in this schemeit can be also used to increase system inertia combined with the inertia element J_f in Fig. 6. In islanded hybrid microgrid, frequency of AC subgrid will change with the load changing because of *P-f* droop charateristic while ω_n is one constant value. Once upon the

steady-state point, the damping power $P_{damp}=\omega D_p(\omega_n-\omega)$ is not equal to zero according to (9). Then the steady-state output active power P_e of interlinking converter is the sum of damping power P_{damp} and P_m. As a consequence, $1/(J_{fs})$ is used to be the intergal part of a PI controller employed for forcing the steady-state difference between AC and DC subsystem output active power to be zero in order to ensure accurate power sharing. On the other hand, during the process of dynamic regulation, $1/(J_{fs})$ can be served as an inertia element with time delay to increase system inertia.What's more, with the application of synchronverter technology, AC-side frequency can be got from system angular speed instead of using a voltage phase-locked loop (PLL) like the traditional ILCs droop control scheme.

In the electrical control part shown in Fig. 7, the regulation of reactive power Q flowing out of ILCs can be realized similarly. The difference between the reference value Q_{ref} and the reactive power Q is tracked and fed into an integrator with a gain 1/K togenerate $M_f i_f$, which will be put into (10) to get the final reference voltage and realize the power control by the voltage/current double closed control with zero steady voltage error meanwhile offering support to the AC bus.

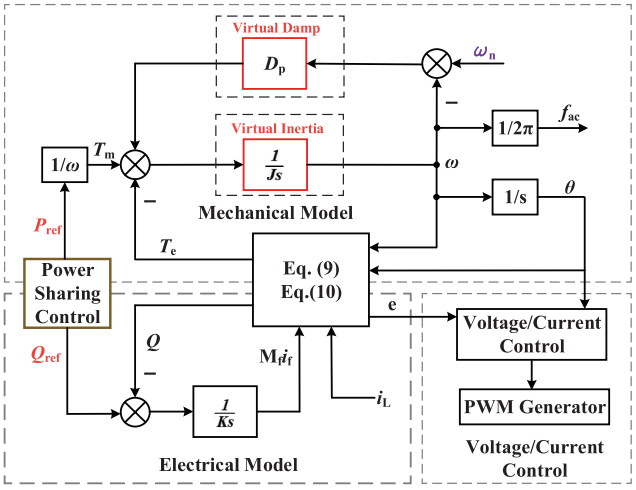


Fig. 7. Application of synchronverter control block.

IV. Simulation Results

In this section, time-domain simulation is used to verify the analytical studies presented in the previous sections. The simulations have been carried out by using Matlab/Simulink. The tested structure of hybrid microgrid comprising a DC subsystem and an AC subsystem is shown in Fig. 8. The ILC adopts traditional six-switch DC/AC converter presented in Fig. 4 and links to the AC bus through an LC filter. Integrated by various DGs, the AC subsystem is modeled by an inverter controlled by P/f and Q/U_{ac} droop control methods described in Fig. 2. Due to the wide distribution of DGs in the actual microgrid, the line impedance between PCC and DGs should be also considered. As for the DC subsystem, it's modeled by one voltage-controlled source with P/U_{dc} droop characteristic.

System parameters of the tested hybrid microgrid are given in Table I. The total rating power of AC subgrid is 10 kW over an allowable frequency variation of 49 Hz<f<51 Hz and an AC voltage range 215 V<U_{ac}<225 V. The corresponding value of the DC subsystem is 10 kW over an available DC voltage range 590 V<U_{dc}<600 V. To verify the feasibility of this proposed control strategy, loads connected to the two subgrids are switched between "light" and "heavy" condition and the test is organized as two transient cases. At the beginning, the hybrid microgrid works in a steady state under light load condition. At 1s, DC-side load switches from light to heavy. At 3s, when the microgrid reachessteady state, AC-side load changes from the light condition to a heavy mode. Waveforms of frequency and power are presented as follows with analysis.

TABLE I
System Parameters

Parameter	Value
DC Subgrid Rated Power	$P_{ac,max}$=10kW
AC Subgrid Rated Power	$P_{dc,max}$=10kW
DC Voltage Range	590V<U_{dc}<600V
AC Voltage Range	215V<U_{ac}<225V
AC Frequency Variation	49Hz<f<51Hz
Circuit Parameter	**Value**
ILC DC-side Capacity	C_{dc}=4700uF
LC Filter	L_f= 3mH C_f=35uF
Line Impedance	L_Z=2mH R_Z=0.2Ω
Contol Parameter	**Value**
Inertia Coefficient	J_f=2e-5 J=0.06
Damp Coefficient	D_p =50
Load Parameter	**Value**
DC-side Load	1.3kW (Light) 6.3kW(Heavy)
AC-side Load1	3.7kW (Light) 8.7kW(Heavy)
AC-side Load2 (Faults)	3.7kW (Light) 6.5kW(Heavy)

A. Improved Frequency Transient Stability

This paper is devoted to the improvement of frequency dynamic stability during AC-side load transients. Fig. 9 describes the waveforms of frequency adopting different ILCs control methods under the same condition. At 1s, DC-side loads switch from the light mode to heavy mode and AC subgrid autonomously outputs more power to share the power supply with frequency decrease. While AC-side loads increase a lot suddenly at 3s, the AC bus frequency controlled by the traditional ILCs control strategy in Ref [6] could oscillateseverely and even over modulated beyond the normal frequency operating range (49 Hz~51 Hz) as shown in Fig. 8(a), which has a terrible frequency transient stability obviously. As for the simulation results of this improved strategy presented in Fig. 9(b), AC-side frequency could regulate smoothly without any oscillation from the current point to the steady-state value no matter what DC-side or AC-side load changes suddenly. Consequently, the simulation results

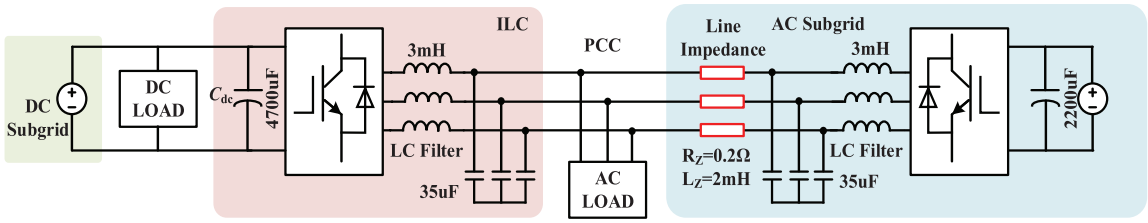
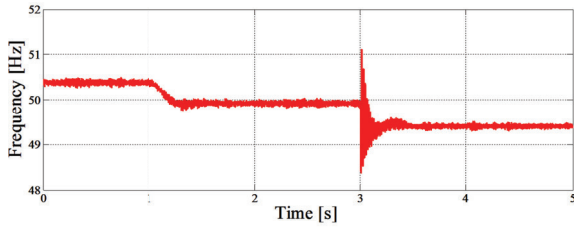
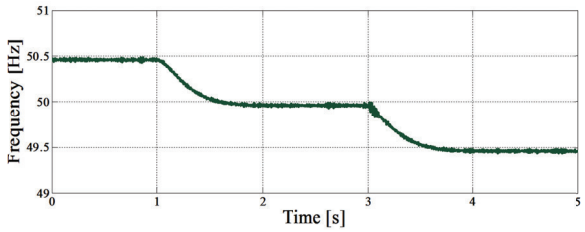


Fig. 8. Structure of the tested hybrid AC/DC microgrid.

in Fig. 9 prove that this improved strategy is effective and has a better performance on the frequency transient stability.



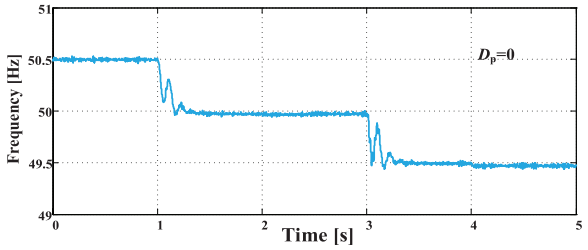
(a) traditionalcontrol scheme



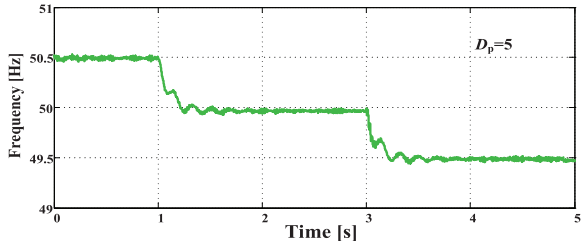
(b) improved control scheme

Fig. 9. Simulation waveforms of AC-side frequency for load transitions.

It's worthwhile to note that virtual damp plays an important role in the dynamic response of frequency corresponding to the AC-side active power. Suitable damp coefficient can completely damp the AC-side frequency and active power-



(a) without damp



(b) small damp

Fig. 10. Simulation waveforms of AC-side frequency with different damp.

fluctuation and makes it possible to regulate smoothly during load transients. Fig. 10 gives the test results of AC-side frequency with different virtual damp coefficients. There are obvious frequency fluctuations during either DC-side or AC-side load transient without the application of virtual damp (D_p=0). After given a small damp coefficient (D_p=5), fluctuations of frequency are suppressed availably although there're still some slight oscillations. While the virtual damp is large enough (D_p=50), the frequency can regulate absolutely smoothly shown in Fig. 9(b).

B. Proportional Power Sharing

Besides dynamic frequency stability, proportional power sharing is the main task of ILCs that must be achieved. To facilitate the results analysis, set DC and AC subgrid rated power to be the same that both are 10 kW as presented in Table I. Therefore, as long as the two subgrids output power can be equal under different load conditions in the steady state, then it will demonstrate that the two subgrids output power are proportional to their rated energy value. From Fig. 11, in the first steady state from 0s to 1s, the DC-subgrid output power is about 2.5 kW equal to the AC-side output value. In the second steady state from 1s to 3s, the output active power of DC subsystem is 5 kW similar to the AC subgrid; lastly in the third steady state, the two subgrids output powers are still approximately equal to each other. As a result, this improved control scheme can achieve the basic control objective about proportional power sharing.

As for the dynamic power response of both AC and DC subsystem, it's because of the DC-side load transient at 1s that DC subgrid outputs large amount of power at once but does few effects on the other side subgrid of ILCs. However, with the application of virtual inertia and virtual damp, the AC subsystem can still output power smoothly at 3s instead of changing largely or even overshooting just like the waveform of DC subsystem at 1s despite of AC-side load transient. What's more, at 1s due to the DC-side load changes the output power of DC subgrid increases a lot at once to meet the power demand. In order to balance the two subsystem power supply, ILCs manage power flows from AC-side to the DC-side. As Fig. 11(c) shows that the value of ILCs output power is negative. Similarly, from 3s to 5s AC-side load is heavier than the DC subgrid, the ILC exchange power from DC subsystem to AC subsystem and value of the transferred power is positive shown in Fig. 11(c).

Dynamic responses of AC current under the two transient events are given in Fig. 11(d) and (e). Either increasing

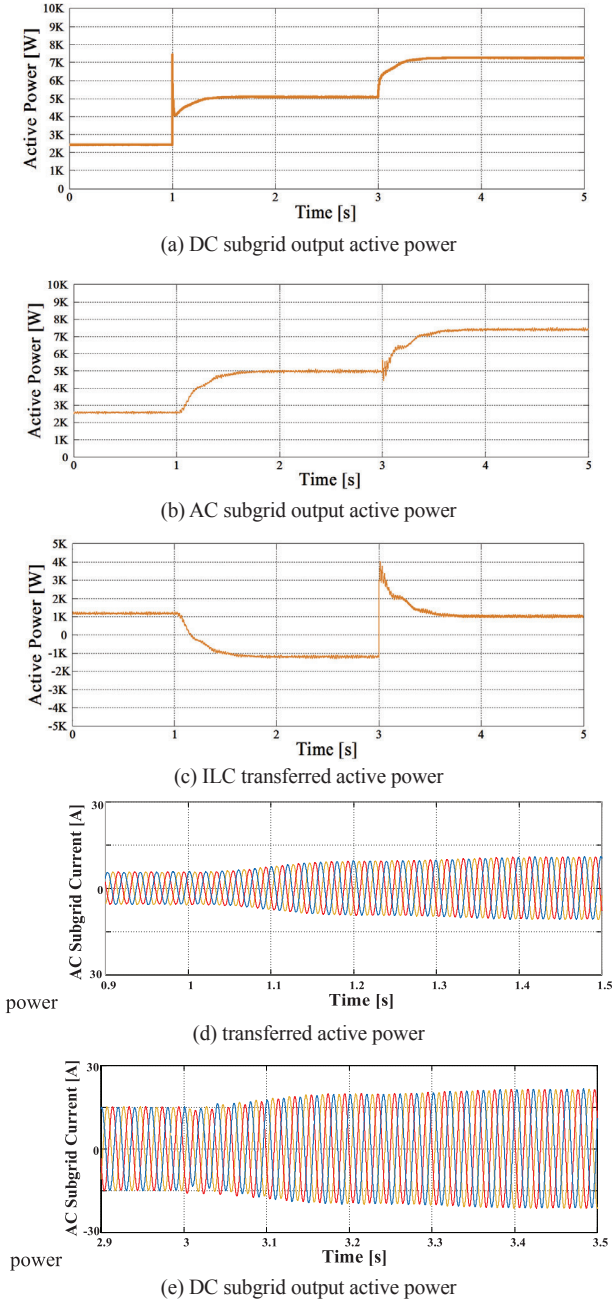


Fig. 11. Simulation waveforms of DC-AC subgrid and ILC output Active power and AC currents for load transitions.

DC-side load or AC-side load, AC subsystem outputs more current to realize proper power sharing and meet all the load demand. During the dynamic regulation progress, the peak currents change smoothly maintaining a stable operation of hybrid microgrid.

C. Higher Reliability Test During AC Subgrid Faults Events in Islanded Mode

In order to further validate the higher reliability of this scheme, in this section the paper simulates a subgrid fault event in islanded mode by breaking down the connection between AC-side loads and AC bus. As Fig. 12 shows, at the beginning the hybrid microgrid works in a steady operation; then at 1s, the AC bus disconnects with the loads all of a sudden, it's obvious that AC-subsystem output power changes to be zero later and ILCs manage power from DC bus to the AC-side loads to provide uninterrupted power supply. As for the frequency, it can change stably and reach steady state during the process of transient regulation. Besides, in

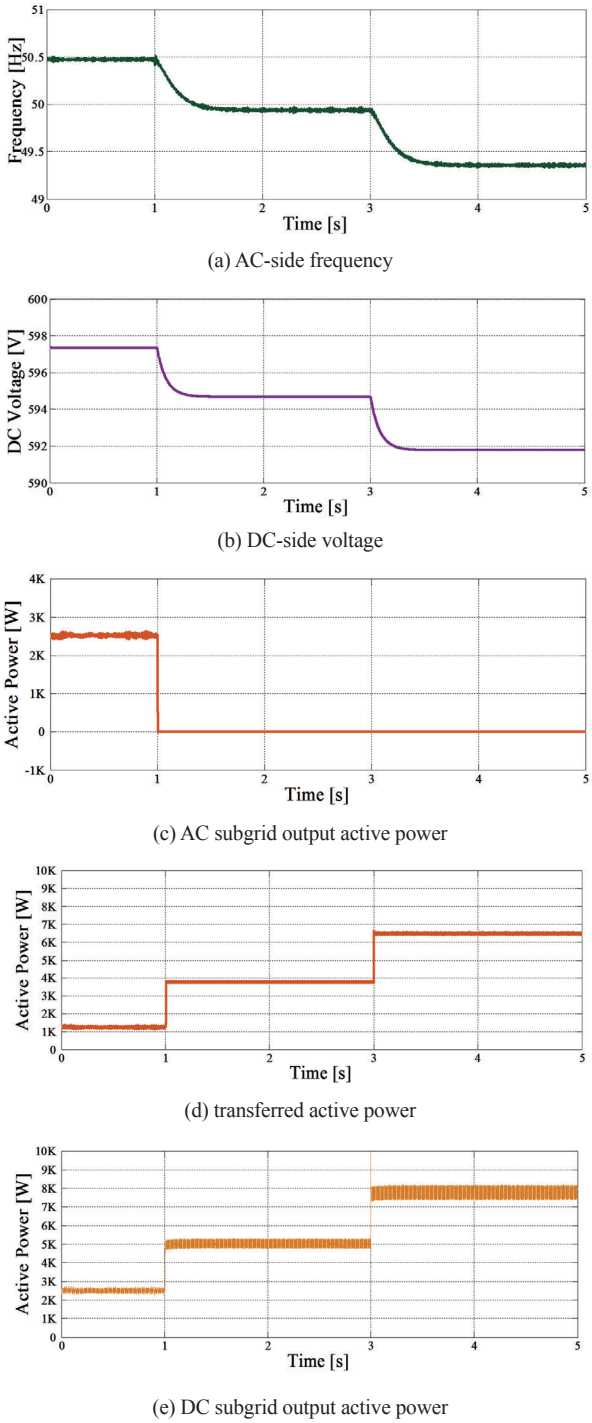


Fig. 12. Simulation waveforms of DC-AC subgrid and ILC output active power for load transitions.

order to further test the dynamic frequency stability, the AC-side loads change from the light to heavy mode at 3s. As we can see from Fig. 12, AC-side subgrid frequency can still regulate smoothly within allowable variation without the assistance of AC bus in the islanded operation. Compared to the general normalized droop control, this enhanced method performs higher reliability and dynamic frequency stability.

V. Experimental Results

The proposed control scheme was further vilified experimentally by the OPAL-RT real-time digital simulator. The proposed control scheme was further vilified experimentally by the OPAL-RT real-time digital simulator. Experimental system parameters and the tested system structure are the same as those used in the simulation and presented in Table I and Fig. 8. A standard DC/AC inverter controlled by P/f and Q/U_{ac} droop control methods and a normal line impedance (R=0.2 Ω, L=2 mH) are formed to be the AC subgrid in the tested hybrid microgrid. DC subgrid is realized by a voltage-controlled DC source with droop characteristic. The maximum output active power of both AC and DC subsystem is set to be 10 kW for the sake of discussion. With respect to the application of synchronverter technology, the ILC adopts a standard DC/AC converter with LC filter to be controlled as a voltage-controlled source with high inertia. This scheme is devoted to deal with the weakness of poor dynamic frequency stability in traditional normalized droop control methods. Therefore, only active power flows and frequency performance are required to be observed in this test. For simplicity, there're two converters controlled with droop characteristics shown in the second section to represent AC and DC subgrid separately. And the other two converters were paralleled and connected to the DC and AC buses to serve as ILCs. The experiments were performed under the condition of 10 kHz switching frequency and carried out as following conditions.

The first test is shown in Fig. 13 with the two subgrids both working in normal state with a DC load of 1.3 kW and an AC load of 3.7 kW. At the beginning, AC-side loads demanded more power than loads of DC subgrid, and thus the ILCs exchange about 1.2 kW power from the DC subsystem to AC subsystem to share the output power proportionally shown in Fig. 13(b). At 2s, DC-side load is increased to be 6.3 kW leading to more supplied active power of DC subsystem than AC subsystem. While reaching to the steady state, the output active powers of AC and DC subgrid both equal to be 5 kW by exchanging -1.3 kW power. At 6s, the AC-side load increases by 5 kW and the exchanged active power of ILCs changed from -1.3 kW to 1.2 kW. In the whole experiment, the output active power of DC Subgrid and AC Subgrid can be always equal on steady state as presented in Fig. 13(b), which proves that this proposed scheme can manage proportional power sharing between the dual subgrids. Fig. 13(a) shows that AC-side frequency appears as high inertia and damp and performs good dynamic regulation ability, which can always change smoothly without any os-

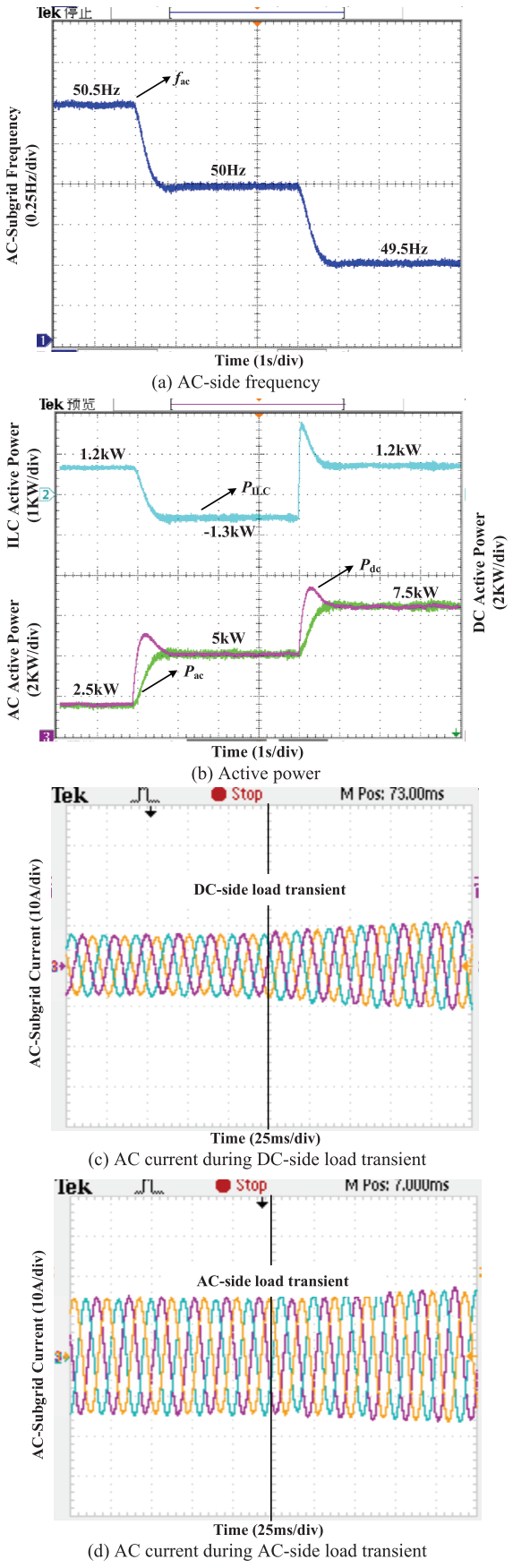
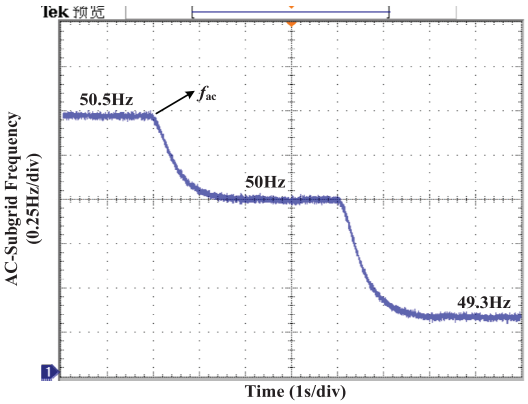


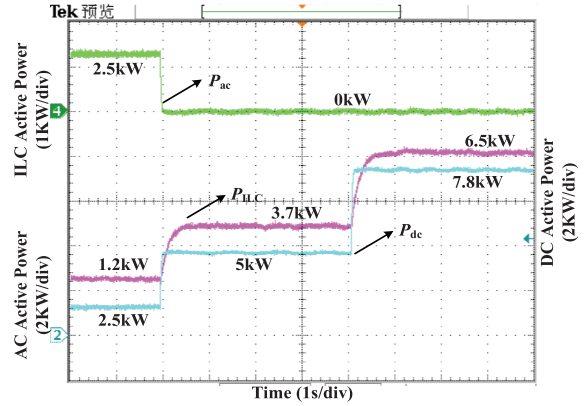
Fig. 13. Waveforms of hybrid microgrid under normal condition.

cillation during loads transients. Besides, dynamic responses of the AC subsystem under the two transient conditions are presented in Fig. 13(c) and (d). The AC current can also regulate smoothly without distortion during the dynamic regulation progress ensuring the safe and feasible operation the AC subgrid.

Experimental results of the other test is shown in Fig. 14 with AC subgrid faults while operating in islanded mode. Similarly, in the first two seconds the hybrid AC/DC microgrid operated steadily in a normal state. At 2s, disconnect the inverter served as AC subgrid from AC-side loads to equal the state of AC subsystem faults events. Increase AC-side loads by 2.8 kW suddenly at 6s to make further verification of dynamic frequency stability. Fig. 14(a) shows that AC-side frequency can always change smoothly without any fluctuation and verifies that this improved method optimize the frequency transient stability to a great extent. Fig. 14(b) shows that DC subgrid and ILCs could still operate steadily and provide uninterrupted power supply for the AC-side extreme loads without AC subsystem. What's more, the whole experiment shown in Fig. 14 also verifies it feasible to offer voltage support for the AC-side loads and increase system faults tolerance.



(a) AC-side frequency



(b) Active power

Fig. 14. Waveforms of hybrid microgrid with AC subgrid faults events.

VI. Conclusion

This paper proposes an improved wireless ILCs control strategy with synchronous generator characteristic for hybrid mcicrogrid. It aims to solve the problem of poor dynamic frequency stability as well as power oscillation during AC-side load transients. Compared to conventional normalized droop control method, this strategy adopts direct frequency control to realize proportional power sharing and apply synchronverter technology to ILCs to increase system inertia of microgrids and damp AC bus frequency oscillations. Besides, exchanging power with voltage-type synchronverter technology could also offer uninterrupted power supply to the extreme AC-side loads during AC subgrid faults events. Finally, experiment results based on OPAL-RTLAB platform verify that this modified method can greatly improve the frequency transient stability and manage proportional power sharing meanwhile.

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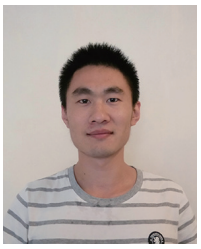

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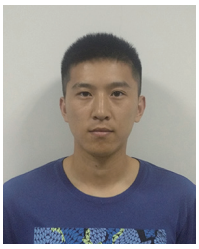

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