Emerging Trends in Silicon Carbide Power Electronics Design

H. Alan Mantooth, Tristan Evans, Chris Farnell, Quang Le, and Robert Murphree

***Abstract*—The emergence of wide bandgap power semiconductor devices has opened the possibilities of improved electrical performance and power density. Advanced research into wide bandgap power electronics also includes advances in integrated circuit design, semiconductor device modeling, 3D electronic packaging, and computer-aided design of wide bandgap based electronics. These emerging trends are described along with some early results indicating the additional improvements possible in power density. Operation at extreme temperatures also becomes more feasible.**

***Index Terms*—Gallium nitride, power integrated circuits, power semiconductor devices, power electronics, silicon carbide, wide bandgap semiconductors.**

I. Introduction

WIDE bandgap power semiconductor device technology has become a key enabler for the miniaturization of power electronic systems. This fact has been described and demonstrated in the literature for the past decade or more for many applications. A search of the literature in IEEE Xplore alone reveals over 40,000 articles on wide bandgap related activities alone! Of these, hundreds would be focused on applications exclaiming the virtues of using SiC MOSFETs, JFETs, diodes, SJTs, and IGBTs. Over a similar timeframe investigators at Purdue, Cornell, NASA Glenn, GE, Arkansas, and KTH Stockholm have demonstrated integrated circuitry in silicon carbide (SiC) [1]-[11]. These circuits have been analog, mixed-signal, or digital and have been realized in a variety of technologies including bipolar, JFET, nMOS and CMOS.

A primary motivation for the desire to utilize SiC integrated circuits as opposed to silicon or silicon-on-insulator is revealed in high power density packaging efforts. Attempting to compactly package gate drivers, protection circuits and maybe even controllers with the power devices yields a desire to have circuitry that accommodates the junction temperatures produced by the SiC power devices. In some packaging architectures, shown later in the paper, orienting the gate driver on top of the power device is the ultimate in lower gate-loop and maybe even power-loop inductances to achieve clean switching waveforms. As such, a perfect coefficient of thermal expansion (CTE) match between the two die relieves the stress on the interconnect used between the power die and the integrated circuit die leading to longer term reliability – a fact that MUST be addressed as part of high power density, heterogeneous integrated design activity.

In order for all-SiC systems to be fully realized, where the term "all" refers to not only the power devices but also the integrated circuitry, several aspects of the design space must be simultaneously considered. These design flow issues will be described in Section II and include optimization, circuit analysis and modeling, as well as board level analysis and modeling. In many higher power systems, it also involves power module design and system assembly design and analysis. All of these issues together constitute a change in design thinking from traditional silicon based power electronics design.

As will be described in Section II, circuit analysis prior to circuit fabrication is an important element in any electronics design process. Circuit analysis relies on accurate models of the components in the circuit in order to produce results that predict the behavior of the circuit under a variety of electrical and environmental conditions. Section III describes the importance of semiconductor device models to the design process.

Section IV describes some of the SiC integrated circuits recently developed for all-SiC power converters and applications. These circuits represent a few of the key functions needed.

II. Design Automation for SiC Systems

Power electronics design is becoming increasingly multi-disciplinary with the advent of wide bandgap (WBG) devices. The ability for silicon carbide and gallium nitride devices to switch so fast has brought more simultaneous issues into play in order to fully realize the potential of these more ideal switches. These devices can operate at higher junction temperatures, which promotes higher reliability if proper thermal management is designed in. These devices can switch faster, so they allow the size of passives to decrease. Also, because of the faster switching, circuits are more prone to parasitics that can cause excessive ringing in voltage and current waveforms and unwanted electromagnetic interference generation. So, it is apparent that these WBG technologies promote miniaturization of power electronics [12].

Due to these trends toward higher power density and miniaturization, power electronics is entering a phase of greater integration. And, this integration is increasingly heterogeneous as defined by efforts to embed passives, integrated low-voltage circuitry, and sensors into the same package, board, or module platform with the power semiconductor devices. This integrative activity and the desire of many to optimize the design

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tradeoffs demands new design automation tools [13]-[15].

A typical model-based engineering design flow for integrative systems is shown in Fig. 1 [16]. The V-diagram essentially begins in the upper left with the system requirements capture into an executable form. From here the process descends into a partitioned set of subsystems that are successively themselves partitioned and individually designed and verified. The V-diagram is then ascended on the right-hand side to ensure that what was designed meets the subsystem(s) and system specifications. This design approach has been applied to thousands of systems ranging from airplanes to cell phones. Power electronic systems are no different. In fact, as their complexity is increasing, appropriate tools for the various analysis, verification and validation steps required in the V-diagram must evolve or be created.

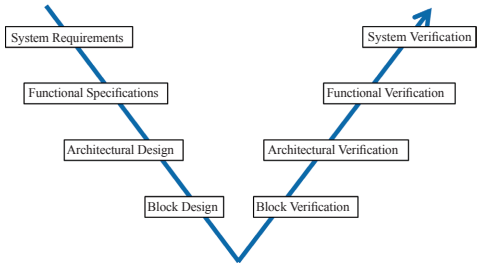

Fig. 1. The V-diagram design flow that represents a top-down specification and partitioning of a system and a bottom-up verification of the proposed designs. This approach allows for specification negotiation and helps to ensure first-pass success.

In the design flow of Fig. 1, as applied to traditional silicon power electronics in a systems such as more electric aircraft, electric cars, electric ships or hybrid heavy equipment, the typical toolset in today's terms would involve Matlab/Simulink® for some higher-level system analysis, controls development, and even some more idealized circuit analysis (often coupled with the control algorithms). It would involve a SPICE-like simulation tool such as LTSpice™, PLECS®, or Saber® for circuit analysis. Board level layout and analysis would be performed by any number of tools, but most would not typically possess proper signal integrity analysis capabilities Further, if the design called for power modules, then these are taken off the shelf with, at best, some equivalent model of the parasitics associated with the module.

With silicon carbide devices, higher switching frequencies, and higher power densities, this toolset is simply not rich enough. Thermal considerations are a first order concern. Electrical parasitics present in both the power modules and on the printed circuit boards must be accounted for or the circuitry simply may not work. In fact, WBG module design often needs to be tailored to the application to maximize performance and reliability. In the absence of advanced tools, this will lead to a degree of customization that results in expensive design and slow the adoption of the technology.

A. Circuit Analysis and Modeling

Circuit analysis tools have incrementally evolved over the past 45 years since SPICE was introduced by UC Berkeley in the 1970s. Clearly, engineers have for decades made due with macromodels and inferior device models for power electronics. The introduction of Saber in the late 1980s began to change this and open up the possibility of having analysis algorithms and models more suited to power electronics [17]. More will be discussed about semiconductor device models in Section III. Some degree of algorithm generalization in terms of integration order and type more ideally suited to periodic sinusoidal systems was introduced in Saber.

Research into switching circuit modeling techniques was also developed through the 1990s as well [18]-[20]. Other research into switching systems simulation was investigated, but found most of its applications in the digital domain [21]. State-space formulations have been advocated here and there through time, but none seem to find their way to mainstream tools. More recently PLECS has taken hold for power electronics as a commonly used tool. All of these approaches remain viable for WBG design, but perhaps it is time for a new formulation. One that is more dedicated to the nature of switching converters, and is more amenable to the design optimizations that the community seeks to achieve.

A comprehensive description of circuit analysis is a standalone topic for a manuscript or book. The main point to make in the context of this paper is that while the field of circuit analysis has matured, there is room for additional tools that may help to advance the multi-dimensional design tradeoff space that power electronics designers seek to command. A tool that runs fast, gives fairly accurate results, and can account for electrical, thermal, and electromagnetic issues.

B. Board Level Design and Analysis

One of the major benefits of using SiC devices is the remarkably low switching losses associated with these devices. This is in part due to their significantly faster transition times which minimizes the time in which the device is in the triode region of operation and reduces switching losses. Due to these fast switching characteristics and associated high *dv/dt* of SiC devices, power electronics designers are now required to factor board parasitics into their design process in a way similar to that of RF and high-speed digital circuit designers. In the past, power electronics designers were accustomed to working with frequencies in the 4 kHz to 20 kHz range with relatively low *dv/dt* (say 5 kV/μs depending on the device). These relatively slow transients allowed many of the board parasitics to be considered negligible by designers. With the emergence of SiC and other WBG devices, it is now possible, and routinely beneficial, to increase the fundamental switching frequencies from the single kHz range to the 100s of kHz range, and associated *dv/dt* transients in the 10-100s of kV/μs range, which allows for capacitors and inductors to be much more effective filters, at the frequency of interest, while also significantly reducing their size and weight. By this same line of reasoning, the once negligible board and trace parasitics can have an overwhelming negative effect on circuitry, and must be analyzed to mitigate adverse effects such as ringing, crosstalk, and conducted or radiated

electromagnetic interference (EMI).

In order to appropriately analyze the effects of board parasitics on the circuits associated with power electronics applications, a new iterative PCB design flow was developed and implemented. Fig. 2 shows the iterative design process currently used in the University of Arkansas (UA) power electronics groups.

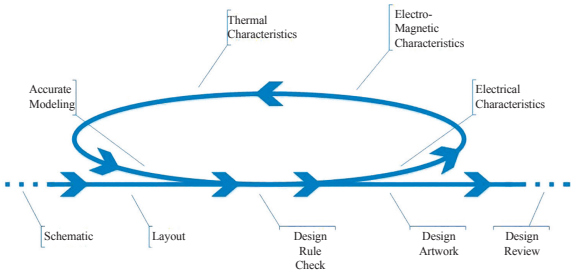

Fig. 2. Progression of general design flow illustrating iterative modeling process.

As a first step the circuit schematic is created and simulated using OrCAD™ PSpice, LTSpice, or PLECS tools to verify ideal operation. Once basic functionality of the circuit schematic is achieved the printed circuit board (PCB) layout is accomplished using Cadence Allegro™. At this point in the process it is common for power electronics engineers using silicon devices to verify certain "best practices" have been implemented during a design review and have the PCBs be sent out for fabrication. In our design flow we instead continue our analysis by exporting the generated board files to ANSYS SIWave™ and perform a parasitic extraction. Fig. 3 shows an impedance scan of a non-ideal PCB layout using SIWave.

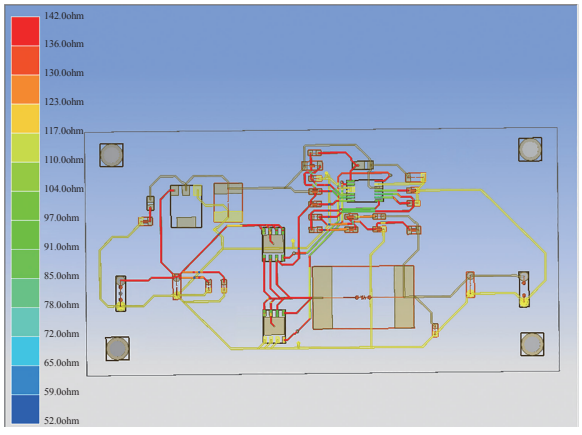

Fig. 3. Impedance scan of a non-ideal PCB layout.

Once the parasitic analysis has been completed using SIWave™ it is then exported to a PSpice circuit library which can then be incorporated into either the original OrCAD simulation or, for more advanced control algorithm evaluation, it may be imported into an OrCAD/Matlab-Simulink co-simulation environment that allows for a coupled controls-circuit simulation of the engineer's design.

With the circuit now available in the ANSYS tool suite, more advanced analysis may also be performed. The high *dv/dt* and *di/dt* switching characteristics of SiC and other WBG devices contribute significantly to radiated EMI that can adversely affect a product's compliance with FCC standards. It has also been observed that this radiated EMI can cause significant corruption of analog-to-digital converters (ADCs), gate drivers, and even controllers such as digital signal processors (DSPs) that have, in turn, caused catastrophic device failures (Fig. 4). By accurately modeling the circuit's conductive traces, along with high fidelity device modeling, an accurate representation of any transmission paths acting as antennas may be identified and subsequently mitigated. Fig. 5 shows the near-field simulation results for the example non-ideal PCB shown above.

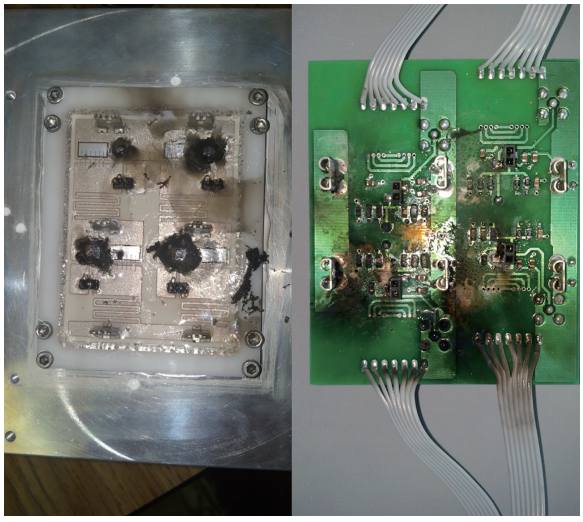

Fig. 4. Destroyed SiC power module (left) and gate driver board (right) due to EMI coupling back into the gate drivers and falsely triggering a power device leading to a shoot-through condition.

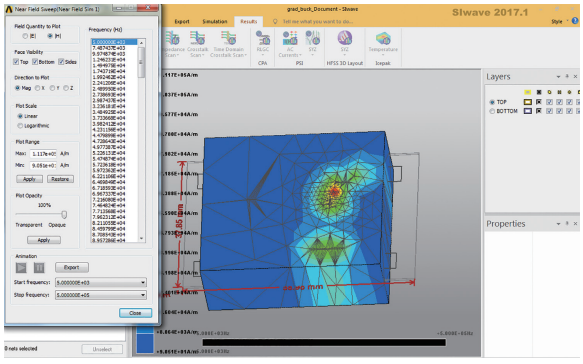

Fig. 5. Near field simulation results and frequency window as produced by SIWave.

Once all analyses have been completed for this base iteration, subsequent improvements and iterations are performed until all design specifications are met and the designer has a high confidence interval of success. This iterative process is analogous to the layout, extraction, analysis, and verification approach used in integrated circuit design prior to submission for fabrication.

C. Power Module Design

Reiterating, as the state of WBG devices advances, so too must the design and manufacture of power electronic modules in order to achieve greater power density. The higher operating temperature afforded by next-generation power semiconductors can reduce the cooling requirements, thereby reducing the overall size and weight of a system. Likewise, higher switching frequencies offered by these devices directly correlates to a reduction in both the size and weight of system-level passive components [12], [22]. Furthermore, integration of some of these passive components inside the module can have a profound impact on power density. For example, incorporation of decoupling capacitors allows for low impedance paths for parasitic current oscillation, mitigating some of the drawbacks of high frequency operation [23]. However, there are several limitations of conventional packaging techniques that are hindering the adoption of WBG devices. This includes not only the physical limitations of the materials chosen for packaging, but also geometrical considerations that a designer must carefully consider.

Among some of the most profound issues a power module designer faces are those related to parasitic inductance. These stray inductances in both the commutation and gate-source loops of power modules can cause several problems. The high operating frequency of WBG devices along with their high slew rates can lead to scenarios where a high *di/dt* leads to large voltage overshoots during switching transients. This overshoot reduces the safe operating area of the module and is a contributor to EMI issues [22], [24]. Additionally, gate-loop inductance limits the gate-source voltage rise and fall times which, in turn, increases transient duration and switching losses [25]. These can sometimes even end in catastrophic failure of the module as seen in Fig. 4.

This high *di/dt* and *dv/dt* associated with the fast switching of WBG devices is a major contributor to conducted and radiated EMI. Any methods employed to reduce stray parasitics in the module will have a direct impact on this. Research in this area by incorporating 3D packaging techniques has shown reduction in EMI as well as the benefits associated with a 3D structure. These include higher power density and the possibility for double-sided cooling [22], [26], [27]. Fig. 6 shows an example of a next-generation 3D, wire bondless module.

While the attractive thermal properties of WBG devices offer the possibility of higher device reliability and thermal capability, this does not guarantee the reliability of the system around these devices. Therefore, high reliability at high operating temperature is a crucial consideration. High temperature relates directly to system reliability in the form of failure mechanisms such as die attachment fatigue or bondwire cracking due to power and thermal cycling under harsh operating conditions [28], [29]. Delamination of direct-bonded copper (DBC) during extreme temperature cycling is another well-known failure mechanism that can be mitigated using the step-edge approach for the copper trace to reduce the thermal stress [30]. Undoubtedly, mitigation of these failure mechanisms will improve the reliability of the overall system. Therefore, detailed analysis is essential in the design phase.

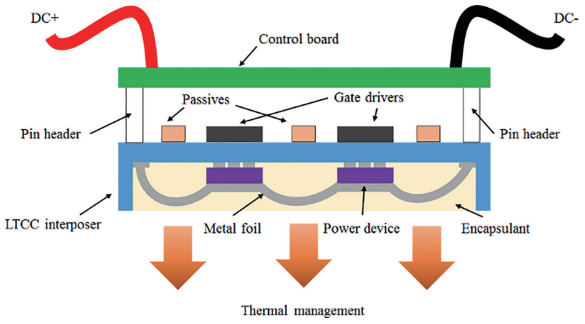

Fig. 6. A 3D power device and gate driver arrangement that significantly reduces generated EMI.

Due to the multidisciplinary nature of power module design, the abovementioned design objectives must be analyzed simultaneously in the design process. Presently, state-of-the-art methods employing high fidelity numerical simulations in an iterative loop are used to simultaneously analyze and synthesize reliable power module designs [31], [32]. While such techniques ensure high accuracy, they are usually computationally expensive, increasing evaluation time and reducing design flexibility. Alternatively, early work in [33] has employed thermal simulations along with lifetime analysis in a response surface based multi-objective optimization routine. This has reduced the number of simulations needed in search of an optimized design. Furthermore, the work in [34] has used strategies borrowed from VLSI work to develop an efficient automated design algorithm. An approach from [35] has shown fast and accurate design by employing reduced order modeling in an optimization loop. Most recently, the work in [36] has allowed more flexible parametric design using thermal resistance networks and closed form equations for both thermal and mechanical analysis. Overall, the abovementioned efforts for CAD tools, models, and algorithms have shown a promising future for a mature design automation flow for power electronic modules – even those that would be heterogeneously integrated with drivers, protection circuits, sensors, and passives where appropriate.

D. System Assembly Design and Analysis

One of the existing gaps in design automation for power electronics is cabinet-level design. Once the boards, modules, and subsystems are designed, then the task of design and layout of the cabinet is required. This includes electrical and thermal considerations as well as relevant standards pertaining to the application space such as industrial drives, electric grid, and automotive. Best practices and design tools have been identified as a need by engineers in the switchgear industry in particular.

III. Semiconductor Device Modeling

One of the emerging trends in SiC power electronics is the development of low-voltage SiC circuitry to be packaged with the SiC power die. One of the keys to being able to realize

accurate simulations of SiC circuits is accurate semiconductor device models. This is true for the power electronic circuit analysis [37], [38] as well as the low-voltage circuitry.

Designing integrated circuits depends heavily on the transistor models. Much effort is spent creating models that reflect all of the key characteristics of the transistors used in IC design. The models are typically charge-conserving so that all charges and resulting nonlinear capacitances are accurately modeled over bias and temperature. The models are typically non-quasi-static and capture the effects of bandgap voltage, mobility, and a host of observed physical phenomena [39]. The models are geometry scalable and temperature scalable within a certain regime. And, statistical and variability behavior is modeled so that Monte Carlo analysis and process corner evaluations can be performed in order to center and tolerance the designs. This level of precision engineering is necessary to create the applications we enjoy today in communications, consumer electronics, and computing. The power electronics industry does not enjoy this level of sophistication in its design procedures and levels of automation as outlined in the previous section. And, until WBG power electronics came along, one could argue it was not necessary for most applications. That situation is changing however.

Several generations of silicon transistor models have been created by a number of groups around the world as process technology marched from barely submicron to nanometer scales. Some of the most oft-used of these models are the Berkeley Short-channel IGFET Models (BSIM).

In the IC design world, the industry came together to standardize on compact models as these transistor models are known. After some investigation, the UA device modeling team chose the BSIM4 standard model to make modifications to in order to create a low-voltage SiC MOSFET model for both *n* and *p* type devices [40]. This new model known as BSIM4SIC has all of the features of BSIM4, but with appropriate modifications for SiC. The enhancements which are related to the SiC MOSFET are implemented in the Verilog-A version of the BSIM470. Those enhancements include:

- Non-silicon substrate and non-SiO_2 gate dielectric model using the model flag MTRLMOD. Assigning 1 to the parameter activates the new model,
- A new mobility model that includes the effects of Coulomb scattering resulting from the presence of interface trapped charge. The model can be selected by assigning 3 to the model parameter MOBMOD,
- Trap assisted leakage current modeling of the junction diodes,
- A new definition of effective gate-to-source voltage for the C-V model,
- Effective oxide thickness model for high-κ gate dielectric, electric and physical oxide thickness model to take into account the effects of process variation,
- A charge centroid model for quantum mechanical tunneling of inversion carriers into the oxide,
- A new temperature dependent bandgap model,
- Enhancement of the threshold voltage shift model due to pocket implant,

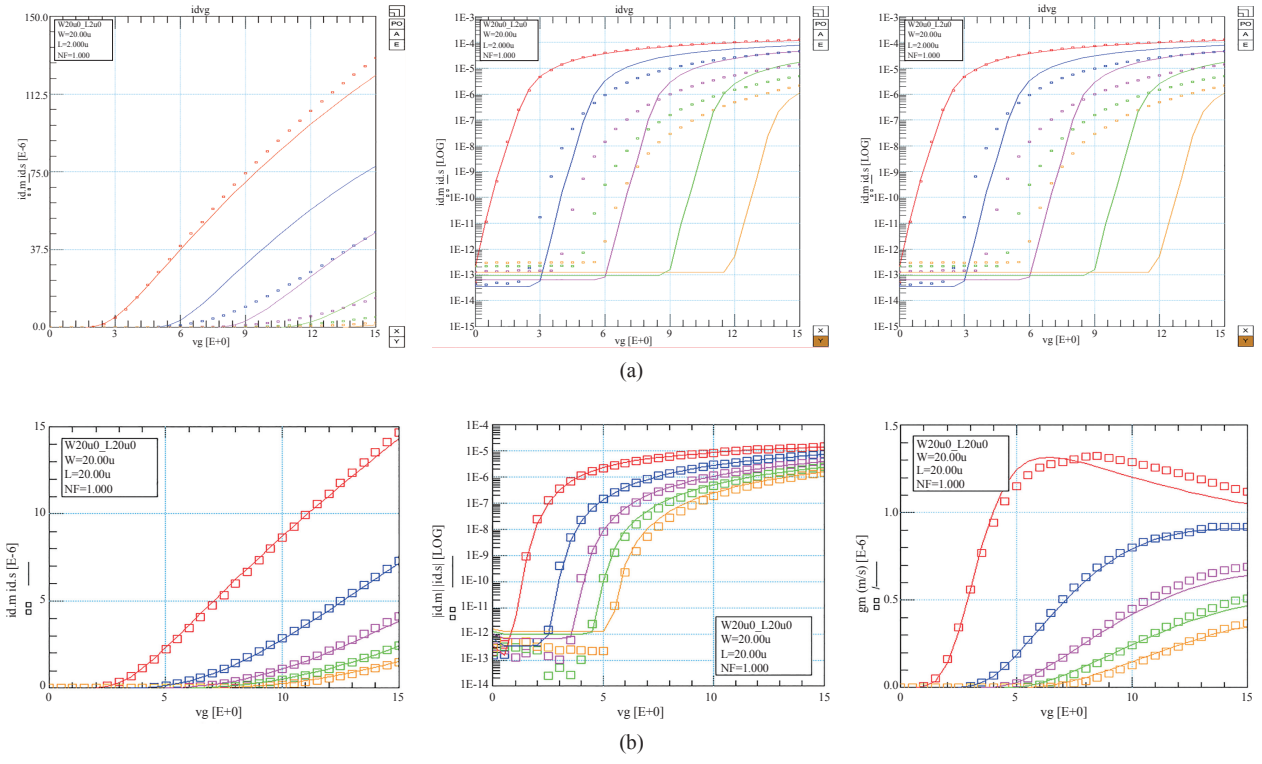

Fig. 7. The best fit curves for BSIM4 against nFET measured data illustrating the body effect (top curves left to right): drain current vs. gate voltage for various back gate voltages at low v_{ds}; drain current vs. gate voltage at high v_{ds}; transconductance (g_m) vs. gate voltage. The same curves for BSIM4SIC illustrating how well the new model can be fit to the measured data because it possesses the correct physics.

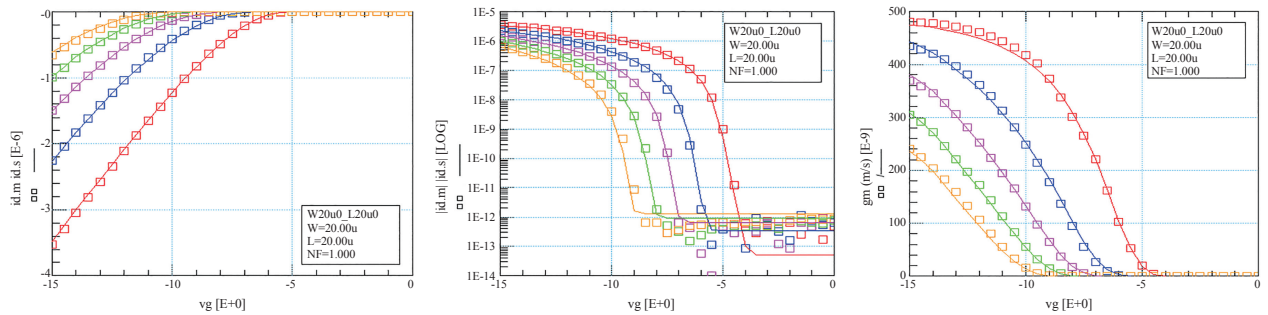

Fig. 8. The best fit curves for BSIM4SIC against pFET measured data illustrating the body effect (top curves left to right): drain current vs. gate voltage for various back gate voltages at low v_{ds}; drain current vs. gate voltage at high v_{ds}; transconductance (g_m) vs. gate voltage.

- A new body effect model,
- A new soft saturation (transition from triode to saturation) model,
- A new channel length and temperature dependent zero bias mobility model, and
- A new temperature scaling model.

Many of these effects including flat band voltage shift, mobility reduction, non-monotonic temperature behavior, soft velocity saturation, and the non-silicon-like body effect can be traced to interface trapped charge in SiC devices.

The results given in [40] show exhaustively how the new model compares to measured data and previous model versions. One example for illustration is the body effect modeling. Fig. 7 shows the best fit for the traditional BSIM4 model to the measured data of SiC devices and the fit for BSIM4SIC in part b. These results are for an nFET device, but similar results were obtained for a pFET (Fig. 8). These sample curves provide insight into the importance of the transistor models for IC design activity and are another example of a design automation component required to effectively pursue all-SiC power converters.

IV. SiC Integrated Circuit Design

The maturity of traditional silicon power process technologies has led to the nearly complete realization of silicon's potential. Fundamental limitations of silicon prevent it from keeping pace with the power electronics industry's growing demand for increasing power density and concomitant higher operating temperatures. As a result, there has been a notable market shift towards SiC and GaN power devices. These wide bandgap materials are advantageous in power electronics applications due to offering higher critical electric fields and thermal conductivity compared to silicon.

While SiC power devices are commercially available, the corresponding control and protection circuitry is currently silicon based. This introduces a limiting factor for the efficient operation of power modules, particularly at high temperatures since silicon and silicon-on-insulator (SOI) based devices are limited to approximately 125 °C and 250 °C, respectively [41], [42]. To operate in high temperature environments without a significant degradation in product lifetime, these circuits require dedicated cooling solutions that increase costs and add parasitic elements.

To realize the potential of wide bandgap power devices, packaging techniques and integrated circuitry must be developed with similar operational capabilities. With demonstrated operation at temperatures exceeding 300 °C, SiC CMOS ICs represent a viable approach to meeting these requirements [6]-[9]. Flip-chip packaging techniques allow for the realization of a 3D wire bondless power module in which the SiC CMOS gate driver, power management, and protection ICs connect to a power device using solder balls and an interposer. This reduces parasitic elements, yielding the potential for higher switching frequencies along with improved efficiency and reliability.

A. SiC Gate Driver

The SiC CMOS gate driver shown in Fig. 9 and presented in [6] has achieved operation above 400 °C with sinking and sourcing capabilities of 8 A and 4 A, respectively. As shown in Fig. 10, the design enables an adjustable drive strength by implementing multiple output stage splices that can allow for higher efficiencies when driving smaller loads. A fault detection feature was also incorporated due to yield issues experienced in previous SiC IC fabrication runs.

B. SiC Power Management and Protection Circuitry

The development of a SiC gate driver with features comparable to a commercially available silicon based counterpart will

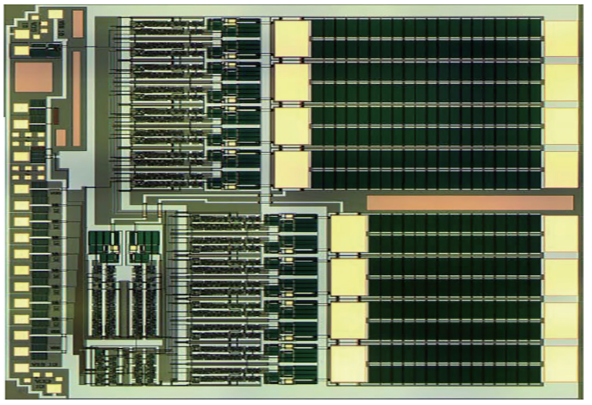

Fig. 9. A die micrograph of the SiC CMOS gate driver fabricated in the HiTSiC® process.

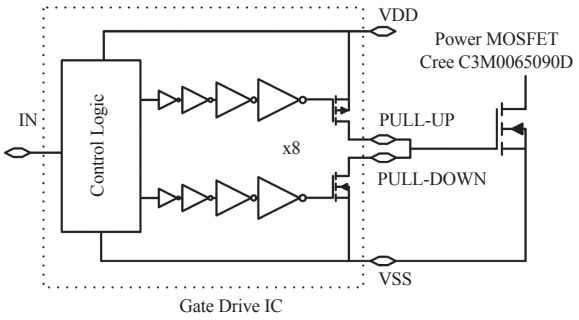

Fig. 10. The schematic of the SiC CMOS gate driver fabricated in the HiTSiC® process.

require an integrated voltage regulator and protection circuitry. The SiC CMOS linear regulator shown in Fig. 11 was designed and fabricated in the same process as the gate driver and is functional at over 400 °C [9]. The regulator provides an output voltage of 15 V from an input voltage of 20 V to 30 V and achieves a continuous output current of 100 mA. An all-NMOS SiC UVLO design has also been presented in [43] and provides a template for the necessary protection circuitry.

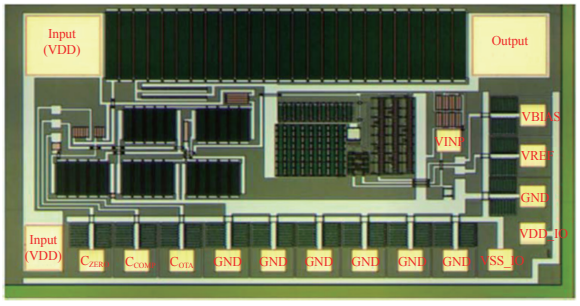

Fig. 11. A die micrograph of the SiC CMOS linear regulator fabricated in the HiTSiC® process.

C. Extending the State of the Art SiC IC Technology

A foundation of SiC CMOS designs has been established with a multitude of mixed-signal circuitry including op-amps, bandgap references, and data converters [8], [44]. More complex designs will be formed by building upon the experience gained in previous design and testing phases. In the case of op amps, for example, a shift towards a higher gain architecture such as the recycling folded cascode [45] will improve the load regulation of the linear regulator. This enhances the precision of the regulator output voltage for a given range of load currents, which can be critical in power electronics applications.

An offset cancellation scheme is another key to the progression of SiC ICs. By implementing this in conjunction with the op amp and bandgap reference in a linear regulator, a temperature stable output voltage can be achieved. The culmination of these efforts creates a path to a fully integrated, intelligent gate driver that provides functionality similar to commercially available silicon based parts while breaking the barriers to even greater power density.

V. Conclusion

Economy and performance are benefits that come with high power density power electronics, just as in the case of integrated circuit electronics. High density power electronics require the heterogeneous integration of disparate technologies including power semiconductor devices, driver, protection and control circuitry, passives and voltage isolation techniques. One of the keys to advancing power electronic integration has been the commercial reality of wide bandgap power semiconductor devices.

This paper described some of the key emerging trends in SiC power electronics design. One of these trends is in design automation tools for module and board layout, device modeling, parasitic extraction, and verification techniques to address fast switching WBG technologies. Gaps indeed exist in the power electronics design automation space, and advances will be needed to maximize performance. Another trend is wide bandgap integrated circuitry. While this paper focused on SiC, there are efforts on GaN IC design to couple it with GaN devices [46]. A key enabler for WBG IC design is semiconductor device modeling for low-voltage devices. This is another emerging trend [47], [48]. The ability to design and manufacture wide bandgap integrated circuits as drivers, controllers, and protection circuitry allows them to be packaged in close proximity to the power device die to minimize parasitics that would adversely impact system performance. More 3D packaging approaches are likely to be demonstrated as part of the effort to achieve low-inductance, high power density electronics.

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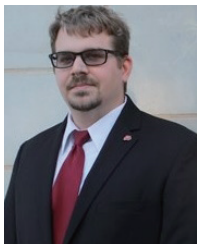

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