A Review of SiC Power Module Packaging: Layout, Material System and Integration

Cai Chen, Fang Luo, and Yong Kang

Abstract—Silicon-Carbide (SiC) devices with superior performance over traditional silicon power devices have become the prime candidates for future high-performance power electronics energy conversion. Traditional device packaging becomes a limiting factor in fully realizing the benefits offered by SiC power devices, and thus, improved and advanced packaging structures are required to bridge the gap between SiC devices and their applications. This paper provides a review of the state-of-art advanced module packaging technologies for SiC devices with the focuses on module layout, packaging material system, and module integration trend, and links these packaging advancements to their impacts on the SiC device performances. Through this review, the paper discusses main challenges and potential solutions for SiC modules, which is critical for future SiC applications.

Index Terms—Packaging material system, power module integration, SiC advanced packaging.

I. INTRODUCTION

RAPID development in power electronics systems poses strong demand for better power semiconductor devices. Silicon (Si) device has been dominating in this area for decades, and now it almost hits the material theoretical limitations [1] for further improvement on the device's switching and conduction performances. Therefore, Wide Bandgap (WBG) material based devices start to attract attention of power electronics engineers.

Compared to Si power devices, WBG power semiconductors has lower intrinsic carrier concentration (10-35 orders of magnitude), higher electric breakdown field (4-20 times), higher thermal conductivity (3-13 times), and larger saturated electron drift velocity (2-2.5 times) [2]. Translating these characteristics into device specifications, given the same die size and thickness, WBG devices can provide higher breakdown voltage, higher current, higher operating temperature, higher switching speed and lower switching loss over Si devices. TABLE I [3], [4] summaries the figure-of-merit comparisons for WBG and Si devices, which shows that, theoretically, the performance of SiC and GaN devices surpasses that of Si devices regarding switching loss, switching speed and current density with orders

TABLE I
MAIN FIGURE-OF-MERIT COMPARISONS FOR WBG AND SI POWER SEMICONDUCTORS

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81000
BFM	1.0	14.8	125.3	223.1	186.7	25106
FSFM	1.0	11.4	30.5	61.2	65.0	3595
BSFM	1.0	1.6	13.1	12.9	52.5	2402
FPFM	1.0	3.6	48.3	56.0	30.4	1476
FTFM	1.0	40.7	1470.5	3424.8	1973.6	5304459

JFM : Johnson's figure of merit is a measure of the ultimate high frequency capability of the material.
BFM : Baliga's figure of merit is a measure of the specific on-resistance of the drift region of a vertical FET
FSFM : FET switching speed figure of merit
BSFM : Bipolar switching speed figure of merit
FPFM : FET power handling capacity figure of merit
FTFM : FET power switching product
BPFM : Bipolar power handling capacity figure of merit
BTFM : Bipolar power switching product figure of merits

of magnitude. However, these outstanding benefits cannot be demonstrated in power electronics converters on the same scale due to the packaging limitations [5]-[9]. Power device packaging, which is the bridge between power device and its application, has become a bottleneck for WBG device applications [10]. The challenges in SiC power module packaging are brought by the unique characteristics of SiC devices, which can be summarized in following aspects:

A. High Switching Speed (dV/dt and di/dt)

Compared to Silicon devices, SiC device has much lower C_{oss} and Q_g, and they can switch at much higher dV/dt and di/dt [11]. High switching speed enables low switching loss and high switching frequency, which can potentially improve the converter power density and efficiency. Nevertheless, this new feature poses strong challenges for parasitic control. With the same amount of parasitic inductance, higher di/dt will generate higher voltage overshoot and ringing across the device, which can significantly increase the device switching losses, device voltage stresses and EMI noises. With the same amount of parasitic capacitance, higher dV/dt will result in higher common mode noise, which can increase the load for EMI filtering in converters.

High switching speed also brings challenges in device paralleling. Multi-chip parallel operating is an effective way for power scaling at the module level. Current balancing in both steady-state and dynamic region is the key design consideration
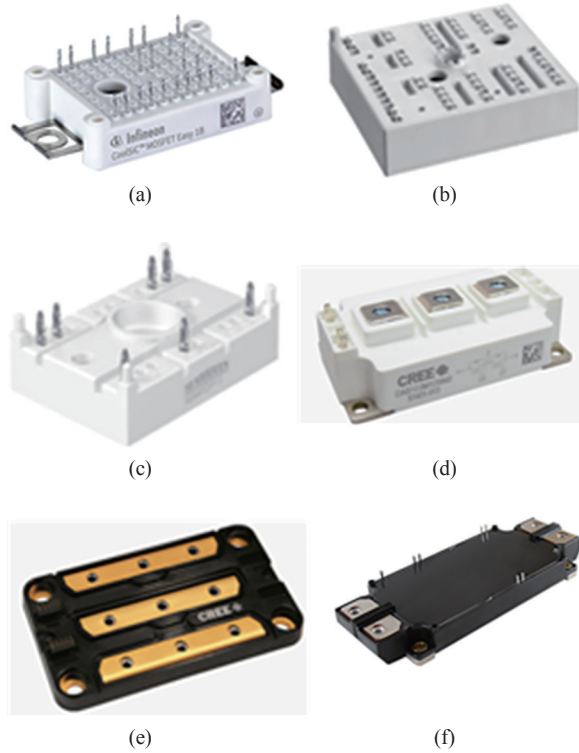
Fig. 1. Some commercial SiC power module packages: (a) Infineon Easy1B, (b) SEMIKRON MiniSKiiP, (c) SEMIKRON SEMITOP, (d) Wolfspeed 62 mm, (e) Wolfspeed high Performance 62 mm, (f) ROHM type C.

in device paralleling, which is usually realized by symmetrical layouts for the paralleled devices. High switching speed increases the sensitivity of parasitic symmetry makes it difficult to maintain current balance at high switching speed.

B. High Operation Temperature and High Electric-Field

SiC device provides the potential to achieve higher power density, which means the power package for SiC devices will also need to take much higher loss density. SiC device has the extraordinary capability for high-temperature operation up to 200°C -300°C. This temperature has been way beyond the suitable range for traditional packaging material systems for Si devices, which usually no higher than 175°C. It is important to search for new packaging material systems which can reliably sustain such a high-temperature operation.

For the same breakdown voltage, SiC device die is much thinner than SiC devices. This feature leads to challenges on the mechanical stability considerations for SiC power module packaging. Selections of appropriate substrates, die-attachment materials and encapsulation material to match with the thermal expansion coefficient of the SiC devices are the key factors to the success of SiC packaging.

Due to the same thin die thickness feature, to handle the same voltage, SiC device package will need to sustain higher electric field than that in Si power device packages. This new feature requires new insulation packaging materials to support in device applications.

In response to these challenges, this paper provides a review

from three approaches including advanced module layout, material system selection and module integration. Each approach provides a solution to one or a couple of the challenges listed above. For a fair comparison, this paper firstly presents an overview of the state-of-the-art packaging approaches for commercially available SiC devices, and then this paper summaries the new advancement in research works for advanced packaging structure, packaging material systems and the module integration trend, from both academia and industry. The prospected trend for the future of SiC module packaging is included in the last part of this paper.

II. THE STATE-OF-THE-ART FOR COMMERCIALLY AVAILABLE SiC POWER DEVICES

Driven by the emerging market, SiC device manufactures tried best to pull available resources together to provide their products to meet users' demand. TABLE II and TABLE III list major SiC manufacturers with their product specifications [12]-[16], which present the state-of-the-art packaging for commercially available SiC power products, as summarized below:

SiC discrete devices are available from 650 V to 1700 V while maximum rated current is around 120 A. In this range, TO247/220/263 and SOT 227 packages are the dominating forms of power devices. There are varieties on the pin-configurations and Kelvin Gate structure in these traditional packages. However, the nature of TO and SOT packages introduce high parasitic power loop inductances (usually around 20-30 nH) and high thermal impedance, which reduces the benefit of using SiC devices [17].

SiC Power modules are commercially available from Wolfspeed, RHOM, GeneSiC, Infineon and SEMIKRON [18]-[22]. Both Wolfspeed and RHOM provide 2-level, half-bridge, and phase-leg modules. RHOM's module is in an EconoDual package, which is similar to the state-of-the–art IGBT package. Its packaging loop inductance is around 15 nH. Wolfspeed provides different packages from its product line for different applications. 63 mm standard packaged modules. This traditional package has been widely adopted by high power Si IGBT devices. It provides benefits of high technical maturity and low cost. However, this package also comes with obvious disadvantages including high parasitic loop inductance (15 nH- 20 nH), moderate thermal impedances and heavy packaging weight. These features can potentially limit the performance of WBG devices. To address those problems, Wolfspeed announced their new generation SiC modules in their new HT package. The new design has 9 nH power loop inductance with ultra-light weight and improved thermal management. These are enabling features to unleash the potential of WBG devices. The module from GenSiC consists of a single switch instead of a phase-leg. It is in SOT-227 package, which is a standard package for Si power switches. Infineon and SEMIKRON also launched new full SiC power module and the inductance can be reduced to 15 nH.

Commercially available packages support device junction temperature up to 200°C (from STMicroelectronics and CREE), most of the off-shelf modules stays with the same temperature range as Si modules (150 °C -175°C).

TABLE II
COMMERCIAL DISCRETE SiC DEVICES

Manufacturer	Wolfspeed				ROHM			USCi			STMicroelectronics	
Voltage (V)	900	1000	1200	1700	650	1200	1700	650	1200	1200	650	1200
Technology	SiC MOSFET				SiC MOSFET			SiC Cascode		SiC JFET	SiC MOSFET	
Package	TO247/TO263	TO247/TO263	TO247/TO247	TO247/TO263	TO247/TO220	TO247	TO247/TO268	TO247	TO247	TO247	TO247	TO247
Current (A)	11.5 - 36	22 - 35	10 - 90	5 - 72	29 - 118	10 - 95	6	20	20 - 35	21 - 38	100	12 - 65
Operating Temperature (°C)	150	150	150	150	175	175	175	150	150	175	200	200
C_{oss} (pF)	20 - 60	40 - 60	23 - 220	12 - 171	35 - 148	41- 237	19	178	57	53000	305	30 - 170
Ron (mΩ)	65 - 280	65 - 120	25 - 280	45 - 1000	17 - 120	22 - 160	750	45	60 - 100	45 - 80	22	69 - 690
Q_g (nC)	9.5 - 30.4	21.5 - 35	20.4 - 161	13 - 188	172	42 - 178	17	47.5	47.5	62	215	22 - 122

TABLE III
COMMERCIAL SiC POWER MODULES

Manufacturer	Wolfspeed		ROHM	GeneSiC	Infineon	SEMIKRON
Voltage (V)	1200	1700	1200	1200	1200	
Package	45mm/62mm/High Performance 62mm	62mm	Type C/E	TO247/SOT227/TO263	AG-EASY1B-2	MiniSKiiP/ SEMITOP/ SEMI-PACK/ SEMITRANS
Current (A)	20 - 325	225	80 - 300	25 - 160	50 - 100	14 - 541
Operating Temperature (°C)	150 - 175	150	150 - 175	175	150	175
C_{oss} (pF)	100 - 2570	2500	2000 - 4000	>440000	470	NC - 1644
Ron (mΩ)	3.6 - 80	8	9.67 - 43.75	10 - 100	11 - 23	NC
Q_g (nC)	270 - 3200	4400	560 - 1500	55	62 - 250	NC - 2268

These two tables shows that most of the SiC power device manufacturers provide their SiC devices with traditional packages due to the low cost and timely market availability. Although the industry has been aware of the importance of power module packaging for SiC device, the demand on advanced power package has not yet been matched with its research and development.

III. ADVANCED PACKAGING STRUCTURES

A standard traditional power module package (as shown in Fig. 2, insert a picture here) includes a 7-layer structure, including a heat-sink, a base-plate, a DBC substrate, and die-attachments between these layers. The top side of the device is usually wire-bonded to external lead-frames, while the bottom side of the device is attached onto the DBC traces. The current flow in the device goes from the bottom contact vertically through the device and bond-wires to the terminals of the module. The module is often filled with encapsulation material to prevent the device and bond-wires from environment contamination/vibration. This module structure usually comes with high parasitic power loop inductance ranging from 20 nH to 30 nH.

As stated in the introduction, SiC device has high speed switching capability, which makes the device is sensitive to its packaging parasitics. Parasitic inductance in the power module
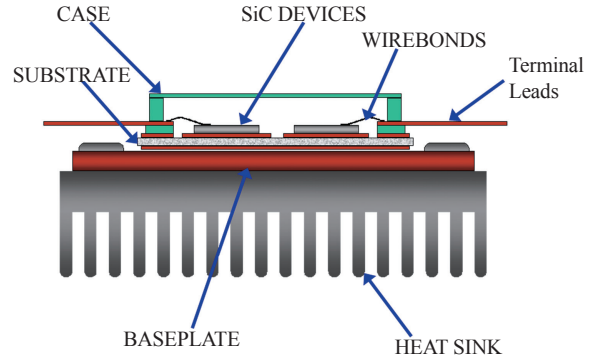

Fig. 2. The cross-section of a traditional wire-bonded power module.

induces high voltage overshoot and ringing on switching devices, which then increases the device switching loss [23] and EMI emission from the modules. Advanced packaging structure can significantly help to minimize of the loop parasitics by optimizing its current commutation loop layout within the package. Therefore, advanced packaging structure can sufficiently realize high efficiency and high frequency switching operation using SiC devices. By reducing the voltage ringing at high switching speed, this type of designs can also reduce the EMI emission from the power module.

The other benefit of using advanced packaging structure is

possibility of "double-side cooling". These structures, especially "wire-less" structures, provide two paralleled cooling paths for the SiC device from both top and bottom. This type of designs can tremendously reduce the equivalent "junction-to-ambient" thermal resistance, and thus, achieve high power density in the module.

The third benefit of using advanced packaging structure is that it is easier to achieve parasitic balancing in multiple loops while keep the same loop-minimization philosophy for each path. This advantage helps to realize multi-chip paralleled operation in SiC modules with low unbalanced in dynamic current sharing during switching transitions, and low EMI emission.

Some of the typical advanced structures are listed below.

A. Improved Wire-Bonded and Hybrid Structures

Commercial available WBG power modules employing traditional IGBT packages are mostly based on wire-bond technology and 2-Dimensional structure. Those packages, such as Econo-dual® and 62 mm packages, have high parasitic inductance (> 15 nH), and thus, to achieve stable, clean switching, the *dV/dt* of these module are usually limited to 50 V/μs. This limitation also restricts the potential of further reduction on switching losses.

The traditional wire-bonded structure has strong limitations on the parasitic control, but its advantages of maturity, simplicity and low-cost attracts the attention of manufactures.

To advance the conventional wire-bonded module design to fit with WBG device requirements while keep its advantages, lots of improvement and optimization work for wire-bonded structures has been proposed. C. Zhen from Center for Power Electronics Systems (CPES) [24] presented an improved wire-boned structure for 1200 V/60 A SiC power module in 2013 as shown in Fig. 3(a). This module adopted three-dimension (3D) leadframe in a two dimension (2D) wire-bonded multi-chip SiC module to enhance the symmetrical Kelvin Source connection for each switching device. This module also integrates the decoupling capacitors onto the substrate so that the switching ringing can be sufficiently suppressed. W. Miao and Luo. F from University of Arkansas (UARK) combined this concept with symmetrical power loop design using "double-ended-sourced" busbar structure [25] in a 15 kW SiC multichip module design as shown in Fig. 3(b), and effectively reduce the circulating current and improved the dynamic current sharing in multi-chip SiC modules. Although the external connection in these designs is 3D- leadframe, the overall module design still consists of a 2D power loop on the same single DBC plane.
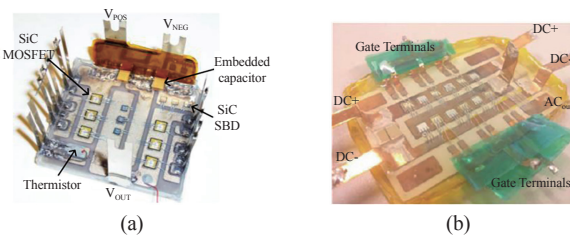
To further reduce the power loop inductance in wire-bonded structure, researchers started thinking of changing 2D power loop into 3D to reduce the loop area. Fig. 4 from Z. Chen and R. Wang from CPES [26], [28], and C. Chen from Huazhong University of Science & Technology (HUST) proposed a hybrid package for SiC modules [27]. This concept utilizes multi-layer substrates (DBC + DBC or DBC + PCB) to separate device die and current commutation traces, while the dies sits in a "caved space" surrounded by a second layer substrate. The top pads of devices can be wire-bonded to the adjacent trace pads on the top substrate layer, and then the current commutation will be between top and bottom substrates, therefore, the power loop current goes vertically between different layers instead of circulating in the same DBC plane.
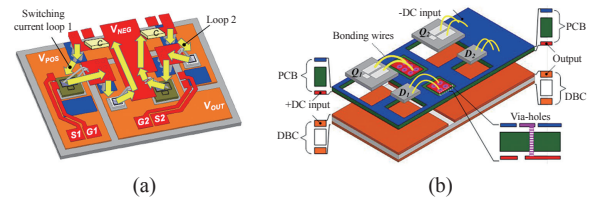

(a) (b)

Fig. 4. Hybrid packaging structure: (a) CPES's work [26], (b) HUST's work [27].

These improved structure and hybrid structure adopts benefits from wire bonding technologies with significant reduction of parasitic inductance. The inductance of these improved structure ranges from several nH to tens of nH. However, this package still has bonding-wires, which is a major contributor to the parasitic inductances. Moreover, the use of wire-bond technology requires bonding pads on the top surface of devices. This structure limits heat dissipation from the top side of the device, which makes it hard to use "double side-cooling" concept in wire-bonded packages.

B. Wireless Structure

Wireless planar structure eliminates the bonding wires, and thus it can help to reduce the packaging parasitics. Moreover, using different bonding material with the chip upper surface, different types of planar structure can be obtained. Some of them are:

1) Direct-Lead-Bonding (DLB) Structure

A direct-lead-bonding uses a copper lead for the top side connections as illustrated in Fig. 5. The top surface (emitter/cathode) connection is made directly by Pb-free soldering of a copper tab to the chip's surface [29]. The large area of top copper

(a) (b)

Fig. 3. Improved SiC Power Modules: (a) CPES's optimized design [24], (b) "double-ended-sourced" structure power module [25].
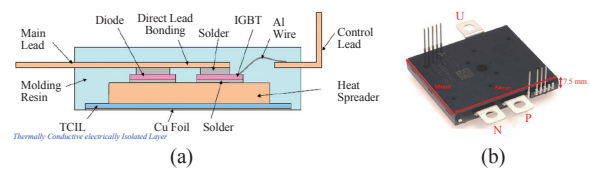

(a) (b)

Fig. 5. Illustration of DLB technology: (a) DLB structure [29], (b) Mitsubishi T-PM DLB IGBT Module [30].

lead can form a 3D power loop to reduce the parasitics. But, the thermal performance nearly hasn't improvement. Based on this structure, the Mitsubishi had developed the T-PM DLB module (Fig. 4) [30]. Which has the internal inductance reduced to 57% and internal lead resistance reduced to 50% of a wire bonded module. Furthermore, the module has more than 10 times longer lifetime. Because of the large bonding area and less thermal expansion caused by the partial temperature dissipation on the chip surface. Although this technology has not yet been used in SiC power module, it has the potential for applying it in SiC packaging for its outstanding performances.

Based on this DLB technology, a full SiC 1200 V/300 A half-bridge module had been designed by Silicon Power Corporation [31] as shown in Fig. 6. It achieved 3x the current in 1/3 the volume of the successor commercial 1200 V/100 A PowerEx module.
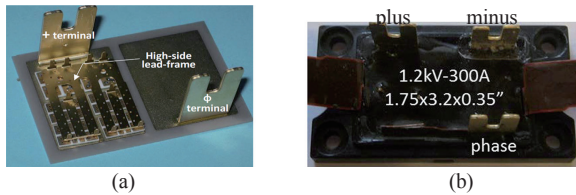

(a)   (b)

Fig. 6. Full SiC DLB module by Silicon Power Corporation: (a) inside view of one segment, (b) outside view of the whole module. [31]

2) SKiN Structure

SKiN structure uses a flex printed circuit board. In which Ag sintered directly on the top of chips and the heat sink is sintered to the DBC [32]. As the loop height is reduced, parasitic inductance can be reduced up to 10% in SKiN technology. The thermal performance has no improvement. Moreover, the SKiN technology enhances the power cycling lifetime by a factor of almost 200 relatives to the classical module design and by a factor of 40 related to state-of-the-art industrial modules.

Nowadays, this technology has been further used in a 1200 V/400 A modified SiC power module design by SEMIKRON [33] as shown in Fig. 7, and a below 1 nH parasitic power module can be obtained.
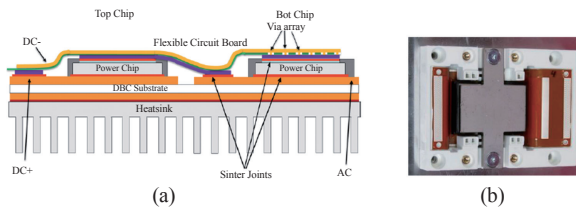

(a)   (b)

Fig. 7. SKiN technology used in SiC power module: (a) Modified SKiN structure, (b) 1200 V/400 A power module. [33]

3) Embedded Structure

Embedded structure is a multi-layer design that uses a separate layer of substrate to enclose the power semiconductor devices, as shown in Fig. 8(a). In this structure, the power semiconductor devices are mounted in the openings on the ceramic frame with an adhesive polymer that surrounds the device edges

or laminated PCB materials. After this assembly, Cu seed is deposited on the top as the interconnect layer for chip pad connection. And the Cu seed is filled with Cu by electroplating, and the Cu is structured by etching [34], [35]. As shown in Fig. 8(b), the sic embedded module proposed by CPES had reduced parasitic inductances, improved power density, and low mechanical stress [36]. In this structure, associated SMD components can be integrated in the module and placed on the top routing layer in this structure.
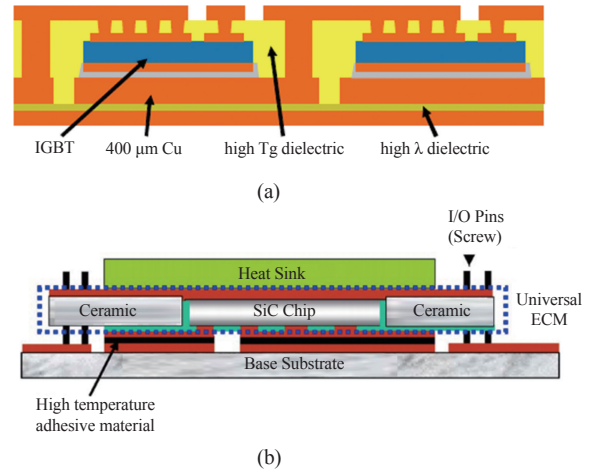

(a)

(b)

Fig. 8. Embedded structure: (a) illustration of the chip embedded [34], (b) a SiC embedded module [36].

4) Semikon Planar Interconnect Technology (SiPLIT®)

In this structure, the entire module (Fig. 9) is coated with a soft, epoxy- based insulation film applied by vacuum lamination processes. The Cu connection is developed using sputtered and galvanic Cu deposition processes (typical thicknesses are 50 μm-200 μm, depending on chip rated currents and thermal impedance requirements) [37], [38]. Since the copper connection is attached on the surfaces of DBC and chips like SKiN structure, a small loop area can be obtained. The stray inductances of this power module structure, as shown in Fig. 9(b), can be reduced by 50% (about 5 nH). A remarkable 20% R_{th}-reduction is achieved which is attributed to the additional thermal path offered by the Cu interconnects to the substrate surface. In addition, large area thermal contact improves the power cycling capability and surge current robustness significantly.
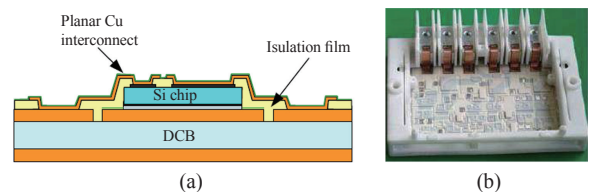

(a)   (b)

Fig. 9. Illustration of SiPLIT technology: (a) cross-section of power module, (b) SiPLIT module. [37]

5) 2.5D Structure

This is also a multilayer, multi-substrate structure. The power

chips are attached on the same substrate while the other substrate is used for routing/interconnections between two power chips. The terminal pads on the power device are connected to the routing layer through metal interposers. Due to the height difference between MOSFET/IGBT and diode chips, the top side normally will add copper pin, metal post, shim material, as shown in Fig. 10 [39]-[46]. In the case that all heights of the power chips are the same, these devices can be directly attached to the top substrate. This structure had been widely used in the applications, especially the EV/HEV systems for its low parasitic and low thermal resistance features. Many SiC power modules based on this technology are also developed. Some typical modules are shown in Fig. 11. These power module [46], [47] shows beyond 30% reduction in thermal resistance and parasitic. This structure can also be considered as an "improved version" of "Press-pack" concept.
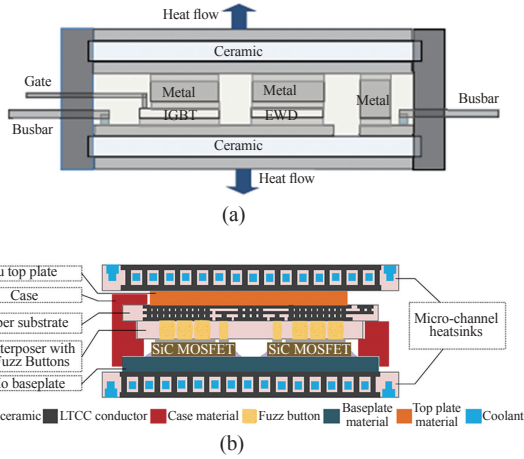

(a)

(b)

Fig. 10. Two side DBC planar bonding structures: (a) metal post connection [39], (b) pressure contact interposer connection [46].
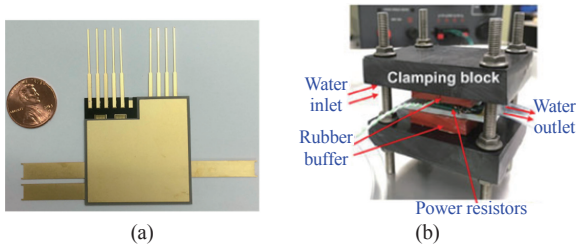

(a)   (b)

Fig. 11. Two side DBC planar bonding based SiC module: (a) ORNL's 1200 V/100 A SiC module [47], (b) uark's pressure contact interposer SiC module [46].

C. 3D Packaging Structures

3D structure can achieve extremely low parasitics (less than 1 nH), which is much lower than that in wireless structures. 3D structures discussed in this paper include power chip on chip (CoC) and wafer level CoC *etc*. 3D structure [48]-[55]. These types of structures can be summary as:

1) Chip-on-Chip (CoC) Structure

CoC is a structure that can tremendously reduce the parasit-

ics. In this structure, two power chips are vertically conneted through a metal interconnections, such as vias, copper or solder bumps *etc*. Fig. 12 shows a press-packed chip-on-chip IGBT structure. The prototype exhibits superior switching performances with reduced parasitics and EMI emissions. Also, the CoC SiC power module can use this method. [51] proposed an only 0.25 nH ultra-low inductance embedded CoC structure design as shown in Fig. 13.
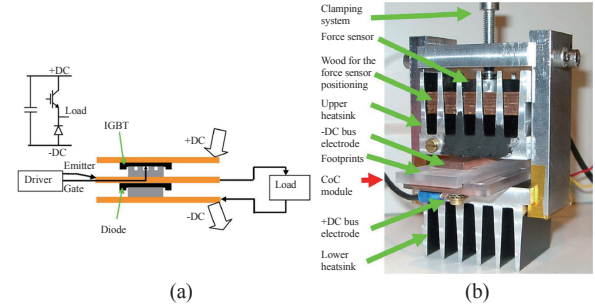

(a)   (b)

Fig. 12. Press-pack CoC IGBT buck module: (a) Electrical circuit and side view of the buck module, (b) Prototype of CoC 3D power module. [48]
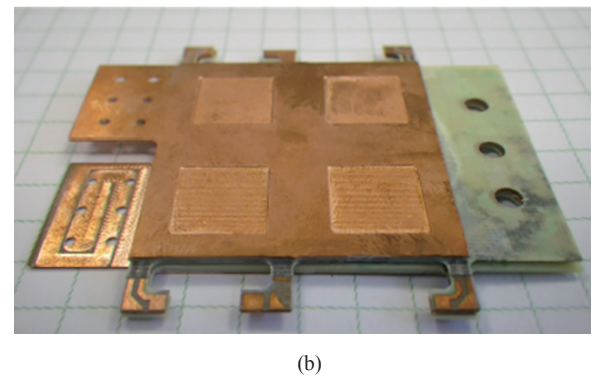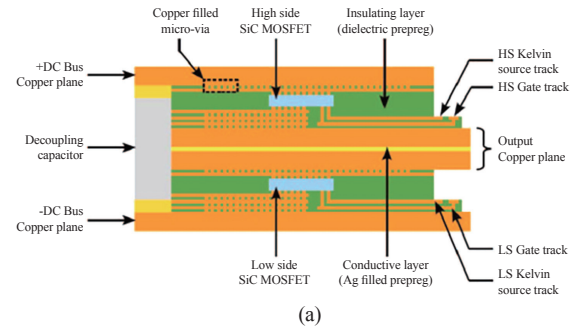

(a)

(b)

Fig. 13. CoC 3D SiC power module: (a) overview of CoC module with embedded die, (b) prototype picture. [51]

2) Wafer-Level Packaging Structure

Wafer-level chip-scale packaging technology can reduced the parasitic to smallest and especially suitable for WBG devices. Wafer-level packaging technology uses the semiconductor fabrication processes such as chemical vapor deposition (CVD), physical vapor deposition(PVD), photolithograpy and deep reactive Ion etching *etc*. to assemble devices at wafer level. Fig. 14 illustrates wafer-level copper bonding processes for the
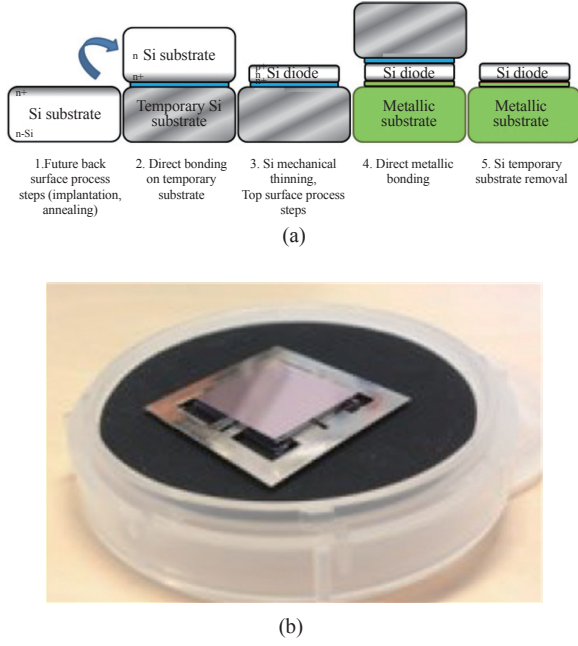
(a)

(b)

Fig. 14. 3D wafer-level packaging for vertical power devices: (a) wafer level direct bonding processes on a metallic substrate, (b) power module picture. [54]

direct attachment of high-current copper contact onto Si devices [54]. At module level, high-side and low-side power devices can be vertically interconnected through their metal contacts. Another wafer level packaging concept utilizes the Through
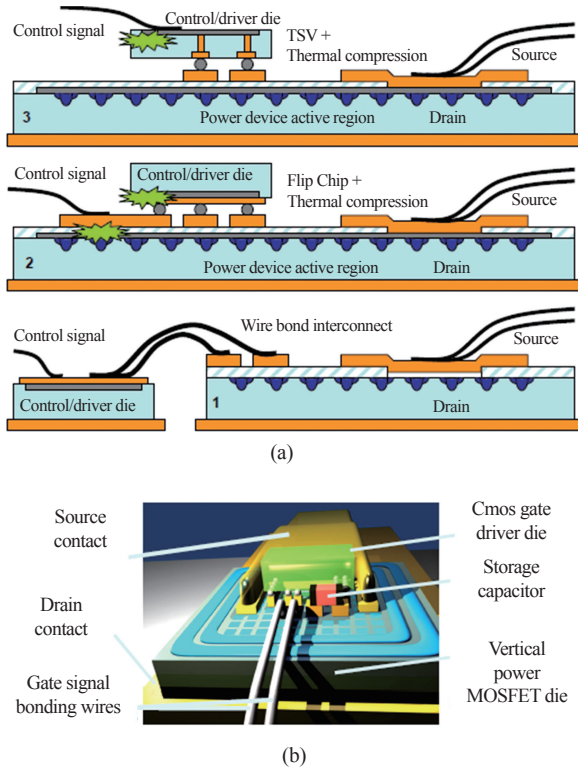

(a)

(b)

Fig. 15. Gate drive chip on power chip 3D wafer-level packaging structure: (a) TSV interconnection possibilities between the power device and gate drive, (b) Possible representation of the 3D power module. [55]

Silicon Vias (TSVs) to connect the gate drive chips and power chips, as shown in Fig. 15 [55]. This approach provides potential solution of wafer-level integration for the gate driver and the power chip. Although these technologies had only been demonstrated in Si power module packaging, they offer attractive and inspiring features to SiC power module.

IV. PACKAGING MATERIAL SYSTEM

The State-of-the-art silicon packaging material systems can operate up to 175ºC which is in compatible with the limits of Si devices. WBG devices, which can operate at much higher temperatures (200-350ºC) and electric fields (10x than Si devices), requires updated packaging material systems to provide compatible high breakdown voltage strength, compatible thermal-mechanical characteristics for better Coefficient of Thermal Expansion (CTE) matching with SiC material, and the capability of withstanding higher operating temperatures. These challenges mainly characterized to four parts – substrate, die attachment, bonding and encapsulation.

A. Substrate

A power packaging substrate consists of two metal layers and an insulation layer, usually a ceramic layer, in the middle. Different metal and ceramic materials provide different performances in module packaging. TABLE IV lists a comparison among four normally used ceramic materials [56]-[59]. Among all choices, Al_2O_3 is the most economic choice but has the highest thermal impedance and moderate mechanical strength. BeO has the highest thermal conductivity, however, the dust particle formed during its processing is hazardous to health. In comparison, AlN is a safe material featuring much higher thermal conductivity than Al_2O_3, and closer CTE matching with SiC materials. Its flexural strength is similar to that of Al_2O_3, so is its

TABLE IV
MAIN THERMAL, MECHANICAL AND ELECTRICAL CHARACTERISTICS OF CERAMIC SUBSTRATES

	Si_3N_4	AlN	Al_2O_3	BeO
Dielectric constant	8~9	8~9	9~10	6-8
Loss factor	2×10^{-4}	3×10^{-4}	3×10^{-4}-1×10^{-3}	3×10^{-4}
Resistivity (Ω·m)	$>10^{12}$	$>10^{12}$	$>10^{12}$	$>10^{12}$
Dielectric breakdown strength (kV/mm)	10 - 25	14 - 35	10 - 35	27-31
Thermal conductivity (W/m·K)	40-90	120-180	20-30	209-330
Bending strength (MPa)	600-900	250-350	300-380	≥250
Young Module (GPa)	200-300	300-320	300-370	330-400
Fracture toughness (MPa·m$^{1/2}$)	4-7	2-3	3-5	1-2.5
CTE (mm/m·K)	2.7-4.5	4.2-7	7-9	7-8.5
Available substrate technologies for thick film metallization	AMB (Cu)	DBC (Cu), AMB (Al)	DBC (Cu)	DBC (Cu)

thermal cycling lifetime. Si_3N_4 is a better choice in terms of its much higher thermal cycling reliability, but the penalties are its higher material cost and lower thermal conductivity [60].

According to the differences in manufacturing process, these substrates fall into four major categories: direct bonded copper (DBC) [61], [62], direct bonded aluminum (DBA) [63]-[66], insulated metal baseplate (IMB) [67], [68] and thick film copper (TPC) [69], [70].

1) DBC is widely used in different packaging applications because of its balance between outstanding performances and relatively low cost. DBC is made through high temperature process, during which a thin copper-oxide on the copper foil is used to create a eutectic bond between the copper and ceramic. However, the oxidization layer on the bonding interface creates a weak point of delamination, and thus, DBC has moderate life-time in thermal cycling. Active Metal Brazing (AMB) process is another choice to join the metal and the ceramic [61]. Using AMB process can eliminate the oxidization layer, and thus, it can improve the life-time of the substrate.

2) DBA has to be mentioned. [63] It uses AlSi-brazing to bond the aluminum and the ceramic. The DBA substrate with the Al alloy base plate is capable of increasing the module reliability in terms of thermal cycling. However, thermal conductivity of DBA is not better than that of DBC. To further improve the thermal conductivity of DBA substrates, lots of variations have been proposed [71]. In these variations, Al is used as a buffer to release the thermal-mechanical stresses, and a layer of copper is deployed to enhance the thermal conductivity of the substrate. Fig. 16 shows the combination of these metal layers in new DBA substrate design, which has significant increasing in life-time of their thermal cycling.
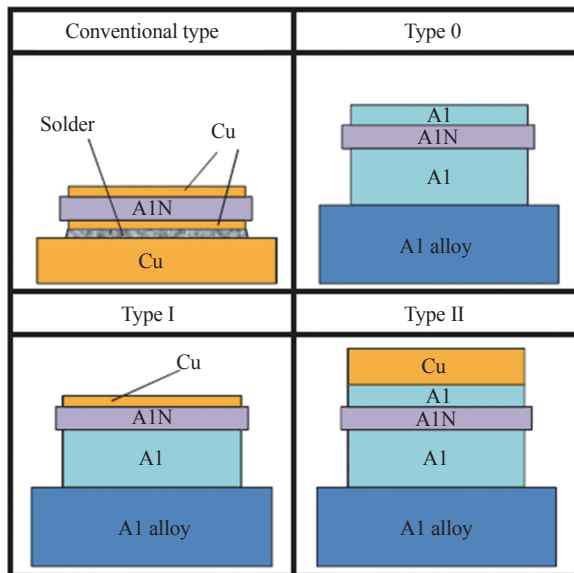

Fig. 16. Schematic showing a comparison between three types of module structures and the conventional modules structure. [71]

3) IMB is another good substrate candidate. Since IMB do not have complexity of fabrications and high temperature treatment as DBC, IMB has lower fabrication cost and long term reliability. It consists of a highly thermal-conductive insulating resin sheet, a copper baseplate and thick copper foils. IMB has good heat dissipation while satisfying the isolation requirement. It's reported in Mitsubishi IGBT module that (Fig. 17), with optimized IMB insulating material and thickness, the module's life-time in thermal cycling has been enhanced, and the effective chip-mounting area has been increased by 23% [67]. The Samsung used a similar CBM^{TM} substrate [68]. The life time reliability has been extended more compared to the DBC substrate even in extreme test conditions.
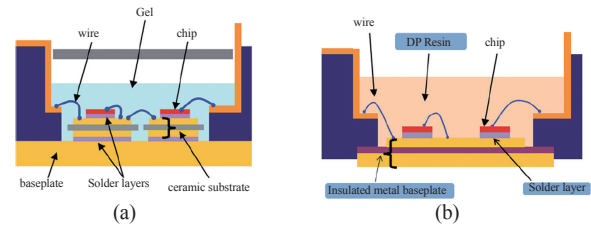

Fig. 17. Cross-sectional view of package: (a) conventional ceramic substrate and (b) proposed IMB. [67]

4) Another method to form metal bonded ceramic substrates is using TPC [69], [70] technology. Thick layers of copper paste are applied by screen printing process and are fired at 850-950 °C to sinter the metal powders and create a high adhesion bond between the metallic film and the ceramic substrate. This technology provides excellent temperature cycling reliability and opens possibility to combine power and logic components by parallel realization of thin and thick Cu pattern tracks. As shown in Fig. 18, standard DBC substrates on alumina failed before 200 thermal shock cycles (−40 °C, +150 °C), thick print copper substrates on alumina show no sign of delamination even after 2000 cycles and thick print copper on aluminum nitride remains stable up to 1800 cycles.
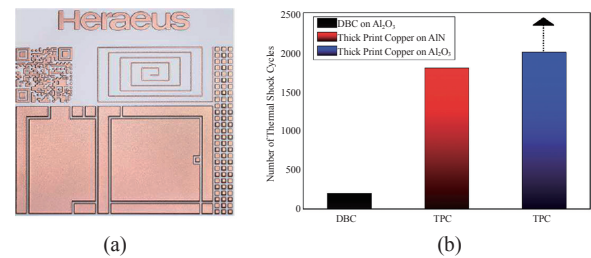
Fig. 18. TPC substrate: (a) 300μm thick printed copper substrate, (b) reliability comparison results. [69]

Fig. 19 shows the comparison of above four types of substrate, as shown in the DBA, CBM and TPC have the highest reliability. Since the constraint of high temperature isolation material for CBM, it cannot work at high temperature SiC packaging. Therefore, DBA derivative types and TPC will be a good candidate for high temperature WBG device packaging.
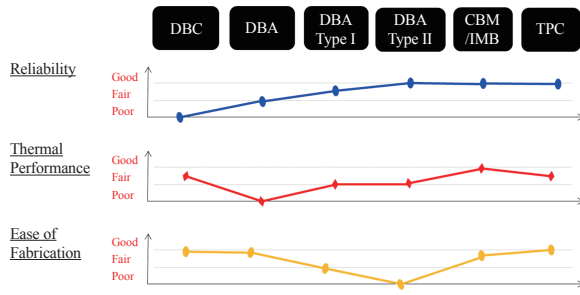
Fig. 19. Comparison of different types of substrates.

B. Die-Attaching Materials

Die-attaching materials fall into many categories, spanning both high and low temperature use. The five main categories are (1) epoxy adhesives, (2) alternative resins, (3) eutectic die attach solders, (4) soft soldering and (5) silver-glass material [72]. Two of the most commonly used die-attach materials today are solder alloys and conductive epoxy. Most silver filled epoxies used in commercial small-signal devices fail at temperatures near 200 °C. Their low operational temperatures are not workable solutions for high temperature applications. Alternative resins with the use of organic compounds are applicable also to low power Si devices.

Beyond 200 °C, [72] had summarized the existing die attaching materials as shown in Fig. 20. In the low temperature range 200~300 ℃, the tin-lead (Pb-Sn) and lead-free tin-silver-copper (SAC) alloy solder are listed in the figure. As we can see in the middle range 300~400 ℃, the tin-lead (Sn-Pb) solder systems

have high liquidus points and they have been popular for high temperature die attach materials thus far.

However, the higher the Pb content, the slower the throughput in automated die attach machines, due to the time required for the Pb-Sn liquid to re-solidify after the die attach operation is completed, causing voiding in between the die and substrates' crevice. For larger dies, which require more die attach material coverage, the voiding issue will be more pronounced. Additionally, since the ban on hazardous materials in consumer electronics since 2006, and beyond consumer electronics in the whole electronics industry nowadays, the Pb solder are forbidden [73]. Hence, the lead-free high temperature solder are emergency technology. It is worth noting that lead-free silver sintering, diffusion soldering and reactive multilayer bonding are emerging die attach technologies with the potential to provide improved chip to substrate interconnection in terms of mechanical, electrical, high temperature and thermal performance [74]-[78]. As depicted in the high temperature range in the figure, these solders have very high liquidus temperature.

Silver sintering is also known as low temperature joining technique (LTJT). The process is based on the spontaneous sinter ability of silver particles in the nano and micro scale with applied pressure at temperatures of above 220 °C [79]-[85]. Silver sintered interconnections show numerous advantages such as a remarkable high melting point of 961 °C, a far better thermal conductivity (250 W/mK) and an enhanced electrical conductivity (41 MS/m). In addition to the positive mechanical characteristics, such as a CTE value of 19 μm/mK and a good tensile strength of 55 MPa, they show considerably enhanced reliability in thermal and power cycling tests. Today, silver sin-
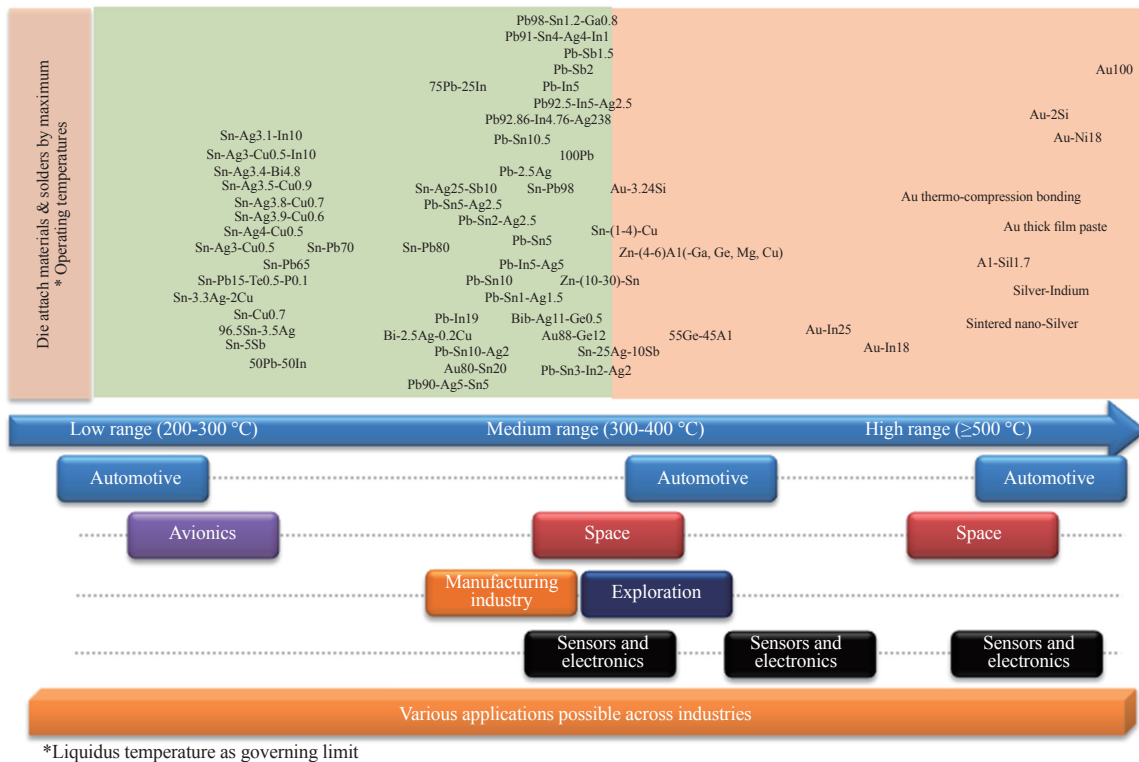

Fig. 20. Various die attach materials and solders, their operating range and application possibilities. [72]

tering is applied during industrial manufacturing for a range of selected products but has not been introduced as a flexible and versatile technology platform into mass manufacturing. The root cause for the current situation is that quality issues and failures in silver-sintered contact interfaces in dependence of chip and substrate metallization, as well as variations in the sintering process, are not understood in detail and will be the aim of further research.

Diffusion soldering describes an interconnection technology based on a metal interlayer where solid-solid as well as liquid-solid diffusion between joining materials is stimulated. Transient Liquid Phase Bonding (TLPB) realized by bonding of parent materials with pre-deposited low-melting metal layer, whereas Transient Liquid Phase Soldering (TLPS) involves usage of the printed standard soft solders as interlayer for intermetallic phase (IMP) formation [77], [86]-[89]. The diffusion solder have Ag/In [90], [91], Ag/Sn [92], Au/In [93], [94], Au/ Sn [95], [96], Cu/Sn [97], [98], and Ni/Sn [99]. Considered the cost and environment friendly, the Cu-Sn alloy solder has been a good candidate for high temperature applications. Because of lack of the understanding of physical principle, characterization and soldering processes, the use of these materials are not well known.

In summary, the presented new concept joining technologies show remarkable properties with the potential to improve the quality of power electronic packaging. Hence, knowledge of specific quality and reliability-affecting factors, as well as the availability of adequate testing methods for a detailed characterization of the formed metallic joints, are necessary in order to assure a high strength and a long term reliability of silver sintered, diffusion soldered or reactive bonded devices.

C. Bonding Methods

Copper wire bonding (Fig. 21(a)) is one of the most promising technologies for connecting high current interconnections in power electronics assemblies [76], [100]. The high flexibility in the layout and established quality from the aluminum wire bonding process are two reasons to promote the development of Cu wire bonding. Using copper material over aluminum for wire bond interconnections provides two key benefits such as, increase in current capacity by 37% and the excellent thermal conductivity of copper (~80% better compared to Al). Recently, novel heavy wire bonds made of an Al and Cu composite material [101] were introduced as shown in Fig. 21(b). In contrast to a pure Cu-wire no change in the metallization of the chip surface is necessary to establish a stable bonding process. The new material is still under development with the goal to increase the Cu content to a maximum without yield problems during the bonding process.
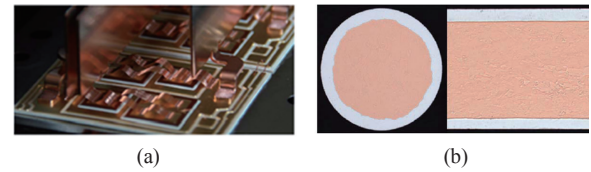

Fig. 21. Novel wire-bonding: (a) Cu wire-bonding [76], (b) Cu-Al wire bonding [101].

Another bonding method should be noted is Cu and Al ribbon bonding [100], [102], [103] as shown in Fig. 22. Due to the lower number of ribbons required to achieve the same interconnect resistance as for wire bond interconnects. These connections can carry higher currents and show better power cycling capabilities in dependence of the respective bonding process and the chosen ribbon material. Al or Cu ribbon bonding is an attractive new interconnection solution for the replacement of wire bonds between the power semiconductor and the substrate.
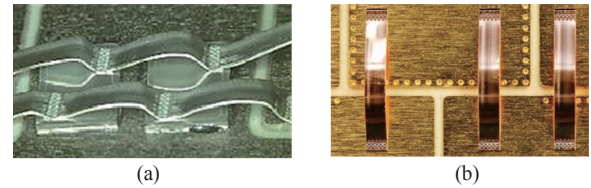
Fig. 22. Ribbon bonding: (a) Al ribbon [100], (b) Cu ribbon [102].

TABLE V
SUMMARIES CANDIDATES FOR HIGH VOLTAGE ENCAPSULATION

Material	Part Number	Manufacturer	Dielectric Constant	Breakdown strength	Temperature Range (ºC)
Dielectric Fluid	Novec® 7500	3M	5.8	35 kV, 0.1" gap	128 max.
Polyamide Imide (PAI)	Torlon® 4203	Boedeker Plastics	4.2 (@ 1 MHz)	100 – 280 kV/mm	260 max.
Epoxy	Hysol® -60NC	Henkel	21.7	550 V/mil	-
Silicone	3-6635	Dow Corning	20.5	20 kV/mm	-80 to 200
Silicone	Sylgard® 567	Dow Corning	2.79 (@ 100 kHz)	16 kV/mm	-45 to 200
Silicone	TSE3051	Momentive	2.8	18 kV/mm	-
Silicone	CF2186	Nusil	35.4	19.5 kV/ mm	-140 to 315
Silicone	R-2188	Nusil	2.6 (@ 100 kHz)	500 V/mil 19.5 kV/mm	-
Benzocyclobutene (BCB)		Dow Chemicals	2.65	530 kV/mm	

D. Encapsulation

Encapsulation materials protect the power module components from external environmental damages, such as moisture, solvents, gases, and radiations [104], [105]. In addition, encapsulation materials improve the voltage ratings of the packages, in high voltages modules (>1000 V) and prevent arcing between different electrodes. However, the soft conventional encapsulation materials mainly designed for Si conventional module are limited to low temperature of about 200 °C. Therefore, identifying new materials for higher temperature application is mandatory.

Without considering hermetic packaging where gases, vacuum and liquids can be used as dielectrics, three types of materials might be suitable for high-voltage high-temperature power electronic packaging; glasses, hydroset ceramics and polymers. The main drawbacks of glasses are they have high firing temperatures more than 500 °C and they have high Young modulus causing high thermo-mechanical stresses.

In contrast, hydroset ceramics offer low curing temperature (curing can be realized at room temperature). However, those ceramics get a high Young modulus (>100 GPa) and a coefficient of thermal expansion (CTE) between 3 and 6 ppm/°C that can induce high stresses in the structure. The CTE mismatch materials can lead to severe reliability problem.

Polymeric encapsulation is the third type of materials and can be divided into two categories: soft and hard encapsulation. Soft encapsulation materials exhibit a very low Young modulus in order of several MPa and a high CTE. Silicone gels belongs to this kind of polymers and are widely retained for encapsulating high voltage multi-chip power assemblies, due to their very high softness and high insulating electrical properties. However, the literature review shows that high temperature commercially available silicone gels exhibit a maximum temperature limit lower than 250 °C for continuous service of operation [57], [106]. The review also reveals that a trade-off between high temperature ability and softness of silicones generally exists. In fact, a slight extension of the temperature range (up to 250 °C - 275 °C) might be obtained with the use of silicone elastomers.

In the second category, polymers are relatively hard and exhibit a low CTE and a relatively high Young modulus (several GPa). The reliability of some of the second category polymers (like polyimide BPDA-PDA and PA-HT), tested at temperature exceeding the 300 °C seems satisfactory [107]. However, the deposition technique of the former and the limited thickness (50 μm) of the latter (deposited by polymer vapor deposition) reduce their use at the wafer level.

Other polymers, like benzocyclobutene BCB are candidates and are stable at the temperature above 300 °C, but the major issue encountered for thick films is the void generation during the curing process [108].

In response to the high-voltage/ high electrical-field feature in SiC modules, encapsulation material with high breakdown voltage is also important to the packaging system. Off-shelf choices for these materials include silicone Gels, PAI materials

and BCB materials. TABLE V summaries candidates for high voltage encapsulation [109]-[115].

V. SiC Module Integration

SiC devices is capable of high switching speed and high-temperature operation, yet it is sensitive to the packaging parasitics. Using advanced structure can significantly help with this problem. Integrating power devices with its associate components, structurally and functionally, is another way to solve this puzzle.

Module-level integration integrates associated components, such as decoupling capacitors, gate drivers, temperature sensors, current sensors and protection circuits, in the same package. This idea has been proven to be capable of further mitigating the influences from packaging parasitics. It is a good approach to improve the density and efficiency of power electronics converters [25]-[27], [51], [116]-[123]. The Intelligence Power Module (IPM) is one of the successful products which demonstrate this concept. SiC module may require a higher level of functional and structural integration trimmed for the new characteristics of the device [27], [51], [53], [55], [121], [122], [124].

A. Integration of Decoupling Capacitor

References [24]-[28], [51] described a solution that embedded discrete Multilayer Ceramic Capacitor (MLCC) decoupling capacitors in the SiC modules, as shown in Fig. 13. This integration approach can significantly reduce the distance between power device pair and the decoupling capacitors, and thus reduces power loop parasitics, suppresses the voltage overshoot and improves current sharing among paralleled devices. This method can achieve clean switching waveforms, low electromagnetic interference, and higher power efficiency at high switching speed.

B. Integration of Gate Driver

Integrating gate drives with the power chip in the module can tremendously reduce the gate driving loop inductance and improve the driving performances. Using Silicon-on-Insulator (SOI) technology or SiC low voltage device technology, high-temperature gate driver integration can be realized in SiC modules.

Fig. 23 illustrates an integrated design from SEMIKON that SOI gate driver ICs is directly mounted on the DBC substrate in

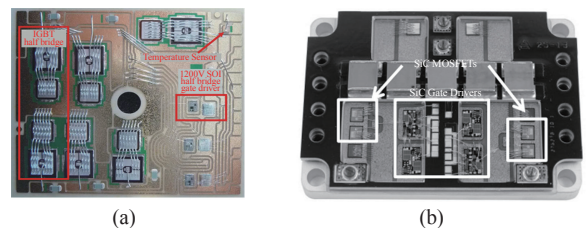(a)   (b)

Fig. 23. Integration of decoupling capacitor and gate driver: (a) SOI gate driver integration in IGBT power module [126], (b) decoupling capacitor and SOI gate driver integration in SiC power module [119].

a 1200 V IGBT half-bridge MiniSKiiP module [125], [126] and demonstrated significant improvement in the module switching performance. The University of Arkansas had developed a SiC half-bridge switching module with integrated SiC gate drivers and dc-decoupling capacitors [119], [127]. The integrated gate drivers require no gate-damping resistance because of the extrememly low parasitic gate inductance.

C. Integration of EMI Filters

Increasing switching speed is usually an advantage from the thermal and efficiency points of view, yet it has detrimental effects on the EMI emission. The "side-effects" of fast switching is that SiC module may generate too much EMI noises, and thus, a more bulky EMI filter is required at the converter level. Integrating EMI filters in SiC module and "self-containing" the noises within the module is a promising approach from converter design point of view. References [123], [128] provide a solution to directly integrate the CM filter capacitors in the power module, as shown in Fig. 24. This makes it possible to "capture" the high-frequency harmonics directly at the source.
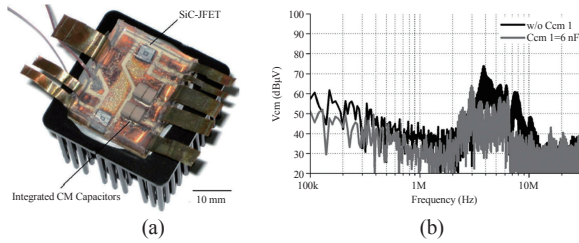

(a)   (b)

Fig. 24. The power module with integrated common mode filtering: (a) SiC-JFET power module prototype with integrated CM capacitors, (b) EMI spectrum comparison between with and without integration. [123]

D. Integration of Sensor

Integrated sensors are often present in Si- IGBTs [129] or power modules like in Infineon's MIPAQ family, providing valuable information, which can be used either for monitoring, failure mitigation or studying the device aging. It is then obvious that such information is valuable for SiC-MOSFETs as they begin to be integrated into power systems.

Temperature and current sensors can be integrated into the package separated from the main device; in this case, providing information on the package temperature and device current. However, this type of method cannot react fast and the additional current sensor will increase the loop distance. The sensor integrated in the SiC-MOSFET active area by monolithic in-
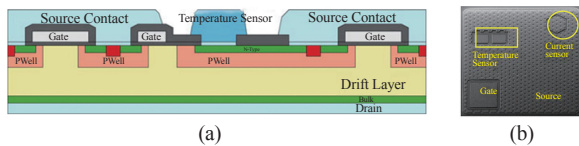

(a)   (b)

Fig. 25. Monolithic integrated sensor in SiC MOSFET: (a) schematic of cross-section, (b) SEM picture of fabricated 2.25 mm^2 SiC power MOSFET with monolithically integrated temperature and current sensors. [124]

tegration technology will be an emerging technology to solve it. This can provide a more precise temperature measurement in the device itself, allowing fast reaction in case of failure and more accurate information. As shown in Fig. 25, [124] proposed a SiC MOSFET with monolithic integrated sensor.

E. Integration of Thermal Management System

In a SiC power module, the heat-sink can be integrated with the baseplate or with the DBC. This integration strcture can significantly reduce the thermal impedance in the module through eliminating thermal-interfaces between the SiC device die and the ambient. Nowadays, the pin-fin baseplate power module [130]-[133] is widely used in automotive applications. The power module described in reference [130]-[133] integrated pin-fin on the baseplate and can be directly mounted on a liquid cold plate. Fig. 26(a) shows the new Mitsubishi J1-Series pin-fin integrated IGBT module, which demostrate a 76% weight reduction and 30% thermal performance improvement for three phase inverter solutions. Fig. 26(b) shows a pin-fin integrated, double-sided cooled, SiC module design from ORNL [47] , which achieves a 40% reduction in thermal resistance.

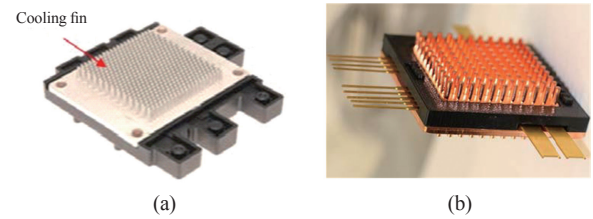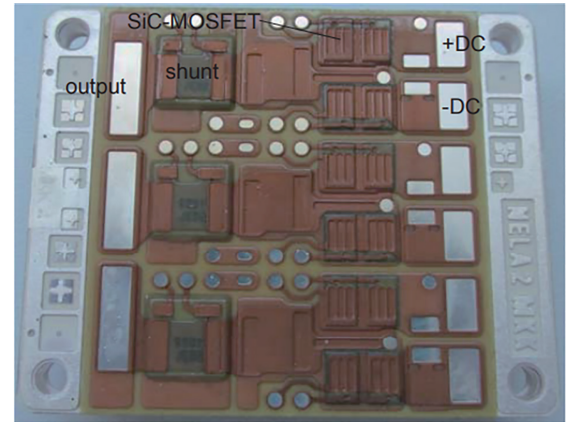(a)   (b)

Fig. 26   Pin-fin integrated power module: (a) Mitsubishi J1-Series IGBT module [130], (b) SiC pin-fin double sided cooling module [47].

(a)

(b)

Fig. 27. Full SiC power module with cooling sintering on substrate: (a) top view, (b) side view. [134]

However, the mechanical assembly and the liquid sealing for the pin-fin module is a weak point in the system, and a threaten to the life-time of the module. An alternative approach is to sinter the ceramic substrate directly onto a sealing-free heatsink such as a microchannel copper cooler [134]. This combination offers a very low thermal path between substrate and cooling liquid. Fig. 27 shows a SiC power module [134] with ceramic substrate directly sintering on a sealing-free heatsink micro-channel copper cooler.

VI. Conclusion

This paper provides overview for the state-of-the-art packaging technologies for SiC power modules. The paper covers the information regarding off-shelf SiC devices and the advanced packaging technologies from on-going research efforts. The paper summarizes these research advancements for SiC modules from three aspects: (1) module layout and structures, (2) new packaging material systems, and (3) module integration trend.

According to existing literatures, the focal points of on-going SiC module research include: (a) parasitic inductance minimization for power loop and gate loop, (b) high temperature operation design and (c) module integration to further optimize SiC switching operation with EMI noises self-containment and better thermal management. Most of the new packaging layouts, structures and integration schemes are developed for reducing the influences from package parasitics and side-effects of fast switching. The packaging materials system for SiC device is more determined by its nature of high temperature/high electric-field operation. The design trade-off is typically in thermal-mechanical-electrical multi-physics domain. Integration is an important trend for SiC devices as it provides numerous benefits for SiC switching operation. All these new approaches are for the purpose of unleashing the intrinsic benefits from SiC devices in its applications to achieve higher power density and efficiency over Si-based power conversion. It is clear that, duplicating Si packaging technologies and "dropping-in" SiC device will not have desire performance output that matches to SiC characteristics. New packaging architecture trimmed for SiC is required for future power electronics systems.

Thermal management is another important topic for SiC packaging, yet its content is relatively independent to the device itself and worth another paper dedicate on this topic.

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