Review of GaN Totem-Pole Bridgeless PFC

Qingyun Huang and Alex Q. Huang

***Abstract*—Switching-mode AC/DC converters are widely used in modern power supplies for computers, data centers and telecommunication equipment. Achieving Power Factor Correction (PFC) and high efficiency are the two most important requirements. In many cases, high power density is also of tremendous interest. Both power efficiency and power density are greatly influenced by the power devices, the topology and the control used. Compared with conventional Si power MOSFET and Si super-junction MOSFET, the newly introduced 600 V GaN devices not only eliminate the reverser recovery, but also have much lower switching and driving losses. These excellent properties enable the emergence of the totem-pole bridgeless AC/DC converter as the next generation preferred solution for PFC instead of the state-of-the art Si-based boost PFC. In this paper, the key technologies and designs for both hard-switching and soft-switching GaN totem-pole PFC are reviewed and the key performance metrics are compared. A soft switching, 3.2 kW totem-pole PFC prototype with 99% efficiency and 130 W/inch3 power density has been achieved in the author's group as a proof of the concept. Based on the power density comparison, the high frequency soft-switching GaN totem-pole PFC is the preferred choice to achieve both high efficiency and high power density at the same time.**

***Index Terms*—Bridgeless PFC, PFC, soft switching, totem-pole PFC, WBG power device.**

I. Introduction

SWITCHING-MODE AC/DC converters are widely used in modern power supplies for computers, data centers and telecommunication equipment [1]. It is predicted that the data center alone will consume about 10% of the total electricity by 2020 [1]. High efficiency and high power density are two factors driving the technology innovation and evolution.

Before the emerging of the wide-band-gap (WBG) devices, the 600 V Si super-junction (SJ) MOSFETs are the-state-of-the-art power devices for offline AC/DC power supplies with a 400 V DC bus and with a power level below several kW. Due to the poor reverse recovery property of the Si MOSFET and Si SJ MOSFETs, negative current condition is not preferred in these devices and it is hard to find a topology better than the conventional Boost power factor corrector (PFC) operating in Continuous Conduction Mode (CCM). The semi-bridgeless dual-Boost PFC has lower conduction loss, but its utilizations of the devices and the inductors are much worse compared with the conventional Boost PFC [2]. Thus, in the past few decades, the conventional Boost PFC has been the most mature solution for the single phase offline PFC. Due to the relatively large switching loss, the switching frequency is typically below 100 kHz, limiting the reduction of the converter size. Two example of hardware based on the conventional Boost PFC with Si SJ MOSFETs are shown in Fig. 1 [3], [4].

(a) (b)

Fig. 1. Examples of hardwares based on the conventional Boost PFC with Si SJ MOSFETs: (a) Eltek product AC/DC (PFC+LLC) product, 3 kW, 4.25 x 1.69 x 13 inch^3 [3]; (b) ST 3 kW PFC evaluation board, 9.6 x 4.3 x 1.4 inch^3 [4].

The emerging of the 600 V GaN devices, which have low on-resistance, fast switching speed, and zero reverse recovery loss, are fundamentally changing the above conclusion hence the design of the AC/DC converters [5], [6]. For the PFC stage of the AC/DC power supplies, the totem-pole bridgeless PFC with 600 V GaN devices has shown superior performance compared with the conventional Boost PFC and the semi-bridgeless dual-Boost PFC [1], [7]. The GaN totem-pole PFC can achieve very low conduction loss thanks to the ever decreasing device R_{on} that is inherently a feature of any WBG power device [5]. The device and inductor utilization is high and the EMI noise is also low in the totem-pole PFC [7]. The GaN totem-pole PFC can work under hard-switching mode or soft-switching mode. Note that, for hard-switching mode, the totem-pole PFC cannot be used with the Si SJ MOSFETs due to the severe reverse recovery loss in SJ MOSFETs. However, the GaN totem-pole PFC has been proven to be able to work under hard-switching mode with 99% efficiency due to the elimination of the reverse recovery issue [7], [9], [10]. In the hard switching case, the dominant dynamic loss is the device's turn-on loss since the turn off loss is very low due to the lossless charging of the output capacitance C_{oss} of the device [5], [6]. The dominant turn-on loss can be further eliminated by employing the zero-voltage-switching (ZVS) technique in which the energy stored in the output capacitance E_{oss}, is recovered. ZVS based GaN totem-pole PFC has been shown to operate well above 1 MHz switching frequency while still maintain 99% efficiency [1], [8]. The soft-switching GaN totem-pole PFC with increased switching frequency and efficiency therefore significantly improves the power density compared with the CCM Boost PFC [1], [8].

This paper is organized as follows. In Section II, the 600 V GaN devices are discussed in detail. In Section III, the topologies of GaN totem-pole PFC is reviewed and compared with the con-

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The authors are with the University of Texas at Austin, Austin, Texas, USA (e-mail: qyhuang@utexas.edu; aqhuang@utexas.edu).

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ventional PFC topologies. In Section IV and V, the technologies and the performances of the hard-switching and soft-switching GaN totem-pole PFC are reviewed respectively. Finally, the summary and conclusions are included in Section VI.

II. 600 V GaN FETs

GaN heterojunction FET (HFET) is a superior device that is commercially available from 30 V to 600 V. The device is typically fabricated on GaN-on-Si wafers and utilizes a lateral structure with Source, Gate and Drain terminals all on the same side of the wafer. A lateral structure has lower utilization of the chip area compared with a vertical power device. However, this is not a major factor preventing the GaN HFET to achieve amazing performance gains over competing vertical Si power devices such as Si SJ MOSFET. Due to the high channel mobility (~2000 cm^2/V-s) and the elimination of the substrate conduction resistance R_{sub}, as well as the very short drain to source spacing requirement that is inversely proportional to the peak electric field strength of the GaN material, the lateral GaN HFET's R_{on} is still significantly reduced for a given chip size. This reduction in R_{on} or $R_{on\text{-}sp}$, directly results in the reduction of the chip size which translates to smaller device capacitance. Furthermore, the lateral HFET structure where the charge layer is concentrated on a thin top layer and the terminals are non-overlapping with each other, the junction capacitance (C_{iss}, C_{oss}) is further reduced compared with vertical devices even if the chip area is the same. Thus, the smaller chip size and the lateral structure both contribute to a substantial reduction of the device capacitance. This feature makes the GaN HFETs very close to an ideal high frequency switch. Due to the absence of any PN junction in the GaN FET, there is no minority carrier injection hence no stored charge. This results in a reverse recover free operation of the GaN HFET when it is used as a rectifier. This is a major advantage of GaN over Si power MOSFETs.

The performances of the 600 V state-of-the-art Si SJ MOSFET, SiC MOSFET and GaN HFETs are compared in TABLE I. Three normalized device figure of merits (FOMs) are comapred in TABLE I. The smaller the FOM, the better the device is. FOM1 represents the speed of the gate driving. The smaller the FOM1, the faster the gate drives. For FOM1, both SiC and GaN devices are much better than Si SJ MOSFET. The enhancement-mode GaN FETs have much smaller FOM1 than SiC MOSFET. However, the SiC MOSFET has smaller FOM1 than cascade GaN FET. This is caused by the high input capacitance of the integrated low voltage Si MOSFET in the cascode GaN structure. FOM2 represents the switching loss for both hard-switching and soft-switching. The smaller the FOM2, the less the switching loss. Note that the state-of-the-art Si SJ MOSFET of Infineon G7 series has even lower FOM2 than SiC and GaN devices. And GaN FETs are not better than SiC MOSFETs. FOM3 represents the reverse recovery loss. The smaller the FOM3, the less the reverse recovery loss. Both SiC and GaN devices have significant reduction of the reverse recovery loss. The enhancement-mode GaN FETs have zero reverse recovery loss. The reverse recovery loss of the cascode GaN FET is not zero due to the reverse recovery loss of the low voltage Si MOSFET. The severe reverse recovery loss of the Si SJ MOSFETs causes that the synchronous rectification of Si SJ MOSFETs is not preferred under the hard switching condition. However, the WBG devices have changed this phenomenon, especially the enhancement-mode GaN devices, since they eliminate the reverse recovery issue. This in turn enable the use of totem-pole circuit for PFC as discussed in the next section.

TABLE I
COMPARISON OF 600 V FETS

600V FETs	Part Number	R_{on} (mΩ)	C_{iss} (nF)	FOM1 (R_{on}•C_{iss})	Q_{oss} (μC)	FOM2 (R_{on}•Q_{oss})	Q_{rr} (μC)	FOM3 (R_{on}•Q_{rr})
Si SJ	IPT60R028G7 [11]	28	4.82	135	0.074	2.072	8.7 (100A/μs, 400V)	243.6
SiC MOS	SCT3030 [12]	30	1.53	45.9	0.085	2.55	0.13 (1100A/μs, 600V)	3.9
Enhancement-Mode GaN FET	GS66516T [13]	25	0.52	13	0.113	3.25	0	0
	PGA26E07BA [14]	56	0.405	22.68	0.045	2.52	0	0
Cascode GaN FET	TPH3207WS [15]	35	2.2	77	0.11	3.85	0.18 (1000A/μs, 400V)	6.125

III. Topology of GaN Totem-Pole Bridge-Less PFC

The Boost PFC is the most conventional topology for the server power supply products [2]-[4], [16]-[19]. As shown in Fig. 2(a), a diode bridge rectifier is cascaded with a Boost converter. A diode with low reverse recovery charge has to be used. A popular choice is to use a 600 V reverse-recovery-free SiC Schottky diode. The Boost PFC has low cost, low CM noise and high reliability. However, the efficiency is low due to the high conduction loss in the diodes.

The semi-bridgeless dual-Boost PFC, as shown in Fig. 2(b), eliminates one low frequency diode in the line current path [20]-[22]. Thus, the efficiency is improved compared with the conventional Boost PFC. Since the grid side is directly connected to the DC side by D_1 or D_2, the common mode (CM) noise is also low. In this topology, the two Boost converters will alternatively work during the positive and negative half line cycles. The low utilization of the inductors and devices reduces the power density and increases the cost compared to the conventional Boost

PFC.

The totem-pole bridgeless PFC, as shown in Fig. 2(c), has only one MOSFET and one low frequency diode conducting at any time. Thus, it has the lowest conduction loss compared with the conventional Boost PFC and the semi-bridgeless dual-Boost PFC [2], [23]-[26]. This topology consists of one high-frequency half-bridge (S_1 and S_2) and one line-frequency half-bridge (D_1 and D_2). During the positive half line cycle, since D_2 is conducted, the grid neutral point is connected to the negative terminal of the DC side. S_2 is the active switch, while S_1 acts as the synchronous rectifier (SR) switch. During the negative half line cycle, since D_1 is conducted, the grid neutral point is connected to the positive terminal of the DC side. S_1 is the active switch, while S_2 is the SR switch. In the totem-pole PFC topology, the body-diode of S_1 or S_2 provides the freewheeling path of the inductor current. Thus, if the Si SJ MOSFETs are utilized for S_1 and S_2, the totem-pole PFC cannot work at hard-switching mode due to the extremely severe reverse recovery issue of the Si SJ MOSFETs as clearly shown in TABLE I. Therefore, with Si SJ MOSFETs, the totem-pole PFC has to operate in soft-switching mode, such as the critical conduction mode (CRM) or the quasi-square-wave (QSW) mode [24]. However, with Si SJ MOSFETs, even a single hard switching event would possibly destroy the device due to the large reverse recovery energy and voltage over-shoot. Hence ensuring the soft-switching in Si based totem-pole is needed and this drives up the cost and system control complexity. Thus, even though the totem-pole bridgeless PFC has been proposed for more than twenty years, it does not receive much attention until the emerging of the 600 V GaN devices.

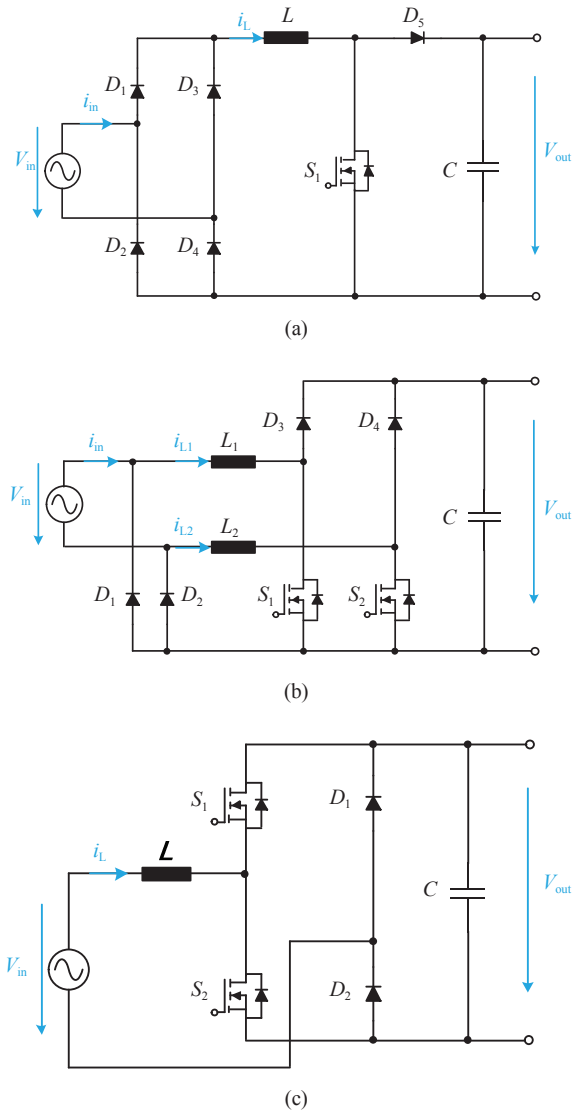


Fig. 2. (a) conventional Boost PFC; (b) semi-bridgeless dual-Boost PFC; (c) conventional totem-pole bridgeless PFC.

As discussed in the previous section, the 600 V GaN FETs not only eliminate the reverse recovery issue, but also achieves low switching loss. Thus, the GaN totem-pole bridgeless PFC, as shown in Fig. 3, draws tremendous interests from industry and academia. Compared with the conventional totem-pole bridgeless PFC, Si SJ MOSFETs are replaced by GaN FETs for S_1 and S_2. Since there is no reverse recovery issue, the GaN totem-pole can work at either hard-switching or soft-switching mode. For soft-switching mode, even if several switching cycles lose the soft-switching, the GaN FETs would not be destroyed. Hence the reliability of the soft-switching GaN converter is still high. In addition, the two low frequency diodes are further replaced by two line-frequency Si SJ MOSFETs to take advantage of their low condition loss once they are turned on. As shown in Fig. 4, during the positive half line cycle, S_4 is reversely conducting the AC grid current since the neutral point is connected to the negative terminal of the DC side. During the negative half line cycle, S_3 is reversely conducting the grid current by connecting the grid neutral point to the positive terminal of the DC side. Thus, there are no diodes in the line current

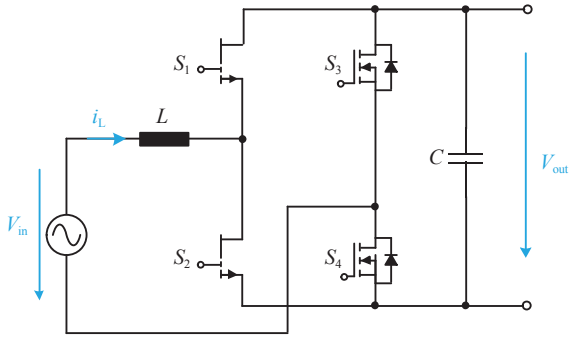


Fig. 3. GaN totem-pole bridgeless PFC.

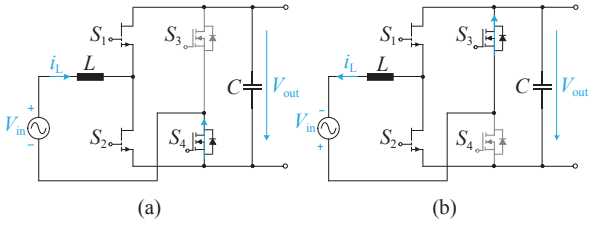


Fig. 4. Equivalent circuit during (a) positive half line cycle, and (b) negative half line cycle.

path. The GaN totem-pole PFC therefore could realize the lowest conduction loss compared with the conventional Boost PFC, the semi-bridgeless dual-Boost PFC and the conventional totem-pole PFC. Moreover, since the inductor and the GaN FETs are fully utilized in both positive and negative half line cycles, the power density also can be improved.

IV. Hard-Switching Totem-Pole PFC

The hard-switching totem-pole PFC utilizes the constant frequency pulse width modulation (PWM). Thus, hardware design and controller development for the hard-switching totem-pole PFC is as simple as those for the hard-switching conventional Boost PFC.

A. Control

With constant frequency CCM operation, the inductor current for the positive half line cycle is shown in Fig. 5.

The simplified control diagram is shown in Fig. 6 [7], [27]. The outer loop is the low-bandwidth DC voltage loop. The output of the voltage controller is the amplitude of the current reference. The inductor current is sensed and filtered. The output of the current controller is the duty-cycle. Then, the constant frequency PWM and the AC voltage polarity together determine the gating signals of G_1 and G_2. The gating signals of G_3 and G_4 are only determined by the AC voltage polarity.

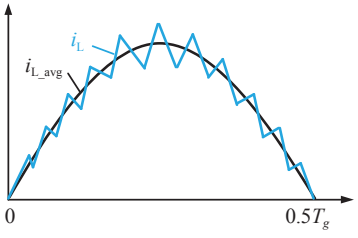


Fig. 5. Inductor current waveforms of hard-swicthing GaN totem-pole PFC.

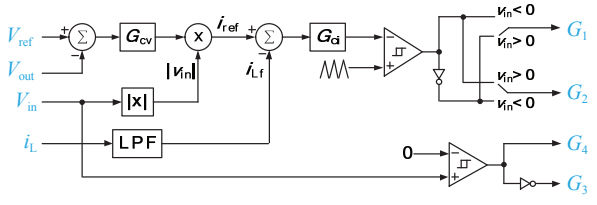


Fig. 6. Control diagram of hard-switching GaN based totem-pole PFC.

B. Frequency and Magnetic

Even though the turn on losses of the GaN FETs are much lower than those of the Si SJ MOSFETs, the turn on loss is still one of the dominated parts in the total power loss of the hard-switching totem-pole PFC. To achieve 99% efficiency, the switching frequency must be kept low such as 100 kHz which is very similar to the frequency of the hard-switching Boost PFC. Thus, the sizes of the switching frequency related passive components, including the EMI filters and the main inductors, are not improved. The total power density of the hard-switching GaN totem-pole PFC is still limited, even if the efficiency can be up to 99%.

An inductor for a 3 kW 100 kHz hard-switching GaN totem-pole PFC is shown in Fig. 7. The size is 50x40x51 mm^3. Actually, the CCM GaN totem-pole PFC can use the same inductors as the CCM Boost PFC under the same power and frequency conditions.

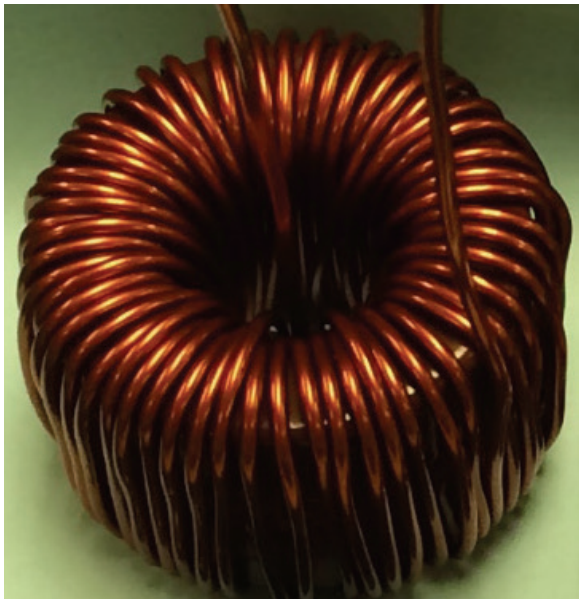


Fig. 7. An inducor (size: 50x40x51 mm^3) for a 3 kW 100 kHz hard-switching GaN totem-pole PFC.

C. Efficiency and Density

Two examples of the hard-switching GaN totem-pole PFC are shown in Fig. 8 [29], [27]. Both of them are working at about 65 kHz, and have 99% peak efficiency. A detailed com-parison of the hard-switching PFC is listed in TABLE II. Compared with the-state-of-the-art Boost PFC and the Semi-bridgeless PFC, GaN totem-pole PFC has higher efficiency. However, since the frequency is not increased, the hard-switching GaN totem-pole PFC does not improve the power density. The state-of-art CCM GaN totem-pole PFC prototypes only achieve lower than 70 W/inch^3 power density [27]-[29].

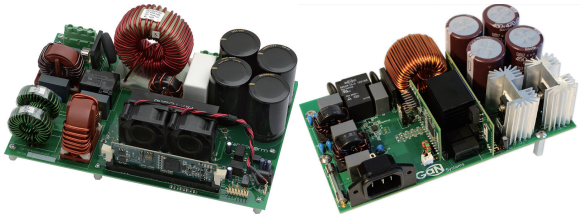


Fig. 8. Examples of hard-switching GaN totem-pole PFC: (a) Transphorm 4 kW, 66 kHz [29]; (b) GaN Systems 3 kW, 65 kHz [27].

TABLE II
COMPARISON OF HARD-SWITCHING PFC

Topology	Company	Power (kW)	Switching Frequency (kHz)	Efficiency of half load (%)	Efficiency of full load (%)	Power Density (W/inch^3)
Boost PFC	ST [4]	3	111 (3 channels)	98.7	98.5	52
Semi-briddge-less PFC	Infineon [30]	3	90	98.6	98.2	<70
	Infineon [28]	2.5	65	99.1	98.6	<70
GaN totem-pole PFC	GaN Systems [27]	3	65	99	98.7	<70
	Transphorm [29]	4	66	99	98.5	<70

V. SOFT SWITCHING TOTEM-POLE PFC

As discussed previously, increasing the switching frequency is the most straightforward way to improve the power density of the totem-pole PFC. However, the switching loss is still a big barrier. Since the turn off losses of GaN devices are less than one tenth of the turn on losses, zero-voltage-switching is potentially a great way to increase the switching frequency and keep a high efficiency. The turn-off loss can approach zero if hard-driven gate is utilized [1], [5], [6], [9].

A. Dual-Mode Soft-Switching Operation

For conventional Boost PFC, critical conduction mode (CRM) can be used to achieve ZVS soft-switching [31], [32]. How-ever, when the input voltage is lower than half of the output voltage, only partial ZVS can be achieved [32]. For totem-pole PFC, since there are two high-frequency switches in one half bridge, quasi-square-wave (QSW) mode can be utilized to achieve fully ZVS under any voltage ratios [8], [33]-[35]. Thus, a dual-mode soft-switching operation is proposed in [33]-[35].

As shown in Fig. 9, there are two operation modes during one half line cycle. When the input voltage is lower than half of the output voltage, the converter operates in CRM. In CRM, the SR GaN FET is turned off when the inductor current becomes zero. The drain to source voltage of the active GaN FET is resonant from V_{out} to zero. Thus, ZVS can be realized. When the input voltage is higher than half of the output voltage, the converter operates in QSW mode. In QSW mode, the SR GaN FET is turned off when the inductor goes down across zero and to the required negative current. The negative inductor current provides additional energy to help discharge the output capacitances (C_{oss}) of the GaN FETs and the parasitic capacitance of the inductor.

In CRM, the SR turn off current i_{SR_off} is zero. In QSW mode, the required SR turn off current i_{SR_off} decreases with the increasing of vin. i_{SR_off} can be calculated by the sensed signals (v_{in} and V_{out}) and the circuit's parameters (L and C_{oss}) [33]-[35]. This dual-mode soft-switching operation not only achieves full-range ZVS, but also minimizes the conduction loss under full-range ZVS.

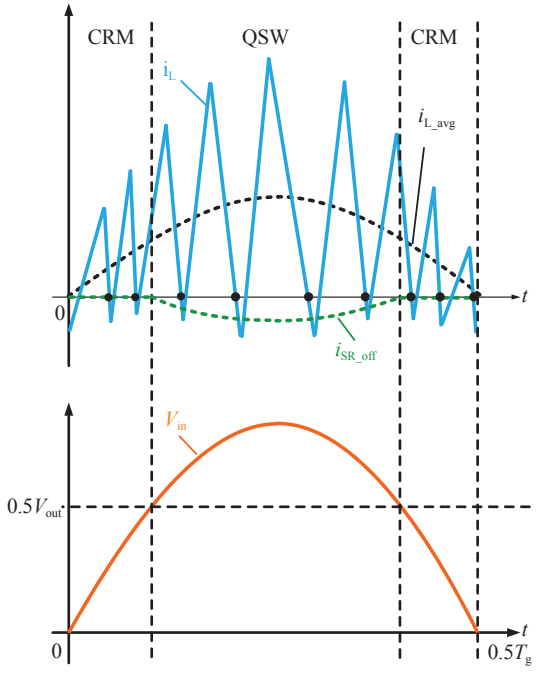


Fig. 9. Inductor current waveforms of soft-swicthing GaN totem-pole PFC.

B. Control

Two control methods can be used for the soft-switching totem-pole PFC. One is the hysteresis current control [36]. Upper and lower current reference bands determine the on/off of the switches. However, high-speed and isolated inductor current sensing is very challenging. Another control method is the on-time control as shown in Fig. 10 [33]-[35]. A zero-crossing-detection (ZCD) is needed to generate the ZCD signal. With the

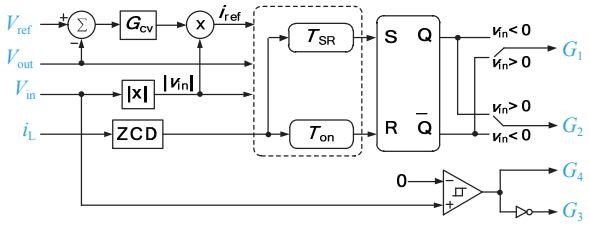


Fig. 10. Control diagram of soft-switching GaN based totem-pole PFC.

ZCD signal, gating signals are determined by the calculated active-GaN-FET on time and SR-GaN-FET on time.

The conventional ZCD method uses the current shunt, the high-speed comparator and the digital isolator to generate and transfer the ZCD signal [33]. However, this method not only causes additional loss on the current shunt, but is also sensitive to the noise. Paper [37] proposes an advanced method which uses the saturated inductor and the comparator to generate the ZCD signal. This method not only reduces the loss and cost, but also improves the noise-sensitivity.

C. Frequency Range and Magnetics

The frequency variation for the dual-mode soft-switching totem-pole PFC is shown in Fig. 11. Due to the need to achieve the ZVS, the frequency is varying and can be much higher than the hard-switching totem-pole PFC. The frequency can be from several hundred kHz to several MHz [33]-[35].

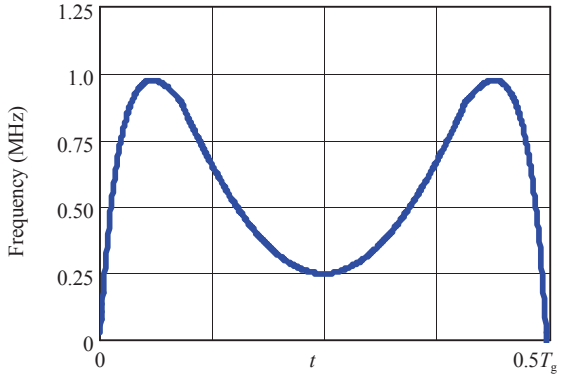


Fig. 11. Switching frequency variation under the conditions: P_{out}=1.6 kW, v_{in}=240 VAC, V_{out}=400 V, L=9.5 μH.

The high frequency inductor design is a challenge for soft switching totem pole PFC. Four high frequency ferrite materials are compared under 100 °C and 1 MHz as shown in Fig. 12 [38]-[41]. The four materials are 3F45 of FERROX-CUBE, N49 of TDK, P61 of ACME, ML91S of HITACHI. The core loss data under sinusoidal excitation without DC bias obtained from the datasheets are shown in Fig. 12(a). However, in totem-pole PFC, the inductors are usually under rectangular excitations. The core loss data under rectangular excitations without DC bias, which can be obtained by testing [42], [43] or calculations [44], are shown in Fig. 12(b). By comparing Fig. 12(a) and (b), significant difference is observed. For the same material, the core loss under rectangular excitation is much higher than the core loss under sinusoidal excitation. In addition, under sinusoidal excitation, the core loss of P61 is similar to that of ML91S. However, under rectangular excitation, the core loss of ML91S is much less than that of P61. In general, ML91S from HITACHI is the best among the four materials.

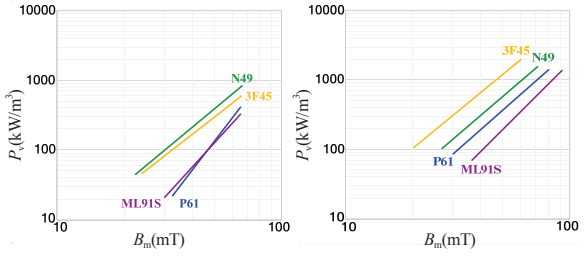


Fig. 12. Core loss of four materials under 100 °C and 1 MHz: (a) sinusodial excitation without DC bias; (b) rectangular excitation without DC bias [38]-[41].

The ferrite core shapes are also critical for the high-efficiency and high-density inductor design. Based on the data in Fig. 12, the core loss significantly increases as the flux density swing ΔB increases. ΔB is formulated as

$$\Delta B = \frac{E\Delta t}{NA_e} \tag{1}$$

where $E\Delta t$ is the voltage-second of the inductor, N is the number of turns, and A_e is the effective area. Thus, increasing N or A_e can reduce ΔB. However, increasing N will significantly increase the winding loss. This is not only caused by the need for more windings, but also by the increasing of the gap length which leads to the fringing effect. The calculation of the gap length l_g is derived as

$$l_g = \mu_0 N^2 \frac{A_e}{L} \tag{2}$$

where μ_0 is the permeability of the air. l_g is proportional to N^2 and A_e. Thus, increasing A_e is better than increasing N. Several commercial low-profile cores are recommended in TABLE III. This paper introduces a new index V_e/A_e to evaluate the performance of the core shapes for the high frequency inductor design. As long as the window area is enough for the windings, smaller V_e/A_e is more efficient than larger V_e/A_e.

TABLE III
RECOMMENDED CORE SHAPES FOR SOFT-SWITCHING TOTEM-POLE PFC

	Core Shape	A_e(mm^2)	V_e(mm^3)	V_e/A_e(mm)
EE	E32/6/20	130	5380	41.4
	E22/6/16	78.3	2550	32.6
	E18/4/10	39.3	960	24.4
ER	ER32/6/25	141	5400	38.3
	ER23/3.6/13	50.2	1340	26.7
EQ	EQ30	108	4970	46.1
	EQ25/LP	89.7	2370	26.4

D. Multi-Phase Interleaving and the Control

For the soft-switching totem-pole PFC, the high current ripple causes challenges for the design of the input filter. Multi-phase interleaving is a possible solution. Fig. 13 shows an example of

the comparison of the current ripple without dual-phase interleaving and the current ripple with dual-phase inter-leaving. The input current ripple is significantly reduced with the interleaving.

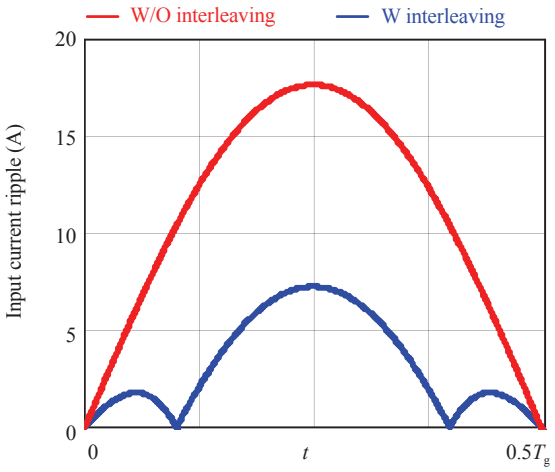


Fig. 13. Comparison of the input current ripples: V_{in}=240 VAC, V_{out}=400 V, P_o=1.6 kW.

However, the multiphase interleaving PFC introduces an additional challenge in control because the control is a variable frequency one. Two kinds of control methods for the multi-phase CRM Boost PFC have been utilized to address this issue.

The first method is the open-loop methods [45], [46]. Using the open loop control methods, there is a master phase, and the other phases are slave phases. The master phase is controlled like a one-phase PFC. The slave phases' turn on or turn off instants are synchronized to the turn on or turn off instant of the master phase with a phase delay. The delay time is generated based on the detection of the master phase's switch-ing frequency. Then, the slave phases turn off or turn on instants are self-controlled like a one-phase PFC. The open loop methods are easy for implementation. However, the slave phases' soft-switching or current control could be lost during the transient.

The other kind of method is the closed-loop method [34], [35], [46], [47]. In the closed-loop method, the multiple phases are controlled with soft-switching. At the same time, an additional feedback control adjusts the interleaved phases between the multiple phases. The closed-loop method requires high speed calculation if the frequency is in the MHz range. Otherwise, the delay of the phase-interleaving feedback contro-ller would cause the oscillations of the currents [46]. On the contrary, the open loop methods do not have this risk even if using lower speed digital processor [46].

In general, for high frequency multiphase GaN totem-pole PFC, the open loop interleaving methods are better than the closed-loop interleaving methods [46].

E. Efficiency and Density

As a proof of concept development, a 3.2 kW GaN dual-phase soft-switching totem-pole PFC is developed and tested. The picture of the prototype is shown in Fig. 14. The size is 7.9x1.8x1.8 inch^3. The power density achieved is 130 W/inch^3. The frequency distribution under full load condition is shown in Fig. 11. The maximum frequency under full load is 900 kHz.

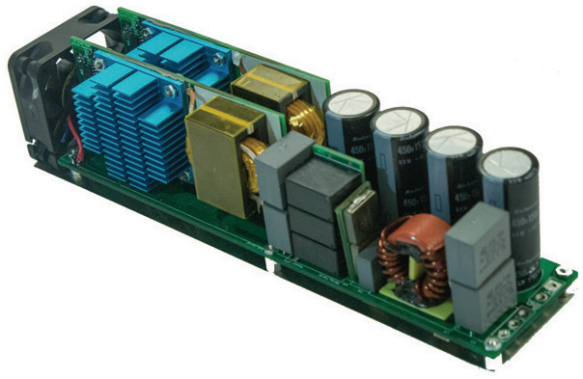
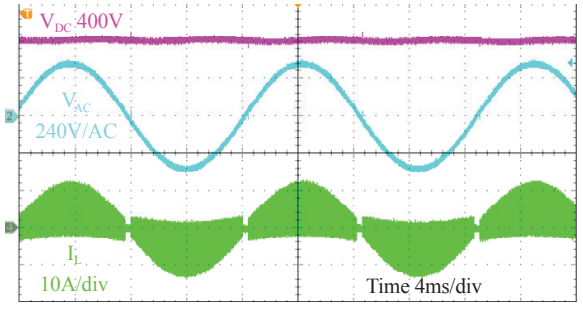
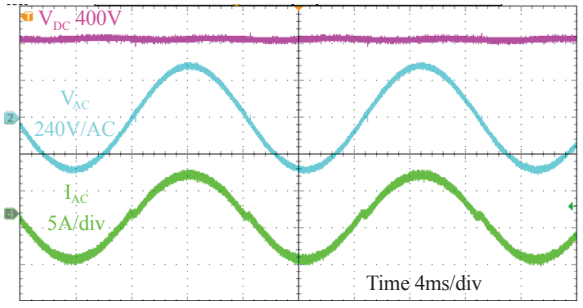


Fig. 14. Protype of a 3.2 kW GaN dual-phase soft-switching totem-pole PFC.

The testing waveforms for one phase are shown in Fig. 15. During the zero-crossing time of the AC voltage, the voltage second of the inductor is almost zero. The inductor current is easily distorted during the zero-crossing time. Since this issue also exists in the conventional Boost PFC, all existing solutions [48]-[51] to this issue for conventional Boost PFC can be used for the totem-pole PFC. All previous methods focus on improving the current dynamic response. Hence more complexities are introduced in the control. Another simple and effective method is to add a 20~40μs blanking time for all gating signals during



(a)



(b)

Fig. 15. Testing waveforms for one phase soft-switching totem-pole PFC under the conditions: v_{in}=240 VAC, V_{out}=400 V, P_o=1.6 kW, L=9.5 μH.

TABLE IV
COMPARISON OF SOFT-SWITCHING PFC

Topology	Company/Institution	Power (kW)	Frequency Range (kHz)	Efficiency of half load (%)	Efficiency of full load (%)	Power Density (W/inch^3)
2 Phase CRM Si-based Boost PFC	Ilmenau University of Technolog [52]	1	50-500	97.5	97.5	<50
2 Phase ZVS GaN Totem-pole PFC	CPES [1]	1.2	1000-2500	99	98.8	700 (without bulky cap, controller, fan)
	Author's group	3.2	250-900	99.05	99	130

the AC voltage zero crossing time. During the blanking time, all the gating signals are zero. This method still introduces some small current distortion, however the THD standards still can be satisfied. As shown in Fig. 15(b), the AC current is clamped to zero during the zero-crossing time using the blanking method.

The efficiency curve for one phase of the prototype is shown in Fig. 16. The efficiency is over 99% from half load to full load. The comparison of the soft-switching PFCs is shown in TABLE IV. The dual-phase interleaving ZVS GaN totem-pole PFCs show superior performance compared with the CRM Boost PFC.

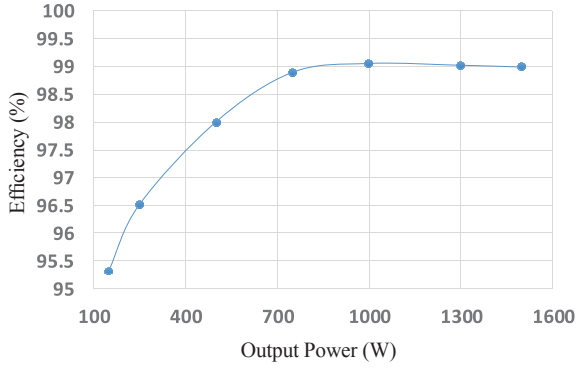


Fig. 16. Efficiency curve of one phase of the prototype under the conditions: v_{in}=240 VAC, V_{out}=400 V, L=9.5 μH.

VI. CONCLUSIONS

In this paper, the technologies, control and performances of the GaN totem-pole PFC are reviewed. Several conclusion remarks can be made. First, the currently available 600 V GaN devices have shown superior perfor-mances compared with the Si SJ MOSFETs, especially the zero reverse-recovery loss in the enhancement-mode GaN FETs. By eliminating the reverse recovery issue, the GaN totem-pole true-bridgeless PFC is poised to be the next generation PFC solution with ultra-high efficiency and high power density. It can work under CCM hard-switching mode with over 99% efficiency. However, the limited switching frequency of hard-switching GaN totem-pole PFC does not improve the power density compared with the CCM Si Boost PFC and clearly shown in Fig. 17. The ZVS GaN totem-pole PFC can push the switching frequency well above MHz level while maintaining 99% efficiency. A 3.2 kW MHz 99% efficient ZVS GaN totem-pole PFC developed by the author's group achieves an amazing 130 W/inch^3 power density, which is more than two times of the power density of the best CCM GaN totem-pole PFC. In addition, this paper also points out that the hardware design and the control of the CCM GaN totem-pole PFC are similar to those of the Boost PFC. The soft-switching totem-pole PFC can achieve full input-and output-voltage range ZVS using the dual-mode ZVS control. The multiphase inter-leaving technique significantly reduces the input current ripple and is well suited for higher power PFCs. The high frequency ferrite materials and core shapes are also reviewed and recommended.

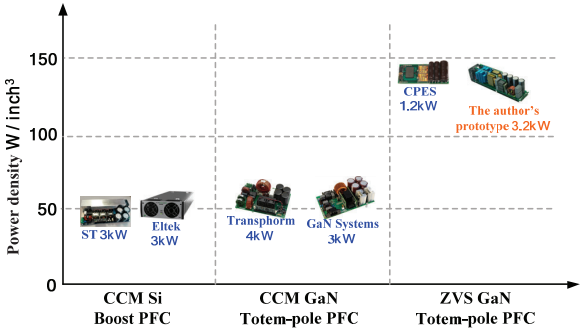


Fig. 17. Comparison of the power density.

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Qingyun Huang received the B.Sc. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2010, and the M.Sc degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2013. From 2013 to 2017, he was a PhD research assistant student in FREEDM Systems center, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC. He is currently working toward the Ph.D. degree in Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas.

His current research interests include topology and design of high power density power converters, application of Wide-band-gap devices, and digital control of power electronics.

Alex Q. Huang was born in Zunyi, Guizhou, China. He received his B.Sc. degree from Zheijiang University, China in 1983 and his M.Sc. degree from Chengdu Institute of Radio Engineering, China in 1986, both in electrical engineering. He received his Ph.D. from Cambridge University, UK in 1992. From 1992 to 1994, he was a research fellow at Magdalene College, Cambridge. From 1994 to 2004, he was a professor at the Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, Virginia. From 2004 to 2017, he was the Progress Energy Distinguished Professor of Electrical and Computer Engineering at NC State University where he established and led the NSF FREEDM Systems Center. Since September 2017, he has become the Dula D. Cockrell Centennial Chair in Engineering at University of Texas at Austin.

Since 1983, he has been involved in the development of modern power semiconductor devices and power integrated circuits. He fabricated the first IGBT power device in China in 1985. He is the inventor and key developer of the emitter turn-off (ETO) thyristor. He developed the concept of Energy Internet and the smart transformer based Energy Router technology. His current research interests are power electronics, power management microsystems and power semiconductor devices. He has mentored and graduated more than 80 Ph.D. and master students, and has published more than 500 papers in international conferences and journals. He has also been granted more than twenty U.S. patents. He is the recipient of the NSF CAREER award, the prestigious R & D 100 Award and the MIT Technology Review's 2011 Technology of the Year award.