Review of State-of-the-Art Integration Technologies in Power Electronic Systems
Kangping Wang, Zhiyuan Qi, Fei Li, Laili Wang, and Xu Yang

Abstract—As an important development direction of power electronic systems, the integration technologies can bring many benefits, such as size reduction, reliability improvement, cost saving and so on. With the continuous development of power semiconductor devices, especially the emergence of wide band-gap devices, more advanced integration technologies are needed. This paper reviews the state-of-art integration technologies, including active and passive integration technologies. Active integration technology is reviewed in terms of the interconnect, packaging material, packaging structure, and module integration. Passive integration technology is reviewed from the aspects of magnetic integration technology, electromagnetic integration technology, and low-temperature cofired ceramic (LTCC) technology. Higher-level integration technologies, namely power supply on chip (PwrSoC) and power supply in package (PwrSiP), are also investigated, which are mainly used in low power applications.

Index Terms—Active integration, power electronic integration technology, passive integration, power module, wide band-gap device.

I. INTRODUCTION

POWER electronics integration is a technology that integrates multiple power electronic components into a single module, which can offer many benefits such as size reduction, costs saving, and reliability improvement. In recent years, the power electronics integration technology has attracted more and more attentions, especially with the emergence of wide bandgap devices. According to device characteristics and manufacturing process, the power electronic integration technologies can be mainly classified into active integration technology and passive integration technology.

The integration of active components into a module, i.e. active integration technology, can realize low parasitics, good thermal performance, high reliability, etc. In most of available commercial power modules, the interconnections are realized by wire-bonding technology [1]-[5], shown in Fig. 1. However, this traditional packaging structure is not suitable for wide band-gap (WBG) devices which can operate at much higher frequency and temperature than Si devices [6]-[8].

This is because wire-bonding structure has large parasitic inductance (usually more than 10 nH) and limited heat dissipation capability [5], [9]. Besides, the lead-solder in die attachment has some drawbacks, such as low thermal conductivity, low melting point, and contamination to environment [10]-[12]. So advanced active packaging technologies involving wirebond-less interconnection technology [5], [13]-[21], advanced packaging materials [10], [22]-[26], advanced packaging structures [27]-[34] and module integration technologies [35], [36] are required to be developed.

The passive components, namely inductors, capacitors and transformers, generally occupy a large space of the total volume, which is harmful to the miniaturization of power converters. The passive integration technology, which is to integrate multiple passive components into a single module, has considerably advantages, such as size reduction and cost saving. The magnetic integration is to integrate the inductors and transformers into a single core, which has been successfully applied in some topologies, such as Cuk converter [38], forward converter [39], current-doubler rectifier [40], multiphase converter [41] and LLC converter [42], [43]. The integration of the capacitors and the magnetic components, namely the electromagnetic integration, can further reduce the number and size of the passive components. It has been implemented into LLC converters and asymmetrical half bridge circuit with current-doubler rectifier [44]. Moreover, the integration of all the components of a converter, including passive components, switches, drivers, and controllers, as a module or chip, can achieve greater improvement. Two typical examples are power supply on chip (PwrSoC) and power supply in package (PwrSiP). In recent years, the low-temperature cofired ceramic (LTCC) magnets have gained much attentions in the 3D integration modules due to its low profile and flexible structure.

In order to break through the bottleneck of integration technologies for further improving the performance of power
converters [45], this paper provides a review of the integration technologies from the aspects of active packaging integration and passive integration. Section II reviews the active integration technologies, including interconnection technology, packaging material technology, packaging structure technology, and module integration technology. Section III reviews the passive integration technologies, including the magnetic integration technology, electromagnetic integration technology, PwrSoC and PwrSiP technology, and LTCC integration technology. Section IV concludes the paper.

II. Active Integration Technologies

The integration of active devices can reduce the interconnection parasitic inductance, improve the thermal dissipation capability, reduce the cost, etc. The emergence of wide bandgap devices, such as SiC and GaN, puts higher demands on the active integration. This section will review the active integration technologies from the aspects of interconnection technology, packaging materials, advanced packaging structures, and module-level integration.

A. Interconnection Technology

The interconnection technology is to realize the connection of die to die, and die to external terminals or circuits, which is an indispensable part of packaging technology. The traditional interconnection is based on wire-bonding technology, which has large parasitic inductance, limited heat-dissipation capability and low reliability, etc. Advanced interconnection technologies, including improved wire-bonding interconnections and wirebond-less interconnections, have been developed.

1) Improved Wire-Bonding Interconnection

To utilize the advantages (such as easy realization and low cost) of conventional wire-bonding technology, advanced wire-bonding technology has been developed. In Fig. 2(a), by employing a 3D lead-frame structure, the symmetrical Kelvin Source connection for each switching device was enhanced, which can realize reduced parasitic inductance [46]. In [47], a “double-ended-sourced” busbar structure in the multi-chip module was used to realize symmetrical power loop, thus the circulating current was reduced and dynamic current was balanced, shown in Fig. 2(b). However, the power loop in these improved wirebond-less structures are still a lateral structure. In [48]-[50], a hybrid packaging structure with multilayer substrates are utilized to realize the vertical power loop with small parasitics.

2) Wirebond-Less Interconnection

So far, several wirebond-less technologies have been put forward, including flip-chip technology, dimple array interconnection technology, embedded packaging technology, metal-post interconnection technology, etc.

a) Flip-Chip Technology

At the beginning, the flip-chip technology was widely used in the field of microelectronics integration, due to its low-cost, high density, and reliable interconnections [5]. This technology eliminates the wire-bonds by utilizing solder joints for interconnecting devices. Compared to conventional wire bonding package structure, flip-chip structure has reduced parasitics and improved reliability. Owing to these benefits, it is extended to power electronics applications. A flip-chip on flex (FCOF) integrated power electronics module (see Fig. 3) was proposed by John G. Bai, et al. in 2003 [19]. In the module, the power chips are flip-soldered on a double-sided flexible copper-clad laminate. For better thermal performance, the power chips are also soldered onto a patterned direct bond copper (DBC) substrate. Between the flex substrate and DBC substrate, an organic underfill material is filled to achieve encapsulation, which can help to reduce thermal stress and improve heat dissipation. However, this technology cannot carry large current and is not suitable for vertical power devices. This technology is expected to be used in lateral GaN modules.

b) Dimple Array Interconnection Technology

With the purpose of enhancing thermal reliability of the solder bump, Simon S. Wen developed the dimple array interconnect (DAI) technique in 2001 [14], [18], [20]. As shown in Fig. 4, the copper flex with pre-formed dimples are used to replace wire bonds as electrical interconnections. The dimpled metal interconnects enable easy forming of solder joints with the underlying devices. Smooth fillets in solder bumps can be formed to significantly reduce the thermal stresses and strains.

The solder joint always forms an hourglass-shape in the DAI processing, which suffers a very small inelastic strain during thermal cycling. Furthermore, DAI provides better thermal management, due to its simpler thermal interfaces, shorter heat dissipation path through the interconnects [14]. However, it requires a special equipment to produce and install the
copper sheet with dimple array.

c) Embedded Packaging Technology

Fig. 5 shows the conceptual embedded power packaging structure. In the structure, the embedded power devices are mounted in the openings etched out of the ceramic frame, and surrounded by an adhesive polymer. After a dielectric layer is coated on the upper surface of ceramic and power chips, via hole through the dielectric is formed on the die pad. And then the interconnections are realized by metallization on surface of the insulation layer [5], [13], [15]-[17]. The base substrate provides electrical interconnection and thermal dissipation path of power chips. This structure can realize reduced parasitics, improved power density, and low mechanical stress.

d) Metal-Post Interconnection Technology

The metal posts interconnected parallel plate structure (MPIPPS) was proposed to achieve interconnections by metal posts in [16], [18]. As shown in Fig. 6, the power chips are sandwiched between two substrates. The bottom of device is attached to the bottom plate by conventional solder die-attach processes, whereas the topside’s connection to the top plane is realized through an array of metal posts. Through elimination of the wire-bonds, this technology can reduce the parasitic inductance of the interconnections.

Furthermore, MPIPPS can improve the heat dissipation capability of package due to the two directional heat transfer paths through the substrate and metal post. In addition, active heat dissipation can be implemented by filling the solid or liquid insulating thermal conductive materials in the space between parallel plates and the metal posts. In [21], the experimental results show that the maximum junction temperature of the IGBT chips in the MPIPPS module is 17 °C lower than that in wire-bonding module.

B. Packaging Material Technology

The state-of-the-art commercial power devices only can operate up to 175 °C, which is mainly limited by packaging materials besides packaging structure. To enable WBG devices operating at high temperatures (200–350 °C), advanced packaging materials are required to provide compatible CTE with WBG chips, and reliable high temperature performance [37]. It is essential to conduct a review of the packaging materials, which mainly include substrate materials, die-attaching materials, and encapsulation materials.

1) Substrate Materials

The substrate provides cooling, interconnection, and mechanical support for the power modules. The commonly used substrates are DBC ceramic substrate and insulating metal substrate (IMS).

In DBC ceramic substrates, Al₂O₃, AlN, BeO and Si₃N₄ can be used as the insulating materials [51]. Though BeO has the highest thermal conductive performance, it is not commonly used because the particle generated during the processing is harmful to human health. The Si₃N₄ material is also not commonly used for its low thermal conductivity and high material cost. Because the strong adhesion of substrate and copper can be easily achieved, Al₂O₃ is the most commonly used insulating materials. Compared with Al₂O₃, AlN has much higher thermal conductivity and closer CTE to SiC, but the AlN DBC substrate is costlier due to more complicated manufacturing process. With the development of manufacturing technique, AlN has the potential to replace Al₂O₃.

Generally, IMS consists of a highly thermal-conductive insulating resin sheet, a copper baseplate and thick copper foils, which can achieve good heat dissipation, and is cheaper than DBC due to the relatively simpler fabrications. IMS has been successfully applied to Mitsubishi IGBT module [37]. The life time of the module in thermal cycling has been enhanced by optimizing IMB insulating material and thickness, and a 23% increment of the effective chip-contacting area has been achieved.

2) Advanced Die-Attaching Materials

Soft solder is the most commonly used packaging material in power electronics. But its low thermal conductivity and melting point limits the power devices to operate up to 175 °C, which cannot fully exploit high temperature advantage of the WBG devices. Moreover, the lead solder is harmful to human’s health and the environment, so the lead-free die-attaching materials are preferred. The nano silver sintering and transient liquid phase bonding (TLPB) are two promising alternatives.
a) Nano Silver Sintering

Nano silver sintering is a low temperature joining technique (LTJT). Due to the size effect, the melting point of silver particles in nano and micro scale is far below that of silver bulk [10], [23]-[26]. By applying a certain pressure and temperature of above 220 °C, silver particles will be melted and sintered spontaneously under the effect of liquid phase capillary force. The sintered silver has high thermal conductivity (250 W/mK), high electrical conductivity (41 MS/m) and high melting point (close to 961 °C). It has demonstrated good mechanical characteristics with a CTE value of 19 μm/mK and a tensile strength of 55 MPa. So far, silver sintering has been applied to industrial manufacturing for a range of selected products. But it is not a versatile approach for mass manufacturing mainly due to the quality issues and failures in silver-sintered contact interfaces. This sintering technique needs to be further improved.

b) Transient Liquid Phase Bonding

TLPB uses the diffusion between a high melting point and a low melting point material [19]. Many materials such as Ag/In, Ag/Sn, Au/In, Au/Sn, Cu/Sn, and Ni/Sn can be used as the soft solder with lower melting point. In the process of TLPB, the first step is to melt the low melting point material to form intermetallic phase (IMP) between the liquid and solid phase. Then after all the liquid phase transformed to IMP, a recommended maximum pressure of 0.3 MPa is required to contact the substrates while avoiding squeezing out of the liquid phase. The solid bond shows a higher remelting temperature than the initial process temperature. It has been reported that the IMC ε-phase Ag₃Sn has a melting temperature of 480 °C and the ζ-phase Ag₅Sn with a melting temperature of up to 724 °C, which are much higher than that of pure Sn with 232 °C.

3) Encapsulation Materials

Encapsulation provides protection for power module against mechanical stress, electrical breakdown, chemical erosions, α radiations, and so on. However, conventional encapsulations are only suitable for applications below 175 °C. To achieve higher operating temperature, the new encapsulation materials should have the characteristics, e.g. high thermal conductivity, close CTE to semiconductor materials, high dielectric strength, etc. Several encapsulants are reported to be able to operate above 250 °C. However, some of their properties may degrade when the temperature is close to 250 °C [52], [53]. As for underfills and molding compounds, their low glass-transition temperature (Tg) limits the high temperature operation, so appropriate modification of the chemical composition is required to achieve higher Tg. High-Tg polymers, such as polyimide, bismaleimide, and cyanate ester, are potential encapsulants for high-temperature (>250 °C) operation. However, the internal stress caused by mismatching CTE with semiconductors needs to be limited. Potting compounds limited by their thermal decomposition also need appropriate modification to improve thermal stability [11].

C. Advanced Packaging Structures

In traditional power modules, a 2D layout structure is employed, in which the heat is transferred in one direction and the parasitic inductance of the interconnections are large. The more advanced structures, including 2.5D structures and 3D structures which can achieve double-sided cooling and smaller parasitic inductance, are preferred for high power density applications.

In the 2.5D structures, there are usually two substrates, one of which is for the attachment of power chips and heat sink, and the other is for interconnection [30]. In addition, copper pin, metal post or shim material is required to match the height difference between MOSFET/IGBT and diode dies [37]. The most representative packaging technology is the planar-bond-all technology which features three-dimensional planar electrical interconnection and double-sided cooling [29], [31], [32], shown in Fig. 7. The advanced packaging structure can achieve 75% reduction in parasitic inductance and 40% reduction in thermal resistance. Another typical 2.5D packaging structure is Semikron’s all-sintered SKiN® package [27], [28], shown in Fig. 8. All solder and bond wire contacts are eliminated by using silver diffusion sintering joints, and the flex foil is firstly introduced for interconnections. In this structure, the parasitic inductance can be reduced up to 10%.

The 3D packaging structure is a novel concept based on stacking power dies [30], which can achieve ultra-low parasitics, compact package and excellent thermal performance. The chip-on-chip (CoC) structure proposed by Nottingham is a representative 3D structure [33], in which two power chips are vertically stacked and connected through vias,
D. Module-Level Integration

Integrating the power chips with some associate components into a module can bring many benefits, such as reduced parasitics, improved thermal conductivity. The associate components which can be integrated into the module include the decoupling capacitors, gate drivers, temperature sensors, current sensors, protection circuits, etc.

The integration of decoupling capacitor is to reduce the power loop inductance by eliminating the parasitic inductance between the connection of module to external circuit. The module integrated with the decoupling capacitor shown in Fig. 11, achieves over 60% reduction of power loop parasitic inductance (just 1.63 nH) compared with the baseline module [36] in Fig. 10. The method of integrating decoupling capacitor to reduce power loop inductance was also demonstrated in [54]. Furthermore, the integration of double sided fin-pin heatsinks in Fig.

III. Passive Integration Technologies

Passive devices, especially magnetic components, often occupy a considerable volume, and become one of the main bottlenecks to improve the power density of the converters. Integrating multiple passive components can reduce their number, size and cost. This section will review some passive integration technologies, including magnetic integration technology, electromagnetic integration technology, Pwr-
SOC and PwrSiP technology, and LTCC integration technology.

### A. Magnetic Integration Technology

The magnetic components, namely inductors and transformers, occupy a considerable space of the total volume, which have harmful effects to the power density. To solve this problem, the magnetics are integrated into one core. There are many converters have applied the magnetic integration technology. For example, Cuk converter and forward converter are integrated into a single core by Slobodan. Cuk [38] and G. D. Bloom [39], [58], [59], respectively. An improvement of forward converter is made in [60]. The three magnetic components of the current-doubler rectifier (CDR) are integrated into single integrated component [61], shown in Fig. 13(a). To minimize the termination loss, the windings are integrated [62], shown in Fig. 13(b). An improvement is made by [63] [64]. The windings at the center leg are split into the two outer legs, resulting in increasing in coupling coefficient of primary and secondary, shown in Fig. 13(c). The filtering inductance in aforementioned topology has a limited value. A new design with increasing filter inductance is proposed in [65], shown in Fig. 13(d). But the increasing of the secondary windings that conduct large current, induces large winding losses. Thus, a trade-off between filter inductance and winding losses should be made. Some topologies have already implemented the integrated CDR to increase power density and reduce power losses [66], [67].

Another typical application of magnetic integration is for multiphase converter of which the inductors are integrated into one magnets. The integrated inductors [68] can be divided into noncoupled inductors [69] and coupled inductors [70]. The integrated inverse coupled inductors can not only reduce current ripple by increasing steady state inductance, but also increase transient respond by decreasing transient inductance [41], [71]. As the interleaved phases increase, the asymmetry of the circuit as well as the complexity in design and control increase with limited benefits [72]. Although inverse coupled inductors have better performance in steady state and transient state than noncoupled inductors, winding path of coupled inductors is much larger. A twisted core coupled inductor is proposed [73], shown in Fig. 14. In [74], a lateral coupled inductor using ferrite material is proposed, shown in Fig. 15.

In addition, the magnetic integration is also employed in some resonant converters, such as LLC converter [42], [43]. The resonant inductor of LLC converter is realized by large leakage inductance of transformer. In order to achieving large inductance, an auxiliary core around primary windings and a low permeability layer between the primary and secondary are proposed in [43] and [42], respectively. For high output current situation, LLC converter with matrix transformer is proposed [75], [76]. The transformer consists of two cores, each of which integrates two matrix components. To further improve power density, a novel structure integrated four matrix transformer of LLC converter is proposed by CPES [77], achieving power density of 900 W/in$^3$, shown in Fig. 16. Shielding technique is used to reduce EMI effect of LLC converter with matrix transformer at high frequency [78].

### B. Electromagnetic Integration Technology

To further reduce the number and size of the passive components, the electromagnetic integration that combines the magnetics and capacitors is developed. The integrated passive module can be used in resonant applications [79], non-resonant [80] applications, as well as used as EMI filters [81]-[83].

An integrated LC structure is proposed [84]-[86], shown in Fig. 17(a). The structure has a dielectric material sandwiched between two planar conductors, and a module having distribu-
uted inductance and capacitance is formed. To further save space, capacitors, inductors and transformers are integrated together, forming the integrated LCT module [87]-[90]. For the resonant tank that contains magnetizing inductance, the structure of LLCT is obtained, shown in Fig. 17(b).

However, the optimized volume can’t be achieved without accurate electromagnetic design and loss model. For the sake of the optimized design of the integrated module, electromagnetic model and design as well as loss calculation are developed [91]-[97]. Besides, to ensure the reliable operation, thermo-mechanical analysis is described in [98]. To further improve the power density without exceeding the highest temperature of material, a method for heat dissipation is essential. In [99], heat extractors are embedded into the magnetic core, shown in Fig. 18. A prototype that can achieve power density more than 1 kW/in\(^3\) is obtained.

The LLCT modules have been implemented into resonant converter such as LLC resonant converter and non-resonant converter, namely asymmetrical half-bridge pulse width-modulation converter (AHBC) [44], [80], [100]. In [44], the LLC resonant tank is integrated into LLCT module, as shown in Fig. 19(a). The volume of passive integrated module is reduced to 14.6 cm\(^3\). In [80], LLCT modules are implemented into current-doubler rectifier. To save the footprint, two LLCT modules are integrated into a single planar magnetic core, shown in Fig. 19(b). The total volume is 60 cm\(^3\), which is much smaller than the discrete module. Therefore, by using LLCT module in the converter, the profile and volume can be decreased.

### C. Power Supply on Chip and Power Supply in Package

A higher-level integration is to integrate the magnetic components with other components of the converter together, including the switches, drivers, and controllers. This kind of integration is possible to obtain a very high-power density, along with improved reliability and efficiency. At present, the technology is mainly used for low voltage and low power applications due to its complexity. The integration technology can be classified into two categories as PwrSiP and PwrSoC [105]-[107].
PwrSoC is a wafer-level integration where the magnetic components are built in or on silicon die. A typical example is a micro-inductor built on silicon for a 20 MHz DC-DC converter in Fig. 22 [108]. The coil is typically formed by depositing conductor on silicon wafers with a maximum thickness of 50 μm. The thickness of the magnetic material covering the coil is generally limited to within 10 μm. This inductor can only handle 500 mA of currents due to the limited coil thickness. R. Meere et al. builds a 100 MHz magnetic core inductor on silicon wafer, and it shows higher efficiency than a comparable air core inductor on silicon even at 100 MHz [109]. P. Dhagat et al. proposes a V-groove inductor to increase the current capability [110]. A V-shaped groove is formed on the silicon substrate by etching, as shown in Fig. 23. More copper materials can be deposited in the groove to form a thicker coil conductor, and as a result, this inductor can handle up to 7 A of current. More researches have conducted to further optimize this V-groove inductor [111]. Another typical example is the air-core inductor presented in [112]. The converter’s operating frequency is pushed to 500 MHz, where the inductor needs only a very small value of 1.54 nH. This inductor was fabricated in a 65 nm CMOS chip. The output capacitor is also integrated into the chip. The total area occupied by the inductor and capacitor is only 1.1 mm², as shown in Fig. 24.

PwrSiP is to package a full converter into a single module, in which the magnetics and other components are connected internally. Compared to PwrSoC, PwrSiP is easier to be built and it can handle more power. Many companies have launched their own products [107], as shown in Fig. 25. To further improve the power density, many studies have been carried out. A power-system-in-inductor structure is proposed in [113], [114] where magnetic component is used as a package housing and the whole converter is packaged within the magnetic component, as shown in Fig. 26. Compared with the traditional plastic packaging structure, the inductor can gain much more space in the same package. As a result, the inductor can obtain greater inductance value and smaller DC resistance, which helps to improve the converter’s efficiency. In addition, the thermal performance of the module can be improved because the thermal conductivity of the magnetic material is higher than that of the plastic material. Another typical example is the 3D integrated point of load (POL) converter proposed by CPES [115], [116]. Fig. 27 shows the concept of a 3D integrated POL converter. The active devices are soldered on the one side of the PCB or DBC substrate, and a low profile LTCC inductor is placed on the other side of the substrate. This module can operate at up to 5 MHz [117]. The power density of the 3D integrated POL converter can achieve a power density of as high as 1100 W/in³, which is around 10 times higher than that of industry products at the same current level.
The LTCC material is made of ferrite tapes and ceramic tapes through stacking, pressing, co-firing and other steps [118]. It can be used to build passive components with low profile and flexible structure, which can help improve space utilization and facilitate integration [115], [119]. The CTE of LTCC material is around 5 ppm/°C, which is close that of silicon material, so that hybrid integration could be easily realized. The LTCC material also has higher thermal conductivity than FR4 used in PCB and thus features better thermal management.

An ultrathin coupled inductor based on LTCC technology was fabricated in [120], [121] for an interleaved buck converter. The thickness of the LTCC coupled inductor is only 1.3 mm. Another advantage of the LTCC inductor is that it has a distributed air gap, which is beneficial to reduce the AC loss of the winding when compared with the traditional air gap inductor. However, the flux density distribution of the distributed air-gap LTCC inductor is not uniform in the magnetic cores, which can cause the magnetic core near the conductor to saturate easily while the core away from the conductor is not fully utilized. To address this problem, Wang et al. [122]-[124] proposes a multi-permeability distributed air-gap magnetic structure. The internal permeability is lower than the external permeability, so a more uniform magnetic flux density distribution can be obtained. The multi-permeability LTCC inductor can achieve higher inductance value and relatively stable inductance value than the single permeability LTCC inductor without increasing the inductor size. A nonlinear LTCC inductor is proposed in [125]-[127]. The core of the LTCC inductor is made of ferrite tapes with different permeability. As the DC current increases, the ferrite tapes with high permeability gradually saturates, causing the inductance to drop gradually. This nonlinear inductor has a relatively large light-load inductance, which can help reduce light-load current ripple and thus improve the light-load efficiency. Fig. 28 shows a prototype of the nonlinear LTCC inductor with two different permeability.

CPES has conducted a series of studies for 3D POL integration using the low profile LTCC inductors as a substrate [128]-[136]. The use of low profile inductors allows for more efficient use of space when integrated with the active devices. Fig. 29 shows the LTCC inductors substrate. As the frequency increases, the LTCC inductor can be made thinner, thereby increasing the power density. To obtain a better performance of the LTCC inductor substrate, some studies have been carried out. The characteristics of the LTCC ferrite tape is explored detailly in [137]. Li et al. [136] proposed several models to calculate inductance for the LTCC inductor. A numerical model is proposed in [138] and an analytical model is proposed in [139] to calculate the core loss. Based on these studies, the LTCC inductor substrate is fully optimized for 3D integrated POL converter. Along with the layout optimization to reduce parasitic inductance, the use of DBC substrate to enhance heat dissipation, and the use of GaN devices to reduce switching losses, the switching frequency of the 3D integrated POL converter is pushed up to 5MHz [117]. Furthermore, a two phase LTCC coupled inductor is designed for the 3-D integrated POL converter, in which the frequency of the AC magnetic flux of the LTCC inductor reaches 10 MHz. The core thickness of the LTCC coupled inductor is only 0.4 mm.

IV. CONCLUSIONS

This paper reviews the state-of-the-art integration technologies involving active and passive integrations. The active integration technologies are reviewed from the aspects of interconnection technology, packaging material technology, packaging structure technology, and module-level integration technology. The emergence of wide band-gap semiconductor devices puts forward higher requirements for active integration technologies, especially parasitic and cooling issues. Great advancements have been made in active integration technologies. 1) Advanced wirebond-less technologies and advanced packaging structures (including 2.5D structures and 3D structures) have been developed to realize small parasitics and high heat-dissipation capability; 2) Emerging die-attaching materials, such as nano-silver sintering and TLPB, have demonstrated excellent high-temperature performance, and are promising for high power density applications; 3) The modules with integrated gate driver, decoupling capacitor, sensors, and heat sinks, etc. have been developed to achieve better performance. The passive integration technologies are reviewed from the aspects of the magnetic integration technology, electromagnetic integration technology, PwrSoC and PwrSiP technology, and LTCC integration technology. Magnetic integration technology and electromagnetic integration technology can effectively reduce the size of passive components, and have been applied to the various circuits, such as current-doubler rectifier, multiphase...
converter, LLC converter, etc. PwrSoC is a wafer-level integration and suitable for low current (below several amps) applications, while PwrSiP can handle currents up to 40 A. CPES has successfully developed a 3D integrated module with power density up to 1100 W/in². The LTCC magnetics have been successfully applied to high-frequency high-current 3D integrated module, and are expected to be extended to higher power integrated modules.

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