Analysis and Design of a 1200 V All-SiC Planar Interconnection Power Module for Next Generation More Electrical Aircraft Power Electronic Building Blocks

Mattia Guacci, Dominik Bortis, Ivana F. Kovačević-Badstübner, Ulrike Grossner, and Johann W. Kolar

Abstract—Compact, light weight and efficient Power Electronic Building Blocks are seen as fundamental components of future More Electric Power Systems, e.g. More Electric Aircraft. Core elements supporting the trend are power modules employing solely SiC MOSFETs. In order to take advantage of the high switching speed enabled by SiC, novel modules concepts must be investigated. For example, low inductance planar interconnection technologies, integrated buffer capacitors and damping networks are possible solutions to mitigate switching overvoltages and oscillations at the switching node occurring for conventional modules. In this paper, the analysis and the design of a novel ultra-low inductance 1200 V SiC power module featuring an integrated buffer-damping network are discussed. The power module is first described and characterized with impedance measurements. Afterwards, a general optimization procedure for the sizing and the selection of the integrated components is presented and measurements are performed to verify the analysis and to highlight the improvements of the proposed solution.

Index Terms—All-SiC Power Module, Damping Network, Integrated Buffer Capacitor, Planar Interconnection Technology.

I. INTRODUCTION

The More Electrical Aircraft (MEA) concept targets the replacement of mechanic, pneumatic and hydraulic systems of commercial aircraft with electric power converters and actuators, aiming for decreased fuel consumption and/or emissions reduction, increased reliability and/or lower maintenance effort [1]. The turning point of the trend can be traced back to 2010, when the milestone of 1 MVA of electric power was reached on board of Boeing™ B787. An electric power requirement of 1.6 MVA is planned for the next generation of aircraft [2], motivating the increased interest of the power electronics community in MEA. In particular, the Horizon2020 European Project 636170 - Integrated, Intelligent Modular Power Electronic Converter (12MPECT) [3], building on the expertise in device packaging, thermal management, converter design and reliability analysis of European industry and academia, intends to demonstrate significant advances in terms of power-to-weight ratio and efficiency of power converters for MEA. The primary goal is the realization of a Power Electronic Building Block (PEBB), i.e. a 99% efficient 3-phase inverter (cf. TABLE I) achieving a power-to-weight ratio of 10 kVA/kg, i.e. three times higher than nowadays available solutions [4].

PEBBs, i.e. modular power converters with defined functionality and simplified interfaces, combined with switching stages based on power modules employing solely Silicon Carbide (SiC) semiconductors (All-SiC PMs), can push the already strict requirements concerning compactness and light weight established in the aircraft industry even further, while still enabling reduced complexity and costs. The PEBBs approach reduces the engineering effort both in the design and in the maintenance phase of a power electronic system while SiC intrinsic qualities, e.g. higher switching speed, lower on-state voltage and improved temperature withstanding capability allow a reduction of the losses, output filter downsizing and low cooling requirements [5]. However, in order to guarantee the reliability of the PEBB and to fully utilize SiC performance, an ultra-low inductance PM designs is required. In fact, parasitic inductances in combination with the enabled high switching speed could cause significant overvoltages and undesired ringing [6]. This ultimately compromises the lifetime of the PM and increases its electromagnetic noise emissions [7].

To explore the state-of-the-art in terms of commutation...
loop inductance $L_{CL}$ in 1200 V All-SiC PMs [8]–[10], a comprehensive analysis of commercially available PMs is conducted. Most of nowadays available designs employ bond wires to interconnect the dies and feature $L_{CL}$ values in the range of 10 nH to 30 nH (cf. TABLE II). In order to allow a fair comparison between the PMs, a figure-of-merit is defined as

$$FOM = \left( \frac{R_{ds}I_{ds}^2}{V_{ds}I_{ds}} \right) \left( \frac{100}{L_{CL}} \right)^{-1}.$$ \hspace{1cm} (1)

The lower limit of $L_{CL}$ only slightly reduces to around 6 nH if research prototypes are considered [11]–[15]. Differently, when planar interconnection technologies are considered [16], [17], i.e. bond wires are replaced by wide coplanar structures [18], $L_{CL}$ can be reduced below 2 nH [19], [20] (cf. TABLE III). PMs adopting this solution provide benchmarks for the next generation of PMs. Additionally, planar interconnection technologies facilitate symmetric designs and enable doublesided cooling [7], [21] aiming towards an even increased power density.

A second measure allowing the utilization of SiC high switching speed is the integration of a buffer capacitor in the PM. It allows the decoupling of $L_{CL}$ from the parasitic inductance ($L_{ext}$) of the connection between the PM and the external input filter capacitor [11]. If a sufficient amount of capacitance is selected, the current during the switching transient is provided from the integrated capacitor and only the portion of inductance inside the PM ($L_{CL}$) experiences a fast current variation $dI/dt$ [22], mitigating the overvoltage. On the other hand, the paralleling of the buffer capacitor with the external capacitor introduces an undamped resonance network. Therefore, in order to prevent prolonged oscillations, a suitable damping network must be additionally integrated. Ultimately, the sizing of the buffer capacitor and of the optimized damping network result from a trade-off between required volume and effectiveness of the solution. Moreover, the impact of parasitic inductances, e.g. $L_{CL}$ and $L_{ext}$, on the performance of the buffer-damping network is not known in advance and therefore a widely applicable approach is desired. Accordingly, the focus of this paper is first on the design and experimental analysis of an All-SiC PM half-bridge arrangement featuring planar interconnections; second, the design procedure for an optimized integrated buffer-damping network with low sensitivity towards parasitic inductance is discussed. In order to experimentally validate the benefits enabled from a low inductance PM design and explore its limit, the PM prototype of Fig. 1 (a), featuring a planar interconnection technology, is characterized in Section II. The effectiveness of an integrated buffer capacitor against overvoltage is proven with measurements in Section III. Subsequently, in Section IV, the optimization of an integrated damping network is discussed and its performance are analyzed. Afterwards, a guideline for a general design procedure is described in Section V. Finally, conclusions are...
TABLE II
COMMUTATION LOOP INDUCTANCE OF COMMERCIAL AVAILABLE
1200 V All-SiC PMs

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>$I_s$ (A)</th>
<th>$R_{ds,on}$ (m$\Omega$)</th>
<th>$L_{CL}$ (nH)</th>
<th>FOM</th>
</tr>
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<tbody>
<tr>
<td>Cree™</td>
<td>138</td>
<td>13.0</td>
<td>15</td>
<td>0.45</td>
</tr>
<tr>
<td></td>
<td>285</td>
<td>5.0</td>
<td>14</td>
<td>0.60</td>
</tr>
<tr>
<td></td>
<td>256</td>
<td>3.6</td>
<td>5</td>
<td>2.60</td>
</tr>
<tr>
<td>Rohm™</td>
<td>180</td>
<td>7.8</td>
<td>25</td>
<td>0.34</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>4.7</td>
<td>13</td>
<td>0.65</td>
</tr>
<tr>
<td>Semikron™</td>
<td>523</td>
<td>5.6</td>
<td>15</td>
<td>0.27</td>
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TABLE III
COMMUTATION LOOP INDUCTANCE OF All-SiC PMs IMPLEMENTING PLANAR INTERCONNECTIONS

<table>
<thead>
<tr>
<th>Research Facility</th>
<th>$V_a$ (V)</th>
<th>$I_a$ (A)</th>
<th>$L_{CL}$ (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Univ. of Notthingham, et al. [23]</td>
<td>2500</td>
<td>-</td>
<td>1.7, ... 2.6</td>
</tr>
<tr>
<td>Univ. of Grenoble, et al. [7]</td>
<td>1200</td>
<td>144</td>
<td>&lt;2</td>
</tr>
<tr>
<td>Univ. of Tennessee, et al. [24]</td>
<td>1200</td>
<td>-</td>
<td>2.6</td>
</tr>
<tr>
<td>Fraunhofer™ IZM, et al. [19]</td>
<td>-</td>
<td>-</td>
<td>0.9</td>
</tr>
<tr>
<td>Semikron™ [20]</td>
<td>1200</td>
<td>400</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Fig. 2. Impedance measured from the DC terminals of the PM shown in Fig. 1 when (blue) both MOSFETs are conducting and (red) blocking. Series RL and LC equivalent circuits (dashed) with the values given in the figure match the measurements respectively. For frequency higher than 110 MHz, only the simulated curves converging to $L_{CL} = 1.6$ nH are shown.

connections (100 μm thick) from $S_h$ to AC (green) and from $S_l$ to DC$_-$ (yellow). A 50 μm thick polyamide-base material isolates the substrates from the interconnections.

Because of the selected technology, only one copper layer is available, therefore is not possible to overlap yellow and green connections aiming to a vertical design which would yield to an even lower $L_{CL}$ [18]. The area of the horizontal commutation loop (highlighted in grey), including the DC terminals and the MOSFETs, is minimized, whereas the distances are only constrained by the manufacturing process and/or isolation requirements. The overall size of the Al$_2$O$_3$ ceramic substrate (dashed in Fig. 1 (a)-(c)) results 39.4 mm$^2$13.8 mm with an overall maximum thickness of 1.3 mm.

B. Commutation Loop Inductance

In order to verify the effectiveness of this design solution, $L_{CL}$ is characterized with multiple impedance measurements. The measurements are conducted with a precision impedance analyzer Agilent™ 4294A in combination with the adapters 42941A and 16047E. Different adapters and connections to the PM influence the measurement, however the relative standard deviation results below 10%.

More in detail, when both MOSFETs are conducting, the circuit seen from the DC terminals of the PM can be approximated by a RL series connection, where $R = 2R_{	ext{sho}}$ and $L = L_{CL}$. Differently, when both MOSFETs are in the blocking state, the impedance resemble a LC series connection, where $L = L_{CL}$ and

\[
C = \frac{1}{2} \left( C_{gds} C_{gd} + C_{ds} \right) = \frac{1}{2} \left( C_{\text{obs}} - \frac{C_{th}^2}{C_{th}} \right) \tag{2}
\]

is defined by the parasitic capacitances of the two SiC MOSFETs connected in series (neglecting $C_s$). The impedance of ideal RL and LC equivalent circuits are analytically calculated in the frequency domain and the value of $R$, $L$ and $C$ are selected in order to best approximate the measured curves, as
shown in Fig. 2. The value of \( R_{\text{on,dc}} \) is additionally measured during the conduction of a DC current where, in accordance with [25], approximately 25 m\( \Omega \) results for each MOSFET; moreover, inserting in (2) the values of the parasitic capacitances specified in [25] for \( v_{\text{ds}} = 0 \) V, an equivalent capacitance \( C = 1.4 \text{nF} \) results as expected. Even if the frequency measurement range of the instrument is limited to 110 MHz, the analytical curves clearly converge to the extrapolated value of \( L_{\text{cl}} = 1.6 \text{nH} \).

Remark: nowadays, the evaluation of \( L_{\text{cl}} \) is typically entrusted to the electromagnetic modelling of the PM supported by specialized softwares, such as Ansoft\textsuperscript{TM} Q3D [12]–[14]. According to the trend, the 3D CAD file provided from the PM manufacturer is imported in Q3D and, after simulating the described experiment, \( L_{\text{cl}} = 2.7 \text{nH} \) results. The relative discrepancy is significant and the simulated value shows excessive variations depending on the setting of the excitation ports in the simulation tool. This issue is under investigation [26], however the cause is identified in the hypothesis of equipotential excitation ports, ultimately representing the boundary conditions for the simulated electromagnetic problem.

C. Gate Loop Inductance

The connection from the PM to the gate driver plays an important role in the shaping of the voltage and current waveforms during a switching transient. In a first approximation, the path from the driver to the gate connection on the die can be represented with the inductance \( L_g \) shown in Fig. 1 (c). Intuitively, \( L_g \) limits the changes of the gate current, reducing the bandwidth of the driver. This consequently increases the delay time and the current rise time, ultimately increasing the switching losses [27].

Additionally, the charging process of \( C_{gs} \) excites a resonance at \( f_{\text{res}} = \frac{1}{2\pi}\sqrt{L_g C_{gs}} \), and, in order to limit \( v_{gs} \) below the gate voltage rating of the MOSFET, a lower boundary for the gate resistance \( R_{g,\text{lim}} \) is set, \( R_{g,\text{lim}} \) proportional to \( L_g \) but while being effective in damping the resonance, it also limits the maximum switching speed.

Based on the premises above, it is clear that the minimization of the gate connections length should be of main concern for the design of a PM. The integration of the gate driver is only ideally a valid option, because it requires additional effort, leads to higher costs and size, and increases the failure rate of the PM [28]. Short, wide and coplanar connections are more realistically advised as best practice. For convenience, however, gate and source terminals are typically routed all together and next to each other to one side of the PM. Adopting this approach, the value of \( L_g \) can easily reach 30 nH [11], resulting in the mentioned drawbacks.

Additionally, if the connection to the source of a MOSFET is partially shared between gate driver and bridge-leg, a fraction of \( L_g \), \( L_s \), in Fig. 1 (c)), known as common source inductance, is shared with the path defining \( L_{\text{cl}} \). Consequently, a change on \( L_s \) directly affects \( v_{gs} \) according to

\[
v_{gs} = v_{gs,0} - L_g \frac{di_{gs}}{dt}
\]

E.g. with a current slope of \( 10 \frac{A}{ns} \), each 100 p\( \Omega \) of \( L_s \) subtracts 1 V from \( v_{gs,0} \) during a turn-on transition, providing a negative feedback reducing the switching speed. This issue is well known and can be avoided splitting the power source and the gate source connection, i.e. Kelvin source. It is less transparent, instead, that even if \( L_g \) and \( L_{\text{cl}} \) are physically independent, the magnetic coupling between them (\( M_{g,\text{cl}} \)) basically plays the same role as \( L_g \). Although it is difficult to experimentally quantify the impact of \( M_{g,\text{cl}} \) on \( v_{gs} \), it is important to be aware of its consequences once the gate driver is arranged in the close proximity of the PM.

In the considered PM, gate and Kelvin source solder pads are directly accessible from the top of the dies (\( G_L, G_H \) and \( S_L, S_H \) indicated in Fig. 1 (a)). In particular, \( S_H \) directly contacts \( T_{\text{in}} \) and is separated from the copper interconnection carrying the load current to AC (yellow); the same applies for \( S_L \), separated from DC_. Short and wide copper connections are used to connect the solder pads to the driver, reducing \( L_g \) to only 6 nH. In this way, low values of \( R_g \) could be selected, achieving high switching speed therefore minimizing the switching losses without the risk of damaging the gate dielectric. With the aim of further reducing \( L_g \), a solution featuring overlapping gate connections on a flexible PCB could be used. In the case at hand, Q3D simulations performed on the complete setup [26], obtained by merging the CAD file of the PM and of the gate driver PCB, showed negligible coupling.
III. Integrated Capacitive Snubber

The amount of capacitance necessary at the DC side of a converter (C_{dc}) can vary in a wide range depending on the power rating and input voltage V_{dc} and it typically results in a bulky structure (e.g. C_{dc} \approx 100 \mu F in the considered setup) that hardly finds place in the closest proximity of the switching stage, i.e. the PM. The inductances of the conductors connecting C_{dc} to the DC terminals of the PM significantly contribute to the total power loop inductance L_{PL} = L_{ext} + L_{CL}. In particular, its ideal lower boundary is limited by the parasitic inductance of C_{dc} (ESL), typically in the order of 10 nH to 20 nH [29]. A significant L_{ext} vanishes the benefit of a low inductance PM design, therefore a possible solution, i.e. the integration of a buffer capacitor in the PM (cf. Fig. 3), is analyzed in this section.

The circuit supporting the first part of the explanation is shown in Fig. 4 (a). It represents the PM of Fig. 1 (dashed box) connected in a Double Pulse Test (DPT) setup and simplified for the case of a hard turn-on switching transition of the high-side MOSFET T_H. The parameters of the DPT setup and the values of the parasitic elements introduced in Fig. 4 (a) are summarized in TABLE IV (herein L_{ext} = 15 nH and R_g = 1.5 \Omega if not differently specified).

A current step through L_{ext}, originating from the switching transition, excites the resonance between L_{PL} and C_{o} (C_{dc} \rightarrow \infty). C_{o} represents the parallel connection of the output capacitance (C_{oss}) of the low-side MOSFET T_L with the parasitic capacitance of the PM from the switching node to DC_ (C_p cf. Fig. 1 (c)). While the latter depends only on the geometry of the PM (i.e. C_{p} = 45 pF), C_{oss} is non-linear, i.e. C_{oss}(v_{ds}); however, in order to best model the resonance occurring on a DC voltage bias, C_{oss}(V_{dc}) = 215 pF [25] is considered. This results in C_{o} = 260 pF.

The frequency dependent parasitic resistance R_{ac}(f) > R_{ds,on} of the L_{PL}C_{o} resonant network, typically much smaller than its characteristic impedance, \sqrt{L_{PL}/C_{o}} \approx 8 \Omega, is the only damping element present. Consequently, a voltage spike and a prolonged oscillation at the voltage v_{ov} across T_L occurs, as shown in blue in Fig. 5. v_{ov} reaches 896 V (v_{ov,pk}), more than 300 V above V_{dc}, and strongly oscillates when R_g = 1.5 \Omega. This waveform provides other information on the parameters of the equivalent circuit of Fig. 4 (a). Knowing C_{o}, L_{PL} can be calculated from the resonant frequency f_{tot} = 1/2\pi \sqrt{L_{PL}/C_{o}} = 77 MHz and 16.6 nH results as expected (L_{PL} = L_{ext} + L_{CL} = 15 nH + 1.6 nH). Additionally, analyzing the exponential decay of

\[ v_{ov}(t) = V_{dc} + (v_{ov,pk} - V_{dc})e^{-t/\tau}, \]

with a time constant of \tau = 48 ns, R_{ac}(f_{tot}) = 0.7 \Omega results. The...
value of $R_{ac}$ completes the linear model shown in Fig. 4 (a), enabling the simulation of the waveforms of $v_{ov}$; hence, the oscillation after the switching transient and its decay can be compared with measurements. However, correct initial conditions, i.e. the amplitude of the current step $I_{int, pk}$ exciting the resonance, must be set and therefore must be known in advance. For this reason, a measurements-based approach is initially preferred to optimize the buffer-damping network.

With the integration of the buffer capacitor $C_b$ in the PM, as shown in Fig. 4 (b) and Fig. 3, $L_{PL}$ is split in $L_{ext}$ and $L_{CL}$, and $L_{CL}$ is minimized. Consequently, the high frequency current components excited during the switching transient are confined in a smaller loop (green in Fig. 4 (b)) and bypass $L_{ext}$ significantly reducing $v_{ov,pk}$. The final goal of quantifying the achievable improvements and dimensioning $C_{bn}$ several experiments are performed.

Two measured waveforms (red and yellow) are shown in Fig. 5 for two different values of $C_{bn}$ = 2.5 nF and 10 nF. The main resonant frequency is now shifted to $f_{ext} = \frac{1}{2\pi \sqrt{L_{ext} C_{bn}}} < f_{int}$ ($f_{int} = 26$ MHz and 13 MHz, respectively) because $C_b > C_{bn}$ and $L_{ext} \approx L_{PL}$. Due to the lower resonant frequency, $R_{ac}$ reduces $(R_{ac}(f_{ext}) \approx 0.1 \ \Omega, ... 0.2 \ \Omega)$ and correspondingly increases to 105 ns and 294 ns, prolonging the oscillation.

Moreover, connecting $C_b$ is a second resonant network resonating at $f_{int} = \frac{1}{2\pi \sqrt{L_{int} C_b}} = 247 \ \text{MHz} > f_{int}$ (because $L_{int} < L_{PL}$) is formed. The associated oscillation is only partially visible on the waveforms, given the ultra-low inductance design and the higher frequency of voltage dependent resistance. Nevertheless, if needed, it can be damped at the AC side of the PM [30]. However, it is worth noticing that, if $f_{int}$ exceeds the parasitic frequency of the output filter, less attenuation might be guaranteed from it.

Fig. 5 provides an additional information on the effective capacitance of $C_{bn}$. In this setup, $C_{bn}$ is implemented by connecting one or more *Kemet* 1500 V $X7R$ ceramic capacitors [31] with values between 4.7 nF and 12 nF in parallel (cf. Fig. 3). A reduction of capacitance, due to the DC voltage offset, is expected and confirmed from the measurements.

Knowing $L_{ext}$ and measuring $f_{ext}$, the effective value of $C_b$ can be calculated in the different cases; the resulting capacitance is always approximately half of the nominal value $C_{bn, nom}$. For the sake of clarity, the reported value of capacitance always refers to the effective one.

Overvoltage and oscillation can become more severe in case of higher switching speed or in designs featuring bigger $L_{int}$. Fig. 6 (a) summarizes $v_{ov,pk}$ for different combinations of $R_g$ and $L_{ext}$ which, without $C_b$, have a strong influence on $v_{ov,pk}$. As can be noted, $L_{ext} = 35 \ \text{nH}$ and $R_g = 1.5 \ \Omega$ cause $v_{ov}$ to exceed the voltage rating of CPM2-1200-0025 (i.e. 1200 V). Additionally, the sensitivity of $v_{ov,pk}$ towards $L_{ext}$ is plotted (b). Without $C_b$, it is above 15 V, while with $C_b$ bigger than 5 nF, it is limited below 5 V in both cases.

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$C_b = 2.5 \ \text{nF}$ is sufficient to maintain $v_{ov,pk} < 900 \ \text{V}$ for all the considered combinations. Increasing $C_b$ to 5 nF is only effective on the worst case (orange), whereas $C_b > 5 \ \text{nF}$ brings no real further improvement from this point of view. This is clarified in Fig. 6 (b), where the sensitivity of $v_{ov,pk}$ towards $L_{ext}$ is plotted. Almost independently from $R_g$, the sen-
Damping Network Optimization

As discussed in Section III, $C_s$ effectively limits $v_{ov(pk)}$ and relaxes the design constraints on $L_{ov}$, but indirectly modifies the impedance of the input filter ($Z_0$ in Fig. 4 (b)) as shown in Fig. 7. As a consequence, the main resonant frequency, clearly visible at the output voltage $v_{ov}$, is shifted from $f_{ext}$ to $f_{ext}$. As described in Section III, due to the reduction of $R_{ac}$, less damping is provided and the oscillation is prolonged. Then, with the considered values, $f_{ext}$ enters the regulated EMC spectrum ($f_{ext} < 30$ MHz) negatively affecting the electromagnetic noise compatibility of the PEBB. Finally, the ringing at $v_{in}$ reflects on the current flowing through $C_{ac}$, the comparable amplitude and reduced damping degrade its lifetime.

This premise motivates the analysis and the optimization of a damping network presented in this section. Different damping approaches are discussed in literature [33]; the simplest damping approach avoiding steady-state losses is a series $R_sC_s$ network in parallel with $C_s$ [34], [35] (cf. Fig. 3 and Fig. 4 (c)). This approach is selected to facilitate the integration in the PM. In first place, a design procedure should be defined to dimension $R_s$ and $C_s$, once $L_{ov}$ and $C_b$ are fixed. [33] proposes an optimization routine that, given the maximum allowed peak of the buffer-damping ($C_s$ - $R_sC_s$) network output impedance ($Z_{ov(pk)}$), provides the value for $R_s$ and $C_s$ ensuring optimal damping, i.e. minimizing $Z_{ov(pk)}$

![Output Impedance Z_0 vs. Frequency](image)

### Table V

<table>
<thead>
<tr>
<th>$L_{ov}$(nH)</th>
<th>$C_b$</th>
<th>$C_{b,nom}$(nF)</th>
<th>$C_d$</th>
<th>$C_{d,nom}$(nF)</th>
<th>$R_d$(Ω)</th>
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<td>15</td>
<td>2.5</td>
<td>4.7</td>
<td>5.0</td>
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This closed form procedure is preferred over an analytical approach [36]. In order to explore the effectiveness of this solution, a wide set of measurements with damping network featuring different combinations of $R_s$ and $C_d$ is performed and the results are commented in the following.

Fig. 8 (a) shows $Z_{ov(pk)}$ for different $R_s$-$C_d$ pairs in the range $0.5 \Omega < R_s < 10 \Omega$ and $2 \text{nF} < C_d < 10 \text{nF}$ with $L_{ov} = 15 \text{nH}$, $C_s = 2.5 \text{nF}$ and $R_{ac} = 200 \text{mΩ}$. Only three values for $R_s$ (0.5 $\Omega$, 1.5 $\Omega$ and 4.7 $\Omega$) and $C_d$ (2.5 $\text{nF}$, 5 $\text{nF}$ and 10 $\text{nF}$) are considered in the experiments. Thus, the highlighted nine different combinations for $R_s$ and $C_b$ having $Z_{ov(pk)}$ in the range between 1.8 $\Omega$ and 9.4 $\Omega$, are analyzed. The performance of the damping network outside this range rapidly decay. In Fig. 8 (b)-(d), the corresponding measured waveforms of $v_{ov}$ are illustrated.

Because of the additional capacitance $C_d$ and resistance $R_d$, $v_{ov(pk)}$ is now limited to values below 600 $V$, even if $C_b = 2.5 \text{nF}$ is considered. As shown in red in Fig. 8 (c), $Z_{ov(pk)} = 3 \text{Ω}$ (e.g. $R_s = 1.5 \text{Ω}$ and $C_d = 5 \text{nF}$) results to be sufficient to limit $v_{ov(pk)}$ below $V_{dc} + 50 \text{V}$ and to cancel the oscillation after its first peak in the considered conditions. Correspondingly, Fig. 7 (yellow) shows how the integration of this $R_sC_s$ network reduces $Z_{ov(pk)}$ from 30 $\Omega$ to 3 $\Omega$, effectively damping the resonance. A $C_s$-$R_sC_s$ network featuring a smaller $Z_{ov(pk)}$ (yellow in Fig. 8 (c)) does not show significant improvement on the damping performance, however, the associated value of $C_d$ increases, complicating the integration.

Fig. 8 (b) and (d) additionally confirm how $Z_{ov(pk)}$ is a good indicator of the performance of the damping network. Given the shape of the isolines, Fig. 8 (d) shows three measurements where, even changing the value of $C_d$, $Z_{ov(pk)}$ remains between 4 $\Omega$ and 5 $\Omega$. As a consequence, the resulting $v_{ov}$ waveforms are similar in the three cases. Differently, the three measurements reported in Fig. 8 (b) cover almost the full range of $Z_{ov(pk)}$ (i.e. 2.5 $\Omega$, ... 9.4 $\Omega$) and the performance of the damping network significantly improves (i.e. from almost ineffective to comparable with the optimized design).

Ultimately, the values reported in the first row of TABLE V ($L_{ov} = 15 \text{nH}$) are selected.

In Fig. 8 (a), the locus of [33]-optimum solutions, revisited to consider the influence of $L_{ov}$, is additionally marked with a white dashed line. As expected, fixed $Z_{ov(pk)}$ (i.e. an isoline), it selects the corresponding design featuring minimum $C_s$. Therefore, an alternative usage of the 2D-plot of Fig. 8 (a) consists in finding the value of $R_s$ minimizing $Z_{ov(pk}$ once the maximum value of $C_d$ is given, e.g. from volume constraints. The entire optimization procedure is repeated for $L_{ov} = 35 \text{nH}$ and the values of the resulting components are also reported in TABLE V for comparison. Intuitively, a bigger $C_d$...
compared to the design optimized for \( L \) overall capacitance but features four times higher sensitivity.

In fact, for the first design, considering 152 mΩ/nH, the sensitivity of \( L \) is fixed to 2.5 nF, \( Z_b \) is fixed to 2.5 nF, \( L \) is finally examined. The measured peak voltage across \( R_d \) is shown to be 2.7 Ω, 2 Ω, 1.5 Ω and sub-optimal performance comparable to Fig. 8 (c). This information is more than expected results in \( Z_{pk} = 4.5 \) Ω and sub-optimal performance comparable to Fig. 8 (c).

The behavior of the two optimized snubbers (TABLE V) is finally examined. The measured peak voltage across \( R_d \) amounts to around 50 V in both cases and is therefore not of concern. Differently, the occurring losses could be problematic: in the considered setup, with a switching frequency of 30 kHz, the losses amount to 0.75 W and 1.25 W in the case of \( L_{ext} = 15 \) nH and 35 nH respectively. Intuitively, a more critical situation (i.e. \( L_{ext} = 35 \) nH) generates more losses to achieve the same performance. Nevertheless, in both cases a power resistor rated for 2 W (Vishay™ Thin Film power resistors [37]) can be used, as shown in Fig. 3.

V. DESIGN PROCEDURE GUIDELINE

After clarifying the optimization of the damping network, a guideline of the described procedure for the design of the \( C_b-R_dC_d \) network (Section III and IV) is provided in this section (cf. Fig. 10). First, the followed measurements-based approach is considered:

(i) **Worst Case Conditions:** setup the DPT in the worst case scenario, i.e. for the highest \( V_{pk}, L_{ext} \) and \( L_{c} \).

(ii) **Optimization Constraints:** define the safety margins \( V_{pk,max} \) and \( V_{ov,max} \). Limit the maximum value of \( C_b \) and \( C_d \) that can be integrated in the PM, e.g. a 1210 ceramic chip (\( C_{max} \)) due to limited volume.

(iii) **Buffer Capacitor:** measure \( V_{ov, pk} \) after a hard turn-off switching transition of \( T_1 \) in the DPT setup. Iteratively decrease the value of \( R_d \) and increase the value of \( C_b \) until the highest switching speed (\( R_b = 0 \) Ω or \( v_{ov} > v_{pk,max} \)) limiting \( V_{ov, pk} < V_{ov, max} \) with \( C_b < C_{max} \) is reached (cf. Fig. 6 (a)). Further increasing \( L_{ext} \) only slightly
Fig. 10. Flow-chart providing a guideline for the design of the $C_d R_c C_L$ network as presented in this paper. Set the worst case conditions, the experiments described in Fig. 6 (a) define the required value for $C_{ov}$ while the procedure presented in Fig. 8 (a) results in the optimized damping network $R_c C_d$. A simulation based approach, considering the equivalent circuit of Fig. 4 (c), gives accurate results once precise initial conditions and values of the parasitic elements are set.

(i) $I_{ov, max}$ $V_{ov, max}$ $C_{OV, max}$
(ii) $I_{pk, max}$ $V_{pk, max}$ $C_{pk, max}$

Measurement Simulation

(iv) $Z_{0,pk}$ $R_c$, $L_{ext}$ $C_d$
(v) $C_{d}$, $R_c$

Fig. 5

Fig. 6 (a)

Fig. 4 (b)

Fig. 7

Fig. 8 (a)

Fig. 4 (c)

Parasitic Elements: extract the values of $L_{ext}$ and $R_{ext}$ from the ringing and the damping at $v_{ov}$ (cf. Fig. 5).

Damping Network: for given $C_{ov}$, $L_{ext}$ and $R_{ext}$ calculate $Z_0$ for a defined range of $R_d$ and $C_d < C_{ov, max}$ (cf. Fig. 7). Plot $Z_{0,pk}$ as a function of $R_d$ and $C_d$ (cf. Fig. 8 (a)) and select the $R_d C_d$ pair minimizing $Z_{0,pk}$.

Verification: $V_{ov,pk}$ is reduced further below $V_{ov,max}$ and the oscillation is optimally damped (cf. Fig. 8 (c)). Measure the losses occurring in $R_d$ to guarantee continuous operation. Further increasing $L_{ext}$ only slightly worsen the damping performance (cf. Fig. 9).

If at the end of the procedure the result is too conservative, the constraints on $V_{ov,max}$ and $C_{ov, max}$ can be tightened and the steps from (iii) on repeated. A more compact or more efficient, but as well effective, design is obtained. Differently, if the specifications cannot be met, the mentioned constraints must be loosened or $L_{ext}$ must be reduced.

A simplified simulation-based approach is validated in parallel to the entire analysis. The equivalent circuit shown in Fig. 4 can reproduce the damped and undamped measured waveforms of $V_{ov}$ once all its parameters are correctly set. While the values of the parasitic elements $R_{pk}(f)$, $L_{ext}$ and $L_{CL}$ can be entrusted to FEM simulators, the amplitude of the current step exciting the circuit, i.e. the peak of the switched current $i_{pk}$ is unknown. Unfortunately, the capacitive current peak and the reverse recovery current peak, non-linear and correlated to the MOSFETs’ characteristics and dynamics, add to the load current $i_{ext}$. Therefore, either full confidence is placed on the Spice model of the MOSFETs (when available), or conservative assumptions, based on the MOSFET datasheet, are necessary. Nevertheless, the analytical approach summarized in Fig. 4 (c) and TABLE IV is valuable, especially for a preliminary analysis of the problem.

Finally, it is worth noticing that the applicability of the guideline can be generally extended to PMs without integrated buffer capacitors and to PCB-based converters where $C_{ov}$ does not find place in the closest proximity of the bridge-leg.

VI. CONCLUSION

A novel, ultra-low inductance (i.e. 1.6 nH) All-SiC PM for More Electrical Aircraft application featuring a planar interconnection technology is analyzed in this paper.

Despite the low parasitic inductance of the PM, the full exploitation of SiC power MOSFETs’ high switching speed requires precautions concerning switching overvoltages and ringing at the switching node. Measurements proved that the integration of a buffer capacitor is generally an effective measure to minimize the drawbacks associated to the parasitic inductance of the connection to the external capacitor. However, although this solution mitigates the overvoltage, it even aggravates the oscillation, as now a resonant network is formed by the two capacitors and the inductance of the interconnection. Consequently, the integration of a $R_c C_d$ damping network is recommended. At the expenses of only 1 W of losses and in a limited footprint, the switching overvoltage peak is significantly reduced (-80%) and the oscillation is optimally damped. Both solutions are analyzed in detail, optimized for the considered setup, verified with measurements and finally commented.

Ultimately, the designed PM is operated with a gate resistance of only 1.5 Ω (in order to minimize the switching losses) without experiencing any undesired effect due to the achieved high switching speed. This outcome validates the effectiveness of the buffer-damping network and allows the designers to explore the limit performance enabled from All-SiC PMs featuring planar interconnection technologies.

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