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EDITORIAL

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Editorial for the Special Issue on Distributed Energy Resources

TRANSFORMATION of the existing electric power systems into modern smart grids is gaining momentum as mostjurisdictions are seeking ways to lower their energy consumptions, life cycle costs and greenhouse gas (GHG) emissions. The transformation requires the integration of significant renewable energy into the existing power systems, which has posed tremendous technical and operational challenges involving the issues of voltage and frequency stability, insufficient energy storage, resources for system balancing and dispatch, renewable energy intermittency, and much more. During a recent research trip of mine to an island country, I got the first-hand experience in how the fast down-ramping events of a large central photovoltaic (PV) plant could cause load shedding and PV generation curtailment. Innovative solutions are needed to support this power system transformation, as the need for additional system resources can no longer be met by building more central generation plants.

As an integral part of modern power systems, distributed energy resources (DER) have been rapidly deployed throughout the world, initially as an effective means of clean generation to displace fossil fuels and subsequently as resources to provide power system functions such as ancillary services and peak load reduction. DERs include distributed generation systems such as wind, solar and CHP systems, energy storage units including electric vehicles, controllable loads, and associated power conversion and control systems, all in power distribution networks. The innovative solutions to facilitate the seamless integration of DERs into electric grids and the creation of new power systems resources have never been more important than today. These solutions are critical to enabling maximum penetration of renewable energy, while allowing utilities to maintain high standards of grid stability, reliability, flexibility, and economy. The purpose of this Special Issue is to review the state-of-the-arts in the DER fields and to disseminate the recent technological advancement in DERs, pertinent to analysis, design, conversion, control, performance, and application.

The Special Issue on Distributed Energy Resources collected 5 papers on diverse topics, ranging from the state-of-the-art reviews to the focused new discoveries. The first paper entitled "Optimal Design and Operation of a Remote Hybrid Microgrid" as written by Dr. Farzam Nejabatkhah and his colleagues at the University of Albert (Canada) presented the design, operation, and dispatch strategies for an isolated hybrid microgrid containing photovoltaic (PV) systems, battery energy storage systems (BESS) and diesel generators. A Northern remote off-grid community in Canada was used for the case study. Custom models to accurately represent all components of the hybrid microgrid in the Northern climate were developed. Optimization algorithm that minimizes the annual system cost were developed to size the PV and BESS. The paper demonstrated both cost saving and power quality improvement with the installation of PV and BESS systems, which may present guidelines for achieving similar benefits in other isolated hybrid microgrids.

The second paper contributed by Dr. Meiqin Mao and her colleagues at Hefei University of Technology (China) has a title of "Decentralized Coordination Power Control for Islanding Microgrid Based on PV/BES-VSG". The paper proposed a decentralized virtual synchronous generator (VSG)-based adaptive coordinated control strategy for islanded microgrids consisting of photovoltaic generators combined with battery energy storage (BES) on the DC side (PV/BES-VSG). With the proposed method, the droop characteristics of VSGs could be adaptively adjusted according to the DC bus voltage. The local controllers of PV/BES-VSG units could switch between the operating modes automatically without the need of a central controller. In this way, the power sharing among PV/BES-VSG units was achieved according to the maximum output power of PVs and the limit of charging/discharging power of BES, leading to the maximum utilization of renewable energy resources.

The third paper on "Power System Support Functions Provided by Smart Inverters–A Review" was contributed by Dr. Xin Zhao and his colleagues at the University of New Brunswick (Canada). The paper reviewed the new development in international standards relevant to "smart inverters" for distributed energy resources, particularly for the provision of grid support functions, such as reactive power control, harmonic compensation, voltage and frequency fault ride-through, which is key to achieving higher utilization of renewable energy based distribution generation systems in the distribution power networks. Experimental results from smart inverters were given in the paper to demonstrate the implementation of these power system support functions in contributing to reduced cost of energy and additional system resources.

The fourth paper is on an interesting topic of "Integration of Distributed Energy Resources into Offshore and Subsea Grids", and was submitted by Ms. Razieh Nejati Fard and Dr. Elisabetta Tedeschi of the Norwegian University of Science and Technology (Norway). This paper reviewed the recent developments in offshore and subsea electric distribution grids, particularly in case of high penetration of distributed and intermittent renewable energy sources. The paper provided an overview of electric loads operating in the ocean environment, their power and energy demands, and their main operational characteristics and corresponding maturity of technologies.

This paper presented the emerging trends in the electrification of the ocean space through the development of "offshore smart grids", a fascinating area where most of us would have not been exposed to yet.

The fifth paper entitled "Reconfiguration of NPC Multilevel Inverters to Mitigate Short Circuit Faults Using Back-to-Back Switches" was composed by Mr. Weiqiang Chen and his colleagues at University of Connecticut. This paper proposed a new reconfiguration method to mitigate short circuit faults in any devices and at any voltage levels in neutral point clamped (NPC) multilevel inverters which have been widely used as power conversion apparatuses for distributed energy resources. Simulation was conducted on a five-level NPC inverter with non-idealities to verify the proposed reconfiguration method. A five-level NPC inverter was built and tested to experimentally demonstrate that the proposed method could lead to a quick and effective recovery of the NPC inverter from faulty conditions.

I would like to express my deep gratitude to the industrious and thorough work of the guest associate editors of this Special Issue in selecting these high quality papers from a pool of manuscripts submitted for consideration for publication. I wish to thank the tremendous efforts of the expert reviewers who have provided invaluable, in-depth comments and suggestions in assessing and recommending the submitted manuscripts.

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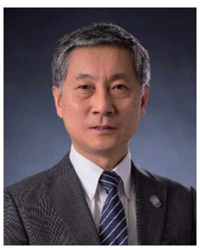

Liuchen Chang received B.S.E.E. from Northern Jiaotong University in 1982, M.Sc. from China Academy of Railway Sciences in 1984, and Ph.D. from Queen's University in 1991. He joined the faculty of University of New Brunswick (UNB) in 1992 and is a professor in Electrical and Computer Engineering. He was the NSERC Chair in Environmental Design Engineering for the Atlantic Provinces during 2001-2007, the Principal Investigator of Canadian Wind Energy Strategic Network (WESNet) during 2008-2014, and played a pivotal role in establishing the Emera and NB Power Research Centre for Smart Grid Technologies at UNB in 2016/2017. He is a vice president of the IEEE Power Electronics Society.

Dr. Chang was the recipient of CanWEA R.J. Templin Award in 2010 for his contributions in the development of wind energy technologies, and the Innovation Award for Excellence in Applied Research in New Brunswick in 2016 for his contributions in renewable energy conversion. He is a fellow of Canadian Academy of Engineering (FCAE). He has published more than 350 refereed papers in journals and conference proceedings. Dr. Chang has focused on research, development, demonstration and deployment of grid-connected power converters, renewable energy based distributed generation systems and direct load control systems.

Optimal Design and Operation of a Remote Hybrid Microgrid

Farzam Nejabatkhah, Yun Wei Li, Alexandre B. Nassif, and Taeho Kang

***Abstract*—High operational costs, environmental concerns and fuel handling challenges in diesel-based remote off-grid systems have prompted the application of alternative sources of energy and energy storage systems. Based on these drives, operators of isolated microgrids have been seeking out these alternatives. In response, a Canadian utility is investigating the application of utility scale photovoltaic (PV) generation and Battery Energy Storage Systems (BESS) to supplement existing Diesel Generators (DiGs) in an off-grid community. This paper presents the design, operation, and dispatch strategy for this hybrid PV/BESS/DiG isolated microgrid. A Northern remote off-grid community in Canada is used as a case study. Custom models to accurately represent all components of the hybrid microgrid in the Northern climate are developed first. Then, optimization algorithm that minimizes the Annual System Cost (ASC) are developed to size the PV and BESS. The algorithm incorporates the cost of the BESS, the rated power limits of PV and BESS, and the prime rating capability of DiGs. Finally, the paper proposes to optimally site the BESS by minimizing the total system loss and optimizing the voltage profile along the feeders. The study reports both cost saving and power quality improvement with the installation of PV and BESS, and presents guidelines on how to generalize these results to other hybrid isolated microgrids.**

***Index Terms*—Annual system cost (ASC), battery energy storage system (BESS), diesel generators (DiGs), dispatch strategy, hybrid microgrid, optimization, photovoltaic (PV).**

I. Introduction

HIGH transmission cost of electricity is often the reason remote communities are operated off-grid. In these cases, diesel generators (DiGs) present themselves as a more economic option to the electric utility. In Canada, there are around 300 remote off-grid communities that are mostly powered by DiGs [1]. Fuel transportation is often a challenge to those communities, especially during the months without road access (ice roads are typically available from December to March only). At the same time, the load growth in those communities often prompts continual investment on additional diesel storage tanks if DiGs remain the only generation option. In recent years, there has been a strong drive to install photovoltaic (PV) farms and battery energy storage systems (BESS) to support DiGs in remote communities in Canada, in a number of government incentives [2]-[4]. In such systems, optimum sizing and siting of PV and BESS, as well as their control strategies are important topics.

In general, the sizes of power sources in microgrids are determined by using optimization problem [5]-[8], in which the components of microgrids are modelled from different perspectives, e.g., economic models, power models and dynamic models, considering various objectives [9]-[16]. Their locations also have profound effect on the microgrid performance. While the PV system location is typically constrained by land requirements and availability, the BESS location is much more flexible. In general, BESS' allocation methods can be divided into two groups: 1) optimum battery operation [17]-[20] and 2) optimum microgrid operation [21]-[29]. In the first category, objectives such as installation [17], maintenance [18], and operation [19] are considered. These methods are not commonly used in power system since they are not holistic. In the second category, different objectives such as transient stability improvement [21], power losses minimization [22], [23], voltage stability/profile improvement [24]-[26], load shifting and peak shaving [27], distributed generation support [28], [29] are considered.

This paper presents the design procedure, operation and dispatch strategy of a hybrid PV/BESS/DiGs microgrid. The optimal sizes of PV and BESS systems, and the optimal location of the BESS are determined. A Northern remote off-grid community in Canada is used as a case study. Here, Annual System Cost (ASC), which contains Annual Capital Cost (ACC), Annual Operation Maintenance Cost (AOMC), Annual Replacement Cost (ARC), Annual Fuel Cost (AFC), and Annual Emission Cost (AEC), are minimized subjected to the microgrid's configuration and operation constraints to achieve optimal size. The design process is verified by extensive simulations. In this paper, the influence of battery bank cost, rated power limits of PV and BESS, and prime rating capability of DiGs on the optimum size of PV and BESS are studied in detail. In the microgrid, the BESS location is determined by considering total system loss and voltage profile of the buses.

II. Hybrid Microgrid Components

The simplified configuration of the hybrid PV/BESS/DiGs microgrid to be set-up in the case study remote community is shown in Fig. 1. In this model, the load demands are lumped together and represented as a single load ($P_L(t)$). The

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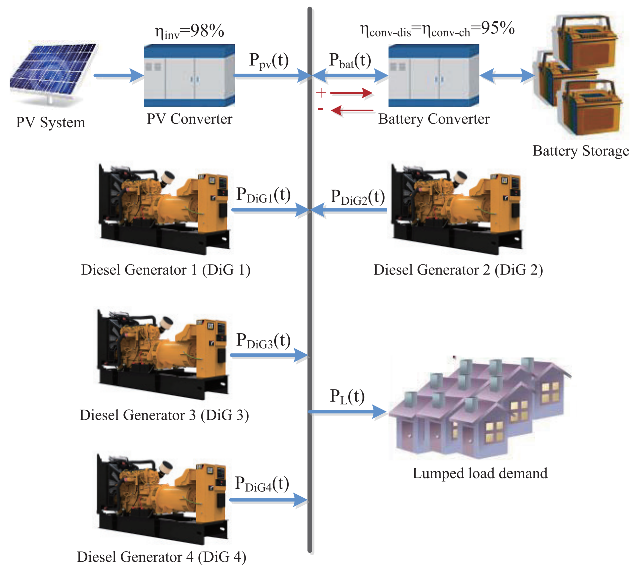


Fig. 1. Simplified configuration of the desired hybrid PV/BESS/DiGs microgrid on a remote site in Northern Canada.

microgrid components are studied and modeled as follows.

A. Photovoltaic (PV) System

The output power of PV module is obtained using (1) [30]-[32], which is multiplied by N (the number of PV modules) for PV system output power ($P_{pv}(t)$) calculation:

$$P_{pv\text{-}module}(t) = \eta_{pv}(t) \times A_{pv} \times E(t) \tag{1}$$

where $\eta_{pv}(t)$ is the instantaneous efficiency of PV module, A_{pv} is the area of each PV module in m^2, and $E(t)$ is the total solar irradiance in W/m^2. In this model, the instantaneous efficiency of PV module is obtained by:

$$\eta_{pv}(t) = \eta_{pv\text{-}ref} \times \eta_{MPPT} \times [1 - \beta \times (T_c(t) - T_{c\text{-}ref})] \tag{2}$$

where $\eta_{pv\text{-}ref}$ is the PV module reference efficiency, η_{MPPT} is the Maximum Power Point Tracking (MPPT) efficiency (assumed to be 1), β is the temperature coefficient of efficiency, $T_c(t)$ is the PV cell temperature in °C, and $T_{c\text{-}ref}$ is the PV cell reference temperature. In (2), the PV cell temperature can be obtained by:

$$T_c(t) = T_a(t) + [(NCOT - 20) / 800] \times E(t) \tag{3}$$

where $NCOT$ is the normal cell operating temperature and $T_a(t)$ is the ambient temperature in °C. In the PV model (1), the total solar irradiance ($E(t)$) has three different components:

$$E(t) = E_b(t) + E_d(t) + E_r(t) \tag{4}$$

where $E_b(t)$ is the direct radiation, $E_d(t)$ is the sky diffuse radiation, and $E_r(t)$ is the ground reflected radiation. In this paper, details on the model of $E(t)$ and PV module are obtained from [30] and [33].

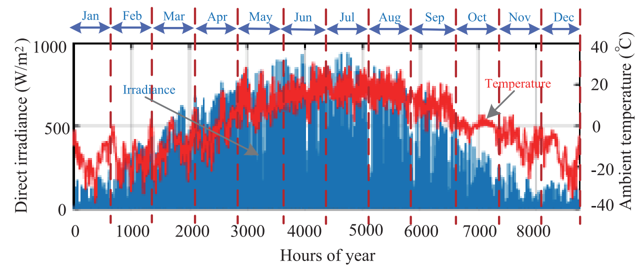


Fig. 2. Yearly direct irradiance and ambient temperature data of the site with hourly intervals.

Considering the model of PV system, the inputs of this mathematical model are the direct irradiance on the solar module ($E_b(t)$) and the ambient temperature ($T_a(t)$) on the site, as shown in Fig. 2 with hourly intervals. Data analysis reveals average values of irradiance and ambient temperatureto be 129.72 W/m^2 (standard deviation 202.63 W/m^2) and 0.98 ℃ (standard deviation 14.02 ℃), respectively.

B. Battery Energy Storage System (BESS)

The battery banks' State of Charge (SOC) should be bounded in order to protect them against damage and prolong their lifetime [34], [35]. The SOC of battery bank at hour t depends on previous SOC value at hour $t-1$. In (5), available energy of battery bank at hour t is presented [34]-[36]:

$$C_B(t) = C_B(t-1) \times (1-\sigma) + P_{bat}(t) \times \Delta t \tag{5}$$

where $C_B(t)$ and $C_B(t-1)$ are the available capacity of battery banks at hour t and $t-1$, σ is the battery self-discharge rate, $P_{bat}(t)$ is the battery power at hour t, and Δt is the time step (in this paper, it is an hour). In this study, Lithium-Ion battery with nominal capacity of 15 kWh for an individual battery bank will be used, in which the constraints on its SOC are considered as follows:

$$C_{B\text{-}min} = 10\% \times 15\ kWh = 1.5\ kWh \tag{6}$$

$$C_{B\text{-}max} = 100\% \times 15\ kWh = 15\ kWh \tag{7}$$

where $C_{B\text{-}min}$ and $C_{B\text{-}max}$ are the minimum and maximum allowable energy levels of battery bank during discharging and charging modes, respectively. All energy level values must be multiplied by the number of battery banks N_{bat}. Here, the battery banks charging and discharging efficiencies are both 97%, resulting in roundtrip efficiency (DC-to-storage-to-DC energetic efficiency, or fraction of storage energy that can be retrieved) of 95%.

C. Diesel Generators (DiGs)

To use the DiGs in acceptable efficiency range, they must operate above a minimum output value [37]. In (8), optimum operating range for the individual DiG is provided:

$$30\% \times P_{DiG\_R} \le P_{DiG}(t) \le 90\% \times P_{DiG\_R} \tag{8}$$

where $P_{DiG}(t)$ is the individual DiG's power and P_{DiG_R} is the rating power, which is 1.145 *MW* for each DiG on the site.

D. Load Demand

As mentioned, the overall community load is lumped and represented as a single load (the site load demand data for a year will be shown in Fig. 6). After analyzing data, it is concluded that the average of load demand is 1.4688 *MW* (standard deviation 0.3318 *MW*), and the minimum and maximum are 0.8177 *MW* and 2.4536 *MW*, respectively.

III. Dispatch Strategy of Hybrid PV/BESS/DiGs Microgrid

The objective of dispatch strategy is to match the load demand and the PV, BESS, and DiGs production. In general, the most important function is the BESS charging strategy. There are two main strategies [38]:

- Load Following Control Strategy (LFCS): In this strategy, the BESS is just charged when free energy is available. This control strategy is usually used when renewable power sources penetration is high enough (excess/free energy is high enough).
- Cycle Charging Control Strategy (CCCS): In this strategy, whenever it is possible, the BESS is charged to its predefined set-point state of charge (by free energy or by increasing the power of DiGs). This control strategy is mainly used when renewable power sources penetration is not high enough. Although the CCCS imposes additional fuel costs to the DiGs for charging the BESS, it reduces the amount of time the battery bank spends at a low state of charge. It also tends to reduce the number of DiGs' start-up and the number of battery charge-discharge cycles that occur throughout the year. Thus, it can be cost-effective.

In this study, since the maximum PV power limit is not high enough (1.5 *MW* – to be discussed later), the CCCS is a better option. Also, the study of annual system cost and monthly system cost of both LFCS and CCCS have confirmed the cost-effectiveness of CCCS in this case study system.

Fig. 3 shows the flowchart of dispatch strategy used in this study. The outcome of this strategy is the output powers of DiGs and BESS, and the amount of excess power and unmet load demand at hour *t*. It is worth to mention again that the time step in this paper is an hour.

The PV system always tracks its maximum power point (MPP). The PV system output power is assumed constant during each Δt. The BESS is discharged to reduce the number of DiGs start-ups and the system total cost (see $\oplus$ in Fig. 3). The BESS is charged whenever enough power can be provided (see $\ominus$ in Fig. 3). On the DiGs operation, their operating powers should be within their minimum and maximum powers range. The DiGs are started-up sequentially

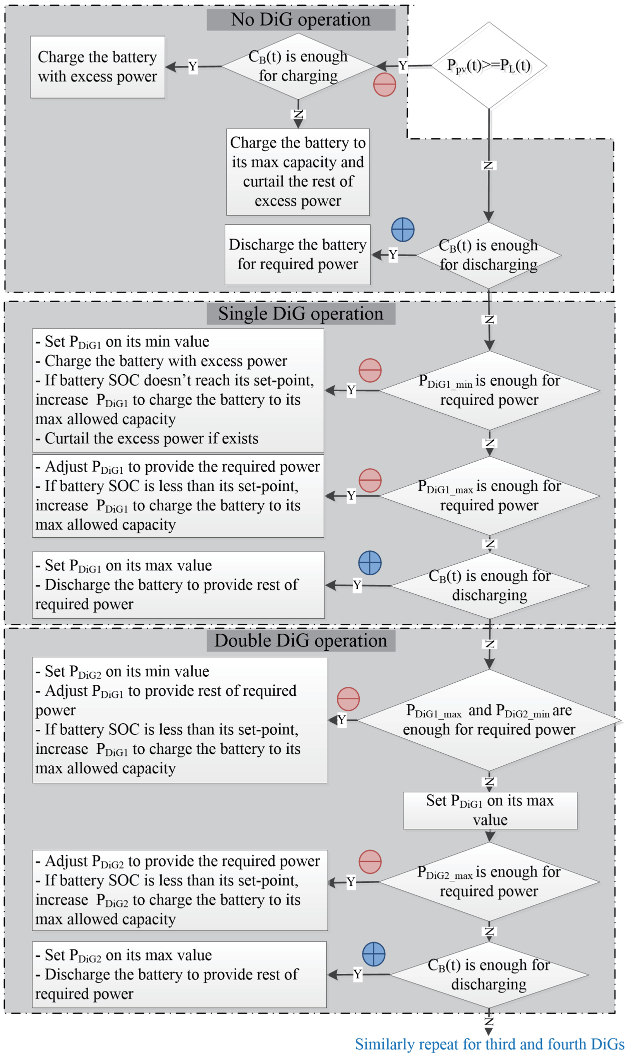


Fig. 3. Flowchart of dispatch strategy of the hybrid PV/BESS/DiGs microgrid.

when the output power of PV and running DiGs, along with BESS maximum discharge power cannot meet load demand.

IV. Optimal Sizing of PV and BESS

This section defines the objective function to address the optimal size of PV and BESS and presents simulation results.

A. Objective Function

The objective function minimizes the Annual System Cost (ASC), to best benchmark the cost analysis. The ASC includes Annual Capital Cost (ACC), Annual Operation Maintenance Cost (AOMC), Annual Replacement Cost (ARC), Annual Fuel Cost (AFC) of the DiGs, and Annual Emission Cost (AEC) of the DiGs. In the ASC calculations, the PV modules, the PV inverters, the battery banks, the battery converters, and the diesel generators are considered. In (9), the ASC is presented:

TABLE I
Parameter Values Used for ACC Calculation

Parameters	Values
Cost of diesel generators	$0/kW
Cost of PV system including module, converter, and installation	$3/kW
Cost of BESS including battery, converter and installation	1. $1350/kWh 2. $1800/kWh 3. $3733/kWh
Annual inflation rate	2%
Nominal loan interest rate (nominal discount rate)	8%
Project lifetime	20 years

$$ASC = ACC + AOMC + ARC + AFC + AEC + ADC \quad (9)$$

The following describes the aforementioned annual costs [30], [34], [36]-[40]. The parameter values have been provided by the owner and operator of the off-grid microgrid studied in this paper.

1) Annual Capital Cost (ACC)

The ACC of each component is calculated using (10).

$$ACC = C_{cap} \times CRF\,(i, y) \quad (10)$$

where C_{cap} is the each component capital cost in \$, y is the project lifetime in year, CRF is the capital recovery cost (a ratio used to calculate the present value of an annuity, a series of equal annual cash flows) and i the is real interest rate (or called real discount rate). The calculations of CRF and i are presented in (11) and (12).

$$CRF(i, y) = \frac{i \times (1+i)^y}{(1+i)^y - 1} \quad (11)$$

$$i = \frac{(i' - f)}{(1+f)} \quad (12)$$

where i' is the nominal loan interest (or nominal discount rate) and f is the annual inflation rate. TABLE I lists parameters used for the ACC calculation of each component in this paper.

2) Annual Operation Maintenance Cost (AOMC)

The operation maintenance cost calculations use the parameters shown in TABLE II. Based on these parameters, the AOMC of different components are:

$$AOMC_{DiG} = 0.03201(\$/kW/h) \times P_{DiG_R}\,(kW) \times \text{operation hours}\,(h/yr) \quad (13)$$

$$AOMC_{PV\text{-}System} = 35(\$/kW/yr) \times P_{pv\text{-}module\text{-}nominal}\,(kW) \times N_{PV} \quad (14)$$

$$AOMC_{BESS} = 0.02(1/yr) \times C_{cap\text{-}BESS}(\$/kWh) \times 15(kWh) \times N_{bat} \quad (15)$$

TABLE II
Parameter Values Used for AOMC Calculation

Parameters	Operation Maintenance Cost
Diesel generators	$0.03201/kW per hour
PV system including module and converter	$35/kW per hour
BESS including battery & converter	2% per hour

3) Annual Replacement Cost (ARC)

The ARC is the annual cost for replacing components during project lifetime. Considering components' lifetime, only the BESS (batteries and converters) need to be replaced. The ARC of BESS will be:

$$ARC = C_{rep} \times CRF\,(i, y) \times f_d\,(i, N) \quad (16)$$

where C_{rep} is the BESS replacement cost in \$, and f_d is the interest factor. The interest factor (f_d) is a ratio used to calculate the present value of a cash flow that occurs in any year of the project lifetime, which is calculated using (17).

$$f_d(i, N) = \frac{1}{(1+i)^N} \quad (17)$$

where N is the BESS lifetime. In this paper, C_{rep} is considered the same as C_{cap} for the BESS, and the lifetime is 15 years.

4) Annual Fuel Cost (AFC)

The AFC of each DiG is calculated as follows:

$$AFC = C_f \times \sum_{t=1}^{8760} F(t) \quad (18)$$

where C_f is the fuel cost per liter and $F\,(t)$ is the hourly fuel consumption in \$/h. The $F\,(t)$ is calculated for each DiG as:

$$F(t) = a \times P_{DiG}\,(t) + b \times P_{DiG\_R} \times S\,(t) \quad (19)$$

where $P_{DiG}\,(t)$ is the DiG generated power in kW, P_{DiG_R} is the DiG rated power in kW, and $S\,(t)$ is the state of DiG, which is zero when not running, and one when running. The dispatch strategy determines the $P_{DiG}\,(t)$ of each DiG. In (19), a and b are obtained from the diesel engine's fuel consumption curve versus its generated power. Based on data of fuel consumption of the existing DiGs in the case study microgrid and using curve fitting of MATLAB software, the a and b are calculated as 0.2167 and 0.0269, respectively.

Since the AFC can be a representation of carbon emission, its minimization not only reduces the cost of fuel but also the pollutant emission to the atmosphere. In this paper, C_f is considered as \$1/*Liter*.

5) Annual Emission Cost (AEC)

The carbon emission and its penalty are considered in this study. The AEC is the annual cost to capture carbon emission generated by the diesel generators. For each DiG, the AEC is calculated as follows:

$$AEC = \sum_{t=1}^{8760} \frac{E_f \times E_{cf} \times P_{DiG}(t)}{1000} \quad (20)$$

where E_f is the emission factor in kg/kWh, and E_{cf} is the emission cost factor in $\$/ton$. The E_f of DiGs on the site is 0.634 kg/kWh, and E_{cf} is assumed to be $\$30/ton$ (E_{cf} is referred to carbon tax, which has been effective on Jan. 1, 2017 in Alberta with the price of $\$20/ton$. The price has been raised to $\$30/ton$ on Jan. 1, 2018).

B. Constraints

The practical constraints of the optimization problem can be divided into configuration constraints and operation constrains. The configuration constraints are the maximum number of PV modules (N_{pv_max}) and battery banks (N_{bat_max}). In this paper, the maximum amount of PV power and battery banks were set at 1.5 MW and 750 kWh due to budget constraints. Since the 340 W PV modules and 15 kWh battery banks are assumed, N_{pv_max} and N_{bat_max} are 4412 and 50.

The operation constraints are the balance of generated and consumed power, the constraint on the energy level of BESS, and the optimum operating condition of DiGs. All these operation constraints are addressed in the dispatch strategy, and are reviewed as:

$$\sum_{j=1}^{4} P_{DiG_j}(t) + P_{pv}(t) + P_{bat}(t) = P_L(t) \quad (21)$$

$$C_{B\_min} \le C_B(t) \le C_{B\_max} \quad (22)$$

$$30\% \times P_{DiG\_R_j} \le P_{DiG_j}(t) \le 90\% \times P_{DiG\_R_j} \quad j = 1, \dots, 4 \quad (23)$$

C. Simulation Results

The components of hybrid microgrid are modeled in MATLAB software, and the optimization problem is solved to achieve the optimal number of PV modules and battery banks. T he influences of 1) battery bank cost, 2) PV and BESS maximum powers limits, and 3) prime rating control of the DiGs on optimization results are also studied.

1) Results Under Different Battery Bank Cost

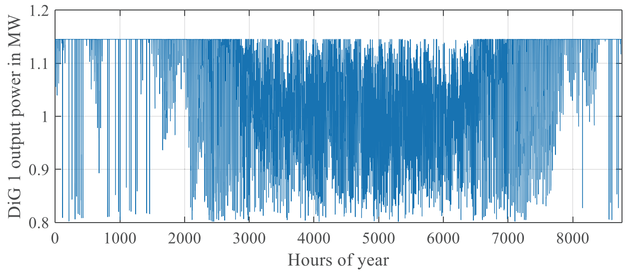
TABLE III presents the simulation results, which include the optimal number of PV modules and battery banks, the minimum value of ASC, and the operation information of power sources under different BESS costs. The results suggest maximizing the amount of PV modules (P_{pv_max}=1.5 MW) for optimal operation for all BESS costs. However, increasing the BESS cost results in decreasing number of battery banks. From the results, the installation of PV system and BESS decrease the Annual System Cost (ASC).

The results also suggest that the higher the number of battery bank, the lower the operating hours of DiGs. This is expected since the BESS tends to reduce the number of DiGs' start-ups, which leads to reduced DiGs operating hours (when the BESS optimal size is large enough, the third diesel generator is not running). When a DiG is running, its output power is increased to charge the BESS if needed (since the BESS is controlled under CCCS). That's why the annual energy production of the first DiG is increased when the higher amount of BESS is installed. About the second DiG, since its number of start-ups (and as a result, its operation hours) is reduced drastically by the BESS installation (e.g. from 7427h under no battery installation to 4201h under the installation of 315 kWh battery banks), its energy production is also reduced. Under the proposed Cycle Charging Control Strategy (CCCS), DiGs are not started-up exclusively to charge the battery, and only the already running DiGs are used.

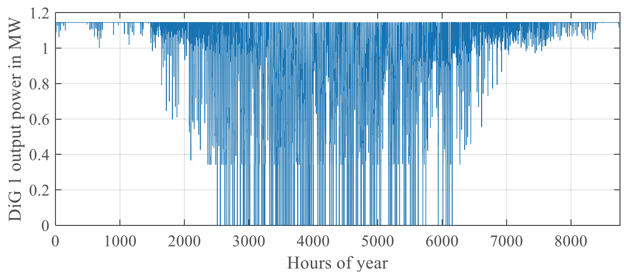
TABLE III
RESULTS OF OPTIMIZATION UNDER DIFFERENT BATTERY BANK COST (P_{pv_max}= 1.5 MW AND P_{bat_max}= 750 kWh)

Parameters		Values			
BESS cost (Converter+batt.)		No PV-Batt	\$ (1350) /kWh	\$ (1800) /kWh	\$ (3733) /kWh
Annual overall load energy		13182 MWh	13182 MWh	13182 MWh	13182 MWh
Optimal number of PV modules		0 (0W)	4412 (1.5 MW)	4412 (1.5 MW)	4391 (1.49 MW)
Optimal number of battery banks		0 (0Wh)	21 (315 kWh)	14 (210 kWh)	0 (0 Wh)
Annual System Cost (ASC)		\$4.2021M	\$3.9951M	\$4.0129M	\$4.0325M
DiG 1	Annual hours	8760h	8506h	8577h	8699h
	Annual energy	9348 MWh	8726 MWh	8647 MWh	8377 MWh
	Annual fuel	2.295 ML	2.153 ML	2.138 ML	2.083 ML
DiG 2	Annral hours	7427h	4201h	4487h	5346h
	Annual energy	3818 MWh	2456 MWh	2536 MWh	2821 MWh
	Annual fuel	1.0561 ML	0.6617 ML	0.6879 ML	0.7760 ML
DiG 3	Annual hours	44h	0h	2h	43h
	Annual energy	15.114 MWh	0 Wh	0.6870 MWh	14.77 MWh
	Annual fuel	4630.4 L	0 L	210.47 L	4525.2 L
Batt	Annual energy charge	0 Wh	161.2 MWh	84.66 MWh	0 Wh
	Annual energy discharge	0 Wh	156.57 MWh	81.37 MWh	0 Wh
PV	Annual energy	0 Wh	2042 MWh	2042 MWh	2032 MWh
	% of annual load	0%	15.5%	15.5%	15.4%

Fig. 4 and Fig. 5 show output power of the first and the second DiGs without the PV and BESS installation, and with

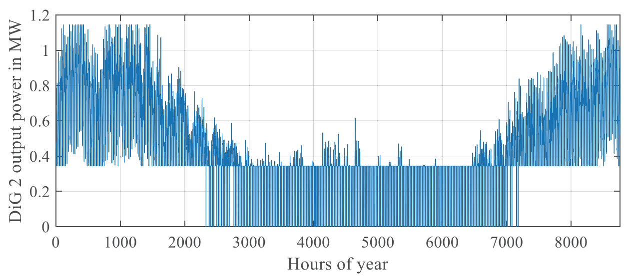


(a)

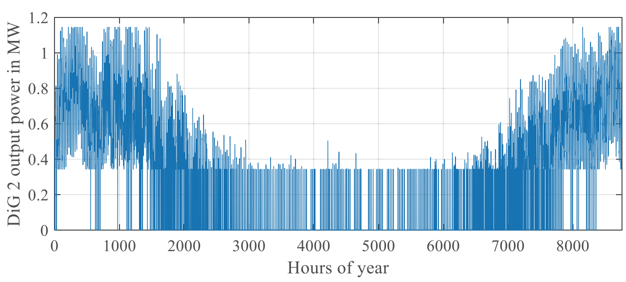


(b)

Fig. 4. Output power of the first DiG; (a) without PV & BESS installation, and (b) with the optimized PV and BESS installation, $C_{cap\text{-}bat}$ = \$1350/ kWh, $P_{bat\text{-}opt}$ = 315 kWh, and $P_{PV\text{-}opt}$ = 1.5 MW.



(a)



(b)

Fig. 5. Output power of the second DiG; (a) without the PV & BESS installation, (b) with optimized PV & BESS installation, $C_{cap\text{-}bat}$ = \$1350/kWh, $P_{bat\text{-}opt}$ = 315 kWh, and $P_{PV\text{-}opt}$ = 1.5 MW.

the optimized PV and BESS installation ($P_{bat\text{-}opt}$ = 315 kWh and $P_{PV\text{-}opt}$ = 1.5 MW under $C_{cap\text{-}bat}$ = \$1350/kWh). The results confirm that the PV and BESS installation reduce the operation hours of the first and the second DiGs, especially in the summer season when the output power of PV system is high, and the load demand is low. Also, the second DiG should operate most of the time when the PV and BESS are

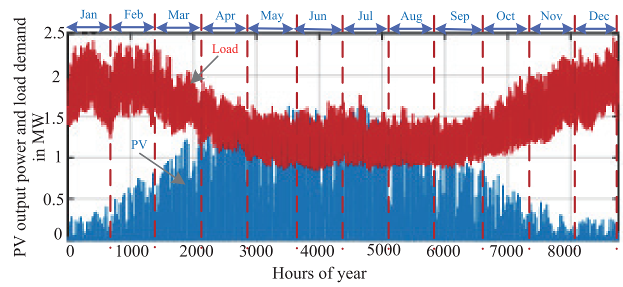
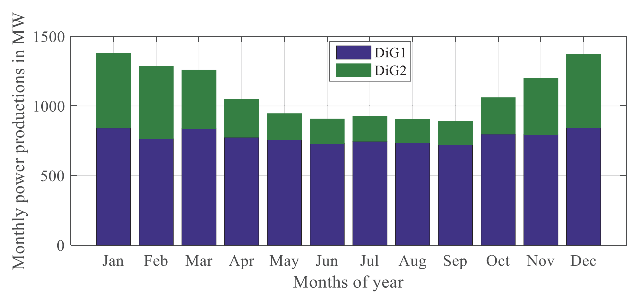
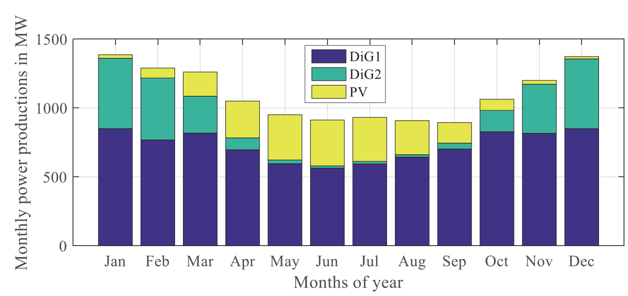


Fig. 6. Yearly load demand and PV system power production on the site.



(a)



(b)

Fig. 7. Monthly power production of the power sources; (a) without the PV & BESS installation, (b) with optimized PV & BESS installation, $C_{cap\text{-}bat}$ = \$1350/kWh, $P_{bat\text{-}opt}$ = 315 kWh, $P_{PV\text{-}opt}$ = 1.5 MW.

not installed (especially in the winter season, when the load demand is high). Fig. 6 shows the yearly load demand power and the PV system produced power ($P_{pv\_nominal}$ = 1.5 MW).

For clear illustration of the output powers of different power sources during the months of a year, monthly power productions of the first and second DiGs and the PV system are shown in Fig. 7, without the PV and BESS installation and with the optimized PV and BESS installation ($C_{cap\text{-}bat}$ = \$1350/kWh). One main point from the results is that in the presence of PV system in the summer season (when PV output power is large enough), the high portion of load demand is supplied by a single DiG and the PV source. However, in the winter season, due to PV source's small output power, the two DiGs are the major power sources.

In Fig. 8, different elements of the ASC function (ACC, AOMC, ARC, AFC, and AEC) are shown. As shown in the figure, the installation of PV and BESS reduce all the cost components except the ACC and ARC (due to the PV and BESS purchasing). Also, the AFC, AOMC, and ACC are the top three expensive cost components of the ASC. Moreover,

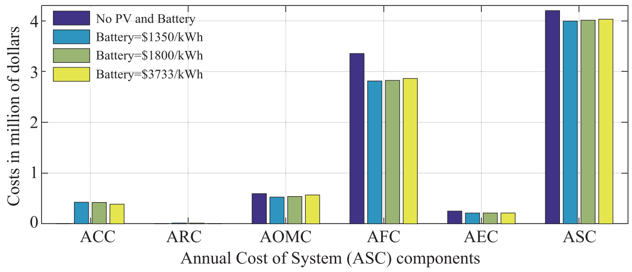


Fig. 8. Different elements of the ASC under optimal PV and battery size.

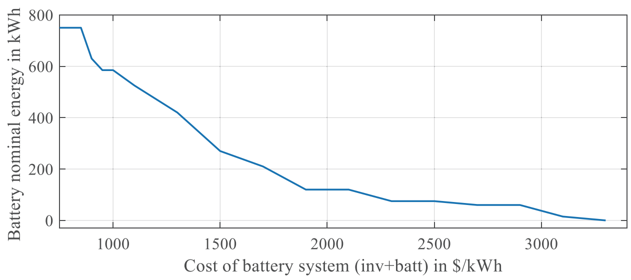


Fig. 9. Optimal size of the BESS under different battery bank costs.

TABLE IV
Evaluation of PV and Battery Maximum Limits Increase on the Optimization Results; $P_{pv\_max} = 5\ MW$, $P_{bat\_max} = 4\ MWh$

Parameters	Values	
BESS cost	\$1350/*kWh*	\$1800/*kWh*
Annual overall load energy	13182 *MWh*	13182 *MWh*
Optimal # of PV modules	6163 (2.095 *MW*)	6160 (2.095 *MW*)
Annual PV energy production	2852 *MWh*	2851 *MWh*
Optimal # of battery banks	27 (405 *kWh*)	16 (240 *kWh*)
Annual DiGs operation hours	11615*h*	12144*h*
Annual DiGs fuel consumption	2.6365 *ML*	2.6540 *ML*
Annual DiGs capital maintenance cost	\$0.42571 *M*	\$0.44510 *M*
Annual System Cost (ASC)	\$3.9566 *M*	\$3.9768 *M*

the AOMC goes down when larger BESS is installed (since it depends on the operation hours of the DiGs). Since the AFC of diesel generators depend on their energy production, they have the same variation pattern as the DiGs' energy production under different BESS costs (explained earlier for TABLE III). The variation of the AEC and the AFC are also similar under different battery bank cost since the AEC depend on the fuel consumption.

Considering the above discussions, it is important to clarify how the BESS cost influence the optimization results. An increase in the BESS cost reduces the optimal battery size. Fig. 9 shows the optimal size of BESS under different battery bank costs. When the BESS cost (including the battery and converter costs) goes higher than \$900/*kWh*, the optimal size starts to decrease from its maximum limits (750 *kWh*), and when it reaches \$3450/*kWh*, the optimization converges to zero number of battery bank. Note that this optimization only considers the ASC minimization. In practice, for the PV power smoothing control, the minimum amount of BESS is still required.

TABLE V
Evaluation of Enabling DiGs Prime Rating on Optimization Results (P_{pv_max}= 1.55 MW, P_{bat_max}= 750 KWh)

Parameters	Values	
BESS cost	\$1350/*kWh*	\$1800/*kWh*
Annual overall load energy	13182 *MWh*	13182 *MWh*
Optimal # of PV modules	4412 (1.5 *MW*)	4410 (1.5 *MW*)
Annual PV energy production	2042 *MWh*	2042 *MWh*
Optimal # of battery banks	18 (270 *kWh*)	4 (60 *kWh*)
Annual DiGs operation hours	12297*h*	12924*h*
Annual DiGs fuel consumption	2.8037 *ML*	2.8250 *ML*
Annual DiGs captial maintenance	\$0.45070 *M*	\$0.47368 *M*
Annual Capital Cost (ACC)	\$0.42009 *M*	\$0.39776 *M*
Annual Replacement Cost (ARC)	\$0.01335 *M*	\$3956 *M*
Annual Operation Maintenance Cost (AOMC)	\$0.51050 *M*	\$0.52832 *M*
Annual Fuel Cost (AFC)	\$2.8037 *M*	\$2.8250 *M*
Annual Emission Cost (AEC)	\$0.21284 *M*	\$0.21302 *M*
Annual System Cost (ACS)	\$3.9605 *M*	\$3.9681 *M*

2) Results Under Increased Maximum Power Limits of PV and Battery

To evaluate the influence of maximum power limits of PV system and BESS on the optimization problem, they are increased into P_{pv_max} = 5 *MW* and P_{bat_max} = 4 *MWh*. TABLE IV provides the simulation results for two different BESS costs, \$1350/*kWh* and \$1800/*kWh*. TABLE III and TABLE IV allow drawing the following conclusions:

- The optimal PV system size is 2.095 *MW*.
- Since the optimal size of PV system is increased from 1.5 *MW* to 2.095 *MW*, the DiGs operation hours and their fuel consumptions are reduced.
- The optimal size of BESS increases when higher limits are allowed.
- Although the optimal size of PV and BESS are increased under higher maximum limits, the ASC reduces.

3) Results Under Diesel Generators Prime Rating Enabled

The DiGs under study can have their maximum output power increased from 1145 *kW* to 1280 *kW* for the maximum of 8 hours each day. This is called prime rating. Applying this capability provides different results, which are shown in TABLE V for the BESS costs of \$1350/*kWh* and \$1800/*kWh*. From the table, enabling the prime rating capability provides the smaller amount of optimal BESS. This is reasonable since the purpose of prime rating is to reduce the number of DiG start-ups, like the BESS control target. Also, since the purposes of prime rating of DiGs and the BESS installation are the same, the DiG operation hours and fuel consumptions are similar with and without prime rating consideration. The results suggest that the ASC is lower with the prime rating enabled than without it, since the BESS are expensive.

D. Discussions

The results presented in this section suggest that:

- In each microgrid, there is an optimum amount of PV power that minimizes the annual system cost, and the higher PV power installation cannot guarantee the lower ASC.
- The optimal size of BESS directly depends on its capital costs. Increasing the BESS cost leads to the smaller optimum size of BESS.
- Since the BESS reduces the number of DiG start-ups, a larger BESS size leads to fewer operation hours of the DiGs.
- The PV system and the BESS installation reduce all the ASC components except the ACC and ARC (due to the PV and battery initial costs).
- The Annual Fuel Cost (AFC) of diesel generators, the Annual Operation Maintenance Cost (AOMC), and the Annual Capital Cost (ACC) are the most expensive cost components of the ASC.
- Since the Annual Operation Maintenance Cost (AOMC) of diesel generators depend on their operation hours, it goes down when larger amount of the BESS is installed.
- Since the Annual Fuel Cost (AFC) of DiGs depends on their energy production, it will go down in the presence of PV and BESS.
- The diesel generators are the most expensive components of hybrid microgrid. Their costs go beyond that of an engine and alternator. The cost of building, fuel storage tank, and maintenance must also be considered.
- Enabling the prime rating capability of DiGs results in smaller optimal size of the BESS since it takes the BESS responsibility in reducing the number of DiGs start-ups.

V. Allocation of the PV and BESS

In this study, the installation location of PV system was determined by land acquisition limitations. As a result, only the battery bank allocation is addressed. Two objectives are included in the optimization problem: 1) the total loss of system, and 2) the voltage profiles of nodes. The microgrid under study was modeled in CYME software and its Long-Term Dynamic module (this module offers a time-series simulation tool). Six nodes suitable for the BESS installation were selected first. Then, the Long-Term Dynamic simulation is run for a year, with the BESS sited in each selected node. The output active and reactive powers of DiGs, PV system, and BESS, as well as the voltage profiles of all nodes are monitored to choose the best node among candidates. Fig. 10 shows the simplified schematic of the case study with the six selected locations for the BESS installation.

A. BESS Allocation Considering System Total Power Loss

The simulation results are provided in TABLE VI. The results allow us to conclude that when the BESS is placed close to the diesel generators (locations #1 to #3), the output active and reactive powers of DiGs as well as the total loss of system are smaller than in all other cases. As a result, they

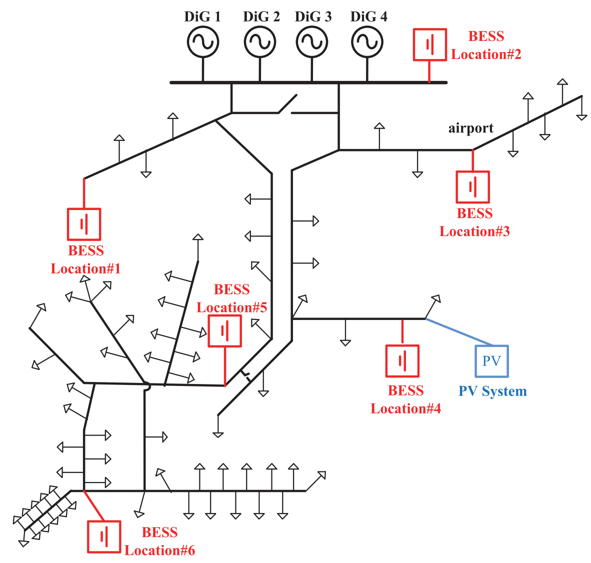


Fig. 10. Simplified schematic of the case study site in Northern Canada and the six selected locations for the BESS installation.

TABLE VI
Simulation Results From Cyme When Battery Banks Are Placed in 6 Chosen Locations

BESS Locations	Annual First and Second DiGs Energy Production		Annual Loss of System (W)
	Active	Reactive	
#1	11290 *MWh*	1322 *MVarh*	183,314,200
#2	11289 *MWh*	1315 *MVarh*	182,157,500
#3	11293.7 *MWh*	1324.4 *MVarh*	187,264,100
#4	11293.9 *MWh*	1324.5 *MVarh*	187,439,300
#5	11295 *MWh*	1324.9 *MVarh*	188,426,600
#6	11296 *MWh*	1325 *MVarh*	189,849,600

are good candidates for placing the BESS.

B. BESS Allocation Considering Voltage Profile of Nodes

Here, the voltage profiles of nodes are considered for the allocation of BESS. In the study, the “worst downstream under-voltage” and “worst downstream over-voltage” during a year are identified. TABLE VII and TABLE VIII present the simulation results for the worst downstream under-voltage and over-voltage when the BESS are placed in the six different sites. The results allow us to conclude that installing the BESS near loads (locations #4, #5 and #6) could increase the under-voltages in the system and could produce large over-voltages. Since all the worst under-voltages are in the acceptable range (higher than 95%), it is better to place the BESS close to the diesel generators (locations #1, #2, or #3) to reduce the worst over-voltages. As an example, the worst downstream over-voltage when the BESS is placed in location#1 and in location#6 are shown in Fig. 11 and Fig. 12, which verify the above discussions.

Through the above study, we found that it is recommended to allocate the BESS close to the diesel generators to reduce 1) the system total power loss, 2) the diesel generators output active and reactive powers, and 3) the worst downstream over-voltages.

TABLE VII
DATA ANALYSIS OF WORST DOWNSTREAM UNDER-VOLTAGES DURING A YEAR IN PERCENT, ACHIEVED FROM CYME

BESS Location	Min	Max	Ave.	Stand. Deviation
#1	96.30%	100.05%	98.4136%	0.7747%
#2	96.30%	100.05%	98.4137%	0.7751%
#3	96.37%	100.03%	98.4088%	0.7740%
#4	96.53%	100.10%	98.4013%	0.7984%
#5	96.55%	100.10%	98.3958%	0.8108%
#6	96.56%	100.10%	98.3911%	0.8240%

TABLE VIII
DATA ANALYSIS OF WORST DOWNSTREAM OVER-VOLTAGES DURING A YEAR IN PERCENT, ACHIEVED FROM CYME

BESS Location	Min	Max	Ave.	Stand. Deviation
#1	102.01%	104.52%	103.487%	0.7910%
#2	102.02%	104.64%	103.553%	0.7936%
#3	102.1%	105%	103.95%	0.8058%
#4	102.24%	105.94%	104.0141%	0.8125%
#5	102.24%	106.12%	104.0135%	0.8372%
#6	102.24%	106.28%	104.0127%	0.8612%

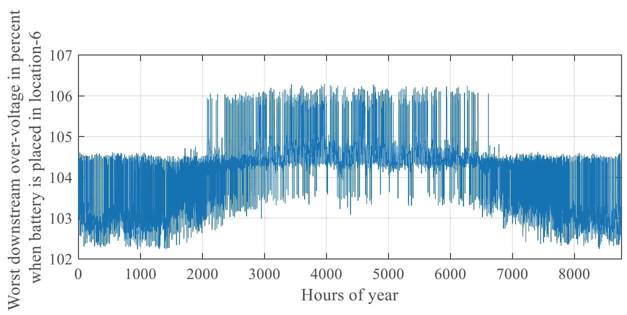


Fig. 11. Worst downstream over-voltage when the BESS is placed in location #6.

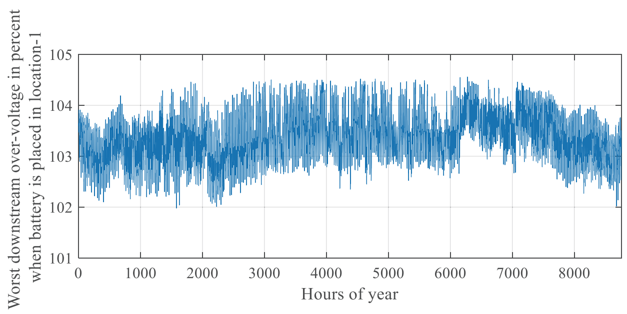


Fig. 12. Worst downstream over-voltage when the BESS is placed in location #1.

VI. CONCLUSIONS

In this paper, the design, operation, and dispatch strategy for a hybrid PV/BESS/DiGs isolated microgrid were presented. The optimal sizes of PV and BESS systems and the optimal location of the BESS were determined, and a Northern remote off-grid community in Canada was used as a case study. The Annual System Cost (ASC) was minimized as an objective function to determine the optimal sizes of PV system and BESS. The study revealed that:

1) There is an optimum size of PV system that minimizes the ASC, and increasing the PV power installation cannot guarantee lower ASC.
2) The BESS optimal size is primarily affected by its capital cost.
3) The higher amount of BESS installation reduces the DiG start-ups, resulting in lower DiG operation hours.
4) The DiGs are the most expensive components of the microgrid.
5) The AFC, AOMC, and ACC are the top three expensive cost components of the ASC.
6) The DiG prime rating capability reduces the number of DiGs start-ups. This effect is similar to that of the BESS, thus resulting in smaller optimal size of BESS.

In this paper, the BESS was also allocated considering the system total power loss and voltage profiles of the nodes. The results revealed that installation of the BESS close to the DiGs leads to smaller power loss, DiGs output active and reactive powers, and worst downstream over-voltages. The results of the paper can be generalized to similar isolated microgrids.

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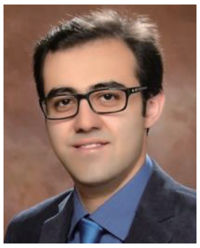

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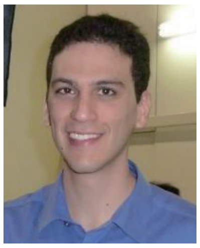

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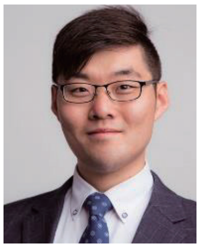

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Decentralized Coordination Power Control for Islanding Microgrid Based on PV/BES-VSG

Meiqin Mao, Cheng Qian, and Yong Ding

***Abstract*—Virtual synchronous generator (VSG) technology for integration of distributed energy resources attracts increasing attentions for its enabling inverters to simulate the inertia and damping characteristics of synchronous generators and improve the stability of the system. In this paper, a decentralized VSG-based adaptive coordinated control strategy is proposed for islanding microgrids consisting of photovoltaic generators combined with battery energy storages in DC side (PV/BES-VSG). By the proposed method, the droop characteristics of VSGs can be adaptively adjusted according to the DC bus voltage. In this way, the local controllers of PV/BES-VSG units can switch operating modes automatically without the need of a central controller, so that the power sharing among PV/BES-VSG units is allocated according to the maximum output power of PVs and the limit of charging/discharging power of BES instead of merely rated capacity of the inverters. To test the proposed method, an islanding model of microgrid with two PV/BES-VSG units in parallel is built in Matlab/Simulink. The simulation results show that by the proposed control strategy, the coordination control between PV and BES, and between PV/BES-VSG units can be effectively realized with maximum use of PV power under the premise of the rational distribution of power.**

***Index Terms*—Decentralized coordination control, power sharing, PV/BES-VSG unit, virtual synchronous generator.**

I. Introduction

As one of renewable energy sources (RESs), photovoltaic (PV) generation system has been booming during last decades all over the world for its important role in solving global energy crisis and environmental problems [1], [2]. Specifically in China, by the end of 2017, the total installation of PV sreaches 130.25 GW [3], ranked the first top globally. And according to the report from IEA [1], by 2040 solar power will be the single largest source of low-carbon electricity generation, with all renewable generations accounting for 40% of the total electricity production. But, most of installed PVs are generally connected to the power system or microgrids through inverters, which provide much faster control than traditional power systems because of the application of power electronic devices and PWM control methods [4].Therefore,the total inertia of the whole power system, especially of microgrids decreases greatly with the increasing penetration of PVs, leading frequency becomes sensitive to the fluctuations in loads and renewable energy systems, and posing a great challenge to stable operation of power system [5].

To address the problem aforementioned, the concept of Virtual Synchronous Generator (VSG) is presented, by which, an inverter can be controlled to behave as traditional synchronous generator and provide enough or desired inertia for the power system [6]-[8] so that the dynamic performances of the system can be enhanced. So far, the developments of VSG for microgrids are focused on enhancing system stability [9], [10], distributed control of converters [11] for power system and power sharing in microgrids [12].

In the typical VSG systems above, battery energy storages or PV panels are used as primary energy sources for the inverters [13]. The corresponding control method may be grouped into two categories: centralized control and decentralized control. In the centralized control methods, a central energy management system (EMS) is required [14], [15], which relies on the communications between units and a central controller and may reduce the system reliability.

To reduce the reliance on communications, decentralized coordination control without communication has attracted wide attentions [16]. The droop control method without communication is usually used to realize the power sharing and energy management in the microgrid with multiple hybrid PV and battery energy storage systems. But according to the relationship between total PV power available, BES charging/discharging power limits, SOC levels and load demands, there will be a variety of operation modes. This feature of the micrgrids brings great challenges to the design of individual local controllers. In current proposed methods, each local controller in the microgrid identifies the current operation mode with accessing to local information, through a state machine method [17], or via microgrid AC bus frequency [18], [19]. In the reference [17] the control strategy mainly focuses on the power flow management between hybrid PV/BES unit and microgrid, the coordinated control of the DC-DC converters at DC side are not discussed in details. In [18], AC frequency is used to reflect Battery SOC condition, while the PV generation regulates its output power based on measured frequency to keep the frequency stable. The control strategy in [19] relies on battery energy to regulate the AC-bus frequency, the local controllers determine the operation state of each unit by the corresponding power relationship, and generate logic signals for switching operation mode. Switching error of operation mode at any unit will result in the operation failure of the microgrid. Therefore, more adaptive decentralized control methods are expected to address issues above [20], [21].

In this paper, the VSG-based inverter, together with the

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combined PV and battery energy storages (BES) hybrid unit at DC side, is defined as a PV/BES-VSG unit. And decentralized adaptive coordinated control strategy is proposed for islanding microgrid with multiple PV/BES-VSG units to keep the frequency and voltage stable meanwhile taking the most advantage of PVs. With the proposed method, the droop characteristics of VSGs can be adaptively adjusted according to the DC link voltage, and local controller for each PV/Battery-VSG unit obtains the information about the available PV power, the battery SOC, the output power of the inverter of its own unit and the microgrid frequency to switch operating states automatically. An islanded microgrid model with two PV/BES-VSG units is built in Matlab/Simulink to verify the effectiveness of the proposed control strategy.

The rest of the paper is arranged as follows. The structure and operation states of microgrid are described in Section II. The proposed control strategy is discussed in Section III. Typical operating modes analysis for PV/BES-VSG is discussed in Section IV. In Section V, the proposed method is verified by simulations in Matlab/Simulink considering various operating conditions, followed by conclusions in Section VI.

II. Structure of Microgrid with Multiple PV/BES-VSGs

A. Structure of the Microgrid

The structure of the microgrid investigated in this paper is depicted in Fig. 1. It consists of multiple PV/BES-VSG units. Each PV/BES-VSG unit contains a PV subsystem, a BES subsystem and a VSG-controlled inverter. PV subsystem includes PV array and a boost DC-DC converter. BES subsystem includes batteries and a bidirectional dc/dc converter. The PV unit and the BES unit are both connected to the DC side. The inverter adopts VSG control to supply the required power for the local loads which are represented as Z_{Load}.

B. Operating Mode Analysis of Microgrid

For the microgrid with PV/BES-VSG units shown in Fig. 1, the power flow coordination control to maintain the power balance of such a microgrid is required from three aspects:

1) Power flow management between different PV/BES-VSG units;
2) Power flow management among PV, BES and output power of the inverter in each PV/BES-VSG unit;
3) Power flow management between PV and BES in each hybrid PV/BES-VSG unit.

In practice, for the case 3), to avoid depleting the battery prematurely, battery should either stay idle or be charged when surplus power becomes available, that is, battery supplies power only when all other PV generations reach their upper limits. For the case 1) and 2), PV available power, battery conditions and the load demands should all be taken into consideration to optimize load sharing.

Considering the discussions above and depending on maximum output PV power available, charging power ratings of the batteries and the load demands, the operation states of the microgrid can be grouped in four main states as follows.

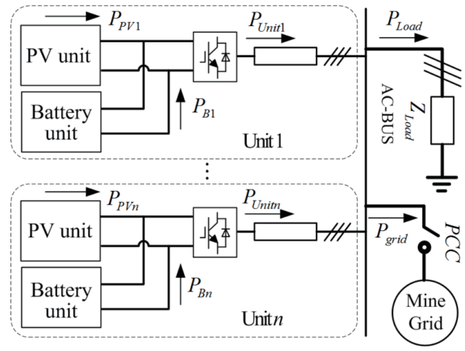

Fig. 1. Structure diagram of the researched microgrid.

State I: The total PV maximum power is larger than the sum of the total battery charging power limits and loads, as shown in (1).

$$\sum_{i=1}^{n} P_{PV\_MPPTi} > \sum_{i=1}^{n} \left| P_{ch\_\lim i} \right| + P_{Load} \tag{1}$$

where, P_{PV_MPPTi} is PV maximum power available (under standard test condition, P_{PV_MPPTi} is equal to its peak power P_{PV_pp}); $P_{ch\_\lim i}$ is battery charging power; P_{Load} is the load power.

With the condition of (1), if each VSG is assumed to share load demands with the PV operating at maximum power point (MPP), the load power sharing coefficient η_i for i^{th} PV/BES-VSG unit can be described as in (2).

$$\eta_i = P_{PV\_MPPTi} / \sum_{i=1}^{n} P_{PV\_MPPTi} \tag{2}$$

But in this case, for each PV/BES-VSG unit, there are two possible operating states, as shown in (3) and (4), respectively.

$$\forall i \le n \ , P_{PV\_MPPTi} > \left| P_{ch\_\lim i} \right| + \eta_i P_{Load} \tag{3}$$

$$\exists i \le n \ , P_{PV\_MPPTi} < \left| P_{ch\_\lim i} \right| + \eta_i P_{Load} \tag{4}$$

In the case shown by (3), all PV generation units can produce enough power to balance the loads by sharing coefficient in (2), leading PV curtailment necessary in all PV units, and all batteries can be charged with maximum power. Meanwhile, in the case shown by (4), the maximum power of PV from the i^{th} PV/BES-VSG unit is not high enough to share the loads by the power sharing coefficient in (2) with accommodating the charging demand of its battery. In other words, if it still shares load power according to η_i, the battery charging power for i^{th} PV/BES-VSG unit needs to be reduced. However, for the whole microgrid, the maximum utilization of PV generation is not realized. Therefore, the inverter of the unit meeting in (4) has to enter in PCM (Power Controlled Mode), its output power is controlled shown as in (5).

$$P_{Uniti} = P_{PV\_MPPTi} - \left| P_{ch\_\lim i} \right| \tag{5}$$

In this way, all batteries are charged with maximum power to maximize use of PV power while curtailment of PV output power should be performed in some units to keep power balance, with rest PV units operating at MPP.

State II: The total PV maximum power is less than the sum of the total battery charging power limits and load demands, but is larger than the load demands, as shown in (6).

$$\begin{cases} \sum_{i=1}^{n} P_{PV\_MPPTi} < \sum_{i=1}^{n} \left| P_{ch\_\lim i} \right| + P_{Load} \\ \sum_{i=1}^{n} P_{PV\_MPPTi} > P_{Load} \end{cases} \tag{6}$$

With the condition of (6), all PV units operate at MPP, the batteries absorb the surplus power, and the battery charging power is related to its corresponding SOC and power rating, the load power sharing coefficient λ_i is presented as in (7).

$$\lambda_i = \left| P_{ch\_\lim i} \right| / \sum_{i=1}^{n} \left| P_{ch\_\lim i} \right| \tag{7}$$

Then, the output power of each inverter is shown in (8). It is worthy to note that the inverter output power may be negative, that means, some units with less PV power will get the power from others with more PV power.

$$P_{Uniti} = P_{PV\_MPPTi} - \lambda_i \left(\sum_{i=1}^{n} P_{PV\_MPPTi} - P_{Load} \right) \tag{8}$$

State III: The load is larger than the total PV maximum power, but is less than the sum of the total discharging power limits of battery and the total PV maximum power, as shown in (9).

$$\begin{cases} \sum_{i=1}^{n} P_{PV\_MPPTi} < P_{Load} \\ \sum_{i=1}^{n} P_{PV\_MPPTi} + \sum_{i=1}^{n} \left| P_{disch\_\lim i} \right| > P_{Load} \end{cases} \tag{9}$$

where, P_{disch_lim} is battery discharging power.

With the condition of (9), all PV units operate at MPP, the batteries will be discharged to keep power balance, and their discharging power are related to their corresponding SOC and power rating, the power sharing coefficient ξ_i is presented as in (10).

$$\xi_i = P_{disch\_\lim i} / \sum_{i=1}^{n} P_{disch\_\lim i} \tag{10}$$

Then, the output power of each inverter unit is controlled as shown in (11).

$$P_{Uniti} = P_{PV\_MPPTi} + \xi_i \left(P_{Load} - \sum P_{PV\_MPPTi} \right) \tag{11}$$

State IV: The total load is larger than the sum of the total PV-maximum power and the total battery discharging power limits, as shown in (12).

TABLE I
POWER DISTRIBUTION FOR EACH UNIT

MG Operating State	PV/BES-VSG Unit Operating State	P_{PVi}	P_{Bi}	P_{Uniti}
I	1	$P_{ch\_\lim i}+\eta_i P_{Load}$	$P_{ch\_\lim i}$	$\eta_i P_{Load}$
I	2	P_{PV_MPPTi}	$P_{ch\_\lim i}$	(5)
II	3	P_{PV_MPPTi}	$\lambda_i(\sum P_{PV\_MPPTi}-P_{Load})$	(8)
III	4	P_{PV_MPPTi}	$\xi_i(\sum P_{PV\_MPPTi}-P_{Load})$	(11)
IV	5	P_{PV_MPPTi}	$P_{disch\_\lim i}$	(13)

Note: Roman and Arabic numerals are used to distinguish the operating states of microgrid and PV/BES-VSG unit, respectively.

$$\sum_{i=1}^{n} P_{PV\_MPPTi} + \sum_{i=1}^{n} \left| P_{disch\_\lim i} \right| < P_{Load} \tag{12}$$

With the condition of (12), the whole microgrid is overloaded,with all PV units operating at MPP and the batteries discharged with the power limits.The inverter enters in PCM, and its output power is controlled as shown in (13). Then, frequency is reduced greatly. This will trigger non-critical load shedding to ensure the continuity and reliability of power supply.

$$P_{Uniti} = P_{PV\_MPPTi} + P_{disch\_\lim i} \tag{13}$$

To sum up the discussions above,from the view of the whole microgrid, there are four operating states in total, but for each PV/BES-VSG unit, there will be five operating states, as listed in TABLE I.

III. Control Strategy for Microgrid with PV/Battery-VSG Unit

A. Proposed Control Strategy

For the microgrid with PV/BES-VSG units shown in Fig. 1, the operation of each PV/BES-VSG unit can be divided into five states as shown in TABLE I. But both in state 3 and 4, the batteries are used to keep generation or consumption balance. Therefore, the two states can be merged as one state to reduce the design complexity of the controllers. Considering the operation characteristics of microgrid and PV/BES-VSG units, the operation of each PV/BES-VSG unit can be divided into four states.

To achieve the objectives aforementioned, the proposed decentralized coordination control is shown in Fig. 2. The control method consists of three subsystem controller: PV controller, ESS controller and VSG controller.

PV controller: In the PV controller shown in Fig. 2, the hysteresis comparator in the control loop is used to switch the control modes of the PV controller. PV controller collects DC-link voltage v_{dc}, comparing with reference voltage v_{dc_PVref}. If the hysteresis comparator outputs 1, PV operatsat MPP, corresponding to state 2, 3, 4 and 5, as shown in TABLE I. If the hysteresis comparator outputs 0,PV changes into VCM (voltage controlled

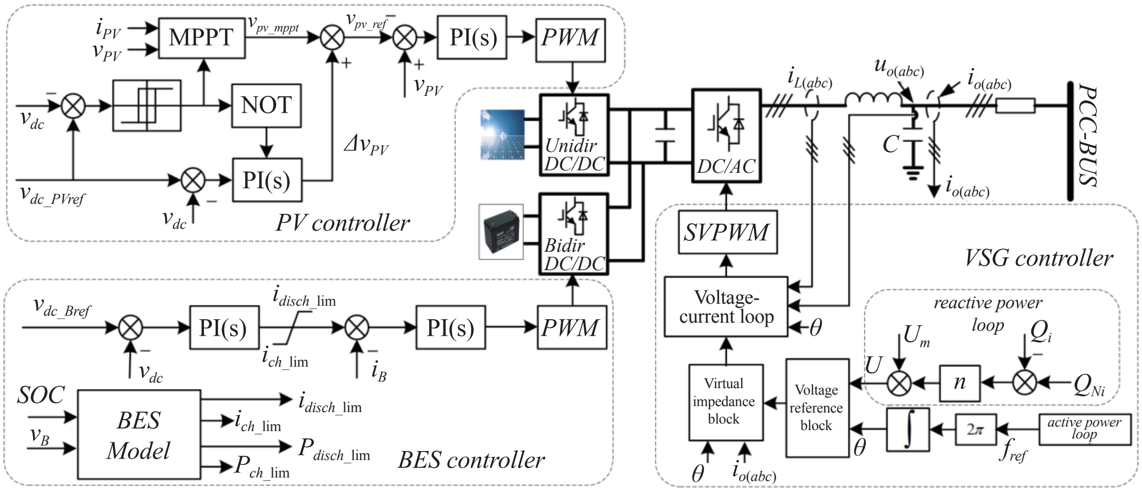

Fig. 2. Control structure of the proposed control strategy.

mode), PV output power is controlled based on output power of inverter and battery charging power, corresponding to state 1. The outer loop is DC-link voltage loop, regulating DC-link voltage. The inner loop is to control operation voltage of PV array, in which v_{PV} and i_{PV} represent PV array output voltage and PV array output current, respectively.

BES controller: BES (battery energy system) controller adopts voltage and current dual-loop control. The outer voltage loop is DC-link loop, regulating DC-link voltage. The upper and lower output limits of the following PI controller are determined by battery SOC, limiting the charging/discharging current. The inner loop is battery current loop. When the output of DC-link voltage loop reaches saturation, it indicates the battery charging/discharging current has reached the maximum value, and the current loop will limit actual charging/discharging current to the allowable range through PI controller. Under this situation, the terminal voltage of battery changes slowly, the battery enters into PCM, corresponding to the state 1, 2 and 5 in TABLE I, otherwise, it operates in VCM, corresponding to the state 3 and state 4.

The function of BES model in Fig. 2 is to obtain the maximum charging/discharging current and power limits based on battery SOC and terminal voltage v_B, where, i_{ch_lim}, P_{ch_lim} represent maximum charging current and power limits, respectively, and i_{disch_lim}, P_{disch_lim} represent maximum discharging current and power limits, respectively. v_{dc_ref} is DC-link voltage reference, i_B is battery output current. The detailed BES model is introduced in [22].

VSG controller: With reference to the simplified electrical model of synchronous generator, the swing equation of synchronous generator is added to the power loop of the inverter, and with the energy storage device, a virtual moment of inertia is produced to make it present the characteristics of a synchronous generator. The control block diagram for VSG controlled inverter (referred to as VSG) is shown in Fig. 2. It consists of three loops. The outer-loop is the power loop and contains the *ω-P* droop frequency regulation function, and the inner-loop is a typical voltage and current double loops. The drive signals are produced using SVPWM technology. In addition, since the line in low-voltage microgrid has a large resistance-to-inductance ratio, a virtual impedance control loop is introduced to decouple the active and reactive power control of the inverter with VSG and improve the power distribution accuracy between parallel VSGs [23]. This paper mainly focuses on active power sharing, so reactive power control is beyond the scope of this paper.

One of advantages by VSG control technology is that the parameters can be adjusted adaptively based on demands. However, the introduction of swing equation increases the order of the system, which leads that inverter is prone to power oscillation during transient process. Transfer function models for multiple VSG-based inverters are established to analyze dynamic response characteristics of VSGs and the influence of parameters.

ΔP_i, ΔP_{refi} are the output power variation and reference power variation of the i^{th} inverter, respectively. J_i and D_i are virtual inertia and damping coefficient of the i^{th} inverter, respectively. $\Delta\omega_i$ represents angular frequency variation of the i^{th} inverter. The small signal model of power control loop can be presented as in (14)

$$\Delta\omega_i = \frac{1}{J_i s + D_i}(\Delta P_{refi} - \Delta P_i) \tag{14}$$

The output impedance of VSG is designed to be inductive when virtual impedance control is applied, thus, the power transfer equation is

$$\Delta P_i = \frac{3}{2}\frac{E_i V}{X_i}\cos\delta_i \Delta\delta_i = k_i \Delta\delta_i \tag{15}$$

where, E_i is the amplitude of inverter output voltage, V is amplitude of PCC voltage, δ_i is phase difference between inverter and PCC, if the virtual inductance is large enough, the output reactance X_i of VSG can be replaced by virtual inductance $X_i = \omega L_{vi}$, phase difference variation $\Delta\delta_i$ can be obtained as

$$\Delta\delta_i = \frac{1}{s}(\Delta\omega_i - \Delta\omega) \tag{16}$$

where, $\Delta\omega$ represents angular frequency variation of PCC.

For the system consisting of multiple inverters, the balanced power flow should satisfy (17) when the load demands change, ΔP_{Load} is load power variation

$$\sum_{i=1}^{m} \Delta P_i = \Delta P_{Load} \tag{17}$$

Then transfer function model can be obtained based on (14) ~ (17)

$$G_{pli} = \frac{\Delta P_i}{\Delta P_{Load}} = \frac{G_i\left(J_i s + D_i\right)}{\sum\limits_{m=1}^{n} G_m\left(J_m s + D_m\right)} \tag{18}$$

where,

$$G_i = \frac{k_i}{J_i s^2 + D_i s + k_i} \;;\; (i = 1, 2, \cdots n\ ) \tag{19}$$

G_{pli} represents the influence of load on the output power of i^{th} inverter. The output power of paralleled VSG-based inverter is not only related to the load demand and its own parameters, but also affected by the parameters of other inverters.

Analyzing G_{pli}, finding that if the parameters satisfy the following relations that is given by (20), G_{pli} will become a proportional component, which is equal to γ_i. When load demand changes, the inverter output power changes proportionally without dynamic oscillation process. The conclusion is affirmed by Fig. 3, and (20) can be derived and regarded as a constraint for parameters designed.

$$J_1 : J_2 : \cdots : J_n = D_1 : D_2 : \cdots : D_n = \frac{1}{X_1} : \frac{1}{X_2} : \cdots : \frac{1}{X_n} = \gamma_1 : \gamma_2 : \cdots : \gamma_n \tag{20}$$

where, γ_i is a introduced constant and $\sum\limits_{i=1}^{n} \gamma_i = 1$

The active power control loop in VSG controller is shown in Fig. 4 in details. It includes four parts: PV-VSG, DC-link voltage regulation, battery-VSG and constant power control. They correspond to four different operation states respectively.

PV-VSG is with Part 1, responding to state 1 in TABLE I, in which, P_{Ni} represents reference power. In this part, the virtual moment of inertia J_{PVi}, damping coefficient D_{PVi} for each PV/BES-VSG unit are proportional to PV peak power $P_{PV\text{-}ppi}$, as shown in (14), α_1, α_2 are constant, and α_1>0, α_2>0.

$$\frac{J_{PVi}}{P_{PV\_ppi}} = \alpha_1, \quad \frac{D_{PVi}}{P_{PV\_ppi}} = \alpha_2 \tag{21}$$

DC-link voltage regulation is with Part 2, responding to state 2 in TABLE I, used for regulating v_{dc}, in which, v_{dc_VSGref} is the reference voltage.

Battery-VSG is with Part 3, responding to state 3 and 4 in TABLE I. In this part, the virtual moment of inertia J_{Bi}, damping coefficient D_{Bi} for each PV/BES-VSG unit are proportional to the sum of battery charging power limit and discharging power limit, as shown in (15), β_1>0, β_2>0.

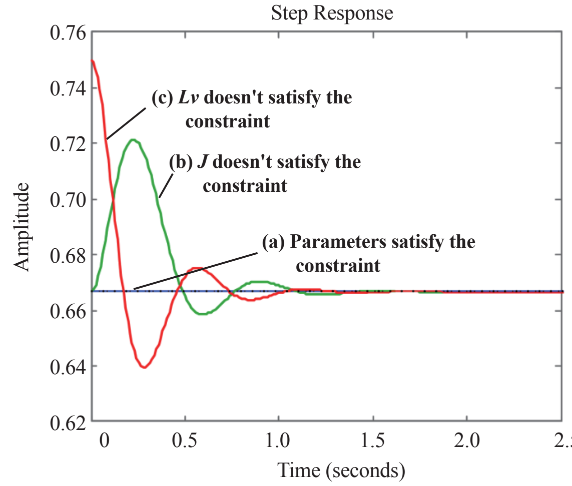

Fig. 3. Step response of G_{pli} for two VSGs system under different conditions of parameters.

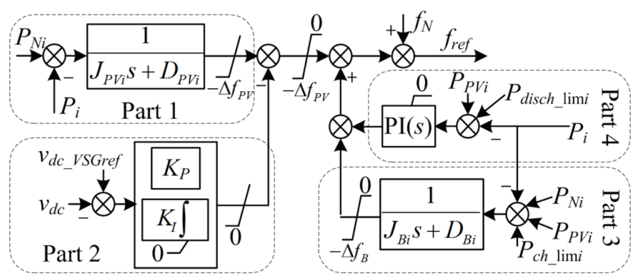

Fig. 4. Control block of active power loop in VSG controller.

$$\begin{cases} \dfrac{J_{Bi}}{\left|P_{ch\_\lim i}\right| + P_{disch\_\lim i}} = \beta_1 \\ \dfrac{D_{Bi}}{\left|P_{ch\_\lim i}\right| + P_{disch\_\lim i}} = \beta_2 \end{cases} \tag{22}$$

Taking i^{th} PV/BES-VSG unit as an example, the power response characteristic of a single VSG is represented by G_i, as shown in (19).

Then, the natural oscillation frequency ω_{ni} and damping ratio ξ_i are shown in (23).

$$\begin{cases} \omega_{ni} = \sqrt{k_i / J_i} \\ \xi_i = 0.5 D_i / \sqrt{J_i k_i} \end{cases} \tag{23}$$

Damping coefficient D_{PVi}, D_{Bi} are the slope reciprocal of f-P characteristic curve of inverter,as shown in Fig. 5. Then, virtual inertia J_{PVi}, and J_{Bi} are designed by considering the overshoot, regulation time of dynamic output power and system stability margin [9]. Meanwhile, the parameters of paralleled inverters should satisfy the constraint conditions shown in (20). When J_{PVi}, J_{Bi}, D_{PVi} and D_{Bi} are selected, α_1, α_2, β_1, β_2 are determined.

Constant power control is with Part 4, responding to state 5 in TABLE I. At steady state, PI controller adjusts inverter output power to P_{PV_MPPTi}+P_{disch_limi}.

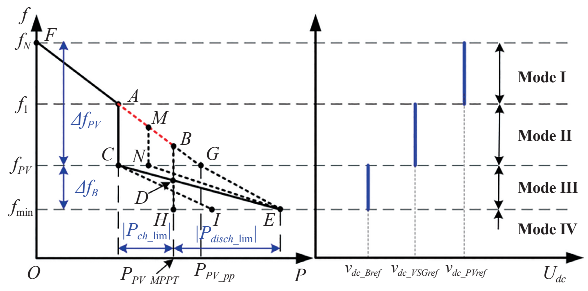

Fig. 5. Output *P-f* characteristic curve of inverter and DC voltage characteristic curve.

It is important to note that, in Part 3 and 4, the active power reference of the VSG controller is P_{PVi}, not P_{PV_MPPTi}.When PV/BES-VSG unit is in state 1 shown in TABLE I, P_{PV_MPPTi} can't be obtained.

B. Control Strategy Analysis

In order to achieve the expected control objectives, this paper realizes the reasonable combination of different control modes between subsystem controllers by setting reference values and saturation values of the controllers output for each subsystem controller, as shown in Fig. 2 and Fig. 3, reducing the coupling between the subsystem controllers to the greatest extent.

PV/BES-VSG unit has four control modes with different combinations. As mentioned above, when the unit is in state 5, there is no controller to regulate DC-link voltage (corresponding to Mode IV with * in TABLE II), which will lead to the system instability. So the value of P_{disch_limi} in VSG controller should be smaller than the value obtained by BES Model in BES controller, then the inverter enters into PCM (corresponding to Mode IV with # in TABLE II). In addition, for the whole microgrid, state 5, which is an overload situation, is an emergency state, PV/BES unit should be avoided to enter into Mode IV, which is solved by load control from central controller in EMS, which is beyond the scope of the paper.

Ignoring Mode IV, *f-P* characteristic curve of inverter with VSG is shown in Fig. 5, the three control modes correspond to the three-segment curves in the frequency range of $[f_N, f_{min}]$, where f_N and f_{min} define the operating frequency limits of the microgrid. In Fig. 4, point *G* refers to PV peak power P_{PV_pp}, due to the change of environment conditions, PV maximum power P_{PV_MPPT} (Point *B*) is usually less than P_{PV_pp}.

The frequency range of Line *FG* is $[f_N, f_{PV}]$, and the droop slope is designed according to (21), where $\alpha_2 = 1/\Delta f_{PV}$. The frequency range of Line *CE* is $[f_{PV}, f_B]$, the droop slope is designed according to (22), where $\beta_2 = 1/\Delta f_B$. The projection of Line *CD* on the horizontal axis refers to battery charging power limit $|P_{ch\_lim}|$, the projection of Line *DE* on the horizontal axis refers to battery discharging power limit P_{disch_lim}. The sum of Δf_{PV} and Δf_B is maximum frequency deviation of microgrid, which is determined by the power quality standards. In this paper, setting $\Delta f_{PV} = \Delta f_B = 0.1$ Hz, then the maximum frequency deviation of microgrid is equal to 0.2 Hz.

Because PV peak power $P_{PV\text{-}pp}$ is the inherent parameter of the microgrid, the droop slope of Line *FG* will not be affected by the operation conditions (such as temperature and irradiance), while actual operation range changes with PV maximum power and battery charging power. For example, Point *B* refers to PV maximum power, for $|P_{ch\_lim}|>0$, actual operation point of the inverter is up to Point *A*. The battery charging/discharging power limit is a function of the battery SOC [22], the scope and the projection of Line *CE* on the horizontal axis change slowly with SOC. Considering battery SOC changing rate is much smaller than the response speed of the controllers, the dynamic change of slope doesn't affect the stability of the microgrid, but optimizes power sharing among the batteries.

TABLE II
PV/BES-VSG UNIT CONTROL MODE

Control Mode (VSG Controller)	Unit State	PV Controller	BES Controller	DC-link Voltage
Mode I	1	VCM	PCM	PV
Mode II	2	MPPT	PCM	VSG
Mode III	3	MPPT	VCM	BES
	4	MPPT	VCM	BES
Mode IV	5 *	MPPT	PCM	
	5 #	MPPT	VCM	BES

Multi-segment operation characteristic, as shown in Fig. 4, is implemented through two steps: 1) multi-segment control of DC-link voltage; 2) set appropriate saturation values of the VSG controllers output.

In Mode I, DC-link voltage is controlled by PV at higher level, battery enters into PCM for the saturation of outer loop, Part 2, 3 and 4 in VSG controller are all ineffective due to saturation, the inverter operates on Line *FA* in the frequency range of $[f_N, f_1]$.

In Mode II, PV works at MPPT, battery remains constant power charging, Part 1 and 2 in VSG controller take effect together, regulating DC-link voltage at middle lever, Part 1, 3 lose effect, the inverter works on Line *AC* in the frequency range of $[f_1, f_{PV}]$.

In Mode III, PV remains MPPT, DC-link voltage is regulated by battery at lower level, Part 1, 3 and 4 in VSG controller are all ineffective due to saturation, the inverter operates on Line *CE* in the frequency range of $[f_{PV}, f_{min}]$.

The DC-link voltage is divided into three levels, guaranteeing only one controller is used to regulate DC-link voltage. The proposed method avoids relying on the communications between subsystems, and reduces the coupling between subsystems.

When PV maximum power is sufficient, leading to necessary PV curtailment in PV/BES-VSG unit, thus, the DC voltage will be raised and controlled by PV unit. As a result, the DC voltage reference is set at a higher level in the decentralized control strategy in this segment. When PV maximum power is not enough, battery is needed to discharge to increase the output power at DC side, thus, the DC voltage will be reduced and controlled by battery. As a result, the DC voltage reference is set at a lower level in the decentralized control strategy in this segment. When PV maximum power is not enough, battery charging power is reduced to keep power balance, thus, the DC voltage will be reduced slightly and controlled by inverter. As a result, the DC voltage reference is set at a middle level in the decentralized control strategy in this segment. Therefore, $v_{dc\_PVref} > v_{dc\_VSGref} > v_{dc\_Bref}$.

The relationship between inverter operation segments and DC-link voltage level is shown in (24).

$$v_{dc\_ref} = \begin{cases} v_{dc\_PVref} \;, f \in [f_N \quad f_1] \\ v_{dc\_VSGref} \;, f \in [f_1 \quad f_{PV}] \\ v_{dc\_Bref} \;, f \in [f_{PV} \quad f_{\min}] \end{cases} \tag{24}$$
$$v_{dc\_PVref} > v_{dc\_VSGref} > v_{dc\_Bref}$$

IV. Typical Operation Scenario Analysis

In this section, typical operation analysis for two scenarios are performed for an islanded microgrid with two PV/BES-VSG units shown in Fig. 1, one is for load change, the other is for insolation change or PV maximum output power change.

A. Load Change Scenario

In this segment, the analysis of operation point shift for the microgrid is performed for load change scenario. At steady state, *f-P* droop curves of the two PV/BES-VSG units are shown in Fig. 6. At start, Unit1, Unit2 work at point K_1, K_2 respectively, maintaining the microgrid frequency at f_1 together. With load increasing, Unit1 enters into PCM first. Unit1, Unit2 work at point M_1, M_2 respectively, and the frequency is controlled by Unit2. Then the increased load is totally overtaken by Unit2 until the frequency drops to f_3. At f_3', Unit2 also enters into PCM, the output power is limited, and the frequency will drop to f_3. At f_3, Unit1 and Unit2 enter into Mode III, the batteries charging powers reduce by ΔP_1 and ΔP_2 to keep generation/consumption balance. The operation points change to N_1, N_2. If the load continues increasing, battery charging powers in each unit reduces proportionally until they reduces to zero (Point D_1 and D_2). After that, batteries start discharging proportionally to meet the load increases.

B. PV Maximum Output Power Change Scenario

In this segment, the analysis of operation point shift for the microgrid is performed for PV maximum output power change scenario. Assuming PVs have the same power rating, thus, their *f-P* droop curves are coincidence. PV maximum output power of one unit is changed. At steady state, their *f-P* droop curves are shown as Fig. 7.

At start, Unit1, Unit2 operate at point *U*, *K* respectively. If PV maximum output power of Unit1 is increased from P_{PV_MPPT11} (Point *R*) to P_{PV_MPPT12} (Point *S*), finally changed to P_{PV_MPPT13} (Point *T*), then the operation points of Unit1, Unit2 will transition from Point *U*, Point *K* to *V*, *M*, then change to *W*, *N*, the frequency is increased from f_a to f_b, f_c.

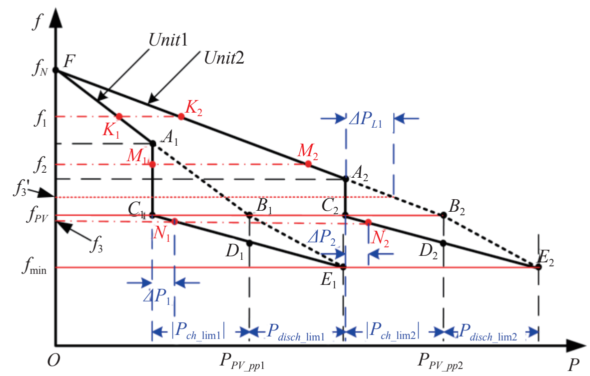

Fig. 6. Load changing operation characteristics.

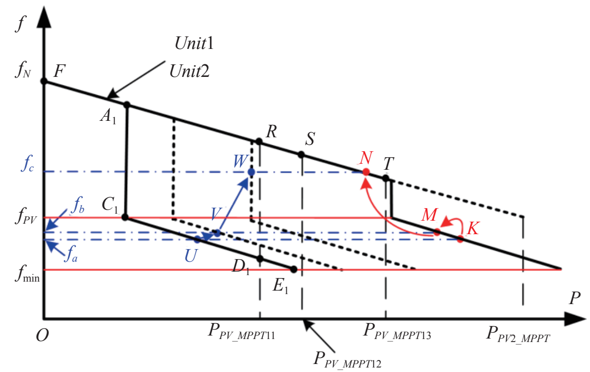

Fig. 7. PV maximum power changing operation characteristics.

V. Simulation Results and Discussions

Simulations for load change and PV maximum output power change scenarios are performed and discussed in this section. A detailed model of an islanding microgrid with two PV/Battery-VSG units is built in the Matlab/Simulink to verify the performance of the proposed decentralized coordination control strategy. BES Model is simplified in BES controller, and the battery charging and discharging power limits are set to be constant and the terminal voltage of the battery is set at 300 V.

A. Load Change Scenario

In this scenario, the main simulation parameters are listed in TABLE III. The simulation results by the proposed control strategy, are illustrated from Fig. 8 to Fig. 11.

The total battery charging power limits is 5 kW, the total maximum PV power is 17.4 kW. Fig. 8 shows the output power profiles of inverters, PVs, batteries responding to the load changes, which is explained as follows.

During 0~2s, the load power is equal to 4.5 kW, the total maximum PV power is more than the sum of battery charging power limit and the load demands, the power relationship is shown as in (2). The batteries are charged with their limit powers 2.5 kW. Inverters share load power based on its own PV maximum output power. Unit1 and Unit2 start curtailing the surplus PV power by adjusting their PV array voltage references

TABLE III
MAIN SYSTEM PARAMETERS FOR CASE I

Parameter	Value	Parameter	Value
Filter inductance	1 mH	P_{PV_pp1}	11.6 kW
Filter capacitance	40 uF	P_{PV_pp2}	5.8 kW
Line inductance	0.1 mH	$\|P_{ch\_lim1}\|$	2.5 kW
Switching frequency	10 kHz	$\|P_{ch\_lim2}\|$	2.5 kW
v_{dc_PVref}	660 V	P_{disch_lim1}	5 kW
v_{dc_VSGref}	650 V	P_{disch_lim2}	5 kW
v_{dc_Bref}	640 V	J_{PV1}	51.2
Δf_{PV}	0.1 Hz	D_{PV1}	1.1×10^5
Δf_B	0.1 Hz	J_{PV2}	25.6
f_N	50 Hz	D_{PV2}	5.5×10^4
U_m	311 V	J_{B1}	35
n	2×10^{-4}	D_{B1}	7.5×10^4
PV temperature	25°C	J_{B2}	35
Insolation	1000 W/m^2	D_{B2}	7.5×10^4

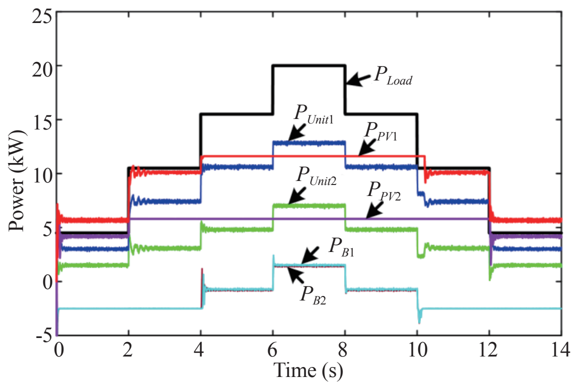

Fig. 8. Output power profiles of units corresponding to changes of loads.

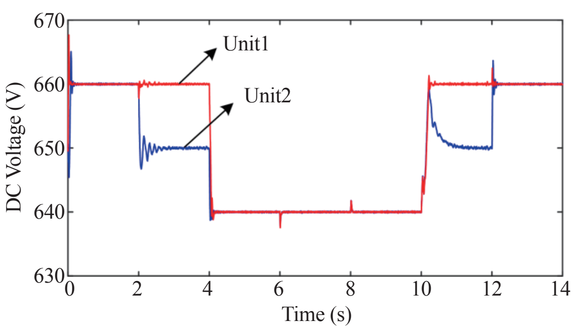

Fig. 9. DC voltages corresponding to changes of loads.

according to the power demand. P_{Unit1} = 3 kW, P_{Unit2} = 1.5 kW, $P_{B1} = P_{B2}$ = -2.5 kW (charging), P_{PV1} = 5.5 kW, P_{PV2} = 4 kW. v_{dc} is regulated by PV unit, so it is kept at 660 V, as shown in Fig. 9.

During 2~4s, load demand is increased to 10.5 kW, the power relationship is shown as (6). The batteries are charged with their limit powers, PV unit in Unit2 starts operating at its maximum PV power, PV unit in Unit1 curtails the surplus PV power according to the power demand. $P_{PV2} = P_{PV\_MPPT2}$ = 5.8 kW, P_{B2} = -2.5 kW, P_{Unit2} = 3.3 kW, P_{Unit1} = 7.2 kW, P_{B1} = -2.5 kW, P_{PV1} = 9.7 kW. In Unit 1, v_{dc} is regulated by PV, so it is kept at 660 V; In Unit2, v_{dc} is regulated by inverter, so it is kept at 650 V, as shown in Fig. 9.

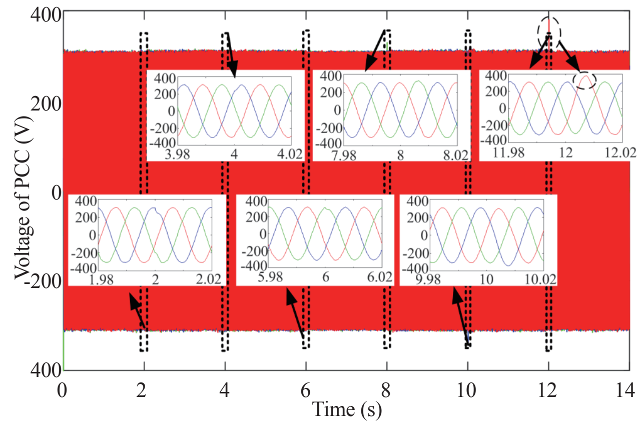

Fig. 10. PCC voltage corresponding to changes of loads.

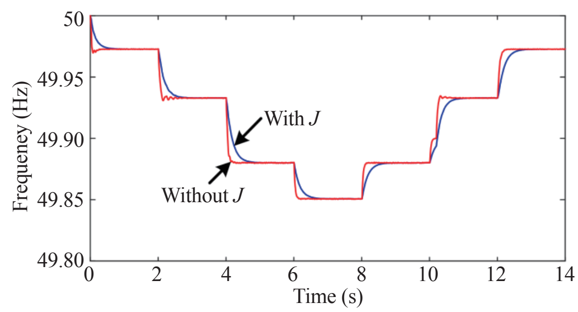

Fig. 11. Frequency of microgrid with and without J corresponding to changes of loads.

During 4~6s, load demand is increased to 15.5 kW, the total maximum PV power is less than the sum of battery charging power limit and the load demands, but the total maximum PV power is more than load demands, the power relationship is shown as (9). PV unit starts working at MPP, $P_{PV1} = P_{PV\_MPPT1}$ = 11.6 kW, $P_{PV2} = P_{PV\_MPPT2}$ = 5.8 kW, but PV power is insufficient to follow the battery charging power limit, thus, the battery charging power decreases with the increased load, $P_{B1} = P_{B2}$ = -0.95 kW, P_{Unit1} = 10.65 kW, P_{Unit2} = 4.85 kW. v_{dc} is regulated by battery, so it is kept at 640 V, as shown in Fig. 9.

During 6~8s, load demand is increased to 20 kW, the total maximum PV power is less than the load demands, the power relationship is shown as (9). PV unit starts working at MPP, P_{PV1} = 11.6 kW, P_{PV2} = 5.8 kW. PV power is insufficient to supply the load, thus, the battery begins to discharge power with the increased load, $P_{B1} = P_{B2}$ = 1.3 kW, P_{Unit1} = 12.9 kW, P_{Unit2} = 7.1 kW. v_{dc} is regulated by battery, so it is kept at 640 V, as shown in Fig. 9.

The following simulation conditions are symmetrical with the conditions above after t = 7s.

The simulation conditions above cover all the possible operation modes for the islanded microgrid with two PV/BES-VSG units. The DC-link voltage and the voltage at PCC of the microgrid are also the same as expected, as shown in Fig. 9 and Fig. 10. In different operation modes, DC-link voltage v_{dc} is controlled by different units, therefore, it has different values. The simulation results demonstrate that the control system works well by the proposed method when the operation points shift because of variation of loads.

Fig. 11 shows the results for two scenarios with and without virtual inertia J. It can be found that VSG can reduce the rate of change of frequency, thus improve the frequency stability of the microgrid.

B. PV Maximum Output Power Change Scenario

In this section, the main simulation parameters are listed in TABLE IV, other parameters are as the same as parameters in case I. The simulation results by the proposed method are illustrated from Fig. 12 to Fig. 15, in which the load power is kept at 15 kW.

Fig. 12 shows the output power profiles of inverters, PVs, batteries responding to the insolation changes, which are explained in detail as follows.

During 0~2s, the insolation of PV1 and PV2 are both 1000 W/m^2, the maximum power of PV1, PV2 are both 11.6 kW. The total maximum PV power is more than the sum of battery charging power limit and the load demands, the power relationship is shown as (2). The batteries are charged with their limit powers 2.5 kW. Inverters share load power equally. PV1 and PV2 start curtailing the surplus PV power by adjusting their PV array voltage references according to the power demand. $P_{Unit1} = P_{Unit2} = 7.5$ kW, $P_{B1} = P_{B2} = -2.5$ kW (charging), $P_{PV1} = P_{PV2} = 10$ kW. v_{dc} is regulated by PV unit, so it is kept at 660 V, as shown in Fig. 13.

During 2~4s,the insolation of PV2 changes to 776 W/m^2, the maximum power of PV1 is kept at 11.6 kW, the maximum power of PV2 is reduced to 9 kW due to the decline of insolation, the power relationship is shown as (6). The batteries are charged with their limit powers, PV2 starts operating at its maximum PV power, PV1 curtails the surplus PV power according to the power demand. $P_{PV2} = P_{PV\_MPPT2} = 9$ kW, $P_{B2} = -2.5$ kW, $P_{Unit2} = 6.5$ kW, $P_{Unit1} = 8.5$ kW, $P_{B1} = -2.5$ kW, $P_{PV1} = 11$ kW. In Unit 1, v_{dc} is regulated by PV, so it is kept at 660 V. In Unit2, v_{dc} is regulated by inverter, so it is kept at 650 V, as shown in Fig. 13.

During 4~6s, the insolation of PV2 changes to 600 W/m^2, the maximum power of PV1 is kept at 11.6 kW, the maximum power of PV2 is reduced to 7 kW due to the drop of irradiation. The total maximum PV power is less than the sum of battery charging power limit and the load demands, but the total maximum PV power is more than load demands,the power relationship is shown as (9). PVs start to work at MPP, $P_{PV1} = P_{PV\_MPPT1} = 11.6$ kW, $P_{PV2} = P_{PV\_MPPT2} = 7$ kW, but PV power is in sufficient to follow the battery charging power limit, so the battery charging power decreases with the increased load, $P_{B1} = P_{B2} = -1.8$ kW, $P_{Unit1} = 9.8$ kW, $P_{Unit2} = 5.2$ kW. v_{dc} is regulated by battery, so it is kept at 640 V, as shown in Fig. 13.

During 6~8s, the maximum power of PV2 is kept at 7 kW, the insolation of PV2 changes to 520 W/m^2, the maximum power of PV1 is reduced to 6 kW due to the drop of irradiation. The total maximum PV power is less than the load demands and the power relationship is shown as (9). PVs start working at MPP, $P_{PV1} = 6$ kW, $P_{PV2} = 7$ kW. PV power is insufficient to supply the load, so the battery begins to discharge power with the increased load, $P_{B1} = P_{B2} = 1$ kW, $P_{Unit1} = 7$ kW, $P_{Unit2} = 8$ kW. v_{dc} is regulated by battery, so it is kept at 640 V, as shown in Fig. 13.

TABLE IV
MAIN SYSTEM PARAMETERS FOR CASE II

Parameter	Value	Parameter	Value
P_{PV_pp1}	11.6 kW	D_{PV1}	1.1×10^5
P_{PV_pp2}	11.6 kW	J_{PV2}	51.2
$\lvert P_{ch\_lim1}\rvert$	2.5 kW	D_{PV2}	1.1×10^5
$\lvert P_{ch\_lim2}\rvert$	2.5 kW	J_{B1}	35
P_{disch_lim1}	5 kW	D_{B1}	7.5×10^4
P_{disch_lim2}	5 kW	J_{B2}	35
J_{PV1}	51.2	D_{B2}	7.5×10^4

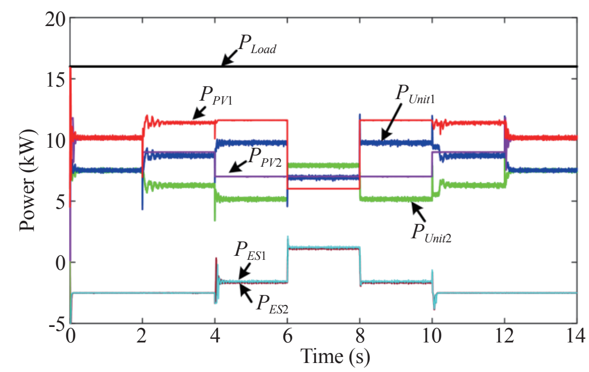

Fig. 12. Output powers of each unit corresponding to changes of insolation.

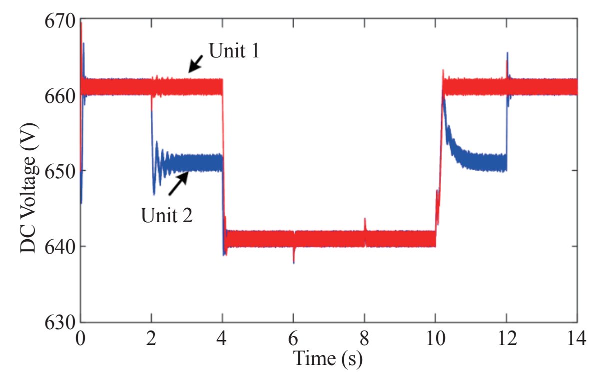

Fig. 13. DC voltages corresponding to changes of insolation.

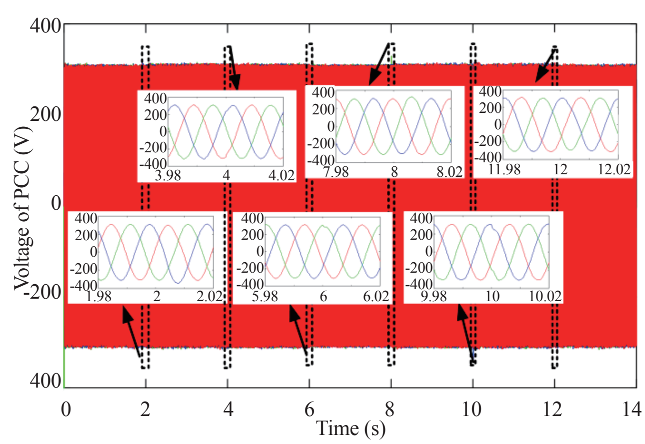

Fig. 14. PCC voltage corresponding to changes of insolation.

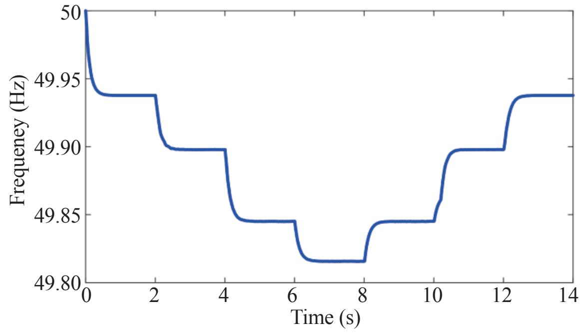

Fig. 15. Frequency of microgrid corresponding to changes of insolation.

The following simulation conditions are symmetrical with the conditions above after t = 7s.

Fig. 14 shows the voltage at PCC, Fig. 15 shows frequency of microgrid. From Fig. 14 and Fig. 15, it can be seen that the voltage and frequency of the microgrids can be kept as stable as expected by the proposed method when the operation points shift with variation of PV maximum output power.

VI. Conclusions

In this paper, a decentralized coordination control method is proposed for load sharing in paralleled inverters with PV/battery-VSG units. The whole system can operate in five states according to the relationship between the load, the total PV maximum output power, the total battery charging, discharging power limits. The operation of PV/BES-VSG unit has four modes. In different modes, the subsystems (PV Controller, Battery Controller, VSG Controller) have different control objectives.

With the proposed method, the droop characteristics of VSGs can be adaptively adjusted according to the DC bus voltage and frequency of the microgrid because local controllers for each PV/Battery-VSG unit are able to switch operating modes automatically.

The simulation results for an islanding microgrid with two PV/BES-VSG units verify that the batteries supply power only when all PV units reach their limits to prolong the battery life, otherwise, the batteries keep charging, therefore the proposed method can maximize the use of PV and ensure the reasonable power sharing between inverters while improving the frequency stability of the microgrid. The proposed method is also applicable to multiple PV/BES-VSG units more than two.

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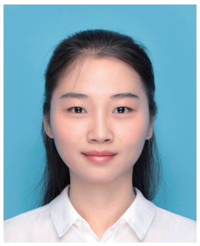

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Power System Support Functions Provided by Smart Inverters—A Review

Xin Zhao, Liuchen Chang, Riming Shao, and Katelin Spence

Abstract—**Renewable energy is seen as a viable alternative to traditional energy sources, and distributed generation (DG) based on renewable energy sources has experienced rapid growth worldwide. High penetration of renewable energy based DG systems makes the grid more vulnerable, and stricter standards have been issued for grid interconnection of DG systems. DG systems are expected to be controllable with high flexibility and reliability. Provision of grid support functions and ancillary services, such as reactive power control, fault ride-through and harmonic compensation, is the key to attaining higher utilization of DG. Such functionalities are implemented in new generation smart inverters, which can contribute to the reduced cost of energy and need for additional system resources. The state-of-the-art power system support functions are summarized in this paper for the purpose of enhancing operation in low-voltage networks. Experimental results are given to better understand the implementation of the functions.**

Index Terms—**Fault ride-through, harmonic compensation, power system support functions, reactive power control, smart inverters.**

I. Introduction

In recent years, there has been a rapid increase of renewable energy based distributed generation (DG) in power systems. These DG systems, such as photovoltaic (PV), wind, etc., have intermittent power output which disturbs the system operation [1], [2]. The penetration level of DG units is expected to further increase in the future. This is because they play an important role in reducing pollution, decreasing power transmission losses, and improving local utilization of renewable energy sources [3], [4].

However, intensely expanding installation of DG units into the grid also brings challenges to the distribution network, such as reverse power flow, voltage deviations, frequency fluctuations, and power quality problems [5]-[7]. The California Public Utilities Commission has initiated a Smart Inverter Working Group to investigate new requirements for inverter-based PV and energy storage systems. The recommendations have been approved to be included in California's Electric Tariff Rule 21, which governs DG interconnection in California utilities. Spurred by the CA Rule 21 update [8], UL released the latest 'Smart Inverter' standard for inverters (UL 1741SA) in September 2016 [9]. Meanwhile, a few IEEE and IEC standards are under revision or new development [10].

These new standards are published in order to regulate the interconnecting DG systems, especially in terms of power system support functions and ancillary services [8], [11]. These highly anticipated standards provide a certification method for smart inverter functionality and will help reduce barriers to large scaled renewable energy deployment. The functions should be developed to minimize the adverse effects from variable renewable energy generation and other grid disturbances [12].

Also, critical customer demands are continuously being updated to facilitate reliable and efficient power generation from DG units, which imposes more challenges for the interfaced inverters. Therefore, new generation smart inverters with enhanced control flexibility are desired to provide power system support functions [3].

Power system support functions from smart inverters such as reactive power compensation, fault ride-through, and power quality enhancement, together with higher reliability demands, are the key to further reducing the total cost of energy. This paper takes PV systems as an example to introduce, review and analyze the power system support functions of smart inverters.

The objective of this paper is to review the available technologies regarding power system support functions of smart inverters. The following sections in the paper describe the power system support functions in detail along with experimental results. The voltage support (reactive power control) function of smart inverters is described in Section II. Harmonic compensation is discussed in Section III. Voltage ride-through control strategy is introduced in Section IV, followed by frequency ride-through in Section V. Then, other power system support functions are introduced in Section VI. The final section gives the conclusion.

II. Reactive Power Control

Traditionally, PV systems are designed with active power control as governed by IEEE 1547 Standard for Interconnecting Distributed Resources with Electric Power Systems. However, the impact of increasing penetration of PV systems in low-voltage distribution networks may change the voltage profile of feeders. If the total installed PV is larger than the capacity of the host feeder, network safety and stability cannot be guaranteed. Specifically, when the production of a feeder surpasses its consumption, a reverse power flow occurs which leads to overvoltage and might cause problems to the coordination of protective devices and disconnection of equipment for stability reasons [13]. So the reactive power control strategy should be adopted to ensure the voltage is within the acceptable range.

Recently, interconnection standards issued in many coun-

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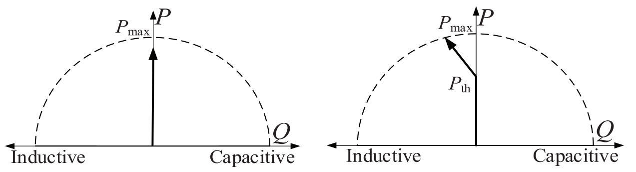


(a) Unity power factor method (b) Active power-dependent method

Fig. 1. Operational curve of inverter.

tries have specified reactive power control strategies in order to maintain power quality or provide ancillary services for the low-voltage networks. Therefore, the inverters should supply reactive power reasonably.

There are many papers focusing on reactive power control, and the control strategies are summarized in this section. Some commonly used reactive power control strategies included unity power factor method [14]-[16], active power-dependent method [16], [17], $Q(V)$ control [18], [19], $Q(V)/P(V)$ control [20], [21], 2-quadrant P-Q planemethod [22]-[24], etc. A detailed analysis is shown as below.

A. Unity Power Factor Method

Previously, the most common reactive power control strategy was the unity power factor method [14]-[16], where the inverter operates with no injection of reactive power into the grid, as shown in Fig. 1(a). This approach is in complete compliance with the previous version of IEEE Standard 1547 and UL1741, which specifies that distributed resources shall not actively regulate voltage at the point of common coupling (PCC) [16], [25], [26].

However, the disadvantage of this method is that there will be overvoltage in the areas with high penetration levels of PV. In some applications, a limit on maximum active power generation is enforced to prevent voltage beyond the allowed range, and this will curtail the active power to the power system [27].

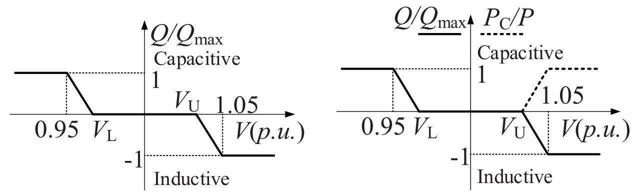
B. Active Power-Dependent Method

Utilities have succeeded in mitigating overvoltage problems due to unity power factor operation by slightly changing the power factor of the inverter. However, the reactive power control results in a considerable power loss to low-voltage grids. Hence, in order to minimize the power loss, the German Grid Codes proposed the standard characteristic curve in Fig. 1(b). The objective of the standard requires the generation unit to operate in reactive power consumption mode when the feed-in active power surpasses a threshold P_{th} in order to mitigate the overvoltage [28]. With the active power-dependent method [16], [17], the general relationship between active and reactive power of a PV system is defined as follows:

$$\mathrm{Q} = \begin{cases} m\left(P\text{-}P_{th}\right) & P > P_{th} \\ 0 & P \le P_{th} \end{cases} \tag{1}$$

where m (< 0) is a slope factor.

This method adjusts the reactive power flow back to the grid based on active power output of the inverter, thus providing a form of voltage regulation due to active power output variations. However, it does not actively regulate voltage at the PCC because the feeder impedance characteristics are not taken into account.



(a) $Q(V)$ control method (b) $Q(V)/P(V)$control method

Fig. 2. Schematic operational curve of PV inverter.

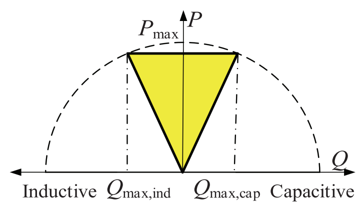


Fig. 3. 2-quadrant P-Q control method.

C. Q(V) Control

The $Q(V)$ control method provides a dynamic voltage-regulation response based on local or area electrical power system voltage [18], [19]. One example of the $Q(V)$ characteristic curve is shown in Fig. 2(a). The inverter is either consuming or producing reactive power if its terminal voltage deviates from the predefined upper/lower critical voltages V_U and V_L, respectively. Owing to the effect of feeder impedance, the voltage of PV inverters near the feeder typically are within the range, so these inverters do not contribute in voltage regulation. But inverters near the end of the feeder need to provide reactive power, causing additional stress on these inverters.

D. Q(V)/P(V) Control

The $Q(V)/P(V)$ strategy has been proposed in order to further mitigate overvoltage when $Q(V)$ control alone is inefficient. One example of the $Q(V)/P(V)$ characteristic curve is shown in Fig. 2(b). The control strategy is similar to the $Q(V)$ method with the addition of an active power curtailment (P_C) feature [20], [21].

E. 2-Quadrant P-Q Control

Fig. 3 illustrates inverter operation in a 2-quadrant P-Q plane, where the inverter can generate either inductive or capacitive reactive power at different voltage levels [22]-[24]. The feasible operating space is enclosed by the triangular-shaded area that represents the total power factor limit and inverter rating curve. The inverter generates inductive reactive power when the voltage exceeds the upper voltage level, and the inverter generates

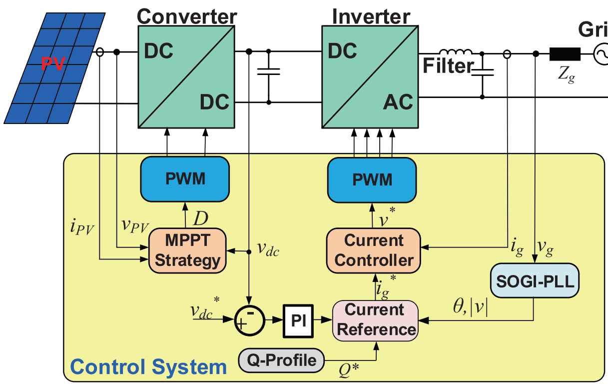


Fig. 4. Schematic diagram of single-phase grid-connected PV system.

capacitive reactive power when the voltage is below the lower voltage level.

There is room for most PV inverters to provide reactive power compensation, since the PV inverters rarely operate at the rated power levels. The maximum available reactive power $|Q_{\max}|$ can be determined by:

$$|Q_{\max}| = \sqrt{S_{\max}^2 - P_{\text{ins}}^2} \tag{2}$$

where P_{ins} is the instantaneous active power and $S_{\max}$ is the maximum apparent power.

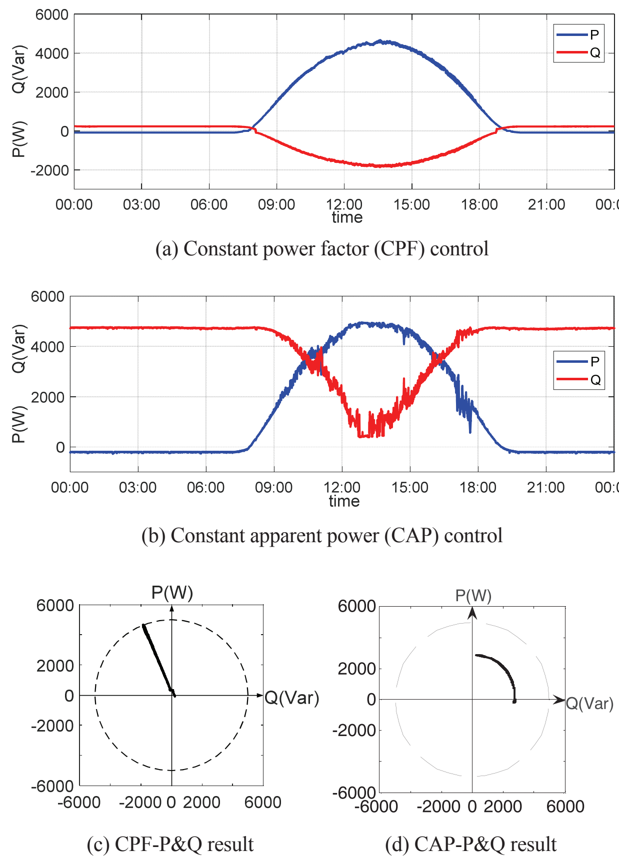
F. Reactive Power Control at Night

Being weather-dependent, active power injection from PV inverters is only possible when there is sufficient solar irradiance. Consequently, while active power is not available during nights, reactive power can be delivered to the grid. That is to say, the PV systems can work as a static Var generator (SVG) and provide dynamic compensation of reactive power to adjust the grid voltage of the power system. This operation mode is referred to as reactive power control at night [3], [29].

Considering the reactive power constraint of a PV inverter shown in (2), the PV inverter can inject reactive power equivalent to the maximum apparent power during the night. The suitable reactive power value is decided by the real-time grid voltage level.

G. Test Results of Reactive Power Control

Residential PV installations are very common and single-phase inverter is required for a PV system connecting to the grid. Fig. 4 shows the schematic diagram of a typical single-phase grid-connected PV system. The two-stage converter is adopted to achieve power conversion, which can achieve a flexible control strategy. The DC/DC converter is adopted to offer maximum power point tracking (MPPT) of PV output and boost the PV panel voltage to an acceptable range for the DC/AC converter (i.e. inverter). The inverter stabilizes the DC-link voltage and controls the grid current with good power quality. In this control system, the reference reactive power Q^* is generated according to the aforementioned reactive power control strategies.



(a) Constant power factor (CPF) control

(b) Constant apparent power (CAP) control

(c) CPF-P&Q result (d) CAP-P&Q result

Fig. 5. Test results of reactive power control.

Two different control objectives are tested based on an actual 5 kW single-phase PV system (parameters are in Appendix), and the 24hr operational results are shown in Fig. 5. Fig. 5(a) and Fig. 5(c) show that the reactive power varies with active power, while the power factor keeps constant based on constant power factor control strategy, taking no consideration of power loss and AC filter capacitor. In Fig. 5(b) and Fig. 5(d), the apparent power keeps constant all the time and the PV inverter provides reactive power equivalent to the maximum apparent power during the night if needed.

III. Harmonic Compensation

Nowadays, many power converter based apparatuses such as variable speed drives and switching mode power supplies, have been used. These loads have created issues in power quality [30]-[32].

For grid-connected generation systems, the current distortion is an important power quality index. For instance, both IEEE Standard 1547 and Rule 21 state that the total harmonic distortion (THD) of grid current injection into distribution system at the PCC should not exceed 5% at the rated current level. However, grid conditions and operational modes may significantly impact the distortion level of the injected current from grid-connected inverter systems. Therefore, a high-performance control solution must be developed for grid-connected systems to produce high-quality power in different operation conditions.

To compensate harmonic distortions in distribution systems, many active and passive filtering methods have been developed [33]. However, installing additional filters is not very favorable due to their high costs and sensitivity to parameter variations. Alternatively, flexible control of grid-connected inverters may be utilized to offer the possibility of power quality improvement. Consequently, the harmonic compensation function could be integrated with the primary power generation by modifying the control strategies [34]-[36]. This is especially attractive considering that PV systems do not always operate at full capacity, and the available capacity can be used to realize harmonic compensation without additional costs [37].

For PV systems participating in power quality enhancement, there are three harmonic compensation objectives in general: 1) PV current harmonic rejection, 2) PCC current harmonic compensation, and 3) PCC voltage harmonic compensation [38]. The first and second objectives can be attained by modifying the current controller of the inverter. Voltage control is essential for achieving the third objective, and virtual impedance is always introduced to accomplish the compensation.

A. Controller Based Methods

There has been significant work done in the area of harmonic compensation using different controllers. Multi-resonant controller (MRC) plugged into proportional-resonant/proportional-integral (PR/PI) controller are the most popular controller for harmonic elimination, which can easily compensate low-order harmonics [39]-[43]. However, the discretization of multiple resonant controllers will result in a heavy computation burden, and the fundamental frequency variation will affect the performance. Also, as mentioned in [42], the phase margin of the system becomes small with MRC and resonances may be triggered if phase-lead compensators are improperly designed.

The study in [44]-[47] considers the use of repetitive controller (RC) based harmonic elimination, and RC with a simple phase compensator can track or reject all harmonics below the Nyquist frequency. It can eliminate harmonics using much less computation than MRC does, but the dynamic response is much slower than MRC's. Also, it is impossible for RC systems to optimize the error convergence rate, since the gain of all the harmonics in RC are equal.

Predictive controller (PC) was known as the deadbeat controller with a high bandwidth and fast dynamic response, which is widely used for current error compensation to offer high quality current to the grid [48]. However, it suffers degraded performance due to the time-delay and system model mismatch [49]. Several methods have been proposed to improve the overall performance of PC. Improved algorithms have been presented to reduce the sensitivity to parameter variations [50]-[52], compensating for the time delay [53], [54] and rejecting disturbances experienced by the control system [55], [56].

A hybrid controller by combining the RC and PR controller is also developed, and it can achieve high-performance regardless of the operational modes [57], [58].

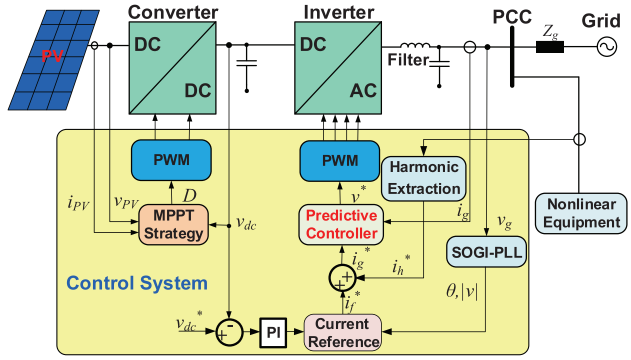


Fig. 6. Control structure of PV systems for harmonic compensation.

B. Virtual Impedence Based Methods

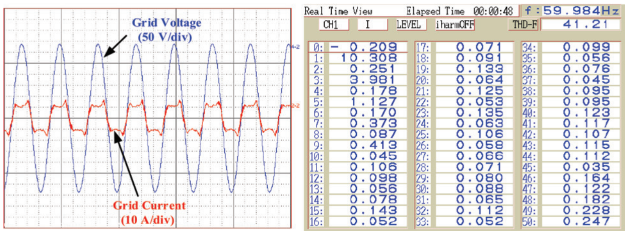
Over time, the virtual impedance concept is increasingly employed for the control of power electronic systems, which is developed to optimize inductance-to-resistance (X/R) ratio of the inverter's equivalent output impedance [59]. Generally, the virtual impedance loop can either be embedded as an additional degree of freedom for active stabilization and disturbance rejection, or be employed as a command reference generator for the inverters to provide ancillary services. The virtual impedance is generally implemented based on the feedback of output filter states and/or the feedforward of the disturbance variables. By shaping the control output impedance, the virtual impedance can be used for harmonic compensation [60].

The virtual impedances at the harmonic frequencies can be implemented in different ways. The research in [61]-[63] considers the inverter as a small resistance at harmonic frequencies, where the PCC voltage is measured and the harmonic components are extracted to produce the reference harmonic current of the inverter. A virtual impedance across the grid side inductance, which can be represented by a series *RL* branch in parallel with a negative inductance, is added through the grid current feedback control [64]. A virtual *RC* damper in parallel with the passive filter capacitor is proposed in [65], where the positive resistance achieves better performance of harmonic resonance damping, and the negative inductance reduces the grid side inductor for the purpose of better harmonic distortion mitigation. In order to eliminate the influence of the virtual impedance on the power control, a high-pass filter is introduced in the virtual impedance control and the virtual impedance is only effective in the high resonance frequency range [66].

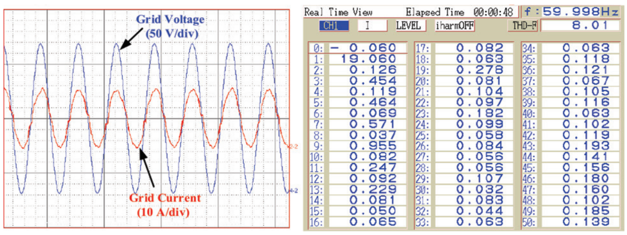
C. Test Results of Harmonic Compensation

The schematic diagram of PV system with harmonic compensation is shown in Fig. 6. The predictive controller based method is adopted to achieve the PCC current harmonic elimination.

The experimental results in Fig. 7(a) shows that the current at PCC is distorted by nonlinear equipment. After adding the PV system to provide harmonic compensation, the current at PCC becomes much more sinusoidal in Fig. 7(b) and the THD of current decreases to 8.01% from 41.21% in Fig. 7(a).



(a) PCC current waveform and harmonics, without compensation



(b) PCC current waveform and harmonics, with compensation

Fig. 7. Test results of PV systems for harmonic compensation.

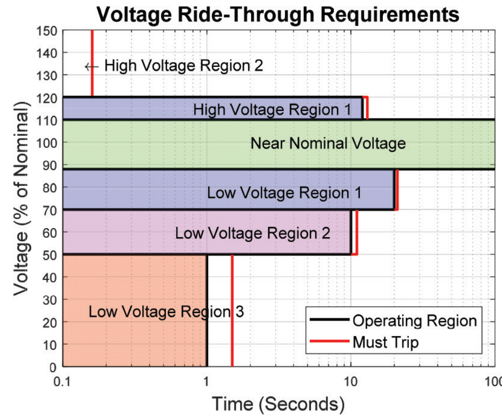


Fig. 8. Voltage ride-through regions according to Rule 21.

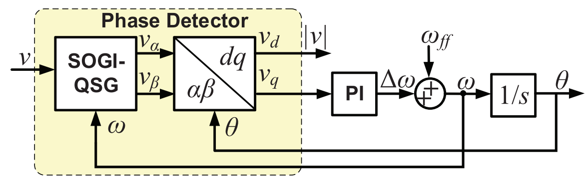


Fig. 9. The structure of SOGI-PLL.

IV. Voltage Ride-Through

Recently, with high levels of penetration of PV generation, maintaining the grid stability represents a greater challenge to the network operators. The events of voltage sags happening every year in many countries have increased. Utilities have released grid codes that require these systems to provide grid support during grid faults. One of them is to introduce the voltage ride-through (VRT) capability into PV systems. To fulfill these grid codes, the PV systems need to satisfy the VRT capability requirement and contribute to stabilizing the grid voltage during a disturbance [67], [68].

Several countries have updated the grid codes for VRT in low/medium-voltage systems. For instance, CA Rule 21 allows PV inverters to ride through faults. The low/high voltage ride-through (L/HVRT) function is a departure from the previous UL 1741/IEEE 1547 standards where only must trip levels and durations were assessed. Now smart inverters must stay connected to the grid for a specific duration and then trip after the must trip time, as shown in Fig. 8 [8], [12].

Along with the updates of grid codes, the control techniques of PV inverters are required to be upgraded as well, because the operation during voltage faults is much different from that of normal conditions. Some issues need to be considered, such as fault detection and the power balance control under different voltage levels. In order to successfully complete the VRT operation, several key technologies should be resolved including voltage detection techniques and power control strategies.

A. Voltage Detection Methods

The voltage detection and synchronization scheme play a major role in the control of PV systems under grid faults. A good synchronization system should respond to a voltage change immediately when a fault occurs. Many methods can obtain the exact voltage dip depth and phase angle within one fundamental period under ideal operation conditions. However these methods are incapable of coping with harmonics and unbalanced grid conditions. Nowadays, phase-locked loop (PLL) technique based synchronization methods have become the most widely used solutions. Some methods have been proposed to enhance the performance under polluted grid conditions.

Two widely-used PLLs, the enhanced PLL (EPLL) [69]-[71] and the second-order generalized integrator (SOGI)-based PLL (SOGI-PLL) [72]-[74], are based on the combinations of adaptive filters with a sinusoidal multiplier and a quadrature signal generator system. These PLLs can only filter high frequency harmonics; however, the low frequency harmonics are not eliminated.

Recently, more advanced PLL techniques have been presented, which enable robustness of synchronization against both the low and high order harmonics. A PLL based on a multi harmonic decoupling cell (MHDC) technique scheme is proposed [75], [76], which can achieve an accurate performance under harmonic distortions. However, it increases the complexity resulting in heavy computation. To eliminate the DC offset and harmonics of SOGI-PLL under grid faults, several methods have been proposed in the literature [77]-[81]. A new second-order SOGI-QSG (SO-SOGI-QSG) presented [81] inherits the simplicity of the SOGI-QSG and also has better disturbance attenuation.

Reference [82] has compared several widely-used PLL methods in terms of accuracy and dynamic response during voltage faults, and it reveals that the SOGI-PLL is a promising synchronization technique in single-phase grid-connected systems for VRT. Therefore, the SOGI-PLL has been adopted to detect both phase and magnitude of grid voltage in single-phase PV systems, and the structure of SOGI-PLL is shown in Fig. 9.

B. Control Strategies

The control diagram of the PV system with VRT capability

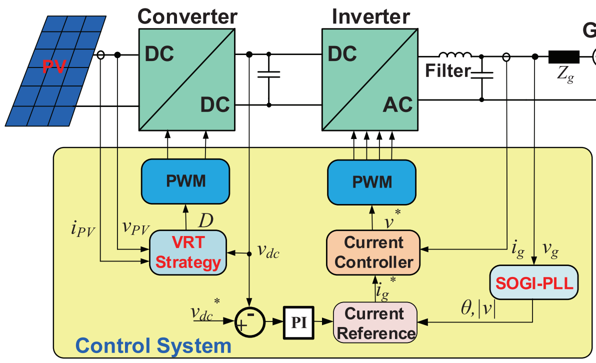


Fig. 10. Control diagram of PV system with VRT capability.

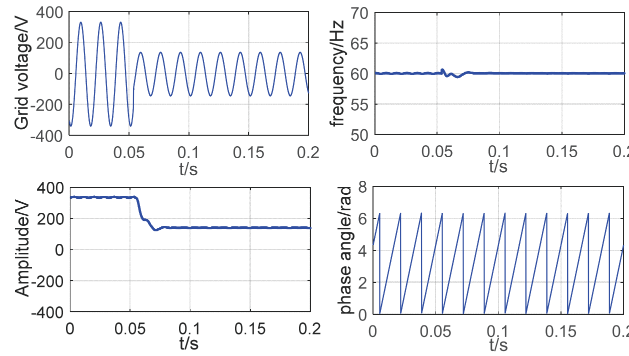


Fig. 11. Experimental result of SOGI-PLL under grid voltage dip.

is shown in Fig. 10. The SOGI-PLL is used to detect both the phase and amplitude of the grid voltage quickly during a voltage fault. However, the control strategy should be modified during a voltage fault to satisfy the grid codes.

Some methods have been proposed to achieve better performance under grid voltage faults. The maximum current amplitude control for the inverter is presented [83], [84] to provide the maximum reactive power under the allowable current amplitude. Different reactive power injection strategies are proposed to improve the reliability [85], including constant average active power control, constant active current control, constant peak current control, and thermal optimized reactive power control strategy. To improve the output waveform quality and maintain safe operation by attenuating double-line-frequency voltage ripple during a grid voltage drop, a DC-link voltage adjustment method for the inverter is proposed [86]. The concept of multi-mode operation for PV power systems is presented to maintain balanced power [87]. According to the new standard Rule 21, the control strategies of PV system is given as below.

1) MPPT Mode

The converter should be in continuous operation when the grid voltage is in the "Near Nominal Voltage" region in Fig. 8, so the DC/DC converter should remain in its MPPT mode to harvest the maximum power from the PV array.

2) Constant Power Control Mode

If the grid voltage is in Low Voltage Regions 1 & 2 defined in Fig. 8, the present active output power and current of the single-phase inverter may be higher than the allowable maximum value. So the MPPT function of the boost converter should be abandoned, and the simplest way is to turn off the switches of the boost converter. However, in order to continuously deliver the solar energy to the grid and to shorten the MPPT response time after the grid fault is cleared, the constant power control mode should be adopted.

3) Momentary Cessation Mode

If the grid voltage is in Low Voltage Region 3 or High Voltage Region 1, the PV system shall work in momentary cessation mode and cease to energize in not more than 0.16s but not trip. Therefore, the switches of the boost converter and single-phase inverter should be turned off but the breakers and contactors of the PV system should keep closed.

C. Test Results of Voltage Ride-Through

A grid simulator (California Instruments MX22.5) is adopted to generate grid voltage faults, and experimental results of the 5 kW single-phase PV system are given to validate the performance of the synchronization technique and the voltage ride-through control strategy.

1) PLL Results

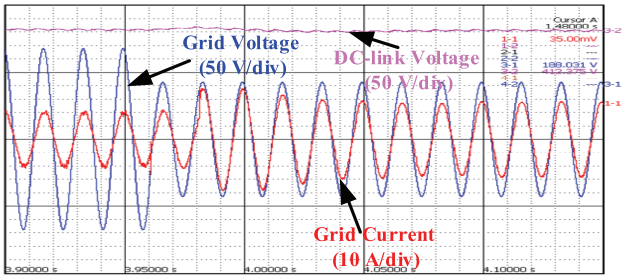
The amplitude step of grid voltage is generated by the grid simulator to simulate a grid voltage dip fault from 240 V to 100 V, shown in Fig. 11. The experimental results show that the SOGI-PLL can detect the voltage amplitude and phase angle precisely in different voltage levels and has a good dynamic response to amplitude changes. The settling time of the amplitude is about 1 grid cycle. The frequency and phase angle are not affected significantly when the voltage dips.

2) VRT Results

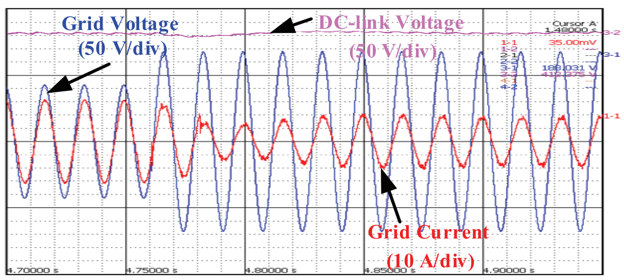
The performance of VRT is evaluated experimentally, and different scenarios are implemented to test the multi-mode operation of PV systems mentioned before.

When the grid voltage dips to 63% of its normal value shown in Fig. 12, the voltage is in Low Voltage Region 2 according to Rule 21. So the PV system should be in mandatory operation and the control mode of converter should change from the MPPT mode to the constant power control mode. The PV system can keep the connection and deliver power to the grid during voltage dips, and there is no overcurrent and overvoltage. The inverter returns to the MPPT mode after the voltage recovers.

When the grid voltage dips to 42% of its normal value shown in Fig. 13, the voltage is in Low Voltage Region 3 according to Rule 21. So the PV system should work in momentary cessation, and the control mode of the converter should change from the MPPT mode to the momentary cessation mode. The PV system still keeps the connection with the grid but ceases to energize in 30ms after the voltage dips. The system starts delivering power to the grid when the voltage recovers to normal.

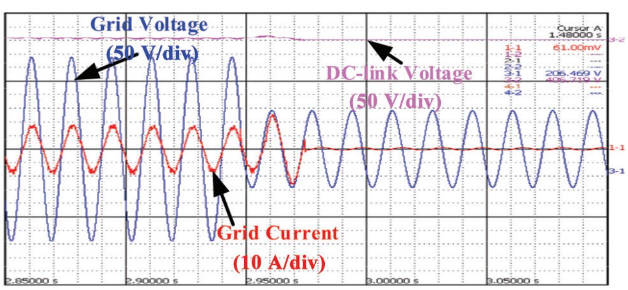


(a) Voltage dips

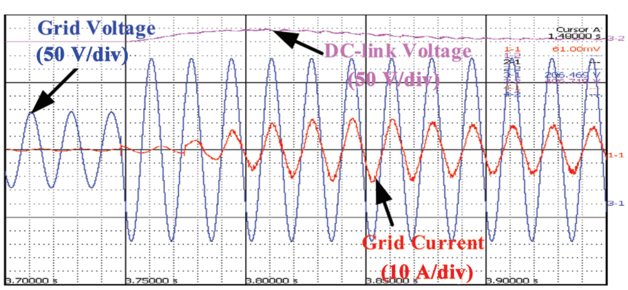


(b) Voltage recovers

Fig. 12. Experimental results of PV system when voltage dips to 63%.



(a) Voltage dips



(b) Voltage recovers

Fig. 13. Experimental results of PV system when voltage dips to 42%.

V. Frequency Ride-Through

A. Introduction

The frequency ride-through (FRT) regions corresponding to Rule 21 are shown in Fig. 14. Smart inverter systems shall remain connected to the power system while the grid is within the "must stay connected frequency-time region", and shall disconnect from the grid outside the frequency-time range.

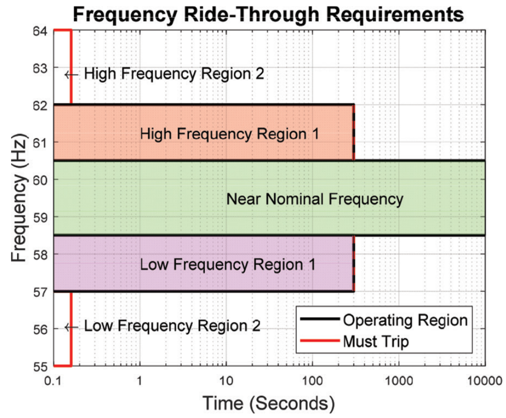


Fig. 14. Frequency ride-through regions according to Rule 21.

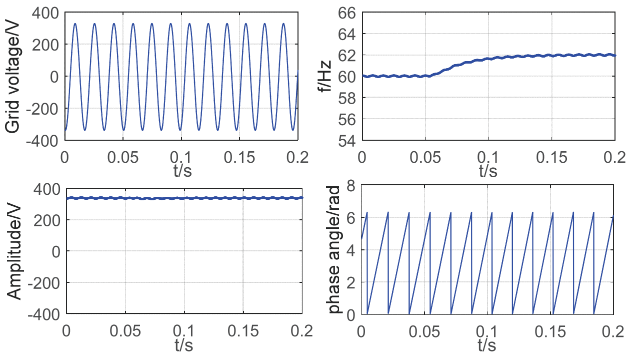


Fig. 15. Experimental result of SOGI-PLL under grid frequency swell.

The high and low frequency protection limits will permit generation systems to ride through temporary frequency rises and dips, thus decreasing the number of unnecessary disconnections by generation systems and possible power outages. Generation systems will no longer disconnect before the frequency levels have had time to possibly recover and return within their normal limits [11].

FRT is easy to implement comparing with VRT, because there is no overcurrent or overvoltage and the control strategy remains unchanged for PV systems during the transition process. The most important issue for FRT is the frequency detection technique, which should be able to detect the frequency accurately with a good dynamic response. Similar to the voltage detection in VRT, a PLL is employed to obtain the frequency, such as the SOGI-PLL.

B. Test Results of Frequency Ride-Through

The grid simulator is adopted to generate grid frequency faults, and experimental results of a single-phase PV system are given to verify the FRT capability of the 5 kW PV inverter.

1) Frequency Detection Results

Experimental results of a grid frequency step change from 60 Hz to 62 Hz are shown in Fig. 15. It validates the frequency-adaptive characteristic of the SOGI-PLL which is able to overcome a big jump of frequency without oscillations. The system has a good dynamic response under frequency changes,

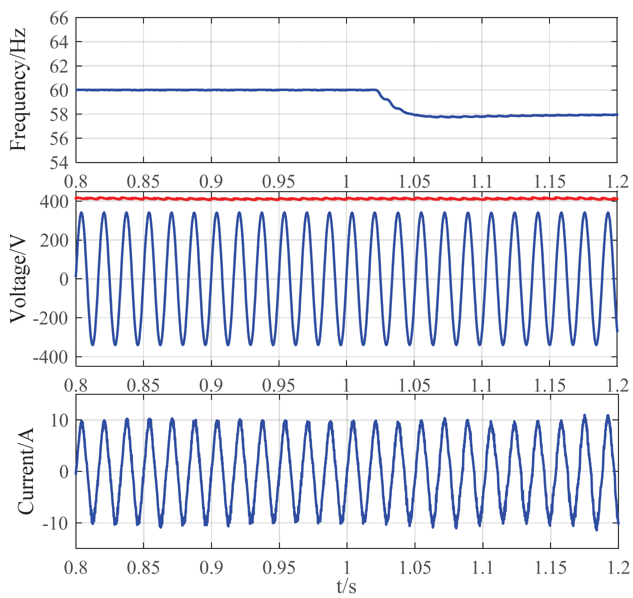


Fig. 16. Experimental result of PV system when frequency dips to 58 Hz.

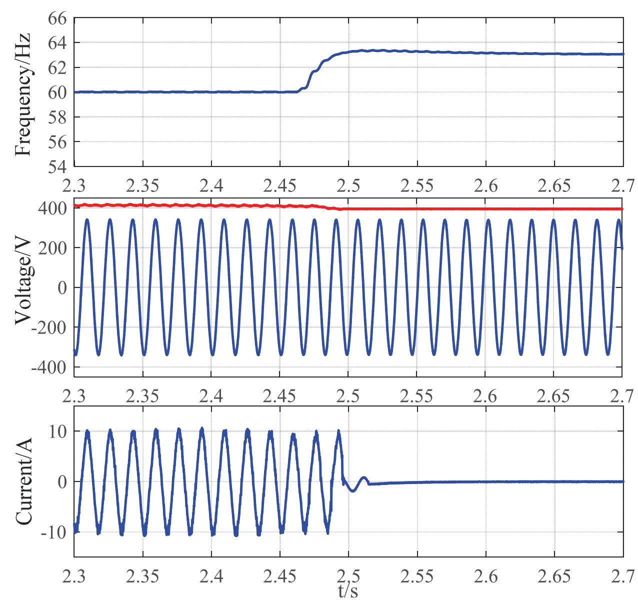


Fig. 17. Experimental result of PV system when frequency swells to 63 Hz.

and the settling time of the frequency is about 3-4 grid cycles. The amplitude is not affected significantly when the frequency swells.

2) FRT Results

Various tests of FRT in different frequency regions have been implemented experimentally, and two scenarios are shown below.

When the grid frequency dips to 58 Hz as shown in Fig. 16, which is in Low Frequency Region 1 according to Rule 21, the PV system should be in mandatory operation. From the result, the PV system can deliver power to the grid during the frequency dip, without overcurrent and overvoltage.

When grid frequency swells to 63 Hz as shown in Fig. 17, which is in High Frequency Region 2 according to Rule 21, the PV system should trip within 0.16 s. The PV system trips in about 50ms after frequency swells, as seen from Fig. 17, satisfying the requirement of the standard.

VI. Other Power System Support Functions

In addition to the aforementioned power system support functions of smart inverters, others functions are mentioned in the interconnection standards. The following gives a brief introduction to some of them.

A. Freq/Watt Control

Freq/Watt control is required in DG units in many European countries and is also included as an optional function in Rule 21.

In order to provide frequency support to the grid, an inverter may change its active power output with the changes in grid frequency. As frequency increases, the desired response of the inverter is to decrease its active power output. Contrariwise, as frequency decreases it is desired for the inverter to increase its

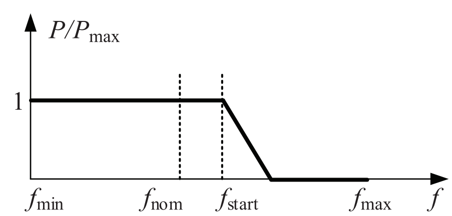


Fig. 18. Characteristic of Freq/Watt control.

active power output [11].

For PV systems, inverters only export no more than the maximum power of the PV panels to the grid. Such inverters may not be capable of increasing their active power and so can only provide an over frequency response. This active power response to a change in frequency is referred to as a Freq-Watt droop function, and the characteristic of Freq/Watt control is shown in Fig. 18.

B. Black Start

Black start capability refers to power system restoration after a power outage on the grid. Research on black start is mainly focused on the restoration of traditional power systems, high voltage direct current (HVDC) systems and microgrid systems. Black start capability is also an optional function according to Rule 21. An inverter-based distributed generation system may operate in a microgrid (possibly just itself) and support additional loads being added, so long as they are within its generation capability [11].

For inverter based systems under such a scenario, an inverter should operate in voltage control mode to generate a stable and clean reference voltage in the absence of the main grid voltage, and facilitate grid synchronization to smoothly switchover from the islanded operation to grid-connected operation when the main grid is restored.

VII. Conclusion

The concept of smart inverters has been emphasized in newly developed DG interconnection standards in order to achieve smooth and grid-friendly integration of large-scale PV systems, and of renewal energy systems in general. Smart inverters could provide a suite of power system support functions. This paper reviews the state-of-the-art power system support functions of smart inverters, such as reactive control, fault ride-through, and harmonic compensation, which could be an enhancement for the new PV inverters to offer additional system resources for grid operation. Viable methods to implement these functions are investigated and tested in a single-phase PV system developed by the authors. Experimental results have demonstrated that smart inverters with power system support functions can provide system resources to alleviate issues created by high PV penetration into the grids.

Appendix

Parameters of Single-Phase PV System Developed by Authors

Parameter	Value	Parameter	Value
Power rating	5 kW	Grid voltage	240 V/60 Hz
AC filter inductor	1.6 mH	ACfilter capacitor	10 μF
DC-Link capacitor	2050 μF	Boost inductor	0.19 mH
Switching frequency	10 kHz		

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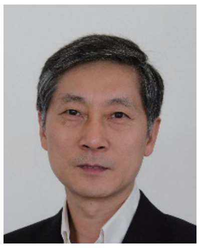

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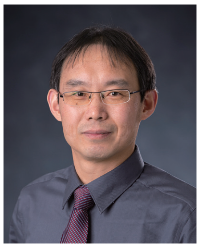

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Integration of Distributed Energy Resources into Offshore and Subsea Grids

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***Abstract*—The main goal of this paper is to outline characteristics and critical aspects related to the design and operation of offshore and subsea electric distribution grids, particularly in the case of high penetration of distributed and intermittent renewable energy sources. At first, the paper provides an overview of electric loads operating in the ocean environment, surveys their power and energy demands and presents their main operational characteristics and corresponding maturity of technology. Subsequently, the potential of marine renewable energy sources is identified by analyzing their degree of development, typical power range and suitability to supply the offshore loads. Based on an up-to-date review of previous studies and real test cases, this paper shows how conditions to enable the development of "offshore smart grids" can be met and it outlines emerging trends in the electrification of the ocean space.**

***Index Terms*—Deep-sea mining, marine energy, offshore grids, offshore wind, oil and gas platforms, subsea applications.**

I. Introduction

DIFFERENT types of renewable energy sources, mostly intermittent in nature, are present in the marine environment, spread over vast regions. Since oceans also host several load centers, characterized by power consumptions of dozens of MW and often located in remote areas, matching power demand and local generation through offshore electric grids could bring advantages in terms of efficiency, grid stability, sustainability and costs, compared to present supply solutions. This, however, requires the proper integration and coordination of various distributed energy systems.

The "*energization*" of the ocean space will occur, at first, through the deployment of independent offshore/subsea microgrids. The variable nature of both offshore loads and marine resources can generate bi-directional power flows, representing challenges for control and protection coordination that are non-dissimilar to those of onshore smart grids. Moreover, the prevailing operation as isolated electric systems will require the careful assessment of stability limits and power quality issues, whereas the possibility of a subsequent interconnection to other offshore systems or integration into the onshore power system, will require the elaboration of control strategies supporting the grid-connected mode of operation. The first necessary step towards the development of any offshore smart grids is, however, to gain an accurate understanding of the power and/or energy characteristics of resources and loads.

Although "moving offshore" has been clearly identified as one of the emerging challenges within the implementation of the smart grid paradigm [1], tailored analyses highlighting the criticalities of offshore grid deployments, compared to corresponding onshore applications, are scarce. In particular, available literature and previous state-of-the-art reviews tend to focus only separately on the different components of offshore and subsea distributed energy systems. Several contributions have surveyed offshore wind developments [2], [3] including floating solutions [4] or generation from other marine energy sources [5]-[7]. Other references have focused on specific offshore loads, mostly highlighting structural and construction aspects [8], [9] or surveyed offshore energy storage applications [10]-[12]. However, cross-cutting contributions are still very limited [13] and a systematic study relating the offshore power generation capabilities with the electrical loads requirements and energy storage potential in the perspective of distributed energy systems is currently missing. The goal of this paper is to contribute to filling this gap, by showing how different offshore components can complement each other and contribute to grid services provision and efficient system operation. The analysis is based on previous techno-scientific contributions, but includes also some of the newest emerging offshore technologies, such as deep-sea mining, which, due to pits novelty, has found limited space in previous papers [14].

II. Electric Loads in the Offshore and Subsea Environment

Electric loads in the ocean environment (e.g. Fig. 1) are similar to concentrated industrial onshore loads. However, the space limitation, cost of maintenance and usually distance to the utility grid differentiate them from the onshore counterparts. The offshore loads can be classified based on power consumption, distance from shore, operational requirements, load cycles, and depth of operation. A significant set of representative ocean loads have been surveyed, which are classified into four main types and presented in this section based on their main application domain. Some of their characteristics are captured in Fig. 2 and Fig. 3.

A. Oil and Gas Platforms

The majority of offshore loads are represented by power consumptions associated to the Oil and Gas (O&G) industry (Fig. 1).

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Fig. 1. Snorre B O&G platform in the Norwegian North Sea (photo: courtesy of Statoil).

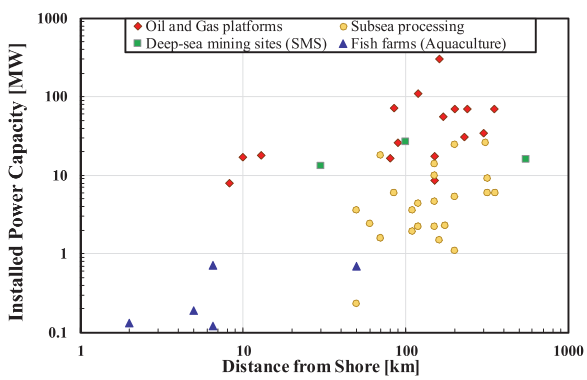

Fig. 2. Installed power capacity and distance from shore of surveyed ocean loads [15]-[61].

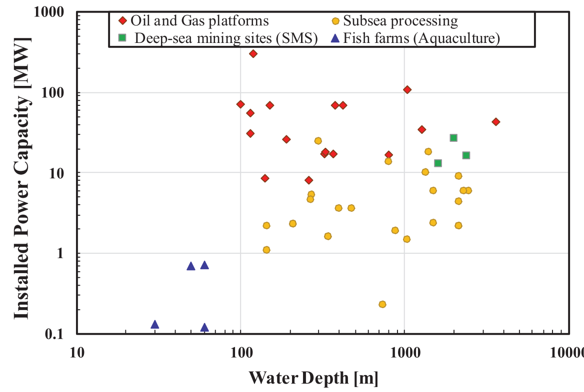

Fig. 3. Installed power capacity and water depth of operation of surveyed ocean loads [15]-[61].

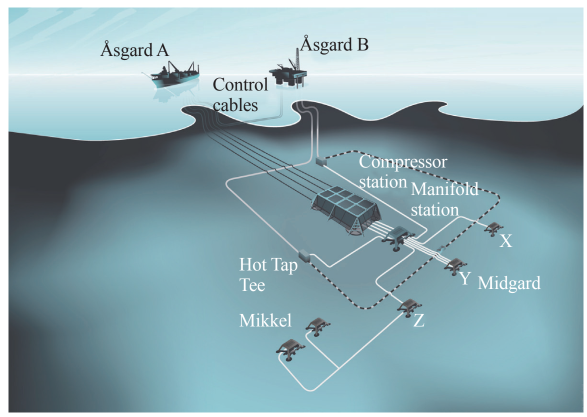

Fig. 4. Asgård gas compression station located in the Norwegian Sea at 300 m water depth with 24.4 MW power consumption (image: courtesy of Statoil).

Globally, more than 1300 O&G rigs are located offshore [62], the largest share of which are in the North Sea (185) and Gulf of Mexico (175). Although drilling an offshore well is similar to the onshore drilling process, offshore rigs face additional challenges due to the water depth (up to 3 km, and increasing, for ultradeep water applications) and the need for an anchored, stable, surface structure to host the drilling equipment and additional facilities. Moreover, compared to onshore wells, offshore O&G platforms need special equipment for oil processing and transportation after extraction. Although this significantly increases the costs (+1500%), the daily production of offshore O&G can be one order of magnitude higher than that of onshore wells and last typically for 10-20 years [63]. Typical power consumptions of offshore O&G platforms are in the range 5-300 MW [64], mostly supplied by local gas turbines [65] or diesel generators [66], [67]. Such power generation strategies cause significant greenhouse gas emissions, triggering increasing interest for more sustainable solutions. The electric distribution system of O&G platforms is characterized as a weak electric grid: power quality issues, such as high reactive power demand/low power factor [68], voltage and current harmonics, voltage notches and common mode voltages [69] may increase the losses and compromise the lifetime and operating conditions of electric components. The estimated financial loss for incidents due to poor power quality in the O&G sector is 250,000-750,000 euros per day [68]. In order to increase the energy efficiency and reduce the CO_2 and NO_x emissions, several platforms have been recently electrified, using either High-Voltage Alternating Current (HVAC) [70], [71] or High-Voltage Direct Current (HVDC) [72], depending on their power demand and distance from shore [73]. Among the advantages of "power-from-shore" solutions, in addition to high efficiency, there are high availability (~ 99%) and systems lifetime (~ 30 years), as well as reduced maintenance needs and repair time [74].

B. Subsea Processing Plants

With recent discoveries in remote and ultradeep waters and harsh environments, such as the Arctic Ocean, an additional trend in the O&G industry is to remove as many components and processing systems as possible from the floating production units and install them on the seabed (e.g. Fig. 4), reducing the required space on the platform or even removing the platform [74], [75]. Subsea processes include gas compression, boosting, water injection and separation. The main power consumptions and deployment characteristics of most of the subsea processing plants currently in operation are presented in TABLE I. Additional details can be found in [76]. Due to the extreme operating conditions, multi-MW power demands, step-out distances up to

TABLE I
CHARACTERISTICS OF THE MAIN OPERATIONAL SUBSEA PROCESSING PLANTS AS OF FEBRUARY 2017 (ADAPTED FROM [76])

	Name of the field or project	Basin/Country	Subsea power [kW]	Water depth [m]	Distance from shore [km]	Tie-back distance [km]
Gas compression	*Asgård, Midgård and Mikel fields (Fig. 4)*	Offshore Norway	24,400	300	200	40
Water injection	*Troll C pilot*	Offshore Norway	1,600	340	70	3.5
	Tordis	Offshore Norway	2,300	210	175	11
	Tyrihans	Offshore Norway	5,400	270	200	31
	Albacora- l'este field	Campos basin (BR)	3,600	400	110	9
Separation	*Troll C pilot*	Offshore Norway	1,600	340	70	3.5
	Tordis	Offshore Norway	2,300	210	175	11
	Parque Das Conchas	Campos basin (BR)	4,400	2,150	120	25
	Perdido	USA (Gulf of Mexico)	6,000	2,438	354	0
	Pazflor	Angola	13,800	800	150	4
	Marlim	Campos basin (BR)	1,900	878	110	3.8
Boosting	*Mutineer*	NW Shelf Australia	2,200	145	150	7
	Brenda&Nicol fields	UK North Sea	1,100	145	200	8.5
	Vincent	NW Shelf Australia	3,600	475	50	3
	Golfinho Field	Espirito Santo Basin (BR)	2,400	1,500	60	11
	Parque Das Conchas (ph1)	Campos basin (BR)	2,200	2,150	120	9
	Parque Das Conchas (ph2)	Campos basin (BR)	2,200	2,150	120	9
	Jubarte field	Espirito Santo Basin (BR)	18,000	1,400	70	8
	Barracuda	Campos basin (BR)	1,500	1,040	160	10.5
	Montanazo & Lubina	Mediterranean	230	740	50	12.3
	Jack & St Malo	USA (Gulf of Mexico)	9,000	2,134	320	13
	Rosa/Girasol	Angola	10,000	1,350	150	18
	Draugen	Offshore Norway	4,600	268	150	4
	Julia	USA (Gulf of Mexico)	6,000	2,287	320	27.2
	Parque das baleias	Espirito Santo Basin (BR)	6,000	1,500	85	10

tens of km, and operating water depths up to 3 km, the technology for subsea processing is continuously evolving. The entire power distribution system, either AC or DC, including umbilicals, protections, monitoring and control systems [77], [78], needs to be optimized: pressure tolerance, [79] and reliability [80] of the power electronics are the most critical concerns due to the prohibitive environmental conditions.

C. Deep-sea Mining

Apart from O&G applications, the boundaries of subsea operations and processing are now being pushed forward by the emerging of deep-sea mining [14], e.g. the extraction of seafloor massive sulfides (SMS) such as zinc, copper, silver and gold, in water depths between 1 and 4 km, at sites where the mineral concentration is much higher than in onshore mines. The first SMS deep-sea mining project, Solwara I, is supposed to start operation in 2018 offshore Papua New Guinea [58]. The mining of the selected site at 1600 mbsl will require heavy work-class Remotely-Operated Vehicles (ROVs). They will need to face the unprecedented technical challenges of excavation in hyperbaric conditions and ore transportation to the sea surface. Despite the similarity in the principle of operation, deep-sea mining may have higher power requirements than similar onshore mining applications. In particular, three different ROVs (Bulk and Auxiliary Miners and Collecting Machine), each with an installed power between 1.8 and 2.5 MW, are supposed to operate in this first project, in addition to the suction pump (>6 MW). The power generation capability of the supporting vessel is 31 MW for a nominal production rate of 1.8 million tons/year (dry equivalent) [58]. Since power consumptions and design considerations are strongly dependent on the depth of operation, subsea mining in deeper waters can be even more demanding [81], [82]. Moreover, a general trend in the ROV industry is to migrate from hybrid electric/hydraulic solutions to all-electric ones [83], since the use of hydraulics for power transmission can reduce the efficiency up to 50% [84], whereas the advantages of all-electric ROVs are: higher reliability, reduced size and weight, high efficiency and no leakage risks. Due to the absolute novelty and lack of any operational experience on any deep-sea mining projects, powering solutions based on renewable energies have not yet been considered, unlike the case of onshore mines, where sustainable power generation has been proposed [85], [86].

D. Aquaculture Applications

Although much less energy consuming compared to the previous applications, the aquaculture sector is one of the competitors for the use of the marine space and contributors to the offshore electric demand. In the aquaculture industry, there is a trend towards using more exposed coastal areas [87] and offshore locations [88] for fish farming, with the advantage of reducing key environmental effects, but with a possible increase in the local energy need.

The typical power consumption of fish farms is characterized by high variability, depending on the production cycles (e.g. hatchery/nursery, grow-out, harvesting or delivery phases), with the feeding phase accounting for up to 60% of the total energy consumption [89]. The maximum electric load is typically in the range 100-200 kW per installation, depending on size and location. Installed power can exceed three times the actual power demand, when locally supplied; whereas grid-connected solutions are now being implemented to mitigate the environmental impact of diesel generation [89].

III. Marine Renewable Energy Resources

Marine energy resources include both offshore wind and ocean renewable energy, where the latter category groups all possible green resources that stem from ocean waters, i.e. tidal energy, wave energy, ocean thermal energy conversion (OTEC) and salinity gradient. Offshore winds are steadier and more powerful than onshore ones, and their exploitation can minimize drawbacks such as scarcity of available land space and visual impact. On the other hand, the higher criticality and cost of Operation and Maintenance (O&M) in offshore wind farms (Fig. 5), typically reduces their availability to between 90% and 95%, whereas it is about 97% for onshore power plants [90]. Offshore wind turbines are following the technological trend of onshore wind, with a consistent increase in the average size and capacity of the installed wind turbines, which, in Europe, reached 5.9 MW in 2017 (+23% increase compared to the previous year) [91]. Some of the biggest challenges of offshore wind deployments compared to onshore ones lie in structural aspects, considered that wind turbine foundations represent a quarter to a third of the overall cost of an offshore turbine, for which installed strength, fatigue load, resistance to dynamic loadings, resistance to scour and corrosion are critical aspects [92]. From an electrical and control standpoint, power electronics covers 100% of the turbine installations since 2005 [93], and full scale power converters are increasing their share, especially for large turbines, although partially rated ones, used with doubly fed-induction generators, still dominate the market [94]. The largest offshore wind turbine is rated 9.5 MW [95] and, globally, the offshore wind capacity operational in 2017 exceeded 18.8 GW [96].

Feasibility and high performance of floating wind turbines, recently tested in array configuration [97], will further impulse the sector. Therefore, the offshore wind installed capacity is expected to reach 66 GW by 2030 [98].

Apart from wind, a significant amount of energy is present in ocean waters (Fig. 6). According to [99], the theoretical potential of tidal power (including tidal range and tidal currents) is 26,280 TWh/year; the corresponding potential of wave energy is 32,000 TWh/year and the theoretical potential associated to OTEC, (i.e. exploiting temperature differences above 20 degrees between surface and deep waters through thermal cycles), has been calculated in 44,000 TWh/year. Finally, salinity gradient (i.e. electricity production by osmotic processes exploiting the different concentration of salt in fresh and salt waters), could provide additional 1,650 TWh/year.

Fig. 5. Dudgeon offshore wind farm with 402 MW generation capacity located in the North Sea, England (photo: courtesy of Statoil).

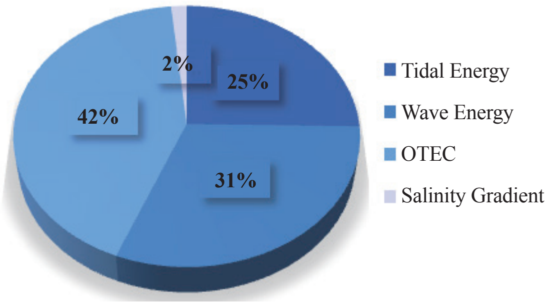

Fig. 6. Potential of ocean energy resources.

Despite the huge potential of ocean energy, the actual exploitable resource depends on the corresponding technological maturity, which is still low. Ocean thermal and salinity gradient technologies have so far been deployed only in few demonstration projects worldwide and are far from technological maturity. On the contrary, tidal energy is technologically established. Tidal barrage plants are in operation in grid connected mode both in Europe (La Rance, France, 240 MW) and Asia (Sihwa Barrage, Korea, 254 MW) [99] and tidal current harvesting has been successfully proved in several test sites [100], [101], exploiting the synergies with the wind turbines technology [99]. Wave energy was extensively researched in the last decades, but the high concept diversification [102] and need for tailored design and control solutions [103] have slowed-down the sector development, which is still at pre-commercial stage [104]. In total, in 2016, 0.5 GW of commercial ocean energy generation capacity was in operation and 1.7 GW under construction [105], 99% of which were tidal range. The estimated installed capacity of ocean energy by 2050 is up to 300 GW from wave and tidal, plus 300 GW from OTEC [102].

Other innovative renewable energy solutions have also been recently proposed to complement and diversify the offshore renewable energy portfolio. One example is constituted by floating photovoltaic plants such as those recently deployed offshore the Netherlands [106].

IV. Offshore Energy Storage

In the last years, the deployment of offshore energy storage systems (ESS) gained momentum, representing a key enabling technology for the implementation of distributed marine energy systems, in particular to mitigate the intermittency and non-dispatchability of offshore renewables. Despite the potential advantages related to the deployment close to power generation sources (i.e. reduced costs for power transmission), limited environmental and visual impact and availability of vast spaces, offshore ESS presents additional challenges compared to onshore solutions. These are due to the harsh sea environment (with risk of corrosion, chemical deterioration etc.), need of high power and energy density, low-maintenance requirements, ballasting and mooring. Still, battery solutions have been often investigated for marine applications and were recently implemented in hybrid offshore wind farms. Currently, offshore battery deployment is considered a feasible solution [107] and, from the industrial standpoint, it is seen as an extension of battery use in the maritime applications [108]. The use of fuel cells is also being considered, due to high power density and good efficiency, modularity, good dynamic load-following characteristics, and reduced emissions [109].

Apart from chemical storage, using flywheels can be a viable option [110], due to their higher lifetime, allowing a number of charge/discharge cycles in the order of 25,000-50,000. Moreover, underwater compressed air energy storage (CAES), exploiting the advantage of high hydrostatic pressure on the seabed, has been recently investigated and tested at small scale by Hydrostor [111]. Similar properties are exploited by the Underwater Pumped Hydro Storage (UPHS), as in the concepts proposed and tested by Fraunhofer institute [112], MIT [113], and other institutions worldwide [114]. Although different energy storage technologies can be considered [11] depending on the power and energy requirements of the services to be provided (as further investigated in Section V), the largest installations such as underwater CAES and UPHS face additional challenges compared to the corresponding onshore versions. These relate to the potential unavailability of vessels suitable for the deployment of large devices at water depth of hundreds of meters [115].

V. Distributed Energy Resources (DERs) to Supply Ocean Loads

The characterization of offshore/subsea electric grids as distributed energy systems was explored only recently to: 1) verify the complementarity of different offshore energy sources; 2) investigate potential, challenges and optimum sizing of ESS for ocean applications; 3) prove the suitability of offshore renewables to supply local loads, without compromising stability and efficiency of the electric grids.

In particular, [116] explores the complementarity of wind and wave energy at three different European test-sites and shows a good matching between the power production of such marine renewables and the corresponding UK electricity consumption pattern. Ref. [117] presents a similar analysis for an Irish test case. A general review of possibilities for combined wind/wave installations is contained in [118].

ESS effect on the short-term stabilization of single offshore renewable sources has been analyzed and applied, in the case of wind installations, over time intervals of 15-60 minutes (i.e. for power smoothing, frequency regulation, capacity firming etc.) in [119] and [120], as well as on longer timescales (i.e. for energy management). Studies on ESS for wave energy applications over different time horizons also exist [121]-[123]. In some cases, the analysis is extended to multiple energy resources for both short-term (power smoothing over few seconds [124]) and long-term ([125]) applications. It is worth noting that the selected domain of application for the optimal energy storage sizing is quite often that of small islands [122], [126], whose power consumption and power system challenges are, however, similar to those of isolated O&G platforms.

Whereas previous investigations on marine renewable sources and energy storage deployments targeted general offshore loads, analyses related to the use of marine renewables to meet the power consumption of specific offshore applications and the impact on the corresponding local power systems have been only recently presented. Most of the contributions target wind integration into the electric distribution systems of O&G platforms. In particular, [127] checks grid code compliance in terms of frequency and voltage stability under load start-up and loss-of-load conditions. Ref [128] considers similar scenarios, in addition to the loss-of-generation case, analyzing the integration of a large wind farm in an O&G field and performs loss analysis. In [129], voltage and frequency stability are assessed for multiple test cases, and NO_x and CO_2 emissions reduction due to wind connection is quantified. The effect of short term wind variability, however, was only taken into account in [130] and [131]: [130] is a basic energy analysis, whereas [131] includes voltage and frequency stability studies under rapidly varying wind conditions, with the goal of assessing grid code compliance, according to the IEC-61892 standard.

Finally, possible stability risks due to electro-mechanical oscillations are addressed in [132] and load management is proposed as a mitigation measure.

The use of wind power to supply subsea equipment, i.e. water injection systems, was proposed by DNV GL and found technically and economically feasible by the joint industrial project WinWin [133]. Moreover, various techno-economic studies to quantify the advantages of supplying aquaculture installations with renewable energy exist. In particular, [134] and [135] evaluate the potential of multiple energy sources (wind, ocean, micro-hydro, solar, etc.) to cover the power need of realistic fish-farms. Plans for a pilot-project using wave power to supply fish farms were proposed by Albatern in [136], whereas the use of a small-scale OTEC system for seaweed production was tested in [137]. TABLE II surveys the main aspects of subsea/offshore DER systems and related grid services investigated in recent studies.

VI. Emerging Trends in Offshore and Subsea Grids

The development of offshore and subsea electric grids, with high degree of flexibility and interconnection can be expected

TABLE II
Survey of the Main Studies Investigating Aspects of Subsea/Offshore DER Systems and Related Grid Services

	Major offshore loads					Marine renewable generation					Offshore storage			
Considered services	Generic loads	Oil and Gas platform	Subsea processing	Deep-sea mining	Aquaculture	Wind energy	Wave energy	Tidal energy	Solar energy	OTEC	Generic ESS	Batteries	CAES/ UPHS	Fly-wheels
Power smoothing	[121] [123]					[107][124] [125]	[121][123] [124][125]				[121] [125]	[107]	[123]	
Variability reduction	[116]					[116][117]	[116][117]							
Loss reduction/ Efficiency improvement		[128] [131]	[74]	[81]	[89] [134] [137]	[89] [107] [128] [131] [134]	[134]		[134]	[137]		[107]		[110]
Voltage stability		[64][65] [127][128] [130]				[64][127] [128][130]								
Frequency stability		[64][65] [127][128] [130]				[64][127] [128][130]								
Power quality evaluation (flicker/harmonic etc.)		[69]	[74]					[100]						
Energy management	[122]				[134] [135] [136]	[122][126] [134][135]	[122][126] [134][135] [136]	[135]	[134] [135]		[120] [122] [126]			
Load management		[132]				[132]								
CO_2-NOx Emission reduction		[64][130] [131]	[133]			[64][130] [131][133]		[101]						

in the next years, and increased monitoring [138] and control [139] capabilities will underpin the *digital transformation* [140], [141] in the offshore sector. Among the emerging trends in the deployment of such systems, *distributed energy storage integration* is ongoing, which will help mitigating renewable energy intermittency and power quality issues in the local grids. This will extend the *pervasive use of power electronics,* used for renewable energy grid integration, electric drives for ocean loads and, potentially, power conditioning for power quality enhancement. Power electronics for ocean applications will require new solutions in terms of pressure [142] and fault tolerance [143], component miniaturization and physic of failure approach for reliability analyses [144]. Furthermore, the *interconnection* of otherwise-isolated offshore electric distribution systems to *offshore HVDC and HVAC grids* will push the innovation from component-level to system-level. Considering the increasing number of offshore HVDC deployments [145], *Medium Voltage DC grids*, already emerging in the maritime sector [146], could be extended to some offshore and subsea systems [147], [148].

VII. Conclusions

The paper offers an up-to-date review of the main offshore and subsea applications. It shows the evolution of marine renewable sources and energy storage systems, outlining how their synergy can be the enabler of the ocean space energization and the adoption of smart grid models in the marine environment.

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Reconfiguration of NPC Multilevel Inverters to Mitigate Short Circuit Faults Using Back-to-Back Switches

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***Abstract*—The main focus of this paper is to propose a reconfiguration method to mitigate short circuit faults in a neutral point clamped multilevel inverter which is widely used as a power conversion system with distributed energy resources. Existing reconfiguration methods use either a redundant strategy or need a large number of additional devices pre-installed in the circuit; these will increase the bulk and complexity of the system. Most existing control-strategy-based methods distort the phase-to-neutral voltage, which results in degradation of power quality. To maintain control-strategy-based reconfiguration, avoid significant change to the circuit topology, and avoid phase voltage distortion, a new and practical reconfiguration method is proposed in this paper. The proposed method is applicable to neural point clamped (NPC) multilevel inverters at any voltage level and can mitigate short circuit faults in any device. A technique of switching series connected switches is selected to combine with the proposed reconfiguration method since it's a practical design consideration for realistic implementation. MATLAB/Simulink is used to simulate a five-level NPC inverter with non-idealities to verify the proposed reconfiguration method. A five-level NPC is also built and tested to experimentally verify the proposed method. Short circuit faults are injected to different devices and the proposed method is verified to quickly and effectively recover the NPC inverter from these faulty conditions.**

***Index Terms*—Fault tolerance, multilevel inverter, reconfiguration, short circuit fault.**

I. Introduction

SINCE many industrial applications require medium to high voltage, multilevel inverters (MLIs) have been widely usedin industry to sustain higher voltage stress due to their cascaded per-phase structure. Other advantages of MLIs include lower common-mode voltage, operation under both high and low switching frequencies, and lower total harmonic distortion (THD) [1]. MLIs have been widely utilized as power converters for distributed energy resources such as in wind energy systems [2], [3] and solar energy inverters [4], [5]. Due to the cascaded structure, more complex control strategies and more semiconductor devices are used in MLIs. The increased number of semiconductor devices increases the risk of failure since the failure of a single device could cause the whole inverter to fail. Researchers have studied the reliability of power electronics to a great extent in an attempt to reduce the risk of failure and to increase the reliability of power electronic systems for distributed energy resources[6], [7]. The most common faults that may occur in MLIs are open and short circuit faults in power switches [8]. One of the most common causes of semiconductor device degradation and failure is related to dielectric breakdown, which could cause the gate voltage to lose control over the collector current, causing a short circuit fault [9]. The short circuit circulation path could cause extra electric stress on other devices or a short circuit condition on the source side; this could result in severe damage to the inverter, source, and load when compared to open circuit faults. To avoid such damage, the redundancy provided by the increased number of semiconductor devices in MLIs is utilized by researchers to develop many effective methods to reconfigure MLIs to recover from faults.

The proposed reconfiguration method can effectively mitigate the most severe fault condition of semiconductors, i.e., short circuit fault. The proposed reconfiguration method can be activated by the trigger signal generated by any fault diagnosis or prognosis method. Compared to the existing reconfiguration methods, which utilize redundancy control strategies or add-on components, the proposed reconfiguration method has less additional components, and unlike some existing methods which also utilize less additional components, the proposed reconfiguration method maintains the peak value of output voltage in the reconfigured condition. The proposed reconfiguration method does not sacrifice the power quality of phase-to-neutral voltage or phase current, which typically occurs in the existing control-strategy-based reconfiguration methods. Further details on related literature and the advantages of the proposed method are shown in Section II. Also in Section II, more background is provided on neutral-point clamped (NPC) MLIs. Section III introduces the principle of the proposed reconfiguration method and a selected voltage balancing technique to achieve the synchronization of series-switched devices. Section IV shows simulation results to verify the proposed reconfiguration method. In Section V, experimental results of implementing the proposed reconfiguration method and the selected voltage balancing technique in a 5-level NPC inverter are shown. Section VI concludes the paper.

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II. Background

A. Post-Fault Reconfiguration Methods in MLIs

The NPC inverter was introduced 36 years ago [10], [11] and is the most widely used topology in industrial applications [12]. A 3-level example is shown in Fig. 1 for illustration. Therefore, many post-fault reconfiguration methods have been developed to ensure continuous operation of NPC inverters. NPC inverters can be switched by sinusoidal pulse width modulation (SPWM) or space vector modulation (SVM) [13]. In SVM, when device failure happens, some voltage vectors cannot be achieved, thus redundant vectors are utilized to compensate for the lost vectors [14], [15]. An effective way to tolerate device failure is to tie the phase which contains the failed component to the neutral point, change the control strategy and operate the two remaining healthy phases to achieve the balanced phase-to-phase voltage [16]-[21]. Another way is by changing the diodes D_1 to D_2 in Fig. 1 to controllable semiconductor devices and utilizing the flexible current path to tie the phase containing the failed component to the neutral point [22]. When the diodes are changed to controllable semiconductor devices, the NPC inverter is modified to become an active-NPC (ANPC) inverter. Redundancy is always a straightforward way to replace the failed device with a new one. This method has been used in other power electronic circuits [23], [24] and is a potential method for MLIs' recovery. Researchers have successfully achieved maintaining the inverter output waveform in fault-tolerant mode with a forth leg installed in the NPC inverter [25]-[28]. Even though the complexity is increased, the output waveform is effectively maintained after a failure occurs in one phase. A promising method in [29] has minor modification of the standard topology shown in Fig. 1; it utilizes fuses which are installed in series with the diodes D_1 and D_2 to disconnect diode legs, then the circulation of fault current is stopped when a short circuit happens.

Many effective reconfiguration methods for MLIs have also been achieved for different topologies. For MLIs which consist of cell units, such as cascaded H-bridge inverters, the failed cell can be bypassed, and the control scheme is modified to provide a balanced phase-to-phase voltage [30], [31]. To minimize the add-on components in a reconfigurable circuit, some control-strategy-based reconfiguration methods have been developed. Reconfiguration of carrier-based modulation strategy can effectively balance the phase-to-phase voltage after a failure occurs, and there are no additional components required in this method [32]. Due to the particularity of flying capacitor MLIs, a control-strategy-based reconfiguration method with minimum add-on component was proposed in [33], the same output voltage levels are achieved with subtraction of capacitor voltage in post-fault condition. For three-phase systems, when one device fails, the corresponding phase leg also fails and may cause unbalanced voltages and currents among phases; a neutral-shifted method was developed to handle the unbalanced condition [30], [34], [35]. These control-strategy-based reconfiguration methods are designed for different topologies and can reduce the complexity and cost of MLIs significantly. More details of reconfiguration of MLIs can be found in [36].

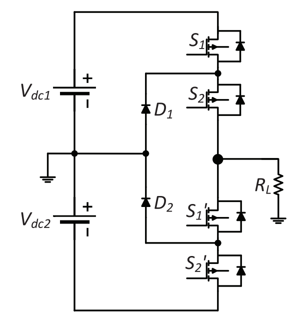

Fig. 1. Single Phase of a Three-level NPC.

Most of the existing reconfiguration methods for NPC have limitations: The SVM-based methods [9], [10] cause extra switching stress for the remaining healthy devices, and complexity of SVM-based methods increases dramatically with the level of MLIs. Tying the whole phase leg which contains only one failed device to the neutral point is not cost effective [16]-[21]. For example, if S_1 in Fig. 2 fails, the output of this phase leg is tied to V_3 to disable this phase leg even though the seven other devices are still in healthy condition; the inverter is thus operated with the remaining two phase legs to achieve a balanced phase-to-phase voltage. Also, after tying the failed leg to neutral, reduced peak value of the output voltage is observed. The ANPC with fault tolerance ability also has the problem of reduced peak output voltage and it is not applicable to various levels besides a 3-level ANPC inverter [22]. Redundant components [23], [24] and forth leg-based methods [25]-[28] are not cost effective since in MLIs, a large number of additional components is required. For the effective method in [29], complex circuitry and additional components are necessary to isolate the failed device or fault current circulation pass.

Existing methods for other topologies typically need additional devices installed in the power circuit even though they are not necessary for the original healthy operation: Additional switches or contactors are pre-installed in the circuit to disconnect the failed cell; these act as bypass contactors to bypass a failed cell or switch; for example, if an H-bridge cell in a cascaded MLI fails, a contactor is used to short the output sides of the failed cell to bypass it, which means that for each unit cell, a contactor should be installed [30], [31]. These cell-bypassing methods rely on the inverter topology, so they are not applicable to the widely-used NPC inverters. The method developed in [33] is only applicable to flying capacitor MLIs. While some control-strategy-based methods can be utilized in NPC inverters and do not require additional components, the reconfigured system typically has a distorted phase voltage and only phase-to-phase voltage is maintained; for example, if S_1 in Fig. 1 fails as an open circuit fault, V_{dc1} is lost in this phase, then the reference waveforms of the other two phases are modified accordingly to achieve the same phase-to-phase waveform [32]. This could cause significant degradation of voltage quality when phase voltage is of interest for grid-tied application, per-phase analysis, modeling, etc. Similar conditions of distorted phase-to-neu-

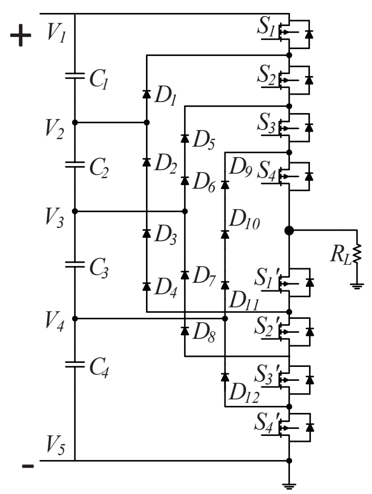

Fig. 2. Five-level NPC.

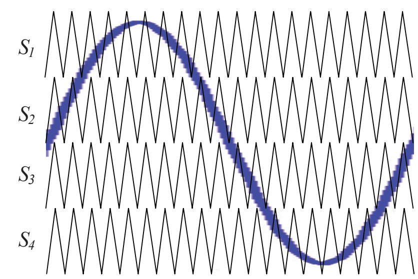

Fig. 3. Level shifted PWM for five-level NPC.

TABLE I
FIVE-LEVEL OPERATION

S_1	S_2	S_3	S_4	Output Voltage
1	1	1	1	V_1
0	1	1	1	V_2
0	0	1	1	V_3
0	0	0	1	V_4
0	0	0	0	V_5

tral voltage happen with the neutral point shift (NPS) method [30], [34], [35].

Therefore, we propose a reconfiguration method that is applicable to mitigate short circuit faults in NPC inverters, and which provides simplicity, ease of implementation, and effectiveness while requiring minimal additional components. The proposed method is applicable to *any-level* NPC inverters, maintains the peak output voltage value, and retains balanced phase-to-neutral and phase-to-phase voltages and currents, simultaneously.

B. NPC MLI Background

The NPC inverter utilizes DC link capacitors to provide various voltage levels and uses proper switching actions of semiconductor devices to transmit the voltage levels to the load. The desired number of voltage levels determines the required number of semiconductor devices and DC link capacitors. Suppose the voltage level is N, then the number of semiconductor switched per leg is $2N$-2 and the number of DC link capacitors is N-1. The topology of a single phase five-level NPC is shown in Fig. 2, as this is the inverter topology used for simulation and experimental results in this paper. Level-shifted PWM is the control scheme used, where switching signals are generated by comparing a sine wave with four level-shifted sawtooth waves with same peak-to-peak values but different offsets [37]. The generation of level-shifted PWM for a five-level NPC is shown in Fig. 3. TABLE I summarizes the five-level operation. The generated PWM signals are sent to S_1 to S_4 in Fig. 2 and their conjugates are sent to S_1' to S_4', respectively.

III. Proposed Reconfiguration Method

A. Proposed Method

The proposed reconfiguration method utilizes the structure of the NPC inverter to reconfigure it from the original voltage level to a decreased voltage level. In this way, even though the number of voltage levels is decreased, the balanced conditions of both phase-to-phase and phase-to-neutral voltages are maintained. A five-level NPC inverter is used as an example to illustrate the proposed reconfiguration method. The proposed method requires installing a back-to-back switch pairs in the lines of different input voltage levels as shown in Fig. 3 where the back-to-back switch pairs are S_a-S_b, S_c-S_d, and S_e-S_f. It should be noted that the back-to-back switch pairs use semiconductors which allow for a fast transition from the failed condition to the decreased-level condition and limit any propagation of the fault current. However, these switches can also be replaced by contactors or relays if they can also provide a fast response. For example, if S_2 in Fig. 2 fails as short circuit fault, when S_3 and S_4 are in on-state, instead of transmitting V_3 to the load, a current from V_2 will flow to the load through D_1, S_2 to S_4. So, the back-to-back switches are used to stop the circulation pass of fault current from blocking the desired voltage.

In healthy condition, the switches S_a to S_f are turned on to ensure the transmission of different voltage levels. Suppose a short circuit fault happens to switch S_1 in Fig. 4(a) as shown in Fig. 4(b); the voltage level V_1 which is supposed to be blocked by S_1 will be passed through S_1, and as a result the diode D_1 will block the lower voltage level V_2. This causes a loss of voltage level V_2, which results in an unbalanced condition. Due to the symmetric configuration of the NPC inverter, the circuit is able to be reconfigured to a decreased level NPC inverter by switching S_1 and S_2, S_3 and S_4, S_1' and S_2', S_3' and S_4' in four pairs which are highlighted by four green dotted rectangular boxes as shown in Fig. 4(c), and turning off S_a, S_b, S_e and S_f as shown in Fig. 4(d). In Fig. 4(d), D_1 to D_4, and D_9 to D_{12} are also disabled with turning off S_a, S_b, S_e and S_f. The disabled components are marked as gray, and the equivalent circuit in reconfigured condition is also shown in Fig. 4(d). The three-level operation in a five-level NPC inverter is listed in TABLE II. As with other reconfiguration methods, the trigger signal of back-to-back switches should be from a fault diagnosis or prognosis algorithm which is used

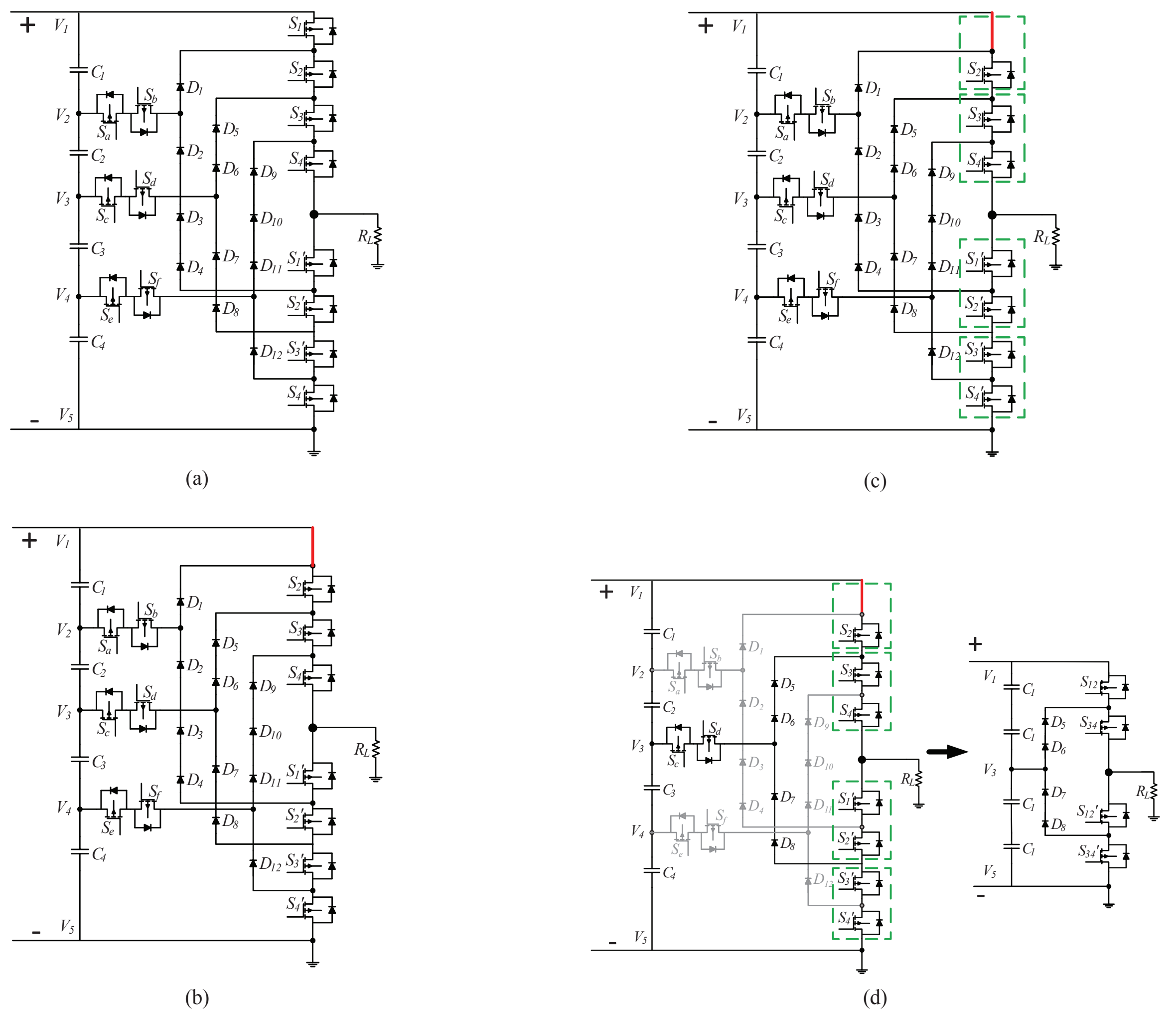

Fig. 4. Proposed topology (a) Healthy condition, (b) Short circuit fault in S_1, (c) Switching in pairs, (d) Fully reconfigured condition with turning off back-to-back switches S_a, S_b, S_e and S_f.

TABLE II
THREE LEVEL OPERATION IN A FIVE-LEVEL NPC

S_1	S_2	S_3	S_4	Output Voltage
1	1	0	0	V_1
0	0	1	1	V_3
0	0	0	0	V_5

to initiate the reconfiguration process. For example, diagnosis methods that have been explored by the authors and which complement this work are shown in [38]. Therefore, the shorted condition of any switch can be considered a passthrough since switches can be paired to tolerate the short circuit condition, and the short circuit path to the source is eliminated by the back-to-back switches.

Even though the voltage level is decreased, the unbalanced condition caused by the short circuit fault is resolved with very limited additional components. The redundancy strategy and forth leg methods can maintain the same voltage level in the post-reconfigured condition [25]-[28], but many more additional components and complicated control strategies are necessary when compared to the proposed method. The ANPC can achieve balanced phase-to-phase voltage without additional components, but it disables the remaining healthy components in the failed leg which is not cost effective. The peak value of output voltage is also reduced significantly [22]. The NPS method achieves a decreased level condition in the failed phase leg without any additional components [30], [34], [35]. However, it also reduces the RMS value of the phase voltage and it is more applicable to open circuit faults of MLIs that contain unit cells. The number of the back-to-back switches is determined by the voltage level of the NPC inverter, if the original voltage level is N, then the required number of back-to-back switches is N-2. This applies to both single-phase, three-phase, or higher phase NPC inverters since the back-to-back switch pairs are shared by all phases. With the N-2 back-to-back switches, the N-level NPC can be reconfigured to different voltage levels.

Suppose that the reduced voltage level is M; if (N-1)/(M-1) is an integer, then an N-level NPC inverter can be reconfigured to M level NPC inverter. The achievable voltage levels of different Llevel NPC inverter are summarized in TABLE III. A drawback of the proposed reconfiguration method is that the sustained

TABLE III
SUMMARY OF ACHIEVABLE VOLTAGE LEVELS

Original Voltage Level	Reduced Voltage Level
3	2
4	2
5	3 & 2
6	2
7	4 & 3 & 2
8	2
9	5 & 3 & 2
…	…

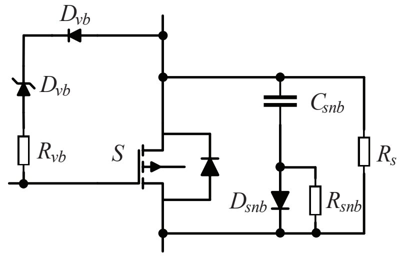

Fig. 5. Hybrid voltage balancing circuit.

voltage of the semiconductor which is in pair with the failed semiconductor is doubled, so the used semiconductor should have higher voltage rating.

B. Synchronization of Series-Switched Devices

The proposed reconfiguration method requires switching series-connected devices, so voltage balancing problems should be considered. When there is a difference in turn-on and turn-off switching times among devices, the voltage of each device will be different, which causes extra voltage stress on some devices [39]. Unbalanced voltage sharing can also be caused by spread of device dynamic and static parameters [40]. To resolve this issue, a proper voltage balancing technique for series-connected semiconductors is chosen. Two main considerations are 1) The voltage balancing technique should use a separate gate driving circuit for each device since one driving circuit for several semiconductors is not applicable to the original healthy operation (an example technique that is not applicable here is shown in [41]); 2) The voltage balancing technique should not have the components which are not necessary for the original healthy operation. Taking both considerations into account, a hybrid voltage balancing method for series-connected semiconductors in [40] is chosen. This method has not been implemented in MLIs but in this paper, it is successfully implemented in an NPC inverter and contributes to balance the voltage of the series-switched devices. The hybrid technique consists of an active voltage clamping circuit and a passive snubber circuit. The circuit for the hybrid technique is shown in Fig. 5, and each semiconductor will be modified as such. Even though the voltage clamping circuit and snubber circuit are added into each switch, they are not only helpful for synchronizing and balancing series-connected switches, but also improve the performance of original healthy operation such that when more than two switches are off, the sustained voltage of each switch is balanced.

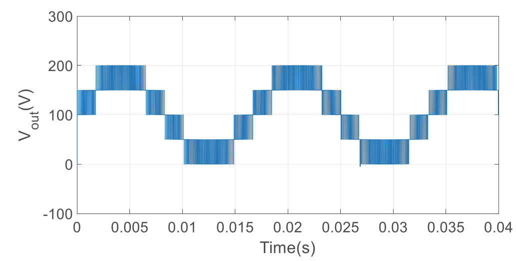

Fig. 6. Output waveform of healthy condition.

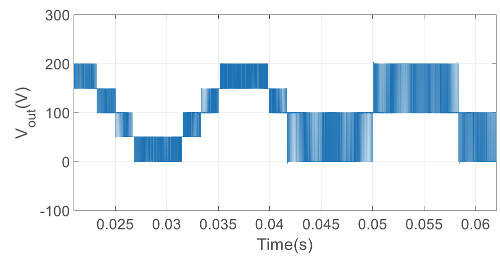

Fig. 7. Output waveform of transmitting healthy condition to reconfigured condition.

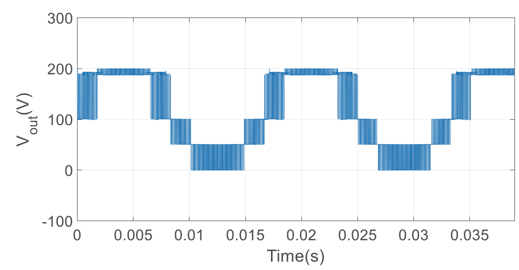

Fig. 8. Output waveform of S_1 short circuit fault.

IV. SIMULATION RESULTS

Simulation in MATLAB/Simulink are first performed to verify the proposed reconfiguration method. A five-level NPC with the same topology as Fig. 1 is built and the switching scheme is level-shifted PWM. For illustration purposes, the DC bus voltage is 200 V, switching frequency is 10 kHz, and fundamental frequency is 60 Hz. The healthy five-level operation output voltage waveform is shown in Fig. 6. Note that the voltages have a DC offset since the reference point is chosen at the negative DC bus side as shown in Fig. 1.

The proposed reconfiguration method is implemented when the circuit is in healthy state; the transition from healthy condition to reconfigured condition is shown in Fig. 7. The distorted phase-to-neutral output waveforms caused by short circuit fault on S_1 and S_3 are shown in Fig. 8 and Fig. 9, respectively. The proposed reconfiguration method is thus implemented when the short circuit in S_1 and S_3 is mitigated using the proposed method as shown in Fig. 10 and Fig. 11, respectively. In Fig. 10 and Fig. 11, the short circuit had occurred before the shown

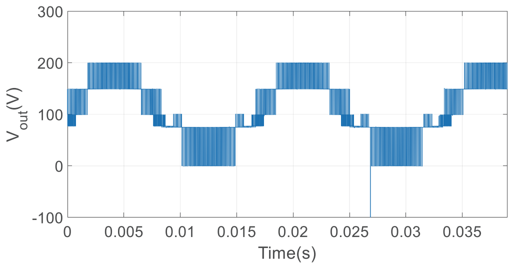

Fig. 9. Output waveform of S_3 short circuit fault.

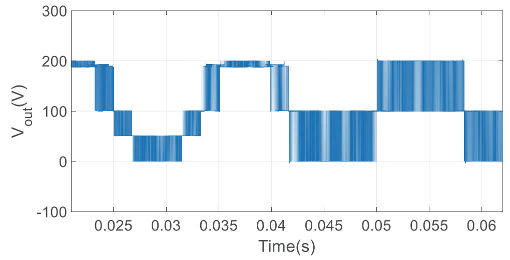

Fig. 10. Output waveform of transmitting S_1 short circuit condition to reconfigured condition.

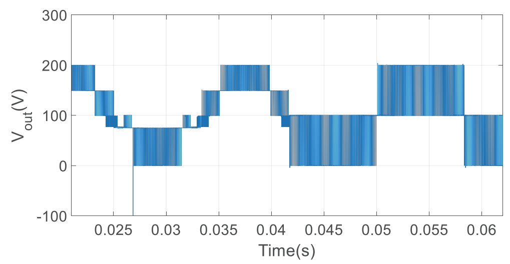

Fig. 11. Output waveform of transmitting S_3 short circuit condition to reconfigured condition.

Fig. 12. Isolated power supplies.

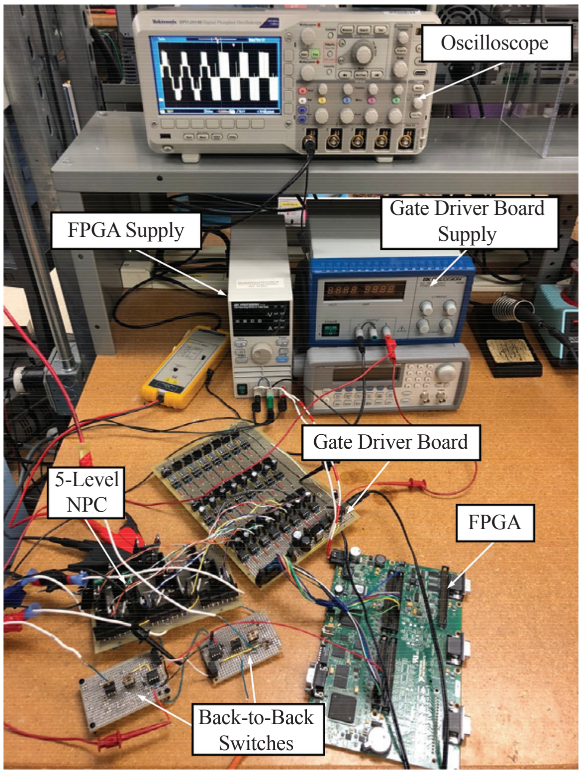

Fig. 13. Hardware Setup.

time scale, and the reconfiguration method is engaged at 42 ms. Results show that the proposed method can be successfully implemented while the circuit is in healthy or failed conditions and indicates that the proposed method can be integrated with either fault diagnosis methods or fault prognosis methods before a fault occurs. The proposed method can clearly balance phase-to-neutral voltages while requiring minimal circuit modification. Experimental verification will also illustrate the voltage balancing and switch synchronization, which is not required but an added benefit to the proposed method.

V. Experimental Verification

A. Experimental Results of a Five-Level NPC Inverter

A five-level NPC inverter which has the same topology as Fig. 1 has been built in hardware. The four isolated DC supplies are shown in Fig. 12 to eliminate the voltage balancing need across capacitors. The whole setup is shown in Fig. 13, with one phase of the inverter used for demonstration purposes. LabView software is used to generate the level-shifted PWM signals and communicate with gate driver board through NI FPGA. The platform performs well in healthy condition with 200 V DC bus and 200 Ω load as shown in Fig. 14. A low voltage condition of 60 V is used when implementing the proposed reconfiguration method to limit the short circuit energy during test; a transient of implementing the proposed method in healthy condition is shown in Fig. 15.

The first step in verifying the proposed method is to ensure that synchronous switching and voltage balancing across series devices is achieved. For this purpose, the hybrid voltage balancing technique in [40] is implemented in the five-level NPC inverter. Fig. 16 shows the experimental results of the unbalanced condition of S_1 and S_2 drain-to-source voltages without the hybrid voltage balancing technique. Fig. 17 shows the balanced

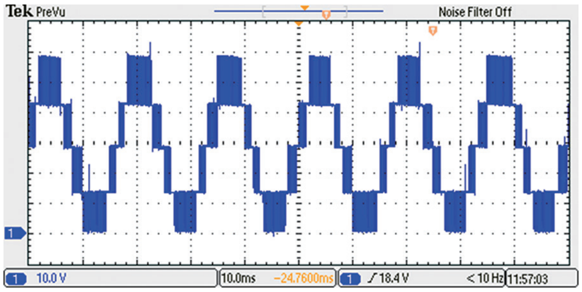

Fig. 14. Healthy operation with 200 V DC bus (10 V/div, 10 ms/div).

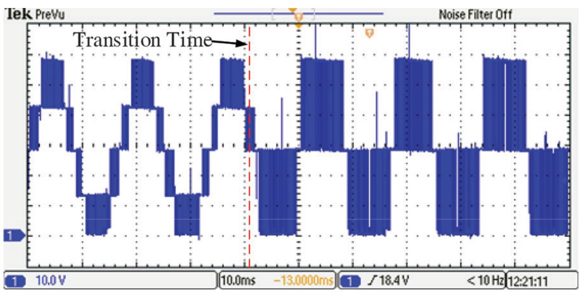

Fig. 15. Phase-to-neutral voltage when implementing proposed reconfiguration method in healthy condition (10 V/div, 10 ms/div).

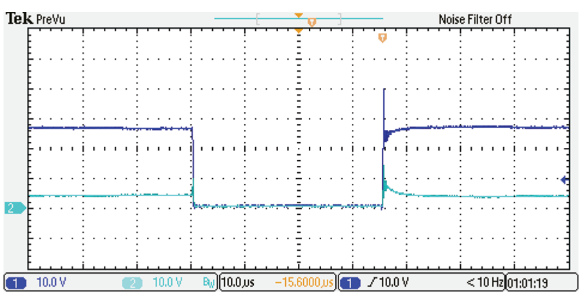

Fig. 16. Unbalanced condition of S_1 and S_2 voltage (10 V/div, 10 µs/div).

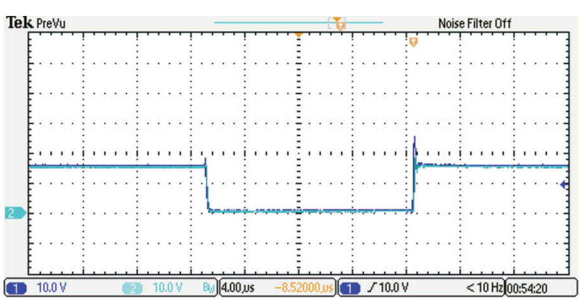

Fig. 17. Balanced condition of S_1 and S_2 voltage (10 V/div, 4 µs/div).

condition of S_1 and S_2 drain-to-source voltages with the hybrid voltage balancing technique. Fig. 16 and Fig.17 verify the effectiveness of the synchronization and hybrid voltage balancing technique in the NPC inverter, and ensures that the proposed method is now applicable.

For validation purpose, the five-level NPC inverter is reconfigured to a three-level when a short circuit fault happens, and only S_a, S_b, S_e, S_f from Fig. 4(a) are actually installed to stop

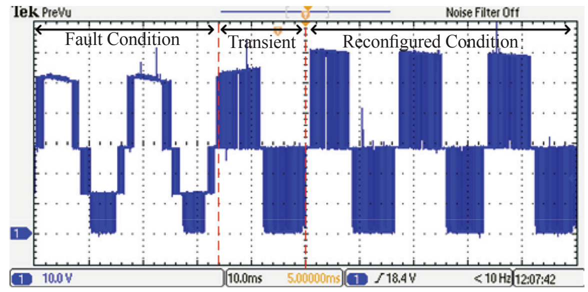

Fig. 18. Phase-to-neutral voltage when implementing proposed reconfiguration method in S_1 short circuit fault (10 V/div, 10 ms/div).

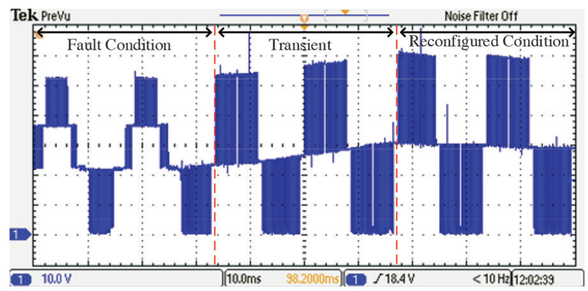

Fig. 19. Phase-to-neutral voltage when implementing proposed reconfiguration method in S_3 short circuit fault (10 V/div, 10 ms/div).

the fault current path. The proposed reconfiguration method is implemented when the short circuit fault happens to S_1 or S_3. Fig. 18 shows the transient of implementing the proposed reconfiguration method when S_1 fails as a short circuit, Fig. 19 shows the transient of implementing the proposed reconfiguration method when S_3 fails as short circuit. In both Figures, the short circuit fault had occurred before the first two cycles shown, and at the beginning of the third cycle, the proposed method is engaged. Waveform deflection is observed during the transient period, which may be due to parasitic elements and/or signal propagation delay. These result in unsynchronized turning off the back-to-back switches while changing control of semiconductor devices to pairs. After the short transient period, the MLI is reconfigured to the decreased-level condition. The method is shown to successfully maintain symmetry in the phase-to-neutral voltage after being distorted by the short-circuit fault. Therefore, the proposed reconfiguration method successfully reconfigures the failed inverter in a fraction of a fundamental cycle. The inverter can then maintain load support and operate in a decreased level condition with balanced phase-to-neutral voltage unlike other existing methods and maintains balanced drain-to-source voltages across series switches as needed.

B. Summary: Comparing the Proposed Method with State-of-the-art

To summarize the state-of-the-art of the proposed reconfiguration method, the shortages of existing reconfiguration methods are checked first. The SVM-based method [14], [15] has more complex control in the reconfigured condition, and utilizing the redundant vector means more switching actions are assigned to the remaining healthy devices which causes extra stress on

TABLE IV
COMPARISON OF DRAWBACK OF PROPOSED METHOD AND EXISTING METHODS

	Proposed Method	*SVM*	*IFPL*	*ANPC*	*CLR*	*FLB*	*FUI*	*FCI*	*FCV*	*MRS*	*NPS*
Reduced Peak Value			•	•						•	•
Unbalanced Per-phase Condition			•	•						•	•
Excessive Add-on Components					•	•	•	•			
Excessive Complexity of Control		•		•			•				
Extra Stress on Devices	•	•					•	•			
Not Applicable to NPC Inverters								•	•		
Not Applicable to Different Levels				•							

these devices. The method of isolating a faulty phase leg (IFPL) [16]-[21] has the drawbacks of reduced output voltage peak and unbalanced per-phase voltages, since the MLI is operated with only two phases. The ANPC fault-tolerant inverter [22] has the same drawbacks of IFPL and since it has additional switching devices, the control complexity is increased. This ANPC fault tolerant inverter is only applicable to a 3-level condition, which means that it is not applicable to the MLIs with other voltage levels. The component-level redundancy (CLR) strategy [23], [24] is not feasible for MLIs since the number of semiconductor devices is very large. The forth-leg-based (FLB) method [25]-[28] has a redundant phase leg, which is not cost effective. The method of utilizing fuses to isolate a faulty device (FUI) [29] has many of add-on components, complex control and extra stress on the remaining healthy devices. The faulty cell isolation method [30], [31] requires additional components installed in each unit cell which is not cost effective, and remaining healthy devices in reconfigured condition will have more voltage stress; also, since this method is only applicable to MLIs which contain unit cells, it is not applicable to NPC inverters. The method of utilizing different voltages of flying capacitors (FCV) [33] is only applicable to flying capacitor MLIs. The method of modifying the reference signal (MRS) [32] does not require add-on components and is easy to achieve, but it causes reduced output voltage peak and unbalanced per-phase condition. The NPS method [30], [34], [35] also has the drawback of reduced output voltage peak.

TABLE IV summarizes the drawbacks of the existing reconfiguration methods and compares these methods with the proposed method. Most of the existing methods have more than two drawbacks, and even though the CLR and FLB only have one drawback, the excessive add-on components significantly increase the system cost. Also, FCV is not applicable to NPC inverters. CLR, FLB, FUI and FCI require add-on components where the number of components increases with the increased voltage levels and if it is a three-phase system, the required number of components is tripled. However, the number of additional components per phase in the proposed method is less than any of these four methods and is not affected by the number of phases, which reduces the total number of additional components significantly. The only drawback of the proposed method is extra voltage stress on the remaining healthy devices in reconfigured condition, which also appears in some of the existing reconfiguration methods.

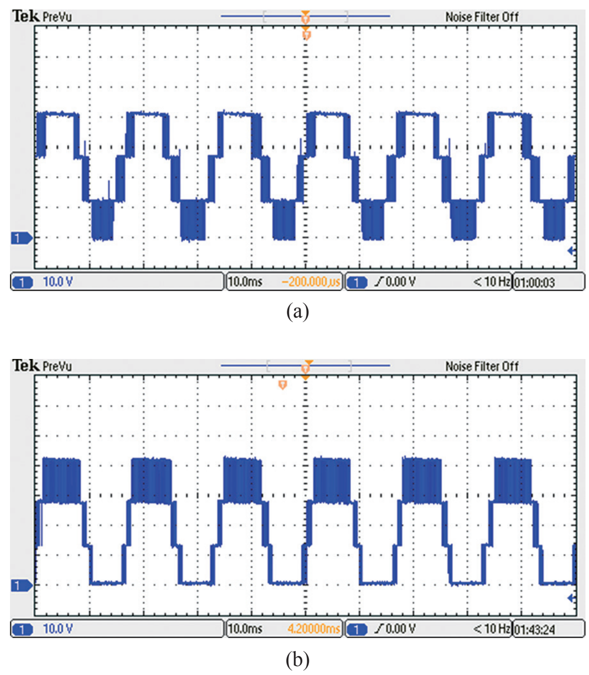

Fig. 20. Phase-to-neutral voltage when implementing MRS method (a) ALM (b) 120° DPWMMIN (10 V/div, 10 ms/div).

Among the existing reconfiguration methods, MRS and NPS are control-strategy-based methods, which do not require additional components and are easy to achieve. These two methods gain the most interest to compare with the proposed method. The decreased peak value of output voltage is an issue when the load requires a stable voltage level. The distorted per-phase waveform is as issue in the following conditions: 1) per-phase analysis of Y-connected loads, 2) unbalanced load conditions with neutral current flow, 3) grid-interconnection standards that limit the line-to-line voltage maximum (e.g. IEEE1547 and AS4777). To better understand the output voltage distortion using both MRS and NPS methods, the phase-to-neutral waveforms of these two methods are generated experimentally and are shown in Fig. 20 and Fig. 21, respectively. It should be noted that both the amplitude-limited modulation (ALM) and 120° discontinuous pulse width modulation minimum (DPWMMIN) modulation methods shown in Fig. 20 as subcategories of the

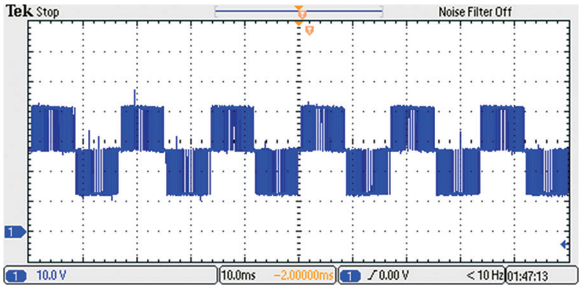

Fig. 21. Phase-to-neutral voltage when implementing NPS method (10 V/div, 10 ms/div).

MRS method. From the figures, it can be observed that the peak value of the per-phase voltage is reduced significantly, and unbalanced condition happens. The NPS method seems to have a balanced phase-to-neutral voltage waveform, but the voltage waveforms of the other two phases remain the same, which causes an unbalanced condition between the three phases.

VI. Conclusion and Future Work

A practical reconfiguration method for short circuit faults in NPC MLIs is proposed in this paper, which overcomes several weaknesses of existing reconfiguration methods. The proposed reconfiguration method is applicable to any NPC MLI with any number of voltage levels and can mitigate short circuit faults on any device. Simulations are shown to verify the effectiveness of the proposed reconfiguration method. A hybrid voltage balancing technique is selected and implemented to enhance the performance of the proposed reconfiguration method. A single-phase hardware platform is built and tested in healthy condition and reconfigured condition to demonstrate the effectiveness of the proposed method in mitigating short circuit faults. Future work focuses on achieving the proposed reconfiguration method at higher power and augmenting a fault diagnosis method to engage the proposed method.

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SPICE Modeling of SiC MOSFET Considering Interface-Trap Influence

Yuming Zhou, Hangzhi Liu, Tingting Yang, and Bing Wang

***Abstract*—SPICE modeling of silicon carbide (SiC) MOSFET considering the influence of interface traps has been carried out, which is able to describe the characteristics of the MOS transistors in all operation modes at different interface trap densities and measurement temperatures. This modeling employs the SPICE level-1 model of MOSFET, but the constant mobility in the piecewise current equations has been replaced by the advanced mobility expression, which can exactly reflect the effect of SiC/SiO$_2$ interface traps on the electrical characteristics of SiC MOSFET. Key parameters in the advanced mobility model are obtained according to charge-sheet model (CSM) of MOS system. The static characteristics of the developed SiC MOSFET model have been validated with the production Datasheet, and the dynamic characteristics have been experimentally verified in Boost converter. Based on the developed model, the effect of SiC/SiO$_2$ interface-trap densities on the switching performances of SiC MOSFET has been quantitatively discussed, and reasonable gate driving voltage of SiC MOSFET with different interface-trap densities has been revealed.**

***Index Terms*—Interface traps, mobility, SiC MOSFET, SPICE modeling, switching loss.**

I. Introduction

RECENTLY, significant efforts have been made to improve the performance efficiency of semiconductor devices applied in power conversion systems. The wide band-gap (WBG) material silicon carbide (SiC) has demonstrated great promise to improve the limitations associated with the current rate of the technology for silicon (Si) power devices [1], [2]. SiC can provide satisfactory performance under high switching frequency applications [3]-[6], thus enabling the use of smaller filter components within the converter circuits. This points to the ability of power devices based on SiC to potentially optimize the power density of next generation power converters [7]. Furthermore, SiC power devices can also sustain high operating temperatures, thus making them attractive candidates for applications in aircraft, automotive, and energy exploration industries, etc [8], [9].

Thanks to recent progress in SiC process technology, SiC MOSFET has been commercialized. It can be predicted that SiC MOSFET will be applied in power converters more and more widely as its price continually decreases. Therefore, an accurate model of SiC MOSFET is necessary for device evaluation, system design, and power converter behavior prediction. Mantooth *et al*., reviewed different compact models of SiC MOSFET developed by many research groups [10]. The categorization and characteristics of different modeling methods on power semiconductor devices were also reported in this literature. Some effects were considered in these models, such as temperature-dependent gate threshold voltage, temperature-dependent carrier mobility, nonuniform current distribution, and so on [11]-[13]. Another important characteristic of trap density at the SiC/SiO$_2$ interface was also included in some SiC MOSFET models. Potbhare *et al*., developed a comprehensive physical model of 4H-SiC MOSFET, which incorporated interface trap densities and Coulombic interface trap scattering, surface roughness scattering, phonon scattering, velocity saturation, and their dependences on bias and temperature [14]. The physics-based models were implemented into a device simulator that is tailored for 4H-SiC MOSFET analysis, and not suitable for circuit simulations and practical applications due to its high complexity. Tanimoto *et al*., developed a compact SiC MOSFET model for circuit simulation by considering the trap density, which is included in the Poisson's equation. The model is constructed in HiSIM_HV, a power MOSFET model developed by Hiroshima University based on surface-potential based MOSFET model [15]. Kraus *et al*., developed a physics-based compact model of SiC MOSFET including the dependence of channel charge and electron mobility on the charge of interface traps in circuit simulator PSpice [16]. However, many fitting parameters were used in this model, and the effect of interface traps can not be obviously found in the expressions which describe the behavior of SiC MOSFET. In this paper, SPICE modeling of SiC MOSFET is carried out in LTspice IV, a high performance SPICE simulator and free of charge. The model is developed for an example device C2M0080120D (1200 V/36 A SiC MOSFET from Cree, Inc). Advanced mobility model is introduced to describe the interface characteristics and temperature on the effect of the electrical performance of SiC MOSFET. The static characteristics are validated with C2M0080120D Datasheet, and dynamic characteristics are verified by the experimental tests on a Boost converter platform.

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II. SPICE Modeling of SiC Mosfet with Interface Trapped Charge

A. Review on Previous SPICE Modeling for SiC Power MOSFET Based on Their Deficiencies

Fig. 1 shows the equivalent sub-circuit model of SiC MOSFET, which is employed in some literatures [11], [12], [17]. The model consists of nine components. M_1: the built-in SPICE level-1 MOSFET, D_1: the body diode, and its junction capacitor is used as drain-source capacitor C_{DS} of SiC MOSFET, R_G: gate resistor, R_S: source resistor, R_D: drain resistor, C_{GS}: gate-source capacitor, C_{GD}: gate-drain capacitor, E_{TEMP}: temperature-dependent voltage source, G_{TEMP}: temperature-dependent current source. The above components play different roles in the operation of SiC MOSFET. M_1 is used to describe the MOS channel. R_D, R_S, and the resistance of M_1 are used to describe the on-state resistance of SiC MOSFET. E_{TEMP} and G_{TEMP} are employed to describe the static characteristics of SiC MOSFET. C_{GD} and C_{GS} are used to describe the dynamic characteristics. Based on the model shown in Fig. 1, Sun *et al.*, simulated some temperature-dependent effects of SiC MOSFET, such as positive or negative temperature coefficient, threshold voltage and transconductance variations with temperature [12]. Wang *et al.*, claimed the application of this model to describe the temperature-dependent characteristics of the SiC MOSFET, particularly the effects induced by the high density of interface traps present at SiC/SiO_2 interface [11], [17], however, the detailed methodology on how to incorporate the effect of interface traps can not be found in the literatures.

The built-in SPICE level-1 component, M_1, is based on Shichman-Hodges' physical model, which represents the behavior of the device in different modes of operation with simple analytical equations. Equation (1) defines the cutoff region, (2) is the linear region, and (3) is the saturation region, and five parameters are used, they are carrier mobility (μ), channel width (W), channel length (L), threshold voltage (V_{TH}), and channel length modulation parameter (λ), respectively.

$$I_{DS} = 0, \text{if } V_{GS} < V_{TH}\,. \tag{1}$$

$$\begin{gathered} I_{DS} = \mu C_{ox}\frac{W}{L}[(V_{GS}-V_{TH})\cdot V_{DS} - \frac{1}{2}V_{DS}^2]\cdot(1+\lambda V_{DS}), \\ \text{if } V_{GS} > V_{TH}\ \&\ V_{DS} < V_{GS}-V_{TH}\,. \end{gathered} \tag{2}$$

$$\begin{gathered} I_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2\cdot(1+\lambda V_{DS}), \\ \text{if } V_{GS} > V_{TH}\ \&\ V_{DS} > V_{GS}-V_{TH}\,. \end{gathered} \tag{3}$$

B. The Novel Model Considering Interface-Trap Influence Based on the Advanced Mobility Expression

The SPICE level-1 model of MOSFET is available in many circuit simulation tools, such as PSpice and Saber, and the model can satisfactorily meet the requirement in accuracy and time consumption. Nevertheless, SPICE level-1 model was originally developed for Si-based devices, and the carrier mobility was constant, this is for the reason that Si MOSFET has a high-quality interface of Si/SiO_2, and the interface issue on the effect of electrical characteristics of Si MOSFET did not need to be considered. For SiC-based MOS devices, however, the very high density of traps at the SiC/SiO_2 interface bring strongly effect on the electrical characteristics of SiC MOSFET [18]. Interface traps can capture carriers in the inversion channel of SiC MOSFET, which leads to the decreasing of on-state current and the increasing of the on-state resistance. Then, the occupied traps become charge centers, which forms Coulombic scattering and lowers the mobility of carriers in channel.

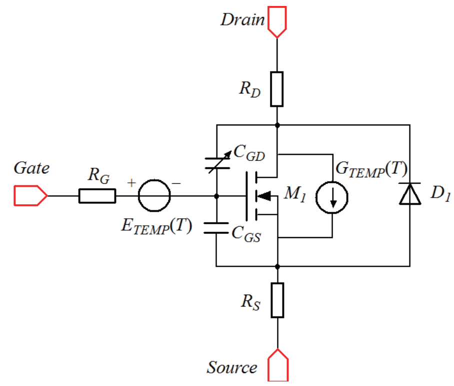


Fig. 1. SPICE sub-circuit model of SiC MOSFET in [11] and [12].

Besides, the mobility degradation of carriers in inversion layer also comes from other scatterings, which are bulk lattice scattering, acoustic phonon scattering, and roughness scattering, respectively. Together with Coulombic scattering, the four different scatterings correspond to four different mobility components. According to Mathiessen's rule, the inversion mobility of carrier μ_{inv} is defined by [14], [19]-[22]

$$\frac{1}{\mu_{inv}} = (\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C})\,. \tag{4}$$

In (4), μ_B is bulk lattice scattering, μ_{AC} is acoustic phonon scattering, μ_{SR} is surface roughness scattering, and μ_C is Coulombic scattering. The corresponding expressions for four different scatterings are summarized in TABLE I [21].

In TABLE I, empirical values of parameters in the four mobility expressions are also listed. $E_\perp$ in μ_{AC} and μ_{SR} is the effective perpendicular electric field at the interface. T, Q_{inv} and Q_{trap} in μ_C are the temperature, inversion charge and trapped charge, respectively.

The effect of interface traps on electrical characteristics of SiC MOSFET is reflected by Coulombic scattering μ_C. If more carriers are trapped, which means that Q_{trap} is higher and Q_{inv} is lower, μ_C would become lower. Under low-field operation of SiC MOSFET, the inversion mobility μ_{inv} is determined by μ_C. Therefore, if we use μ_{inv} in (4) to replace constant mobility in SPICE level-1 MOSFET model, the effect of interface traps on

TABLE I
FOUR MOBILITY COMPONENTS AND THEIR PARAMETER VALUES

Mobility	Expression	Value
μ_B	$\mu_{\min} + \dfrac{\mu_{\max} - \mu_{\min}}{1 + \dfrac{N_{\mathrm{A}}}{N_{\mathrm{REF}}}}$	$\mu_{\max} = 950\ \mathrm{cm^2/Vs}$ $\mu_{\min} = 40\ \mathrm{cm^2/Vs}$ $N_{\mathrm{A}} = 1\times10^{16}\ \mathrm{cm^{-3}}$ $N_{\mathrm{REF}} = 2\times10^{17}\ \mathrm{cm^{-3}}$
μ_{AC}	$\dfrac{B}{E_\perp} + \dfrac{CN_{\mathrm{A}}^{\alpha 1}}{TE_\perp^{1/3}}$	$B = 1.0\times10^6\ \mathrm{cm/s}$ $\alpha 1 = 0.0284$ $C = 3.23\times10^6\mathrm{K\ cm/s\ (V/cm)^{-2/3}}$
μ_{SR}	$\dfrac{D_1}{E_\perp^2}$	$D_1 = 5.82\times10^{14}\ \mathrm{cm^2/V\ s\ (V/cm)^2}$
μ_C	$NT^{\alpha}\dfrac{Q_{inv}^{\beta}}{Q_{trap}}$	$\alpha = 1$ $\beta = 1$ $N = 0.007525\ \mathrm{cm^2/V\ s}$

electrical characteristics of SiC MOSFET can be assessed, and we can quantitatively investigate the effect of different interface-trap density on the switching behaviors of SiC MOSFET.

C. The Modeling for Field and Temperature Dependence Based on Charge-Sheet Model of MOS System

The effective electric field $E_\perp$ and inversion charge Q_{inv} can be obtained according to charge-sheet model (CSM) of MOS system. The charge-sheet model is widely used for calculating the dependence of inversion-layer charge density on surface potential, thus serves as a starting point for describing the current transport in a MOS transistor. The model simplifies the calculation of the inversion charges by assuming that the inversion layer is a charge sheet of infinitesimal thickness, so that the inversion charge Q_{inv} is simply the difference between the total space charge Q_{sc} in the surface space-charge region and the charge within the depletion layer Q_{dep} (in units of $\mathrm{cm^{-2}}$)

$$Q_{inv} = Q_{sc} - Q_{dep}\ . \tag{5}$$

The charge-sheet model equations are also used to calculate the effective electric field in the inversion layer. The effective field in the inversion layer has been reported in [19] to be (ε_S is the permittivity of SiC)

$$E_\perp = 1/\varepsilon_S(1/2Q_{inv} + Q_{dep})\ . \tag{6}$$

Detailed procedure of calculating inversion-layer charge densities of Q_{sc} and Q_{dep} can be found in [21], [23], [24]. Q_{sc} and Q_{dep} are both dependent on surface potential Φ_S, and Φ_S is related with gate voltage and given by an implicit function [25]

$$\begin{aligned} &V_{GB} - V_{FB} - \Phi_S = \\ &\gamma\sqrt{\Phi_S - \varphi_t + \varphi_t\cdot\exp[(\Phi_S - 2\Phi_F - V_{CB})/\varphi_t] + \varphi_t\cdot\exp(-\Phi_S/\varphi_t)}\ . \end{aligned} \tag{7}$$

In this expression, V_{GB} is the applied voltage between gate and bulk, V_{FB} is flat band voltage, γ is bulk effect coefficient, φ_t is thermal voltage and expressed by kT/q, V_{CB} is the voltage between channel and bulk. If some parameters are given, such as the material parameters, physical dimensions and doping concentrations of MOS device, according to CSM model, $E_\perp$ and Q_{inv} are only the function of gate voltage and temperature. And so, the inversion mobility μ_{inv} can be determined by interface trapped charge Q_{trap} for given gate voltage and temperature. In [11] and [12], the temperature-dependent effects are described by E_{TEMP} and G_{TEMP}. In [16], authors also asserted that the influence of a variable temperature on the model parameters is taken into account, but none of parameters in the model can be found to be temperature-dependent, only a thermal equivalent circuit is used to simulate the self-heating. In our model, these effects are described by the temperature-dependent mobility components μ_{AC} and μ_C, temperature-dependent threshold voltage (expressed by 2.437-0.0057*T, obtained by fitting with C2M0080120D datasheet), so we removed E_{TEMP} and G_{TEMP} in Fig. 1, and the equivalent sub-circuit model in this work is shown in Fig. 2.

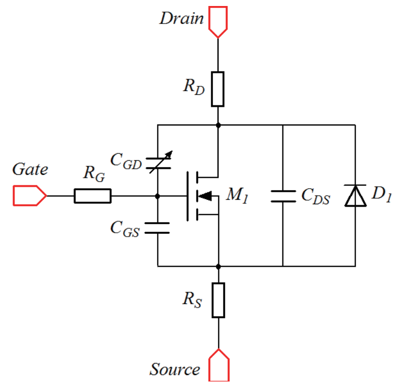


Fig. 2. Proposed SPICE sub-circuit model of SiC MOSFET in this work.

Aside from the Coulombic scattering, roughness scattering also brings strongly influences on the carrier mobility. In [16], the influence is claimed to be included in the current equation, but is not explicitly accounted for. In our model, the roughness scattering is directly related with the effective perpendicular electric field. Increasing gate voltage means the increasing of effective perpendicular electric field $E_\perp$, so the roughness scattering becomes much stronger, which will promote the degradation of carrier mobility.

In [15], the transient SiC MOSFET behavior is reflected by the dynamic trap charges, and the time constants for trapping and detrapping process are the function of time and gate voltage. Comparatively, in our model, the transient behavior of SiC MOSFET is reflected by the action of interface traps on the inversion carriers, which should be more reasonable for the role of interface traps in the operation of SiC MOSFET.

D. The Simplified Model for Gate-Drain Capacitance(C_{GD})

Capacitance between electrodes can storage charge, which can impose effects on the dynamic performance of SiC MOSFET. Three capacitors, C_{GD}, C_{GS} and C_{DS} are used to model the effect. In this model, C_{GD} is modeled based on "switching model" SIEMES [17], but we simplify it by a voltage-dependent current source, and the structure is shown in Fig. 3. In this fig-

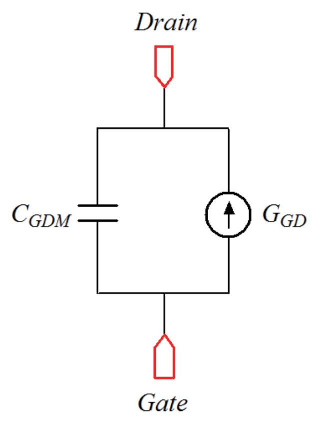


Fig. 3. Simplified C_{GD} model in this work.

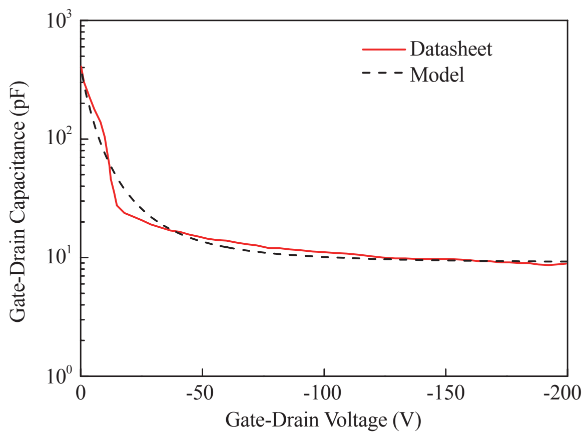


Fig. 4. Comparison of C_{GD} between a simplified model and C2M0080120D Datasheet.

ure, G_{GD} is voltage-controlled current, and is used to represent the C_{GD} when gate-drain voltage (V_{GD}) is less than or equal to 0. C_{GDM} is constant, and represents C_{GD} when V_{GD} is greater than 0. We fit this C_{GD} model with C2M0080120D datasheet [26], and get a new expression for C_{GD}.

$$\begin{cases} G_{GD}=\left(\dfrac{a}{\left(1-{V_{GD}}/{b}\right)^{c}}-a\right)\dfrac{dV_{GD}}{dt}, \quad V_{GD}\le 0 \\ G_{GD}=0, \quad V_{GD}>0\,. \end{cases} \tag{8}$$

Here, a, b, c are all constants, and with the values of 0.40110 e-9, 8.34, and 2.29, respectively. The comparison between C2M00 80120D datasheet and C_{GD} model is shown in Fig. 4.

Compared to the high nonlinearity of C_{GD}, another two capacitors, C_{GS} and C_{DS}, are little affected by the operation of SiC MOSFET, and are modeled by a constant capacitor respectively.

We successfully realized the calculation of $E_{\perp}$, Q_{inv}, Q_{sc} and Q_{dep} in circuit simulator LTspice IV by means of the so-called Arbitrary Behavioral Sources (ABS). After obtaining the inversion mobility μ_{inv} according to (4), we used μ_{inv} to replace the

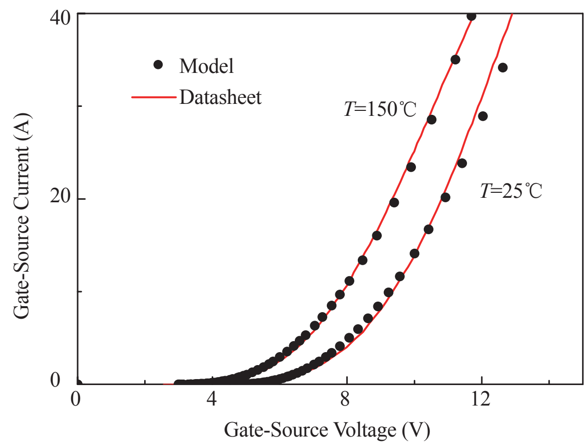


Fig. 5. Comparison of transfer characteristics between this developed SPICE model with C2M0080120D Datasheet.

constant mobility μ in (2) and (3). So, the M_1 in Fig. 2 is characterized with the integration of interface trapped charge Q_{trap} and temperature T, and the effects of Q_{trap} and T on the electrical characteristics of SiC MOSFET can be discussed.

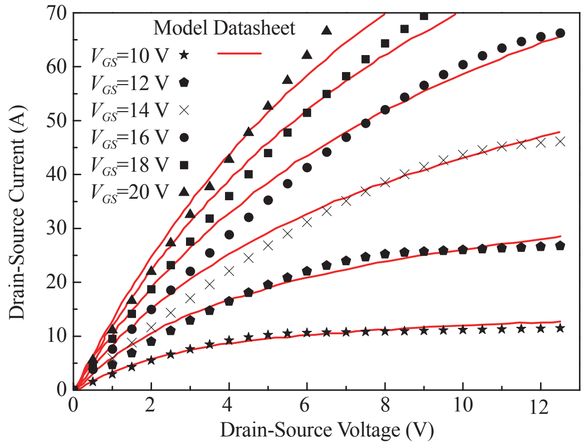
III. Verification of Developed SiC Mosfet Model

A. Static Characteristics Verification

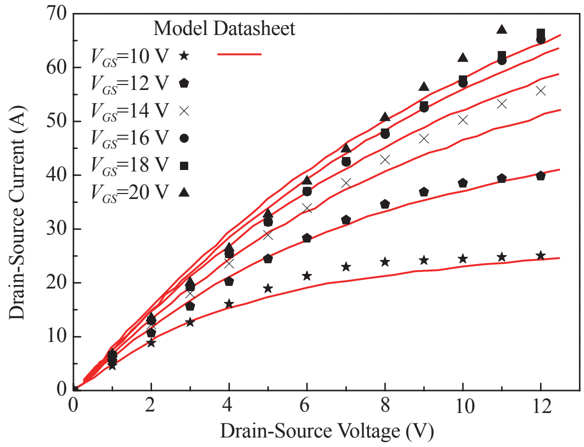
The static characteristics of this developed Spice model are validated against the existing SiC MOSFET C2M0080120D Datasheet [26]. The comparisons of transfer characteristics and output characteristics between the measured results from the Datasheet and the simulation results by the proposed model at 25 ℃ and 150 ℃ are shown in Fig. 5 and Fig. 6. One can see that a reasonable agreement was achieved between the proposed model and the Datasheet, especially the transfer characteristics. Although a deviation appeared for higher gate bias in Fig. 6, however, it is normal and also occurs in other's work [27], [28]. Compared to the physical model of power device, Spice model employs segmented expressions to describe the channel current, more complex physical effect, especially under high field and high temperature, is hardly included into Spice model.

B. Dynamic Characteristics Verification

The dynamic characteristics are verified by experimental results in Boost converter. The schematics of the converter in LTspice IV simulator and the test platform are shown in Fig. 7, respectively. The freewheeling diode (FWD) in the Boost converter is SiC schottky barrier diode (SBD) C4D10120A from Cree. The model of C4D10120A in the simulation is developed by Cree for LTspice IV. Circuit parameters are listed in TABLE II. V_{GS} is the gate-source voltage, V_{DC} is the input voltage of Boost converter, f is the switching frequency, and D represents the duty cycle. All the parameters are same except that the inductance in LTspice IV is 0.01 mH higher than the one in experimental prototype, this is a consideration of the parasitic inductance in experiment circuit.

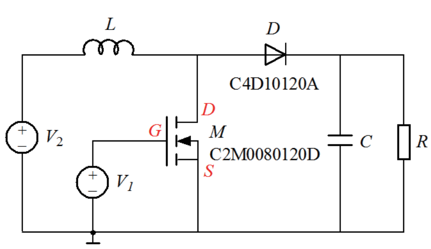


(a)

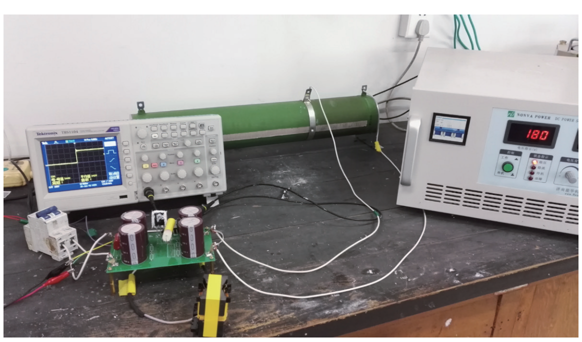


(b)

Fig. 6. Comparison of output characteristics between this developed SPICE model with C2M0080120D Datasheet at 25 °C (a) and 150 °C (b).



(a)

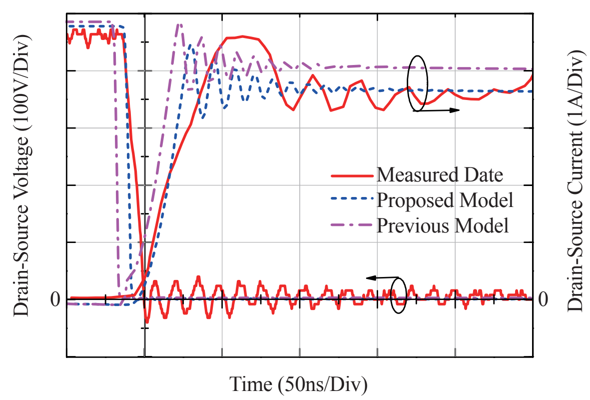


(b)

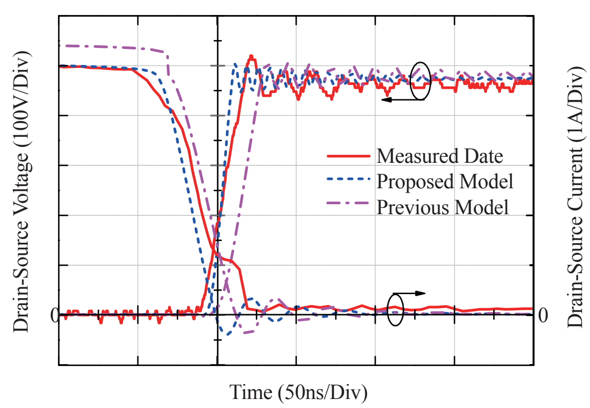
Fig. 7. Schematic of Boost converter in LTspice IV (a) and the experimental platform (b).

TABLE II
PARAMETERS IN BOOST CONVERTER FOR LTSPICE IV AND EXPERIMENT

Symbol	Name	Description	
		Experiment	LTspice IV
V_1	V_{GS}	V_{GS}=20 V, f=130 kHz, D=62%	V_{GS}=20 V, f=130 kHz, D=62%
V_2	V_{DC}	180 V	180 V
L	Inductance	0.5 mH	0.51 mH
M	SiC MOSFET	C2M0080120D from Cree	Developed model in this paper
D	SiC SBD	C4D10120A from Cree	SPICE model from Cree
C	Capacitance	2 μF	2 μF
R	Resistance	290 Ω	290 Ω



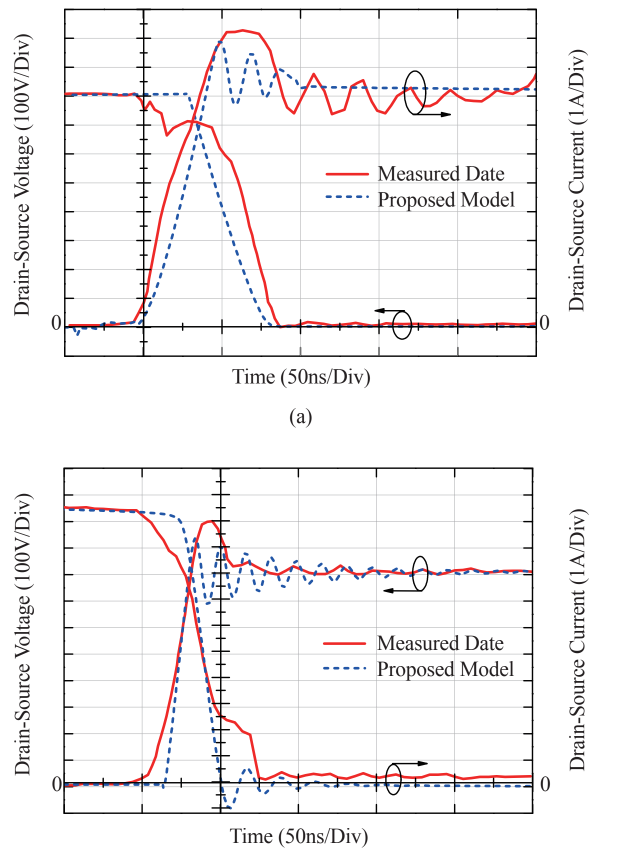
(a)



(b)

Fig. 8. Comparison of turn-on (a) and turn-off (b) waveforms at 470 V between LTspice IV simulation and experiment in Boost converter.

Carefully correlating the number of interface trapped charge, when Q_{trap} is set to 1.39×10^{12} cm^{-2}, reasonable agreement in switching waveforms is obtained between the measured data and the proposed model, which is shown in Fig. 8. At the same time, the results of so-called previous model with a constant mobility are also plotted in Fig. 8 as a reference. One can see that a larger mismatch appears between the measured data and the previous model. In the modeling, to model the stray inductance introduced by cables and connections, a small inductance,



(a)

(b)

Fig. 9. Comparison of turn-on (a) and turn-off (b) waveforms at 800 V between LTspice IV simulation and experiment in Boost converter.

with a value of 7 nH, was placed at the anode of freewheeling diode (not shown in Fig. 7(a)). The value was chosen according to the voltage overshoot measured across the MOSFET during its turning off.

The switching voltage of SiC MOSFET in Fig. 8 is 470 V, to furthermore verify the accuracy of the proposed model, a comparison of higher switching voltage with 800 V was made, and results are described in Fig. 9. Although relatively large deviation occurs, the model can still reproduce the experimental results.

In the simulation of Boost converter, rated with 180 V input voltage, 130 kHz switching frequency and 62% duty cycle, the consumption time of running 100 periods is about 225 s. If we only save hundredth waveform, the consumption time is about 75 s, which is acceptable for power circuit simulation.

IV. Application of the Developed Model in Power Circuit

An important application of the model is to predict the effect of interface traps on the electrical characteristics of SiC MOSFET in power circuits. The issue of power device in circuit is the switching loss, which can determine the working efficiency of power equipments. In this paper, a clamped inductive switching circuit is employed to evaluate the electrical behavior of the

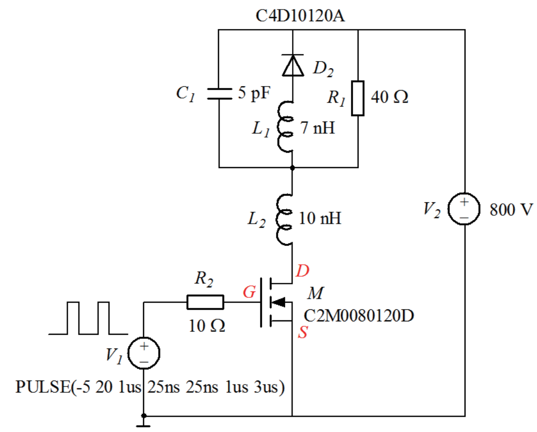


Fig. 10. Clamped inductive switching circuit for simulation of SiC MOSFET's switching loss.

developed SiC MOSFET model with different interface trap densities, and the schematic is shown in Fig. 10. The component parameters are also marked in the schematic. For the gate driving of SiC MOSFET, a step pulse with 1 µs width and 3 µs period is biased to gate electrode through a 10 Ω resistance.

Generally, interface trap can be classified into two types: the acceptor-like trap, located in the upper half of the energy gap, and the donor-like trap, located in the lower half of the energy gap. For *n*-channel MOSFET, playing dominative role is the acceptor-like trap, empty acceptor-like trap is neutrality, and can be negatively charged after capturing an electron. At present, the commercial SiC MOSFET has been believed to be annealed in NO at 1175 ℃ to decrease the density of interface trap. Here, three different distributions of interface acceptor-like trap have been taken to assess the effect of interface traps on the electrical characteristics of SiC MOSFET. Three distributions shown in Fig. 11 are picked from [29], and obtained in NO annealing at 1175 ℃ with different time.

For a continuous energy distribution of interface traps, the trapped charges may be approximated by following expression [21].

$$Q_{trap} = \int_{E_i}^{E_c} D_{it}(E,T)dE \, . \qquad (9)$$

Where, E_i is the intrinsic energy. Q_{trap} corresponding to three distributions of interface trap is 2.87×10^{11} cm^{-2}, 1.83×10^{12} cm^{-2}, 1.63×10^{13} cm^{-2}, respectively, and successively named Q_{trap0}, Q_{trap1}, Q_{trap2}.

The switching waveforms of SiC MOSFET in Fig. 10 corresponding to Q_{trap0}, Q_{trap1} and Q_{trap2} are shown in Fig. 12. It can be seen that interface traps delay the turn-on of SiC MOSFET, and lead the device forward to turn-off in advance. For *n*-channel MOSFET, acceptor-like traps capture the free electrons in the channel, resulting in the decreasing of drain-source current, and more traps mean less electrons. Also, the charged traps become the scattering centers, hindering the movement of electrons, so the rising of the drain-source current I_{DS} and the falling of drain-source voltage V_{DS} both becomes slow during the turn-on of SiC MOSFET. After the gate voltage is removed, the device with higher density of interface traps can turn off more early as a

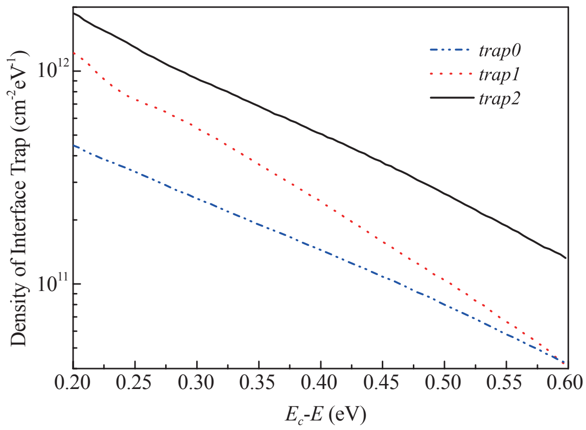


Fig. 11. Three distributions of interface traps for LTspice simulation [29].

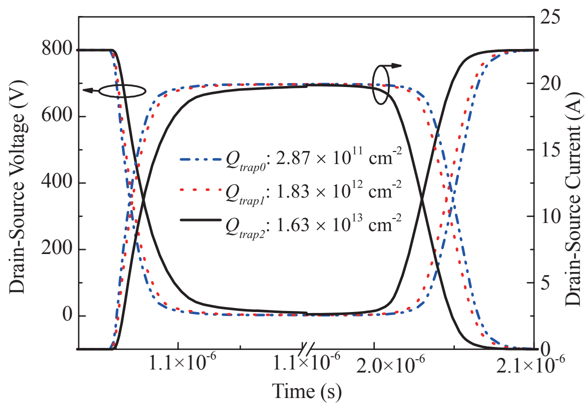


Fig. 12. Switching waveforms of SiC MOSFET for different Q_{trap}.

result of more electrons captured. The simulated results of interface trap's influence on the switching behavior of SiC MOSFET can bring prompt for device application in series or in parallel to improve its power capacity. Synchronization of device operation is required for this application, so these devices should be with the same density of interface traps to avoid the out-of-step in turning-on and turning-off.

The turn-on loss, turn-off loss and total loss of SiC MOSFET for three distributions of interface traps are also calculated by the product of V_{DS} and I_{DS}, the results are listed in TABLE III. We can see that the turn-on and turn-off losses both increase with the increasing density of interface trap. The interface traps delay the turn-on of 4H-SiC MOSFET and the overlapping region of V_{DS} versus I_{DS} increases, which leads to a higher power loss. Though the interface traps drive the device turn-off in advance, the overlapping region also increases with the density of interface traps, so the turn-off loss increases. Higher density of interface traps capture more carriers in the channel, and so the on-state resistance increases.

Extensive application of this developed model is to assess the effect of gate driving voltage on the loss of SiC MOSFET with different distributions of interface traps. We know, higher gate voltage can yield more free carriers in the inversion layer of channel, which can decrease the switching loss and on-state

TABLE III
The Loss of SiC Mosfet for Different Q_{trap}

Q_{trap} (cm^{-2})	Turn-on Loss (W)	Turn-off Loss (W)	Total Loss (W)
Q_{trap0} (2.87×10^{11})	17.58	19.74	52.16
Q_{trap1} (1.83×10^{12})	20.51	20.43	56.35
Q_{trap2} (1.63×10^{13})	37.28	22.30	84.72

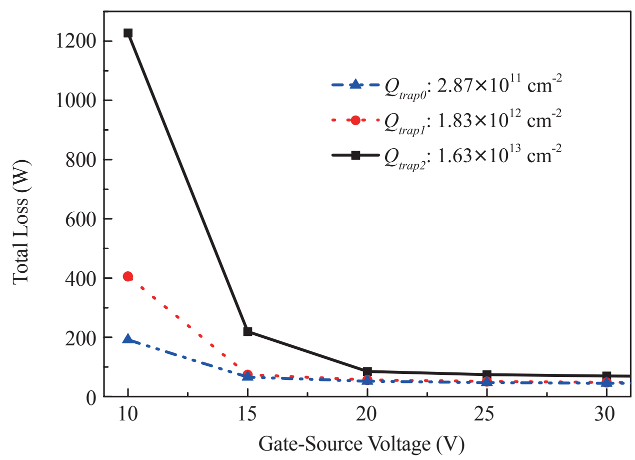


Fig. 13. Relationship between gate voltage and the total loss of SiC MOSFET with different interface traps.

loss, but rise the complexity and the loss of gate driver. However, when the density of interface traps is high, increasing gate voltage seems to be an effective method to decrease the switching loss and on-state loss. Fig. 13 shows the relationship between gate voltage and the total loss of SiC MOSFET for three distributions of interface traps. The first noticed point is that the switching loss is very high when the gate voltage is less than 20 V, but shows less change for gate voltages higher than 20 V. This model is developed taking the C2M0080120D device as example, and the suggested gate voltage in C2M0080120D Datasheet is 20 V, which is consistent with our simulation result, the loss and gate driving complexity can obtain a good tradeoff under this voltage.

V. Conclusions

A novel circuit simulation model of SiC MOSFET is proposed and validated. The model is developed based on the present SPICE level-1 MOSFET model, but the constant mobility has been replaced by advanced mobility which can reflect the effect of interface traps and temperature on the electrical behavior of SiC MOSFET. The including of interface traps in this model makes it suitable for simulating the synchronization of device operation in series or parallel connection, also, the loss of SiC MOSFET can be accurately assessed by applying this model in the design of power converters.

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MVDC Supply Technologies for Marine Electrical Distribution Systems

Uzair Javaid, Francisco D. Freijedo, Drazen Dujic, and Wim van der Merwe

***Abstract*—The increase in the popularity of the medium voltage dc (MVDC) electrical distribution, as a possible evolution of the medium voltage ac (MVAC) electrical distribution for the ship on-board power systems, arises a need for a comparative evaluation and demonstration of feasible technologies for the MVDC supplies. For designing the MVDC supplies in the range from 5-35 kV, different available technologies can be considered for the designs and have a direct influence on the overall system performance. In this paper, different technologies for prime movers, electrical generators and rectifiers are discussed in terms of feasibility for the MVDC supplies. Different supply configurations can be envisioned from these based on the commercial availability, quality of supply, efficiency, dynamic performance and volume. Multi-phase multi-pulse supply configurations are identified and proposed for the marine MVDC systems. Combination of multi-phase generators and multi-pulse rectifiers offer reliable, simple and fault tolerant solution with acceptable dynamics. To explore and highlight these benefits, a six-pulse rectifier sub-module is designed and analysed in two arrangements for multi-pulse configurations, namely parallel and series. It has been shown that with appropriate selection of semiconductor devices, coupled with properly selected fast fuses, excellent fault current (thermal) withstand capabilities can be achieved.**

***Index Terms*—Fault tolerance, multi-phase generation, multi-pulse rectifiers, MVDC electrical distribution, MVDC supplies.**

I. Introduction

SINCE the last decade, both academia and industry have been exploring the possibilities of dc distribution for the ship on-board electrical distribution system [1]-[3]. This has lead to the development of a low voltage dc (LVDC) electrical distribution system (1 kV) for offshore support vessels by ABB, covering power requirements of up to 20 MW, with reported fuel savings reaching 20% [2]. Another LVDC system is developed by Siemens named *BlueDrive PlusC* [4]. These systems demonstrate the benefits of the dc electrical distribution in ships such as lower fuel usage, increased energy density of the system, smaller footprint of the installed equipment, and flexibility in overall ship design. Higher power requirements (more than 20 MW) in larger ships, where the state-of-the-art is the medium voltage ac (MVAC) electrical distribution [5], require migration to medium voltage dc (MVDC) electrical distribution system to achieve the same benefits as shown by LVDC systems.

For the implementation of the MVDC electrical distribution system on ships, one of the key areas for research and development is the on-board electricity generation. In the present systems, i.e., MVAC electrical distribution systems, fixed speed operation of diesel engines is required to maintain ac frequency and the generators are operated in a synchronized manner. The move to the MVDC electrical distribution system removes these synchronization requirements, as the generators are interfaced to the rectifiers and the diesel engines could be operated at variable speeds, achieving optimum fuel consumption and efficient system operation. Possible technologies, for the MVDC supply, have been discussed in literature, highlighting the possible prime movers, generators, rectifiers and energy storage that could be used [6]-[12]. In [6], 7% fuel savings is predicted for the MVDC electrical distribution, where two similar ship on-board systems are compared with one having MVAC and the other with MVDC electrical distribution. In addition to the fuel savings, this opens up opportunities to use high speed prime movers and generators, resulting in higher energy density and smaller footprint [3]. In [7], this prospect is further investigated considering generator technologies starting from the existing low- to high-speed generators and extending to the possible ultra-high speed generators in the future. The possibility of interfacing multi-phase generators with multi-pulse rectifiers, connected in series, is considered in [8], [9], whereas, their impact on the stability of the distribution system is evaluated in [10]. The impact of charging of energy storage on dc-side voltages is discussed in [11], [12].

Another important aspect of the MVDC electrical distribution system is its fault tolerant characteristics. As dc breakers are not readily commercially available for MVDC applications, different works have been presented on possible ways of limiting or blocking the fault current in a very short time, i.e., 4-10 ms [13]-[17]. Different hybrid fault clearing circuits are proposed in [13], [14], but they usually result in high losses [16]. Fault clearing topology for active rectifiers that can isolate the fault current, is presented in [15], while current fold-back principle is proposed for thyristor rectifiers for MVDC marine applications, in [16]. The LVDC electrical distribution systems for ships de-

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ploy multiple strategies to handle high fault currents and ensure high system availability. These strategies include, e.g., generators with high sub-transient reactance (X_g''), overload detection equipment on generators, specially developed fault tolerant busties, fuses, isolator switches, fault current blockage by power converters and short circuit withstand capability of power converters [2], [17].

This paper provides an overview of the feasible MVDC supply technologies, and in particular highlights the advantages of multi-phase multi-pulse supplies. Possible multi-phase multi-pulse supplies are proposed for the MVDC distribution and design of a rectifier sub-module is provided that can be arranged in parallel and series configurations to generate different MVDC distribution voltages. As DC breakers are unavailable, surge current and fault handling capabilities of the proposed rectifiers are analyzed and fast fuses are considered to remove high fault currents. Furthermore, the paper is organized as follows: Section II provides brief qualitative analysis based on commercially available prime movers, generators and rectifiers, commonly used in MVAC system and thus considered ready for the MVDC systems. Possible MVDC supply configurations, predominantly considering various configuration and topologies of rectifiers are presented in Section III, from where system level advantages of multi-phase multi-pulse rectifier configurations are derived. Section IV presents the design of practical MVDC supplies and an analysis is provided considering the surge current and thermal withstand capabilities of the proposed rectifier topologies. Finally, Section V summarizes the findings and concludes the paper.

II. An Overview of the Power Generation Technologies

The future ship on-board MVDC electrical distribution systems, especially power generation applications, are expected to adopt different technologies from the state-of-the-art MVAC and LVDC electrical distribution systems. Moreover, certain equipment, e.g., gearboxes and bulky transformers for voltage coordination are expected to be removed in the MVDC electrical distribution systems to provide flexibility and footprint reduction in the overall ship design [18]. This evolution of the on-board electrical distribution system, from the state-of-the-art MVAC to prospective MVDC system, is illustrated in Fig. 1 with notional MVAC and MVDC systems. In the MVAC systems, fixed speed prime movers and generators are the norm, producing electrical power at constant ac frequency and supplying different loads through different switchboards and voltage coordination transformers [5]. These multi-pulse transformers are especially important for connecting the variable speed drives (VSDs) for propulsion, which are often the major loads of the installation. The MVDC distribution provide possibilities to reduce the equipment footprint, increase energy density and efficiency of the system, as it allows flexibility in design by offering choice of selection between various standard or non-standard power conversion equipment [19].

In the following subsections, a brief discussion is provided on various equipment, commercially available (used), with considerations on their role in the power supplies of the future MVDC ships.

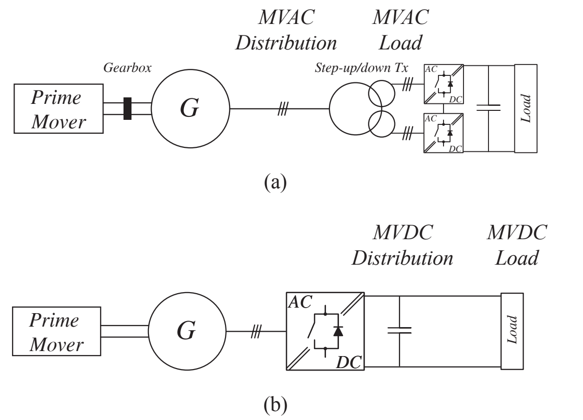


Fig. 1. (a) Simplified notional MVAC distribution with gearbox interfacing prime mover and generator, and multi-pulse transformer connected to the propulsion VSD. (b) Simplified notional MVDC distribution where gearbox and transformer are removed.

A. Prime Movers

The prime mover-generator set is the main source of power for the on-board electrical power systems. Internal combustion engines (ICEs) are usually used as prime movers in many marine applications. These run on diesel or heavy fuel oil (HFO), but wherever gas is available as a cheaper alternative gas turbines, steam turbines or combined cycle turbines can also be found, especially for high speed vessels or liquefied natural gas (LNG) tankers [5]. In an effort to improve the fuel efficiency and reduce emissions of ICEs, ABB has introduced dynamic ac (DAC) and LVDC electrical distribution for large and medium size ships showing 6% and 20% reduction in fuel consumption, respectively [2], [20]. Another opportunity, arising from the use of variable speed operation of the prime movers and lack of requirement for the synchronization of the generators, is the consideration of high speed ICEs and gas turbines as the principle prime movers for high speed generators. This presents the possibility to remove step up/reduction gearboxes, interfacing the prime movers and the generators, considering that their efficiency is around 70% and their size is considerable at high power levels [21]. A summary of the available prime mover technologies is provided in TABLE I.

1) *Internal Combustion Engines:* ICEs, used as prime movers in the state-of-the-art marine MVAC electrical distribution systems, are usually operated at medium (400-1000 rpm) to high speed speeds (1000 rpm and above) [28]. Mainly liquid fuel, e.g., HFO or marine diesel oil, is used, but some applications also utilize gas, e.g., LNG tankers. Additionally, ICEs having dual fuel capability are also being employed, in accordance with the Tier II and Tier III emission reduction programs of International Maritime Organization (IMO) [23]. There is a constant push to improve efficiency and emissions of the ICEs, however, the opti-

TABLE I
SPECIFICATIONS OF ICEs AND GAS TURBINES FOR MARINE APPLICATIONS

PM	Manufacturer	Power Range	Thermal Efficiency	Speed	Fuel Type	Reference
ICE	Wärtsilä	0.92-11.2 MW	42-52%	600-1000 rpm	Liquid/Gas	[22]
	MAN	0.45-12 MW	48-55%	720-1800 rpm	Liquid/Gas	[23]
	GE	1.3-4.7 MW	≈50%	900-1050 rpm	Liquid/Gas	[24]
	Rolls Royce	3.6-9.6 MW	44-48.5%	720/750 rpm	Liquid/Gas	[25]
GT	GE	4.5-42 MW	≈40%	7-3.6 krpm	Gas	[26]
	Rolls Royce	3-40 MW	≈40%	15-3.3 krpm	Gas	[27]
ICE GT	*Literature*	1-10 MW 3-40 MW	≈40%	720/750 rpm 3-15 krpm	Liquid/Gas	[5]

TABLE II
SPECIFICATIONS OF GENERATORS FOR MARINE APPLICATIONS

Gen	Manufacturer	Power Range	Voltange	Speed	Reference
SM	ABB	1-50 MVA	1-15 kV	500-1800 rpm	[30]
	Siemens	0.38-20 MW	0.4-13.8 kV	500-1800 rpm	[31]
	GE	2.5-45 MW	0.4-15 kV	300-1200 rpm	[32]

mum fuel consumption of a medium speed ICE is still very high for constant speed operation in MVAC distribution (around 200 g/kWh for 85% loading). This can be reduced to around 70 g/kWh for a variable speed operation (50% - 100% rated speed), which is possible using dc distribution [2]. Decrease of fuel consumption and operational costs is one of the key commercial motivations for move from MVAC to MVDC ships.

2) *Gas Turbines:* GTs have been deployed in military ships since 1960s and are also finding their way into commercial vessels as auxiliary generators [5]. They are increasingly being considered, as the main prime movers in ships, for power generation as they are reliable and have a smaller footprint compared to ICEs, therefore, ensuring energy density. However, they have rather low efficiency (≈ 40%) and are expensive to run [29]. In the future MVDC system, GTs are expected to be deployed to operate on wide speed range which improves their efficiency, system performance and their compactness also ensures energy density and space saving. Different manufacturers like GE and Rolls Royce are offering different gas turbines ranging from 3-42 MW for marine applications [26], [27].

B. Generators

Another important part of the on-board electric power generation are the electrical machines, operated as generators. In ac systems, these are coupled, either directly or through a gear box, to the shaft of the prime movers that rotate at a constant speed of 720/750 rpm in case of medium speed diesel engines and upto 1800 rpm for high speed diesel engines. Like the prime movers, dc electrical power distribution allows the generators to operate at variable ac frequencies, removing the need for synchronization of different generators on the ship. This allows the system designers to consider high speed generators, e.g., permanent magnet synchronous generators (PMSG), matching the speed of the prime mover and complete removal of the gearbox. A brief summary and key characteristics of a few selected generators are given in TABLE II.

1) *Synchronous Generators:* The most commonly used generator technology, in the on-board electrical distribution systems, is the synchronous generator [5]. These generators usually have 8/10 poles and rotate at speed of 750/720 rpm to produce ac voltage at 50/60 Hz. Generators, with 2, 4 or 6 poles, are also sometimes employed and rotate at their respective speed to produce 50/60 Hz ac. As prime mover and generator rotation speeds are usually not the same, a gearbox is needed to have the correct rotational speed of the generator. Automatic voltage regulators (AVRs) control the excitation current of the field windings (either as direct or brushless excitation) in order to maintain the terminal voltage of the generators. For steady state operations, the voltage regulation is limited to ±2.5% of the nominal voltage, while, voltage transients must not exceed -15% or +20% of the nominal generator voltage. Oscillations, in the generator voltage due to load sharing among different generators or any load variations, are normally damped by the damper windings [5].

2) *Permanent Magnet Synchronous Generators:* Permanent magnet synchronous machines (PMSMs) are mainly deployed in oil and gas industry as turbo compressors [33], but their use as possible generators for dc power systems has been reported in literature [34], [35]. PMSMs can be used in applications where high speed operation, i.e., 8000 rpm and above, is required [35]. The high frequency operation of PMSM is possible due to the use of permanent magnets for magnetic field rather than externally provided excitation for the rotor field winding. Despite the benefits of using the PMSMs, there are certain challenges due to

the lack of long operational experience in marine applications, and the full potential of PMSMs is difficult to assess/realize, as summarized in [7].

C. Transformers

Transformers, in the marine MVAC electrical distribution networks, are mainly used for the reason of galvanic isolation and voltage coordination, considering that rated voltage of electrical generators does not necessarily match the voltage of propulsion motors [5]. These transformers, usually found at the input of propulsion VSDs or large group of LVAC loads, are bulky, heavy and occupy significant space in the already constrained area. Due to use of oil for cooling and insulation and in case of faults, they are a fire hazard and other environmental concerns. However, these transformers usually have multiple phase shifted secondaries and are interfaced to multi-pulse rectifiers providing high quality ac supply to the propulsion inverters, while simultaneously improving the power quality indices (current and voltage distortions) and reducing the negative impact on other components of the marine electrical power system, e.g., generators. At the same time, they provide short circuit limiting impedance in case of faults. IEC standards are also available for design of marine transformers depending on their functionality [36]. While, there is a clear motivation to remove transformers from the future marine MVDC electrical distribution networks, it would be advantageous to preserve possibility to use multi-pulse rectifiers for quality of MVDC supply. For that reason, multi-phase generators are seen as important technology that can provide the same function, even though it is not the exact replacement technology.

D. Rectifiers

Even though rectifiers, as standalone equipment, are not essential part of MVAC ship design, discussion is provided hereafter, as their importance will be significant for MVDC ships. Presently, state-of-the-art VSDs, employed in the on-board MVAC distribution systems in ships, have their own rectifiers as integral part of the package, and since regeneration is usually not needed these are often simple multi-pulse diode rectifiers. In the new ship on-board MVDC electrical distribution system, rectifiers become essential part as they are directly interfaced to generators, provide conversion from ac to dc, and directly impact the quality of the MVDC supply. As this removes the need for synchronization of different generators, it also provides a lot of flexibility in system design and opportunity to use energy dense solutions, such as high speed generators. Various rectifiers topologies, such as diode, thyristor, active (classical 2-level/multi-level topologies) or MMC rectifiers can be considered and their benefits should be analyzed on the system level.

1) *Diode Rectifier Unit:* The schematics of the diode rectifier unit (DRU), with a capacitive filter, is shown in Fig. 2(a). As it is made of passive devices, it lacks the ability to regulate the dc-side voltage or the ac-side currents, but this makes its construction the simplest and cheapest among the different rectifier topologies. The DRUs are employed in the present drive technology [37], especially for marine applications where no regeneration is possible, and are interfaced with input multi-secondary transformers in 12, 18 or 24-pulse series or parallel configurations, but also in the new LVDC marine systems [4].

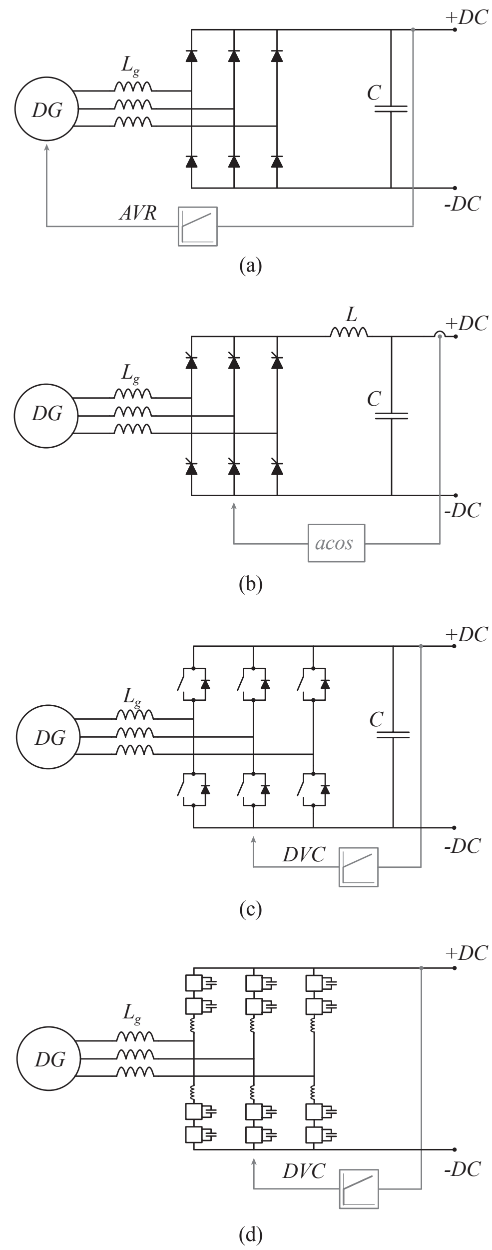


Fig. 2. 3-phase system configuration with different source side converters. (a) Diode rectifier. (b) Thyristor rectifier. (c) Multi-level active rectifier. (d) MMC active rectifier.

2) *Thyristor Rectifier Unit:* The second type of rectifier that can be considered for MVDC supply is the thyristor rectifier unit (TRU), as shown in Fig. 2(b). So far, in marine on-board distribution (except LVDC) they have not been used, but as they provide possibility to regulate the dc-side voltage in a narrow voltage range, they are being considered as a possible MVDC supply side converter [16], [38]. Furthermore, they are being deployed for LVDC

electrical distribution systems as supply side converters [2], even though during normal conditions they are operated as DRUs. TRUs have a more complicated construction compared to DRUs and are more expensive alternative to DRUs. However, in the LVDC distribution systems, TRUs provide possibilities to reduce fault current due to ability to reverse output dc voltage [2] and for those reasons TRUs are also considered for the MVDC electrical distribution systems [16].

3) *Active Rectifier Unit:* The active rectifier unit (ARU) with a capacitive filter is shown in Fig. 2(c) and it represents the most advance solution. Different ARU topologies, e.g., classic 2-level voltage source converter (VSC) and multi-level like 3-L neutral point clamped (NPC), 3-L active NPC (ANPC), 4-L flying capacitor (FC) and 9-L cascaded h-bridge (CHB) are possible and also found in the commercially available products. Among these topologies, the 3-L NPC is most widely used in MV applications [39]. ARUs are relatively expensive compared to the DRUs and TRUs and their ability to allow bidirectional power flow is of limited use, as the regeneration is normally not possible. Additionally, ARUs cannot control currents in case of faults [40], hence, their application in marine systems does not bring much advantage (except for possibility to tightly regulate dc bus voltage), considering system perspective.

4) *Modular Multilevel Converter:* The modular multilevel converter (MMC) (Fig. 2(d)), can be classified as another ARU technology that can be considered for marine MVDC applications as it offers certain advantages: higher efficiency due to lower switching frequency, modularity, voltage scalability and reduced filtering effort due to the presence of sub-modules [41]. The bipolar sub-modules also help in limiting the dc-side fault currents by the converter itself. MMC is reported as a possible supply side converter for marine MVDC electrical distribution systems in [42]. However, MMCs are likely more complicated solution than needed in reality, and especially since their footprint is normally bigger than commercial ARU based on multi-level topologies. Yet, they do offer better scalability and flexibility to adapt to different voltage requirements in MVDC systems.

While different rectifier topologies could be analysed, DRUs are considered in this work for a number of reasons: (i) they are already employed in the commercial marine VSDs with significant operational experience and design knowledge, (ii) TRUs do not have substantial advantages over DRUs unless fault limiting features are highly valued and desired, (iii) ARUs and MMCs, despite being the most advanced four-quadrant solution, are likely too costly for real commercial considerations. Additionally, even without sophisticated control, the dynamic performance of DRUs is also very good for marine applications [38], [43].

III. Multi-Phase Multi-Pulse Marine MVDC Supplies

The expected benefits of the MVDC electrical distribution system, e.g., fuel efficiency, lower operation costs, energy density and smaller footprint to name a few, revolve around the technologies and operation strategies chosen for the MVDC supplies. Marine MVDC supplies are expected to power systems with different distribution voltage levels such as 5, 10, 15, 20, 25, 30 and 35 kV, depending on their power levels [1]. There are already concepts which allow for generator frequency variation in MVAC systems (e.g., 48-60 Hz) such as dynamic AC (DAC) [20], with goal to maximize the efficiency. However, in terms of prime-mover rotational speed or generator ac frequency, much larger variations are expected in MVDC systems (e.g., 50-1000 Hz), when compared to present MVAC systems.

A. 3-Phase Electrical Generation

On the system level and based on previous discussions different configurations are possible for the prime movers, generator types, ac and dc voltage levels, operating frequencies, and type and control of the supply-side converter. However, increase of the power levels is normally followed by the increased MVDC voltage, and considering desire to avoid use of transformers in the system, typical 3-phase generators connected to simple 6-pulse rectifiers have certain shortcomings. Limited blocking voltages of present semiconductors require more devices to be connected in series and this increases the complexity of the auxiliary circuits like voltage balancing circuits and snubbers. Power quality of the 6-pulse rectifiers is also quite low [44], and there is no simple way to implement redundancy, other than redundancy on the system level as it is the case already. Despite being simple and reliable solution, it does not provide sufficient voltage scalability, and for those reasons other solutions are required.

B. Multi-Phase Electrical Generation

To overcome previously described challenges, multi-phase generators characterized with multiple sets of 3-phase windings should be considered. These machines are mostly employed as propulsion motors due the redundancy offered by the multiple sets of 3-phase windings. This redundancy, while of no use in MVAC distribution due to requirement of generator synchronization, has a considerable potential in the supplies for the future MVDC systems. Multi-phase generators coupled with multiple 6-pulse DRUs appear as an attractive solution. Moreover, these multi-pulse DRUs, e.g., 12, 18, 24-pulse depending on the voltage or power requirements of the system, could be built from multiple basic 6-pulse DRU units [37]. The advantages expected from these multi-pulse multi-phase supplies are: high quality of MVDC voltage achieved in a simple way; multi-phase generator to some extent replaces the role of multi-winding transformer; better fault tolerance and introduction of another level of redundancy in the system; provide additional degree of freedom to select voltage classes of generators and motors; ability to utilize present semiconductor technology in an efficient way. Two possible arrangements of these configurations are shown in Fig. 3 and discussed below.

1) *Multi-Pulse Parallel Rectifiers:* The first configuration under consideration is the parallel connection of the rectifiers, as shown in Fig. 3(a). The voltage rating of the

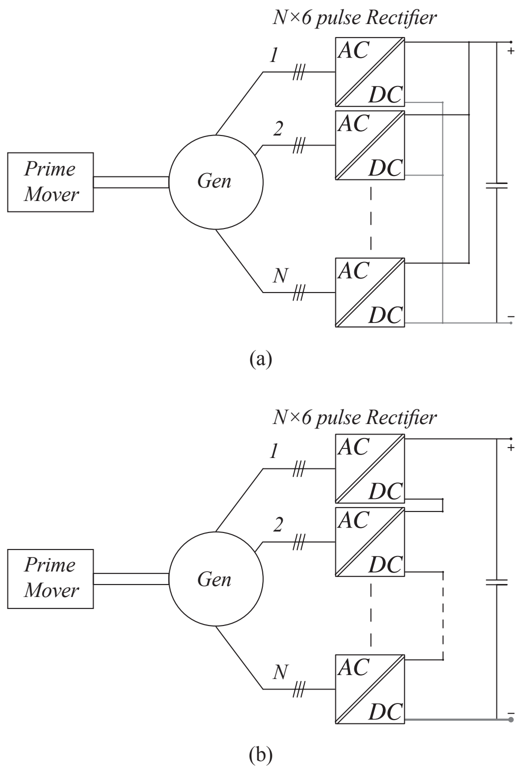


Fig. 3. N×3-phase system configuration. (a) Parallel connection of rectifiers. (b) Series connection of rectifiers.

windings of the N × 3-phase generator are equal to the full ac-side voltage, e.g., 3.7 kV ac for 5 kV dc-side supply or 7.4 kV for 10 kV dc-side supply. However, the total current is divided among the different winding sets i.e., $I_{ac,N} = I_{rated}/N$, where N is the number of 3-phase winding sets of the generator. Moreover, each rectifier is also rated to the full dc-side voltage, and depending on the exact MVDC voltage level (10 kV, 15 kV, ... and selected voltage class of semiconductor devices (4.5 kV, 6.5 kV) there may be a need for a series connection of several devices (including snubbers and static and dynamic voltage balancing circuits). Similar to the case of the generator winding sets, the current through each rectifier is $I_{rec,N} = I_{dc,tot}/N$. The parallel connections of the rectifiers, albeit providing a high quality MVDC supply, eventually leads to situation where the voltage class of the generators and motors are similar/identical. The assumption here is that motors (propulsion or other pumps) are connected to MVDC electrical distribution network through a dedicated inverter. However, in case of a fault resulting in loss of a 3-phase winding set or one of the rectifiers, the system can continue to operate in a de-rated mode. This means all critical loads can be supplied, while, non-essential loads are disconnected. Thus multi-phase multi-pulse parallel rectifiers are suited for ship architecture where fault tolerance is of high importance.

2) *Multi-Pulse Series Rectifiers:* The series connection of several rectifiers is shown in Fig. 3(b). In this case, the voltage rating of each of the generator winding set and rectifier is $V_{ac/dc,N} = V_{ac/dc,tot}/N$. However, as the load current flows through each of the 3-phase winding set and rectifier, the current ratings is $I_{ac,N} = I_{rated}$. The series connection of the rectifiers lowers the required voltage class of the semiconductors, compared to the parallel case, providing more degrees of freedom for the optimization. As devices are expected to block lower voltages, this leads to fewer auxiliary circuits, e.g., snubbers and voltage balancing circuits. Another advantage which this configuration brings is the additional flexibility to optimize the selection of the voltage classes of generators and motors, i.e., generators with lower voltage ratings can supply propulsion motors with high voltage ratings (assuming appropriate insulation coordination on the generator side). However, parallel configuration does not provide redundancy, and in case of fault on any of sub-rectifiers, likely complete supply chain will be out of service. Bypassing faulty sub-rectifier would allow system to continue to operate, but since the MVDC voltage is reduced, this is of little practical relevance.

TABLE III provides a summary of the possible voltage

TABLE III
N×3-Phase System Level Design - Non Isolated - No Gearbox - N×3-Phase Generator - Target 5 -35 kV MVDC

PM	Generator		Rectifier	
	Phase No.	Vltage (V)	Config	MVDC
Any	6	2×3×3.7 kV	DRU,12-p.P	5 kV
		2×3×1.85 kV	DRU,12-p.S	
	9	3×3×3.7 kV	DRU,18-p.P	
		3×3×1.23 kV	DRU,18-p.S	
	12	4×3×3.7 kV	DRU,24-p.P	
		4×3×925 V	DRU,24-p.S	
	15	5×3×3.7 kV	DRU,36-p.P	
		5×3×740 V	DRU,36-p.S	
Higher phase numbers and voltages affects rectifier arrangement		Similar to above	Parallel or Series	10 kV 15 kV 20 kV 25 kV 30 kV 35 kV

TABLE IV
Rectifier Module Parameters Considered in this Study

Module Parameters	
Rated Power (P_n)	9 MW
Rated DC Voltage (V_{dc})	5 kV
Rated AC Voltage (V_{ac})	3.7 kV
Rated Frequency (f_n)	50 Hz
Generator Inductance (L_g)	$0.1\times \frac{V_{dc}^2}{2\pi f_n S_n}$ mH
Cable Parameters	
Cable Inductance (L_c)	0.347 mH/km
Cable Resistance (R_c)	0.089 Ω/km
Cable Capacitance (C_c)	0.307 μF/km

TABLE V
DESIGN OF 9 MW 6-PULSE RECTIFIER MODULE

Device		Parameters	6-Pulse Rectifier Module
Manufacturer	ABB	V_{RRM} *(V)*	1310 @ 2 devices connected in series
Model	5SDD06D600	$I_{d\,avg}$ *(A)*	300
V_{RRM} *(V)*	6000	$I_{d\,peak}$ *(A)*	910
$I_{f\,avg}$ *(A)*	662	$I_{d\,rms}$ *(A)*	520
$I_{f\,rms}$ *(A)*	1040	*No. of devices*	24
I_{FSM} *(A)*	10500	*Loss per device (W)*	740
v_f *(V)*	1.066	*Total Loss (W)*	17700
r_t *(mΩ)*	0.778	*Efficiency*	99.5%

classes of the multi-phase generators to achieve a certain dc-side voltage. A variety of combinations are possible, providing flexibility for the ship designers to optimize the overall system and carry out voltage coordination between generators and motors.

IV. DESIGN, SIMULATION AND COMPARISON OF THE MVDC SUPPLIES

In this section, design of a 6-pulse DRU sub-module is presented, which then can be arranged in parallel and series configurations to achieve high quality MVDC supplies for different power levels and distribution voltages to demonstrate the effectiveness of multi-phase multi-pulse rectifiers. Furthermore, fault withstand capabilities of these supplies are investigated and need for fast protection is elaborated, considering the lack of DC breaker technology, fast power electronics fuses could be considered for protection of the rectifiers in case of faults.

A. Design of DRU Sub-Module

In order to realize different MVDC supplies, a 5 kV 6-pulse DRU module is designed for parameters given in TABLE IV, using ABB diodes rated at 6 kV blocking voltage [45]. The blocking voltage requirement for the devices is calculated using $V_{RSM} = \sqrt{2}V_{S,rms} \times k$, here V_{RSM} is absolute maximum rating of the diode, $V_{S,rms}$ is the rms value of the ac voltage and k is safety factor usually taken as 2.5 [46]. For this case, devices are required to block 13.1 kV which translates into connection of 2 devices (with auxiliaries) in series to fulfill this requirement. Additionally 2 more devices, in similar arrangement, are required to be connected in parallel for the rectifier to withstand high fault currents (discussed later w.r.t. I^2t), leading to 4 (2+2) devices per branch of the DRU sub-module. Schematics of the DRU sub-module are given in Fig. 4. Furthermore, these parallel-connected devices are considered to have minimal discrepancies in their v_f and r_t, respectively. This ensures that the current is almost evenly shared by the 2 sets of diodes. The device parameters and sub-module losses and efficiency, for the operation, at rated power are given in TABLE V.

As losses are incurred at each device, the device junction temperature (T_j) should not exceed the maximum junction temperature limit $T_{j\,max}$ specified in the data sheet and, in this case, $T_{j\,max}$ is 150 ℃ [45]. The temperature difference between junction and heat sink can be calculated using $\Delta_{JH} = P_{loss} \times (R_{th,jc} + R_{th,ch})$, here $R_{th,jc}$ and $R_{th,ch}$ are the thermal resistance from the junction to the case and the case to the heat sink, respectively. For the losses given in TABLE V (calculated using procedure specified in [47]), and $R_{th,jc}$ = 42 K/kW and $R_{th,ch}$ = 8 K/kW from data sheet [45], the resultant Δ_{JH} = 37 ℃ . Considering 80 ℃ at the heat sink, T_j = 117 ℃ which is smaller than the $T_{j\,max}$ = 150 ℃ limit specified for each device. Therefore, the rectifier module has sufficient thermal ratings to operate at full load.

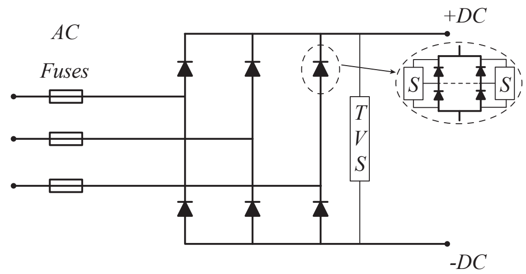


Fig. 4. DRU sub-module with snubbers (S) and transient voltage suppression (TVS) circuts.

B. Case 1: 5 kV, 18 MW, Parallel 12-Pulse Rectifier

The first case considers a medium speed diesel engine (720/750 rpm), operated in a DAC configuration for efficient fuel usage, driving a 6-phase generator (2 x 3-phase) interfaced to a parallel 12-pulse rectifier, as shown in Fig. 5(a). Each 3-phase winding set of the generator is rated at 3.7 kV and 9 MW. The voltage rating of the generator also defines its insulation requirements. The connection of two 9 MW rectifier modules in parallel generates a high quality 5 kV dc-side voltage and also provides redundancy and fault tolerance in the system. In case of any generator or rectifier fault, e.g., failure of one of the 3-phase winding set or rectifier module, the system can be operated in a de-rated mode, i.e., non-essential loads can be disconnected from the system. The LC-filter at the output of the rectifier is designed according to the steps highlighted in [47]. The ac-side input voltage and current, and dc-side voltage and current of the each DRU sub-module are given in Fig. 6(a), Fig. 6(c) and Fig. 6(e), whereas, dc-side voltage and current for the complete rectifier system supplying a 18 MW load are

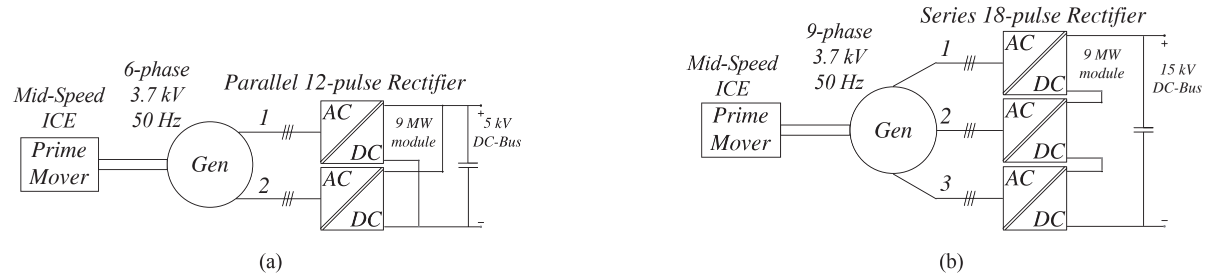


Fig. 5. Proposed multi-phase multi-pulse configuration. (a) Case 1: 5 kV, 18 MW, parallel 12-pulse rectifier based dc supply. (b) Case 2: 15 kV, 27 MW, series 18-pulse rectifier based dc supply.

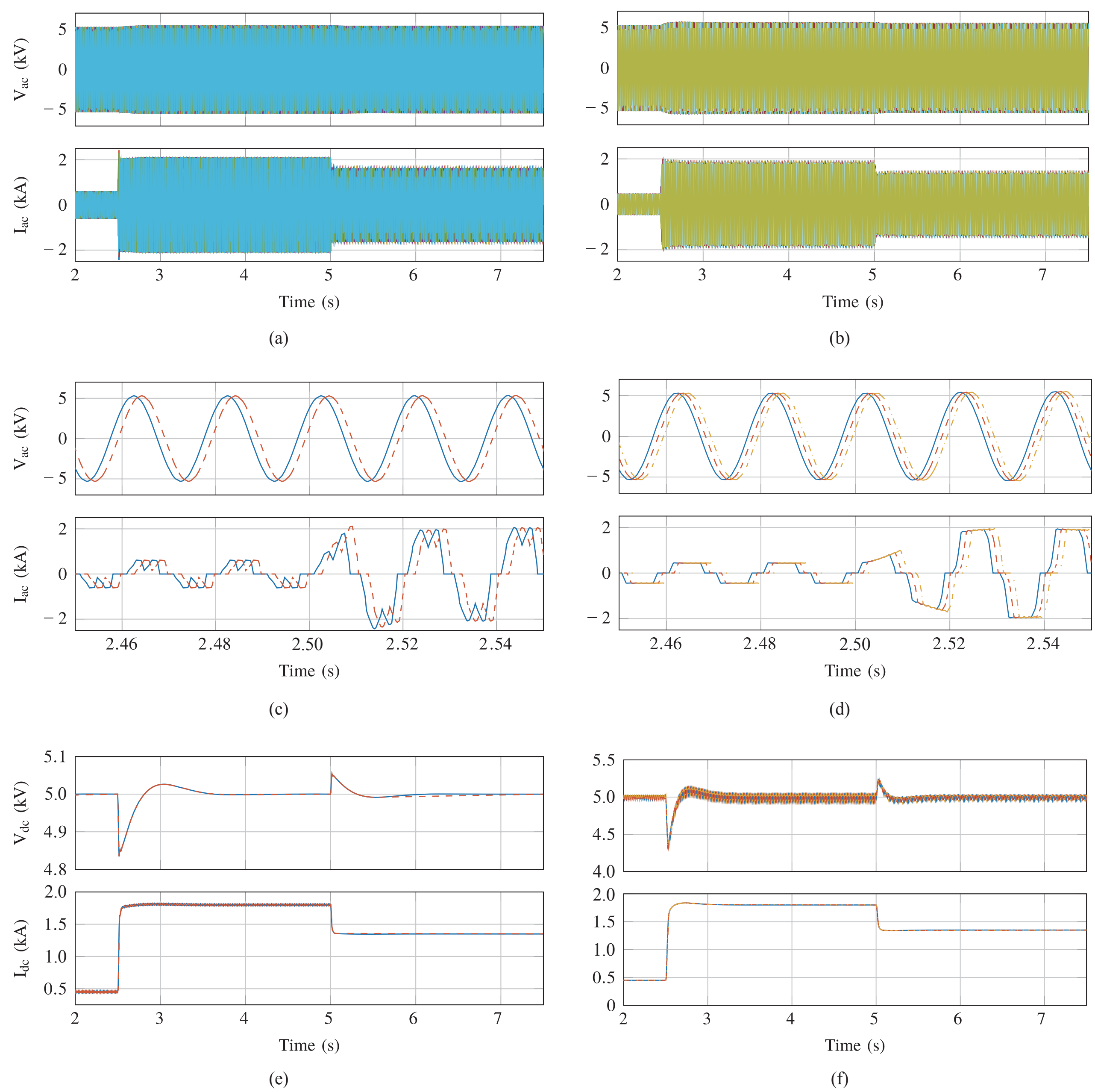
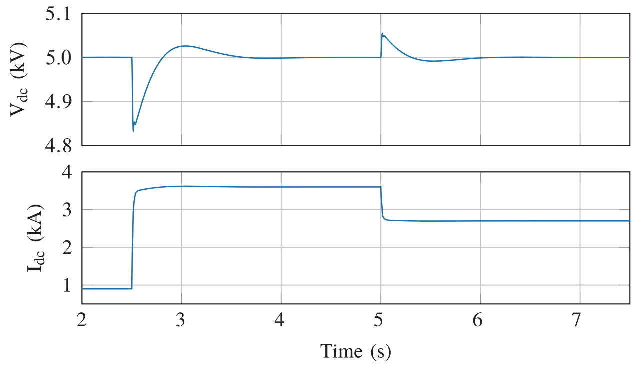
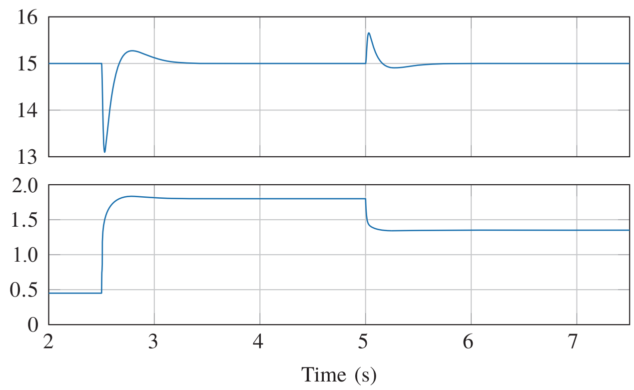


Fig. 6. The ac and dc-side voltage and current wave forms for DRU sub-modules for case 1 and case 2. (a) AC voltage and current for case 1, highlighting envelope of the voltages and currents. (b) AC voltage and current for case 2, highlighting envelope of the voltages and currents. (c) Zoom in of the load change from 25% to 100% at 2.5 s (solid for phase A of the 1st winding set and dashed for phase A of the 2nd winding set). (b) Zoom in of the load change from 25% to 100% at 2.5 s (solid for phase A of the 1st winding set, dashed for phase A of the 2nd winding set) and dash-dotted for phase A of the 3rd winding set). (e) DC voltages and currents for case 1 with solid for 1st sub-module and dashed for 2nd sub-module. (f) DC voltages and currents for case 2 with solid for 1st sub-module, dashed for 2nd sub-module and dash-dotted for 3rd sub-module.



(a)



(b)

Fig. 7. Time domain simulations for (a) Case 1. (b) Case 2.

shown in Fig. 7(a). The load is changed from 25% to 100% at 2.5 s and then dropped to 75% at 5 s. The only control working is the AVR of the generator which corrects the voltage.

C. Case 2: 15 kV, 27 MW, Series 18-Pulse Rectifier

The second system configuration also considers a medium speed diesel engine driving a 9-phase generator (3 x 3-phase) interfaced to a series 18-pulse rectifier (Fig. 5(b)). Each generator 3-phase winding set is rated for a voltage of 3.7 kV and 9 MW. The diode rectifier module designed earlier is used here as well and 3 of it are connected in series to realize a 15 kV dc supply rated at 27 MW. As discussed earlier, the series multi-pulse rectifiers provide flexibility when it comes to selecting voltage classes of the generators and the loads, e.g., here a generator rated at 3.7 kV can supply a propulsion motor rated at 11 kV without the requirement of a step up transformer. In case of any faults, e.g., generator or rectifier side faults, this configuration requires the system to be shutdown and repaired before supplying the loads again. The ac-side input voltage and current, and dc-side voltage and current of the each DRU sub-module are given in Fig. 6(b), Fig. 6(d) and Fig. 6(f), whereas, dc-side voltage and current for the complete rectifier system supplying a 27 MW load are shown in Fig. 7(b). The load is changed from 25% to 100% at 2.5s and then dropped to 75% at 5s. Again, only the AVR of the generator corrects the terminal voltage.

D. Fault Withstand Capabilities

Faults are inevitable to happen in complex systems and the different equipment present is characterized with fault withstand capabilities. Generally, power electronics equipment has much lower over-current withstand capability compared to other equipment. Thus, knowing surge current and thermal capabilities of all the equipment is of high importance for developing protection coordination strategies. In the state-of-the-art MVAC electrical distribution systems the initial short circuit current is usually 10-15 times the rated current. This current then settles to 3-5 times the rated current, in 500ms-1s, when the ac circuit breaker is operated [5]. However, the surge current and thermal capabilities of power electronic devices are much lower than the generators, transformers, cables, and so on. This means that these devices are the bottlenecks for the protection coordination strategies. Following the physical settings of the LVDC system, as discussed in the introduction, the proposed MVDC supplies are considered to be equipped with multi-phase generators having an excitation removal system to lower the short circuit currents, even though this is very slow action, considering fault dynamics. Additionally, two scenarios are defined to test the proposed rectifier topologies for their fault handling capabilities considering a dc pole to pole fault. These different scenarios consider the removal of the generator excitation at 2ms, with a excitation time constant of 5s:

- Generator with rated X_g''.
- Generator with 1.5 rated X_g''.

The two scenarios test the impact of the excitation removal, higher X_g'' and different distribution lengths on the fault energy and its implications on the fault withstand capability of the rectifiers. The 12-pulse parallel and 18-pulse series DRUs for 5 KV and 15 kV MVDC distribution, respectively, are simulated for the above scenarios with a 10% fault impedance and fault at two different points in the distribution system. The simulations results of the dc-side voltage, currents and fault energy (I^2t) are shown in Fig. 8. It can be observed from Fig. 8 that after the fault condition occurs at 2s, the fault currents are lower for a higher X_g'' but this has negligible impact on the peak of the fault current, which is almost 10 times the rated current for both cases. Additionally the farther the fault is from the source, the higher is the impact of the cable, which results in a lower peak of the fault current. It is worth noting that the surge current after fault for 12-pulse rectifier reaches upto 31 kA, shown in Fig. 8(a), but it is shared among the two rectifier modules, whereas, for the 18-pulse rectifier where the initial surge is 17.6 kA, shown in Fig. 8(b), all the current flows through each of the modules. The surge current I_{FSM}, of the device selected to design these rectifiers, is given in TABLE V and has a value of 10.5 kA for a 10 ms half-sine pulse. As two parallel connected devices are used in each module, their combined surge capability is 21 kA for a 10 ms half-sine pulse, and in both cases the initial fault current pulses of 10 kA and 4.5 kA (10ms half-sine pulse) are below the surge current capability of the rectifiers. Thus, both rectifiers are sufficiently sized to handle initial fault currents.

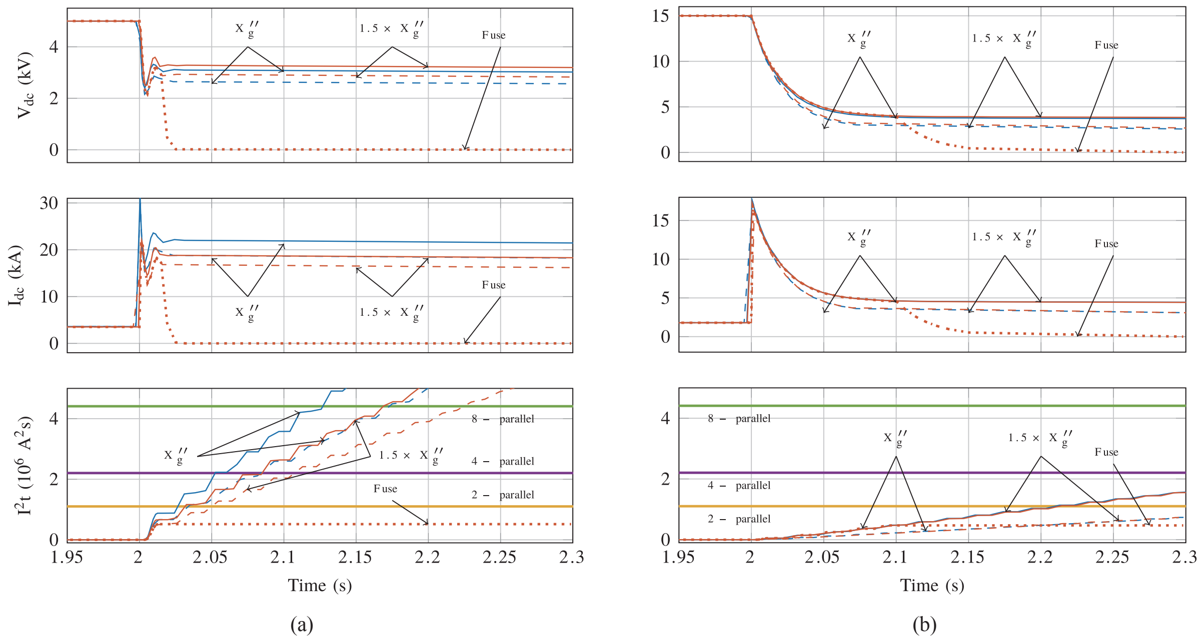


Fig. 8. Simulation results for dc-side pole to pole fault at 2 s. Considering (i) Rated X_g" with two different points for fault: at 10 m (solid line) and at 200 m (dashed line) from source, (ii) 1.5 Rated X_g" with two different places for fault: at 10 m (solid line) and at 200 m (dashed line) from source and (iii) 1.5 Rated X_g" with ac-side fuses (dotted line). A comparison of fault I^2t with allowed I^2t of two, four and eight parallel devices conductiong. (a) Case 1. (b) Case 2.

The bottom plots in Fig. 8 show the fault energy for the two scenarios, discussed earlier, and compares it with the thermal capabilities of different number of devices in parallel. It can be observed for *Case 1*, from Fig. 8(a), that the fault energy rises very fast, i.e., in 25ms surpasses the combined I^2t capacity of two parallel connected diodes. Even with higher X_g" and L_c = 0.14 mH, the I^2t capacity of two parallel connected diodes is surpassed in 50 ms. It can also be observed that even connection of 8 diodes in parallel is not enough to with stand the fault energy and, therefore, other means are required to protect this rectifier. For *Case 2*, Fig. 8(b), the rise of fault energy is rather slow, compared to *Case 1*, and but it still surpasses the I^2t of the diodes in around 200ms. Similar to *Case 1*, external means are required to protect this rectifier as the fault current only goes to zero after several seconds and connecting several devices in parallel might not sufficient to with the fault energy in this time. For the analysis, number of diodes in parallel have been considered, while in reality the problem could be analyzed from the view of DRUs in parallel.

One inexpensive way to protect these rectifiers would be to consider fuses on the ac-side (no dc-side fuses because there is no regeneration) that can melt in a few milliseconds. These fast fuses also limit the fault current and the resultant energy through the diodes. In order to protect the rectifiers, in *Case 1* and *Case 2*, these fuses must act fast enough to protect the rectifiers for both high and low fault currents. For *Case 1*, the fault current is 21.5 kA for for rated X_g" and $L_c = 7\ \mu$H, however, with higher X_g" and L_c = 0.14 mH, the fault current is lower, i.e., 16.6 kA. As in both scenarios the fault current are relatively high, the fuses selected must be fast enough and sized adequately to act within a few milliseconds. For *Case 2*, the fault current is 5 kA for rated X_g", while, a higher X_g" reduces it to 3 kA, irrespective of cable impedance. In both scenarios, the fault current is close to the rated current of 1.8 kA, i.e., 2.7 and 1.7 times, respectively.

In both cases, to protect the rectifier the ac-side fast fuses must be able to withstand rated current and voltage, under normal conditions, and act fast enough to block the fault currents, i.e., their I^2t must be lower than the of the diodes I^2t for the same currents. The impact of fuses on currents and voltages, for both cases, can be seen in Fig. 8. High power applications usually leads to possible series and parallel connection of available fuses and must be specially sourced from the manufactures [48], [49]. The manufactures must ensure < 10% mismatch between different fuses and proper working under normal and fault condition to ensure reliability and protection.

V. Conclusion

This paper critically analyses the available and proposed technologies for the ship on-board power supplies and the practices of the state of the art MVAC electrical distribution systems in ships. Different technologies are proposed as supply technologies, in literature, for the future MVDC supplies, e.g., high speed gas turbines, high speed PMSGs, and active rectifiers and MMCs for ac/dc conversion. These technologies have their benefits but they are either not commercially available or are too expensive for marine applications. In commercial drives, multi-pulse rectifiers are connected to multi-secondary transformers to produce high power quality on the dc-side. As transformers are set to be omitted from the emerging MVDC systems, 3-phase generation can be replaced with N-phase generation, which will provide the benefit of using the multi-pulse rectifiers to have high quality dc supply.

As illustration, two designs of multi-phase multi-pulse

MVDC supplies, driven by medium speed ICEs (operated in DAC mode) are presented and discussed. These supplies are: i) a 2 x 3-phase generator interfaced with parallel 12-pulse rectifier for a 18 MW, 5 kV dc distribution, and ii) a 3 x 3-phase generator interfaced with series 18-pulse rectifier for a 27 MW, 15 kV dc distribution. To realise these supplies, a 6-pulse DRU sub-module is designed with commercially available diodes, which can withstand thermal load under normal operation. Additionally, these two rectifiers are analysed under different fault scenarios and it is shown that they can handle the high surge currents. However, it is also seen that if the faults are not cleared in a few milliseconds, the rectifiers will fail due to every high fault energy. To protect these rectifiers, special purposes fast fuses could be used, placed on the ac-side, to clear these faults.

Additionally, the two notional systems presented here highlight the benefits of multi-phase multi-pulse dc supply. It can be observed that parallel connection of rectifiers improves not only the dc-side supply but also adds redundancy and fault tolerance to the system. Series connection of rectifiers also improves the dc side supply and adds the flexibility in choosing voltage class of generators and motors. The choice of parallel or series rectifiers depends on the system designers, the requirements of the system and the availability of the required equipment.

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Experimental Investigation on the Transient Switching Behavior of SiC MOSFETs Using a Stage-Wise Gate Driver

Georges Engelmann, Tizian Senoner, and Rik W. De Doncker

***Abstract*—A multiple stage gate driver for SiC MOSFETs based on a switched resistor topology is introduced and a hardware realization is presented. The measurement setup is shown in detail to highlight the quality of the shown measurement results. The evaluation of the stage-wise driver is conducted by comparing the switch and diode peak voltages as well as peak currents with regard to the switching losses to a reference driver. The switching transients are generated using a double pulse test bench. A detailed investigation on two- and three-stage operation for both, the turn-on and turn-off events are presented. A variation of gate resistors and different timings is conducted for each stage and evaluated using the resulting measurements. It is shown that the drain-source peak voltage is reduced by 45% while maintaining equal turn-off losses. Analogously, a reduction of 51% of the diode peak voltage and a reduction of 50% of the peak reverse recovery current at the same time is feasible for equal turn-on losses.**

***Index Terms*—MOSFET switches, power electronics, semiconductor device measurements, switched resistor circuits, test equipment.**

I. Introduction

POWER electronic converters are used in a wide field of applications and a growing tendency is seen. Their appearance is growing in low- and medium-voltage applications. They are the key technology for renewable energies or electric traction systems, especially electric vehicles [1]-[3].

Reductions in volume and weight are a crucial aspect to achieve lower costs of the converters. This leads to a higher integration level of the converters [4], [5]. A high integration level creates the need for good thermal power flow by using e.g., thermal interface materials [6]. Furthermore, this integration level of power electronic converters can be increased using the emerging high-temperature wide-bandgap (WBG) power semiconductors [7]-[9] as higher switching frequencies can be achieved, which in turn allows a reduction of the filter size. However, higher switching frequencies and steeper switching slopes are the source for higher electromagnetic interference (EMI) [10].

An extensive comparison of the switching performance between insulated-gate bipolar transistors (IGBTs) and silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) is presented in [11], [12]. Considerable efforts have been made to affect the switching behavior of IGBTs, for example to influence the EMI, voltage stress or switching losses [13]-[16].

As the switching times of SiC MOSFETs are reduced by at least a decade compared to the switching times of IGBTs, the design of an active gate driver (AGD) is more challenging. Nevertheless, various approaches, which are widely known for silicon power semiconductors, are found in literature, such as protection circuitry [17], current controlled gate drivers [18], resonant gate drivers [19] or gate drivers for series connected MOSFETs [20] or medium-voltage SiC MOSFETs [21]. Some investigations tend to handle parasitic turn-on [22], [23] or influence the switching speed using passive components in the gate path [24]-[26]. Very high switching speeds for WBG power semiconductors are achieved using inductive feedback as shown in [27]. Similar to integrated current sense structures for IGBTs, integrated current sense structures of SiC MOSFETs are appearing for protection or current sensing applications [28].

A two-stage AGD using analog circuitry with high bandwidth is presented in [29]. A multi-level AGD influencing the gate voltage during the Miller plateau is shown in [30].

In this work, a multiple-stage AGD for a 1.2 kV SiC MOSFET *CPM2-1200-0040B* based on a switched resistor topology is presented. A similar approach as shown in [15], [30] is followed to influence the switching behavior. The influence on the switching behavior for two- and three-stage operation is shown for the turn-on as well as the turn-off event. The investigations are evaluated against a reference push-pull gate driver. The goal is to show that the voltage peaks and current peaks can be reduced individually without a penalty on switching losses. TABLE I lists the device pa-

TABLE I
Specifications of the SiC MOSFET and Test Setup

Description	Specifier	Value
Blocking voltage	U_{DSS}	1200 V
Rated current	I_D	63 A
DC-link voltage	U_{dc}	700 V
Test current	I_D	60 A
Junction temperature	ϑ_j	35 °C

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rameters and test conditions at which the investigations are carried out. The junction temperature ϑ_j is given as 35 °C as all measurements are conducted at room temperature inside the test bench. Due to the fast switching slopes of the SiC devices, high bandwidth equipment has to be used and the correct employment of the latter is crucial for accurate measurement results [31]. Therefore, a dedicated section dealing with the measurement setup is included in this paper.

II. Stage-Wise Gate Driver Topology

The proposed stage-wise driver consists of a state-of-the-art voltage source gate driver using a variable gate resistance R_{gate}. The influence on the switching behavior is accomplished by changing the value of the gate resistance during the switching action. The presented topology already led to good results using silicon IGBTs as shown in [15]. In comparison to a switching event using an IGBT, the fall and rise times of voltage and current of a SiC device are at least a decade faster. This means, that if the switching event of an IGBT lasts for 100 ns (e.g., see [15], Fig. 11), it will last for less than 10 ns when using a SiC device. The gate driver, which is presented in [15], has a minimum time resolution of 10 ns due to the limited clock speed of the field-programmable gate array (FPGA). A timing of less than 1 ns is required to be able to influence the switching behavior of SiC devices. The employed topology of the driver is shown in this section. The high resolution timing, which is required as input stage to the driver hardware, is introduced in section III.

A. Topology

The schematic topology of the driver is shown in Fig. 1. It consists of three parallel branches, of which each constitutes of a push-pull stage configuration. Each branch consists of a turn-on and turn-off gate resistance $R_{g,on,n}$, $R_{g,off,n}$, an n-channel and p-channel MOSFET $Q_{on,n}$, $Q_{off,n}$ as well as a dual low-side driver chip IC_n. A comparison among several commercial gate driver integrated circuits (ICs) and n- and p-channel MOSFETs is conducted. The ICs with the fastest rise times (n-channel) or fall times (p-channel) using a dummy 10 nF capacitive load are selected. The selected devices are listed in TABLE II including the rise and fall times using the 10% . . . 90% borders of the dummy and gate capacitor voltage. The gate-source capacitance C_{gs} of the selected power semiconductor is 2 nF [32]. Assuming a RC charging curve, the time constant is reduced by a factor of 5 for the given SiC MOSFET compared to the dummy capacitor, resulting in 1.9 ns. However, the rise and fall times are still significant compared to the envisaged time resolution and the expected duration of the switching events. As the aim of the stage-wise driver is to only partially charge (or discharge) the gate capacitance during each stage, only a fraction of the indicated rise/fall time is required and thus within an acceptable range for the presented driver. The gate driver is supplied using the supply voltages $U_{GS,off} = 0$ V and $U_{GS,on} = 18$ V.

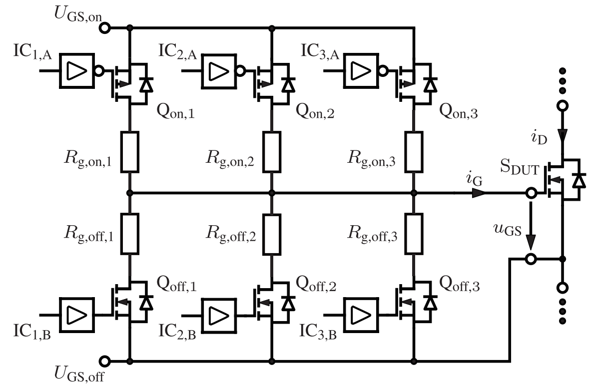


Fig. 1. Topology of the proposed stage-wise driver.

TABLE II
Selected Devices for the Driver Design

Device	Part nr.	rise/fall time	
IC_n	*UCC27523*		
$Q_{on,n}$	*BSZ180P03NS3E*	1.9 ns[1]	9.4 ns[2]
$Q_{off,n}$	*DMN3035LWN*	1.9 ns[1]	9.4 ns[2]

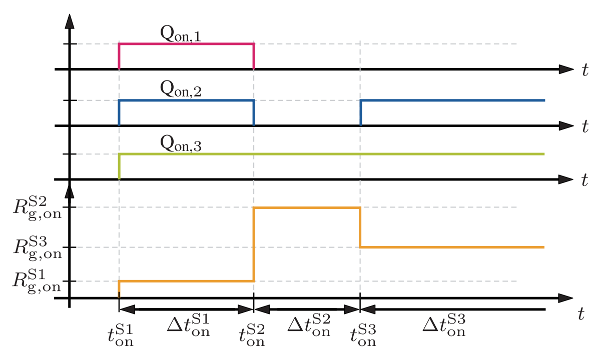


Fig. 2. Operation principle of the stage-wise driver.

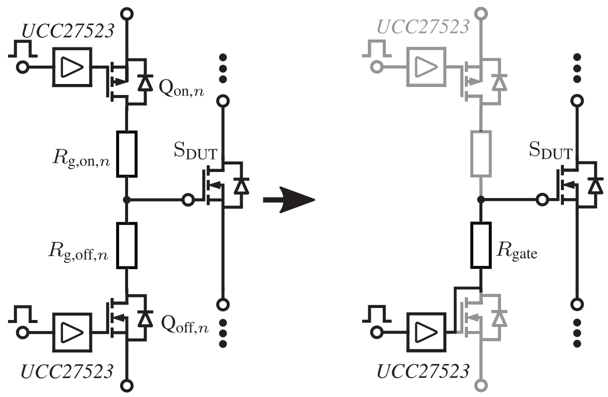
B. Operation Principle

The operation principle of the stage-wise driver is shown using an exemplary sequence for a turn-on event plotted in Fig. 2. During a state S, one or more MOSFETs $Q_{on,x}$ are turned on resulting in an effective gate resistance $R^{S}_{g,on}$. In the plotted exemplary waveforms, the switches $Q_{on,1}$, $Q_{on,2}$ and $Q_{on,3}$ are turned on at the same time during stage one. The effective first stage gate resistor results in

$$R^{S1}_{g,on} = R_{g,on,1} \parallel R_{g,on,2} \parallel R_{g,on,3}.$$

The first stage lasts for a time Δt^{S1}_{on}. Analogously, the gate resistance for the second stage is set to $R^{S2}_{g,on} = R_{g,on,3}$ for a duration Δt^{S2}_{on}. The third stage is, in this example, the last stage and thus lasts until the device under test (DUT) is switched off. This is indicated by setting the third stage tim-

[1] The indicated time is normalized to the gate capacitance $C_{gs} = 2$ nF.
[2] This is the measured rise/fall time using a 10 nF capacitance.



(a) Stage-wise driver. (b) Reference driver.

Fig. 3. Reference driver circuit.

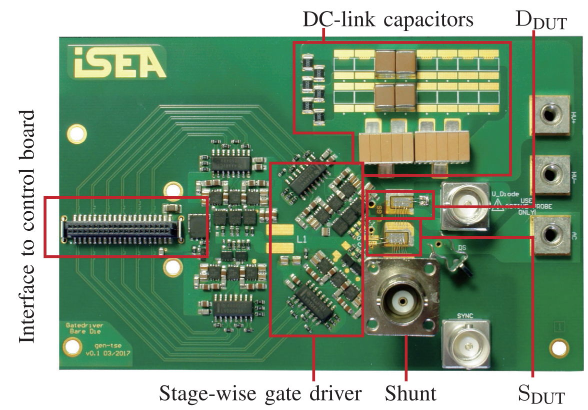


Fig. 4. Photograph of the PCB containing the driver and SiC bare dies.

ing to infinite $\Delta t_{on}^{S3} = \infty$.

C. Gate Driving Strategy

The goal of manipulating the switching waveforms is to achieve lowest switching losses while reducing the device stress at the same time. A similar approach as used in [15], [30] is employed.

This goal is achieved with an initial fast (dis)charging of the gate. Therefore, the smallest possible gate resistance is chosen for the first stage. However, a small gate resistance results in a high u_{DS} overshoot (turn-off event) or a high i_S, u_{Diode} overshoot (turn-on event), which are reduced by slowing down the (dis)charging process during the second stage using an increased gate resistance. A third stage, using a small gate resistance, is appended because the second stage resistance would result in very high switching losses for the remaining switching process.

However, besides the qualitative approach, no quantitative approach regarding timing and resistor values is known prior to the investigations. Therefore, a large variation of the different timings and resistor values are conducted to allow the deduction of an optimum driving strategy.

D. Reference Design

To allow an evaluation of the stage-wise gate driver, a classical single stage reference driver is needed. To avoid any unnecessary influence of, for example, the layout, on the switching behavior, the stage-wise driver is slightly modified, as shown in Fig. 3. One channel of the dual low side gate driver *UCC27523* is reconfigured to directly drive the gate resistance R_{gate}.

III. Hardware Realization

Parasitic inductances or capacitances have a high impact on the switching behavior [33]. Especially, when switching using high voltage or current slopes, the influence of these parasitic elements rises. Thus, a good layout of the switching cell and driver is crucial to achieve the desired results.

TABLE III
Valuse of the Different Stary Inductances

Inductance	Value	Inductance	Value
$L_{\sigma,DC}$	3.8 nH	$L_{\sigma,Switch}$	2.0 nH
$L_{\sigma,Diode}$	1.7 nH	$L_{\sigma,Shunt}$	6.8 nH

Apart from the switching cell and driver board, the control board is introduced. The control board generates the different gate signals for the different branches.

A. Switching Cell and Driver Board

The printed circuit board (PCB) containing the switching cell and gate driver is pictured in Fig. 4. The control signals for the driver chips are transmitted using low-voltage differential signaling (LVDS) from the FPGA on the control board. A LVDS to single ended converter (*SN65LVDS048AD*) controls the dual low side driver ICs. The high-side gate is short circuited on the PCB (as seen in Fig. 4) as only the low-side MOSFET S_{DUT} is switched in the double pulse test. A close-up view on the low-side MOSFET is seen in Fig. 5. The Bayonet Neill-Concelman (BNC) plugs allow a repeatable measurement of the high-side diode voltage u_{Diode} and low-side drainsource voltage u_{DS}. The source current is measured using a T&M *SDN-414-10* current viewing resistor (CVR). The different stray inductances of the switching cell are determined using a current pulse generator [34] and methodology as described in [33]. The resulting values, corresponding to the schematic shown in Fig. 8, are listed in TABLE III. It is noticed, that the CVR is responsible for 47.5% of the total stray inductance.

B. Control Board

A photograph of the front and back side of the control board is shown in Fig. 6(a) and Fig. 6(b). The board hosts an *AT32UC3A1512* microcontroller (MCU) and a Xilinx Spartan 6 *XC6SLX9* FPGA. The MCU connects to a personal

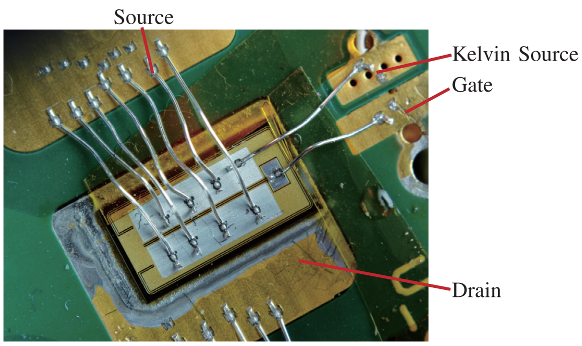
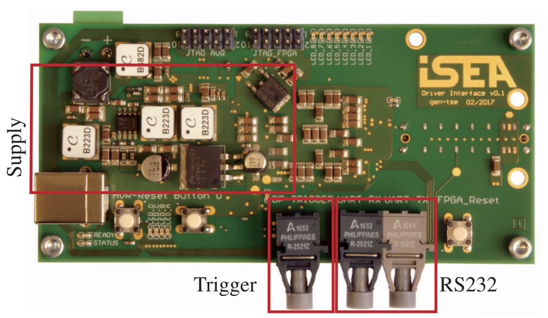
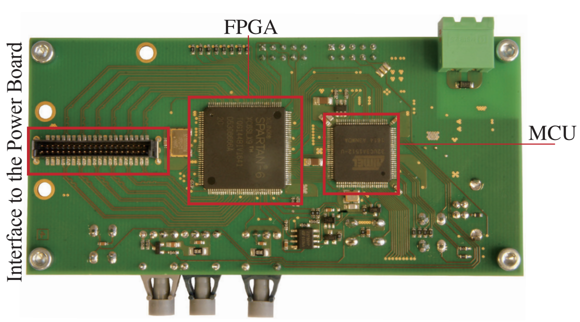


Fig. 5. Close-up view on the low-side SiC bare die.



(a) Top view



(b) Bottom view

Fig. 6. Photograph of the control board.

computer (PC) via *RS232* to allow on the fly configuration of the FPGA. A serial peripheral interface (SPI) bus ensures communication between the FPGA and MCU.

The main function of the FPGA is the generation of the different gate signals for each branch. A precise time resolution of less than 1 ns is required for an appropriate control of the SiC power semiconductors. The maximum clock speed of the employed FPGA of 300 MHz does not allow a higher time resolution than 3.33 ns. To achieve higher time resolutions, the delay-locked loop (DLL) functionality of the digital clock manager (DCM) of the FPGA is used. A very precise timing is achieved using the phase shift φ, as shown in Fig. 7. In total, four DCM blocks are available in the FPGA. Using a clock frequency of 50 MHz, the DLL allows a precise timing control of the edge of a signal of up to 23 ps.

IV. Measupement Setup

Measuring the voltage and current waveforms of SiC devices properly is not a trivial task [31]. As the measurement setup influences the resulting measurements to a large extend [35], a detailed description of the employed setup is shown prior to the main investigations on the gate driver.

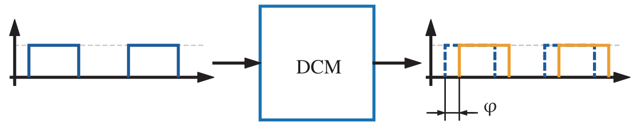


Fig. 7. Delay-locked loop operation principle.

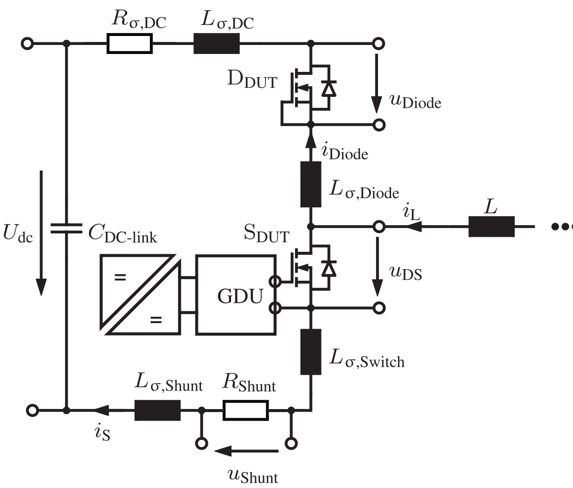


Fig. 8. Schematic of the switching cell used for the double pulse tests.

The evaluation of the driver is made by comparing the resulting transient switching waveforms of the low-side semiconductor to the measurement results achieved using a push-pull reference driver. A double pulse test bench [36] is employed to conduct automated series measurements using different DC-link voltages, currents and temperatures [37].

The waveforms are recorded using a Teledyne LeCroy *HDO6104* oscilloscope using a vertical resolution of 12 bit, 1 GHz bandwidth and a 2.5 $^{\mathrm{GS}}/_{\mathrm{s}}$ sample rate. A schematic of the electrical circuit of the switching cell is shown in Fig. 8. Two 900 V, 1.25 μF CeraLink capacitors are used in parallel with four ceramic capacitances to form the DC-link capacitor $C_{\mathrm{DC\text{-}link}}$. The voltage measurements u_{DS}, u_{Diode} and u_{GS} are made between the drain tab and kelvin source contacts. The low-side switch current i_{S} is measured using the indicated CVR.

The high-side diode current i_{Diode} is calculated using the low-side current i_{S} and inductor current i_{L} using (1). As the inductor current is not measured during the double pulse test, it is retrieved using a linear interpolation of the switch current i_{S} prior to turning the switch off at the time where it is still fully on ($t = t_{\text{turn-off,-}}$) and shortly after it is switched back on ($t = t_{\text{turn-on,+}}$) as indicated in (2) and (3).

$$i_{\mathrm{Diode}} = i_{\mathrm{L}} - i_{\mathrm{S}} \tag{1}$$

$$i_{\mathrm{L}}\left(t = t_{\text{turn-off}}\right) = i_{\mathrm{S}}\left(t = t_{\text{turn-off,-}}\right) \tag{2}$$

$$i_{\mathrm{L}}\left(t = t_{\text{turn-on}}\right) = i_{\mathrm{S}}\left(t = t_{\text{turn-on,+}}\right) \tag{3}$$

A certain inaccuracy in the given current measurement method is taken into account. First, the measured source current i_S does not exactly represent the MOSFET channel current due to the parasitic output capacitance C_{oss}. However, literature shows that the influence of the output capacitance C_{oss} cancel each other when considering the sum of the turn-on and turn-off losses [38]. Besides calorimetric switching loss measurements, no accurate MOSFET channel current measurement technique, which is independent of the output capacitance C_{oss}, is known. For precisely this reason, the later on conducted measurements are compared to reference measurements which are recorded under exactly the same conditions. Second, the high-side diode current i_{Diode} is, besides the output capacitance C_{oss} of the high-side switch, additionally distorted by parasitic capacitances across the load inductance, or generally between the AC terminal and ground. The latter could be improved by using a CVR in the high-side path in combination with isolated low voltage measurement equipment.

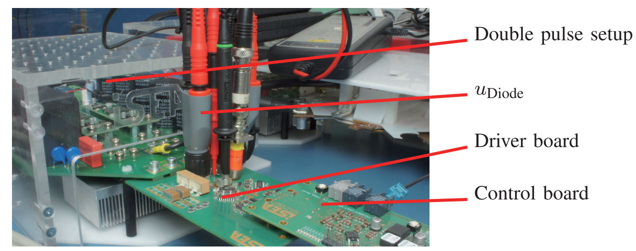
As the CVR connects the oscilloscope ground to the source potential of the low-side switch, the utilization of a further passive probe is not envisaged as the grounding terminal of the probe would create a ground loop via the oscilloscope to the CVR. This would facilitate circulating currents through the shielding of the coaxial cables and herewith disturb the measurements [35]. However, as an extensive study between various active differential and passive probes for small and large signal measurements got conducted prior to this work, the passive probe *PP018-2* largely outperforms the remaining probes for gate voltage measurements.

Thus, the following compromise is made: Exactly the same double pulse measurement is conducted twice after each other, first with only the passive probe connected to gate followed by a measurement with only the coaxial cable of the CVR connected. The gate voltage is measured additionally using the active probe for both measurements, which is used to synchronize and merge both measurements. The use of the active probe signal to merge the merging procedure is considered as valid, as the repeatability of the measured signal is very good. Using this procedure, it is guaranteed that no unnecessary distortion occurs due to circulating currents in the coaxial shielding. The only drawback, which is disregarded, is the influence of an eventual jitter of the various ICs used for the AGD. The employed measurement probes are summarized in TABLE IV. A photograph of the setup is pictured in Fig. 9.

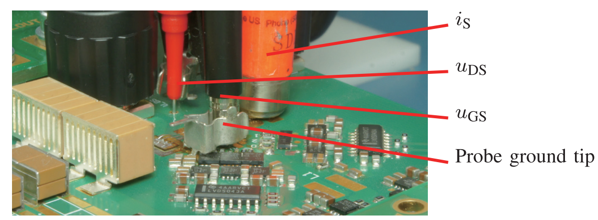
As the switching times of the SiC MOSFETs, which are within 10 ns ... 20 ns, are in the same range as the probedelays, a delay compensation is required. As no appropriate information is available in the provided data sheets, the individual propagation delays of the probes are measured using a Tektronix *Type 109* pulse generator and a high-voltage probe calibrator *KHT 1000*. The resulting values are indicated in TABLE IV. The propagation delay of the CVR is due to the coaxial cable (*Radiall R284C0351005*) with a length of 1 m and external 50 Ω terminator.

TABLE IV
MEASUREMENT EQUIPMENT

Manufacturer	Part Nr.	Measured signal	Probe delay	Bandwidth
PMK	*BumbleBee*	u_{DS}, u_{Diode}	12.3 ns	300 MHz
Testec	*TT-SI 9101*	u_{GS}	11.7 ns	100 MHz
Teledyne LeCroy	*PP018-2*	u_{GS}	6.3 ns	500 MHz
T&M Research	*SDN-414-10*	i_S	5.4 ns	2000 MHz



(a) Measurement setup



(b) Close up view

Fig. 9. Photograph of the measurement setup.

V. Reference Measurements

The measurements using the reference driver are introduced and presented in this section. As the stage-wise gate driver makes use of various gate resistances during a single switching event, the results cannot be simply compared to a reference measurement using a specific gate resistance. Thus, the reference measurements are made using various gate resistances in the range R_{gate} = 0.5 Ω ... 10 Ω.

A. Measurements of the Turn-On Event

The turn-on measurements cover the turn-on event of the low-side switch as well as the turn-off event of the high-side diode. The measured waveforms using the different gate resistors are shown in Fig. 10. The respective voltage and current slopes are indicated for the current waveforms as well as for the switch and diode drain-source voltage u_{DS}, u_{Diode}. The voltage and current fall and rise slopes are indicated in the respective figures. The slopes are calculated using the 10% ... 90% borders of the waveforms, excluding the inductive voltage drop during the turn-on event (see Fig. 10). Depending on the gate resistance R_{gate}, current slopes ranging from 3.4 $^{A}/_{ns}$ ... 20 $^{A}/_{ns}$ are reached. The slope of the low-side drain-source voltage $\frac{du_{DS}}{dt}$ reaches values from −19 $^{V}/_{ns}$ ... −57 $^{A}/_{ns}$

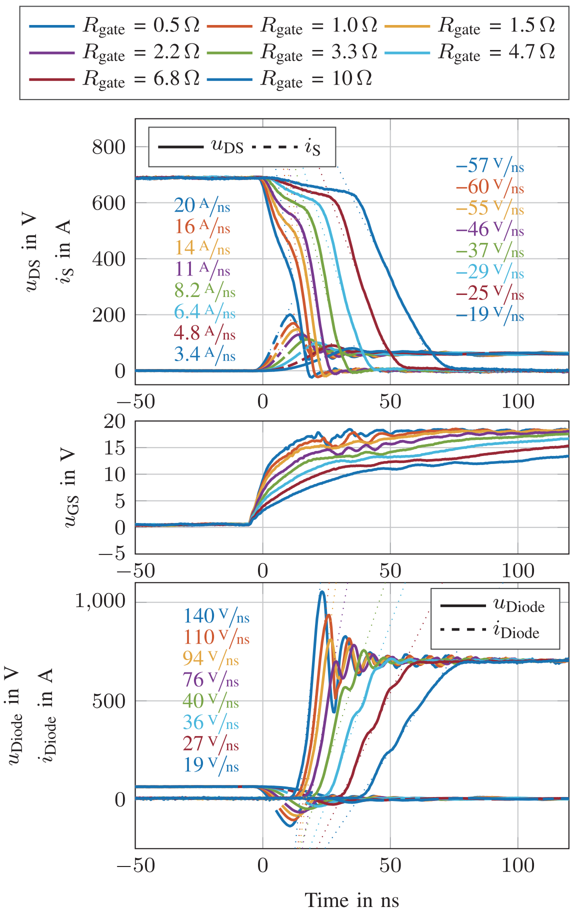


Fig. 10. Reference turn-on event measurements using different gate resistors.

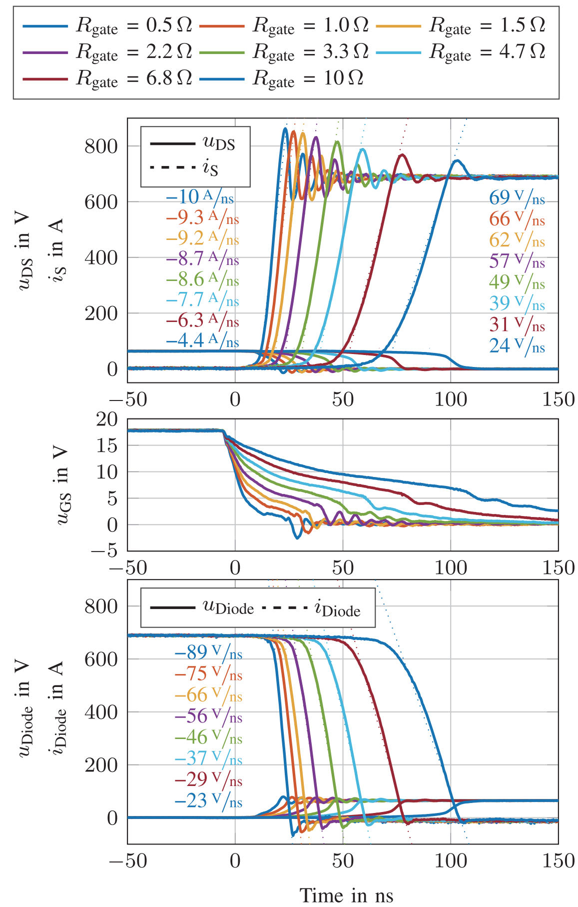


Fig. 11. Reference turn-off event measurements using different gate resistors.

whereas the voltage slope of the diode reach higher values ranging from 19 A/ns ... 140 A/ns.

B. Measurements of the Turn-Off Event

Analogously, the reference measurements of the turn-off event are shown in Fig. 11 together with their corresponding slopes. The current slopes reach from −4.4 A/ns ... −10 A/ns. The slope of the diode voltage u_{Diode} ranges from 22 V/ns ... 82 V/ns whereas the switch voltage slope $\frac{\mathrm{d}u_{\text{DS}}}{\mathrm{d}t}$ ranges from −23 V/ns ... −89 V/ns.

C. Switching Losses

The switching losses of the various switching transitions are calculated using

$$E_{\text{sw}} = \int_{t_{\text{start}}}^{t_{\text{end}}} p_{\text{sw}} \mathrm{d}t = \int_{t_{\text{start}}}^{t_{\text{end}}} (u_{\text{DS}} \cdot i_{\text{S}})\, \mathrm{d}t.$$

The start and end times t_{start} and t_{end} are chosen using the 3% borders of the peak power. A more detailed description of the switching loss extraction algorithm is given in [15]. The resulting switching losses using the reference driver with various gate resistances are shown in Fig. 12.

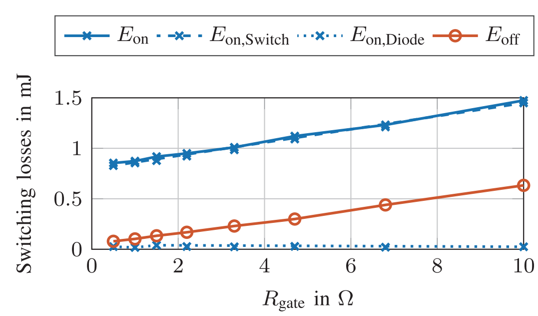


Fig. 12. Calculated switching losses using the reference driver with various gate resistances at U_{dc} = 700 V, I_{D} = 60 A.

VI. Stage-Wise Driver Turn-On Operation

The influence of the stage-wise gate driver on the turn-on event is investigated in this section. At first, a simple change of resistor, from a small value to a larger value, is shown. The aim of slowing down the gate charging is to reduce the diode peak voltage $\hat{U}_{\text{Diode}}$ and the switch peak current $\hat{I}_S$. Afterwards, a third stage is introduced, which further improves the switching behavior.

A. Investigations on the Two-Stage Turn-On Event

The two-stage turn-on event is investigated using the setup

TABLE V
Two-Stage Driver Setup for the Turn-On Event

Stage S	$R^{S}_{\mathrm{g,on}}$	$\Delta t^{S}_{\mathrm{on}}$
1	$0.5\,\Omega$	0 ns … 1.2 ns, ∞
2	$2.2\,\Omega$ … $10\,\Omega$	∞

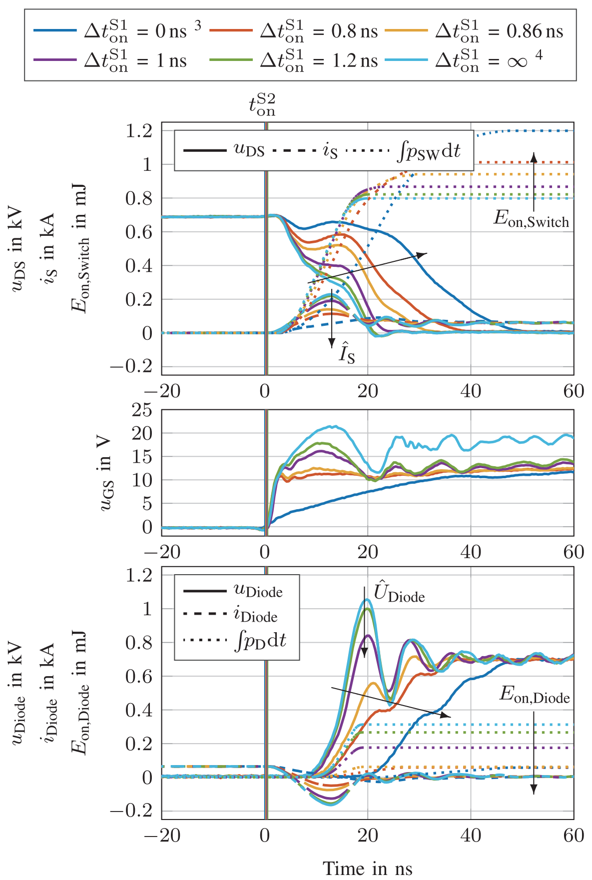


Fig. 13. Two-stage turn-on event waveforms using $R^{S2}_{\mathrm{g,on}} = 10\ \Omega$.

as listed in TABLE V. The resulting transient waveforms using a second stage gate resistance $R^{S2}_{\mathrm{g,on}} = 10\ \Omega$ are plotted in Fig. 13 including two reference waveforms ($\Delta t^{S1}_{\mathrm{on}} = 0$ ns, $\Delta t^{S1}_{\mathrm{on}} = \infty$) for comparison. It is seen, that it is possible to manipulate the waveforms between the two reference measurements. It is shown in Fig. 13, that the diode peak voltage $\hat{U}_{\mathrm{Diode}}$ is reduced down to the DC-link voltage U_{dc}, thus eliminating the overshoot. As it is seen from Fig. 13, that although the turn-on losses are increasing as expected with a shorter duration of the first stage, the losses in the diode are decreasing. As the total turn-on losses include the losses in the diode as well as the switch, an optimum operation point for the turn-on event using a two-stage gate driver has to be found.

B. Investigations on the Three-Stage Turn-On Event

To improve the two-stage switching behavior, a third stage using a small gate resistance comparing to the second stage gate resistance $R^{S3}_{\mathrm{g,on}} < R^{S2}_{\mathrm{g,on}}$ is appended. The driver setup listed in TABLE VI is applied. A good initial setup is chosen for the first and second stage. The resulting waveforms are plotted in Fig. 14.

TABLE VI
Three-Stage Driver Setup of the Turn-On Event

Stage S	$R^{S}_{\mathrm{g,on}}$	$\Delta t^{S}_{\mathrm{on}}$
1	$0.5\,\Omega$	0.86 ns
2	$50\,\Omega$	0 ns … 15 ns
3	$2.2\,\Omega$	∞

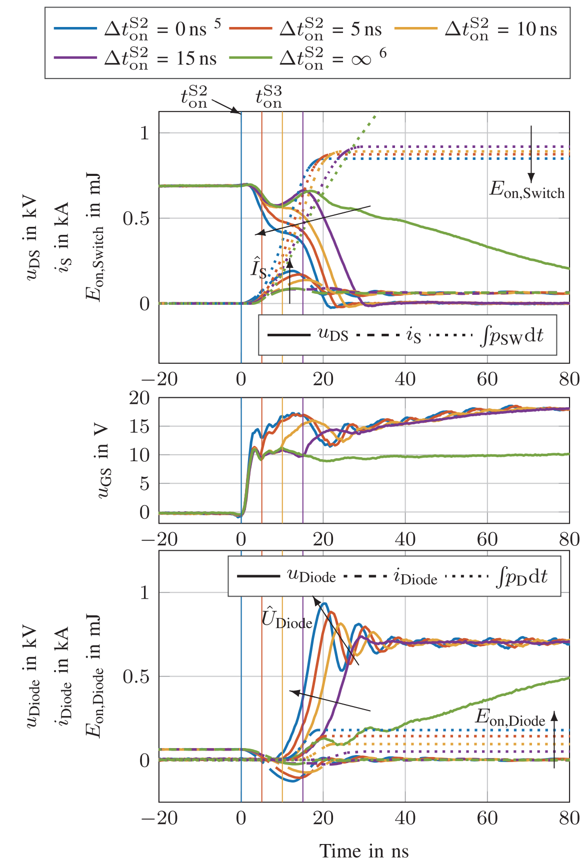


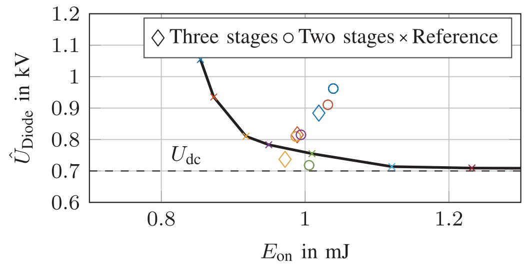
Fig. 14. Three-stage turn-on event waveforms.

It is observed that, by introducing a third stage with a small gate resistance, the losses in the switch decrease comparing to the two-stage operation ($\Delta t^{S2}_{\mathrm{on}} = \infty$). However, the diode losses as well as the device stress ($\hat{I}_{\mathrm{S}}$, $\hat{U}_{\mathrm{Diode}}$) increase at the same time. The evaluation of the performance of the three-stage operation is shown in the following section.

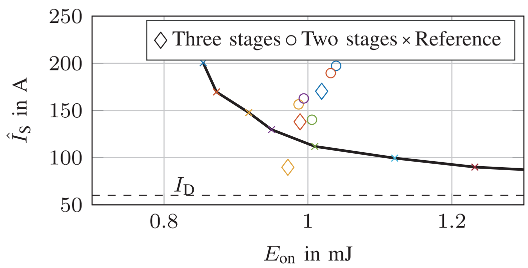
C. Evaluation of the Stage-Wise Turn-On Operation

The preceding sections showed the ability of the AGD to influence the stress and the switching losses of the power semiconductor. It becomes clear from Fig. 13, that during the

[3] Equivalents a single-stage turn-on event using $R_{\mathrm{gate}} = 10\ \Omega$.
[4] Equivalents a single-stage turn-on event using $R_{\mathrm{gate}} = 0.5\ \Omega$.
[5] Equivalents a two-stage turn-on event: $R^{S1}_{\mathrm{g,on}} = 0.5\ \Omega$ to $R^{S2}_{\mathrm{g,on}} = 2.2\ \Omega$.
[6] Equivalents a two-stage turn-on event: $R^{S1}_{\mathrm{g,on}} = 0.5\ \Omega$ to $R^{S2}_{\mathrm{g,on}} = 50\ \Omega$.



(a) High-side diode overshoot voltage vs. turn-on energy



(b) Reverse recovery peak current vs. turn-on energy

Fig. 15. Device stress vs. turn-on energy.

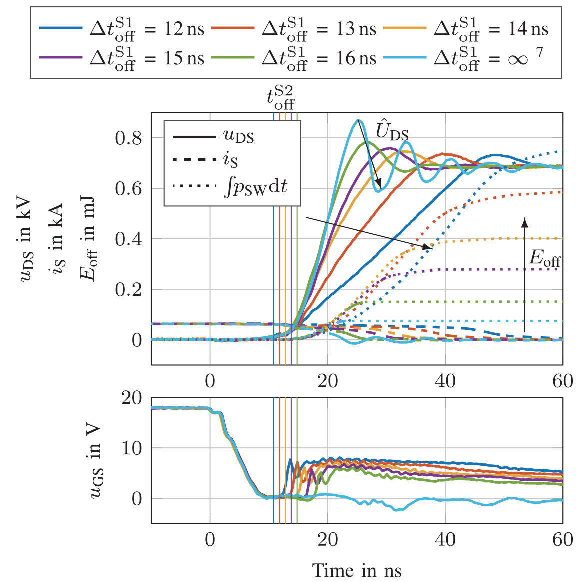


Fig. 16. Two-stage turn-off event waveforms using $R_{\text{g,off}}^{\text{S2}} = 15\ \Omega$.

TABLE VII
TWO-STAGE DRIVER SETUP OF THE TURN-OFF EVENT

Stage S	$R_{\text{g,off}}^{S}$	$\Delta t_{\text{off}}^{S}$
1	0.5 Ω	12 ns … 16 ns
2	4.7 Ω, 12 Ω, 15 Ω, 18 Ω	∞

TABLE VIII
THREE-STAGE DRIVER SETUP OF THE TURN-OFF EVENT

Stage S	$R_{\text{g,off}}^{S}$	$\Delta t_{\text{off}}^{S}$
1	0.5 Ω	15.6 ns
2	100 Ω	5 ns … 15 ns
3	4.7 Ω	∞

first stage, a high precision in the timing is required as very little influence (<1 ns) has a high impact on the remaining switching transient of the power semiconductor.

A quantitative comparison of the stress and the switching energy for the turn-on event is plotted in Fig. 15, containing both, the reference as well as the two- and three-stage measurements. It is seen, that using the two-stage operation, the device stress can be influenced over a wide range, however with additional costs in turn-on losses. A good two-stage parameter selection as a basis for the three-stage operation allows a reduction of the stress and of the losses at the same time, compared to the reference driver. A reduction of the diode peak voltage $\hat{U}_{\text{Diode}}$ by 51% as well as a reduction of the reverse recovery peak current $\hat{I}_{\text{S}}$ by 50% is reached for equal turn-on losses E_{on}.

VII. Stage-Wise Driver Turen-Off Operation

Analogously to the turn-on event investigations, the influence of the different stages on the turn-off event is investigated. The impact of the two-stage operation on the switching transients is shown first, followed by an investigation of a third stage.

A. Investigations on the Two-Stage Turn-Off Event

The two-stage analysis is carried out using the driver setup as shown in TABLE VII. The gate is discharged using a high current in the beginning and is slowed down after a certain time $\Delta t_{\text{off}}^{\text{S1}}$ with switching to a higher gate resistance $R_{\text{g,off}}^{\text{S2}}$.

The resulting waveforms are plotted in Fig. 16. The two-stage operation allows a reduction of the drainsource voltage peak $\hat{U}_{\text{DS}}$, however with increased turn-off losses.

B. Investigations on the Three-Stage Turn-Off Event

The influence of a third stage is shown using the setup listed in TABLE VIII. The time $\Delta t_{\text{off}}^{\text{S2}}$ is increased using a 2.5 ns step size. Fig. 17 shows the resulting waveforms. A slight increase of the peak voltage $\hat{U}_{\text{DS}}$ together with a reduction of the turn-off losses is observed. The rate of change of both quantities compared to the two-stage operation decides whether an overall improvement is achieved. It is noticed, that a noticeable effect on the waveforms is seen only a certain time after the gate resistance got changed.

C. Evaluation of the Stage-Wise Turn-Off Operation

It is shown, that an influence on the switching transients is as well possible during the turn-off event. However, certain delays in the reaction of the transient behavior are seen, as for example in the gate voltage waveform plotted in Fig. 16.

The resulting device stress ($\hat{U}_{\text{DS}}$), extracted from the two

[7] Equivalents a single-stage turn-off event using $R_{\text{gate}} = 0.5\ \Omega$.

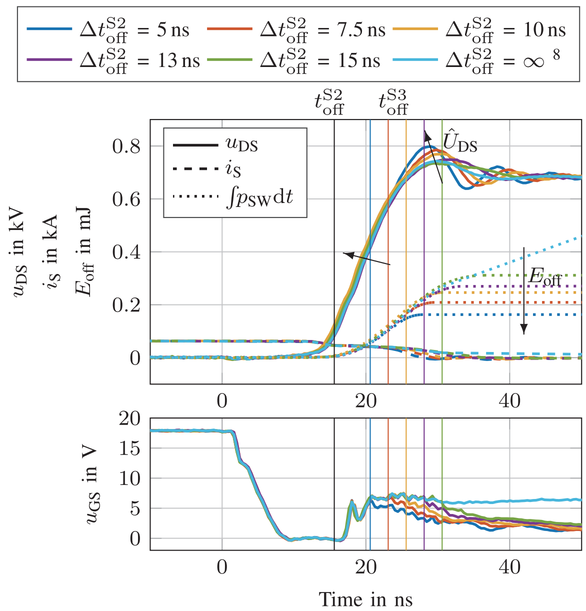


Fig. 17. Three-stage turn-off event waveforms.

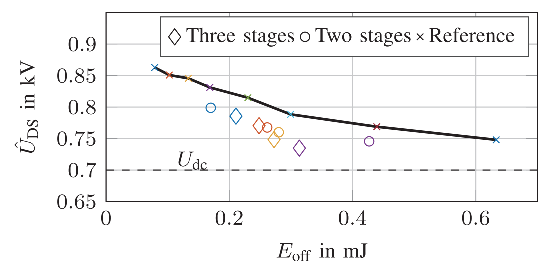


Fig. 18. Low-side switch voltage overshoot vs. turn-off energy.

and three-stage measurements, is plotted against the turn-off energy in Fig. 18. It is seen, that implementing a second stage during the turn-off event gives a better performance of the power semiconductor as all measurement points are found below the reference measurements. The introduction of a third stage shows the possibility of further improvement compared to the two-stage operation.

However, the key statement of the investigation is, that the introduction of an initial fast discharging stage is crucial to achieve improved switching behavior. All together, the drain-source peak voltage $\hat{U}_{DS}$ is reduced by up to 45% while maintaining equal turn-off losses E_{off}.

VIII. Summary of the Switching Behavior

A summary of the switching behavior using the variations of timing and resistances of the different stages is given for both, the turn-on as well as for the turn-off event of the SiC MOSFET. TABLE IX shows the influence of rising gate resistance $R^S_{g,on}$ and rising stage time Δt^S_{on} on the device stress, $\hat{I}_S$ and $\hat{U}_{Diode}$, as well as on the turn-on loss energies $E_{on,Switch}$ and $E_{on,Diode}$. Analogously, the influence of the gate resistances $R^S_{g,off}$ and timings Δt^S_{off} on the transient voltage overshoot $\hat{U}_{DS}$ and turn-off energy E_{off} is tabulated in TABLE X.

[8] Equivalents a two-stage turn-off event changing from $R^{S2}_{g,off} = 0.5\ \Omega$ to $R^{S3}_{g,off} = 100\ \Omega$.

TABLE IX
Summary of the SiC MOSFET Turn-On Behavior

	$\hat{I}_S$	$\hat{U}_{Diode}$	$E_{on,Switch}$	$E_{on,Diode}$	E_{on}	Reference
$R^{S1}_{g,on}\uparrow$	$\searrow$	$\searrow$	$\nearrow$	$\rightarrow$	$\nearrow$	Fig. 12, Fig. 15
$\Delta t^{S1}_{on}\uparrow$	$\nearrow$	$\nearrow$	$\searrow$	$\nearrow$	$\searrow$	Fig. 13
$R^{S2}_{g,on}\uparrow$	$\searrow$	$\searrow$	$\nearrow$	$\searrow$	$\nearrow$	Fig. 13, Fig. 15
$\Delta t^{S2}_{on}\uparrow$	$\searrow$	$\searrow$	$\nearrow$	$\searrow$	$\nearrow$	Fig. 14
$R^{S3}_{g,on}\uparrow$	-	-	$\nearrow$	$\nearrow$	$\nearrow$	

TABLE X
Summary of the SiC MOSFET Turn-Off Behavior

	$\hat{U}_{DS}$	E_{off}	Reference
$R^{S1}_{g,off}\uparrow$	$\searrow$	$\nearrow$	Fig. 12, Fig. 18
$\Delta t^{S1}_{off}\uparrow$	$\nearrow$	$\searrow$	Fig. 16
$R^{S2}_{g,off}\uparrow$	$\searrow$	$\nearrow$	Fig. 18
$\Delta t^{S2}_{off}\uparrow$	$\searrow$	$\nearrow$	Fig. 17
$R^{S3}_{g,off}\uparrow$	-	$\nearrow$	

The mechanism contributing to the performance improvement of the AGD, compared to the reference driver, relies on the modulation of the gate charge during the switching transient. A fast dis-/charging of the gate is envisaged during the switching phase, where the stress on the device is not critical. However, during the critical phases, the gate dis-/charging is reduced and the measurements show, that this results in less stress on the power semiconductor compared to a single-stage gate driver.

IX. Conclusions

In this work, a stage-wise gate driver based on a switched resistor topology for SiC MOSFETs has been presented. A detailed description of the measurement setup as well as the switching loss extraction has been shown as this is crucial to achieve reliable measurement results. The performance of the stage-wise gate driver was evaluated by benchmarking the device stress, resulting from the switching transients, against the switching losses. Furthermore, the evaluation included a comparison to a reference gate driver, based on a standard push-pull stage using various different gate resistances. A detailed analysis of the two- and three-stage operation of the AGD was conducted for the turn-on and the turn-off event.

It has been shown that the drain-source peak voltage $\hat{U}_{DS}$ got reduced by 45% while maintaining equal turn-off losses E_{off}. The turn-on event shows a reduction of 51% of the diode peak voltage $\hat{U}_{Diode}$ and a reduction of 50% of the peak reverse recovery current $\hat{I}_S$ at the same time for equal turn-on losses E_{on}. This allows the utilization of a higher DC-link voltage, resulting in a higher power rating of a given converter with a given power semiconductor. This is crucial to reduce price per kilowatt of future high density power electronic converters.

The mentioned achievements should not be considered as the total potential of the driver as no optimization or search for an optimum point was carried out. Furthermore, it is noticed that a closed loop control of the switching trajectory is hardly achievable due to the large delays and late reaction of the power semiconductor.

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