Continuous-Control-Set Predictive Control and Noise Tolerance Strategy for Phase-Shift Modulation DAB Topological Clusters

Tianqu HAO, Jiazheng HUANG, Zheng DONG, Zhenbin ZHANG, and Qian CHEN

***Abstract*—A continuous-control-set predictive control strategy is proposed for the phase-shift-modulation dual-active-bridge topological cluster. This strategy addresses two critical issues: high sensitivity to model parameters and sampling noise in traditional model predictive control. The steady-state error is analyzed in detail, considering model parameters and modeling methods. We establish a unified and simplified predictive model that is suitable for different dual-active-bridge topologies, reducing dependence on model parameters and computational burden. To mitigate sensitivity to sampling noise, we design a noise tolerance enhancement strategy by redefining a coefficient in the simplified model. This strategy expands the noise tolerance range while maintaining excellent dynamic performance, low system cost, and computational burden. The proposed control strategy is verified by using an experimental platform with TMS320F28379D as the core controller. Results show that our strategy effectively reduces sensitivity to model and noise while ensuring excellent dynamic performance compared to traditional model predictive control. The strategy is universal and significantly reduces the computational burden.**

***Index Terms*—Dual-active-bridge topological cluster, model predictive control, noise tolerance, simplified model.**

I. Introduction

RECENTLY, with the increasing integration of distributed power sources and energy storage devices into the grid, bidirectional isolated DC/DC converters have gained widespread use in DC microgrids, electric vehicles, and photovoltaic power generation [1]–[6]. These converters, such as dual-active-bridge (DAB) converters, dual-bridge-series-resonant converters (DBSRC), CLLC converters, and others, serve as interface devices for bidirectional power flow and have been extensively studied [7]. Among the various modulation strategies for these topologies, phase-shift modulation stands out due to its advantages of a high degree of freedom, fixed switching frequency, and fast dynamic response. These advantages simplify the design of magnetic components and enable multi-dimensional performance optimization, making it particularly suitable for high-power applications [8]–[10].

In modern power systems, energy storage devices operate under uncertain conditions due to the randomness and variability of load operating conditions. To achieve better dynamic performance, DC/DC converters need to be equipped with effective control strategies. Model predictive control (MPC), a nonlinear control strategy, offers advantages such as fast dynamic response, multi-objective control, and easy integration of constraints. Consequently, MPC has found increasing use in power electronics control [11]–[12]. Extensive research has been conducted on the application of MPC in various topologies, including DAB converters [13]–[14], DBSRCs [15]–[16], and CLLC converters [17]. Research results indicate that the steady-state performance under MPC is highly influenced by the accuracy of the predictive model parameters [18]. Additionally, even small sampling noise disturbances can lead to significant fluctuations in control variables [19]. Consequently, the extreme sensitivity to model parameters and sampling noise have emerged as two critical factors limiting the practical application of MPC in engineering.

Parameter identification and predictive model reconstruction are two key approaches to address the issue of high sensitivity to predictive model parameters in MPC strategies. For a multi-DAB-module system, the impact of parameter mismatch on steady-state performance has been analyzed, then an online parameter identification method based on recursive least squares has been proposed [20]. This method successfully eliminates steady-state error in the output voltage caused by parameter mismatch. However, it is limited to specific DAB converters and lacks universality. Also, a model predictive power control (MPPC) strategy has been introduced [21], which relates the control variable solely to the input and output voltage. However, this strategy requires an integrator to correct the output voltage, resulting in a potential degradation of system dynamics. For the three-phase DAB converter, a model-free discrete-control-set predictive control (MFPC) strategy has been proposed [22]. It uses the adaptive forgetting factor recursive least squares method to rectify the predictive model, achieving fast and unbiased control of the output voltage. However, precise

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model is still needed to acquire the output current on the secondary side, and the calculation process is complex, imposing a heavy computational burden on the controller.

To mitigate the challenge of high sensitivity to sampling noise in model predictive control, current research focuses on improving processor performance, incorporating peripheral hardware filters, employing software filters, and reconstructing state space models. Yang [23] analyzed the impact of switching noise, quantization noise, and measurement noise on the control performance of DAB converters. They propose noise suppression methods such as increasing sampling frequency, reducing signal transmission delay, and raising the controller's basic frequency. However, these solutions increase system costs and are not practical for engineering applications. The Kalman Filter algorithm [19] was introduced to enhance the robustness of continuous-control-set model predictive control by utilizing optimal estimated values of state variables instead of measurements, effectively addressing the influence of measurement noise. However, this system still relies on the Kalman Filter for steady-state state variable estimation, requiring significant storage space and computing power. Babayomi [24] combined a hybrid cascaded extended state observer with model-free predictive control to improve interference and noise suppression capability. Nonetheless, compared to the control strategy proposed previously [19], this approach incurs higher computational costs.

In summary, existing work has limitations in addressing the challenges of high sensitivity to model parameters and sampling noise in model predictive control. These shortcomings are as follows:

(i) Traditional parameter identification strategies result in complex predictive models, leading to a significant computational burden.

(ii) Current noise tolerance range improvement strategies struggle to strike a balance between dynamic performance, system cost, and computational burden.

(iii) The predictive models lack the ability to facilitate algorithm transplantation across different topologies.

To address the challenges posed by model parameters and sampling noise in MPC schemes, this article presents a novel continuous-control-set predictive control strategy based on a simplified model. This approach effectively mitigates the control target deviation caused by model parameter mismatch and approximation errors in modeling methods. Moreover, it significantly reduces the computational burden on the controller. Furthermore, the Kalman Filter algorithm is employed to correct the simplified model parameters instead of relying on real-time optimal estimation of sampling values. This integration enhances the accuracy of the model and contributes to improved control performance. In addition, a simple yet efficient noise tolerance range improvement strategy is proposed to reduce the sensitivity to sampling noise in traditional model predictive control. This strategy achieves a balance between a fast dynamic response and a wide noise tolerance range. The proposed control strategy is versatile and applicable to various dual-active-bridge topological clusters.

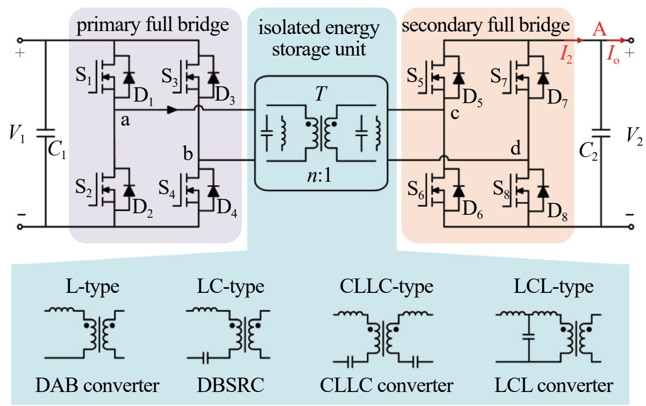

Fig. 1. Variation of cumulative index for islanding detection.

The structure of this paper is as follows. In Section II, the working process of the isolated phase-shift modulation DC/DC converter is analyzed. By considering the DBSRC as an example, the steady-state error of the system is quantified from two perspectives: model parameters and modeling methods. A unified simplified predictive model based on the Kalman Filter algorithm is then established. In Section III, the two-step continuous control set predictive control is employed to obtain the optimal control quantity. Additionally, a noise tolerance range improvement strategy is proposed by redefining the simplified model parameters, ensuring fast dynamic response and reduced computational burden. Section IV presents the experimental results. Finally, Section V concludes the paper.

II. Phase-Shift-Modulation Converters

A. Operating Process

The common phase-shift modulation control technique is utilized in various converters such as DAB converters, DBSRC, CLLC converters, among others. These converters adjust the phase-shift angle of the drive signals between the primary and secondary switches to regulate the phase difference between voltage and current in the energy storage components. This enables bidirectional power flow across a wide voltage gain range. Fig. 1 illustrates the topology cluster of phase-shift modulation converters, comprising two full bridge modules and an isolated energy storage unit. Each full-bridge module consists of four switches (S_1–S_4 and S_5–S_8) and four freewheeling diodes (D_1–D_4 and D_5–D_8). The isolated energy storage unit incorporates a high-frequency transformer with a ratio of n:1 and energy storage elements of different structures. It is important to note that different combinations of energy storage elements form different types of converters. The input-side and output-side filter capacitances are represented by C_1 and C_2, respectively. i_2 denotes the current of the secondary full bridge module, while i_o represents the output current. I_2 and I_o is the average current of the secondary full bridge module and load, respectively, and the equation $I_2 = I_o$ is hold.

Fig. 2 illustrates the operation waveforms of a DBSRC

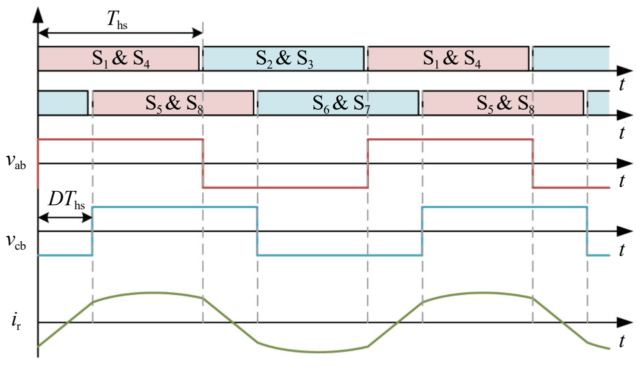

Fig. 2. Operating waveforms of DBSRC.

under single phase-shift modulation. In this analysis, we consider the grouping of switches on the primary or secondary side full bridge, where a group consists of switches such as S_1 and S_4. During the dead time preceding the switch conduction, the paralleled parasitic capacitors of the switches within the corresponding group undergo a charging process. Meanwhile, the complementary switches on the same side undergo a discharging process resulting in the switch terminal voltage reaching zero before opening. This achieves a zero voltage switching (ZVS) condition. In Fig. 2, T_{hs} represents half the switching cycle time, and i_r denotes the current flowing through the resonant inductor. By adjusting the phase-shift duty cycle, denoted as D, the magnitude and direction of power flow can be freely switched, offering flexibility in the operation of the converter.

Applying Kirchhoff's current law to node A shown in Fig. 1, the differentiation of output voltage can be discretized by the forward Euler method as

$$C_2\frac{\mathrm{d}V_2}{\mathrm{d}t}=C_2\frac{V_o(k+1)-V_o(k)}{T_c}=i_2(k)-i_o(k) \tag{1}$$

where T_c denotes the control cycle, which is usually set a few times higher than the switching cycle to reduce the computational burden in fixed-frequency phase-shift modulation converters. Assuming zero loss of the converter, the value of I_2 can be calculated using the ratio of transmitted power to the output voltage.

Using the transmitted power of DBSRC calculated previously [25], the deviation between the actual value and the reference value of output voltage in the k-th moment can be expressed as

$$\Delta V_2(k)=\frac{1}{C_2 f_c}\frac{8nV_1\sin(\pi D_{opt})}{\pi^2 X_{LC}}-\frac{1}{C_2 f_c}I_o \tag{2}$$

where D_{opt} represents the optimal phase-shift duty in the k-th moment under MPC strategy, and X_{LC} represents the impedance of the LC resonant tank.

Substituting the above analysis process into other phase-shift modulation converters, we can obtain the output voltage deviation of different topologies, as shown in Table I. Parameter L, $X_{LC.all}$, and X_{LCL} denote the impedance of the energy storage unit for the DAB converter, the CLLC converter and the LCL converter, respectively. It is worth noticing that the above parameters are the equivalent impedances reflected to the primary side from the secondary side.

TABLE I
OUTPUT VOLTAGE DEVIATION OF DIFFERENT TOPOLOGIES

Topology	Output voltage deviation
DBSRC	$\Delta V_2(k)=\frac{1}{f_c C_2}\frac{8nV_1\sin(\pi D_{opt})}{\pi^2 X_{LC}}-\frac{1}{f_c C_2}I_o$
DAB converter	$\Delta V_2(k)=\frac{1}{f_c C_2}\frac{nV_1 D_{opt}\lvert 1-D_{opt}\rvert}{2f_s L}-\frac{1}{f_c C_2}I_o$
CLLC converter	$\Delta V_2(k)=\frac{1}{f_c C_2}\frac{8nV_1\sin(\pi D_{opt})}{\pi^2 X_{LC.all}}-\frac{1}{f_c C_2}I_o$
LCL Converter	$\Delta V_2(k)=\frac{1}{f_c C_2}\frac{8nV_1\sin(\pi D_{opt})}{\pi^2 X_{LCL}}-\frac{1}{f_c C_2}I_o$

B. Steady-State Error Analysis

In the design process of magnetic components for isolated DC/DC converters, the initial values of the inductance of the transformer and inductors are measured in the specific environment (test frequency: 1 kHz; test current: 0.5 mA; ambient temperature: 25 °C). Due to the long-term operation and the frequent load switching during the converter operation, problems such as high coil current, uncertain switching frequency, and heating of the magnetic core may occur, resulting in a significant difference between the inductance coefficient A_L of the magnetic core and the design reference value. This can cause the magnetic components of the converter to deviate from the initial measurement value during the actual operation, making it difficult to operate stably at the pre-designed working point. Meanwhile, due to factors such as modeling methods, switch losses, and dead time of complementary switch driving signals, the model accuracy can be affected and the transmission power of the converter under model predictive control cannot accurately track the given value, even if there is no measurement bias in magnetic components.

Taking DBSRC as an example, we assume that the actual value of the resonant tank impedence and the output filter capacitor are X_{LC} and C_2, while the substitution values of both in the predictive model are X_{LC}' and C_2'. Ignoring modeling error temporarily, the output voltage reaches V_2 in the steady state, i.e.,

$$V_2(k+1)=\frac{8n\sin(\pi D)}{\pi^2 C_2 f_c X_{LC}}V_1-\frac{I_o}{C_2 f_c}+V_2(k)=V_2 \tag{3}$$

Parameters X_{LC}' and C_2' are introduced into the predictive model when the MPC algorithm operates in a digital signal processor. The optimal phase-shift duty cycle in the next moment should be set to keep the predicted output voltage equal to the given voltage V_2^*. Thus, we get

$$\frac{8n\sin(\pi D)}{\pi^2 C_2' f_c X_{LC}'}V_1-\frac{I_o}{C_2' f_c}+V_2(k)=V_2^* \tag{4}$$

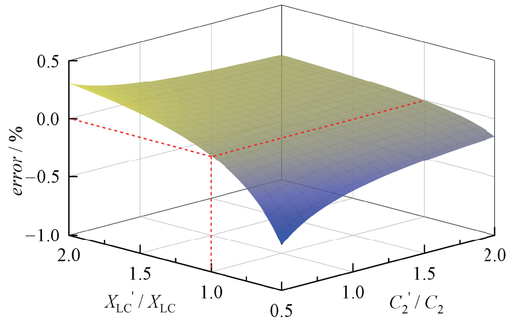

Fig. 3. Output voltage deviation caused by model parameter variations.

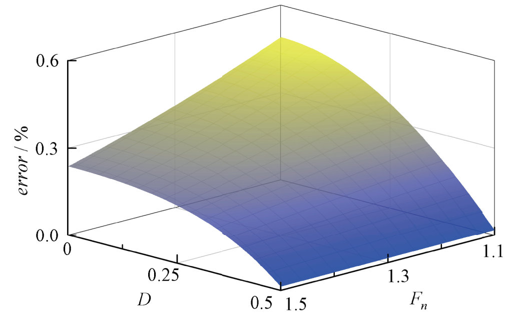

Fig. 4. Output voltage deviation caused by modeling method.

The output voltage remains unchanged in the steady state, which means that $V_2(k+1)$ is equal to $V_2(k)$. Combining (3) and (4) gives

$$\frac{V_2}{V_2^*}=\frac{1}{2}\left(\sqrt{1-\frac{X_{LC}-X'_{LC}}{X_{LC}}\frac{4P}{V_2^{*2}C'_2 f_c}}+1\right) \tag{5}$$

where P is the transmitted power of DBSRC. It can be seen from (5) that the output voltage deviation increases as the transmitted power rises gradually.

In order to further explore the impact of model parameters, a surface graph is presented to show the influence of the resonant tank impedance and output side capacitance on the output voltage under the same transmitted power, which is shown in Fig. 3 with the output voltage error expressed as *error* = (V_2 − V_2*) / V_2* × 100%.

It can be concluded from Fig. 3 that: (i) the deviation of the output voltage is always zero as long as the resonant tank impedance is accurate (see the red dotted line in Fig. 3); (ii) the inductance mismatch affects the voltage deviation regardless of the accuracy of the capacitance value; (iii) as the capacitance ratio of the model value to the actual value increases, the voltage deviation shows lower sensitivity to the inductance mismatch.

Besides the impact of mismatch of the model parameters on the output voltage, the transmitted power deviation caused by modeling methods also makes it hard for the output voltage to track its given value. Ignoring parameter error temporarily, the output current I_2 from time-domain analysis (TDA) can be expressed as [26]

$$\begin{cases} I_2=\dfrac{2n\left(F_n^2-1\right)V_1}{\pi X_{LC}}g(D) \\ g(D)=\dfrac{\cos\left(\pi D/F_n-\pi/2F_n\right)-\cos\left(\pi/2F_n\right)}{\cos\left(\pi/2F_n\right)} \end{cases} \tag{6}$$

where F_n is the resonant ratio given by f_s / f_r. The resonant frequency f_r can be obtained from the resonant inductance L_r and capacitance C_r.

We assume that the inductance and capacitance are accurate to neglect the influence of model parameters mismatch. The predicted phase-shift duty cycle satisfies that the voltage in the next moment is equal to the given voltage V_2* under fundamental harmonic analysis (FHA) while the actual voltage is V_2, then we can obtain

$$\frac{8n\sin(\pi D)}{\pi^2 C_2 f_c X_{LC}}V_1-\frac{I_o}{C_2 f_c}+V_2=V_2^* \tag{7}$$

Combining (7) and (8) yields

$$\begin{cases} \dfrac{V_2}{V_2^*}=1-h\left[\dfrac{4n\sin(\pi D)}{\pi^2}-(F_n^2-1)g(D)\right] \\ h=\dfrac{2nV_1}{V_2^* C_2 f_c X_{LC}} \end{cases} \tag{8}$$

Fig. 4 shows the influence of the FHA method on the output voltage. Compared to the precise modeling based on power balance using the TDA method, it can be concluded that: (i) as the phase-shift duty cycle decreases, the voltage deviation is more susceptible to the resonant ratio; (ii) as the resonant ratio decreases, the voltage deviation is more susceptible to the phase-shift duty cycle; (iii) the output voltage steady-state error caused by FHA modeling method always exists.

According to the above analysis, we observe that: (i) the voltage deviation caused by the modeling method can be eliminated by utilizing the TDA method based on a precise power balance equation; (ii) the voltage deviation caused by both model parameters and modeling methods can be eliminated simultaneously by parameter identification. However, the computational burden is relatively high due to the predictive model.

Apart from DBSRC, other types of converters also suffer from transmitted power deviation caused by the mismatch of model parameters and modeling methods, and the above conclusions still hold.

C. Simplified Model

For the various dual-active-bridge topologies, as shown in Fig. 1, the relationship between transmitted power and control quantity is different. Therefore, a unified predictive model cannot be constructed to meet the engineering requirements in various scenarios. Based on the analysis of the factors affecting the voltage deviation given in Section II.*B*, we propose here a unified simplified model that is suitable for the phase-shift modulation topology cluster, and the Kalman Filter algorithm is introduced to solve the correlation coefficients of the simplified model iteratively to achieve fast and unbiased control.

The deviation between the actual output voltage and the given value depends on the phase-shift duty cycle D and the output current I_o. When the average current on the secondary side I_2 determined by D is equal to the output current I_o, the output voltage reaches the given value, i.e., ΔV_2 is zero. According to Table I, it can be seen that in the output voltage deviation models of different topologies, only the relevant term of D are distinct, while the coefficients of I_o are the same, all of which are $1 / C_2 f_c$. Considering the simplicity of calculation and the universality of the predictive model, the relevant term of D in the output voltage deviation can be simplified as a linear term. Therefore, in Table I, the output voltage deviation in discrete time can be simplified as

$$\begin{cases} \Delta V_2(k) = G(k) \cdot D(k) - \dfrac{1}{C_2 f_c} I_o \\ \Delta V_2(k) = V_2(k+1) - V_2(k) \end{cases} \tag{9}$$

where $I_o(k)$ is the sampling value of the output current at the k-th moment, and $D(k)$ is the calculated value of the phase-shift duty cycle at the k-th moment. Parameter $G(k)$ represents the control gain, which is related to the actual operating condition of the converter at the current moment.

Generally, the voltage deviation of the resonant DC/DC converter topology is affected by many factors and has significant nonlinear effects. If a linear simplified model with a fixed control gain is used to replace the complex nonlinear model which ignores the circuit parasitic parameters, the output voltage is difficult to track the reference value quickly and accurately due to parasitic parameters, model accuracy, operating power, and other factors under a fixed control gain. The magnitude of $G(k)$ has a crucial impact on the control accuracy of the converter. Therefore, to eliminate the output voltage steady-state error, it is necessary to choose an appropriate $G(k)$ according to specific operating conditions.

The parameter identification algorithm can eliminate the steady-state errors caused by circuit parameter variations and modeling methods simultaneously. Therefore, in order to correct the control gain in real time when ΔV_2 is equal to zero under different loads, we introduce the Kalman filtering algorithm to estimate $G(k)$ accurately. Expressing (9) in matrix form, the state predictive equation of the linear discrete system can be obtained as

$$y(k) = X(k)^T H(k) \tag{10}$$

where

$$\begin{cases} y(k) = \Delta V_2(k) \\ X(k) = \left[G(k) \ -1/C_2 f_c\right]^T \\ H(k) = \left[D(k) \ i_o(k)\right]^T \end{cases} \tag{11}$$

According to (9)–(11), the linear simplified model based on the Kalman Filter is established as

$$\begin{cases} X(k) = X(k-1) + K(k)\left[y(k) - X(k-1)^T H(k)\right] \\ K(k) = \dfrac{P(k-1)H(k)}{R + H(k)^T P(k-1) H(k)} \\ P(k) = \left[I - K(k)H(k)^T\right] \cdot P(k-1) + Q \end{cases} \tag{12}$$

where $P(k)$ is the covariance matrix of the estimation error at the k-th moment and K is the Kalman gain. R and Q represent the covariance matrices of measurement noise and process noise, respectively. It is worth mentioning that the convergence rate of the Kalman Filter is affected by the Kalman gain, in the range of 0 to $1 / H$. When K is close to 0, the optimal state estimation relies more on the state estimation at the last moment. When K is close to $1 / H$, the optimal state estimation relies more on the measurement value at this moment.

In (12), the parameter $y(k)$, which is equal to ΔV_2, can be measured directly. $H(k)$, $X(k-1)$, and $P(k-1)$ can be obtained from the values at the last moment. $X(k)$, $P(k)$, and $K(k)$ are the variables to be solved later, which can be obtained from (12). The offset-free model predictive control will be achieved by iterative correction of the control gain $G(k)$. Due to the fact that only the variable $G(k)$ in the first line of $X(k)$ is unknown, the process of optimization estimation of $X(k)$ can be simplified, thus alleviating the computational burden in the controller.

III. Continuous-Control-Set Predictive Control Using Simplified Model

A. Solution to Predicted Phase-Shift Duty Cycle

The model predictive control algorithm generally includes three segments: predictive model, rolling optimization, and feedback correction. The control sequence is continuously optimized to achieve fast dynamic response through updating the system state in real-time, solving the open-loop optimization issue online, and repeating the above processes at the next moment. The state-space averaging model of the converter can be used in the predictive model. According to (9), the discretized output voltage of the phase-shift modulation converter can be obtained as

$$V_2(k+1) = G(k) \cdot D(k) - \frac{i_o(k)}{C_2 f_c} + V_2(k) \tag{13}$$

In single-step model predictive control, the controller aims to ensure that the output voltage at the next moment reaches its given value as soon as possible and solves the optimal phase-shift duty cycle within this control cycle. The system's operating process is shown in Fig. 5(a). The output voltage before the k-th moment deviates significantly from the given value, and the converter operates at maximum power with the phase-shift duty cycle being 0.5. The sampling value of the output voltage at the k-th moment is $V_{2.\mathrm{cal}}(k)$. In order to achieve the output voltage of V_2* at the $(k+1)$-th moment, the controller calculates the optimal operating trajectory and obtains the predicted

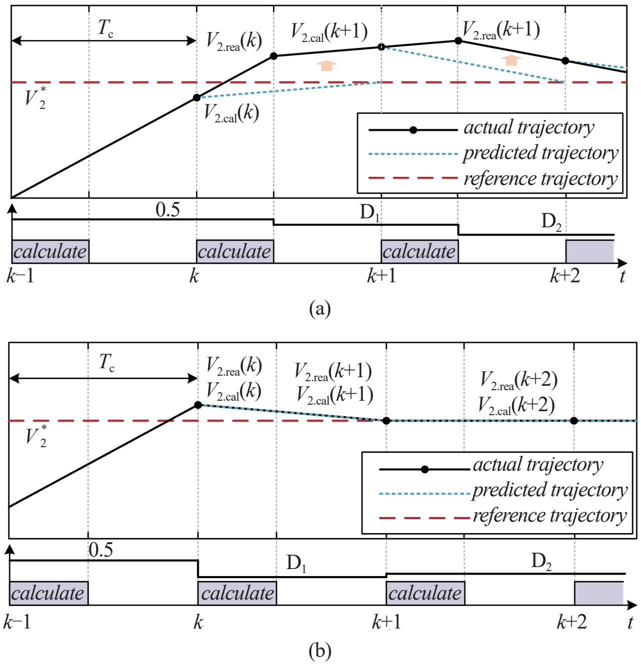

Fig. 5. Schematic diagram of system operation process under different MPC strategies. (a) Single-step model predictive control. (b) Two-step model predictive control.

phase-shift duty cycle of D_1. Considering the calculation time of the controller, the output voltage has risen to $V_{2.rea}(k)$ at the time of updating the phase-shift duty cycle. Thus, the output voltage cannot reach V_2^* at the $(k+1)$-th moment. Similarly, the optimal phase-shift duty cycle D_2 calculated by $V_{2.cal}(k+1)$ at the $(k+1)$-th moment is updated when the output voltage is $V_{2.rea}(k+1)$. Thus, it still cannot satisfy the condition that $V_{2.cal}(k+2) = V_2^*$. Under the single-step model predictive control, the actual output voltage gradually approaches its given value over time. However, the calculation speed is limited due to the cost of the controller. Since the controller's calculation time is non-negligible, the output voltage cannot move along the predicted trajectory, and the dynamic performance of the system deteriorates.

To solve the problem of calculation delay, we adopt a two-step model predictive control to compute the optimal phase-shift duty cycle. According to (9), the output voltage deviation at the $(k+1)$-th moment can be obtained as:

$$\Delta V_2(k+1) = G(k+1)\cdot D(k+1) - \frac{1}{C_2 f_c} i_o(k+1) \tag{14}$$

Combining (13) and (14), the predicted output voltage value at the $(k+2)$-th moment is

$$\begin{aligned} V_2(k+2) = {} & G(k+1)\cdot D(k+1) - \frac{1}{C_2 f_c} i_o(k+1) + \\ & G(k)\cdot D(k) - \frac{1}{C_2 f_c} I_o(k) + V_2(k) \end{aligned} \tag{15}$$

The implementation process of the predictive control with a simplified model (SMPC) proposed in this paper is as follows:

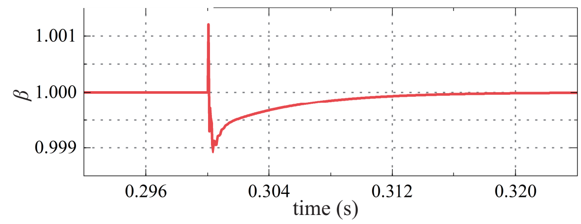

Fig. 6. Simulation of β when the load changes.

The controller calculates the optimal phase-shift duty cycle D_1 at the k-th moment, and updates it at the $(k+1)$-th moment. At the same time, the optimal phase-shift duty cycle D_2 at the $(k+2)$-th moment is calculated. The calculation process is shown in Fig. 5(b). This two-step predictive control algorithm predicts the optimal phase-shift duty cycle for the next time step at the current moment and updates it at the beginning of the next control cycle to ensure that the output voltage at the next step reaches the reference value as quickly as possible.

In (15), V_2 and I_o can be measured. $D(k)$ is the optimal phase-shift duty cycle obtained at the last step, and $G(k)$ can be obtained from (12). The change of load current is small within one control cycle, i.e., $I_o(k+1) = I_o(k)$. The variable $G(k+1)$ cannot be measured directly, but its magnitude can be obtained by fitting the historical data. To reduce the computational burden, we only consider the term related to the control gain at the last moment, i.e.,

$$G(k+1) = \beta(k)\cdot G(k) \tag{16}$$

where $\beta(k)$ is the fitting coefficient. Regarding (16) as the state predictive equation for discrete systems, the one-dimensional data-driven model based on Kalman Filter is established as

$$\begin{cases} \beta(k) = \beta(k-1) + K_\beta(k)\left[G(k) - \beta(k-1)G(k-1)\right] \\ K_\beta(k) = \dfrac{P_\beta(k-1)G(k-1)}{R_\beta + G(k-1)^2 P_\beta(k-1)} \\ P(k) = \left[1 - K_\beta(k)G(k-1)\right]\cdot P_\beta(k-1) + Q_\beta \end{cases} \tag{17}$$

By solving the optimal estimation of the Kalman gain K_β, the prediction of $G(k+1)$ can be achieved.

When the converter reaches the steady state, the control gain G no longer changes, at the operating point of $G(k+1) = G(k)$. When a sudden change in load from 50% to 100% causes the system to break away from the steady state, the simulation of the change process of the fitting coefficient β is shown in Fig. 6. It can be seen that the change of β is extremely small during the harsh transient process. As the estimation process of β will increase the computational burden of the controller, $G(k)$ can be approximated as $G(k+1)$ in practice, which further simplifies the predictive model while ensuring dynamic performance.

B. Improvement of Noise Tolerance

When the measurement value of output voltage fluctuates due to sampling noise or low bit count of the controller's A/

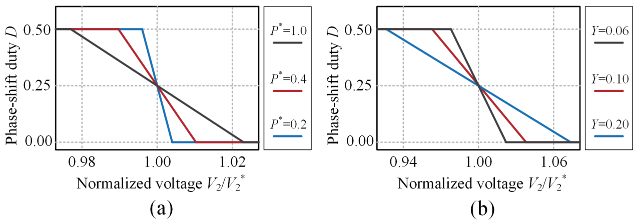

Fig. 7. Relation between phase-shift duty cycle and normalized output voltage. (a) Under different power levels. (b) Under different values of noise tolerance coefficient.

D converter, the measurement noise will be fed back to the predictive model, resulting in the change of the phase-shift duty cycle accordingly. When the system operates in the steady state, the measurement noise of the output voltage is δV_2, and the resulting phase-shift duty cycle change is δD. According to (9), it can be obtained as

$$D+\delta D=\frac{1}{GC_2 f_c}\left(I_o+C_2 f_c \delta V_2\right) \tag{18}$$

In practical circuit, the output filter capacitor C_2 is designed as hundreds of microfarad and the control frequency f_c is usually set in tens of kilohertz. According to (18), a tiny voltage fluctuation can cause D to jump between 0 and 0.5. When D jumps to a larger value, the device current of the switches increases significantly, resulting in increased switching loss. The energy storage unit needs to withstand higher voltage and current stresses and it accelerates device aging. When D jumps to a smaller value, the primary and secondary side switches cannot all achieve ZVS under non-unit voltage gain, resulting in reduced system efficiency. When the phase-shift duty cycle fluctuates between 0 and 0.5, the output voltage noise increases, which is not conducive to the stable operation of the voltage-sensitive loads.

Assuming that the steady-state phase-shift duty cycle of the converter is 0.25, the relationship between normalized output voltage V_2 / V_2* and phase-shift duty cycle D can be plotted according to (18), as shown in Fig. 7. When the output voltage deviates from the reference voltage, the converter will transmit power at its maximum capacity (D = 0.5 or 0) to achieve fast response. When the output voltage approaches the reference value, the phase-shift duty cycle will vary linearly with the output voltage deviation. However, due to the extremely small linear region, a slight fluctuation in the output voltage sampling value can lead to a significant change in the phase-shift duty cycle. Meanwhile, the linear region gradually becomes narrow as the transmitted power of the converter decreases. Therefore, the key to achieving stable operation of the converter is to reduce the sensitivity of D to high-frequency noise.

We define the noise tolerance coefficient as Y, i.e.,

$$Y=\frac{1}{C_2 f_c} \tag{19}$$

Substituting (19) into (9), the output voltage deviation can be expressed as

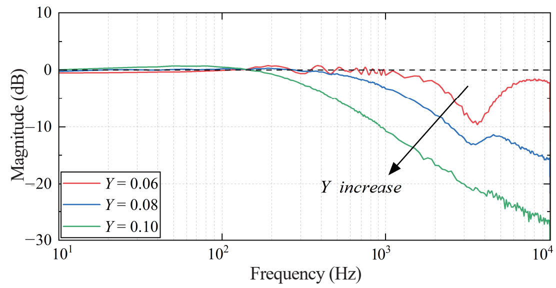

Fig. 8. Amplitude-frequency curves under different values of noise tolerance coefficient.

$$\Delta V_2=G\cdot D-Y\cdot I_o \tag{20}$$

When the system reaches the steady state, the phase-shift duty cycle is

$$D=\frac{Y}{G}\cdot I_o \tag{21}$$

The correction of the control gain G ensures that the output voltage deviation is zero. Thus, the Kalman Filter algorithm can always obtain an optimal estimation of G to satisfy $V_2(k+2)$ = V_2* for different Y values. The operating condition of the system remains unchanged under the same transmitted power and different values of the noise tolerance coefficient. Hence, the value of G increases or decreases proportionally with the change in the noise tolerance coefficient. According to (18), the phase-shift duty cycle can tolerate larger output voltage fluctuations in the linear region as the increment of G. Fig. 7(b) shows the relationship between the normalized output voltage and the phase-shift duty cycle for different values of noise tolerance coefficient when the normalized transmitted power is 1. It can be observed that the linear region becomes wide as the value of Y increases, which means that the sensitivity of D to δV_2 decreases, and a higher tolerance of the system for high-frequency sampling noise is achieved.

AC sweepings based on PLECS are carried out for the steady-state point V_1 = 100 V, V_2 = 100 V, and R_L = 20 Ω. Perturbations from 10 Hz to 10 kHz with amplitude of 0.01 V are superposed on the output voltage steady-state value V_2 = 100 V. The closed-loop transfer function for DBSRC can be defined as

$$G_v(f)=\frac{V_2(f)}{v_2^*(f)} \tag{22}$$

where v_2* is the injected perturbation of the reference output voltage. The sweeping results are presented in Fig. 8, showing the closed-loop transfer function in the frequency domain with different values of Y. The noise tolerance coefficient has a negative impact on the system bandwidth. As the value of Y increases, it moves the pole to a lower frequency and the theoretical dynamic response time of the system slows down. Thus, it is not advisable to take a too large value of Y.

The selection process of Y is as follows: Firstly, we should estimate the noise level. The content of quantization noise and measurement noise is higher, so we use the sum of them to ap-

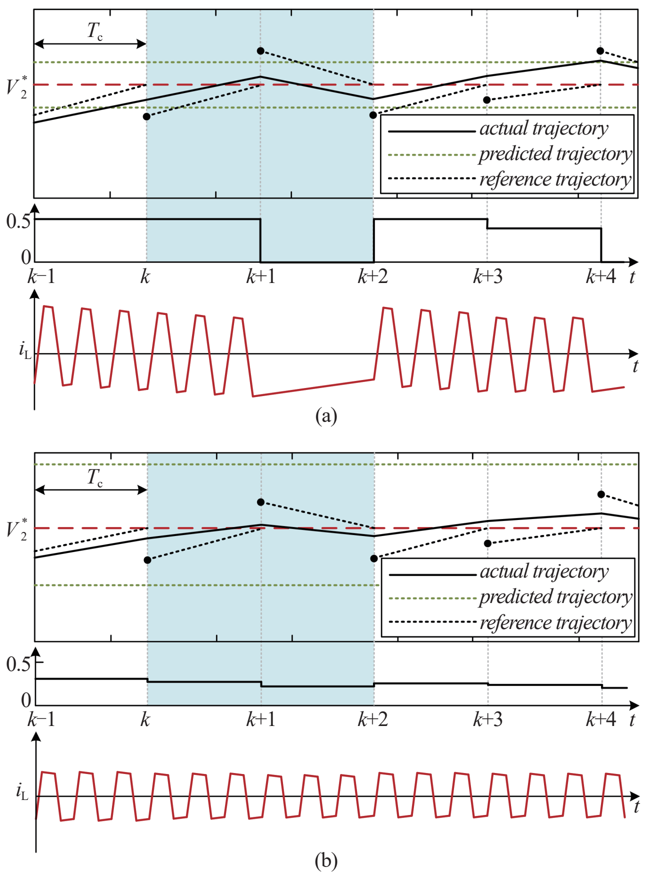

Fig. 9. Schematic diagram of system operation process under different Y. (a) Without noise tolerance strategy. (b)With noise tolerance strategy.

proximate the sampling noise:

$$\begin{aligned}\Delta &= \Delta_{\max}^{q} + \Delta_{\max}^{m} \\ &= \frac{V_{\mathrm{REF}} \cdot V_{\max}}{2^{n+1}} + V_{\mathrm{OS}} \times \frac{V_{\max}}{V_{\mathrm{REF}}}\end{aligned} \tag{23}$$

where the bit of ADC is n, with the maximum input voltage V_{REF}, and $V_{\max}$ is the full scale. V_{OS} is the input offset voltage.

Then, we need to set a suitable Y to ensure δD fluctuates in a small range. According to (18) and (21) :

$$Y_{\min} = \frac{D \cdot \Delta}{I_o \cdot \delta D} \tag{24}$$

where D is the steady-state phase-shift duty cycle, and I_o is the steady-state output current. Obviously, the larger the Y is, the smaller degree the δD fluctuates in. We limit the value of δD to 0.1 generally.

Besides, when the converter output power at maximum capacity (D = 0.5), $\Delta V_{2.\mathrm{m}}$ should be small enough to ensure the fast response in one control cycle

$$Y_{\max} = \frac{D}{0.5 \cdot I_o} \Delta V_{2.\mathrm{m}} \tag{25}$$

where $\Delta V_{2.\mathrm{m}}$ is the minimum value of the voltage error which makes D reach 0.5. The boundary of $\Delta V_{2.\mathrm{m}}$ can be set to 5 V.

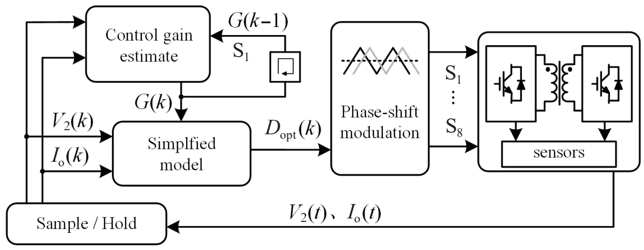

Fig. 10. Block diagram of SMPC.

Finally, we get the range of Y. It is noted that the value of Y should be as close as possible to its maximum value to ensure the priority of noise tolerance.

Fig. 9 is the schematic diagrams of system operation process under different Y, which can further explain the simulation results. It is noted that the switching frequency is three times more than the control frequency. Fig. 9(a) shows the system operation process under $Y = 1 / C_2 f_c$, without the noise tolerance strategy, and Fig. 9(b) means that the converter operates under a higher coefficient Y. The black dots are the measurement values which are affected by the sampling noise. The area between green dashed lines represents the maximum voltage range. When the sampling point exceeds the maximum voltage range, the converter will transfer power at its maximum capacity and the phase-shift duty cycle will reach its boundary value. As the increase of Y, the maximum voltage range become larger, and the phase-shift duty cycle is more difficult to reach its boundary value. Taking the blue area as an example, the control variable with noise tolerance strategy is smoother than that which satisfies $Y = 1 / C_2 f_c$. In addition, the inductor current is not symmetric in Fig. 9(a), which indicates that the transformer is faced with DC bias and saturate easily. However, the introduction of Y means that the actual voltage trajectory can not follow the predicted trajectory, and the dynamic response become slower. Therefore, the coefficient Y can be regarded as a weight coefficient to balance the dynamic response and robustness of the converter.

Fig. 10 shows the block diagram of the continuous-control-set predictive control based on the simplified model proposed in this article. Firstly, the output voltage V_2 and output current I_o are sampled, and the control gain $G(k)$ can be calculated by the optimal phase-shift duty cycle $D_{\mathrm{opt}}(k)$ at the current moment, as shown in (12). Then, $G(k)$ is substituted into the simplified model shown in (15), and the optimal phase-shift duty cycle $D_{\mathrm{opt}}(k+1)$ at the next moment is obtained. It is worth noting that $D(k+1)$ in (15) can be replaced by $D_{\mathrm{opt}}(k+1)$. Finally, the phase-shift duty cycle is updated at the beginning of the next control cycle, and the corresponding triggering signals are generated by the phase-shift modulator to regulate the switches.

IV. Experimental Validation

To verify the effectiveness of the proposed continuous-control-set predictive control strategy based on a simplified model, an experimental prototype is constructed, as shown in Fig. 11.

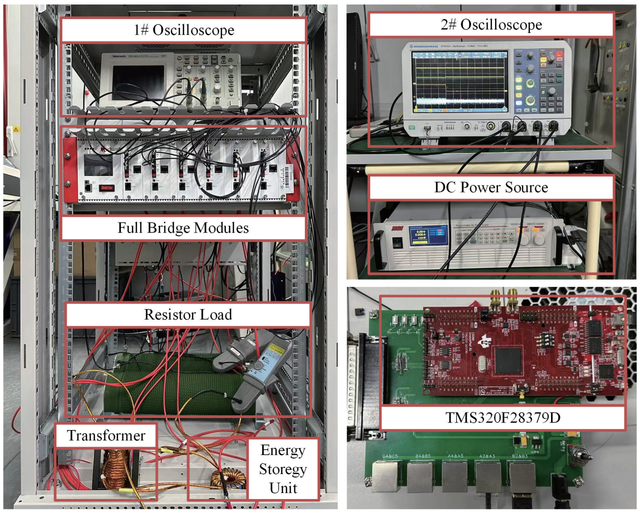

Fig. 11. Experimental prototype.

TABLE II
PARAMETERS OF EXPERIMENTAL PROTOTYPE

Topology	Parameter	Values
General parameter	Input DC voltage (V_1)	100 V
	Output DC voltage (V_2)	100 V
	Transformer turn ratio (n)	1:1
	Output filter capacitor (C_2)	1640 μF
	Load resistor (R_L)	20/40 Ω
DBSRC	Switching frequency ($f_{s,1}$)	40 kHz
	Resonant capacitor (C_r)	1.037 μF
	Resonant inductor (L_r)	44.29 μH
DAB converter	Switching frequency ($f_{s,2}$)	25 kHz
	Series inductor (L_s)	44.29 μH

The experimental platform contains several RT-Unit full-bridge modules with TMS320F28379D controller. By changing the structure of the energy storage unit and the switching frequency, the universality of the proposed control strategy is verified for two topologies of DAB converter and DBSRC. The parameters of the experimental prototype are shown in Table II.

A. Dynamic Performance Comparison

With the load abruptly changing from 40 Ω to 20 Ω, Figs. 12 (a)(c)(e) are the operation waveforms of the DAB converter under PI control, TMPC, and SMPC, respectively. Figs. 12(b) (d)(f) are the operating waveforms of DBSRC under PI control, TMPC and SMPC, respectively. The results show that the recovery time and the voltage overshoot are the worst under PI control regardless of DAB converter (about 66 ms) or DBSRC (about 75 ms) among above three control schemes. However, for TMPC and SMPC schemes, both of them show excellent dynamic performance and the output voltage almost remains

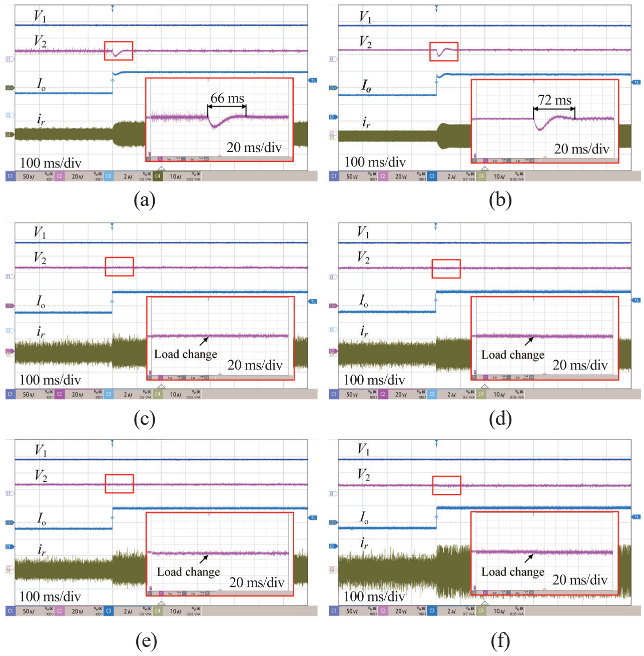

Fig. 12. Dynamic performance comparison when load increases suddenly. (a) DAB converter, PI control. (b) DBSRC, PI control. (c) DAB converter, TMPC. (d) DBSRC, TMPC. (e) DAB converter, SMPC. (f) DBSRC, SMPC. (V_1: 50 V/div; V_2: 20 V/div; I_o: 2 A/div; i_r: 10 A/div; time: 100 ms/div).

unchanged regardless of DAB converter or DBSRC. It can be observed that with the introduction of Kalman filter, the proposed SMPC scheme still maintains excellent dynamic performance as the TMPC scheme does. All two MPC schemes demonstrate faster response than the PI control scheme.

B. Parameter Sensitivity Suppression

The reference voltage is set to 100 V and the load resistance has a constant value of 20 Ω. Fig. 3 and Fig. 4 indicate that both the mismatch of model parameters and modeling method affect the accuracy of the control target. We set an operation condition of 50% mismatch both on the energy storage components impedance and the output side capacitance under the TMPC scheme, while the predictive model of the SMPC scheme is estimated by the Kalman Filter algorithm. The voltage sensors are calibrated under PI control to eliminate the output voltage deviation caused by measurement errors.

Figs. 13(a) and (b) are the operating waveforms under the TMPC scheme, while Figs. 13(c) and (d) are the operating waveforms under the SMPC scheme. The glitches of the output voltage is caused by the switching action, and we avoid setting he sampling points at the switching moment to reduce the interference of switching noise. It can be seen that the voltage deviation always exists under the TMPC scheme regardless of the DAB converter (about 0.75 V) or DBSRC (about 0.92 V). By comparison, the proposed SMPC scheme demonstrates extremely high control accuracy for both topologies. The experiment results prove that the proposed control strategy can effectively reduce the sensitivity of the output voltage to the predictive model.

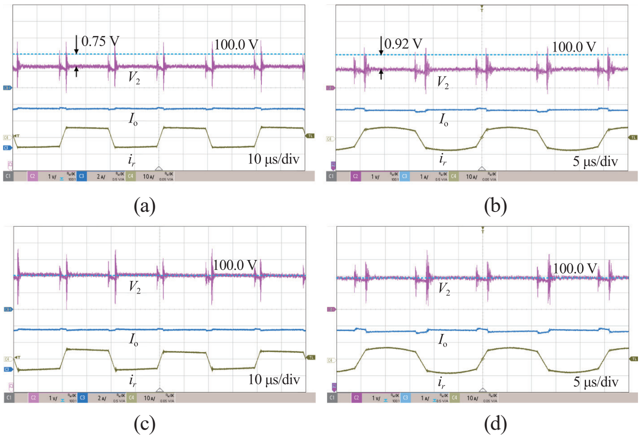

Fig. 13. Steady-state performance comparison under two different MPC strategies. (a) DAB converter, TMPC. (b) DBSRC, TMPC. (c) DAB converter, SMPC. (d) DBSRC, SMPC. (V_2: 1 V/div; I_o: 2 A/div; i_r: 10 A/div).

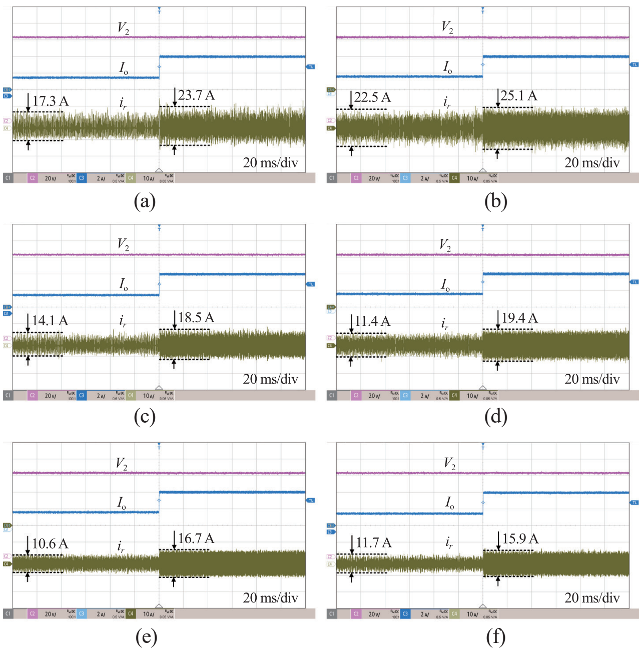

Fig. 14. Current stress comparison under different noise tolerance coefficients. (a) DAB converter, $Y = 0.03$. (b) DBSRC, $Y = 0.03$. (c) DAB converter, $Y = 0.06$. (d) DBSRC, $Y = 0.06$. (e) DAB converter, $Y = 0.12$. (f) DBSRC, $Y = 0.12$. (V_2: 20 V/div; I_o: 2 A/div; i_r: 10 A/div; time: 20 ms/div).

C. Noise Sensitivity Suppression

According to the above analysis, the narrow noise tolerance range causes the large steady-state phase-shift duty cycle to fluctuate and leads to high current stress on the energy storage unit. Therefore, the magnitude of the current stress can reflect the noise tolerance capability of the system.

In the experiment platform, the controller TMS320F28379D has a 12-bit ADC module and the full scale is 3 V, thus the quantizer's least significant bit is

$$LSB = \frac{3}{2^{12}} = 0.732 \text{ mV} \tag{26}$$

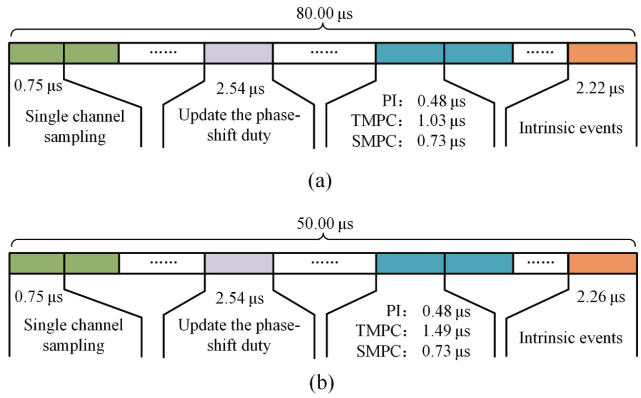

Fig. 15. Running time of different stages in one cycle. (a) DAB converter; (b) DBSRC.

When the rating sampling voltage is 400 V, the maximum quantization noise is

$$\Delta_{\max}^{q} = \frac{1}{2} \times LSB \times 400 = 0.146 \text{ V} \tag{27}$$

According to the datasheet of the voltage sensor chip AMC1311B, the input offset voltage V_{OS} =1.5 mV, thus the measurement noise can reach

$$\Delta_{\max}^{m} = 1.5 \text{ mV} \times \frac{400}{3} = 0.2 \text{ V} \tag{28}$$

Besides, the temperature drift of AMC1311 is 20 µV/°C, which is effected by the chip temperature. However, the thermal noise is much smaller than the quantization noise and the measurement noise, so it can be ignored in the experiment.

Setting the load resistance from 40 Ω to 20 Ω, our experiments are conducted under the proposed SMPC scheme for different values of the noise tolerance coefficient. Fig. 14 shows the operating waveforms of the DAB converter (see Figs. 14 (a), (c) and (e)) and DBSRC (see Figs. 14 (b), (d) and (f)) with the noise tolerance coefficient value Y being 0.03, 0.06, and 0.12. It can be seen that the resonant current decreases by 32.4 % when the noise tolerance coefficient increases from 0.03 to 0.12 at the power of 250 W for the DAB converter, and the resonant current decreases by 32.9% at the power of 500 W under the same condition. The inductor current decreases by 52.9% when the noise tolerance coefficient increases from 0.03 to 0.12 at the power of 250 W for DBSRC, and the inductor current decreases by 33.5% at the power of 500 W under the same condition. Obviously, the proposed SMPC scheme can significantly improve the noise tolerance capability and reduce the current stress of energy storage unit without weakening the dynamic performance, which means smaller switching turn off current and higher system efficiency.

D. Comparison of Running Time

Figs. 15(a) and (b) show the running time of different stages in one control cycle for DAB converter and DBSRC. Compared to the TMPC scheme, the computational time of the DAB converter and DBSRC under SMPC have reduced by 29% and 51%, respectively, and the control target deviation is eliminated completely. Meanwhile, the proposed strategy requires fewer sensors (no input voltage sensor), which implies that the running time can be further reduced. Although the running time under SMPC is longer than PI control, it has much better dynamic performance with the same sensors.

V. Conclusion

This paper proposes a continuous-control-set model predictive control strategy based on a simplified model that is suitable for different dual-active-bridge topologies under phase-shift modulation. The proposed strategy effectively solves the problem of the high sensitivity of the model predictive control to both model parameters and sampling noise with a high level of portability. Compared to the traditional model predictive control, the proposed control strategy does not result in steady-state error caused by model parameter variations and modeling methods. By regulating the noise tolerance coefficient of the simplified model, the system's noise tolerance range is significantly widened, while the converters can still maintain excellent dynamic performance, and the computational burden of the controller is significantly reduced. Experimental results verify the effectiveness of the proposed control strategy.

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