A Novel Space Vector Modulation Scheme for Common-Mode Voltage Reduction in the Hybrid Active Neutral-Point-Clamped Three-Level Inverter with Balanced and Unbalanced DC-Links

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***Abstract*—The hybrid active neutral-point-clamped (HANPC) three-level inverter (TLI) requires much less SiC MOSFETs than a full-SiC ANPC TLI while providing comparable power density. Therefore, the HANPC TLI is an ideal solution for balancing performance and cost. However, excessive common-mode voltage (CMV) amplitudes are observed in conventional modulation methods, especially under unbalanced DC-links. This paper presents a CMV reduction method for the HANPC TLI with balanced and unbalanced DC-links. The scheme employs real-time sampling of photovoltaic array voltages on the DC side, followed by dynamic updates to the space vector diagram (SVD). Due to its inherent advantage of low CMV, zero vector and medium vectors are selected for reference vector synthesis. According to the position of the medium vectors in the updated SVD, the duty cycles are recalculated to ensure the output current quality. Furthermore, switching sequences are optimized through five-segment symmetrical patterning, ensuring minimal switching actions in power devices. Theoretical analysis demonstrates that this modulation method effectively reduces both the magnitude and root-mean-square (RMS) value of CMV while ensuring that SiC MOSFETs and Si IGBTs operate at high and low frequencies, respectively. The hardware-in-loop (HIL) tests validate the efficacy of the proposed modulation strategy.**

***Index Terms*—Common-mode voltage, hybrid active neutral-point-clamped (HANPC), silicon carbide (SiC), unbalanced DC-links.**

I. Introduction

THREE-LEVEL inverters (TLI) are recognized as fundamental components in modern power conversion systems, particularly in renewable energy applications, due to their superior performance over conventional two-level topologies [1], [2]. By generating three distinct voltage levels, these inverters significantly reduce voltage stress on switching devices, minimize output harmonic distortion, and lower electromagnetic interference (EMI) [3]–[5]. These characteristics enable enhanced system efficiency and improved power quality. Reliable operation is ensured for grid-connected photovoltaic (PV) systems.

The hybrid active neutral-point-clamped (HANPC) TLI topology is recognized as an advanced power electronic configuration. Compared with conventional neutral-point-clamped (NPC) inverters, diodes are replaced by active switching devices in HANPC implementations. Improved loss distribution uniformity is achieved through this structural modification. The reduced conduction voltage across switching devices is obtained. Consequently, operational efficiency and power density are elevated [6]–[8].

In the HANPC topology, each phase leg is typically constructed with six switching devices. Four low-frequency switches and two high-frequency switches are integrated in this configuration. Such a configuration makes the inverter more flexible in control and able to adapt to different loads and working conditions requirements. It enables it to have a wide range of application prospects and advantages in high-voltage high-power power electronics applications [9], [10].

In PV systems, however, the advantages of HANPC inverters are often challenged by inherent DC-links voltage imbalances. Such imbalances arise from partial shading, module degradation, or mismatched string configurations in solar arrays [11]–[13]. These conditions lead to unequal power generation across PV strings, causing asymmetric voltage distribution in the DC-links capacitors, the presence of unbalanced neutral-point voltage can degrade the overall performance of both the equipment and the grid [14].

Under severe imbalance, the neutral-point voltage oscillates excessively, amplifying common-mode voltage (CMV) and inducing leakage currents through the parasitic capacitance between PV panels and ground [15]–[17]. Elevated CMV not only degrades system efficiency but also poses safety risks, accelerates component aging, and violates grid codes for

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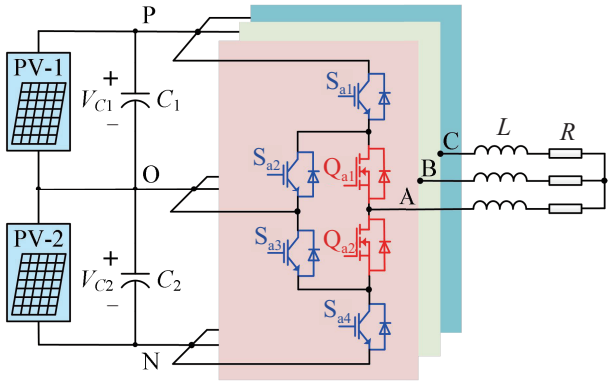

Fig. 1. Topology of the HANPC TLI with unbalanced DC-links.

electromagnetic compatibility (EMC) [18], [19]. Traditional CMV mitigation strategies, such as passive filters or complex modulation schemes, often introduce trade-offs between hardware complexity, efficiency, and current quality [20]. For instance, passive damping resistors reduce CMV at the expense of increased losses, while advanced modulation methods like virtual vector synthesis may compromise dynamic response or require excessive computational resources [21]–[23]. [24] presents a space vector modulation (SVM) strategy for suppressing the CMV in the reduced switch count (RSC) TLI with unbalanced neutral-point voltage, due to topological limitations, this method abandons the medium vector with a lower CMV amplitude. [25] proposes an optimized DPWM (O-DPWM) scheme to reduce the leakage current for three-level inverters under different neutral-point voltage conditions. The proposed method has demonstrated effective suppression of leakage current under unbalanced operating conditions, while exhibiting limited effectiveness in common-mode voltage suppression.

To this end, this paper presents a novel CMV suppression strategy for the HANPC TLI, which is applicable for both balanced and imbalanced DC-links capacitor voltage conditions. Real-time sampling of DC-links capacitor voltages enables continuous updates to the space vector diagram. A revised duty cycle calculation algorithm is introduced. The core innovation lies in the comprehensive utilization of medium vectors for reference voltage vector synthesis.

The remainder of this paper is organized as follows: Section II presents the topology and working principles of the HANPC TLI. Section III introduces the proposed modulation scheme. Section IV gives comprehensive experimental results to verify the correctness and effectiveness of the proposed method. Finally, Section V concludes this article.

II. Working Principle of HANPC TLI with Balanced and Unbalanced DC-Links

In this section, a detailed presentation of the HANPC TLI topology is given, which includes topology structure and operational principles. Fig. 1 shows the general circuit of HANPC TLI, each capacitor is connected to a PV array at both ends [26]. The capacitor voltage is denoted by V_{C1} and V_{C2}, respectively. The HANPC TLI comprises four Si IGBTs switches (S_{x1}, S_{x2}, S_{x3}, and S_{x4}) and two SiC MOSFETs switches (Q_{x1} and Q_{x2}) (x=a, b, c) in each phase.

TABLE I
Output States and Output Voltages Corresponding to Switching States of HANPC TLI

Output state	Output voltage	Switching states (x = a, b, c)					
		S_{x1}	S_{x2}	S_{x3}	S_{x4}	Q_{x1}	Q_{x2}
[P]	V_{C1}	1	0	1	0	1	0
[O+]	0	1	0	1	0	0	1
[O–]	0	0	1	0	1	1	0
[N]	$-V_{C2}$	0	1	0	1	0	1

TABLE II
Basic Voltage Vectors and CMVs for HANPC TLI with Unbalanced DC-Links

Vectors	State	CMV	State	CMV
Zero	[PPP]	V_{C1}	[OOO]	0
	[NNN]	$-V_{C2}$		
P-Type Small	[POO]	$V_{C1}/3$	[PPO]	$2V_{C1}/3$
	[OPO]	$V_{C1}/3$	[POP]	$2V_{C1}/3$
	[OOP]	$V_{C1}/3$	[OPP]	$2V_{C1}/3$
N-Type Small	[NOO]	$-V_{C2}/3$	[NNO]	$-2V_{C2}/3$
	[ONO]	$-V_{C2}/3$	[NON]	$-2V_{C2}/3$
	[OON]	$-V_{C2}/3$	[ONN]	$-2V_{C2}/3$
Medium	[PON]	$(V_{C1}-V_{C2})/3$	[OPN]	$(V_{C1}-V_{C2})/3$
	[NPO]	$(V_{C1}-V_{C2})/3$	[NOP]	$(V_{C1}-V_{C2})/3$
	[ONP]	$(V_{C1}-V_{C2})/3$	[PNO]	$(V_{C1}-V_{C2})/3$
Large	[NNP]	$(V_{C1}-2V_{C2})/3$	[PNP]	$(2V_{C1}-V_{C2})/3$
	[NPN]	$(V_{C1}-2V_{C2})/3$	[NPP]	$(2V_{C1}-V_{C2})/3$
	[PNN]	$(V_{C1}-2V_{C2})/3$	[PPN]	$(2V_{C1}-V_{C2})/3$

Table I summarizes the output states and voltage levels corresponding to all switching states of the HANPC TLI, where "1" and "0" represent the on and off states of semiconductors, respectively. It should be noted that the NPC TLI merely has three output states [P], [N], and [O], the HANPC topology contains four output states [P], [N], [O+], and [O–].

The CMV calculation formula is calculated as follows:

$$v_{CM} = \frac{v_{AO} + v_{BO} + v_{CO}}{3} \tag{1}$$

where v_{AO}, v_{BO}, and v_{CO} are three-phase output voltages. All the basic voltage vectors are summarized in Table II. Obviously, the basic vectors marked in red exhibit the highest CMV magnitudes and should therefore be excluded during reference vector synthesis. Conversely, the vectors highlighted in blue generating minimal CMV and are prioritized in the proposed space vector modulation scheme to achieve effective CMV suppression. Based on this analysis, a systematic CMV mitigation strategy for the HANPC TLI under both balanced and unbalanced DC-links capacitor voltage conditions will be

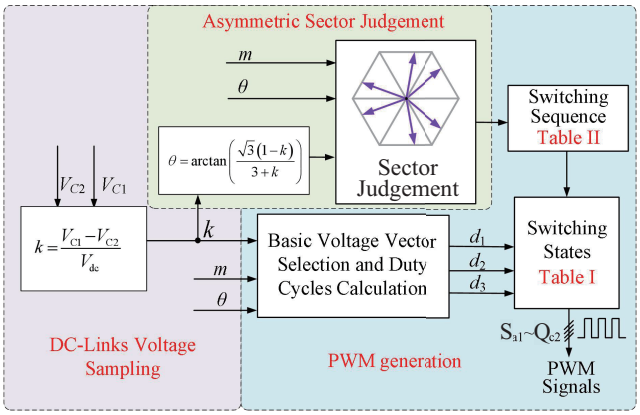

Fig. 2. Overall diagram of the proposed novel modulation method.

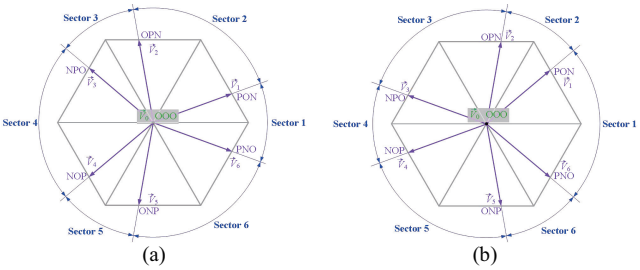

Fig. 3. SVDs for HANPC TLI with unbalanced DC-links. (a) $k > 0$, (b) $k < 0$.

elaborated in the following section.

III. Proposed Modulation Strategy

The proposed modulation strategy consists of three components. Initially, the two capacitor voltages on the DC-links are sampled, and the capacitor voltage unbalance factor k is calculated by the formula. Subsequently, the space vector diagram (SVD) is updated according to the capacitor voltage imbalance factor for sector judgment of the reference voltage vector (V_{ref}). Finally, the duty cycle is calculated based on the capacitor voltage unbalance factor, and the drive signal of the power switching tube is generated based on the corresponding switching sequence. The overall diagram of the proposed method is shown in Fig. 2.

A. DC-Links Voltage Sampling and Sector Judgement

Firstly, the voltages across capacitors C_1 and C_2 are sampled, and noted as V_{C1} and V_{C2}, respectively.

Next, the unbalanced factor k is defined as:

$$k = \left(V_{C1} - V_{C2}\right) / V_{dc} \tag{2}$$

Under unbalanced neutral point (NP) voltage conditions, the capacitor voltage fluctuates in response to variations in the voltages of the two PV arrays, resulting in a corresponding alteration of the SVD, as illustrated in Fig. 3. Consequently, the medium vector expression can be represented by the following equation:

$$\begin{cases} \vec{V}_1\ [\mathrm{PON}] = \dfrac{3+k}{6}\cdot V_{dc} + \mathrm{j}\cdot\dfrac{\sqrt{3}\cdot(1-k)}{6}\cdot V_{dc} \\ \vec{V}_2\ [\mathrm{OPN}] = -\dfrac{k}{3}\cdot V_{dc} + \mathrm{j}\cdot\dfrac{\sqrt{3}}{3}\cdot V_{dc} \\ \vec{V}_3\ [\mathrm{NPO}] = \dfrac{k-3}{6}\cdot V_{dc} + \mathrm{j}\cdot\dfrac{\sqrt{3}\cdot(1+k)}{6}\cdot V_{dc} \\ \vec{V}_4\ [\mathrm{NOP}] = \dfrac{k-3}{6}\cdot V_{dc} - \mathrm{j}\cdot\dfrac{\sqrt{3}\cdot(1+k)}{6}\cdot V_{dc} \\ \vec{V}_5\ [\mathrm{ONP}] = -\dfrac{k}{3}\cdot V_{dc} - \mathrm{j}\cdot\dfrac{\sqrt{3}}{3}\cdot V_{dc} \\ \vec{V}_6\ [\mathrm{PNO}] = \dfrac{3+k}{6}\cdot V_{dc} - \mathrm{j}\cdot\dfrac{\sqrt{3}\cdot(1-k)}{6}\cdot V_{dc} \end{cases} \tag{3}$$

Since the position of the medium vector in the SVD will change with the capacitor voltage offset on the DC-links, it is necessary to compute the position of the medium vector in real time when judging sectors, and the angle of the medium vector [PON] can be calculated by the following formula:

$$\theta = \arctan\left(\frac{\sqrt{3}(1-k)}{3+k}\right) \tag{4}$$

B. Duty Cycle Calculation and Drive Signals Generation

Taking Sector 1 as an example, two fundamental voltage vectors [PON] and [PNO] are used to synthesize the reference voltage vector. The voltage-second balance equation is written as follows:

$$\begin{cases} \vec{V}_{ref} = \vec{V}_1\cdot d_1 + \vec{V}_6\cdot d_6 + \vec{V}_0\cdot d_0 \\ d_1 + d_6 + d_0 = 1 \end{cases} \tag{5}$$

where d_1, d_6, and d_0 are the duty cycle of [PON], [PNO], and [OOO].

The corresponding duty cycle can be calculated as:

$$\begin{cases} d_1 = m\cdot\dfrac{\sqrt{3}}{3+k}\cdot\cos\theta + m\cdot\dfrac{1}{1-k}\cdot\sin\theta \\ d_6 = m\cdot\dfrac{\sqrt{3}}{3+k}\cdot\cos\theta - m\cdot\dfrac{1}{1-k}\cdot\sin\theta \\ d_0 = 1 - m\cdot\dfrac{2\sqrt{3}}{3+k}\cdot\cos\theta \end{cases} \tag{6}$$

Considering the symmetry of SVD, the duty cycle formulas in other sectors are similar to the above analysis and will not be repeated here.

In Sector 1, to satisfy the requirements of reduced switching numbers and harmonic distortions, the switching sequence is arranged as [O$_+$O_O_]-[PNO_]-[PO_N]-[PNO_]-[O$_+$O_O_], as shown in Fig. 4. Within each sampling period, the switching states of all Si IGBTs (S_{a1}–S_{c4}) are maintained unchanged, thereby avoiding additional switching losses. For the SiC

TABLE III
SWITCHING SEQUENCE OF THE PROPOSED METHOD

Sector	Switching sequence
1	[$O_+O_-O_-$]-[PNO_-]-[PO_-N]-[PNO_-]-[$O_+O_-O_-$]
2	[$O_+O_+O_-$]-[PO_+N]-[O_+PN]-[PO_+N]-[$O_+O_+O_-$]
3	[$O_-O_+O_-$]-[O_-PN]-[NPO_-]-[O_-PN]- [$O_-O_+O_-$]
4	[$O_-O_+O_+$]-[NO_+P]-[NPO_+]-[NO_+P]-[$O_-O_+O_+$]
5	[$O_-O_-O_+$]-[O_-NP]-[NO_-P]-[O_-NP]-[$O_-O_-O_+$]
6	[$O_+O_-O_+$]-[O_+NP]-[PNO_+]-[O_+NP]-[$O_+O_-O_+$]

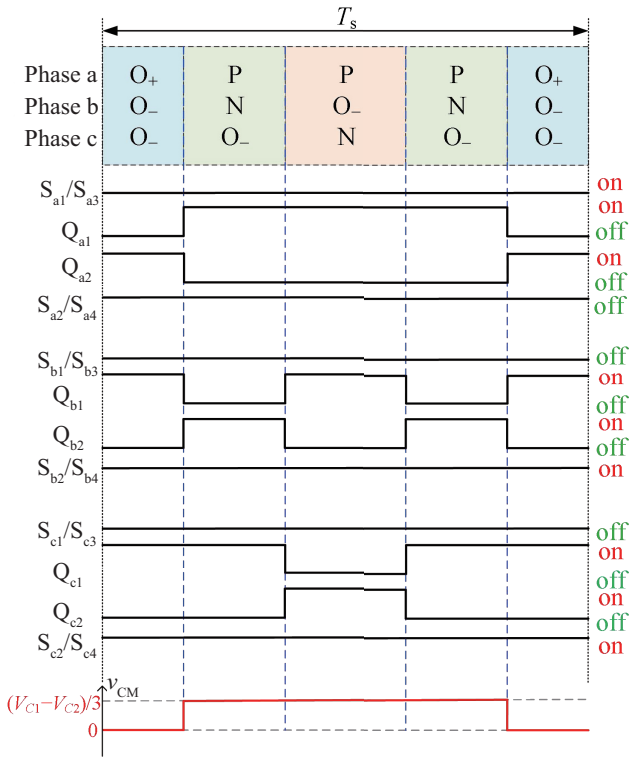

Fig. 4. Switching sequence, switching states, and CMV in Sector 1, k>0.

MOSFETs, the power devices of phase a and phase c undergo a single switching action per cycle, while the power devices of phase b exhibit two switching actions. Similar switching patterns are observed in other sectors. Furthermore, zero vector produces zero CMV, whereas the medium vectors generate a smaller CMV amplitude of only $(V_{C1}-V_{C2})/3$.

By designing a reasonable modulation strategy, the SiC MOSFETs can operate in high-frequency and the Si IGBTs can operate in fundamental frequency, which further reduces switching losses, and thus improves system efficiency. Table III summarizes the switching sequences in all sectors for the proposed modulation strategy.

IV. EXPERIMENTAL RESULTS

To validate the performance of the proposed modulation scheme, an experimental test system of the HANPC TLI is designed, as shown in Fig. 5. The main circuit is implemented

TABLE IV
PARAMETERS FOR EXPERIMENTAL TEST

Parameter	Value
DC Voltage (V_{dc})	540 V
AC output frequency (f)	50 Hz
Switching period (T_s)	100 μs
Sampling frequency (f_{SF})	10 kHz
DC-link capacitors (C_1 and C_2)	2350 μF
Voltage difference	−100 V, 0 V, 100 V
RL load	R_{load} = 10 Ω L_{load} = 7 mH

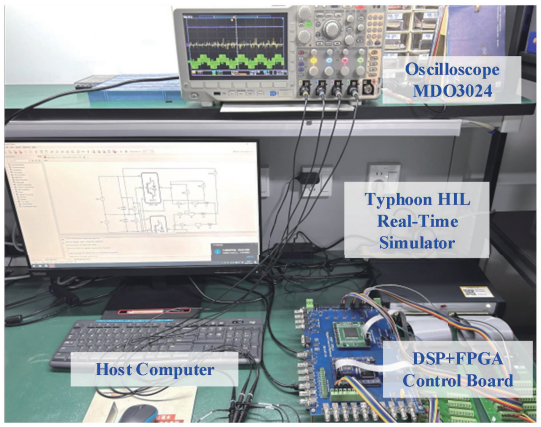

Fig. 5. Photograph of the hardware-based test rig.

based on hardware-in-the-loop (HIL) real-time simulator. The control board is designed to contain digital signal processor (DSP) 28335 from Texas Instruments and field-programmable gate array (FPGA) XC3S500E from Xilinx. The DSP is used to execute the system control strategy, while the FPGA is used to generate the PWM signals. The DSP sends data to the FPGA through an external interface (XINTF) module, which includes the sector number and the duty cycle.

The parameters for both simulation and experimental tests are given in Table IV. To demonstrate the significant advantages of the proposed modulation strategy, three modulation methods suitable for unbalanced conditions are used for comparisons. Method-1 is the hybrid SVM method in [27], method-2 is the CMV reduction method in [28], and method-3 is the proposed CMV reduction scheme.

The first verification is the operation of the three modulation methods in the balanced conditions, and the experimental results are shown in Fig. 6, in which the modulation index m is 0.4 and the voltage difference between two DC-links capacitors is set to be 270 V. The CMVs of method-1 and method-2 are relatively high, because the basic vectors with high CMV magnitudes are utilized by these two methods.

Since method-1 uses all the basic vectors to synthesize the V_{ref}, it achieves an output current total harmonic distortion (THD) of only 1.32%. However, this method exhibits signi-ficantly higher CMV amplitudes, with a peak-to-peak range of 360 V

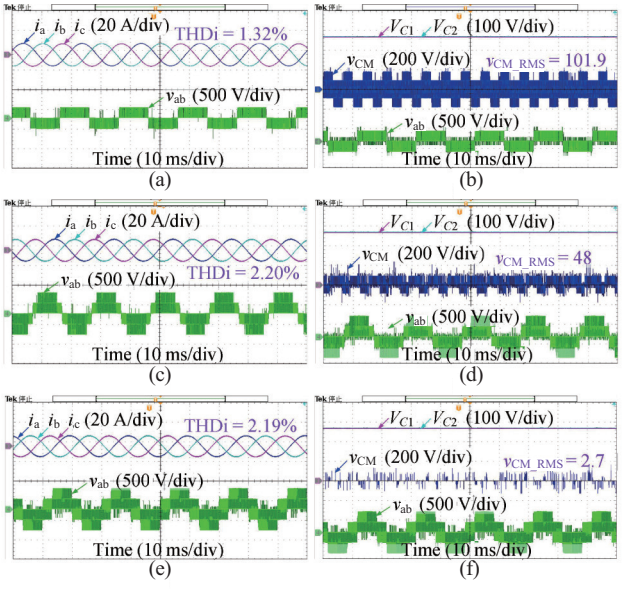

Fig. 6. Experimental results under balanced conditions (m = 0.4, k = 0). (a) Three-phase output currents and line voltage of Method-1, (b) DC power source voltage and common-mode voltage of Method-1, (c) Three-phase output currents and line voltage of Method-2, (d) DC power source voltage and common-mode voltage of Method-2, (e) Three-phase output currents and line voltage of Method-3, (f) DC power source voltage and common-mode voltage of Method-3.

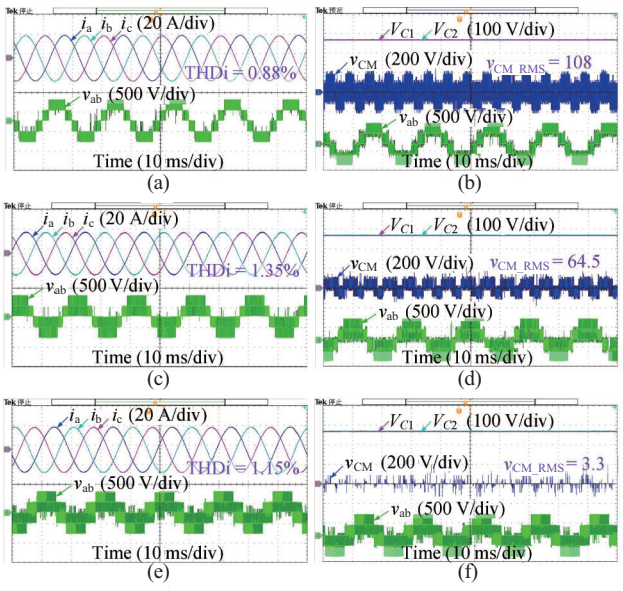

Fig. 7. Experimental results under balanced conditions (m = 0.8, k = 0). (a) Three-phase output currents and line voltage of Method-1, (b) DC power source voltage and common-mode voltage of Method-1, (c) Three-phase output currents and line voltage of Method-2, (d) DC power source voltage and common-mode voltage of Method-2, (e) Three-phase output currents and line voltage of Method-3, (f) DC power source voltage and common-mode voltage of Method-3.

(−178 V to 182 V) and an RMS value of 101.9 V. Method-2 optimizes vector selection by eliminating small vectors with high CMV amplitudes, reducing the CMV RMS value to 48 V while maintaining an output current THD of 2.20%.

The proposed method-3 adopts a medium-vector-dominated synthesis scheme, theoretically achieving zero CMV under balanced conditions. Experimental results confirm its CMV RMS value as low as 2.7 V, with an output current THD of 2.19%, demonstrating a synergistic optimization of CMV suppression and current quality. The proposed method can effectively suppress the CMV, whereas three-phase sinusoidal output currents can be guaranteed at the same time.

TABLE V
COMPARISONS OF DIFFERENT METHODS UNDER BALANCED CONDITIONS

Conditions		Range of CMV	RMS value of CMV	THDi
Method-1	m = 0.4	−178 V ~ 182 V	101.9 V	1.32 %
	m = 0.8	−179 V ~ 182 V	108 V	0.88 %
Method-2	m = 0.4	−85.2 V ~ 91.5 V	48 V	2.20 %
	m = 0.8	−85 V ~ 91 V	64.5 V	1.35 %
Method-3	m = 0.4	0 V	2.7 V	2.19 %
	m = 0.8	0 V	3.3 V	1.15 %

To further validate the adaptability of modulation strategies, experiments were repeated at a higher modulation index (m=0.8). As illustrated in Fig. 7, all three methods maintain stable operation under high modulation index conditions, with CMV suppression characteristics consistent with those observed at low modulation. Notably, method-3 restricts the CMV RMS value to 3.3 V and reduces the output current THD to 1.15%, confirming its applicability across a wide modulation index range. A systematic comparison of CMV suppression and THD performance under balanced DC-links conditions is summarized in Table V. Since method-3 avoids using the basic voltage vectors with high CMV magnitudes, the current THD value is slightly higher than that of method-1 and method-2. Fortunately, the current THD value of the proposed method remains at an acceptable level.

For DC-links voltage imbalance conditions, experiments were conducted with ±100 V deviations (k=±0.1852). As shown in Fig. 8, when the upper capacitor voltage is 100 V lower than the lower capacitor (k=−0.1852) at m=0.4, method-1 exhibits a CMV peak-to-peak range of 358.5 V (−211.5 V to 147 V) and an RMS value of 103.1 V, accompanied by a THD of 1.36%. Method-2 reduces the CMV RMS value to 59 V with a THD of 2.19%, while method-3 leverages the inherent low-CMV characteristics of medium vectors, achieving a CMV RMS value of 18.5 V and a THD of 2.7%.

At m=0.8 (Fig. 9), method-3 increases the CMV RMS value slightly to 25.8 V but further reduces the THD to 2.34%, demonstrating effective CMV suppression and high-quality current output under imbalanced conditions. Quantitative comparisons under these conditions are systematically presented in Table VI.

When the upper capacitor voltage exceeds the lower capacitor by 100 V (k = 0.1852), the experimental waveforms for the case of low and high modulation indices (m=0.4 and m=0.8) are shown in Fig. 10 and Fig. 11, respectively. The CMV suppression performance and output current quality remain consistent with those under negative imbalance conditions. Although the proposed method exhibits marginal THD degradation compared to method-1, it demonstrates a significant

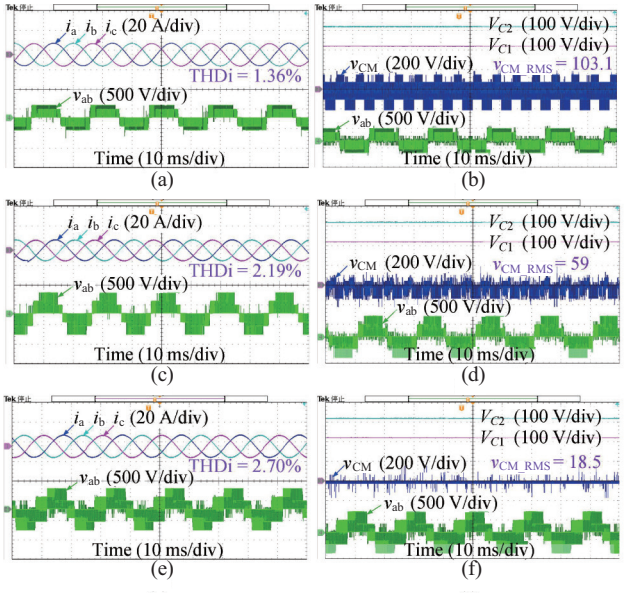

Fig. 8. Experimental results for negative unbalancing coefficient (m = 0.4, k = −0.1852). (a) Three-phase output currents and line voltage of Method-1, (b) DC power source voltage and common-mode voltage of Method-1, (c) Three-phase output currents and line voltage of Method-2, (d) DC power source voltage and common-mode voltage of Method-2, (e) Three-phase output currents and line voltage of Method-3, (f) DC power source voltage and common-mode voltage of Method-3.

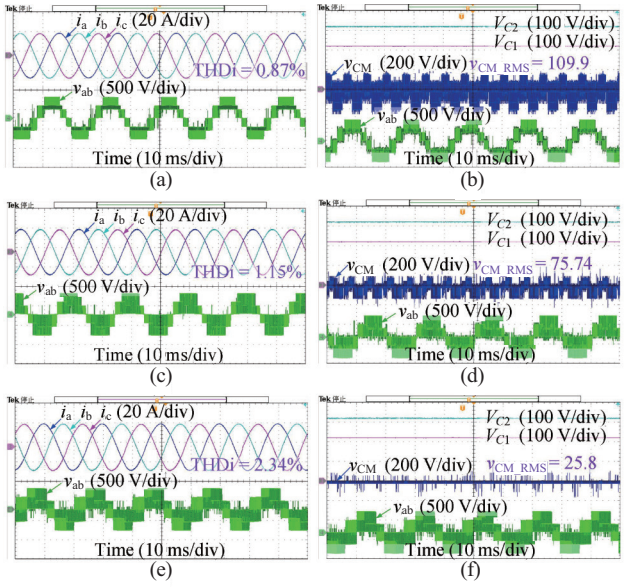

Fig. 9. Experimental results for negative unbalancing factor (m = 0.8, k = −0.1852). (a) Three-phase output currents and line voltage of Method-1, (b) DC power source voltage and common-mode voltage of Method-1, (c) Three-phase output currents and line voltage of Method-2, (d) DC power source voltage and common-mode voltage of Method-2, (e) Three-phase output currents and line voltage of Method-3, (f) DC power source voltage and common-mode voltage of Method-3.

advantage in CMV amplitude reduction. The quantitative performance for positive unbalancing factor is summarized in Table VII.

Overall, method-3 effectively reduces the CMV amplitude and RMS value under different modulation indexes and

TABLE VI
COMPARISONS OF DIFFERENT METHODS FOR NEGATIVE UNBALANCING FACTOR (K = −0.1852)

Conditions		Range of CMV	RMS value of CMV	THDi
Method-1	m = 0.4	−211.5 V ~ 147 V	103.1 V	1.36 %
	m = 0.8	−211.5 V ~ 147 V	109.9 V	0.87 %
Method-2	m = 0.4	−136 V ~ 73 V	59 V	2.19 %
	m = 0.8	−135.5 V ~ 73 V	75.74 V	1.15 %
Method-3	m = 0.4	−28 V ~ 0 V	18.5 V	2.70 %
	m = 0.8	−28 V ~ 0 V	25.8 V	2.34 %

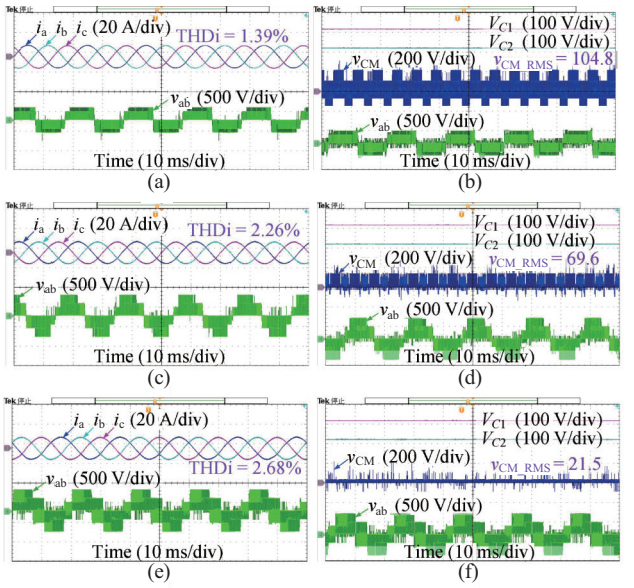

Fig. 10. Experimental results for positive unbalancing factor (m = 0.4, k = 0.1852). (a) Three-phase output currents and line voltage of Method-1, (b) DC power source voltage and common-mode voltage of Method-1, (c) Three-phase output currents and line voltage of Method-2, (d) DC power source voltage and common-mode voltage of Method-2, (e) Three-phase output currents and line voltage of Method-3, (f) DC power source voltage and common-mode voltage of Method-3.

different unbalance factors, thus ensuring the safe and stable operation of the inverter system.

Selected experimental waveforms of the power switch drive signals are depicted in Fig. 12. All three modulation methods achieved hybrid high-low frequency modulation. Method-1 and method-2 generate only one switching action per phase per cycle, whereas method-3 introduces optimized medium-vector timing to achieve precise CMV control, resulting in two switching actions for one phase while maintaining single switching actions for the other two phases, consistent with theoretical predictions. This design ensures minimal additional switching losses while prioritizing CMV suppression.

To verify the influence of unbalanced conditions on the DC side on the loss distribution, a co-simulation platform of Simulink and PLECS was built for the proposed common-mode voltage suppression method, and the corresponding losses were calculated and summarized in Fig. 13. It can be seen from the figure that under balanced conditions, due to its symmetrical

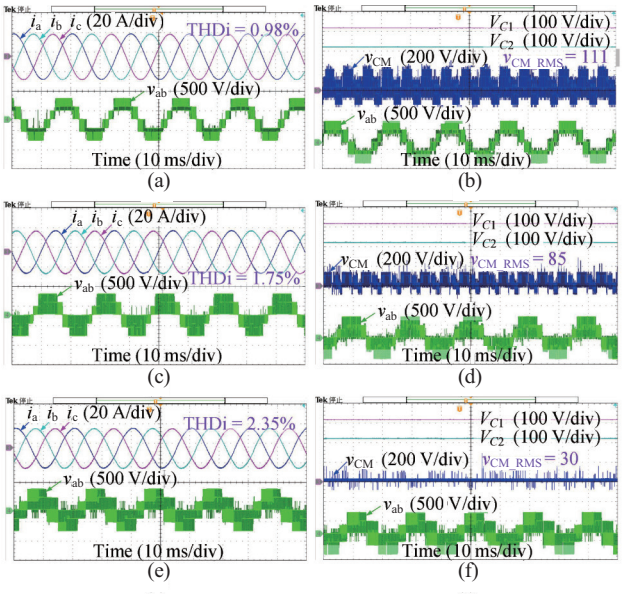

Fig. 11. Experimental results for positive unbalancing factor (m = 0.8, k = 0.1852). (a) Three-phase output currents and line voltage of Method-1, (b) DC power source voltage and common-mode voltage of Method-1, (c) Three-phase output currents and line voltage of Method-2, (d) DC power source voltage and common-mode voltage of Method-2, (e) Three-phase output currents and line voltage of Method-3, (f) DC power source voltage and common-mode voltage of Method-3.

TABLE VII
COMPARISONS OF DIFFERENT METHODS FOR NEGATIVE UNBALANCING FACTOR (K = 0.1852)

Conditions		Range of CMV	RMS value of CMV	THDi
Method-1	m = 0.4	−142.5 V ~ 217.5 V	104.8 V	1.39 %
	m = 0.8	−143 V ~ 217 V	111 V	0.98 %
Method-2	m = 0.4	−68 V ~ 140 V	69.6 V	2.26 %
	m = 0.8	−68 V ~ 141.5 V	85 V	1.75 %
Method-3	m = 0.4	0 V ~ 33 V	21.5 V	2.68 %
	m = 0.8	0 V ~ 32.5 V	30 V	2.35 %

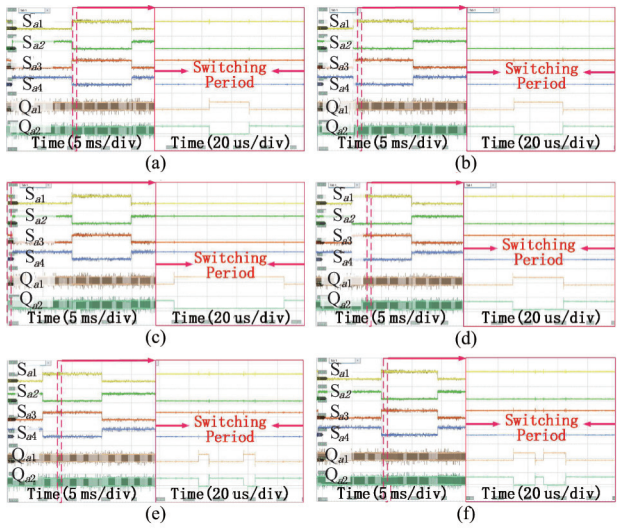

Fig. 12. Drive signals of power switches. (a) method-1, m = 0.8, k = 0, (b) method-1, m = 0.8, k = 0.1852, (c) method-2, m = 0.8, k = 0, (d) method-2, m = 0.8, k = 0.1852, (e) method-3, m = 0.8, k = 0, (f) method-3, m = 0.8, k = 0.1852.

characteristics, the conduction loss and switching loss of power devices can remain relatively balanced. Under the unbalanced condition on the DC-links, when k=−0.1852, the increase in the voltage of the lower capacitor C_2 will increase the switching loss of the power device Q_{a2}, but the overall loss can remain relatively balanced. The same conclusion can be extended to other conditions.

V. CONCLUSION

For the dual-input TLI system, this paper presents a novel CMV reduction method for HANPV TLI with balanced and unbalanced NP voltage conditions. This method eliminates vectors with higher CMV amplitudes. By sampling the DC-links capacitor voltages, an imbalance factor is calculated, which subsequently facilitates the reconfiguration of the SVD, thereby simplifying the computational complexity. Furthermore, a symmetrical five-segment switching sequence that starts and ends with zero vector is designed to reduce harmonics. Experiments verify the effectiveness of the proposed modulation strategy.

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