Improved Transformer-Less Grid-Connected PV Inverter with CCMV for Enhanced Efficiency

Aditi Atul DESAI and Suresh MIKKILI

***Abstract*—This paper introduces a new inverter design known as "Novel H6 inverter" with six switches to address the challenges related to common mode voltage fluctuations, leakage current, conduction losses and efficiency in a grid connected inverter that does not use transformer. Its working and performance is further compared with prevailing inverters without transformer, namely H5, H6-I, H6-II, and HERIC. The focus is on evaluating the common mode voltage and common mode current produced by these inverters. All five inverters are modelled on MATLAB/Simulink platform and a comparative study based on simulation outcome is carried out. Subsequently, the simulation results are confirmed through practical implementation on hardware prototype. The hardware validation provides concrete evidence of the proposed inverter's performance and serves to enhance the credibility of the study's conclusions.**

***Index Terms*—Common mode current, common mode voltage, parasitic capacitance, six switch inverter, transformer-less inverters.**

I. Introduction

THE increasing popularity of inverters without transformer in photovoltaic (PV) systems connected to the grid can be attributed to their advantages, such as lower cost, reduced weight and improved efficiency. This has led to their widespread adoption in distributed PV power generation systems [1]. Nevertheless, the leakage current is also referred as common mode current (CMC) present in transformer-less inverters (TLI) can give rise to electromagnetic interference, and issues related to reliability and security.

The block diagram shown in Fig. 1 depicts a direct link of the solar system to the grid, removing the requirement for a transformer.

In this system, stray capacitance is created due to voltage variation amid PV and ground. C_{pv1} indicates the incidental capacitance between the PV positive terminal and ground; C_{pv2} represents the incidental capacitance between the PV negative terminal and ground; C_{pv} indicates effective stray capacitance. Common mode voltage (CMV) refers to the voltage difference between PV system and ground. The elements that affect parasitic capacitance include the PV cell and module surfaces, the distance between them, dust, and humidity.

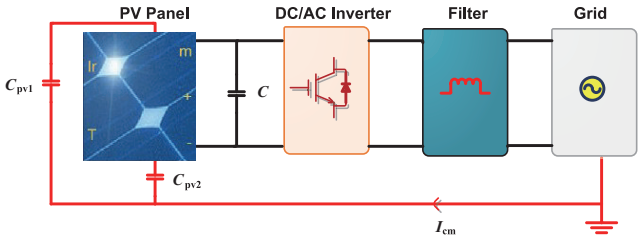

Fig. 1. Representation of PV and Grid integration.

CMV charges and discharges C_{pv} which generates CMC and is indicated as I_{cm}. This CMC affects the safety of the person [2] and also increases electromagnetic interference, grid current variations, and overall system losses.

To ensure the safe functioning of grid connected PV system using TLI, adherence to established safety standards is essential [3]. One crucial safety requirement outlined by VDE 0126-1-1 is that if the CMC exceeds 30 mA, the protective mechanism must initiate the disconnection within 0.3 seconds [4]. This specification aims to swiftly mitigate any potential hazards associated with excessive CMC. Many researchers have compared the existing TLI to eliminate the CMC [5]–[10]. Accordingly, some researchers have suggested methods such as AC isolation, DC isolation, and topologies with the common ground or CMV clamping [11]–[20].

A common-ground inverter based on the Cuk converter with high voltage gain is proposed in [21] to suppress the leakage current. A coupled inductor and a capacitor are connected in series to enhance the Boost capability in the circuit. [22] has proposed a general topology derivation method of the double-grounded single-phase inverters based on graph theory. In [23], a new Buck-Boost DC-AC inverter is developed for PV system with broad input voltage range coverage. [24] proposed to eliminate CMC by a method based on modulation. The suggested carrier-assist modulation stabilized the flying capacitor voltage by altering the pulse sequence and could eliminate CMV. [25] recommended a TLI with five level switched capacitor and boosting capability. [26] proposed a quasi-one-stage four switches inverter with an ability to eliminate CMC. A common mode equivalent circuit is developed in [27], considering the filter and grounding system. In order to

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A. A. Desai is with the Electrical and Electronics Engineering, Goa College of Engineering, Goa 403401, India (e-mail: aditi@gec.ac.in).

Suresh Mikkili is with the Electrical and Electronics Engineering, National Institute of Technology, Goa 403703, India (e-mail: mikkili.suresh@nitgoa.ac.in).

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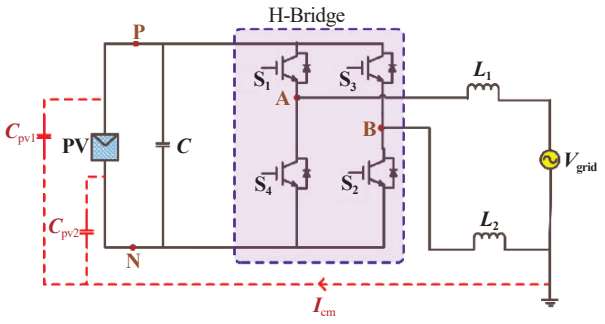


Fig. 2. Path of leakage current between grid and PV in the absence of transformer.

overcome the low-frequency leakage currents, a CMV control method is proposed. A high-dimensional space vector PWM is introduced to synthesize both differential mode voltage and CMV references for the single/three-phase PWM converter. A nine-level inverter with four times the input voltage gain is proposed in [28]. The configuration is designed based on a switched capacitor (SC) along with common ground structure. The common ground helps in avoiding parasitic capacitance. CCMV switched capacitor PV inverter configuration is proposed in [29] that maintains a low-frequency terminal voltage while considering the effect of switch device junction capacitance. In a two stage topology, [30] has proposed a gain unit circuit in the front-stage to improve the Boost capability. In addition, the rear-stage converter has double Buck inverter, which is able to prevent the short circuit of the bridge arms and improves the reliability of the system. Also, it ensures that there is no high-frequency component in the parasitic capacitor voltage, and suppresses the leakage current. A novel reconfigurable LCL filter in PV transformer less inverters is proposed in [31], which eliminates the need for a DC link connection. It also clamps the common-mode voltage to neutral at high frequencies, resulting in the reduction of leakage current. [32] has designed single-phase onboard charger to achieve low leakage current with an MPC based zero sequence control method. A hybrid topology using both decoupling and midpoint clamping technique is adopted in [33] to reduce the root mean square and peak value of leakage current.

In this paper an effort is made to reinforce the current research by recommending a new six switch TLI called Novel six switch inverter to eradicate the CMC, minimize the conduction loss and improve the efficiency. Therefore, this paper first analyzes the working of H5, H6-I, H6-II, and HERIC TLI and then recommends a Novel six switch TLI to improve the limitations of the above inverters. MATLAB/Simulink software is utilized, to simulate these inverters and are further confirmed experimentally in a laboratory setup.

II. Concept of Leakage Current

The PV panel supplies DC input to the 4 switch inverter as shown in Fig. 2. P and N represent the terminals of solar panel; A and B represent the TLI output terminals. The output of the inverter is filtered by symmetrical inductors and fed to a single-phase grid. It is seen that parasitic capacitance C_{pv1} and C_{pv2} exist between PV and ground.

V_{AN} and V_{BN} are averaged to form CMV (V_{cm}), where V_{AN} represents the voltage across node A and N; V_{BN} represents the voltage across node B and N. The expression for V_{cm} is as follows [34], [35]:

$$V_{cm} = \frac{V_{AN+}V_{BN}}{2} \tag{1}$$

The difference between V_{AN} and V_{BN} is called differential mode voltage (V_{dm}). It is given by (2).

$$V_{dm} = V_{AN} - V_{BN} \tag{2}$$

V_{dm} generates a surplus V_{cm} called V_{cm_dm}. It is given by (3).

$$V_{cm\_dm} = \frac{V_{AN} - V_{BN}}{2} \cdot \frac{L_2 - L_1}{2(L_2 + L_1)} \tag{3}$$

Therefore, the total V_{cm} (V_{cm_total}) is given by (4).

$$\begin{cases} V_{cm\_total} = V_{cm} + V_{cm\_dm} \\ V_{cm\_total} = \dfrac{V_{AN} + V_{BN}}{2} + \dfrac{V_{AN} - V_{BN}}{2} \cdot \dfrac{L_2 - L_1}{2(L_2 + L_1)} \end{cases} \tag{4}$$

If identical inductors are used as a filter, such that $L_1 = L_2$, then (4) is reduced to $V_{cm\_total} = V_{cm}$.

CMC (I_{cm}) depends on V_{cm} and equivalent parasitic capacitance C_{pv}. The equation for I_{cm} is given by (5).

$$I_{cm} = C_{pv} \frac{dV_{cm}}{dt} \tag{5}$$

If CMV is maintained constant, then the CMC can be made zero. V_{AN} and V_{BN} values are defined by inverter topologies and modulation schemes. Hence, constant CMV (CCMV) can be obtained by implementing various inverter topologies and modulation methods.

The most commonly used modulation techniques are Unipolar (UPWM) and Bipolar (BPWM). The advantage of UPWM is that it generates three-level voltage, produces low losses, and generates high efficiency. The main disadvantage is that it generates significant CMC due to varying CMV.

Bipolar modulation on the other side results in a two-level voltage and effectively manages the challenges of high core and switching losses. Hence it generates low efficiency in comparison with UPWM. Yet, it produces stable CMV and a low magnitude of CMC.

To exploit the numerous advantages of UPWM technique, this paper employs the same to generate the triggering pulses across all the considered inverters.

III. Existing Transformer-Less Topologies

The TLI topologies which already exist in literature are H5, H6, and HERIC. H5 and H6 topologies are DC-decoupled whereas, HERIC topology is AC-decoupled. H5, HERIC, and two versions of H6 TLI are discussed in this paper in terms of their working, nature of CMV, amount of CMC, conduction losses produced, and efficiency generated.

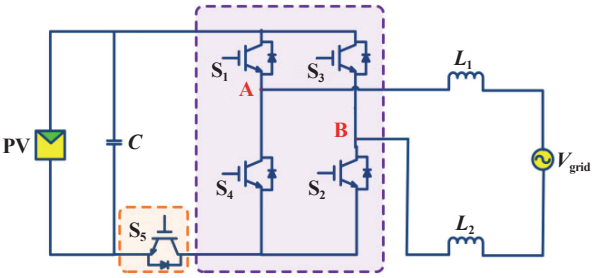


Fig. 3. Illustration of H5 topology.

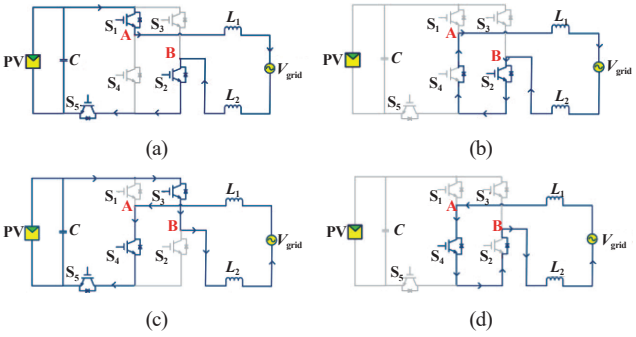


Fig. 4. Demonstration of H5 topology working. (a) Conduction mode for V_g>0, (b) Freewheeling mode for V_g>0, (c) Conduction mode for V_g<0, (d) Freewheeling mode for V_g<0.

A. H5 Inverter Topology:

This topology is an extension of full bridge (FB) inverter with an intermediate switch S_5 between PV system and the FB inverter. Including the fifth switch assures separation of the PV and grid while switching to zero voltage. Fig. 3 represents the H5 topology. In this topology, S_2 operates at 50 Hz during V_g>0; S_4 operates at 50 Hz during V_g<0 whereas, switches S_1 and S_3 function at 10 kHz during the alternate phases of V_g, respectively. S_5 maintains a constant switching frequency for the full cycle.

The H5 topology has four modes of working.

When S_1, S_2, and S_5 are triggered in mode 1, as shown in Fig. 4(a), they establish a conductive pathway between PV and grid. In mode 2, as per Fig. 4(b), the current finds a path through S_2 and built-in diode of switch S_4. In mode 3, as per Fig. 4(c), the grid current has reversed its direction and flows through S_3, S_4, and S_5 and connects the PV to the grid. In mode 4, as per Fig. 4(d), the current finds a path through S_4 and built-in diode of switch S_2.

CMV shuffles between $V_{pv}/2$ and 0 in 4 modes, where V_{pv} is the voltage across the solar panel. Hence, in the H5 topology, CMC flows between PV and grid. Fig. 13(a) and Fig. 13(b) depicts the waveforms for V_{AN}, V_{BN}, and V_{AB}, V_{cm}, and I_{cm} of H5 inverter.

B. H6-I Inverter Topology:

In this topology, there are two symmetrical switches connected with the FB topology. Fig. 5 represents the H6-I topology proposed in [36].

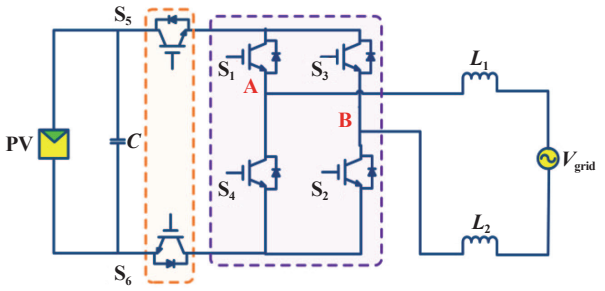


Fig. 5. Demonstration of H6-I inverter.

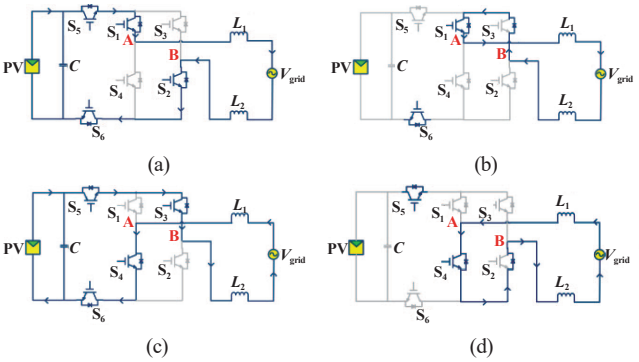


Fig. 6. Demonstration of H6-I topology working. (a) Conduction mode for V_g>0, (b) Freewheeling mode for V_g>0, (c) Conduction mode for V_g<0, (d) Freewheeling mode for V_g<0.

In H6-I inverter, switch S_1 and S_4 function at line frequency, whereas S_2 and S_3 are triggered at switching speed of 10 kHz. To achieve the DC-decoupling, two symmetrical switches, S_5 and S_6, are triggered in a sequential manner at both line frequency and switching speed. The four modes of working are depicted in Fig. 6(a) to 6(d) respectively. In mode 1, S_5, S_1, S_2, and S_6 switches are triggered, leading to positive grid current.

In mode 2, since S_2 and S_5 are off, the voltage V_{AN} gradually decreases whereas V_{BN} increases until the voltages are equal and the inductor current flows between built in diode of S_3 and switch S_1. In mode 3, current through the inductor increases in the reverse direction and flows through S_5, S_3, S_4, and S_6 switches. In mode 4, since S_3 and S_6 switches are off, the voltage V_{AN} gradually increases whereas V_{BN} decreases until the voltages are equal and the current through inductor circulates between S_4 switch and S_2 body diode.

It is seen that CMV does not change in any of the modes. Fig. 13(c) and Fig. 13(d) indicates the waveforms of H6-I inverter topology.

C. H6-II Inverter Topology:

This inverter was proposed in [37]. It has six switches and two diodes. Fig. 7 represents the H6-II topology. The top two and bottom two switches operate at 10 kHz during positive and reverse half cycles, respectively. The middle two switches operate at line frequency.

In mode 1, as depicted in Fig. 8(a), S_1, S_2, and S_3 carry the

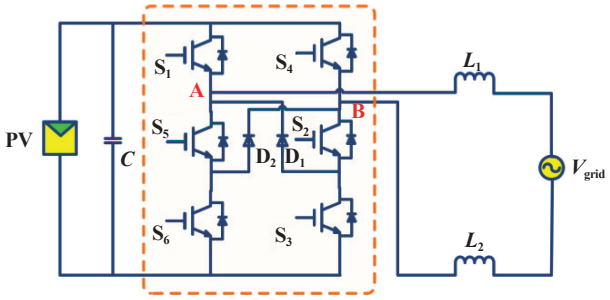


Fig. 7. Demonstration of H6-II inverter.

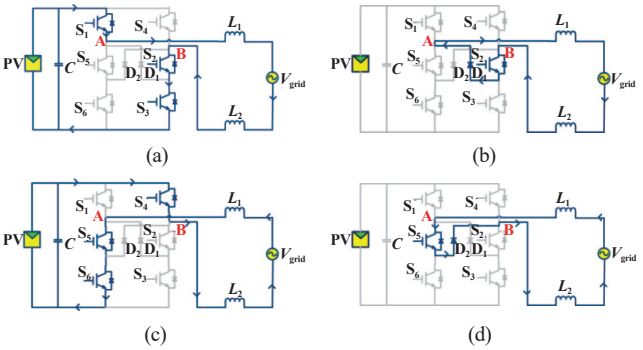


Fig. 8. Demonstration of H6-II topology functioning. (a) Working mode for V_g>0, (b) Idling mode for positive V_g, (c) Working mode for negative V_g, (d) Idling mode for negative V_g.

current. In mode 2, as seen in Fig. 8(b), switch S_2 and diode D_1 carry the current flow. Hence it isolates the PV and the grid. However, CMV remains unchanged and is $V_{PV}/2$. In the third mode, as depicted in Fig. 8(c), the current reverses itself since switches S_4, S_5, and S_6 are operated. In mode 4, as seen in Fig. 8(d), switch S_5 and diode D_2 allow the current to circulate. Thus it disconnects the PV from the grid. From the above, it can be seen that CMV remains constant in all four modes.

Fig. 13(e) and Fig. 13(f) depicts the waveforms of H6-II inverter.

D. HERIC Inverter Topology:

The highly efficient and reliable inverter concept (HERIC) topology is AC-decoupled since two additional switches are added at the output of the inverter terminals. Fig. 9 represents HERIC topology. S_5 and S_6 operate at 50 Hz, while S_1, S_2, S_3, and S_4 switches function at 10 kHz.

The system works in four distinct modes. In mode 1, as depicted in Fig. 10(a), S_1, S_2, and S_5 are turned on. Mode 2, as per Fig. 10(b), is the circulating mode. The current flows through S_6 built in diode and switch S_5. Thus there is no link between PV and grid. In mode 3, as per Fig. 10(c), the current reverses its direction and conducts through S_3 and S_4. Mode 4 is like mode 2, as depicted in Fig. 10(d), where the current through inductor circulates between the body diode of S_5 and switch S_6. Thus there is no connection between PV and grid.

From the above, it can be seen that HERIC inverter maintains constant CMV (CCMV) in all four modes.

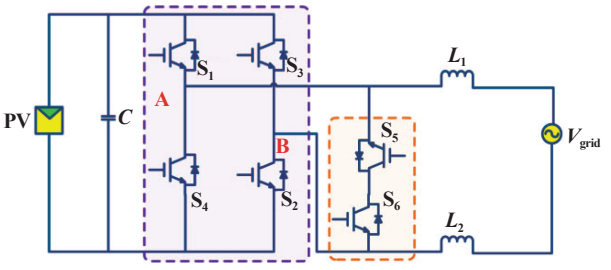


Fig. 9. Illustration of HERIC inverter.

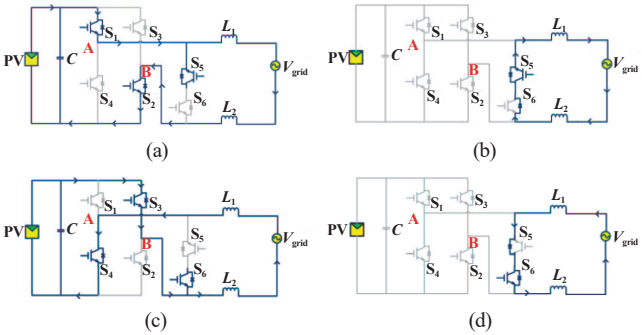


Fig. 10. Demonstration of HERIC topology working. (a) Conduction mode for V_g>0, (b) Freewheeling mode for V_g>0, (c) Conduction mode for V_g<0, (d) Freewheeling mode for V_g<0.

The simulated waveforms of V_{AN}, V_{BN}, and V_{AB}, V_{cm}, I_{cm} of HERIC topology are depicted in Fig. 13(g) and Fig. 13(h) respectively.

IV. Novel H6 Inverter Topology

This Novel H6 inverter is derived from H5 topology. The limitation of the H5 inverter of not maintaining CMV constant throughout 4 modes is overcome in this proposed inverter. Secondly, the conduction losses are reduced in Novel six switch inverter in comparison with H5 inverter. A supplementary switch S_6 is connected in the circuit amid point A and N of PV panel. This extra switch acts as a bypass path and helps in minimizing the conduction loss. Fig. 11(a) denotes the circuit of the Novel H6 inverter. Fig. 11(b) demonstrates the switching technique for the proposed inverter. Fig. 11(c) illustrates the control strategy for the proposed six switch Inverter topology. Second order generalized integrator-phase locked loop (SOGI-PLL) and PR controller is utilized to generate PWM pulses.

A. Working of Novel H6 Inverter Topology:

Novel H6 TLI has four modes of working as follows:

Mode 1:

S_1, S_2, and S_5 are triggered so that PV and grid is connected. This is evident from Fig. 12(a). S_1 and S_5 switches function at 10 kHz, while S_2 works at 50 Hz. Following are the voltage equations:

$$V_{AN} = V_{PV} \tag{6}$$

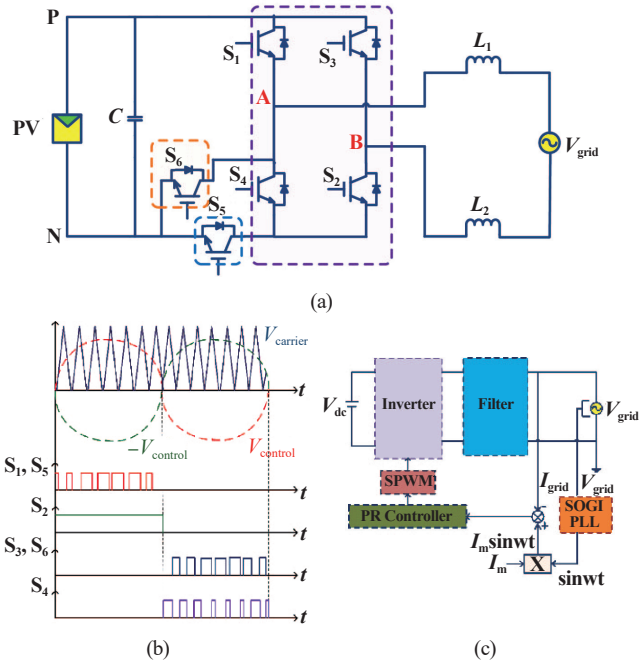


Fig. 11. (a) Novel H6 inverter, (b) PWM pulses, (c) Control strategy.

$$V_{BN} = 0 \tag{7}$$

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{PV} + 0}{2} = \frac{V_{PV}}{2} \tag{8}$$

Mode 2:

It denotes the circulating mode. The current freely circulates from S_2 and diode of S_4. Therefore, there is disconnection between the PV and grid. This can be observed in Fig. 12(b). Following are the voltage equations in this mode:

$$V_{AN} = \frac{V_{PV}}{2} \tag{9}$$

$$V_{BN} = \frac{V_{PV}}{2} \tag{10}$$

$$V_{cm} = \frac{\frac{V_{PV}}{2} + \frac{V_{PV}}{2}}{2} = \frac{V_{PV}}{2} \tag{11}$$

Mode 3:

PV and grid are linked in this conduction mode. There is flow of reverse current which is visible in Fig. 12(c). S_3 and S_6 operate at 10 kHz during grid voltage's reverse half cycle. Only two switches conduct in proposed inverter whereas one extra switch operates in H5 inverter. Hence, proposed inverter reduces conduction losses and enhances the efficiency. The expressions pertaining to voltage are as following:

$$V_{AN} = 0 \tag{12}$$

$$V_{BN} = V_{PV} \tag{13}$$

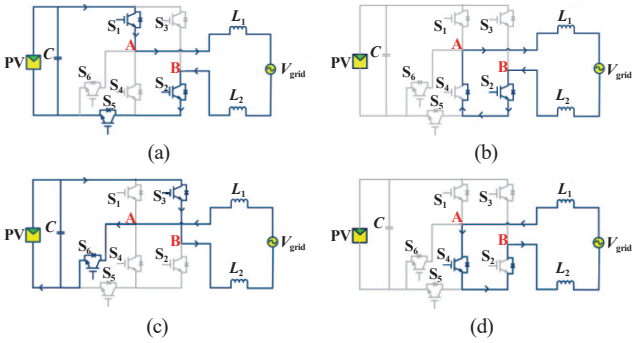


Fig. 12. Demonstration of Novel H6 topology working. (a) Conduction mode for V_g>0, (b) Idling mode for positive V_g, (c) Working mode for negative V_g, (d) Idling mode for negative V_g.

TABLE I
VALUES OF PARAMETER

Parameters	Values
Input D.C Voltage	400 V
Grid r.m.s voltage/Grid Frequency	230 V/50 Hz
Current through grid	7.07 A
DC link Capacitance (C)	500 µF
Switching frequency	10 kHz
Inductance (L_1, L_2)	4.06 mH
Stray capacitor (C_{pv1}, C_{pv2})	1 nF
Resistance of ground	5 Ω

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \tag{14}$$

Mode 4:

This is the circulating mode in which the current through inductor flows through S_4 and body diode of S_2 switch. Therefore, S_4 is complementary to switch S_6 during V_g<0. Therefore, by no chance switch S_4 and S_6 can turn on simultaneously. It is depicted in Fig. 12(d). The expressions pertaining to voltage are as following:

$$V_{AN} = \frac{V_{PV}}{2} \tag{15}$$

$$V_{BN} = \frac{V_{PV}}{2} \tag{16}$$

$$V_{cm} = \frac{\frac{V_{PV}}{2} + \frac{V_{PV}}{2}}{2} = \frac{V_{PV}}{2} \tag{17}$$

The simulated waveforms for V_{AN}, V_{BN}, and V_{AB}, V_{cm}, I_{cm} for Novel six switch inverter are seen in Fig. 13(i) and Fig. 13(j) respectively.

Table I shows the values of parameters for simulation in MATLAB.

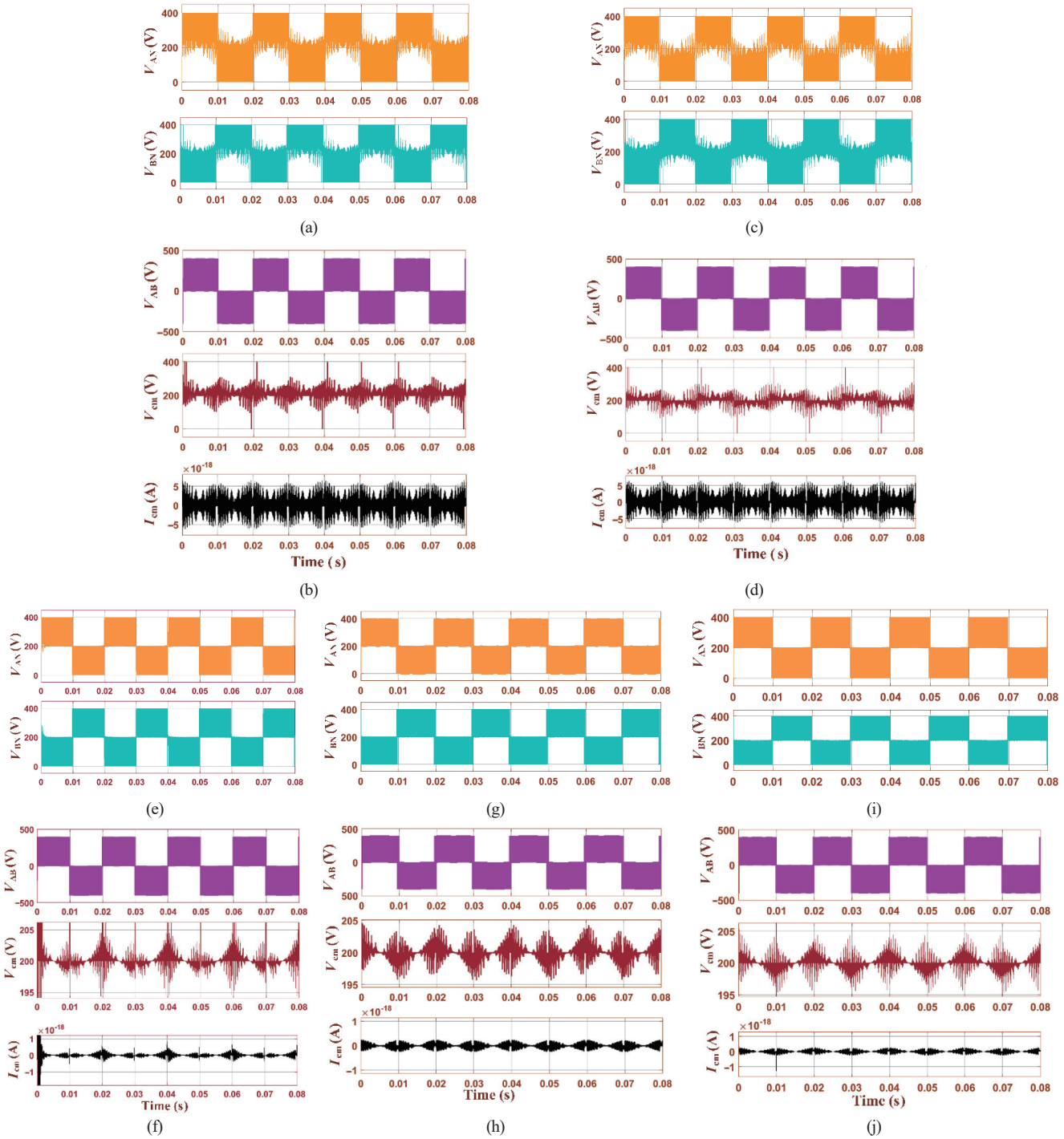


Fig. 13. Simulated waveforms of H5. (a) V_{AN}, V_{BN}, (b) V_{AB}, V_{cm}, and I_{cm}; waveforms of H6-I, (c) V_{AN}, V_{BN}, (d) V_{AB}, V_{cm}, and I_{cm} ; waveforms of H6-II, (e) V_{AN}, V_{BN}. (f) V_{AB}, V_{cm}, and I_{cm}; waveforms of HERIC, (g) V_{AN}, V_{BN}, (h) V_{AB}, V_{cm}, and I_{cm}; waveforms of Novel H6 inverter topology, (i) V_{AN}, V_{BN}, (j) V_{AB}, V_{cm}, and I_{cm}.

V. Hardware Implementation of H5, H6-I, HERIC, and Novel H6 Inverter

To further strengthen the simulation findings, H5, H6-I, HERIC, and novel H6 inverter are implemented in hardware. Hardware is carried out based on the equipment available in the laboratory. Three phase four leg IGBT inverter is used with SKM100GB125DN IGBTs having maximum voltage of 1200 V, maximum current of 100 A and maximum switching frequency of 100 kHz. OP 4500 OPAL-RT, PF515043S01, is used as a controller to produce PWM signals for the inverter. Input DC voltage of 35 V is fed to the inverter circuit by DC power supply. The circuit is realized by connecting a rheostat of 100 Ω, 2 A rating across the output of the inverter. The results are displayed on the Digital Storage Oscilloscope. The waveforms of V_{AN}, V_{BN}, V_{AB}, load current, and $V_{AN} + V_{BN}$ of the inverters are depicted in Fig. 14(a) – (h). The experimental hardware setup for implementation of these inverters is depicted in Fig. 15.

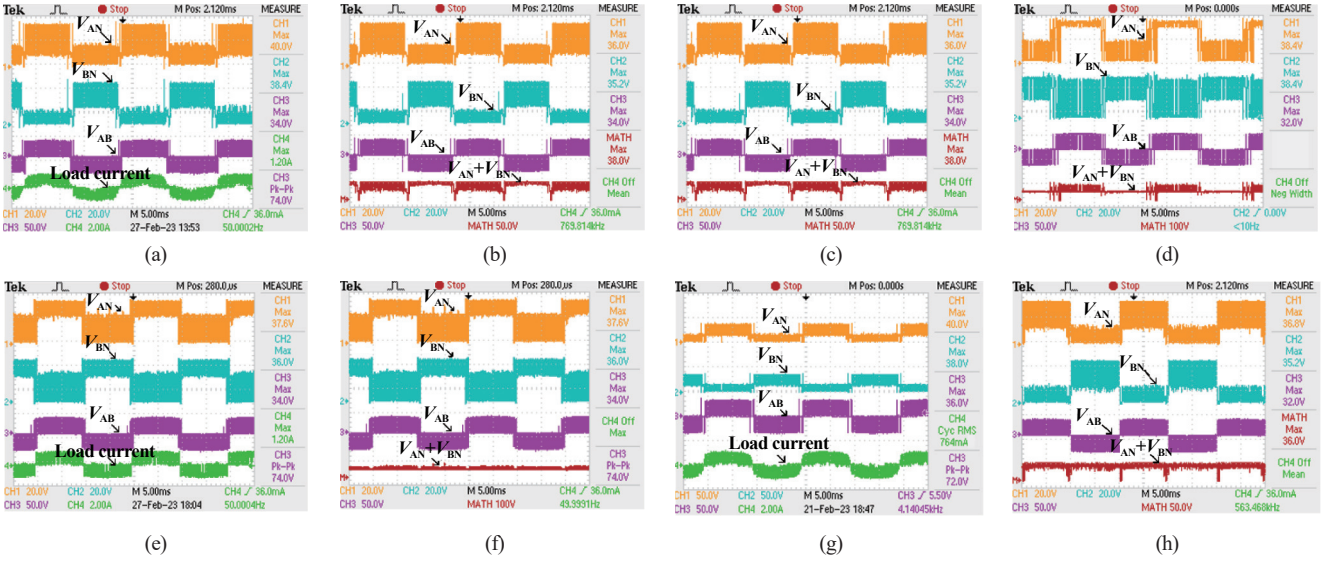


Fig. 14. Hardware results of H5. (a) V_{AN}, V_{BN}, V_{AB}, and load current, (b) V_{AN}+V_{BN}; hardware results of H6-I, (c) V_{AN}, V_{BN}, V_{AB}, and load current, (d) V_{AN}+V_{BN}; hardware results of HERIC, (e) V_{AN}, V_{BN}, V_{AB}, and load current, (f) V_{AN}+V_{BN}; hardware results of Novel H6, (g) V_{AN}, V_{BN}, V_{AB}, and load current, (h) V_{AN}+V_{BN}.

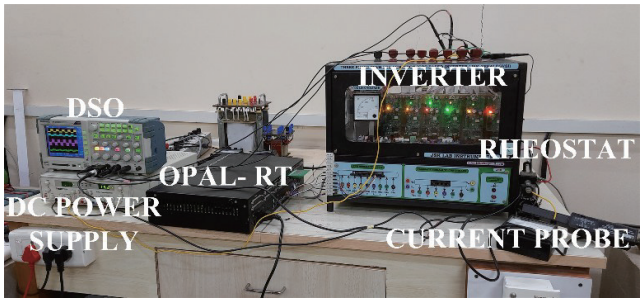


Fig. 15. Experimental Hardware Set up.

Figs. 14(a) and (b) shows the hardware results of the H5 inverter, Figs. 14(c) and (d) depicts the hardware results of the H6-I inverter, Figs. 14(e) – (f) displays the hardware results of HERIC inverter and Figs. 14(g) – (h) showcases the hardware results of Novel H6 inverter. From the above hardware findings, it can be concluded that the simulated results and hardware results are in sync. It is noticed that H5 inverter cannot maintain CMV constant and hence has some CMC flowing from the grid to the PV. H6-I inverter performs better as compared to H5 in maintaining CMV constant. However, H6-I has four switches conducting in both the active modes, whereas H5 inverter has three switches conducting in active modes. Therefore, conduction losses in H6-I inverter are more as compared to H5 inverter. As seen from simulation results and hardware results, it is proved that HERIC inverter maintains constant CMV in comparison with H5 and H6-I inverter.

The proposed Novel H6 inverter also tries to maintain CMV constant in comparison with H5 and H6-I inverter. Thus, the Novel H6 inverter can be regarded at par with HERIC in suppressing the CMC. In H6-II inverter, three switches operate during each conduction mode and it uses two additional diodes in the circuit. In HERIC inverter, in conduction mode, two switches are in operation. Whereas in Novel H6 inverter, three switches operate during positive conduction mode and two switches operate during negative conduction mode. Compared to the HERIC inverter, the Novel H6 inverter experiences higher conduction losses, which can impact its overall efficiency. However, when compared to the DC decoupled inverters, the Novel H6 inverter demonstrates lower conduction losses. As a result, the proposed Novel H6 inverter achieves a higher level of efficiency in comparison with other inverters.

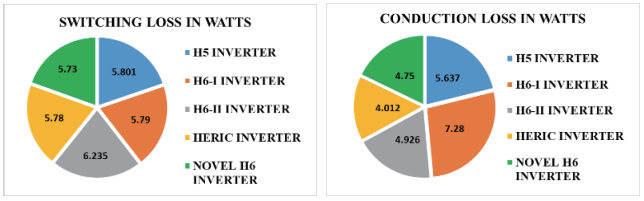
TABLE II
COMPARATIVE ANALYSIS OF TLI

Inverter	H5	H6-I	H6-II	HERIC	Novel H6
Number of switches	5	6	6	6	6
Decoupling	DC	DC	DC	AC	DC
Leakage current (mA) [20]	26.5	31.4	25.4	16.4	19.7
Switching loss (watts)	5.801	5.79	6.235	5.78	5.73
Conduction loss (watts)	5.637	7.28	4.926	4.012	4.75
% efficiency	99.03	98.94	98.98	99.13	99.09

VI. COMPARATIVE ANALYSIS

Table II represents the comparison between various inverters and proposed inverter in terms of number of switches, coupling method used, leakage current, switching loss, conduction loss and efficiency.

The efficiency analysis is obtained by determining the inverter topology losses in MATLAB/Simulink [20]. This technique is suitable for calculation of losses for comparison purpose. Leakage current is obtained from the OPAL RT output [20]. Figs. 16(a) and 16(b) depicts the switching loss and conduction loss respectively in the various TLI with reference current of 10 A. Fig. 17 represents the efficiency of various TLI. It is observed that the conduction loss generated by HERIC inverter



(a) (b)

Fig. 16. (a) Switching losses of TLI, (b) Conduction losses of TLI.

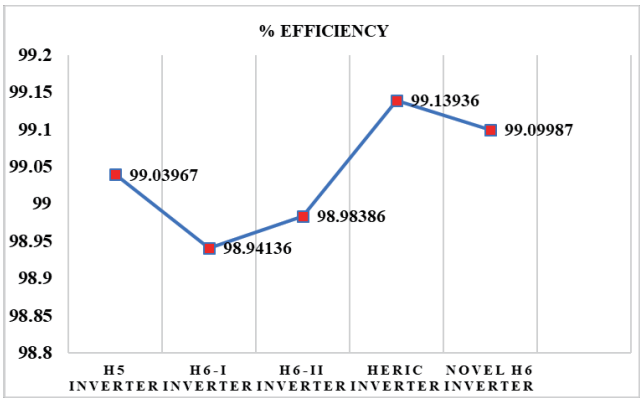


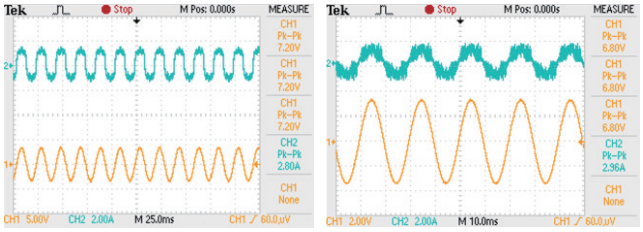
Fig. 17. % efficiency of various TLI.

is 4.01 watts and is least among all the inverters, followed by Novel H6 inverter with a conduction loss of 4.75 watts. Also HERIC inverter has highest efficiency of 99.139% followed by Novel H6 inverter with an efficiency of 99.099%. Figs. 18(a) and 18(b) represents the grid current and grid voltage of H5 and Novel H6 inverter respectively. The total harmonic distortion (THD) of grid voltage for H5 inverter is 5.04% whereas for Novel H6 inverter is found to be 1.99%.

VII. Conclusion

This paper proposes the utilization of a Novel H6 inverter as a recommended solution for mitigating the CMC in PV system connected to the grid without transformer.

The novel H6 inverter succeeds in retaining CMV equivalent to $V_{pv}/2$. The inclusion of S_6, gives an alternate way for the current during the second half cycle of conduction mode. Thus recommended Novel H6 inverter eradicates CMC and also reduces the conduction losses despite the circuit having six switches. The findings from model testing and physical implementation signify the superiority of the recommended Novel H6 inverter in comparison with the conventional inverters considered. Notably, the Novel H6 inverter effectively suppresses the CMC, minimizes conduction losses and enhances overall efficiency. Based on these findings, it can be concluded that the Novel H6 stands out as a highly promising option for PV system connected to the grid. Its performance is deemed second only to the well-established HERIC inverter. The superiority of Novel H6 inverter in terms of CMC suppression, reduced conduction losses, and improved efficiency reinforces its potential as a favorable choice for integrating PV system into the grid.



(a) (b)

Fig. 18. (a) Grid current and grid voltage of H5 inverter, (b) Grid current and grid voltage of Novel H6 inverter.

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Aditi Atul Desai was born in Goa, India, in 1976. She completed B.E. and M.E. in Electrical Engineering from Goa College of Engineering, Goa, India in the year 1998 and 2014 respectively. She received Ph.D. degree in Electrical Engineering from National Institute of Technology, Goa in 2023. She is currently working as Assistant Professor at Goa College of Engineering since December 2010. Her research interest includes renewable energy sources and electrical machines.

Suresh Mikkili obtained his M.Tech. and Ph.D. degrees in Electrical Engineering from the National Institute of Technology, Rourkela in the years 2008 and 2013, correspondingly. He holds the position of Associate Professor in the Department of Electrical and Electronics Engineering at the National Institute of Technology Goa, India, starting from January 2013.

His research interest includes Smart Electric Grid, Electric vehicles, Grid connected/Stand-Alone PV systems, wireless power transfer, power quality issues, and applications of soft computing techniques. He has authored two books, one is published by CRC Press, Taylor & Francis Group, in August 2015 and the other is published by AICTE in 2024 respectively. He has published over 145 papers in prestigious international journals (SCI/SCI-E) and international conferences (Annual/Bi-Annual). He has executed three projects of worth 85 lakhs and executing one project (ANRF PAIR) of worth 100 crores (individual budget is 1.47 crores). He is among the top 2% of scientists worldwide, as reported by Stanford University and Elsevier, for the year 2025.