A Graph-Based Layout Automation Approach for Three-Level SiC Power Modules Considering Complex Mutual-Inductance

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***Abstract*—This paper addresses the challenges of automatically designing low-inductance, compact three-level SiC power modules. The graph-based layout design automation method has the merit of seeking all possible solutions but may result in a significant calculation burden when considering complex mutual-inductance influences. To overcome this limitation, an efficient analytical method is developed to calculate parasitic inductance with mutual-inductance effects considered. Comparisons with numerical and experimental results prove the efficacy and accuracy of the proposed analytical method. A graph-based layout automation approach is developed, enabling multi-objective optimization of parasitic inductance and module footprint by incorporating mutual inductance. The method is applied to a three-level SiC module featuring six chips (four MOSFETs and two diodes). Pareto front solutions are analyzed to identify optimal trade-offs between inductance and compactness, demonstrating the effectiveness of the proposed methodology in enhancing design efficiency and performance for high-efficiency power electronics applications.**

***Index Terms*—Compact, graph method, layout design, low parasitic inductance, mutual-inductance, three-level SiC power module.**

I. Introduction

SILICON Carbide (SiC) devices are renowned for their exceptional performance, characterized by rapid switching speeds, minimal losses, superior thermal conductivity, and high-temperature tolerance [1]–[2]. In the realm of SiC power module design, the three-level topology has become a pivotal trend as it can effectively alleviate the voltage stress on switching devices while simultaneously reducing the harmonic content and electromagnetic interference (EMI) in the output [3]–[4]. When combined with the inherently low switching losses of SiC devices, three-level modules are capable of enhancing systems' reliability and power density, particularly at high frequencies [5]–[6].

With the growing complexity of three-level SiC module structures, pursuing low parasitic inductance in layout design has become a vital focal point [7]–[8]. Large parasitic inductance not only introduces delays in current transmission but also exacerbates switching losses, undermining the systems' overall efficiencies [9]. In response to the low-inductance needs, various approaches and layouts have been proposed. [10] introduced an improved vertical power loop architecture specifically tailored for a three-level T-type module, achieving a remarkable reduction in current commutation loop (CCL) inductance to 4.5 nH. [11] utilized a stacked substrate configuration to effectively minimize the CCL's parasitic inductance.

As the number of chips in parallel increases, it is hard to achieve such a remarkable reduction in CCL's parasitic inductance because conventional layout designs are usually limited by the designers' engineering expertise. Therefore, automated layout design methodologies have increasingly attracted extensive research attention [12]–[13]. [14] introduced an innovative automatic layout method that utilizes sequences. In this approach, the layout structure of the module is characterized by a genetic string, which serves as the foundation for subsequent optimizations. [15] advanced this field by developing a graph-based automatic layout method, and the effective tool, PowerSynth, was developed based on the achievements. [16] expanded the method by enabling the automated generation of templates, proving that the method can seek every possible layout solution.

However, the vast search space of the graph-based approach, which is capable of traversing all possible solutions, on the contrary poses a substantial challenge to the layout automation efficiency, especially for three-level modules with complex current paths. Therefore, it is essential to establish an efficient and precise inductance computation method that considers mutual inductance effects and develops layout design automation based on this computation methodology.

In this regard, this paper presents an innovative analytical method for calculating parasitic inductance in power modules, with mutual inductance effects considered. This method is validated through simulations on typical copper traces, de-

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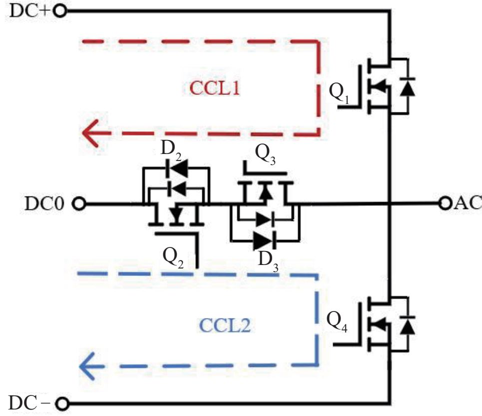

Fig. 1. Typical T-type circuit of a three-level SiC module.

TABLE I
OUTPUT VOLTAGE WITH DIFFERENT SWITCH CONDITIONS

Q_1	Q_2	Q_3	Q_4	Output
on	on	off	off	$+V_{DC}/2$
off	on	on	off	0
off	off	on	on	$-V_{DC}/2$

monstrating its accuracy. A design automation method is introduced, utilizing a graphical connection diagram technique to generate compact and low-inductance layouts. The Pareto front is determined using NSGA-II, an algorithm for multi-objective optimization, to balance inductance and module size. Comparative simulations highlight the method's superiority over existing techniques. The findings contribute to advancing power electronics for high-efficiency applications.

II. Parasitic Inductance Evaluation Method Considering Mutual-Inductance Effects

A. Three-Level Module Structure and Its Parasitic Inductance Characteristics

The three-level SiC power module divides the DC voltage into three voltage levels: $+V_{DC}/2$, 0, and $-V_{DC}/2$, and introduces a neutral point potential. This design produces higher-quality voltage waveforms at the output, effectively reducing the harmonic content and improving power conversion efficiency. A typical three-level SiC power module, as shown in Fig. 1, adopts a T-type topology. The main circuit is composed of four SiC MOSFETs (Q_1, Q_2, Q_3, and Q_4).

To achieve three-level output, different power devices need to be alternately turned on according to specific switching patterns, as shown in Table I. In order to reduce reverse recovery losses, as shown in Fig. 1, external diodes (D_2 and D_3) are introduced. These external diodes have a shorter reverse recovery time, allowing the current to preferentially flow through them during the switching of power devices. As D_2 and D_3 are introduced, the current flow paths in the three-level SiC power module become more complex, with two main CCLs: CCL1 and CCL2, also shown in Fig. 1.

B. Proposed Parasitic Inductance Evaluation Method

In the three-level SiC power module, the current paths of the CCLs are highly complex. During the switching of the devices, the direction of the current undergoes significant reversals, especially during the transitions when multiple devices are turned on or off simultaneously. This reversal phenomenon causes substantial changes in the distribution of magnetic flux enclosed by the current paths, posing a significant challenge to the accurate calculation of parasitic inductance.

Currently, the calculation of parasitic inductance in power devices mainly relies on two approaches: numerical simulation and analytical modeling. Numerical methods can accurately and directly solve for parasitic inductance in complex conduction structures but are computationally intensive. This makes them less suitable for layout automation processes that require thousands or even more iterations. For example, with a population size of 50, and iterating for 1,000 steps for convergence, 50,000 calculations would be needed during the automatic design. Therefore, analytical modeling, in contrast, is advantageous for layout automation applications, as it offers very high efficiency. However, for three-level SiC power modules with complex CCL paths, it remains a key challenge in keeping the balance between the accuracy and efficiency of analytical analyses of parasitic inductance, with mutual inductance effects considered.

To address this issue, this paper proposes a segmented analytical calculation method for self-inductance and mutual-inductance, as shown in Fig. 2. The method can be divided into two levels. The first level uses the connection points between the chips and the copper conductive layer, specifically the bonding wire connection points, as natural segmentation locations. The second level further divides the paths based on the changes of current flow directions. After each path segment is divided, the self-inductance and mutual-inductance of each segment can be calculated based on the physical dimensions of the copper traces. Finally, the overall parasitic inductance is calculated by summing up all the self- and mutual-inductance.

For self-inductance of each copper trace segment, taken segment i shown in Fig. 3(a) as an example, the value can be modeled by [17]:

$$L_i = \frac{\mu l_i}{2\pi}\left(\ln\frac{2l_i}{g_i} - 1\right) \tag{1}$$

where L_i is the self-inductance of segment i, μ is the permeability, and l_i and g_i are the length and equivalent diameter of segment i, respectively. g_i can be formulated as [17]:

$$\ln g_i = \frac{w_i^2 \ln w_i + h^2 \ln h + w_i h \ln\left(w_i^2 + h^2\right)}{\left(w_i + h\right)^2} + \frac{h\,\mathrm{arctg}\dfrac{w_i}{h} + w_i\,\mathrm{arctg}\dfrac{h}{w_i}}{\left(w_i + h\right)} - \frac{3}{2} \tag{2}$$

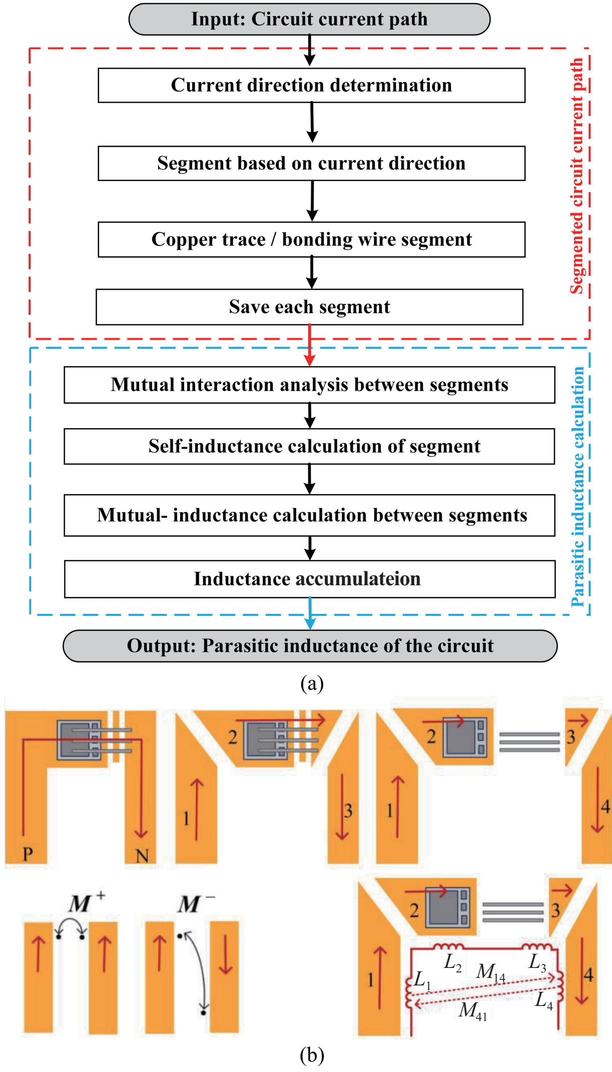

Fig. 2. Segmentation method for analytical modeling of parasitic inductance. (a) Calculation process, (b) Illustration on segmentation.

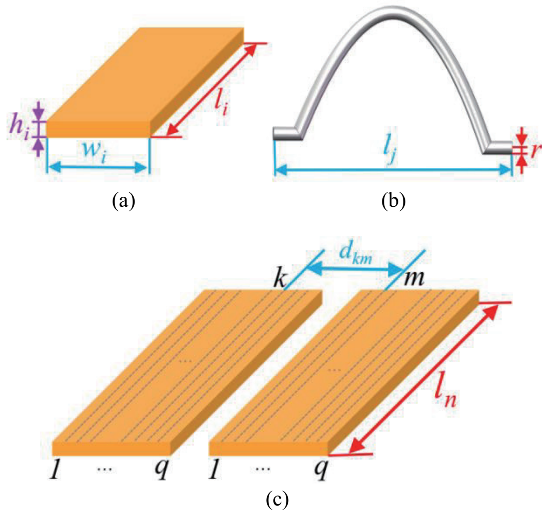

Fig. 3. Illustration on structural parameters of each segment. (a) A typical copper trace segment *i*, (b) A typical bonding wire *j*, (c) Mutual interaction between current branches *k* and *m*.

where w_i is the width of segment *i*, and *h* is the thickness of segment.

For bonding wire segments, taking a bonding wire *j* in segment *u*, as shown in Fig. 3(b), as an example, its self-inductance can be modeled by [18]–[19]:

$$L_j = \frac{\mu l_j}{2\pi}\left(\ln\frac{2l_j}{r} - 1\right) \tag{3}$$

where L_j is the self-inductance of bonding wire *j*, l_j is its length, μ is the permeability, and *r* is the radius of the bonding wire. When a total of *N* bonding wires are connected in parallel, mutual inductance arises between any pair of wires, and its value can be expressed as (between the *a*-th and *b*-th wires, assuming their lengths are both l_j) [18]–[20]:

$$M_{ab} = \frac{\mu_0 l_j}{2\pi}\ln\left(\frac{d+\sqrt{d^2+l_j^2}}{l_j}\right) \tag{4}$$

where *d* is the distance between wires *a* and *b*. The overall inductance for the bonding wire segment *u* can be formulated as [18]–[20]:

$$L_u = \frac{1}{N^2}\left(\sum_{j=1}^{N} L_j + \sum_{1\leqslant a,b\leqslant N,\ a\neq b} M_{ab}\right) \tag{5}$$

For the mutual-inductance between different segments, especially between two copper trace segments, as shown in Fig. 3(c), the values are formulated based on the current branch theory [21]:

$$M_{no} = \frac{1}{q^2}\sum_{1\leqslant k,m\leqslant q,\ k\neq m} M_{km} \tag{6}$$

where M_{no} is the total mutual inductance between segment *n* and segment *o*, M_{km} is the mutual inductance between current filament *k* and current filament *m*, and *q* is the number of current filaments.

The overall inductance can then be obtained by:

$$L_{\text{loop}} = \sum_{i=1}^{p} L_i + \sum_{1\leqslant n,o\leqslant p,\ n\neq o} M_{no} + \sum_{j=1}^{t} L_j \tag{7}$$

where L_{loop} is the total inductance of the circuit, L_i is the self-inductance of segment *i*, M_{no} is the total mutual inductance between segment *n* and segment *o*, L_j is the self-inductance of bonding wire *j*, *p* is the number of segments in the circuit, and *t* is the number of bonding wires.

C. Typical Structure Analyses and Comparisons

To verify the inductance segmentation method, the parasitic inductance of three typical structures (L-shape-bend, Z-shape-bend, and U-shape-bend, as shown in Fig. 4) is calculated and compared with the simulation results obtained using both the partial element equivalent circuit (PEEC) and finite element method (FEM) calculations. Specifically, the L-shape-bend

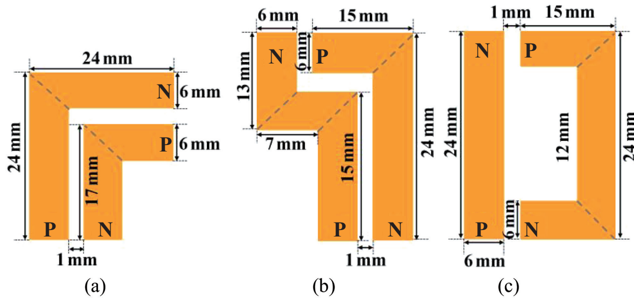

Fig. 4. Three typical copper trace structures. (a) L-shape-bend structure, (b) Z-shape-bend structure, (c) U-shape-bend structure.

structure consists of one bend in each of the two copper traces, the Z-shape-bend structure involves two bends in one trace and one bend in the other, and the U-shape-bend structure features no bend in one trace and two bends in the other. Since most copper trace bending structures can be considered combinations of these three typical structures, validating the accuracy of the proposed algorithm for these three sets of structures can indirectly prove the effectiveness of the proposed method.

The inductance calculated based on the proposed segmentation method and that by FEM and PEEC simulations are compared in Table II. The comparison proves that the proposed methodology can accurately simulate the parasitic inductance (with the largest error of $< 7\%$) while saving effectively the calculation time (by more than 89%). Therefore, the proposed approach is very suitable to be utilized in iterative design automation for modules' layouts.

D. Experimental Validation

To validate the accuracy of the proposed analytical method, a testing sample is fabricated, as depicted in Fig. 5(a). The parasitic inductance of the sample are subsequently measured using the impedance analyzer illustrated in Fig. 5(b). In order to explore the varying mutual inductance interactions, the testing process involved analyzing the scenarios where the positive (P) and negative (N) terminals are connected at different positions. Specifically, case 1 corresponds to the configuration where the P and N terminals are situated on opposite sides, as depicted in Fig. 5(c), whereas case 2 represents the configuration where the two terminals placed on the same side, as shown in Fig. 5(d).

Table III provides a comprehensive comparison of the analytical, PEEC, FEM, and experimentally testes results for the parasitic inductance in the two cases. As evident from the table, the overall parasitic inductance in case 2 is significantly lower than that in case 1. This discrepancy arises from the distinct mutual inductance interactions: mutual inductance superposition occurs in case 1, while mutual inductance cancellation takes place in case 2. Moreover, the analytical computation results demonstrate remarkable accuracy in both two cases, thereby effectively validating the precision of the analytical method in calculating parasitic inductance when different mutual inductance effects are considered.

III. Graph-Based, Multi-Objective Layout Automation Methodology

Given the complex internal electrical connections and numerous constraints within three-level SiC modules, directly designing an overall automatic layout is challenging, as it is difficult to simultaneously consider key factors such as parasitic inductance, mutual inductance, and footprint. This paper proposes a graph-based, multi-stage, multi-objective automatic layout design method, aiming to achieve an optimal balance between the key objectives of CCL inductance and footprint. The overall process is illustrated in Fig. 6.

The layout optimization process is divided into three progressive stages as follows:

Stage I: Initial Layout Generation

Initially, based on the circuit topology, a graph-based method is employed to construct the internal electrical connections within the module, ensuring electrical connectivity. Components are assigned node numbers, with types and size constraints clearly marked, forming an electrical connection netlist. The spatial layout and connection paths of the module are represented using an orthogonal grid graph. As shown in Table III, physical components (4 switches, 2 diodes, and 4 power terminals) are characterized as nodes, with adjacent electrical connections represented as edges. Node rules dictate that switches and diode chips, along with their copper layers, are represented by two nodes, with the bond wires between nodes defined as edges. Power terminals and their associated paths are represented by a single node. In addition, to ensure the terminal locations are physically reasonable and to keep the layout-search problem computationally tractable, the layout constraint is set such that power terminals are fixed at the grid edges, while other nodes are randomly distributed.

After placing the component nodes, a depth-first search (DFS) algorithm is used to recursively search for all possible current paths, generating a set of candidate paths (including path sequences, lengths, and turning points). A path planning algorithm selects paths with lower parasitic inductance that meet layout constraints and are conflict-free. These paths are then set as routing unit nodes to further refine the grid connections, forming a rational initial layout template that lays the foundation for subsequent optimization stages. The specific process is illustrated in Fig. 7.

This approach integrates path optimization methods with initial layout generation, ensuring that both electrical connectivity and parasitic inductance are considered from the outset, thereby providing a more effective initial layout solution.

Stage II: Candidate Layout Screening

During the initial layout generation phase, a large number of layout templates with varying parasitic inductance and layout areas are produced. By defining trace sizes and calculating

TABLE II
COMPARISONS BETWEEN INDUCTANCE CALCULATION RESULTS OF TYPICAL STRUCTURES

Type		Proposed analytical model	PEEC simulation		FEM simulation	
			Result	Difference	Result	Difference
L-shape-bend structure	Inductance	12.96 nH	12.12 nH	6.48%	12.47 nH	3.78%
	Time	0.8 s	10 s	92.00%	31 s	97.42%
Z-shape-bend structure	Inductance	14.21 nH	13.40 nH	5.70%	14.03 nH	1.27%
	Time	1.5 s	13 s	88.46%	35 s	95.71%
U-shape-bend structure	Inductance	22.11 nH	20.71 nH	6.33%	20.59 nH	6.87%
	Time	1.2 s	11 s	89.09%	34 s	96.47%

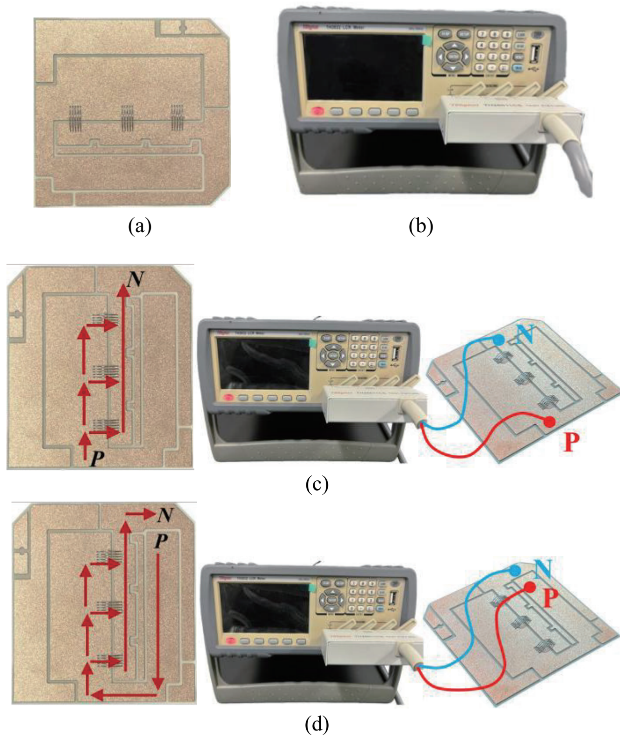

Fig. 5. Parasitic inductance testing platform. (a) Testing sample, (b) Impedance analyzer, (c) Testing case 1, (d) Testing case 2.

TABLE III
COMPARISONS BETWEEN INDUCTANCE OBTAINED BY DIFFERENT METHODS

Method	Case 1		Case 2	
	Value	Error	Value	Error
Test	13.56 nH		7.59 nH	
Analytical method	13.85 nH	2.14%	7.97 nH	5.01%
PEEC simulation	13.70 nH	1.03%	7.66 nH	0.92%
FEM analysis	14.03 nH	3.47%	7.68 nH	1.19%

parasitic inductance and layout area in segments, each layout's key performance indicators are determined. Using these two critical metrics as screening criteria, several candidate solutions

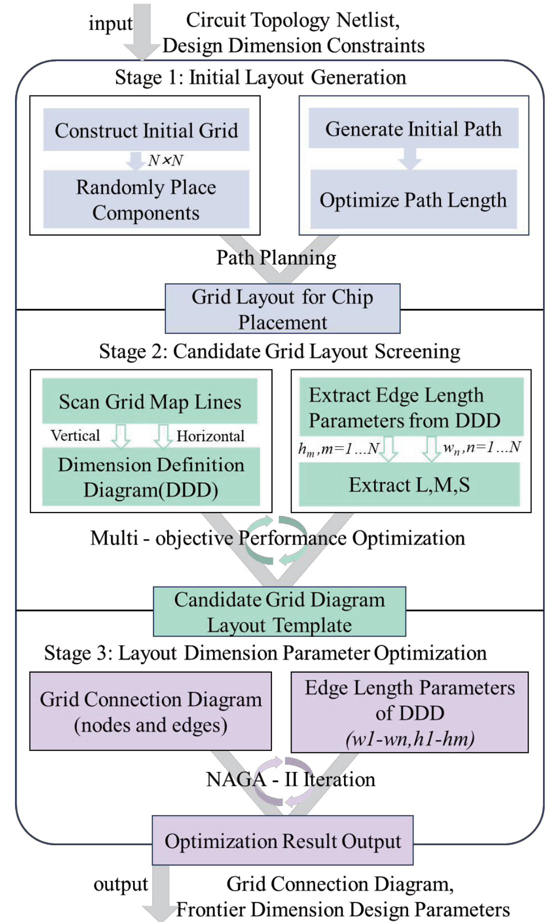

Fig. 6. Processes of the graph-based, multi-stage, multi-objective design automation method.

with lower parasitic inductance and more compact layouts are selected. This ensures preliminary optimization performance while providing high-quality input for subsequent template optimization.

Stage III: Layout Size Optimization

Based on the selected candidate layouts, a multi-objective iterative optimization of the layout templates is conducted using a combination of a graphical interface and the NSGA-II, with the parasitic inductance and footprint objectives as:

TABLE III
Graph Illustration of Different Components in Design

Type	Geometric layout and graphical representation	node attributes
Chip		Length Width Position
Diode		Length Width Position
Terminal		Length Width Position
Copper		Length Width Position

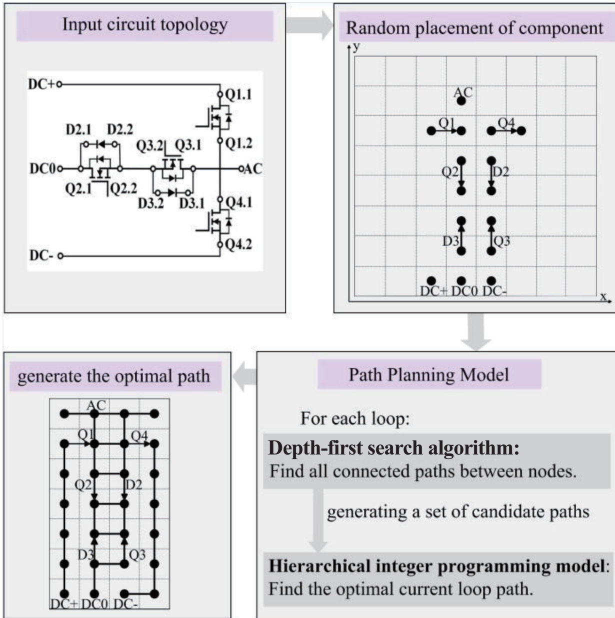

Fig. 7. Steps for generating the connections in stage I.

$$\min F = \begin{cases} L_{\text{loop}} = \max\left(L_{\text{loop1}}, L_{\text{loop2}}\right) \\ S \end{cases} \tag{8}$$

where L_{loop} is the maximum value between L_{loop1} and L_{loop2}. S is the layout area of the entire template.

By dynamically adjusting path widths and component distribution, parasitic inductance is reduced, and layout area is minimized, achieving a balanced enhancement of electrical performance and space utilization. Through a phased graphical modeling approach, this method effectively balances parasitic inductance and layout area while ensuring rational electrical connections, ultimately generating a high-performance three-level SiC module layout that meets design requirements. The phased design logic helps to gradually filter and refine the solutions, ensuring the optimization stability and effectiveness. The NSGA-II method is utilized to conduct optimizations with the CCL parasitic inductance and footprint as objectives.

TABLE III
Structural Parameters

Parameter	Value	Unit
Number of Switch Chips	4	--
Number of Diode Chips	2	--
Size of Switch Chip	6.30×4.80	mm
Size of Diode Chip	4.80×4.80	mm
Thickness of Copper Trace	0.30	mm
DBC Etching	0.70	mm
Welding Spacing	⩾1.00	mm
Size of Bonding Area	⩾1.00	mm
Copper Wire Width	⩾1.00	mm
Size of Power Terminal	⩾3.00×3.00	mm

IV. Module Layout Design and Analysis

A. Multi-Objective Layout Design

To validate the effectiveness of the proposed automation method, the layout of a typical T-type three-level SiC module is designed. The structural parameters are detailed in Table III.

Based on the parameters input, in stage I, a total of 1,309 valid grid connection diagrams are generated. Each of these diagrams satisfied the electrical connectivity requirements, with an average generation time of less than 10 s, which reflects a high level of efficiency. However, the results of the connection diagrams from the first stage are dispersed, with some outcomes being relatively distant from optimal solutions. Therefore, in stage II, a preliminary screening is conducted on the connection structures obtained from the former stage. The selected templates and their smallest layouts are shown in Fig. 8. Building on the results of the second stage, stage III employed the NSGA-II to perform multi-objective optimizations. The Pareto front is illustrated in Fig. 9. With the very efficient inductance computation method, it takes approximately 1.5 min to obtain the output Pareto front solutions, guaranteeing the design automation efficacy.

In Fig. 9, the closer a solution is to the lower left corner, the better it is considered, forming the Pareto front. As can be seen from the figure, the points on the Pareto front are occupied by the optimal three groups of layouts (E/C/D) output from stage II. Among them, Layout C with structural parameters in the Pareto front, as shown in Fig. 9, achieves a balance between parasitic inductance and footprint, which is the layout selected in this study.

The basic structure of the optimal design is illustrated in Fig. 10(a). Based on the optimized design, PEEC simulation model is established, as depicted in Fig. 10(b), for parasitic inductance calculations. The comparisons between the simulated results and that output by the analytical method are tabulated in Table IV. The table demonstrates that the optimized solution significantly outperforms the initial solution in terms of both parasitic inductance and footprint. Moreover, the parasitic

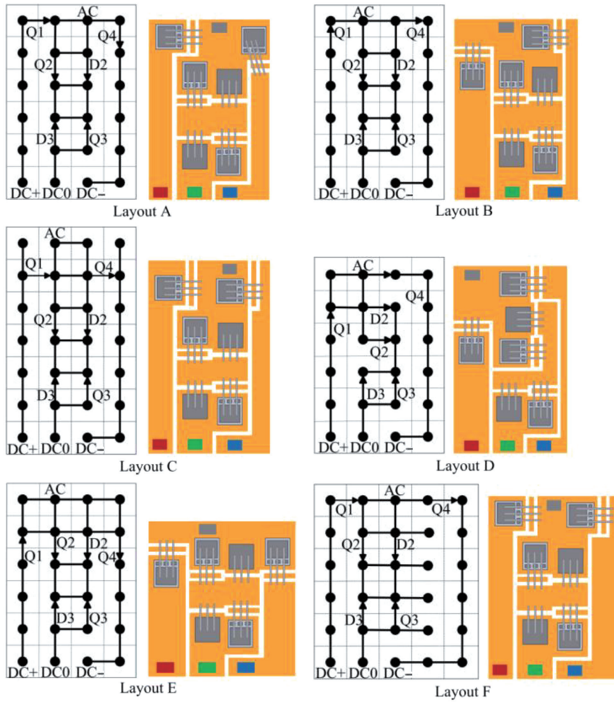

Fig. 8. Typical layouts output in stage II.

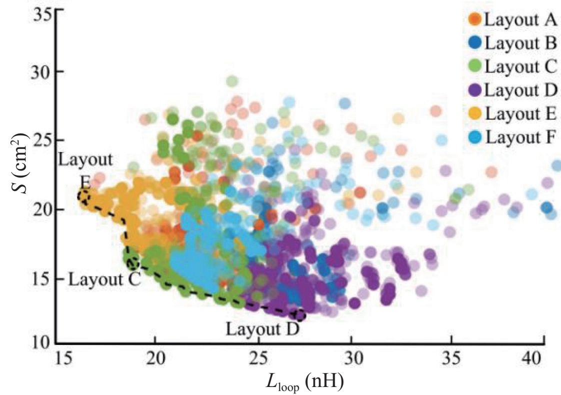

Fig. 9. Pareto front output in stage III.

inductance values output by the optimizer are close to those obtained from the PEEC simulations, thereby validating the effectiveness of the proposed method.

V. Conclusion

This paper proposes an efficient analytical method for calculating parasitic inductance of power modules that accounts for mutual inductance. Using this method, parasitic inductance values for three typical copper trace patterns are calculated and compared with PEEC simulated results to verify the efficiency. The accuracy is then validated by numerical simulations and experimental tests. By integrating the proposed inductance calculation method with a graph-based multi-objective layout design automation strategy, the layout design of a typical T-type three-level power module is completed, and the effectiveness of the approach is validated by comparing the results with

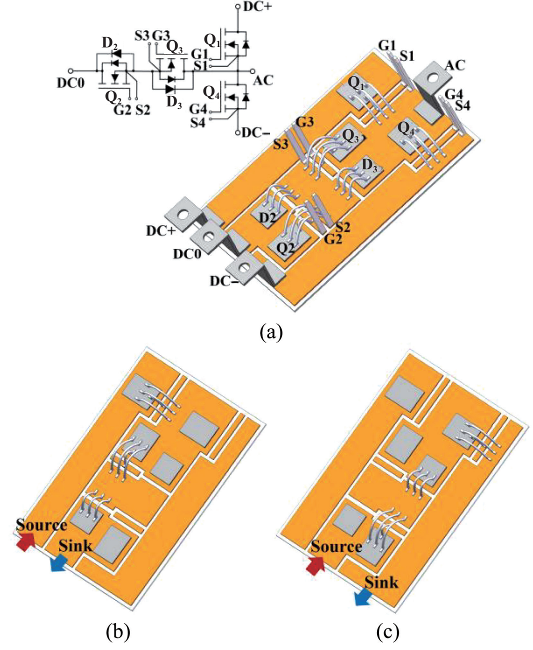

Fig. 10. Module layout structure and simulation models. (a) Module layout design, (b) Simulation model for current path from DC+ to DC0 (L_{oop1}), (c) Simulation model for current path from DC0 to DC− (L_{oop2}).

TABLE IV
Result Comparisons

Solution	L_{loop}			S
	Analytical	PEEC Simulation	Difference	
Initialized Structure	26.73 nH	25.14 nH	6.32%	18 cm^2
Optimized Solution: Layout C	19.60 nH	18.42 nH	6.41%	16 cm^2
Reduced	22.67%	26.73 %	—	11.12%

numerical ones.

Due to the complex current paths in multi-chip-paralleled modules, the proposed method has so far been utilized only on single-chip modules. Extending the approach to multi-chip layouts is feasible, however, and is currently under investigation.

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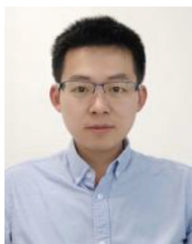

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