A New Single-Phase Switched Capacitor Based Five-Level Inverter With Double Gain for Grid-Tied PV Applications

Palakurthi RAVALI and Annamalai KIRUBAKARAN

***Abstract*—This paper presents a new single-phase, switched-capacitor-based five-level inverter with double voltage gain, designed for renewable energy applications. The topology utilizes switched capacitors (SCs) alongside a simple T-type converter and a half-bridge circuit with self-voltage balancing capability, eliminating the need for additional sensors to balance the capacitors. Furthermore, a midpoint clamping neutral is incorporated to reduce leakage current and common-mode voltage, making it particularly suitable for photovoltaic applications. A simple proportional-resonant (PR) controller is employed for grid current control, while a straightforward level-shifted pulse-width modulation (LS-PWM) technique generates the five-level output voltage waveform using two carrier signals, simplifying control complexity. An experimental setup is developed to validate the effectiveness of the proposed topology with *R* and *RL* loads under both steady-state and dynamic conditions, as well as grid-tied operation. Capacitor voltage balancing and the effect of the modulation index are also presented. Moreover, a hardware-in-the-loop (HIL) cosimulation is performed for grid control using Xilinx System Generator blocks in the MATLAB/Simulink environment, with the results provided. Additionally, a comprehensive comparison highlights the advantages of the proposed topology compared to recent solutions reported in the literature.**

***Index Terms*—FPGA, multilevel inverter, proportional-resonant controller, pulse width modulation, switched capacitor, T-type inverter.**

I. Introduction

MULTILEVEL inverters are widely used due to their numerous advantages such as low harmonic distortion, reduced dv/dt, and superior power quality. There is a growing interest in multilevel inverters within both academia and industry, making them increasingly preferred over two-level inverters for medium and high-power applications. Multilevel inverters offer the advantage of using lower-rated devices, resulting in higher efficiency and reduced size compared to two-level inverters. Traditional inverter topologies, such as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) are widely utilized with the midpoint clamped NPC inverter being particularly favored for various industrial applications [1], [2]. However, challenges such as DC-link voltage balancing and the requirement for a larger number of clamping diodes in higher-level designs increase the system's component count and control complexity, leading to higher losses and reduced overall efficiency. On the other hand, an FC-based multilevel inverter requires a larger number of capacitors, which introduces challenges such as tracking capacitor voltages and managing the pre-charging process, making it more complex. The CHB topology addresses many of the limitations of NPC and FC-based multilevel inverters. However, it requires additional independent DC sources to achieve higher levels.

The advantages of multilevel inverters have recently been leveraged for low-power applications in renewable energy systems, such as fuel cells and photovoltaic systems [3], [4]. To overcome the limitations of conventional topologies, extensive research has been conducted on reduced-part-count multilevel inverters, featuring designs that enhance output voltage through front-end converters or switched-capacitor-based concepts. Switched-capacitor converters (SCCs) address the issue of sensor-based capacitor voltage balancing in conventional multilevel inverter systems (MLIs) while also improving DC-link utilization. Switched- capacitor MLIs (SC-MLIs) typically require only a single DC voltage source. Additionally, they offer excellent voltage boost capability and enable automatic capacitor voltage balancing without the need for auxiliary circuits. The self-balancing of capacitor voltages and the voltage-boosting functionality in SC-MLIs are typically achieved by alternating the capacitors' operation between parallel and series configurations. These approaches not only increase the output voltage but also reduce the voltage stress across switches, resulting in higher efficiency. Consequently, SC-MLIs present a highly advantageous solution for low-power renewable energy applications. In [4], an FC-based five-level inverter is introduced to tackle the leakage current issue in transformerless inverters. However, it requires twelve switches, and the complexity of capacitor voltage balancing adds to the control challenges.

In [5], a quasi-Z source based single-phase T-type five-level inverter with a voltage-boosting feature has been proposed. However, the output voltage is determined by the impedance

Manuscript received June 4, 2025; revised September 13, 2025; accepted October 12, 2025. Date of publication March 30, 2026; date of current version January 13, 2026. No funding was received to assist with the preparation of this manuscript. (*Corresponding author: Annamalai Kirubakaran*.)

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Digital Object Identifier 10.24295/CPSSTPEA.2025.00041

network of the inverter and its shoot-through period. A five-level boost inverter, utilizing ten switches and an FC with a mid-point-neutral clamping feature, is proposed in [6]. A five-level inverter with a reduced switch count of six switches and three capacitors, featuring a boosting capability, is presented in [7]. An alternative approach to minimizing the number of devices, using three DC sources, for five-level operation is proposed in [8]. This topology is modular and can be scaled to generate higher output voltage levels. In [9], a five-level T-type inverter with a dc-dc boost converter is proposed. However, the inverter remains buck in nature, with its output determined by the front-end boost converter. The topology presented in [10] combines the features of both the front-end boost converter and SC concept to generate a five-level output voltage waveform. A new SC-based topology is proposed in [11], capable of generating a five-level output voltage using only six power switches, one diode, and two SCs. However, the primary drawback of this topology is inability to boost the output voltage. Consequently, a higher-rated boost converter is needed to increase the input DC voltage compared to a topology with inherent voltage-boosting capability. In [12], a novel five-level inverter topology is introduced, designed to eliminate leakage current. However, this topology reduces DC bus utilization to 50%. This issue is effectively resolved in [13] with an FB-type topology, which employs an asymmetrical T-type structure to generate a five-level output. It can be observed that the aforementioned topologies require additional switches and front-end boost converters to achieve the desired output voltage. Additionally, the structure is neither unique nor compact and requires more passive components. This also raises concerns regarding the reliability of the inverter for grid- connected operations.

To address the limitations of additional DC sources and switches, this paper introduces a new single-phase five-level inverter designed for grid-connected renewable applications. This article presents a topology based on a T-type circuit and features double voltage gain, incorporating the concept of two SC. The proposed topology offers the following advantages:

1) Sensor-less and automatic voltage balancing of the SC.

2) Self voltage boosting capability without any use of front-end converter.

3) Reactive power capability.

4) Reduced TSV and high efficiency.

5) Simple reduced carrier pulse width modulation (PWM) technique is implemented.

Moreover, many industries are focusing on the implementation of control schemes in digital platforms using DSP or FPGA. To realize the outputs and reduce testing duration, high-end real-time simulators like the OPAL-RT controller, Typhoon HIL and dSPACE MicroLab Box are preferred by many researchers. To address these challenges, in this paper, a hardware-in-the-loop (HIL) co-simulation is performed using the low-cost Spartan-6 FPGA Xilinx System Generator (XSG) blocks in MATLAB software under grid-connected operation. The detailed description of the paper is as follows: Section II provides a comprehensive explanation of the proposed topology, detailing its five-level output voltage generation, capacitor self-balancing, loss analysis, device selection. Section III describes the simulation and experimental results for *R* and *RL* loads under both steady-state and dynamic conditions, as well as grid-tied operation. Furthermore, the procedure for implementing HIL co-simulation and the results under grid control mode are presented. Section IV offers a detailed comparison of various grid-connected five-level inverters to highlight the merits of the proposed topology. Finally, Section V concludes with the remarks.

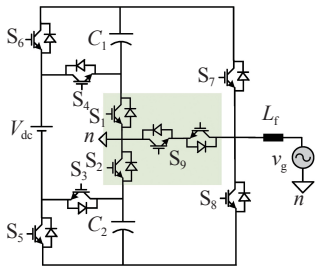


Fig. 1. Single-phase five-level inverter for grid-connected operation.

II. SC Based Five-Level Inverter

A. Proposed Topology

Fig. 1 presents the proposed topology of a new single-phase five-level inverter designed for grid-connected renewable energy applications [14]. The inverter incorporates a mid-point clamped T-type network and a single half-bridge circuit. Capacitors C_1 and C_2 function as SCs, eliminating the requirement of sensors or balancing circuits to manage their charging. This topology demonstrates self-balancing charging capability during the voltage level generation. Additionally, the structure is more compact and reliable compared to the topologies discussed in the previous section. For better clarity, the inverter's complete operation is divided into five modes as shown in Fig. 2, and is described as follows:

Mode 1: In this mode of operation, the positive maximum voltage $V_o = +2V_{dc}$ is obtained. As shown in Fig. 2(a), switches S_2, S_3, S_4 and S_7 are in conduction, and the resultant output voltage is the sum of both the DC voltage V_{dc} and the voltage across C_1.

Mode 2: In this mode of operation, half of the maximum output voltage $V_o = +V_{dc}$ is obtained. As shown in Fig. 2(b), S_2, S_3, S_6 and S_7 are in conduction. During this period, the output voltage is directly provided from the DC source. C_1 is charged to the DC input voltage $+V_{dc}$ by being connected across the source through the activation of S_1.

Mode 3: In this mode of operation, the output voltage generated is $V_o = 0$. As shown in Fig. 2(c), only the bidirectional switches S_9 is in conduction with the mid-point clamping neutral directly connected to the grid.

Mode 4: In this mode of operation, the resultant voltage is half of the negative maximum output voltage $V_o = -V_{dc}$. As shown in Fig. 2(d), S_1, S_4, S_5 and S_8 are in conduction and the output voltage is directly supplied from the DC source. During

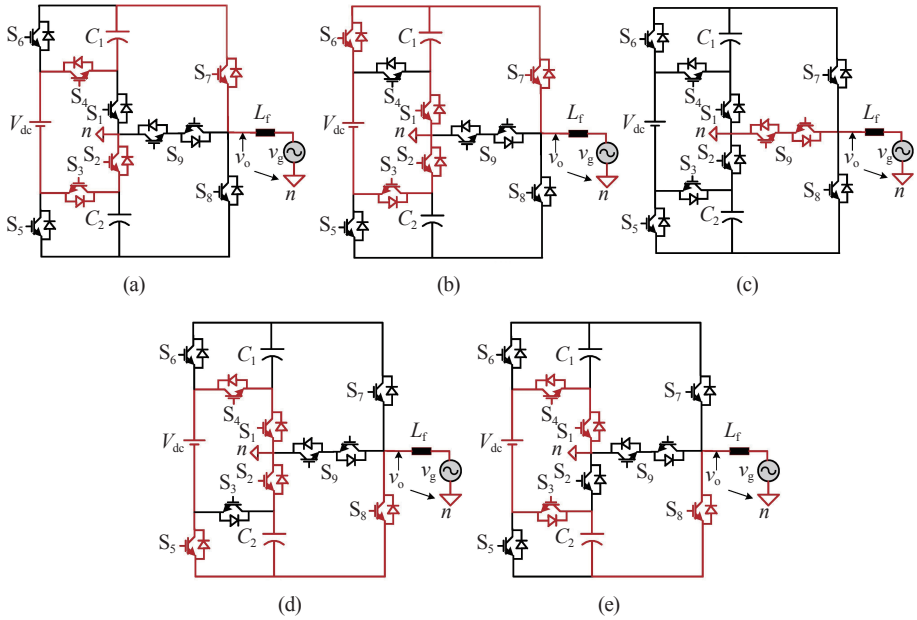


Fig. 2. Different modes of operation of five-level inverter. (a) $v_o = +2V_{dc}$, (b) $v_o = +V_{dc}$, (c) $v_o = 0$, (d) $v_o = -V_{dc}$, (e) $v_o = -2V_{dc}$.

TABLE I
SWITCHING SEQUENCE FOR FIVE-LEVEL OUTPUT VOLTAGE WAVEFORM

V_{out}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	C_1	C_2
$+2V_{dc}$	0	1	1	1	0	0	1	0	0	D	-
$+V_{dc}$	1	1	1	0	0	1	1	0	0	C	-
0	0	0	0	0	0	0	0	0	1	-	-
$-V_{dc}$	1	1	0	1	1	0	0	1	0	-	C
$-2V_{dc}$	1	0	1	1	0	0	0	1	0	-	D

this period, C_2 is charged to the DC input voltage $-V_{dc}$ by connecting it across the source through the activation of S_2.

Mode 5: In this mode of operation, the negative maximum voltage $V_o = -2V_{dc}$ is obtained. As shown in Fig. 2(e), S_1, S_3, S_4 and S_8 are in conduction and the output voltage is the sum of both the DC source $-V_{dc}$ and the capacitor voltage C_2.

B. Self-Voltage Balancing of the Capacitors

Self-voltage balancing is a process in which capacitors maintain their voltage without requiring external sensors or complex controllers. The principle behind this process is that, over a complete cycle, the charging and discharging durations remain equal, ensuring natural voltage balance. This balance is achieved when the average current over the cycle is zero. As a result, this approach simplifies circuit design while ensuring stable operation in multilevel inverters.

From Table I, it is observed that C_1 and C_2 charge during the V_{dc} and $-V_{dc}$ levels respectively and, discharge during the $+2V_{dc}$ and $-2V_{dc}$ levels, and remain unaffected during the zero voltage level.

The voltage variation across C_1 and C_2 during positive and negative half-cycles is shown in Fig. 2. The equivalent circuits of the proposed five-level inverter during charging and discharging modes are illustrated in Figs. 3 and 4.

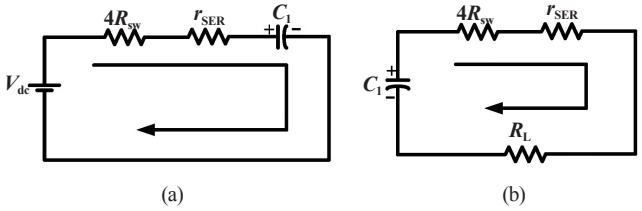


Fig. 3. Equivalent circuit of the inverter of C_1 during (a) charging and (b) discharging.

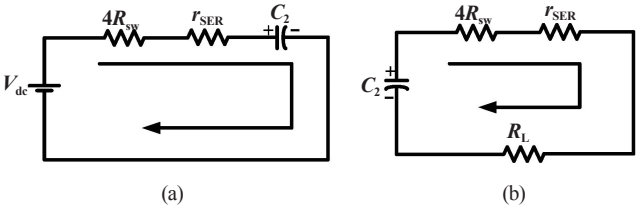


Fig. 4. Equivalent circuit of the inverter of C_2 during (a) charging and (b) discharging.

R_{sw} represents the forward resistance of the switch, r_{SER} is the equivalent resistance of capacitor, and R_L is the load resistance.

The voltage across SC in charging state can be expressed as

$$V_{Cn}(t) = V_{dc}(1 - e^{-t/\tau_c}) \tag{1}$$

where τ_c is the time constant during charging and the value of $\tau_c = R_{eq}C$.

R_{eq} is calculated by using

$$R_{eq} = 4R_{sw} + r_{SER} \tag{2}$$

The voltage across SC during discharging can be expressed as

$$V_{Cn}(t) = -V_{dc}e^{-t/\tau_c} \tag{3}$$

where $\tau_d = R_{eq}C$, $R_{eq} = 4R_{sw} + r_{SER} + R_L$, R_{eq} = equivalent resistance in the discharge mode.

C. Loss Analysis

The main sources of power losses in SC based converter designs originate from switches and capacitors and are primarily of three types: switching losses (P_{sw}), conduction losses (P_{con}) and ripple losses in the capacitors (P_{cap}) [15]. Switching and conduction losses occur in both the diodes and switches. In general, the losses in the switches include both switching and conduction losses. The total losses in a converter can be determined by summing the switching losses, conduction losses, and capacitor losses.

$$P_{losses} = P_{con} + P_{sw} + P_{cap} \tag{4}$$

Switching losses: Switching losses in a semiconductor switch represent the energy dissipated during transition between ON and OFF states. These losses occur due to the simultaneous presence of voltage and current during switching, impacting both power efficiency and thermal performance in the system. Switching losses are calculated using (5).

$$P_{sw} = f_{sw}\left(\frac{V_{on}i_{on}t_{on}}{6} + \frac{V_{off}i_{off}t_{off}}{6}\right) \tag{5}$$

where V_{on}, i_{on} is the voltage and current during turn on period respectively and t_{on} is the turn-on time. Similarly V_{off}, i_{off} is the voltage and current during turn off period respectively and t_{off} is the turn-off time.

Conduction losses: These losses result from the switch's internal resistance or voltage drop and play a significant role in determining the efficiency of power electronic converters. Conduction losses primarily occur when the switch is in the ON-state due to its internal resistance, causing I^2R losses, and the ON-state voltage drop, leading to power dissipation.

The conduction losses of the switch and the diode is calculated as

$$P_{con,\,s} = \sum_{x=1}^{n} (V_s + R_s i_{sx,\,rms}) i_{sx,\,rms} \tag{6}$$

$$P_{con,\,d} = \sum_{x=1}^{n} (V_D + R_D i_{dx,\,rms}) i_{dx,\,rms} \tag{7}$$

Here V_s and V_D represent the voltage drop across the switches and diodes during turn-on time, while R_s and R_D denote the internal resistance of the switches and diodes, respectively. Similarly, $i_{sx,\,rms}$ and $i_{dx,\,rms}$ represent the RMS current through the switches and diodes during operation.

Ripple losses: The current flowing through the capacitor during charging and discharging causes ripple losses, primarily due to its internal resistance. These losses can be calculated as (8) [15].

$$P_{cap} = \frac{1}{2} C f_{sw} \Delta V_C^2 \tag{8}$$

where C *i*s the capacitance and ΔV_C is the ripple voltage of the capacitor.

D. Component Selection

The equations used for the selection of capacitors and filter inductor are as follows:

Selection of C_1 and C_2 :

$$C = \left(\frac{\frac{P}{V_{dc}}}{2 \times \omega \times \Delta V_C}\right) \tag{9}$$

$P = 2$ kW, $V_{dc} = 200$ V, $\omega = 2\pi f$, $f = 50$ Hz, $V_C = 5\%$.

Let us consider the case where the power shared by the source and the capacitor is equal.

$$C = \left(\frac{\frac{1000}{200}}{2 \times 2 \times 3.14 \times 50 \times 0.05 \times 200}\right) = 796\ \mu\text{F}$$

$\therefore$ Smaller $\Delta V_C \Rightarrow$ Lower distortion.

C_1 and $C_2 = 1000$ μF.

Filter inductor L_g:

$P = 2$ kW, $V_{rms} = 230$ V, $V_{dc} = 400$ V, $f_{sw} = 5$ kHz

$$I_{rated} = \frac{P}{V_{rms}} = \frac{2000}{230} \approx 9\ \text{A} \tag{10}$$

A typical design allows 10% – 30% ripple at switching frequency. Let's choose 20%:

$$\Delta I = 0.2 \times I_{rated} = 0.2 \times 9 = 1.8\ \text{A}$$

$$L = \frac{V_{dc}}{4 \times f_{sw} \times \Delta I} \tag{11}$$

$$L = \frac{400}{4 \times 5000 \times 1.8} = 11.5\ \text{mH}$$

$\therefore$ $L \approx 10$ mH for inductor current rating of > 9 A.

E. Level-Shifted PWM

To generate the five-level output waveform, a simple reduced carrier PWM scheme is employed, as illustrated in Fig. 5. In this approach, two carrier signals are compared with a modulated waveform to determine the gating signals required to operate at levels: $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$, as illustrated in Fig. 2. The modulation waveform is a sine wave with its negative half-cycle inverted. Logic gates such as OR and AND are used to realize the five-level output voltage waveform and their implementation is very simple in digital platforms, which reduces control complexity—An added benefit of this work. The logic behind the generation of switching pulses using LS-PWM is shown in Fig. 6. Table I further illustrates the switching sequence required to produce the five-level output voltage waveform. In the table, a state of 0 indicates that a switch is off, while 1 indicates it is on. Importantly, in most operating modes, fewer than half of the total devices are in conduction, highlighting the topology's ability to achieve higher efficiency.

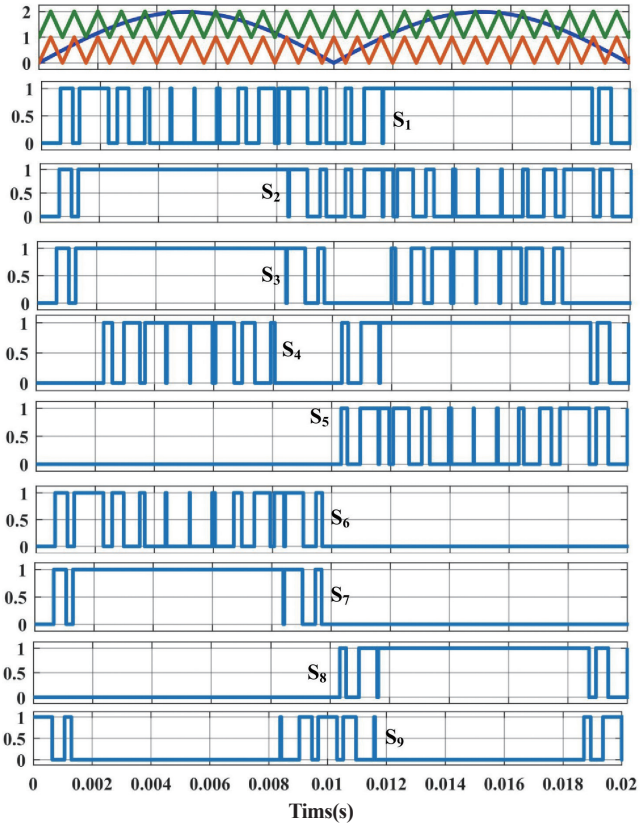


Fig. 5. LS-PWM and the switching signal for each device S_1 to S_9.

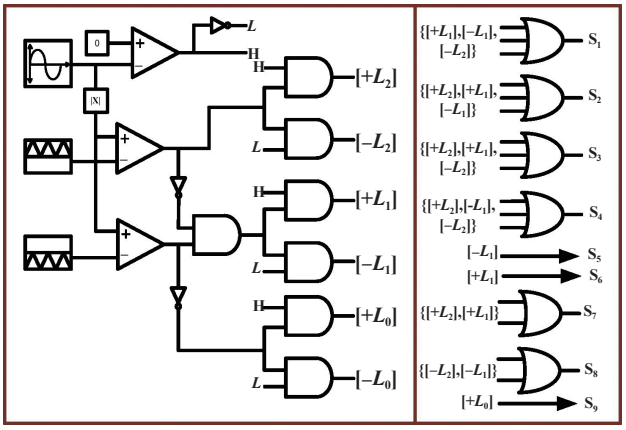


Fig. 6. Control logic for the proposed inverter.

In addition, the charging and discharging of the capacitor are self-balancing and do not need additional sensors, which reduces the overall cost—An added benefit of the SCs concept for multilevel operation.

F. PR Controller

Fig. 7 shows the schematic arrangement for implementing a simple PR controller under grid-connected operation. First and foremost, the grid voltage is passed through a phase-locked loop (PLL) implemented using a simple arc-tangent method to extract the angle for synchronization. The merit of this PLL is

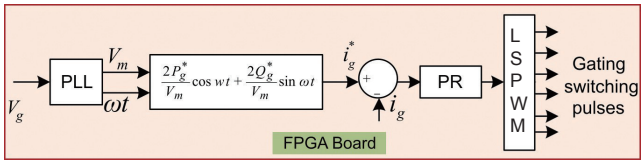


Fig. 7. Closed loop PR controller implementation.

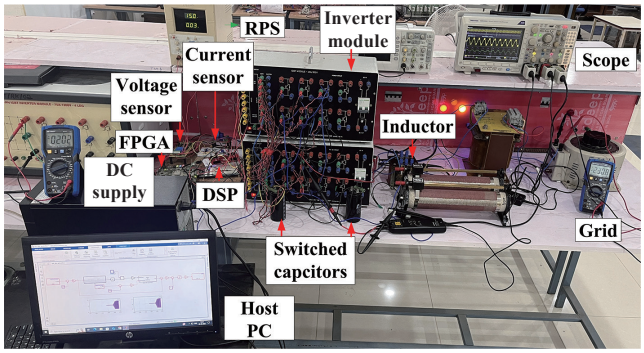


Fig. 8. Experimental setup.

that it does not require any inbuilt PI controllers and provides a quick response [16]. Using this information, the required reference current is generated as (12) given in the MATLAB function block.

$$i_g^* = \frac{2P_g^*}{V_m}\cos\omega t \pm \frac{2Q_g^*}{V_m}\sin\omega t \tag{12}$$

Further, the measured grid current is obtained using a current sensor and is compared to the reference current. The error is processed by the PR controller to generate the modulating waveform (M_a), as shown in Fig. 7. This waveform is then compared with two carrier signals and processed through logic gates to achieve the desired five-level output voltage waveform. In general, the PR controller offers the benefit of a fast transient response, and its tuning is performed according to the procedure detailed in [17].

III. Results and Analysis

A. Open Loop Response

In this section, the performance of the proposed topology is verified through both MATLAB simulation and experimental results. Fig. 8 shows the experimental setup developed in the laboratory. First, the proposed model is built using ten CT60 IGBT switches in the modules with an inbuilt gate driver. The 1000 μF, 500 V capacitors are placed as per the circuit configuration. The control logic is implemented using Xilinx System Generator with a low-cost Atlys Spartan-6 FPGA to generate the firing pulses for all the switching devices. Fig. 9 shows the developed control scheme using Xilinx blocks for the generation of firing pulses. The procedure for the implementation of Xilinx blocks and generation of firing pulses is detailed in [18]. To realize the five-level output voltage waveform for an input

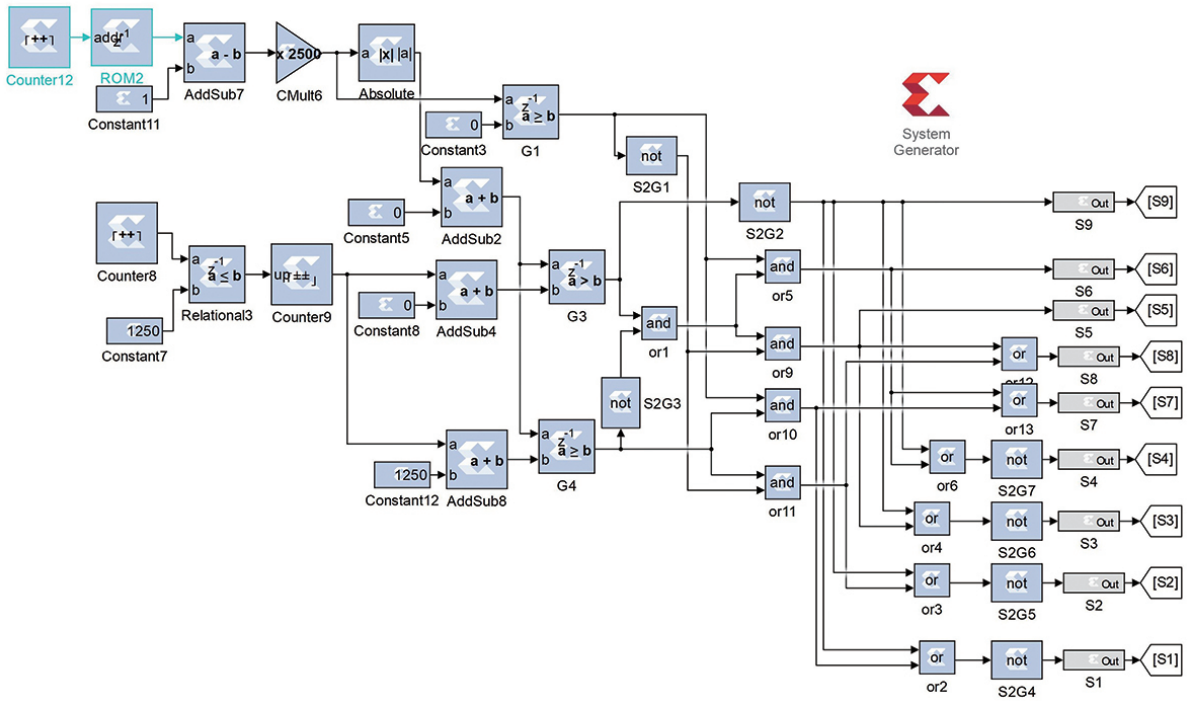


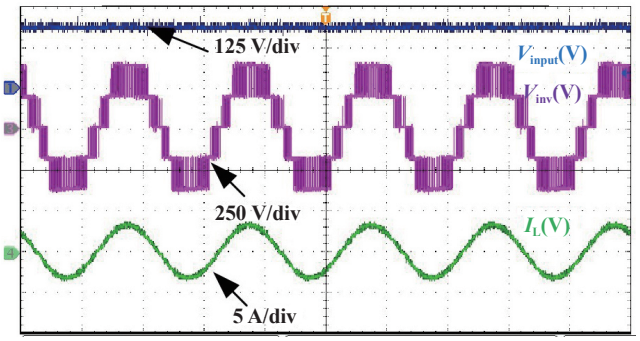
Fig. 9. Firing pulse generation using XSG blocks in Matlab.

TABLE II
SPECIFICATIONS

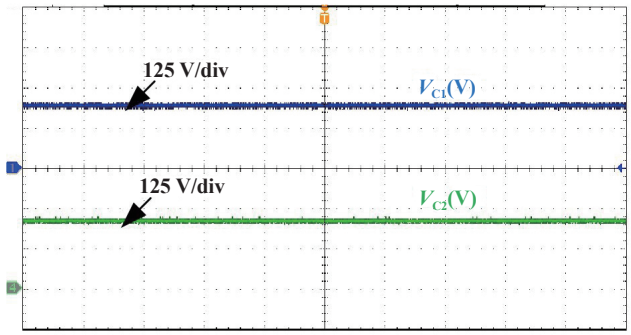
Parameters	Simulation	Experimentation
Input DC voltage	200 V	200 V
Output voltage	400 V	400 V
Grid voltage	230 V (RMS)	230 V (RMS)
Output power	2 kW	2 kW
Swtiches	IGBT	CT60
DC capacitors	1000 µF	1000 µF, 500V
FIlter inductor	10 mH	10 mH
Switching frequency	5 kHz	5 kHz
Fundamental frequency	50 Hz	50 Hz

of 200 V DC and output of 400 V AC, a modulation index of 1 is considered under open-loop operation. Switching frequency of 5 kHz and the fundamental frequency of 50 Hz is considered for the study. The responses of the proposed topology are recorded through a DLP850 Yokogawa ScopeCorder. The detailed specifications of both the simulation and experimental results are given in Table II.

Initially, the performance of the proposed topology was evaluated under varying load conditions, ranging from a 100 Ω resistive load to an *RL* load consisting of a 100 Ω resistor connected in series with a 10 mH inductor. Fig. 10(a) shows the measured waveforms of the DC source input voltage, inverter output voltage, and the corresponding load current. From Fig. 10(b), it can be observed that the DC voltage across C_1 and C_2 is charged to 200 V, equal to the DC source input voltage. This eliminates the need for additional sensors and



(a)



(b)

Fig. 10. Experimental results of (a) input DC voltage, inverter output voltage and load current, and (b) voltage across C_1 and C_2.

balancing circuits for the capacitors. The SC concept boosts the gain to two times, which is a significant advantage of the proposed topology.

Fig. 11 compares the response of the proposed five-level

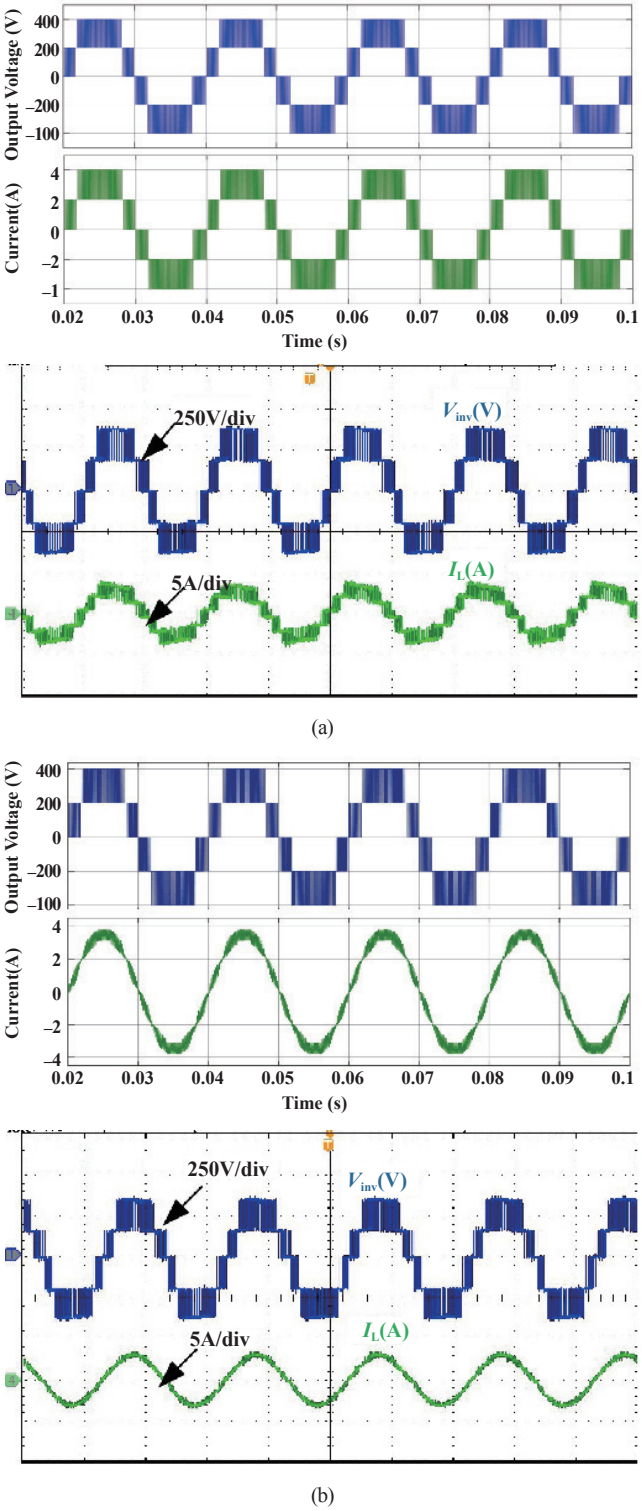


Fig. 11. Comparison of simulation (left) and experimental results (right) under (a) *R*-load and (b) *RL*-load.

inverter under *R* and *RL* loads for both simulation and experimental results. It can be observed that the patterns of both the output voltage and the corresponding load current remain consistent. Moreover, for an *RL* load, the inductor acts as a filter, smoothing the current waveform into a sinusoidal shape, which is evident in both simulation and experimentation. Additionally, the dynamics of the topology are tested for a load transition from *R* to *RL* at 0.06 s, as shown in Fig. 12. The results indicate that the pattern changes accordingly, with the simulation and experimental results closely matching.

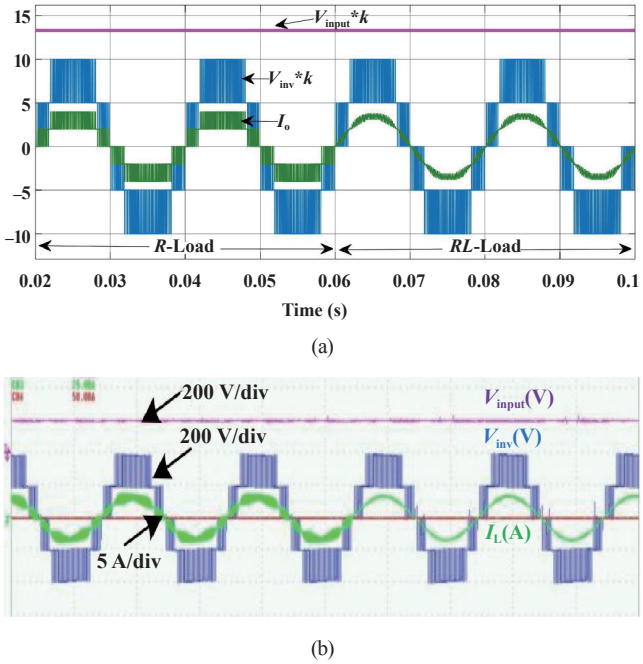


Fig. 12. Comparison of DC input, inverter output voltage and load current changes at *R* and *RL* loads. (a) Simulation results. (b) Experimental results.

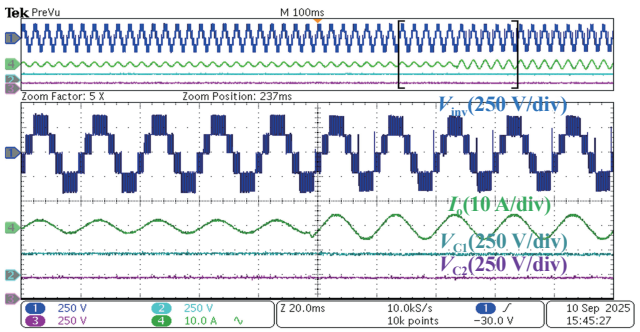


Fig. 13. Experimental results of voltage balancing during load changes.

Figs. 13 and 14 show the response of the inverter output voltage, load current, capacitor voltage, and current through the capacitor during transient conditions. It can be observed that the capacitor voltage remains constant while current flows through the capacitor during the $2V_{dc}$ level generation. This indicates that the charged capacitor is connected in series with the DC source to produce the $2V_{dc}$ level, and the magnitude of the rising current corresponds to the load current. This behavior is consistent for both capacitors during positive and negative level generations.

Additionally, the measured capacitor voltage ripples are shown in Fig. 15. A maximum ripple of 4 V is observed, which corresponds to 2% of the design voltage (200 V per capacitor) under an approximate load current of 2 A. Fig. 16 illustrates the cold start condition, where the voltage across the capacitor

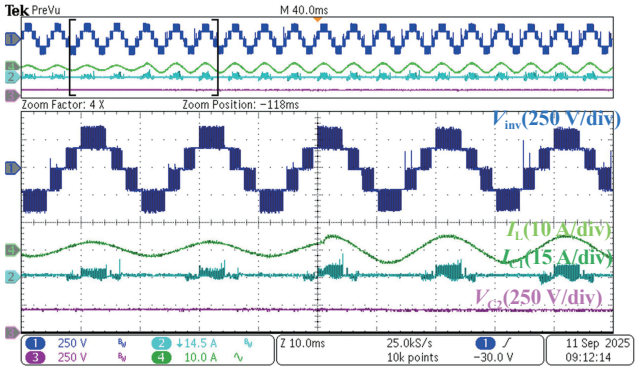


Fig. 14. Experimental waveforms of inverter output voltage, load current, capacitor current, and capacitor voltage during transient conditions.

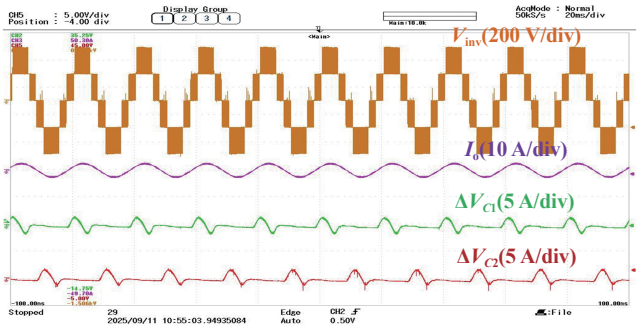


Fig. 15. Experimental results of inverter output voltage, load current, and voltage ripple across C_1 and C_2.

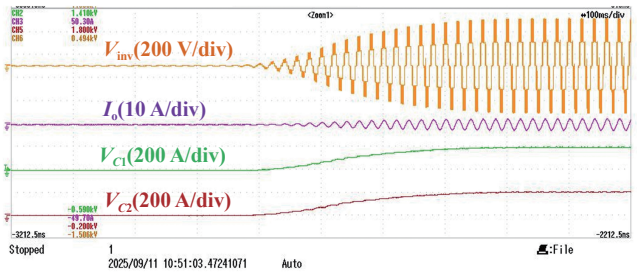


Fig. 16. Experimental waveforms during cold start with a 200 V input voltage.

rises due to switching. It is clearly seen that as the input voltage is applied, the five-level output voltage waveform is generated and the capacitor voltage charges to the 200 V DC input level. Moreover, the effect of modulation index changes from 0.45 to 0.95 is shown in Fig. 17. It is well known that as the modulation index varies, the output voltage level changes from three-level to five-level. Throughout this process, the transient response remains stable, and the capacitor voltage stays steady and equal to the 200 V DC input.

Furthermore, Fig. 18 illustrates the comparison of the measured voltage stress across the various switches for both simulation and experimentation. It can be observed that S_1 to S_6 experience a voltage level of 200 V, while the maximum voltage across S_7 and S_8 is 600 V, and S_9 is rated for a voltage of 400 V. Similar to the simulation, the experimental results and the pattern across the devices remain the same. This demonstrates that

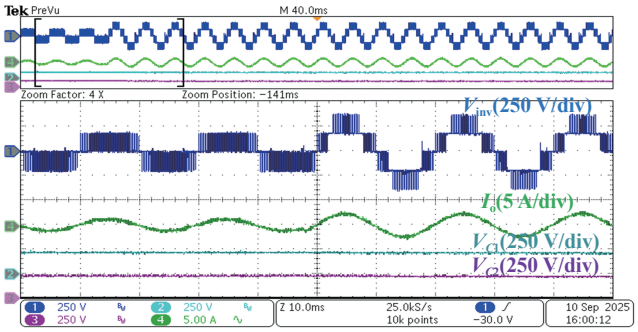
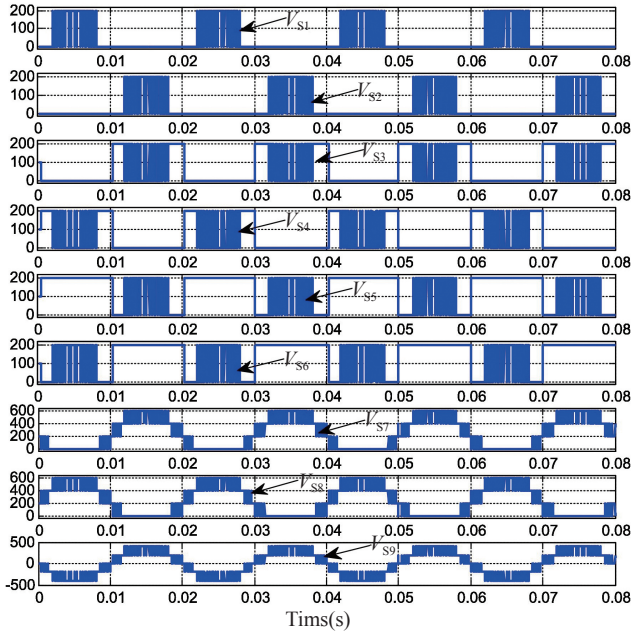
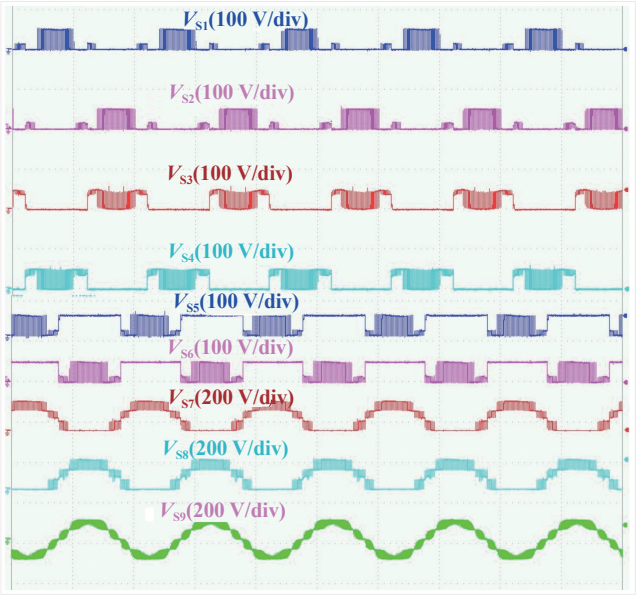


Fig. 17. Experimental waveforms with modulation index changes from 0.45 to 0.9.



(a)



(b)

Fig. 18. Voltage stress across the switches. (a) Simulation results, (b) Experimental results.

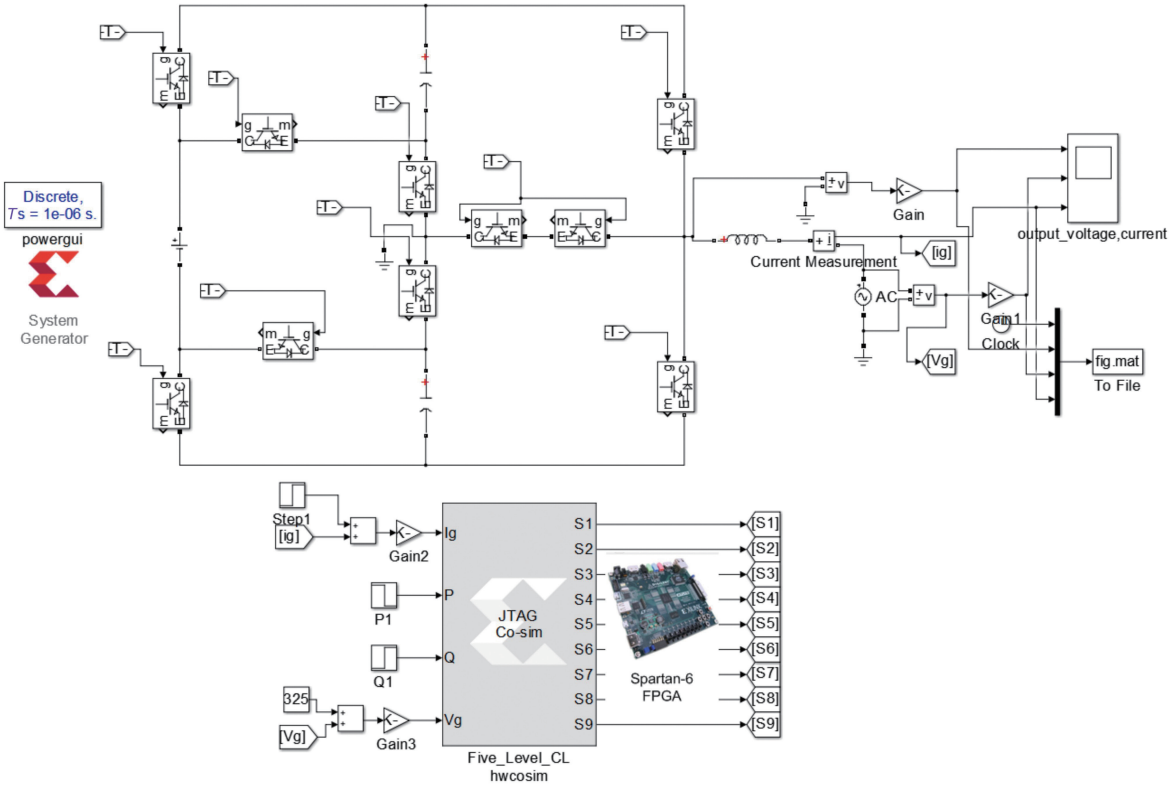


Fig. 19. HIL co-simulation circuit.

most of the switches operate at reduced stress, showcasing an advantage of the proposed topology.

B. HIL Co-Simulation: Grid Mode

Real-time testing of any electric circuit and control scheme is crucial before bringing them to the market. In general, hardware-in-the-loop (HIL) simulation is simple and offers a cost-effective solution. However, HIL systems based on OPAL-RT, Typhoon HIL, and similar platforms are very expensive. Therefore, this section presents an HIL co-simulation operation using a low-cost Atlys Spartan-6 FPGA board in grid-connected mode to evaluate the performance of the proposed topology. Fig. 19 shows the developed power circuit with HIL co-simulation blocks in the MATLAB environment. The HIL co-simulation block interfaces the Atlys board with the power circuit through the HS2 Joint Test Action Group (JTAG) interface.

In general, the clock frequency of the FPGA board is 100 MHz, which can be scaled down to the required frequency. The procedure for generating the carrier and sine waveforms using XSG blocks in MATLAB software is given in [18], [19]. To generate the sine waveform, a ROM block is used, while the carrier waveform is generated using counter and comparator blocks, as shown in Fig. 20. Here, the system clock frequency is scaled to the required value by combining the count value and the explicit period. Similarly, the complete control scheme is implemented using XSG blocks in MATLAB software.

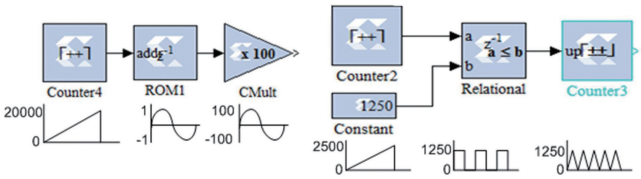


Fig. 20. Xilinx blocks for sinewave and triangular wave generation.

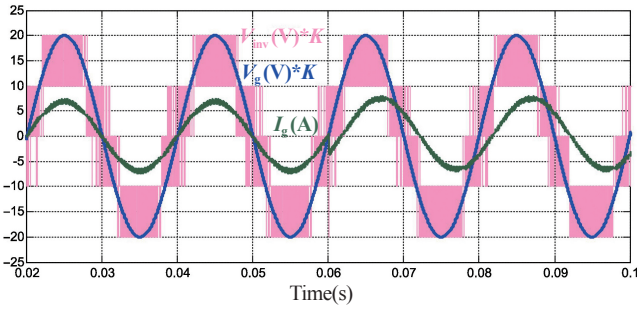
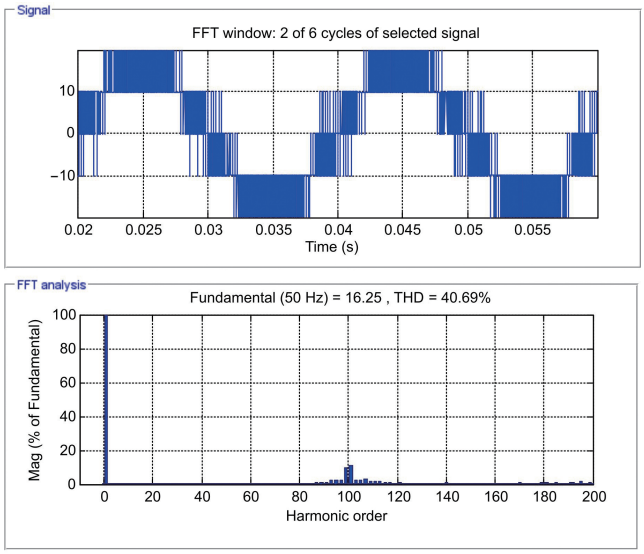


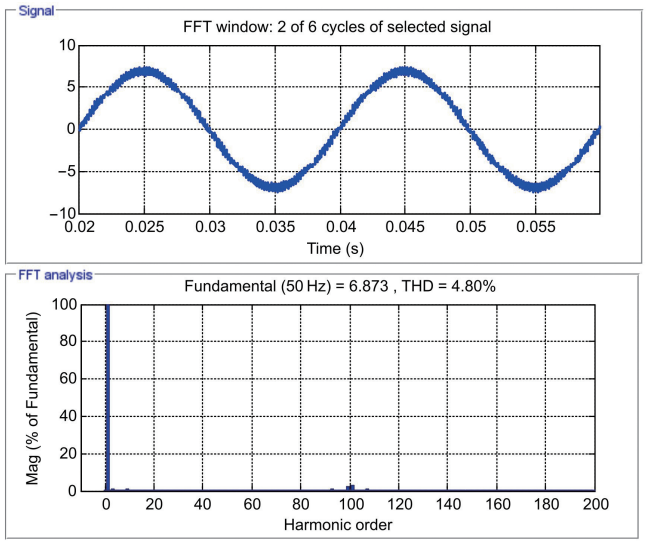
Fig. 21. Response of inverter output voltage, grid voltage and grid current.

$$f = \frac{f_{\text{systemclock}}}{\text{countvalue} \times \text{explicitperiod}} = \frac{100\,\text{MHz}}{2500 \times 20} = 2\,\text{kHz} \quad (13)$$

Fig. 19 displays the proposed five-level inverter with the HIL co-simulation circuit under grid-connected operation. Here, the grid voltage is fixed at 230 Vrms (i.e., 325 V peak) with 50 Hz frequency operation. Fig. 21 illustrates the measured waveforms of the five-level inverter output voltage, grid



(a)



(b)

Fig. 22. Frequency spectrum of (a) inverter output voltage and (b) grid current.

voltage, and their corresponding grid currents. To realize the magnitude of the voltages, they are scaled down to a lower value. It is evident that the inverter voltage, grid voltage, and injected current are in phase at unity power factor (UPF). At instant 0.06 s, the inverter provides reactive power support, and it can be observed that the grid current lags the voltage. However, the inverter output voltage and grid voltage remain synchronized. This demonstrates the effectiveness of the developed control scheme and shows that the PLL blocks perform well when using XSG blocks in HIL co-simulation mode at a lower cost.

Furthermore, Fig. 22 illustrates the frequency spectrum of both the inverter output voltage waveform and the grid current respectively. It can be observed that the total harmonic distortion (THD) of the grid current is around 4.8%, which is within the limits of IEEE 1547 standards.

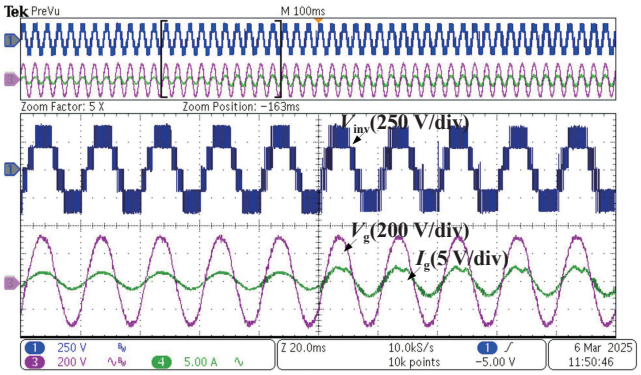


Fig. 23. Experimental results of inverter output voltage (V_{inv}), grid voltage (V_g), and grid current (I_g).

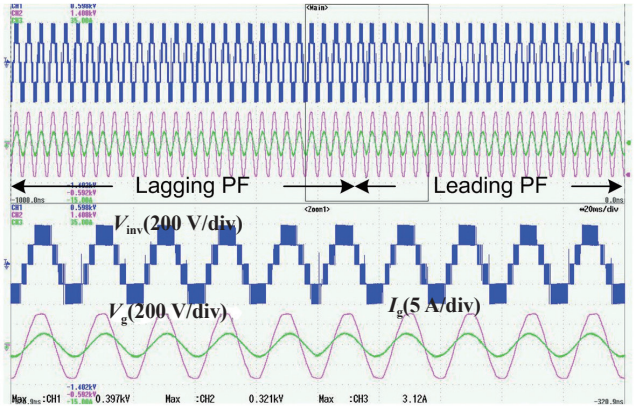
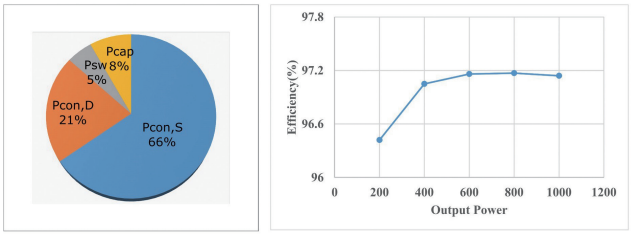


Fig. 24. Experimental results of the proposed inverter under dynamic conditions with the power factor changing from 0.9 lagging to 0.9 leading.



(a) (b)

Fig. 25. (a) Distribution of various power loss, (b) Efficiency curve.

To understand the feasibility of grid connection, the prototype model developed is tested experimentally under unity power factor conditions. The TI LaunchPad F28379 DSP controller is used for PR controller development, and the Spartan- 6 FPGA processor is used for level generation due to the limitations of the FPGA controller available in the laboratory. Fig. 23 depicts the experimental results of the inverter output voltage, grid voltage, and their corresponding injected current. Fig. 24 depicts the experimental results of the proposed inverter. Fig. 25 shows the distribution of various power loss and efficiency curves.

As shown in Fig. 23, it can be observed that both voltage and current are in phase, and the output current is increased from 2

TABLE III
COMPARISON OF VARIOUS GRID-CONNECTED FIVE-LEVEL INVERTERS

Components	CHB	[4]	[5]	[6]	[7]	[9]	[10]	[20]	[21]	Proposed
DC Sources	2	1	1	1	1	1	1	1	1	1
Switches	8	12	10	10	6	8	9	10	10	10
Divided capacitors	2	0	0	0	0	2	0	0	0	0
Capacitors	0	3	2	1	3	0	2	2	3	2
Inductors	0	0	1	0	0	0	1	0	0	0
Diodes(excluding body diodes)	0	0	4	2	2	0	1	1	0	0
Gate drivers	8	12	10	10	6	8	9	10	10	9
Max no. of switches in conduction	4	6	5	6	3	4	6	5	6	5
Total standing voltage	8	6.5	8	5	5.5	7	-	6.5	6	7
Reactive power capability	-	No	No	-	Yes	No	-	Yes	Yes	Yes
Gain	0.5	1	2	2	2	1	4	2	2	2
Capacitor balancing	-	No	-	-	No	No	No	No	Yes	Yes
Output voltage	Boost	Buck	Boost	Boost	Boost	Buck	Boost	Boost	Boost	Boost
Efficiency/%	96.5	96.7	96	-	98.1	-	-	97.35	98	97.2

A to 4 A (peak-to-peak) while maintaining 400 V at the inverter output. This demonstrates that the developed topology performs well for grid integration. Next, the proposed topology is tested under dynamic conditions, with the power factor changing from 0.9 lagging to 0.9 leading as shown in Fig. 24. It can be observed that despite the change in power factor, the magnitude of the current remains the same. The current smoothly transitions from a lagging to a leading position relative to the grid voltage.

Additionally, efficiency is a critical factor for all power electronic converters in promoting the proposed topology. Hence, in this work, a loss analysis is carried out, as discussed in the previous section, considering switching losses, conduction losses, and capacitor ripple losses. The proposed topology achieves a maximum efficiency of 97.2% compared to the 96.5% efficiency of the CHB inverter at a 5 kHz switching frequency and 1 kW rated power. Finally, it is evident that the proposed SC inverter operates in boost mode with a double voltage gain, further highlighting its superior performance and efficiency.

IV. COMPARATIVE ANALYSIS

In this section, a detailed comparison of various grid-connected five-level inverter topologies is conducted to demonstrate the merits of the proposed topology. Table III presents a comparison of the proposed topology against well-established five-level inverters such as CHB, and other recently proposed five-level inverters [4]–[10]. Notably, the proposed topology is simple, compact, and requires only a single DC source, unlike CHB. Most recently proposed topologies demand more devices and driver circuits compared to the proposed topology. The topologies proposed in [4], and [9] are buck in nature, while the topology proposed in [7] is competitive in terms of device counts but has a more complex structure and control scheme. In [20], an SC-based MLIs is proposed, and the comparison shows that the devices, total standing voltage (TSV), and efficiency of these topologies are close to the proposed topology. However, the proposed topology inherits the features of a reliable T-type structure and a half-bridge circuit, showcasing its merit compared to discrete switches. Additionally, the boosting factor is twice that of other topologies, highlighting the unique and compact structure of the proposed design.

Indeed, SC topologies face limitations such as voltage balancing challenges, high inrush current during startup, and limited scalability. However, these issues can be addressed through the self-balancing capability of the proposed topology and optimized system design, leading to improved efficiency. In particular, inrush current can be effectively mitigated by incorporating pre-charging circuits with relays and current-limiting resistors to gradually charge the capacitors during startup. Controlled voltage application via PWM-driven switches further ensures a smooth voltage rise, reducing sudden current surges. Moreover, the techniques proposed in [22] for managing startup inrush current can protect power components from stress and enhance overall system performance and reliability.

V. CONCLUSION

In this paper, an FPGA implementation of a new single-phase five-level inverter is presented for grid-connected renewable applications. The proposed topology offers simplicity, compactness, and double voltage gain using two switched capacitors for boosting, along with a five-level output voltage waveform. The complete operation and development of control schemes have been detailed. Experimental and simulation results demonstrate the effectiveness of the proposed topology under both open-loop and grid-connected modes. The total harmonic distortion (THD) of the injected grid current is measured at 4.8%, ensuring high power quality for grid-connected renewable applications. Additionally, the topology is capable

of providing reactive power support. Finally, a detailed comparison is made to highlight the significance of the proposed five-level inverter in terms of device count, output voltage capability, and structural effectiveness.

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