Analysis and Optimized Design of Conducted Common-Mode EMI Characteristics of CLLC Circuits

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***Abstract*—The CLLC converter offers advantages such as high efficiency, high power density, bidirectional Buck-Boost capability, and soft-switching operation, and has been widely applied in automotive onboard chargers and renewable energy systems. Electromagnetic compatibility (EMC) is one of the critical performance indicators for CLLC circuits. To investigate the conducted common-mode (CM) EMI characteristics of the CLLC converter, a CM EMI equivalent circuit model was established based on the noise transmission mechanism, and an equivalent model of the CLLC converter was derived, clarifying the noise source characteristics and the key CM noise transmission path impedances. The noise source characteristics under different operating conditions were analyzed to reveal the CM noise behavior in each condition. Based on this analysis, a symmetry-based design method for optimizing the CM EMI performance of the CLLC converter was proposed, and the impacts of resonant inductor and capacitor symmetry were examined. The correctness of the CM characteristic analysis for the CLLC converter is verified through simulations and experimental tests. By constructing a symmetric resonant cavity structure, the CM noise is attenuated by 20–30 dB, which further validates the feasibility of the symmetric structure-based optimization design method.**

***Index Terms*—CLLC converter, common-mode EMI, symmetrical structure.**

I. Introduction

AGAINST the backdrop of global energy transition and the rapid development of the new energy vehicle industry, the onboard charger (OBC) has become a core component of the electric vehicle energy supply system, with its performance and reliability receiving increasing attention in the field [1]–[4]. In OBC systems, resonant DC-DC converters play a key role in achieving high-efficiency energy transfer. Among them, the CLLC resonant converter has become the mainstream topology for the DC conversion stage of automotive chargers due to its advantages, including high efficiency, high power density, bidirectional power flow, and soft-switching operation. This topology not only affects the energy transfer performance of OBC systems but also significantly impacts their electromagnetic compatibility (EMC) characteristics. Therefore, investigating the electromagnetic interference (EMI) characteristics of CLLC circuits holds both theoretical significance and practical engineering value for improving the overall EMI performance of OBC systems.

Current research on CLLC converters primarily focuses on circuit parameter design, control strategies, and magnetic integration technologies, while systematic studies on their EMC characteristics remain limited. In OBC systems, the differential-mode interference generated by CLLC circuits is largely bypassed by the DC bus capacitors at the output of the front-end power factor correction (PFC) stage. As a result, the main EMI impact of CLLC circuits on OBC systems manifests as common-mode (CM) interference [5]–[7]. Early-stage analysis and optimization of the CM noise characteristics of CLLC circuits can therefore provide critical theoretical guidance and practical reference for subsequent EMI filter design.

Existing studies on CM EMI in CLLC circuits mainly focus on analyzing and optimizing parasitic parameters or implementing additional CM inductors and Y-capacitors in the circuit. [8] proposed altering the layer structure of planar PCB high-frequency transformers and designing adjacent layers on the primary and secondary sides at equipotential to achieve zero CM noise. However, this approach is relatively complex and may increase winding losses in the high-frequency transformer. [9] further proposed a shielded winding design to optimize the CM EMI performance of planar transformers, effectively suppressing the CM noise current through the transformer. Nevertheless, this method requires additional PCB layers for the shielded winding design, resulting in higher costs. Besides transformer optimization, [10] utilized the phase difference characteristics of noise sources in LLC converters to achieve CM noise cancellation through balancing capacitors. Yet, the effective frequency range of this method is limited and relies on the valid frequency region of the dual-capacitor transformer model. [11]–[12] propose an optimal design method of symmetric planar transformers for LLC converters to achieve CM noise optimization. However, they only analyze the CM characteristics under one operating condition, fail to analyze the differences in CM characteristics under different operating conditions, and do not specifically analyze the impact of the symmetry of resonant components on the optimization effect. Therefore, it is necessary to clarify

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the CM EMI characteristics of the CLLC circuit under different operating conditions, and then explore a more effective optimization method for CM noise.

To address these issues, this paper investigates the CM noise transmission mechanism and suppression strategies of CLLC circuits. Based on the substitution theorem and superposition principle, a CM equivalent model of the CLLC circuit is established to reveal the main CM noise transmission paths and influencing factors. Combining the characteristics of CM noise sources, an analytical model of the CLLC circuit's CM noise is derived, and the CM behavior under different operating conditions is systematically analyzed. Based on noise source characteristics, a symmetry-based CM noise optimization method is proposed, achieving significant noise suppression through symmetric design of resonant inductors and capacitors. Finally, circuit simulations and prototype experiments are conducted to verify the effectiveness of the proposed models and optimization method, providing theoretical and engineering guidance for low-EMI design in automotive chargers.

The structure of this paper is organized as follows: Section I analyzes the basic CM noise transmission paths and establishes the CM equivalent circuit model of the CLLC circuit based on the substitution and superposition theorems. Section II further investigates the characteristics of noise sources and develops an analytical model for the CM behavior of the CLLC circuit. Section III proposes a symmetry-based CM noise optimization method and analyzes the effects of resonant inductor and capacitor symmetry. Section IV presents simulation and prototype experimental results to validate the CM characteristic analysis and the effectiveness of the proposed symmetrical optimization design.

II. Modeling and Analysis of Common-Mode EMI Characteristics for CLLC Circuits

A. Analysis of Common-Mode Noise Transmission Mechanism in CLLC Circuits

The topology of the CLLC circuit is shown in Fig. 1. Switches Q_1–Q_4 form the primary full bridge, while Q_5–Q_8 constitute the secondary full bridge. L_{rp}, L_{rs}, C_{rp}, and C_{rs} represent the primary and secondary resonant inductors and capacitors, respectively. T denotes the high-frequency isolation transformer, and L_m is the magnetizing inductance. The resonant inductors, resonant capacitors, and high-frequency transformer together form the CLLC resonant tank. The CLLC circuit typically operates under variable-frequency control, and changes in the switching frequency modify the impedance characteristics of the resonant tank, thereby regulating the output voltage or current.

Within the dashed frame in Fig. 1, the components constitute a line impedance stabilization network (LISN). The midpoints of the four bridge arms, labeled A, B, C, and D, serve as voltage transition nodes. C_{g1}–C_{g4} represent the bridge midpoint-to-ground parasitic capacitors, and C_o is the output-to-ground parasitic capacitor. In isolated circuits, the electric field coupling between the primary and secondary windings of the transformer forms a CM noise transmission channel.

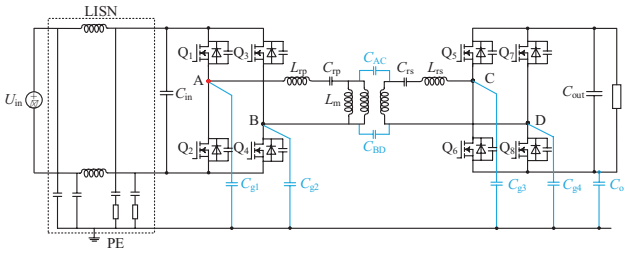

Fig. 1. CLLC converter topology considering key parasitic parameters.

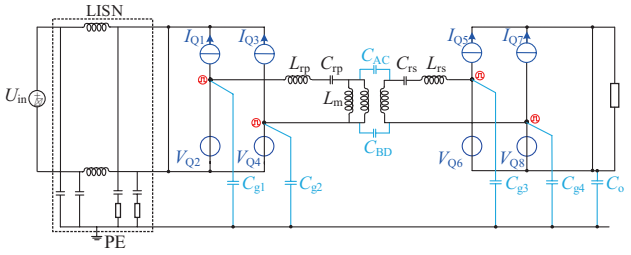

Fig. 2. Equivalent circuit using the substitution theorem.

To accurately analyze the conducted CM EMI characteristics, the transformer must be modeled. [13]–[14] proposed a two-capacitor transformer model based on the principle that CM EMI conduction through the transformer should follow displacement current laws. Accordingly, this study employs a lumped two-capacitor model to represent the transformer, where C_{AC} and C_{BD} denote the primary and secondary distributed capacitances, respectively.

To clarify the noise transmission mechanism, the substitution theorem is applied to model the switches (considered as noise sources according to EMC theory) using equivalent voltage and current sources. Switches Q_2, Q_4, Q_6, and Q_8 are replaced by voltage sources V_{Q2}, V_{Q4}, V_{Q6}, and V_{Q8} that match their voltage waveforms, while switches Q_1, Q_3, Q_5, and Q_7 are replaced by current sources I_{Q1}, I_{Q3}, I_{Q5}, and I_{Q7} that correspond to their current waveforms. Since the high-frequency components of the input and output voltages are relatively small, the input and output capacitors can be approximated as short circuits within the conducted EMI frequency range, as illustrated in Fig. 2.

Further, based on the superposition principle, when only the current sources act, the voltage sources are short-circuited. In this case, the CM noise generated by the current sources is shorted by the input and output bus and cannot flow through the LISN. When only the voltage sources act, the current sources are open-circuited. The CM noise generated by the voltage sources mainly propagates along two paths: through the switch-to-ground parasitic capacitances and through the transformer parasitic parameters. For analytical convenience, the CM EMI equivalent circuit of the CLLC converter is derived as shown in Fig. 3, where R_{cm} represents the CM equivalent resistance of the LISN.

As shown in Fig. 3, the CM noise at the LISN side is determined by two main factors: the parasitic capacitors, which define the CM noise transmission paths and impedance characteristics, and the voltage transitions caused by the high-frequency switching of the devices, which act as the primary

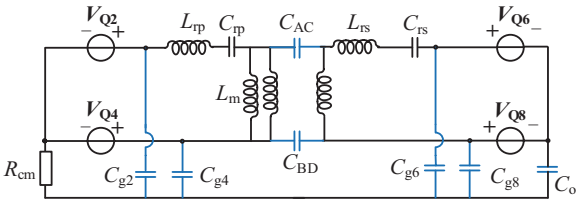

Fig. 3. CLLC circuit common-mode EMI equivalent circuit model.

excitation sources. These voltage transitions are critical for describing the CM noise characteristics of the circuit, highlighting the necessity of further analyzing the CM noise source characteristics of the CLLC circuit.

B. Analysis of Noise Source Characteristics for CLLC Circuits

Based on the CM equivalent circuit model presented previously, the noise sources V_{Q2}, V_{Q4}, V_{Q6}, and V_{Q8} are identified as the primary contributors to the generation of CM noise. To further elucidate the noise formation mechanism in CLLC circuits, it is essential to analyze the characteristics of these noise sources.

The CLLC circuit operates with a switching frequency f_s and a resonant frequency f_r. Based on the relationship between the switching frequency and the resonant frequency, the circuit can operate under three conditions: under-resonance ($f_s < f_r$), quasi-resonance ($f_s = f_r$), and over-resonance ($f_s > f_r$). To further investigate the impact of operating conditions on the conducted CM EMI characteristics of the CLLC converter, Fig. 4 presents the time-domain waveforms of V_{Q2}, V_{Q4}, V_{Q6}, and V_{Q8} under the under-resonance, quasi-resonance, and over-resonance conditions.

From the time-domain waveforms shown in Fig. 4, it is observed that under quasi-resonance and over-resonance conditions, all noise sources (V_{Q2}, V_{Q4}, V_{Q6}, and V_{Q8}) exhibit square-waveforms with a duty cycle of approximately 0.5. Taking the quasi-resonance condition as an example, the Fourier decomposition of these waveforms can be expressed as:

$$\begin{cases} V_{Q2}(t) = V_{in}\cdot d + \sum_{n=1}^{\infty}\left[\frac{2V_{in}}{n\pi}\sin(n\pi d)\right]\sin(n\omega_o t - n\pi) \\ V_{Q4}(t) = V_{in}\cdot d + \sum_{n=1}^{\infty}\left[\frac{2V_{in}}{n\pi}\sin(n\pi d)\right]\sin(n\omega_o t) \\ V_{Q6}(t) = V_{out}\cdot d + \sum_{n=1}^{\infty}\left[\frac{2V_{out}}{n\pi}\sin(n\pi d)\right]\sin(n\omega_o t - n\pi) \\ V_{Q8}(t) = V_{out}\cdot d + \sum_{n=1}^{\infty}\left[\frac{2V_{out}}{n\pi}\sin(n\pi d)\right]\sin(n\omega_o t) \end{cases} \quad (1)$$

where n is the harmonic order and d is the duty cycle of the square wave.

According to this decomposition, the theoretical spectrum of the noise sources contains only odd-order harmonics. Furthermore, V_{Q4} lags V_{Q2} by half a period, and V_{Q8} lags V_{Q6} by half a period. This phase relationship leads to the harmonic characteristics that: odd-order harmonics of the same order are phase-opposite, while even-order harmonics have the same amplitude and phase.

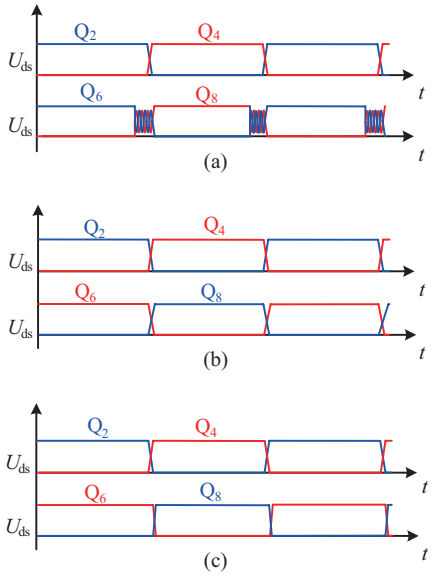

Fig. 4. CLLC circuit common-mode EMI equivalent circuit model. (a) Time-domain waveform of the under-resonance operating condition noise source, (b) Time-domain waveform of the quasi-resonance operating condition noise source, (c) Time-domain waveform of the over-resonance operating condition noise source.

In contrast, the under-resonance condition exhibits distinct characteristics. Under this condition, the primary-side noise sources V_{Q2} lags V_{Q4} remain square waves with a duty cycle close to 0.5, while the secondary-side noise sources V_{Q6} lags V_{Q8} generate high-frequency oscillations due to resonant effects. To analyze the secondary-side noise sources, the waveforms are decomposed into a square-wave component and a high-frequency oscillation component, as illustrated in Fig. 5. The high-frequency LC oscillations affect the spectral content within their frequency range and may result in resonance peaks in the CM noise spectrum. Therefore, the main component of the noise sources under the under-resonance condition remains the fixed-duty-cycle square wave, and its phase and amplitude characteristics are consistent with those observed under the quasi-resonance condition.

Based on the above analysis, the following conclusions can be drawn: (1) the noise spectra of the CLLC circuit mainly consist of odd-order harmonics; (2) for harmonics of the same order, the odd-harmonic amplitudes of V_{Q2} and V_{Q4} are equal, while their phases are opposite; the odd-harmonic amplitudes of V_{Q6} and V_{Q8} are equal, with opposite phases. These noise source characteristics provide a theoretical basis for subsequent analysis of CM noise spectral behavior and the design of noise suppression methods.

III. Common-Mode Characteristics of the CLLC Circuit Under Different Operating Conditions

After establishing the CM EMI equivalent circuit and identifying the characteristics of primary and secondary noise sources, the theoretical expression of common-mode noise voltage can be derived using the nodal voltage equations based on Fig. 3. In practical applications, the four switching transistors

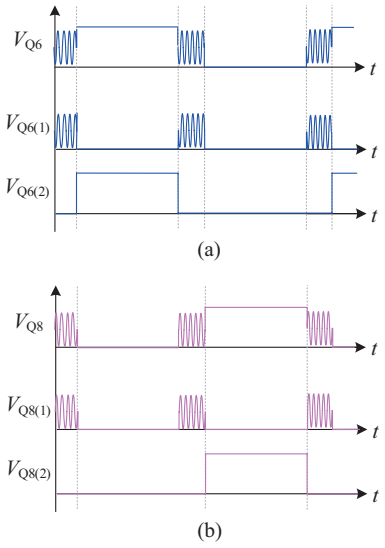

Fig. 5. Decompose the secondary-side noise sources under under-resonance operating conditions. (a) V_{Q6} waveform decomposition, (b) V_{Q8} waveform decomposition.

on the primary side typically share the same size, model, and device stress. Assuming these primary-side switches have identical parasitic capacitances to ground, the CM noise flowing through these capacitances cancels each other out due to the phase relationship of the noise sources. The same holds true for the secondary side. Therefore, the CM noise of the CLLC converter is mainly transmitted through the transformer. To simplify the analysis, assuming all switching transistors have a uniform parasitic capacitance to ground (denoted as C_g) will not introduce significant errors into the qualitative analysis of the CLLC converter's CM characteristics.

$$\begin{cases} V_{cm} = R_{cm}\,j\omega(2C_g + C_o)\Delta_1(V_{Q4} - V_{Q8})/\{j\omega(2C_g + C_o)\cdot \\ \quad (j\omega C_{AC} + Y_{rs} + Y_{rp}n_T{}^2 + j\omega C_{AC}n_T{}^2 - 2j\omega C_{AC}n_T) + \\ \quad 4R_{cm}\left(j\omega C_g\right)^2\left[Y_{rs} + Y_{rp}n_T{}^2 + j\omega C_{AC}(n_T+1)^2\right] + \\ \quad \Delta_2 + 2R_{cm}\,j\omega C_g\Delta_3\} \\ \Delta_1 = -\omega^2 C_{AC}C_{BD}(n_T-1)^2 + j\omega(C_{AC}+C_{BD})Y_{rs} + \\ \quad n_T{}^2\,j\omega(C_{AC}-C_{BD})Y_{rp} + 2n_T\,j\omega(C_{AC}+C_{BD})Y_{rp} \\ \Delta_2 = \left[j\omega(C_{AC}+C_{BD})(Y_{rp}n_T{}^2 + Y_{rs}) - \omega^2 C_{AC}C_{BD}(n_T-1)^2\right]\cdot \\ \quad (4R_{cm}\,j\omega C_g + R_{cm}\,j\omega C_o + 1) \\ \Delta_3 = j\omega C_o\left[j\omega C_{AC}(n_T-1)^2 + Y_{rs} + n_T Y_{rp} + 4n_T\omega^2 C_{AC}C_g\right] \end{cases} \tag{2}$$

where n_T is the transformer turns ratio, Y_{rp} and Y_{rs} represent the series admittance of the primary and secondary resonant inductors and resonant capacitors.

It can be seen from this equation that the CM noise at this time can be equivalent to the result of the action of V_{Q4}–V_{Q8}. To simplify the analysis, this paper defines the CLLC CM equivalent noise source $V_Q(t)$ as $(V_{Q4}-V_{Q8})$, performs Fourier expansion on it, analyzes the characteristics of the equivalent CM noise source, and further clarifies the differences in CM

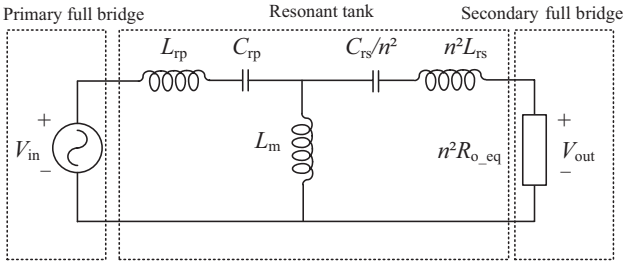

Fig. 6. Fundamental-frequency equivalent circuit diagram.

characteristics under different operating conditions.

By performing Fourier decomposition, $V_Q(t)$ can be expressed as:

$$V_Q(t) = V_{Q4}(t) - V_{Q8}(t) = \sum_{n_{odd}=1}^{\infty}\left[\frac{8}{\pi}\frac{\sin\left(\frac{(2n_{odd}-1)\varphi}{2}\right)\cdot V_{ds}}{2n_{odd}-1}\right]\cdot \sin\left((2n_{odd}-1)\omega t + (2n_{odd}-1)\theta + \frac{(2n_{odd}-1)\varphi}{2} + 90^?\right) \tag{3}$$

$$a_m = \left|\frac{8}{\pi}\frac{\sin\left((2n_{odd}-1)\varphi/2\right)}{2n_{odd}-1}\right| \tag{4}$$

Let n_{odd}=1, 2, 3, …denote the order index of odd harmonics, corresponding to the harmonic orders n=2n_{odd}−1=1, 3, 5, …

To quantify this effect, an amplitude influence factor a_m is introduced, representing the impact of the phase difference on the CM equivalent noise source. For identical electrical and parasitic parameters, a larger a_m corresponds to a higher CM noise amplitude.

Since the phase difference φ varies under different operating conditions, it is essential to clarify its trend. The phase relationship of V_Q essentially reflects the phase difference between the primary and secondary full bridges. The fundamental harmonic method can be used to analyze the phase relationship. The primary full bridge is represented by a sinusoidal voltage source V_{in}, and the secondary full bridge is replaced by an equivalent resistance R_{o_eq}. Referring all parameters to the primary side, the equivalent fundamental circuit is shown in Fig. 6.

According to the fundamental equivalent circuit, the transfer function $H(j\omega)$ from input to output voltage can be derived, and the fundamental phase difference φ_1 between them is expressed as a function of the normalized frequency f_n=f_s/f_r.

$$H(j\omega) = \frac{V_{out}^*}{V_{in}^*} = \frac{j\omega^3 n_{odd}R_{o\_eq}L_mC_{rp}C_{rs}}{\left[\omega^2\left(C_{rs}L_m + n_{odd}{}^2C_{rp}L_m + n_{odd}{}^2C_{rp}L_{rp} + n_{odd}{}^2C_{rs}L_{rs}\right) + \omega^3 n_{odd}R_{o\_eq}C_{rp}C_{rs} - n_{odd}{}^2 - j\omega C_{rs}n_{odd}{}^2C_{rs} - C_{rs}C_{rp}\omega^4\left(L_mL_{rp} + n_{odd}{}^2L_mL_{rs} + n_{odd}{}^2L_{rp}L_{rs}\right)\right]} \tag{5}$$

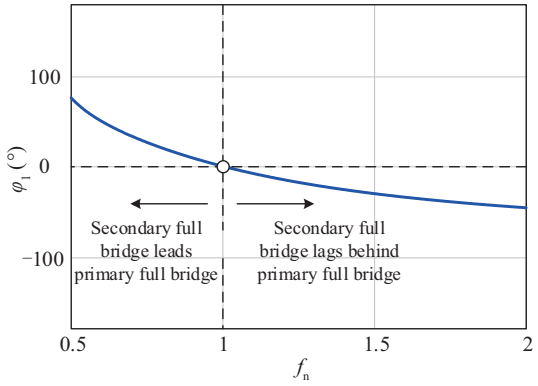

Fig. 7. Variation of fundamental phase difference φ_1 with normalized frequency f_n.

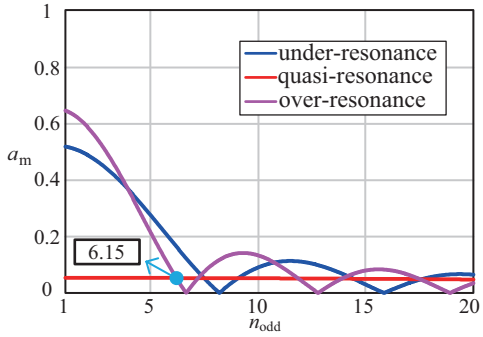

Fig. 8. Variation of phase influence factor a_m with harmonic order n_{odd}.

$$\varphi_1(f_n) = \text{angle}\left(\frac{\dot{V}_{out}}{\dot{V}_{in}}\right) \tag{6}$$

For fixed resonant network parameters, φ_1 depends solely on f_n, and its variation with f_n is plotted in Fig. 7. When f_n=1 (quasi-resonant condition), φ_1=0; when f_n>1 (over-resonant condition), the primary bridge leads the secondary bridge, and $|\varphi_1|$ increases with frequency; when f_n<1 (under-resonant condition), the primary bridge lags the secondary bridge, and $|\varphi_1|$ increases as the frequency decreases. Based on the CM noise model of the CLLC converter, the quasi-resonant condition corresponds to $\varphi_1\approx0$, resulting in the minimum amplitude coefficient of V_Q and thus the lowest CM noise.

To illustrate the influence of φ_1 on V_{cm}, a practical circuit is analyzed with parameters: f_r=100 kHz, n_T=1, L_m=174 μH, L_{rp}=L_{rs}=48 μH, C_{rp}=C_{rs}=50 nF, and R_{o_eq}=80 Ω. Substituting these into the analytical expressions yields phase values of φ_1=23.47°, 2.41°, and −29.34° at f_s=80 kHz (under-resonant), 100 kHz (quasi-resonant), and 150 kHz (over-resonant), respectively. The harmonic amplitude variation of V_Q with phase difference is shown in Fig. 8.

As can be seen from the Fig. 8, before the 11th harmonic (n_{odd}=6), the harmonic amplitude coefficient a_m of the CM equivalent noise source under the quasi-resonant condition is the lowest, indicating that the amplitude of the CM equivalent noise source under the quasi-resonant condition is the smallest. With the same impedance of the CM loop, the CM noise under the quasi-resonant condition is lower than that under other conditions.

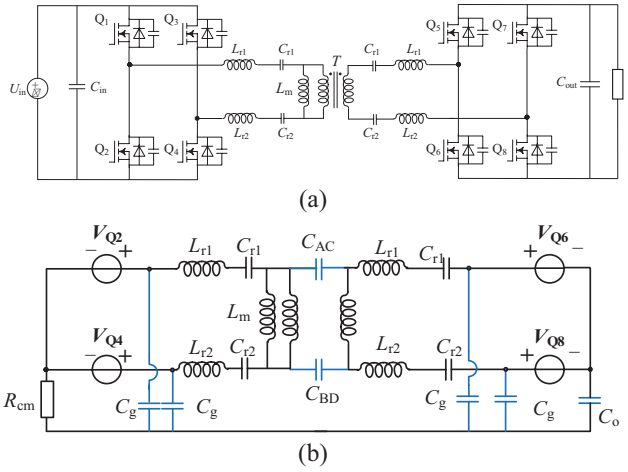

Fig. 9. Topology of the symmetrical CLLC circuit. (a) Symmetrical CLLC circuit diagram, (b) Equivalent circuit of symmetrical CLLC common-mode EMI characteristics.

In summary, the CM characteristics of the CLLC circuit under different operating conditions are as follows:

(i) Quasi-resonant condition: The CM noise spectrum is dominated by odd harmonics. Since $\varphi\approx0$, the equivalent CM noise amplitude is minimized, leading to the lowest CM noise level.

(ii) Over-resonant condition: The CM noise spectrum is mainly composed of odd harmonics. As the ratio f_s/f_r increases, $|\varphi|$ increases, resulting in higher amplitude coefficients and noise.

(iii) Under-resonant condition: The CM noise spectrum also consists mainly of odd harmonics. As the ratio f_s/f_r decrease, $|\varphi|$ increases, resulting in higher amplitude coefficients and higher CM noise. Moreover, the secondary-side resonance introduces high-frequency oscillations, leading to localized peaks in the high-frequency region of the CM noise spectrum.

Having clarified the CM noise characteristics of the CLLC converter under various operating conditions, it is necessary to develop an effective design method for optimizing CM noise suppression.

IV. Common-Mode Noise Optimization Design for Constructing Symmetric Structures

A. Analysis of the Common-Mode Noise Optimization Principle of the Symmetrical Structure

According to the previous analysis of the noise source characteristics, the primary-side noise sources V_{Q2} and V_{Q4}, as well as the secondary-side noise sources V_{Q6} and V_{Q8}, exhibit identical magnitudes and opposite phases for the same odd-order harmonics. Based on this feature, this paper proposes a CM noise optimization method by constructing a symmetrical CM loop, enabling the cancellation and suppression of CM noise. The symmetrical CLLC circuit diagram and its equivalent circuit of CM EMI characteristics are shown in Fig. 9.

To meet the power loop design requirements of the CLLC

converter, the parameters should satisfy $L_{r1}+L_{r2}=L_{rp}=L_{sp}$, $C_{r1}//C_{r2}=C_{rp}=C_{sp}$. Based on the equivalent CM EMI circuit shown in Fig. 9(b), the CM noise currents contributed by individual primary and secondary noise sources can be derived using the superposition theorem, as expressed in (7)–(9).

$$I_{cm1}=\frac{j\omega\left(C_{AC}+C_{BD}\right)\left(-Y_1+Y_2\right)Y_Z\cdot V_{Q4}}{j\omega\left(C_{AC}+C_{BD}\right)\left(Y_1+Y_2+2Y_Z\right)+\left(Y_1+Y_2\right)Y_Z} \tag{7}$$

$$I_{cm2}=\frac{-j\omega\left(C_{AC}+C_{BD}\right)\left(-Y_1+Y_2\right)Y_Z\cdot V_{Q8}}{j\omega\left(C_{AC}+C_{BD}\right)\left(Y_1+Y_2+2Y_Z\right)+\left(Y_1+Y_2\right)Y_Z} \tag{8}$$

$$I_{cm}=I_{cm1}+I_{cm2} \tag{9}$$

where $Y_1=\frac{1}{j\omega L_{r1}+1/\ j\omega C_{r1}}$, $Y_2=\frac{1}{j\omega L_{r2}+1/\ j\omega C_{r2}}$, and $Y_Z=\frac{1}{R_{cm}+1/\ j\omega C_o}$.

From these expressions, it can be observed that when the parasitic capacitances from the switching devices to ground are identical, the noise currents through them cancel out, resulting in CM noise current predominantly flowing through the transformer. When the resonant components satisfy $L_{r1}=L_{r2}$, $C_{r1}=C_{r2}$, i.e., $Y_1=Y_2$, the theoretical CM noise current becomes zero, demonstrating the feasibility of CM noise suppression through symmetrical circuit design.

In practical engineering, however, perfect symmetry of resonant components is difficult to achieve due to manufacturing tolerances. Additionally, transformer leakage inductance can further disturb the symmetry of the resonant inductors. Therefore, it is essential to clarify how the symmetry deviations of resonant inductors and capacitors influence the CM noise suppression performance.

To better characterize the theoretical model of the symmetrical structure, the common-mode loop impedance Z_{cm} is defined as follows.

$$\begin{cases} I_{cm}=\dfrac{V_Q}{Z_{cm}} \\ V_Q=V_{Q4}-V_{Q8} \\ Z_{cm}=\dfrac{j\omega\left(C_{AC}+C_{BD}\right)\left(Y_1+Y_2+2Y_Z\right)+\left(Y_1+Y_2\right)Y_Z}{j\omega\left(C_{AC}+C_{BD}\right)\left(-Y_1+Y_2\right)Y_Z} \end{cases} \tag{10}$$

Among them, I_{cm} represents the CM noise current flowing through the LISN side, and the voltage drop generated by it across the LISN is the CM noise voltage.

It can be seen from the above equation that when the circuit operating condition is determined, the amplitude and phase relationship of the CM equivalent noise source V_Q is constant, and the CM noise current is inversely proportional to the CM loop impedance. That is, the larger the CM impedance Z_{cm}, the smaller the CM noise under the same operating condition.

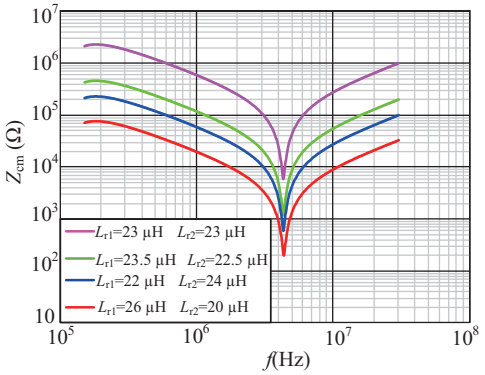

Fig. 10. Analysis of the influence of inductor symmetry.

Thus, the CM noise suppression capability under the symmetric structure can be evaluated according to the variation trend of the CM loop impedance Z_{cm}. Based on this model, the influence law of parameter deviations of resonant components on the CM noise optimization effect can be further analyzed in depth.

B. Influence of Resonant Inductor Symmetry

The previous analysis examined the CM characteristics of the CLLC converter under ideally symmetrical conditions. In practical engineering applications, however, parameter deviations must be considered, among which the symmetry of the resonant inductors is one of the key factors affecting the CM noise suppression performance of the symmetrical structure. On one hand, the resonant inductors inevitably exhibit parameter mismatches due to manufacturing tolerances; on the other hand, the transformer leakage inductance also contributes to asymmetry between the inductors. To quantitatively analyze the impact of inductor parameter symmetry on CM noise cancellation, Fig. 10 presents the CM loop impedance curves under different resonant inductor parameters.

As shown in the Fig. 10, the degree of deviation in inductor symmetry has a significant effect on CM noise suppression across the entire frequency range. When the asymmetry is large, the CM loop impedance becomes evidently unbalanced, degrading the CM noise cancellation effect. Conversely, when the asymmetry is small, the CM noise can be effectively suppressed over a wide frequency band.

It should be noted that the transformer leakage inductance accounts for a considerable portion of the total resonant inductance and thus plays a critical role in determining inductor symmetry. Therefore, while satisfying the resonant parameter design requirements, the transformer leakage inductance should be minimized as much as possible to maintain inductor symmetry and ensure effective CM noise suppression.

C. Influence of Resonant Capacitor Symmetry

After clarifying the effect of resonant inductor symmetry on CM noise within the conduction frequency band, the symmetry of the resonant capacitors is also identified as a key factor that determines the CM noise suppression performance of the

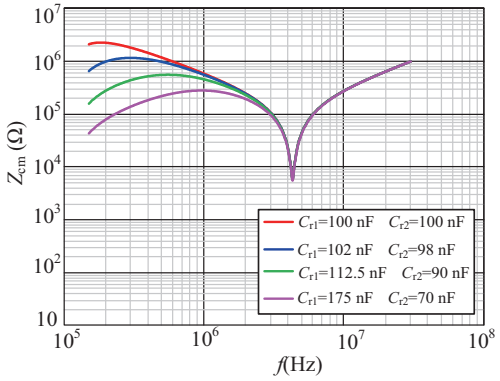

Fig. 11. Analysis of the influence of capacitor symmetry.

TABLE I
BASIC CIRCUIT PARAMETERS OF THE CLLC CIRCUIT

Parameters	Symbol	Unit	Value
Input Voltage	V_{in}	V	200
Rated Power	P_o	W	400
Output Voltage Range	V_{out}	V	130–230
Switching Frequency Range	f_s	kHz	80–150
Resonant Frequency	f_r	kHz	100
Transformer Turns Ratio	n_T	-	1

symmetrical structure. According to the expression of CM loop impedance, Fig. 11 illustrates the impedance curves under various resonant capacitor symmetry conditions.

As shown in Fig. 11, the asymmetry of the resonant capacitors mainly affects CM noise suppression in the low-frequency region. In the medium- and high-frequency ranges, the capacitive impedance is much smaller than the inductive impedance, making its asymmetry less influential on the overall CM noise cancellation performance. Therefore, maintaining the parameter symmetry of both the resonant inductors and capacitors is a fundamental prerequisite for achieving optimal CM noise suppression in a symmetrical CLLC structure.

V. CIRCUIT SIMULATION VERIFICATION

A. Comparison of Simulated CM EMI Noise Spectra of the CLLC Converter Under Different Operating Conditions

To validate the theoretical analysis presented in this paper, simulation models and experimental prototypes of the CLLC circuit were built and designed, with detailed design parameters listed in Table I.

A full-circuit EMI simulation model considering key parasitic parameters was implemented using PSIM. Through simulation, the noise signals across the LISN sampling resistors were obtained. By performing differential-mode and common-mode separation, the CM noise signals were extracted and subsequently fed into the receiver algorithm model to obtain the simulated CM noise.

To verify the theoretical analysis of the CLLC circuit under

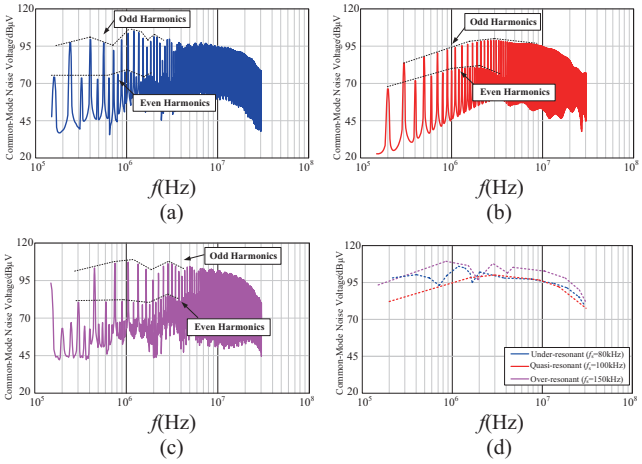

Fig. 12. Simulated common-mode noise spectra under three operating conditions. (a) Under-resonant (f_s=80 kHz), (b) Quasi-resonant (f_s=100 kHz), (c) Over-resonant (f_s=150 kHz), (d) Envelope comparison of CM spectra under three operating conditions.

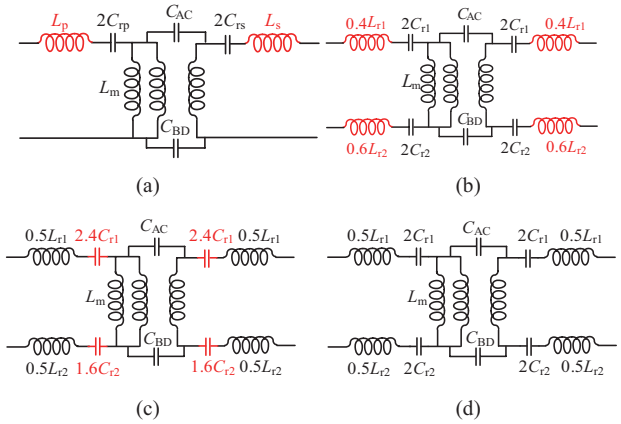

Fig. 13. Resonant tank structure with inductor and capacitor deviations. (a) Structure 1, (b) Structure 2, (c) Structure 3, (d) Structure 4.

three operating conditions, Fig. 12 presents the simulated common-mode spectra for under-resonant, quasi-resonant, and over-resonant conditions.

As shown in Figs. 12(a)–(c), the common-mode noise spectra for all three conditions are dominated by odd-order harmonic components, confirming the correctness of the previously analyzed noise source characteristics. Further comparison in Fig. 12(d) shows that the quasi-resonant condition exhibits the lowest CM noise in the low-frequency range, mainly because the phase of its CM equivalent noise source is close to zero, resulting in the smallest amplitude coefficient of common-mode noise. The simulation results are consistent with the theoretical analysis.

B. Simulation Verification of CM EMI Characteristics of the Symmetrical CLLC Converter

To further evaluate the impact of resonant inductor and capacitor symmetry deviations on common-mode noise suppression, four resonant cavity structures were constructed for simulation: Fig. 13(a) shows the original circuit structure;

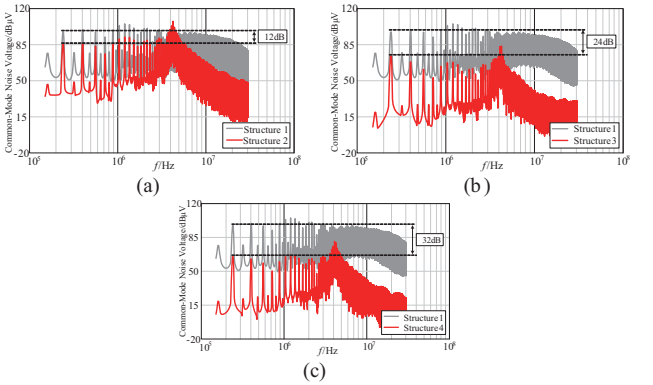

Fig. 14. Simulated common-mode noise spectra with inductor and capacitor deviations. (a) Comparison of simulated CM spectra between resonant tank Structure 1 and Structure 2, (b) Comparison of simulated CM spectra between resonant tank Structure 1 and Structure 3, (c) Comparison of simulated CM spectra between resonant tank Structure 1 and Structure 4.

(b) represents a structure with large symmetry deviations in resonant inductors and transformer leakage inductance; (c) represents a structure with small symmetry deviations in resonant inductors and transformer leakage inductance; and (d) corresponds to a structure with fully symmetric resonant inductors and capacitors.

Fig. 14 presents the simulated common-mode voltage spectra of the four resonant cavity structures under the over-resonant condition.

As shown in Figs. 14(a) and (c), inductor symmetry deviations reduce CM noise cancellation over the full frequency range (≈20 dB difference in the low-frequency band), confirming that inductor symmetry affects CM noise suppression across all frequencies as theoretically analyzed. Comparing Figs. 14(b) and (c), capacitor symmetry deviations primarily impact low-frequency suppression (≈8 dB difference), demonstrating that resonant capacitor symmetry mainly influences low-frequency CM noise optimization. These simulation results validate the theoretical analysis on the effects of symmetry deviations in resonant inductors and capacitors.

VI. Prototype Experimental Verification

To verify the correctness of the theoretical analysis in this paper, an experimental prototype of the CLLC converter was built (with the same parameters as those in the simulation verification) for experimental validation. The prototype and test environment are shown in Fig. 15. The voltage method was adopted during the test, and the differential-common mode separator was CMDM8700 manufactured by R&S.

A. Comparison of Measured CM EMI Noise Spectra of the CLLC Converter Under Different Operating Conditions

To validate the theoretical analysis of the CM noise characteristics of the CLLC circuit under different operating conditions, a prototype was built and experimental measure-ments were conducted, with specific parameters listed in Table I. Fig. 16 presents the measured CM noise spectra for switching frequencies

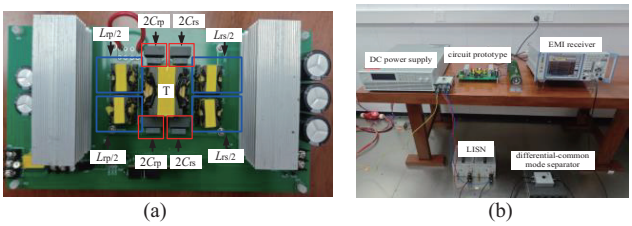

Fig. 15. Experimental Prototype and Test Environment. (a) Experimental Prototype, (b) Test Environment.

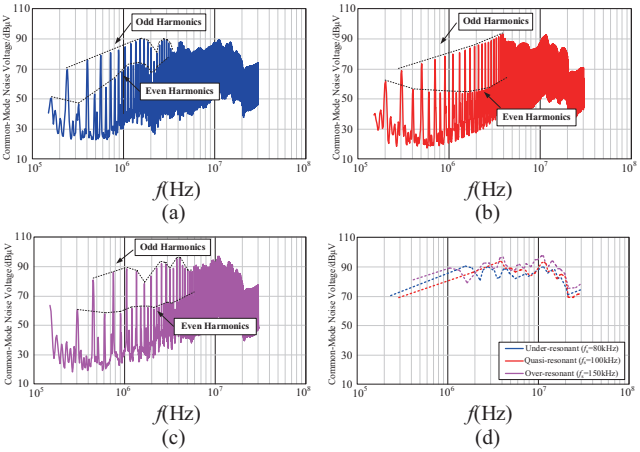

Fig. 16. Measured common-mode noise spectra under three operating conditions. (a) Under-resonant (f_s=80 kHz), (b) Quasi-resonant (f_s=100 kHz), (c) Over-resonant (f_s=150 kHz), (d) Envelope comparison of CM spectra under three operating conditions.

of 80 kHz (under-resonant condition), 100 kHz (quasi-resonant condition), and 150 kHz (over-resonant condition).

As shown in Fig. 16, within the frequency range of 150 kHz–1.5 MHz, the CM noise amplitude under the quasi-resonant condition is significantly lower than that under the other two conditions. This is because the phase of the CM equivalent noise source is close to zero under the quasi-resonant condition, resulting in the minimum amplitude coefficient and, consequently, the lowest CM noise. The experimental results are consistent with the theoretical derivation and simulation analysis presented earlier, confirming the correctness of the mechanism by which the noise source phase relationship influences CM noise under different operating conditions.

B. Experimental Verification of CM EMI Characteristics of the Symmetrical CLLC Converter

To verify the influence of resonant component symmetry on the optimization of CM EMI characteristics, Fig. 17(a) shows the measured CM noise spectrum under over-resonant conditions when the resonant capacitors are symmetrical (C_{r1}=C_{r2}=100 nF) and the resonant inductors are asymmetric (L_{r1}=34 μH, L_{r2}=14 μH). Fig. 17(b) presents the measured CM noise spectrum under symmetric inductors (L_{r1}=L_{r2}=24 μH) but asymmetric capacitors (C_{r1}=220 nF, C_{r2}=68 nF). Fig. 17(c) shows the measured CM noise spectrum when both the resonant inductors and capacitors are symmetric.

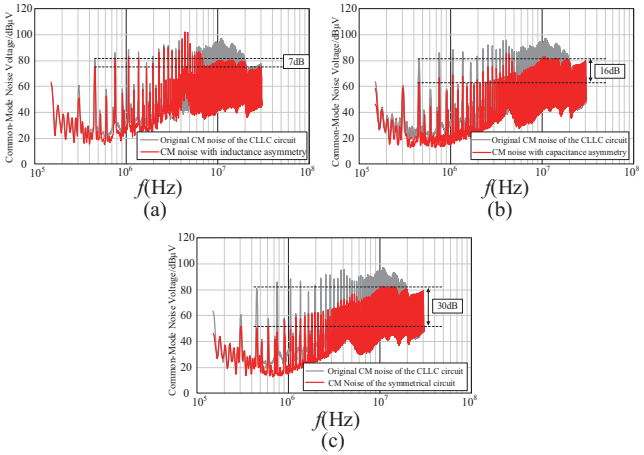

Fig. 17. Measured common-mode noise spectra. (a) Measured CM noise with inductor asymmetry, (b) Measured CM noise with capacitor asymmetry, (c) Measured CM noise with symmetric resonant components.

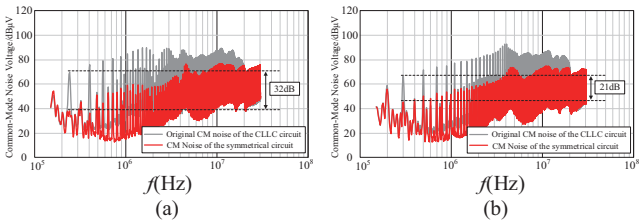

Fig. 18. Measured common-mode noise spectra. (a) Measured CM noise under under-resonant condition with symmetric resonant components, (b) Measured CM noise under quasi-resonant condition with symmetric resonant components.

As shown in Fig. 17(a), significant asymmetry of resonant inductors results in approximately 7 dB CM noise attenuation under over-resonant conditions, with CM noise deterioration at 4–5 MHz—consistent with the earlier theoretical analysis of inductor symmetry (Fig. 10).

From Figs. 17(b) and (c), large asymmetry of resonant capacitors leads to 16 dB CM noise attenuation under over-resonant conditions, indicating capacitor symmetry mainly affects low-frequency CM noise suppression but has little impact on mid- to high-frequencies. This experimental observation aligns well with the theoretical analysis.

To further verify the optimization effect of the symmetric CLLC circuit structure on CM EMI characteristics under other operating conditions, Fig. 18 presents the measured CM noise spectra of the symmetric resonant tank (symmetric inductors and capacitors) under under-resonant and quasi-resonant conditions.

As shown in Fig. 18 and Fig. 17(c), the symmetric structure significantly reduces CM noise under all three operating conditions, achieving approximately 20−30 dB suppression within the 150 kHz–3 MHz band. At the third harmonic frequency, improvements of 32 dB, 21 dB, and 30 dB are achieved for the under-resonant, quasi-resonant, and over-resonant conditions, respectively. The quasi-resonant condition shows a smaller suppression at the third harmonic, mainly because the circuit operates near the series resonance of the resonant inductor and capacitor (f_s = 100 kHz), making the circuit nearly perfectly symmetrical and leaving limited room for further low-frequency noise reduction.

Moreover, the symmetric CLLC circuit does not show significant CM noise improvement in the high-frequency range. This is mainly due to factors such as dead-time settings in the gate-drive signals and differences in the MOSFET conduction times, which cause the phase relationship between primary- and secondary-side noise sources to deviate from perfect anti-phase, reducing CM noise cancellation at high frequencies. The experimental results fully validate the feasibility and effectiveness of the proposed design approach for achieving CM noise cancellation through constructing a symmetric CLLC circuit structure.

VII. Conclusion

This paper investigates the CM EMI characteristics of CLLC converters and proposes a structural symmetry-based optimization method for CM noise suppression. The main conclusions are summarized as follows:

1. An equivalent circuit model for the CLLC converter's CM EMI was established, identifying primary noise sources and key parasitic parameters. Fourier analysis was applied to characterize CM noise spectral features based on this model.
2. Based on the theoretical expression of CM noise voltage, CM EMI characteristics under under-resonant, quasi-resonant, and over-resonant conditions were analyzed. Differences among these conditions stem from noise source phase variations, with the quasi-resonant condition exhibiting the optimal phase and superior CM EMI performance.
3. A CM noise cancellation method leveraging structural symmetry was proposed for the converter's CM noise characteristics, along with a corresponding equivalent model. Simulation and experimental results verified its effectiveness. Further analysis indicates that resonant inductor/capacitor symmetry is critical to noise cancellation—symmetry deviations reduce suppression efficacy, confirming the method's engineering feasibility.

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