Power Conversion Solutions for Future Server Boards Operating Directly From High-Voltage DC

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***Abstract*—The rapid scaling of accelerated computing is pushing rack power well beyond 1 MW, making conventional 48 V distribution increasingly inefficient due to busbar and connector currents. High-voltage DC (HVDC) distribution (e.g., 800 V) enables lower distribution losses and motivates server boards that interface directly to an HVDC bus. This paper addresses two enabling building blocks on the server board: (i) safe hot-swap and eFuse functionality with controlled pre-charging and telemetry, and (ii) high-power-density conversion from 800 V to intermediate-bus voltages. For hot-swap, a 1200 V-rated SiC JFET cascode is evaluated in linear mode and demonstrated to pre-charge 300 µF from 0 V to 800 V in approximately 1.5 s while staying within the device SOA limits. For power conversion, an unregulated LLC-DCX approach is investigated. An 800 V-to-50 V input-series-output-parallel (ISOP) half-bridge converter using GaN switches on the primary and secondary side and a matrix transformer reaches 98.1% efficiency at full load and a peak efficiency above 98.4%. A direct 800 V-to-12 V converter prototype achieves 97% at 6 kW and 98.2% peak efficiency.**

***Index Terms*—DCX, eFuse, GaN, high-voltage DC (HVDC), hot-swap, intermediate bus converter (IBC), LLC, SiC JFET.**

I. Introduction

With increasing power consumption of modern GPUs and higher GPU counts per rack, rack power levels are projected to scale toward 1 MW and beyond [1]. At these power levels, high-voltage DC (HVDC) distribution is increasingly considered as an alternative to conventional 48 V distribution, primarily to reduce distribution currents and the associated losses.

Historically, server power delivery has progressed through several distribution-voltage levels, driven by the need to limit resistive losses and thermal stress as rack power density increased. Early server designs relied on 12 V distribution from rack-level power supplies to individual server boards [2]. As power demand grew, this approach led to very high currents in busbars and connectors, resulting in significant I^2R losses and increasingly challenging thermal management.

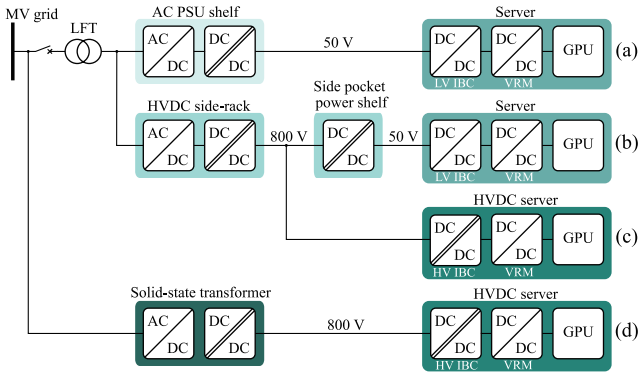

Fig. 1. Evolution of data center power architecture. (a) Today's system with AC distribution and integrated IT racks, (b) Next-generation systems with AC distribution and disaggregated IT racks using 50 V servers, (c) Next-generation systems with AC distribution and disaggregated IT racks using 800 V servers, (d) A future system with data-center-wide HVDC distribution and 800 V servers.

The introduction of 48 V DC distribution (see Fig. 1(a)) was a major step forward, reducing distribution currents by a factor of four compared to 12 V while maintaining compatibility with established safety standards and infrastructure [3]. This architecture enabled rack power levels up to several hundred kilowatts. However, as accelerated computing pushes racks beyond 500 kW toward 1 MW and higher, even 48 V distribution becomes constrained by busbar currents reaching several thousand amperes.

As a next step, the busbar voltage can be increased to ±400 V or 800 V, providing a further reduction in distribution current by up to 16× relative to 48 V systems. This approach reduces required copper cross-sections in busbars and cables and lowers distribution losses. In practice, this typically coincides with a transition from single-phase power supply units (PSUs) to three-phase PSUs with high-voltage DC outputs, since three-phase PSUs offer the advantage that they load the three grid phases equally and are more cost effective at higher power levels. Conversion from 800 V to a lower intermediate-bus voltage can be provided either by a side-pocket power shelf attached to the rack (see Fig. 1(b)) or by a high-voltage intermediate-bus converter (HV IBC) placed directly on the server board (see Fig. 1(c)).

Future server boards may therefore interface directly to an HVDC bus. Fig. 1(d) sketches a facility-wide HVDC architec-

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ture with centralized HVDC distribution (e.g., 800 V DC) and downstream conversion to point-of-load VRM stages on the server board. Moreover, HVDC distribution aligns well with renewable energy sources and battery storage systems operating at similar voltage levels, which may improve overall data center efficiency.

In this paper, we focus on eFuse functionality, hot-swap safety aspects, and power conversion on the server board. We investigate a three-stage power conversion from 800 V to 50 V, followed by an intermediate-bus converter (IBC) to 12 V or 6 V and the final point-of-load (PoL) conversion to the core. This architecture can reduce power-distribution losses and provides flexibility in the physical placement of the IBC. It also supports a mezzanine-card approach, where the GPU is mounted together with IBCs and PoLs on a separate card.

In addition, we analyze a direct power conversion from 800 V to 12 V followed by PoL stages. This approach eliminates one conversion stage and may reduce the required server-board footprint. Direct power conversion from 800 V to 6 V is a further option that is not covered in this paper.

The paper is organized as follows: Section II discusses the safety and pre-charging functions required to hot-plug server boards onto an HVDC bus while the remaining server boards in the rack continue to operate. Section III and section IV detail 800 V-to-50 V and 800 V-to-12 V power converters. A short summary and conclusion section in section V wraps up the key findings.

II. Protection and Pre-Charging of Server Boards

Hot-swap and eFuse functionality are important in data centers to support serviceability and availability. Replacing a server board while the rack continues to operate avoids powering down an entire system for maintenance and reduces operational disruption. This capability becomes increasingly important as rack power increases and HVDC architectures are adopted. In addition, monitoring current and voltage at the interface between the server board and the HVDC bus is essential for safe and reliable operation of accelerated-compute platforms.

As mentioned in the introduction, an HVDC bus architecture at, for example, 800 V can support the growing power demands of racks. However, hot-swapping under HVDC introduces several challenges: the risks associated with high-voltage systems, such as arcing, current surges, and component stress, make the design and implementation of hot-swap functionality more complex. In this section, we address these challenges with a focus on safety, reliability, and system robustness.

A. Requirements of Hot-Swap Power Devices

One of the key functions of hot-swapping is inrush-current control. When the compute tray is hot-plugged into an HVDC bus, input capacitances on the server board must be charged to the nominal bus voltage in a controlled manner to reduce the inrush current and thereby avoid triggering the system's over-current protection. With respect to hot-swap power device selection, there are two main parameters to be considered:

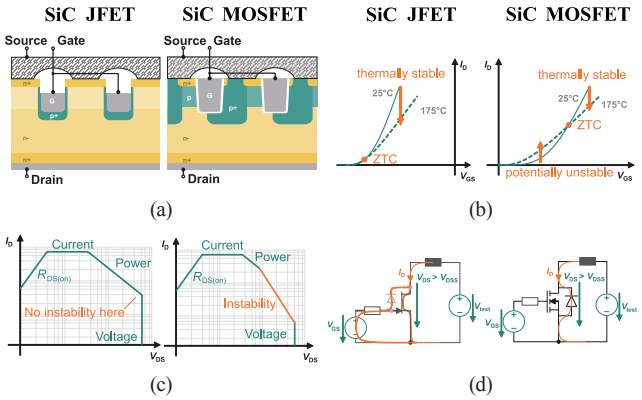

Fig. 2. Comparison of SiC JFET and SiC MOSFET by (a) cell concept, (b) SOA diagram, (c) transconductance, and (d) electric equivalent circuit.

- Safe operating area (SOA) characteristics
- On-resistance in steady-state operation

SOA characteristics describe the range of voltage and current conditions in which a device can operate reliably without damage, considering maximum power-dissipation limits, thermal constraints, and device characteristics (see Fig. 2(b)). This is particularly important during the linear charging phase of the input capacitors of the server board, where the inrush current should be actively controlled immediately after hot-plugging the compute tray. In this phase, the power device is subject to a large drain-source voltage (assuming discharged input capacitances on the server board and the HVDC bus voltage is applied to the hot-swap device) while delivering current to charge the input capacitors of the server board. The charging device must therefore tolerate significant power dissipation for an extended time in linear-mode operation.

Assuming an input capacitance C and a defined start-up time T, the minimum current needed for a linear charging profile from 0 V to V_{BUS} is given by:

$$I_{\mathrm{CHG}} = C\frac{V_{\mathrm{BUS}}}{T} \tag{1}$$

The maximum instantaneous power dissipated by the device at the beginning of the charging process is:

$$P_{\mathrm{CHG,max}} = V_{\mathrm{BUS}} I_{\mathrm{CHG}} = C\frac{V_{\mathrm{BUS}}^2}{T} \tag{2}$$

In contrast, during steady-state operation, the power device is fully ON and the main goal is to provide a low-resistance path to maximize power-delivery efficiency. The selection of the appropriate power device technology, package, and $R_{\mathrm{DS(on)}}$ depends on the power rating of the server board, the allowed pre-charging time, the input capacitances, and the cooling conditions. We consider pre-charging a server board with a thermal design power (TDP) of 12 kW and an input capacitance of 300 µF from 0 V to 800 V in less than 1.6 s. Due to space constraints on the motherboard, the solution needs to fit into an area of less than 4000 mm^2 at very limited height of 8 mm, such that it fits on the power distribution board of the server blade.

B. CoolSiC™ JFET for Hot-Swap Applications

Among high-voltage power technologies suitable for operation on an 800 V DC bus, the 1200 V-rated CoolSiC™ JFET provides a favorable combination of $R_{DS(on)} \times$ A figure of merit and SOA capability [4]. Due to the absence of a MOS channel, the device has monotonically increasing on-resistance with temperature and does not show any current crowding issues during linear operation. Since the JFET is a normally ON device, the cascode combination of a 40 V MOSFET and a SiC JFET guarantees normally OFF operation.

The low-voltage MOSFET type is selected along the guiding principle that its on-state $R_{DS,(on)}$-contribution accounts for less than 10% of the total DC resistance of the power-delivery network.

Fig. 2 shows a comparison of SiC MOSFET and SiC JFET technology with respect to device concept, safe-operating area, transconductance characteristic, and electric equivalent circuit. The key characteristic of the SiC JFET technology is its inherently thermally stable transconductance curve (see Fig. 2(c)), which supports stable linear-mode operation. In comparison, a SiC-MOSFET driven in saturation regime at low currents shows a negative temperature coefficient in its transconductance curve, which can lead to current imbalance, followed by potential device and system failure [5]. This is also reflected in the SOA comparison in Fig. 2(b), where the SOA of the SiC JFET shows only a thermal limitation without any instability regions.

Another important aspect is avalanche ruggedness, which may be needed in fault conditions when a fast disconnect of the server board is required. In this case, the parasitic inductance of the system will drive the hot-swap switch into an avalanche. As illustrated in Fig. 2(d), the SiC JFET can be driven into linear mode by clamping the device through a Gate-Drain Zener diode, thus increasing the single-pulse energy that can be dissipated in the device [6].

C. Linear Mode Control Using XDP701

Using the SiC JFET in cascode configuration enables control of the device in linear mode using Infineon's digital controller XDP701. This control IC integrates a digital loop that monitors V_{DS} and I_D of the device and modulates the gate of the LV MOSFET along a predefined SOA characteristic. The XDP701 IC allows the customer to program the optimal trajectory for controlling the inrush current based on the device's SOA. By modulating the gate of the LV MOSFET, both cascode-connected devices are driven in linear mode while following the preprogrammed trajectory of VDS-ID points in the SOA diagram.

The controller also supports a wide range of protection features: Over-voltage (OV) and under-voltage (UV), over-current (OC) as well as over-temperature (OT) conditions; it also supports real-time telemetry enabling the user to monitor voltage levels and load currents, actual power flow and FET health status through a Power Management (PM) Bus interface.

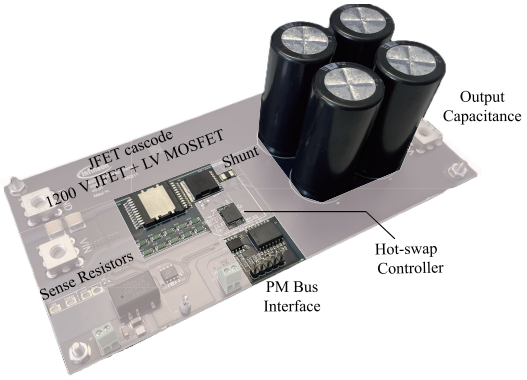

Fig. 3. Experimental validation board to verify hot-swap functionality.

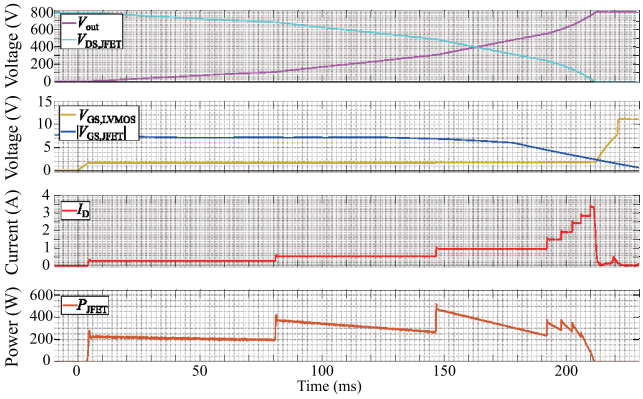

Fig. 4. Pre-charging of a server board with 150 µF input capacitance from 0 V to 800 V in linear mode using a combination of the control IC XDP701 and a 1200 V-rated SiC JFET.

D. Experimental Results

A demonstration board has been developed to evaluate the suitability of a SiC-JFET cascode for HV hot-swap applications (see Fig. 3), as highlighted in the previous section. We use this board to pre-charge a capacitance of 150 µF from 0 V to 800 V in approximately 210 ms. During start-up, the drain-source voltage VDS across the SiC-JFET and the drain current I_D are continuously sensed by the XDP701-1 hot-swap controller. Thus, the controller can follow a pre-programmed SOA profile for the SiC-JFET, realized by a closed-loop PID control that guarantees safe operation at all times.

By modulating the gate of the LV MOSFET, both cascode-connected devices are driven in linear mode while following the trajectory of V_{DS}-I_D points in the SOA diagram. Fig. 4 presents the experimental validation showing the voltage across the SiC-JFET ($V_{DS,JFET}$), the load current (I_D), and the power dissipated in the device during the pre-charging process. As can be seen, the device follows a pre-programmed SOA characteristic, which enables safe operation of the SiC JFET in linear mode.

E. System Solution

With the proven suitability of our CoolSiC™ JFET technology for hot-swap applications, a full system solution meeting safety requirements, protection, and telemetry is developed

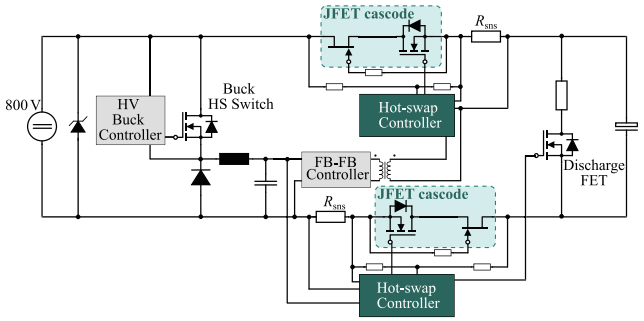

Fig. 5. System solution for hot-plug applications comprising two JFETs in cascode configuration with individual hot-swap controllers.

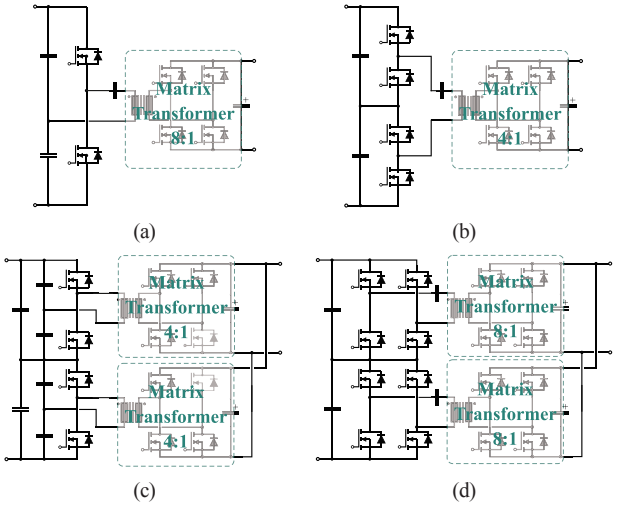

Fig. 6. Topology options for a high-voltage HV IBC with 800 V input and 50 V output. (a) Single converter stage, (b) 3-level stacked half-bridge, (c) ISOP half-bridge converter, and (d) ISOP full-bridge converters.

according to the block diagram shown in Fig. 5. It comprises two HV hot-swap modules, being deployed in each voltage rail as well as an auxiliary bias supply from the HV bus.

III. 800 V to 50 V Power Conversion

One option for power conversion from an 800 V HVDC bus comprises an initial conversion to 50 V using an HV IBC, followed by a low-voltage intermediate bus converter (LV IBC) to 12 V. The 12 V rail supplies the voltage regulator modules (VRMs) for conversion to core voltages below 1 V (see Fig. 1). This architecture reduces distribution losses and supports placing the LV IBC stage close to the load, as it occupies less space than a stage that directly converts from 800 V to 12 V. It can also be realized in a mezzanine-card configuration that consolidates the GPU, IBCs, and PoLs onto a dedicated card. The design objectives for the HV IBC converter are outlined as follows:

- Maintain a constant conversion ratio of 16:1 (i.e., ratio of 800V HVDC bus to 50V)
- Handle input voltages ranging from 760 V to 840 V, given the ±5% tolerance around the 800 V nominal input
- TDP of 6 kW with higher peak power surges for brief time intervals (i.e., 1.8× for 400 µs and 1.5× for 50 ms)
- Full-load efficiency of 98%
- Compact area of 60 mm by 60 mm and a maximum height of 11 mm

These specifications drive trade-offs between topology selection, high-voltage layout and insulation, thermal design within the constrained footprint, and matrix-transformer implementation.

TABLE I
Comparison of RMS Currents of the Primary-Side Switches in the Considered Topologies of Fig. 6

	(b)	(a) and (c)	(d)
Peak current	$2\pi \cdot \frac{P}{V_{DC}}$	$\pi \cdot \frac{P}{V_{DC}}$	$\frac{\pi}{2} \cdot \frac{P}{V_{DC}}$
RMS current	Outer switches $\frac{\pi}{\sqrt{2}} \cdot \frac{P}{V_{DC}}$ Inner switches $\frac{\sqrt{3}\pi}{\sqrt{2}} \cdot \frac{P}{V_{DC}}$	$\frac{\pi}{2} \cdot \frac{P}{V_{DC}}$	$\frac{\pi}{4} \cdot \frac{P}{V_{DC}}$

A. Topology Investigation

The unregulated series-resonant LLC converter topology operating at fixed frequency, also known as DCX, is a good candidate for this application because it provides high efficiency and power density [7]–[9]. It achieves load-current-independent soft-switching by utilizing the magnetizing current and also allows utilization of the leakage inductance as a resonant inductor. Based on this converter topology, four different options have been considered (see Fig. 6): (a) a single converter stage utilizing 1200 V devices, (b) a three-level (3L) stacked half-bridge utilizing 650 V devices, (c) an input-series-output-parallel (ISOP) half-bridge, and (d) an ISOP full-bridge utilizing 650 V devices.

Even though the single DCX converter stage (Fig. 6(a)) offers the advantage of a reduced component count, it concentrates the generated heat on fewer devices, exhibits a larger switch-node voltage swing (worsening EMI behavior), and does not provide a straightforward means to reduce output current ripple (e.g., by interleaving cells). Therefore, this topology was not considered for further analysis.

Although the 3L stacked half-bridge has the advantage of a higher equivalent switching frequency for the transformer, it suffers from unequal current distribution among the switches. As shown in Table I, higher current is experienced by the inner primary-side switches ($\sqrt{3}$ times higher than the outer switches) as well as a high output current ripple, thereby requiring a large output capacitance. The ISOP full-bridge topology (Fig. 6(d)) reduces primary-side current stress and output current ripple; however, it requires twice the number of components compared to other configurations, which increases complexity and cost. The ISOP half-bridge topology (Fig. 6(c)) balances component count, required on-resistance for primary-side switches,

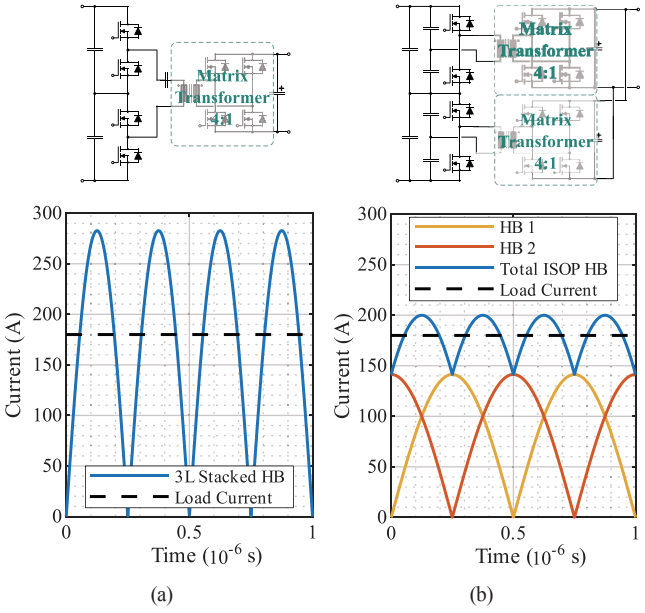

Fig. 7. Output current for the 6 kW 800 V-to-50 V DCX converter in case of (a) 3L stacked Half-Bridge DCX and (b) ISOP Half-Bridge.

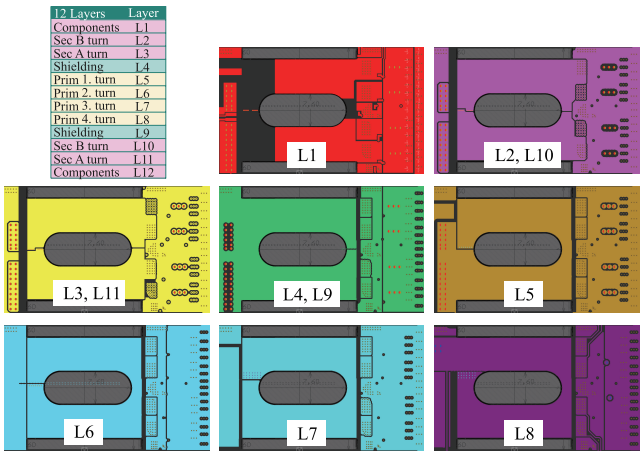

Fig. 8. Layer stack-up and winding layout of one 3 kW 400 V-to-50 V module.

and automatic balancing of the stacked capacitors [10]. Compared to the 3L stacked topology, the ISOP half-bridge allows phase-shifting of two half-bridges, thereby reducing the output current ripple and the required output capacitance, as shown in Fig. 7.

Based on these considerations, the ISOP half-bridge was selected for the prototype implementation. This means that a 6 kW 800 V-to-50 V converter system is composed of two 3 kW modules converting 400 V to 50 V. The balancing of the input capacitors of the two stacked modules is naturally provided by the fact that an increase of the input voltage of one of the modules will lead to a higher power transfer of said module and thus rebalance the capacitor stack [11].

B. Active Switches and Magnetic Design

In order to comply with the power density requirements, the converter operates at a switching frequency of 800 kHz. The combination of high switching frequency and high current density motivates the use of wide-bandgap devices. 650 V 25 mΩ GaN devices were selected for the primary side. For the secondary side, both 80 V 1.6 mΩ Silicon and 100 V 1.1 mΩ GaN devices can provide the required output current with low resistive loss, while the GaN devices also reduce the gate-driving losses as well as the required dead-time due to lower reflected Q_{oss} charges on the primary side.

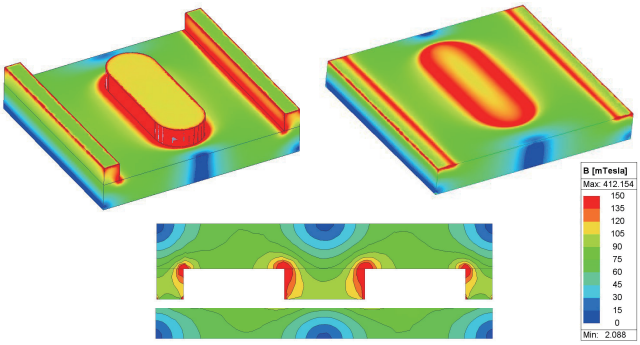

Fig. 9. FEM simulation (with Ansys EDT EM) of the transformer core of one 3 kW 400 V-to-50 V module.

Magnetic design is a key aspect of the system, as the combined losses from the windings and the magnetic core represent a major loss contribution, and transformer volume strongly influences power density. Therefore, given the height constraints, a planar transformer configuration was selected with a layer stack-up as shown in Fig. 8. To handle the high output current, a configuration with two full-bridge secondary outputs in a matrix configuration was selected based on analysis and efficiency targets [12]. The winding design was optimized to minimize AC losses by reducing skin and proximity effects, while also considering manufacturability and reinforced-insulation constraints. Each single-turn secondary winding consists of two parallel layers of 3 oz copper foil, while the primary winding uses four turns of 3 oz copper foil.

The magnetic core design, including air gap and core-limb diameter, was optimized for the switching frequency and to provide sufficient magnetizing current for soft-switching given the equivalent output capacitance on the primary and secondary sides. The core is made of ML95S material and features an elongated limb design to minimize eddy-current losses in the core [13], [14]. FEM simulations (see Fig. 9) were carried out to estimate core loss and related parameters, as summarized in Table II.

C. Board Design and Experimental Results

Finally, a 3 kW module (400 V to 50 V), comprising one of the two stacked half-bridges, has been validated in hardware. In Fig. 10(a), the first physical implementation of this module is illustrated, demonstrating its adherence to the required board size, as well as the component arrangement that forms the converter. Notably, the power MOSFETs are positioned on the top side of the module: the primary-side 650 V GaN devices

TABLE II
CORE LOSS, MAGNETIZING INDUCTANCE, AND PEAK FLUX DENSITIES AS FUNCTIONS OF SWITCHING FREQUENCY (SIMULATED RESULTS)

Parameter	Switching frequency (kHz)				
	800	900	1000	1100	1200
Core loss (W)	8.10	6.46	5.90	5.10	4.53
Magnetizing current (A, pk–pk)	15.53	13.82	12.50	11.16	10.17
Magnetizing inductance (μH)	8.45	8.45	8.45	8.45	8.45
Limb flux density (mT)	192	171	154	140	128
Yoke flux density (mT)	108	96	86	78	72

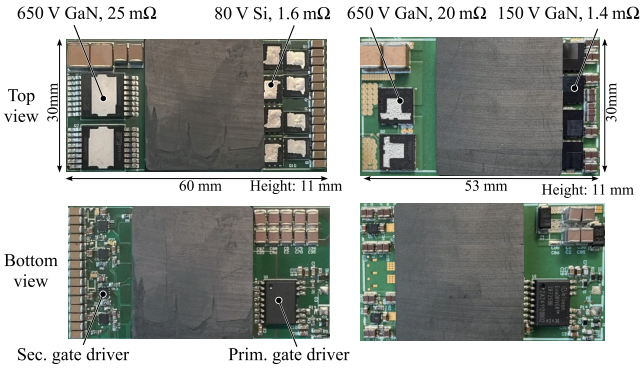

Fig. 10. Top and bottom view of the 3kW modules (400V to 50V) and placement of components. (a) Version with full-bridge rectification, (b) Center-tapped transformer version.

(IGLT65R025D2), utilizing a top-side cooled TOLT package, are located on the left, while the secondary-side 80 V OptiMOS™ devices (ISC016N08NM8SC), featuring an SSO8 top-side cooled package, are situated on the right side. This also allowed for a fair comparison with 100 V GaN devices that have the same footprint as the SSO8 package. The transformer is centrally located on the board. On the bottom side of the module, the synchronous-rectifier drivers are placed, alongside the input and resonant capacitances, completing the converter's component layout.

Fig. 10(b) shows a second version of the module with a center-tap transformer configuration which is currently under development. The center-tap configuration reduces the number of synchronous-rectification switches from eight to four, thereby improving power density to 2810 W/in^3 (module length reduced to 53 mm). The synchronous-rectification (SR) switches are all low-side referenced, which reduces the gate-driving efforts as non-isolated gate drivers can be used. However, the center-tapped approach requires SR devices with double the voltage class in comparison to the full-bridge rectifier, which moves the design into the sweet spot for Infineon's 150 V CoolGaN™ technology.

The measured results of the Si full-bridge rectifier converter design (Fig. 10(a)) operating at 800 kHz show a peak efficiency exceeding 98.2% and a full rated power efficiency of 98.0% at 3 kW, as illustrated in Fig. 11. The prototype uses 650 V GaN switches on the primary side and 80 V Silicon (Si) devices as synchronous rectifiers (SRs). Replacing the synchro-

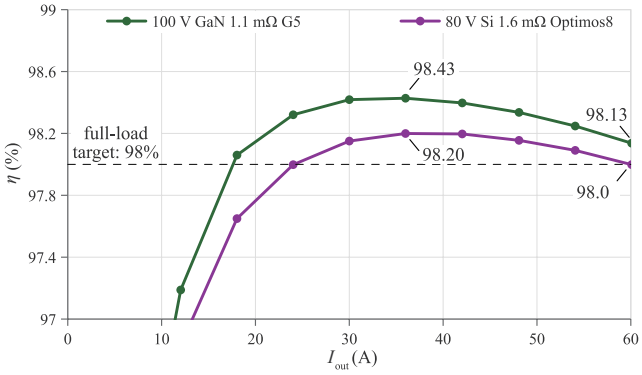

Fig. 11. Measured efficiency curves of a single 3 kW module with V_{in}=400 V and V_{out}=50 V comparing Si versus GaN HEMTs as synchronous-rectification switches within the prototype shown in Fig. 10(a).

nous-rectification switches with 1.1 mΩ GaN devices increases the efficiency to 98.13% at full load and to 98.43% at peak efficiency, as also shown in Fig. 11. The efficiency improvement is mainly due to the reduced conduction losses in the SR switches, as well as lower switching losses due to reduced gate-driving losses and dead-time related losses.

Table III presents a comparison of the demonstrated 800 V-to-50 V converter with state-of-the-art high-voltage DC-DC converters from literature. The table highlights key performance metrics including power level, voltage conversion ratio, topology, efficiency, power density, and switching frequency.

IV. 800 V TO 12 V POWER CONVERSION

As previously discussed, another option for power conversion from an 800 V HVDC bus comprises a direct conversion to 12 V followed by the final PoL stages. This approach removes one conversion stage and can reduce the space and complexity of the power-delivery implementation on the server board. The specific targets for the design are given as follows: the converter operates at a fixed 64:1 conversion ratio and withstands an input voltage range of 800 V ± 5% (which provides a nominal output voltage of 12.5 V). The TDP of the converter is 6 kW, with peak power requirements equal to the 800 V to 50 V HV IBC. An efficiency of 97% is targeted at full load, and the converter dimensions are limited to 125 mm × 40 mm × 8 mm.

A. Topology Investigation

As described in section III, the LLC-DCX resonant converter topology is a suitable candidate for this application. The main differences between the 800 V-to-50 V and 800 V-to-12 V power conversion stages are the much (4×) higher voltage conversion ratio of 64:1 and the significantly (accordingly 4×) higher output current of 480 A at nominal 12.5 V. Therefore, a matrix transformer with center-tap rectifiers is selected for the secondary side. Since a single conversion stage comprising 1200 V devices has considerable drawbacks, as discussed in section III, it was also disregarded for this design, which leaves the three candidate topologies based on 650 V devices shown in

TABLE III
SUMMARY OF STATE-OF-THE-ART HV 800 V/400 V-TO-50 V DC–DC CONVERTERS

Ref	Power	Input voltage	Output voltage	Topology	Primary switches	Secondary switches	Peak efficiency	Full load eff	Power density	Resonant frequency
[15]	3 kW	800 V	48 V	3L DCX with CT rectifier	650 V GaN	80 V Si	98.5%	98%	650 W/in^3	700 kHz
[16]	3 kW	400 V	48 V	HB LLC with FB rectifier	600 V GaN	100 V GaN	98.7%	97.6%	1500 W/in^3	360 kHz
[17]	3 kW	400 V	50 V	FB LLC with CT rectifier	600 V GaN	150 V GaN	97.3%	97.2%	450 W/in^3	1 MHz
[17]	3 kW	360 V	50 V	FB CLL with CT rectifier	600 V GaN	200 V GaN	97.3%	97.0%	550 W/in^3	960 kHz
[18]	6 kW	800 V	50 V	ISOP HB DCX with FB rectifier	650 V GaN	100 V GaN	98.8% est.	98.2% est.	2070 W/in^3	500 kHz
[19]	3 kW	400 V	48 V	HB LLC with FB rectifier	600 V GaN	100 V GaN	98.7%	97.3%	1050 W/in^3	300 kHz
[20]	3 kW	400 V	50 V	FB LLC with CT rectifier	600 V GaN	150 V GaN	97.3%	97.1%	416 W/in^3	1 MHz
[20]	3 kW	400 V	50 V	FB LLC with FB rectifier	600 V GaN	80 V GaN	98%	97.3%	700 W/in^3	1 MHz
[21]	3 kW	400 V	50 V	HB LLC with FB rectifier	650 V GaN	100 V GaN	98.7%	97.5%	1300 W/in^3	330 kHz
[22]	1.8 kW	380 V	48 V	ISO(S&P) HB DCX with CT rectifier	60 V Si	30 V Si	98.0%	96.7%	800 W/in^3	1 MHz
This work	3 kW	400 V	50 V	HB DCX with FB	650 V GaN	100 V GaN	98.43%	98.13%	2482 W/in^3	800 kHz

CT rectifier: center-tapped transformer rectifier; FB rectifier: full-bridge rectifier; ISOP: input-series-output-parallel; HB: half-bridge; 3L: three-level; S&P: series and parallel.

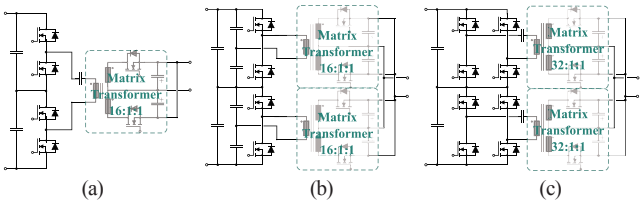

Fig. 12. Evaluated topology options for the 6kW 800 V-to-12 V DCX converter. (a) Stacked Half-Bridge DCX, (b) ISOP Half-Bridge DCX, (c) ISOP Full-Bridge DCX.

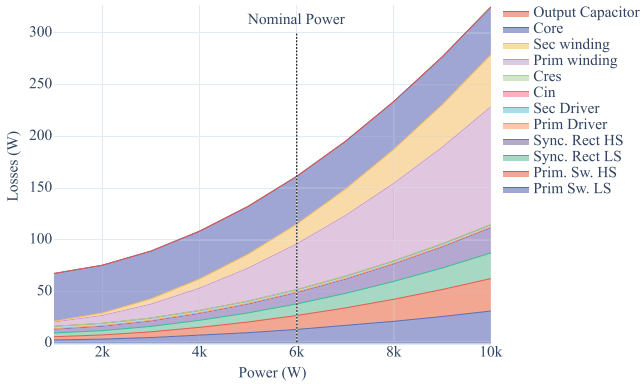

Fig. 13. Loss breakdown of the 800 V-to-12 V DCX converter. The losses of the selected power devices are below the losses of the remaining components.

Fig. 12. Since the same reasons as mentioned in section III also apply to the 800 V-to-12 V converter, the ISOP configuration with half-bridges on the primary side is also selected for this system.

B. Active Switches and Magnetic Design

In order to fit in the specified dimensions, the converter operates at a switching frequency close to 750 kHz. Such a high switching frequency, combined with the high currents and current densities of the design, poses stringent demands on the power switches.

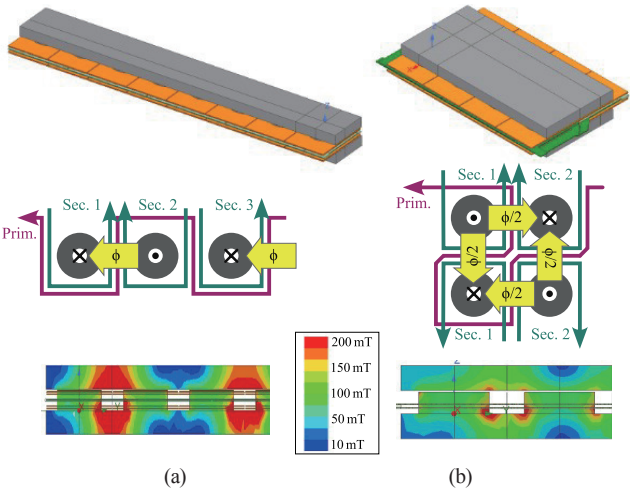

Fig. 14. Comparison of planar matrix-transformer variants for the 800 V to-12 V converter: (a) single row of core pillars and (b) two-row core pillar arrangement for reduced flux density and core losses within the given height.

650 V 25 mΩ GaN devices (IGLT65R025D2) were selected for the primary side. For the secondary side, 40 V 0.7 mΩ Si devices (BSC007N04LS6SC) provide the required output current with low resistive loss, and the termination design was optimized according to [23], [24]. This device selection reduces switching-device losses while keeping a balanced distribution between primary- and secondary-side losses (see Fig. 13).

The magnetic design is of critical importance as the combined power loss from the windings and magnetic core is now the single largest power loss contribution of the system as shown in Fig. 13. Given the high output current demand, a planar matrix transformer configuration has been chosen. The air gap and diameter of the magnetic core pillars are optimized for the switching frequency and equivalent output capacitance on the primary side to achieve ZVS by means of the magnetizing current. The core is made out of DMR59 ferrite material. A comprehensive analysis revealed that a design with eight

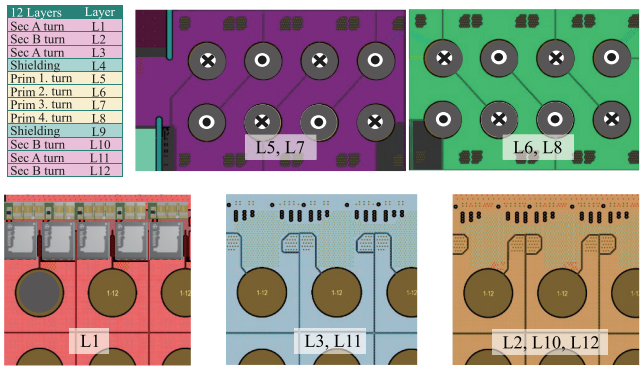

Fig. 15. Details of the selected planar matrix transformer, including winding layout and layer stack.

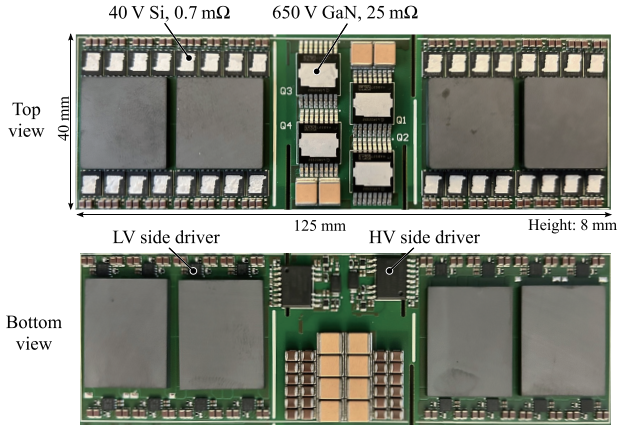

Fig. 16. Top and bottom view of the 6 kW 800 V to 12 V converter and placement of components.

secondary outputs placed in two rows of four pillars is the optimum design choice (see Fig. 14). In comparison to a design with eight pillars in a single row, this configuration reduces the flux density in the top and bottom parts and thus also the core losses within a given height of the converter. This has also been verified by FEM simulations.

Due to the high output current and the large required step-down ratio, the transformer winding design is a critical aspect of the system. As the ISOP configuration is used, the total conversion ratio of 64:1 is divided by two for each module, i.e., 32:1 per 3 kW converter. Since each module employs a half-bridge topology, each transformer needs a 16:1 turns ratio. This is realized by using four matrix transformer elements with four primary turns each. Each matrix transformer element has two secondary outputs with only a single turn each to minimize the secondary-side conduction losses. The details of the winding layout and the layer stack are shown in Fig. 15. For improved EMI performance, the layer stack contains also shielding layers which are referenced to the midpoint of the ISOP stack.

C. Board Design and Experimental Results

Fig. 16 shows the shape and component arrangement of the full 6 kW 800 V to 12 V converter. Each transformer is split into two cores with four limbs, with all power switches being placed on the top side to reduce the thermal resistance to the cold plate. On the bottom side, both primary and synchronous-rectifier drivers are placed, as well as input and resonant capacitances.

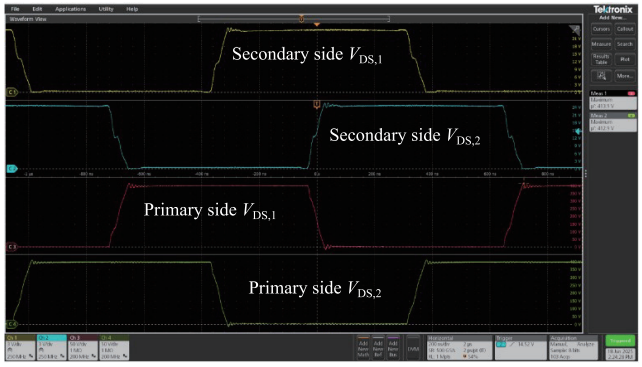

Fig. 17. Measured primary and secondary side switch node voltage waveforms (measured to the respective ground potentials) showing ZVS operation of primary-side GaN switches with smooth switching transitions.

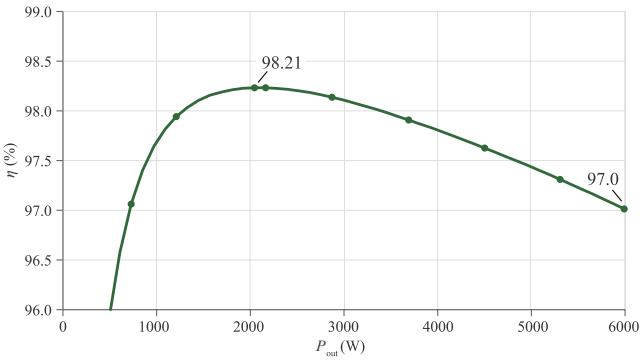

Fig. 18. Measured converter efficiency at V_{in}=800 V and V_{out}=12 V over the entire load range.

The measured waveforms (Fig. 17) of the primary and secondary side switch nodes at half of the rated power confirm zero voltage switching (ZVS) of primary-side devices and show smooth switching transitions enabled by ZVS operation and low parasitic inductance.

Finally, efficiency measurements show more than 98.21% peak efficiency and 97.0% at full rated power of 6 kW (see Fig. 18). These results were obtained with a liquid-cooled cold plate attached to the top side of the design.

V. Conclusion

Growing AI workloads increase the importance of reliable and efficient power-delivery architectures in data centers. This paper evaluates hot-swap and eFuse functionality for server boards connected to an 800 V HVDC bus, including controlled pre-charging and protection using the XDP701 controller and a CoolSiC™ JFET cascode.

We also study two power-conversion options: a three-stage approach (800 V to 50 V, followed by an intermediate bus converter to 12 V or 6 V and subsequent PoL stages) and a direct conversion from 800 V to 12 V followed by PoL stages. The measured full-load efficiency of 800 V to 50 V is 98.1%, while

800 V to 12 V yields approximately 97%. Future work will investigate direct power conversion from 800 V to 6 V.

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