A Thermal Model With the Capability of Characterizing Thermal Coupling Effects for Multi-Chip Power Modules

Zhiqiang ZHANG, Yunfei WANG, Jihui MA, Yuanbin LONG, and Huimin WANG

***Abstract*—Accurate thermal characterizations of power modules are beneficial for design and operation of power converters with the assistance of thermal models. However, the thermal coupling effects (TCEs) may degrade the performance of thermal models, and this becomes more pronounced in multi-chip power modules. To address this, a thermal model that enables to characterize different types of TCEs is presented in this paper. In the proposed thermal model, the properties of the classical thermal models are first provided. Then, different types of TCEs in multi-chip power modules are thoroughly analyzed. It is revealed from the analysis that the TCEs will affect the junction temperature distributions and heat flows, and distinct thermal behaviors are observed with different TCEs. Afterward, the thermal parameters including the self-thermal parameters and the coupling thermal parameters are extracted, and accordingly, the proposed thermal model is obtained. With the proposed thermal model, accurate thermal characterizations for multi-chip power modules are performed. Finally, taking typical insulated-gate bipolar transistor (IGBT) modules as a case study, the validity of the proposed thermal model under various conditions is confirmed through extensive experimental testing.**

***Index Terms*—Junction temperature distributions, multi-chip power modules, thermal characterizations, thermal coupling effects (TCEs), thermal model.**

I. Introduction

INCREASING demands for performance improvement of power electronics necessitate high-efficiency and high-power density converters, leading to a new paradigm of energy conversion [1], [2]. However, with the rapid development of such advanced power converters, reliability issues caused by the fatigue failures of power modules have gradually emerged. It is thoroughly investigated that the thermal stress is the main trouble-maker contributing to the fatigue failures of power modules [3], [4]. Therefore, accurate thermal characterization of power modules, which is typically implemented by using thermal models, is of importance to guarantee the long-term reliable operation of power converters.

Regarding the thermal models, many meaningful attempts have been made for power modules, which can be roughly classified into numerical models [5], [6], analytical models [7], [8], and thermal network models [9]–[30]. The numerical models that are originated from the finite-element analysis (FEA), achieve accurate thermal analysis. However, high computational burden acts as the biggest barrier to its widespread applications. Additionally, the analytical models are proven to be available solutions to deal with the issue of computational burdens in the numerical models. While, the number of the state variables will be highly increased with the increase of the mesh nodes. Considering this, the applicability of the analytical models may be degraded in practice.

Further efforts have been made towards utilizing the thermal network models to characterize the thermal behaviors of power modules. The classical thermal network models, which have already been well-known in the literature and in industry, include the Foster model [9]–[12] and the Cauer model [13]–[15]. As detailed in [9], a frequency-domain thermal network model was established based on the Foster model, in which the low-pass filters were adopted to characterize the heat flow of power modules. With this, this model can provide accurate junction temperature estimations. Based on [9], [11] further proposed an improved frequency-domain thermal network model. In this model, different thermal paths were comprehensively analyzed. By doing so, the accuracy of the predicted thermal behaviors is enhanced. Following that, a real-time adaptive Cauer model was reported in [13], and the main contribution of this thermal model was using the effective heat propagation paths to quantify the effects of module aging. The Foster model and the Cauer model with the advantages of easy implementations and low computation burdens are favorable. Despite this, both types of thermal network models find it difficult to provide precise thermal analysis for power modules with the thermal coupling effects (TCEs). This issue becomes serious when being applied

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in multi-chip power modules [16], [17].

To address the issue of poor thermal analysis in the classical thermal network models, several solutions have been recently progressed. One representative is referred to as the three-dimensional (3-D) thermal network model [18]−[23], where the TCEs are quantified by using the thermal impedance paths between different chips. Among them, a transient 3-D thermal model was proposed in [18] to obtain accurate junction temperature distributions of power modules, in which the effects of uneven power losses and cooling conditions were carefully considered. Following that, in [19], a 3-D compact thermal network model was reported, and the effects of boundary conditions on the parameters of the thermal network model were detailed. Additionally, a dynamic 3-D thermal network model was assigned to estimate the junction temperature in [21]. Compared to other thermal models, a major improvement of this model is the capability of providing an acceptable junction temperature estimation with the issue of base solder degradation. Considering the variations of the junction temperature may affect the parameters of the thermal network model, a 3-D temperature-dependent thermal model was proposed in [23], which enables to accurately predict the junction temperature in a wide junction temperature range. Though the 3-D thermal network models exhibit a satisfactory performance of thermal analysis even with the TCEs, most of them are troubled by the issue of computational burdens, and this problem will become prominent with the increase of the model order.

Other solutions to improve the thermal analysis accuracy are using the 2-D thermal network model, and the task of characterizing the TCEs is implemented by using the thermal impedance matrix [24]−[30]. As shown in [24], a physical thermal network model was developed to accomplish the junc-tion temperature estimation, where the thermal-coupling impedance matrix was used to illustrate the TCEs. However, the availability of this model is undesirable due to its high complexity. [26] presented an interesting thermal model considering the TCEs. In this model, with the artificial intelligence techniques, the characterization process of the thermal impedance matrix was simplified. Meanwhile, a novel frequency-domain thermal network model that includes the Foster model and several low-pass filters was reported in [28]. Notably, this model is commendable for its simple structure and thermal analysis accuracy in multi-timescales. Additionally, [29] investigated the relationship between the parameters of the thermal model and the thermal diffusion angle, and accordingly, the transient thermal impedance matrix was transformed to the steady-state thermal resistance matrix. Then, the TCEs on the junction temperature of power modules were clearly revealed. Moreover, an innovative attempt of thermal network model for multi-chip power modules was made in [30]. In this thermal model, the TCEs were characterized by using the injected power losses from the special node. And, an enumeration method was used as the identifier of the injected power losses and the injected nodes. It is noted that many research efforts have been put on seeking a proper thermal model for multi-chip power modules.

Nevertheless, different types of TCEs on the performance of the thermal models are not effectively investigated. More importantly, many existing thermal models fail to reflect the correct junction temperature of different chips in multi-chip power modules.

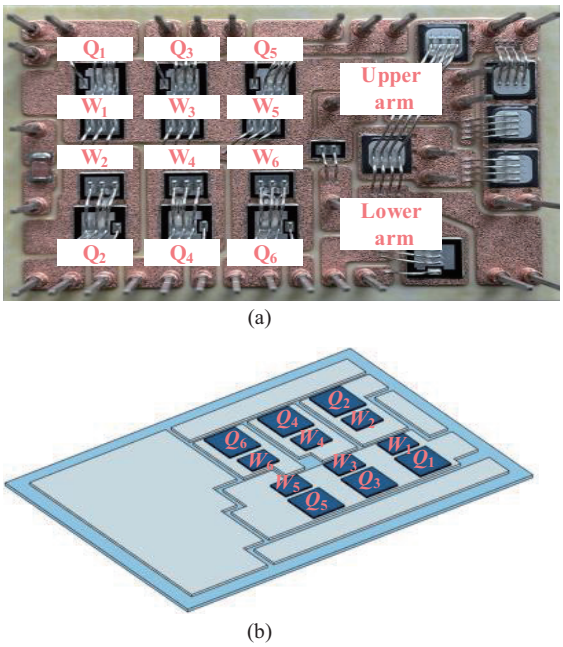

Fig. 1. Structure of the multi-chip IGBT module. (a) Photo. (b) The three-dimensional model of the multi-chip IGBT module.

In light of the above, a thermal model is proposed to provide accurate thermal characterizations for multi-chip power modules in this paper. Interesting benefits are achieved by using the proposed thermal model as follows.

1) Different types of TCEs in multi-chip power modules are detailed. Moreover, the thermal behaviors of the multi-chip power modules with distinct TCEs are fully investigated.

2) With a thorough analysis of the TCEs, the proposed thermal model is developed, which enables accurate junction temperature estimations with various TCEs.

3) According to the proposed thermal model, the junction temperature distribution of multi-chip power modules is provided, and then the junction temperature of different chips under different TCEs is accurately estimated.

The remainder of this paper is structured as follows. Section II analyzes the thermal behavior of multi-chip power modules with different thermal expansion coefficients. Afterward, Section III presents the implementations of the proposed thermal model. In Section IV, with the extracted junction temperature distribution functions, accurate junction temperature estimations for different chips are developed. Using a multi-chip insulated-gate bipolar transistor (IGBT) module as an example, a large number of experimental tests were conducted to examine the performance of the proposed thermal model under various conditions, with the corresponding results presented in Section V. The conclusions of this paper are summarized in Section VI.

II. Thermal Behaviors of Multi-Chip Power Module With Different Types of TCEs

As analyzed previously, the TCEs degrade the performance of the classical thermal network models. Considering this,

TABLE I
DIFFERENT TYPES OF TCES IN THE MULTI-CHIP IGBT MODULE

Name	Thermal coupling mode
Type-1 TCE	TCEs between Q_1 and Q_3
Type-2 TCE	TCEs between Q_3 and Q_5
Type-3 TCE	TCEs among Q_1, Q_3, and Q_5

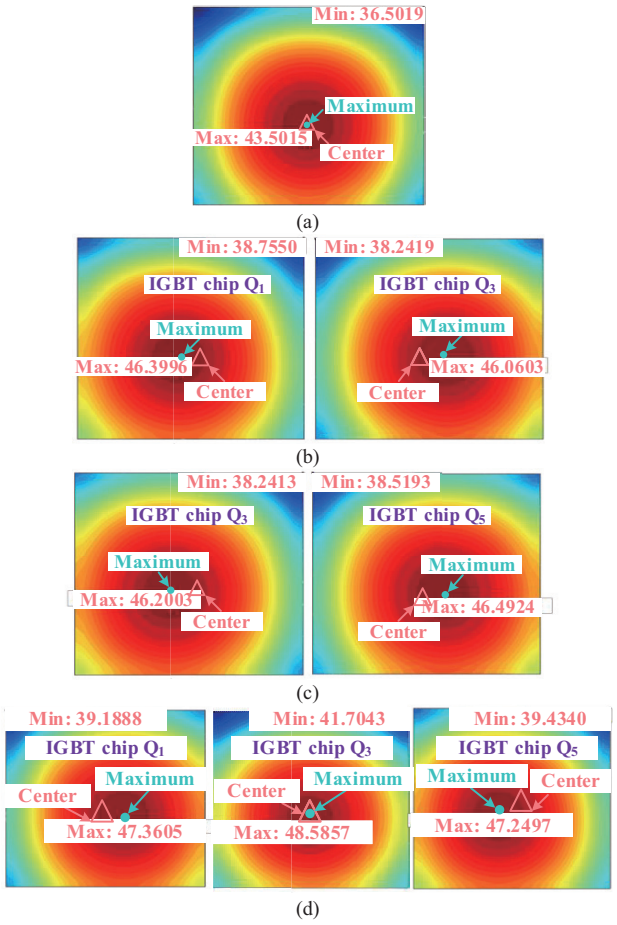

Fig. 2. Junction temperature distributions of the multi-chip IGBT module under different cases. (a) Without TCEs. (b) With the type-1 TCE. (c) With the type-2 TCE. (d) With type-3 TCE.

different types of the TCEs in multi-chip power modules are explored, and the thermal behaviors of multi-chip power module with different TCEs are illustrated in this section.

To fully explore the TCEs, the multi-chip IGBT module of Infineon FP25R12RT4 is used as a case study, which is shown in Fig. 1. Seen from Fig. 1, the tested multi-chip IGBT module includes 6 IGBT chips (i.e., Q_1, Q_2, Q_3, Q_4, Q_5, and Q_6) and 6 diode chips (i.e., W_1, W_2, W_3, W_4, W_5, and W_6).

Notably, in the upper arm of the multi-chip IGBT module, three IGBT chips (i.e., Q_1, Q_3, and Q_5) lie in the same copper layer. That means, the TCEs in the upper arm are more obvious than that in the lower arm. Considering this, three IGBT chips in the upper arm are focused on in this paper, aiming at effectively investigating the TCEs for the multi-chip power modules. It is known from Fig. 1 that there are three types of

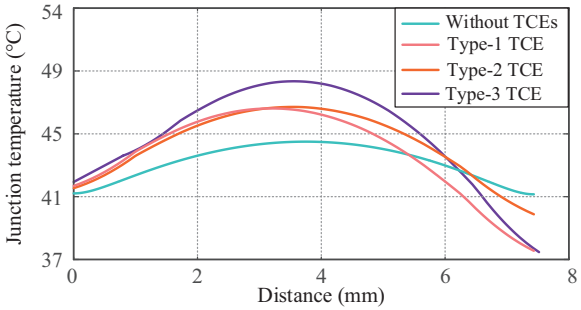

Fig. 3. Junction temperature distribution curves of the multi-chip IGBT module with different types of TCEs.

TCEs, which are listed in Table I.

Fig. 2 shows the simulation results of the multi-chip IGBT module with different types of TCEs. Seen from Fig. 2(a), when the TCEs are absent in the thermal model, the junction temperature distribution of the chip Q_3 is symmetrical, and the maximum junction temperature of the chip Q_3 is located at the center. This situation is changed when the TCEs are considered in the thermal model. That is, with the TCEs, the junction temperature distribution of the chip Q_3 becomes asymmetrical, and the maximum junction temperature in the chip Q_3 is deviated from the center (see Figs. 2(b) and 2(c)). Additionally, obvious increases of the maximum and the minimum junction temperature of the chip Q_3 are observed with the TCEs. According to Figs. 2(b) and 2(c), it is indicated the increase of junction temperature in the chip Q_3 with the type-2 TCE is larger than that with the type-1 TCE, which is because that the distance between Q_3 and Q_5 is less than that between Q_1 and Q_3 (that means, the type-2 TCE is stronger than the type-1 TCE).

It is worth noticing that the type-3 TCE induces the junction temperature redistribution in the chip Q_3. That is, the junction temperature distribution of the chip Q_3 is varied from asymmetrical to symmetrical, and the maximum junction temperature of the chip Q_3 returns to the center (see Fig. 2(d)). This is because there is a bidirectional heat conduction in the chip Q_3 with the type-3 TCE, which is roughly helpful for eliminating the asymmetrical junction temperature distributions. By contrast, both the asymmetry of the junction temperature distribution and the deviation of the maximum junction temperature from the center are clearly seen in the chips Q_1 and Q_5 with the type-3 TCE. Compared to the type-1 TCE and type-2 TCE, larger increases of the maximum and the minimum junction temperature in the chips Q_1, Q_3, and Q_5 are obviously observed with the type-3 TCE.

To further verify the above discussions, the junction temperature distribution curves of the multi-chip IGBT module with different types of TCEs are illustrated in Fig. 3. Seen from Fig. 3, with various TCEs, the multi-chip IGBT module exhibits different thermal behaviors. More specifically, the junction temperature distribution, the maximum and the minimum junction temperature of the multi-chip IGBT module with the TCEs are completely different.

In all, it is concluded that the TCEs will facilitate the junction temperature increase of the multi-chip IGBT module. More specifically, the stronger TCEs cause a larger increase of the junction temperature. Moreover, distinct TCEs will lead to

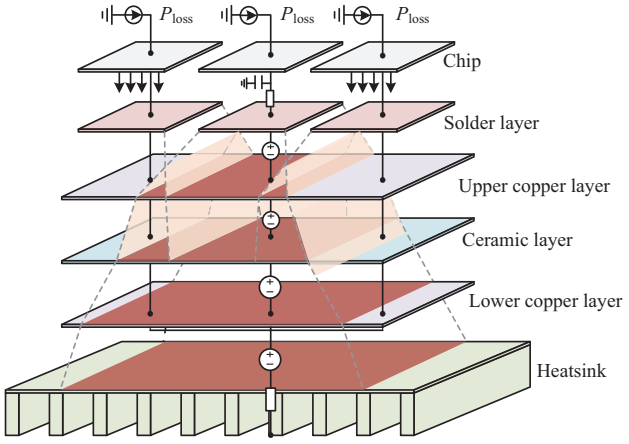

Fig. 4. Block diagram of the multi-chip IGBT module.

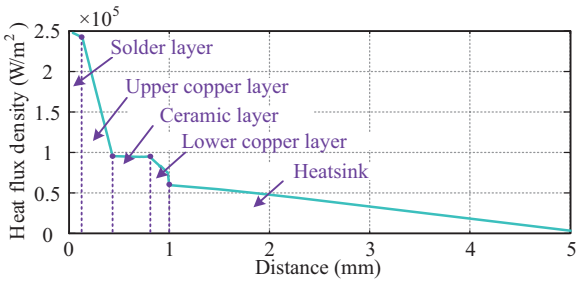

Fig. 5. Heat flux density curve of the multi-chip IGBT module.

different junction temperature distributions of the multi-chip IGBT modules.

III. Proposed Thermal Model With the TCEs

In this section, the thermal parameters of multi-chip IGBT module including the self-thermal resistances (STRs), the self-thermal capacitances (STCs), the coupling thermal resistances (CTRs), and the coupling thermal capacitances (CTCs) are collected. By doing so, the proposed thermal model is accordingly obtained.

A. Extractions of the Self-Thermal Parameters

The structure of multi-chip IGBT module of Infineon FP25R12RT4 is shown in Fig. 4, which includes 6 layers, i.e., the chip, the solder layer, the upper copper layer, the ceramic layer, the lower copper layer, and the heatsink. The chip Q_3 is used as an example to calculate the STRs and STCs at different layers of the multi-chip IGBT module.

It is known that the self-thermal parameters are related to the heat flux and the effective heat propagation area. With this, by executing the FEA simulations, the curves of the heat flux density and the effective heat propagation area are illustrated in Figs. 5 and 6, respectively. Observations in Fig. 5 suggest that the chip is the heat source, and the heat is diffused from the chip to the heatsink. As the distance from the chip increases, the heat flux density experiences a significant decrease, and accordingly, the effective heat propagation area is gradually

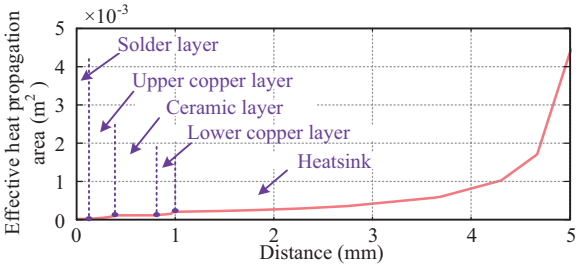

Fig. 6. Effective heat propagation area curve of the multi-chip IGBT module.

increased (see Fig. 6). Notably, because of the poor thermal conductivity of the ceramic layer, both the heat flux density and the effective heat propagation area suffer from slight variations.

With the heat flux and the effective heat propagation area, the STRs and the STCs at different layers can be calculated as [31]

$$\begin{cases} R_{\text{ths}} = \int_0^d \dfrac{1}{K_{\text{T}} A_{\text{Z}}} \mathrm{d}z \\ C_{\text{ths}} = \int_0^d c_{\text{T}} \rho A_{\text{Z}} \mathrm{d}z \end{cases} \tag{1}$$

where R_{ths}, C_{ths}, d, K_{T}, A_Z, c_{T}, and ρ are the STRs, the STCs at different layers, the thickness of different layers, the thermal conductivity, the effective heat propagation area, the specific heat capacity, and the material density, respectively. And, the effective heat propagation area is further expressed as

$$A_{\text{Z}} = \frac{P_{\text{loss}}}{q_{\text{z}}} \tag{2}$$

where q_z is the heat flux density.

Moreover, the effective heat propagation area of the chip is deliberately considered. The surface area of the chip is same to that of the solder layer, and the effective heat propagation area of the solder layer can be regarded as the surface area of the solder layer. However, referring to the chip, it is unavailable to use the surface area as the effective heat propagation area [15]. In this paper, the effective heat propagation area of the chip is obtained with the steady-state junction temperature. That is,

$$T_{\text{j}} = T_{\text{sol}} + P_{\text{loss}} \frac{\int_0^{d_{\text{c}}} \dfrac{1}{A_{\text{c}}} \mathrm{d}z}{K_{\text{Tc}}} \tag{3}$$

where T_j, T_{sol}, d_c, A_c, and K_{Tc} are the junction temperature of the chip, the junction temperature of the solder layer, the thickness of the chip, the effective heat propagation area of the chip, and the thermal conductivity of the chip, respectively. According to (3), the effective heat propagation area of the chip can be given by

$$A_{\text{c}} = \frac{P_{\text{loss}} d_{\text{c}}}{K_{\text{Tc}} (T_{\text{j}} - T_{\text{sol}})} \tag{4}$$

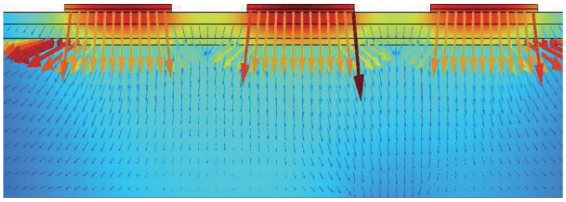

Fig. 7. Thermal diffusion path of the multi-chip IGBT module considering the TCEs.

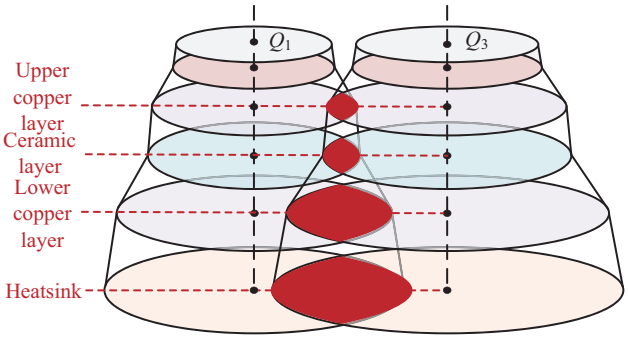

Fig. 8. Thermal diffusion path of the multi-chip IGBT module with the type-1 TCE.

B. Extractions of the Coupling Thermal Parameters

After accomplishing the extractions of the self-thermal parameters, the coupling thermal parameters are accordingly calculated in this section.

The heat flux density distribution of the multi-chip IGBT module considering the TCEs is presented in Fig. 7. Seen from Fig. 7, it is clear that the isotherms and the heat flux density distributions are varied, and different heat flux densities are crossed, which means the appearance of the TCEs. Notably, the coupling thermal parameters are highly related to the overlapping area of the thermal diffusion path between different chips [32], [33].

Taking the multi-chip IGBT module with the type-1 TCE as an example, the coupling thermal parameters are calculated. Fig. 8 illustrates the thermal diffusion path of the multi-chip IGBT module, in which the effective heat propagation area is equivalent to a circle for simplifying the thermal analysis. As shown in Fig. 8, the crossing of the thermal diffusion paths of the chips Q_1 and Q_3 starts at the upper copper layer. That is, the TCEs occur from the upper copper layer to the heatsink (see the red area in Fig. 8).

Inspired by Fig. 8, the cross-sectional area of the layer with the type-1 TCE is depicted in Fig. 9. In Fig. 9, O_1, O_3, A, B, r_1, r_3, d_{13}, and A_{z13} are the center of the effective heat propagation area of the chip Q_1, the center of the effective heat propagation area of the chip Q_3, the intersections of the two effective heat propagation areas, the radius of the effective heat propagation area of the chip Q_1, the radius of the effective heat propagation area of the chip Q_3, the distance between O_1 and O_3 (which can be measured), and the cross-sectional area (this is the area

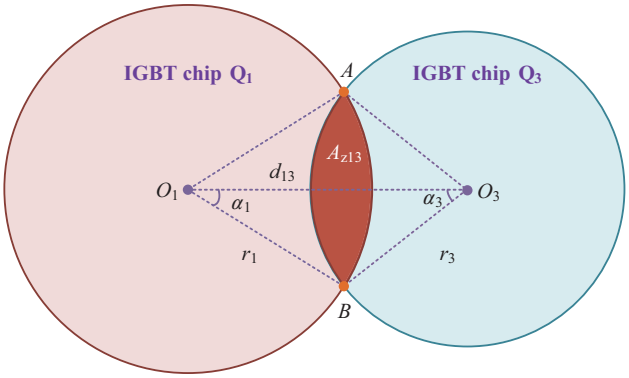

Fig. 9. Cross-sectional area of the layer with the type-1 TCE.

where the type-1 TCE occurs), respectively. According to Fig. 9, it is obtained that

$$\pi r_1^2 = A_{z1} = \frac{P_{loss1}}{q_{z1}} \tag{5}$$

With A_{z1}, P_{loss1}, and q_{z1} being the effective heat propagation area, the power losses, and the heat flux density of the chip Q_1, respectively. Subsequently,

$$r_1 = \sqrt{\frac{P_{loss1}}{\pi q_{z1}}} \tag{6}$$

Similarly, it can be given by

$$r_3 = \sqrt{\frac{P_{loss3}}{\pi q_{z3}}} \tag{7}$$

where P_{loss3} and q_{z3} are the power losses and the heat flux density of the chip Q_3, respectively. With the cosine law, it is clear that

$$\begin{cases} \cos(\alpha_1) = \dfrac{r_1^2 + d_{13}^2 - r_3^2}{2r_1 d_{13}} \\ \cos(\alpha_3) = \dfrac{r_3^2 + d_{13}^2 - r_1^2}{2r_3 d_{13}} \end{cases} \tag{8}$$

Then,

$$\begin{cases} \alpha_1 = \arccos\left(\dfrac{r_1^2 + d_{13}^2 - r_3^2}{2r_1 d_{13}}\right) \\ \alpha_3 = \arccos\left(\dfrac{r_3^2 + d_{13}^2 - r_1^2}{2r_3 d_{13}}\right) \end{cases} \tag{9}$$

With (8), it can be further obtained that

$$\sin(\alpha_1) = \sqrt{1 - \left(\frac{r_1^2 + d_{13}^2 - r_3^2}{2r_1 d_{13}}\right)^2} \tag{10}$$

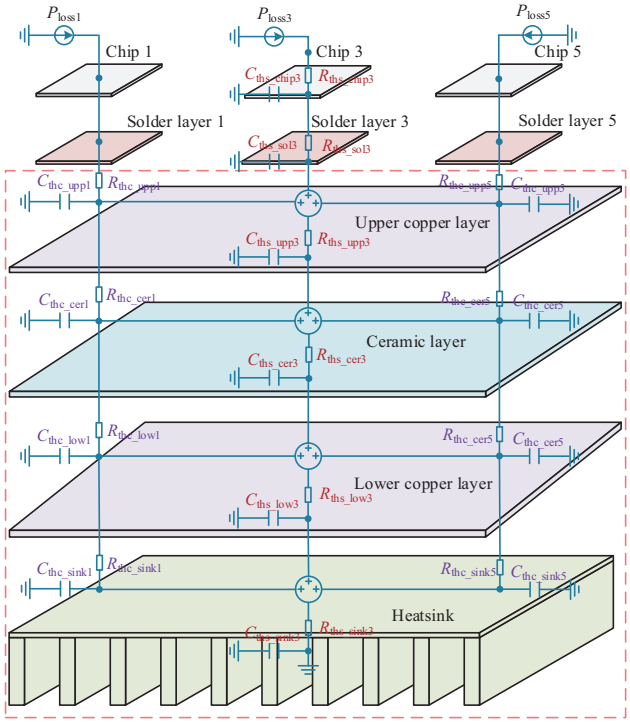

Fig. 10. Proposed thermal model of the chip Q_3 with the TCEs.

Based on Fig. 9, the cross-sectional area can be calculated as

$$A_{z13} = \alpha_1 r_1^2 + \alpha_3 r_3^2 - n_1 \sin(\alpha_1) d_{13} \tag{11}$$

It can be derived from (1) that

$$\frac{R_{thc}}{R_{ths}} = \frac{\int_0^{d_m} \frac{1}{K_T A_{z13}} dz}{\int_0^{d_m} \frac{1}{K_T A_{z1}} dz} \tag{12}$$

$$\frac{C_{thc}}{C_{ths}} = \frac{\int_0^{d_m} c_T \rho A_{z13} dz}{\int_0^{d_m} c_T \rho A_{z1} dz} \tag{13}$$

Eventually, by manipulating (12) and (13), the CTR and the CTC are given by

$$R_{thc} = R_{ths} \frac{\int_0^{d_m} \frac{1}{A_{z13}} dz}{\int_0^{d_m} \frac{1}{A_{z1}} dz} \tag{14}$$

$$C_{thc} = C_{ths} \frac{\int_0^{d_m} A_{z13} dz}{\int_0^{d_m} A_{z1} dz} \tag{15}$$

where R_{thc}, C_{thc}, and d_m are the CTR with the type-1 TCE, the CTC with the type-1 TCE, and the thickness of the layer,

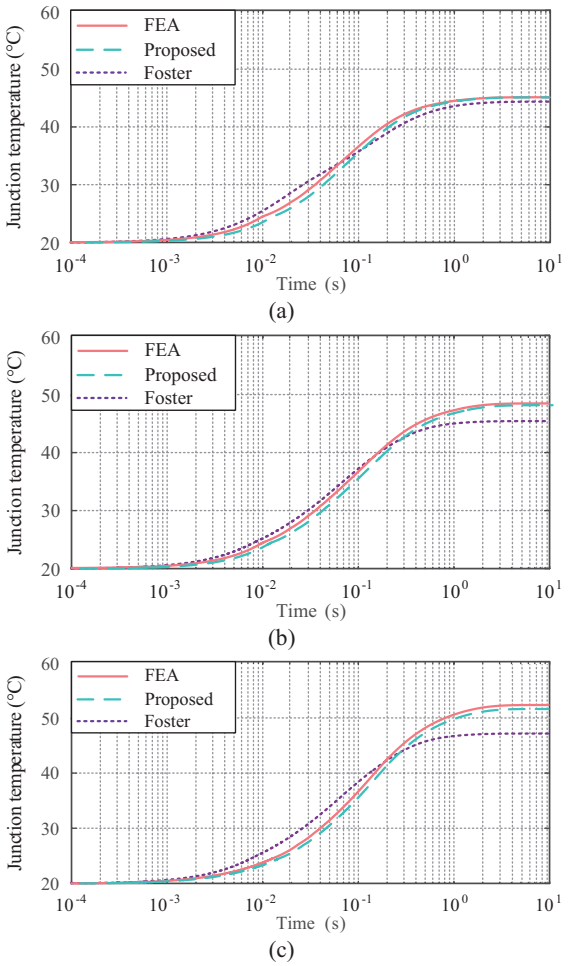

Fig. 11. Performance comparison between the proposed thermal model and the Foster model under different cases. (a) Without the TCEs, (b) With the type-1 TCE. (c) With the type-3 TCE.

respectively. Similar analysis can be adopted to extract other CTRs and CTCs, which is not described further.

After extracting the STRs, STCs, CTRs, and CTCs, the proposed thermal model is established, which is shown in Fig. 10. Seen from Fig. 10, the self-thermal parameters appear in different layers of the multi-chip power modules. While, the coupling thermal parameters are only introduced into the layers where the TCEs occur (from the upper copper layer to the heatsink).

C. Performance Analysis of the Proposed Thermal Model

To explore the effectiveness of the proposed thermal model, simulations are carried out, and a performance comparison between the proposed thermal model and the Foster model under different cases is developed, which is shown in Fig. 11. According to Fig. 11(a), the estimated junction temperature from the proposed thermal model makes a satisfactory agreement with the actual junction temperature from the FEA. By comparison, for the Foster model, a degraded junction temperature estimation performance is observed.

The same conclusion can be drawn according to Fig. 11(b), in

TABLE II
RESULTS OF ε UNDER DIFFERENT CASES

Type	Without TCEs	Type-1 TCE	Type-3 TCE
Proposed	0.33%	0.39%	0.51%
Foster	2.71%	7.04%	7.75%

which the type-1 TCE is considered in this case. Seen from Fig. 11(b), since the proposed thermal model is able to accurately characterize the type-1 TCE, an achievement of good junction temperature estimation is made through the proposed thermal model. While, as expected, the Foster model undergoes an unsatisfactory performance of junction temperature estimation due to its inadequate capability of characterizing the TCEs.

The performance of the proposed thermal model is further compared to that the Foster model under the type-3 TCE, which is presented in Fig. 11(c). As shown in Fig. 11(c), the estimated junction temperature matches the actual junction temperature well with the case of the type-3 TCE.

As for the Foster model, the type-3 TCE makes the junction temperature estimations afflicted by a large estimation error. To clearly illustrate the performance comparison, an evaluation coefficient ε is adopted as

$$\varepsilon = \frac{|T_{\text{fea}} - T_{\text{est}}|}{T_{\text{fea}}} \tag{16}$$

where T_{fea} and T_{est} are the actual junction temperature provided by the FEA and the estimated junction temperature by the thermal model, respectively. With (16), Table II concludes the results of ε under different cases, which confirms that the proposed thermal model features a better performance of junction temperature estimation, especially with the TCEs.

IV. JUNCTION TEMPERATURE ESTIMATION FOR DIFFERENT CHIPS WITH DIFFERENT TYPES OF TCES

The proposed thermal model is regarded as an estimator of junction temperature for multi-chip IGBT modules. Despite this, the estimated junction temperature disables to reflect the junction temperature of different chips of the multi-chip IGBT module. Considering this, in this section, the junction temperature estimation of different chips with the TCEs is elaborated.

Fig. 12 shows the steps of junction temperature estimation for different chips with the TCEs: the extraction of the proposed thermal model, the junction temperature estimation of the chip Q_3, the fitting of junction temperature distribution function, and the junction temperature calculations of different chips.

Step 1. Extractions of the proposed thermal model: After extracting the self-thermal parameters and the coupling thermal parameters, the thermal model is first obtained (more details can be seen in Section IV). It should be noted that the extraction of single-chip thermal network parameters in this work is supported by FEM simulations. In practical applications, such parameters are typically derived from transient thermal impedance testing, with FEM simulations employed solely as a complementary method when experimental extraction is not feasible.

Step 2. Junction temperature estimations of the chip Q_3: With the proposed thermal model, the junction temperature of the chip Q_3 under different types of TCEs is estimated.

Step 3. Fitting of junction temperature distribution functions: With the assistance of the FEA simulations, the junction temperature information with the distance of the multi-chip power module is carefully collected. Consequently, the junction temperature distribution functions of the multi-chip power module are fitted.

Step 4. Junction temperature calculations of different chips: By using the FEA simulations, multiple junction temperature distribution functions of the multi-chip power module are extracted. With the estimated junction temperature at the specific node of the chips Q_3, the specific junction temperature distribution function is determined. Then, based on the distance information of the chips Q_1 and Q_5, the junction temperature at the specific nodes of the chips Q_1 and Q_5 is calculated. Repeat the same method, and eventually, the junction temperature of the chips Q_1 and Q_5 is provided.

Moreover, to further characterize the thermal properties of multichip power module, the surface temperature distribution of the multi-chip module obtained through FEA simulation analysis is shown in Fig. 13, and the temperature data of the chips was collected along the diagonal line marked on the left side of Fig. 13(a). Generally, the quadratic function is assigned to extract the junction temperature distributions of different chips [34], [35]. Therefore, based on Fig. 13, it can be given by

$$\begin{cases} T_{\text{j1}}(x) = -0.4496x^2 + 30.32x + 46.91 \\ T_{\text{j3}}(x) = -0.4504x^2 + 27.18x + 49.82 \\ T_{\text{j5}}(x) = -0.4842x^2 + 34.82x + 45.08 \end{cases} \tag{17}$$

where T_{j1}, T_{j3}, T_{j5}, and x are the junction temperature of the chip Q_1, the junction temperature of the chip Q_3, the junction temperature of the chip Q_5, and the horizontal distance of the chip (unit: mm), respectively.

The same method is applied for the multi-chip IGBT module, and the 2-D junction temperature distribution functions of different chips can be obtained that

$$T_{\text{j}}(x, y) = ax^2 + bx + cy^2 + dy + f \tag{18}$$

where a, b, c, d, f, and y are the fitted gains of the 2-D junction temperature distribution function and the vertical distance of the chip (unit: mm), respectively.

Table III lists the 2-D junction temperature distribution functions of different chips with the TCEs. Generally, the determination coefficient is used to evaluate the performance of the fitted junction temperature distribution functions, and a large

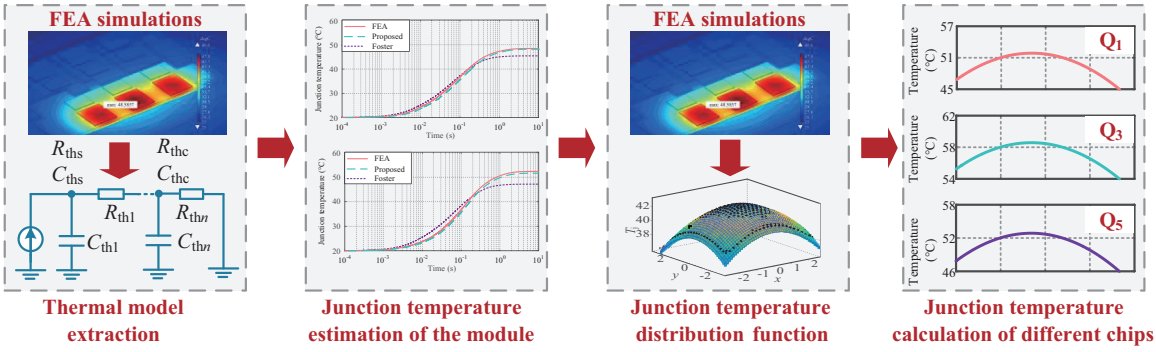

Fig. 12. Steps of junction temperature estimation for different chips of the multi-chip IGBT module with the TCEs.

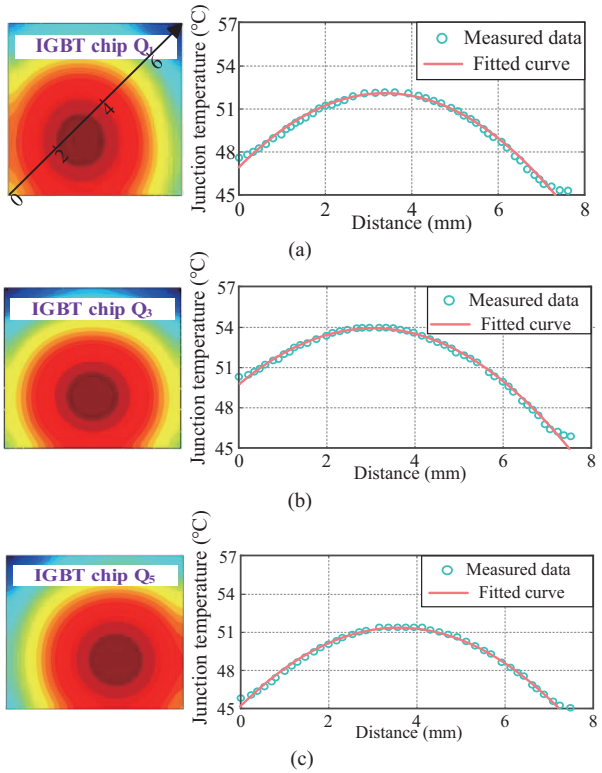

Fig. 13. Junction temperature distribution functions of different chips. (a) The chip Q_1. (b) The chip Q_3. (c) The chip Q_5.

TABLE III
2-D Junction Temperature Distribution Functions of Different Chips Under Different Types of TCEs

Test case	2-D junction temperature distribution function	Determination coefficient
Without TCEs	$T_{j3}(x,y) = -57x^2+110x-38y^2-72.07y-41.3$	0.9912
Type–1 TCE	$T_{j1}(x,y) = -51x^2-3.038x-39y^2-5.024y+45.26$	0.9909
	$T_{j3}(x,y) = -51x^2+4.072x-39y^2-75.44y+8.87$	0.9912
Type–2 TCE	$T_{j3}(x,y) = -52x^2-4.54x-39y^2-4.732y+45.83$	0.9916
	$T_{j5}(x,y) = -52x^2+4.3x-40y^2-4.938y+46.12$	0.9915
Type–3 TCE	$T_{j1}(x,y) = -50x^2-3.69x-39y^2-5.104y+45.38$	0.9912
	$T_{j3}(x,y) = -46x^2-0.253x-41y^2-4.975y+47.16$	0.9915
	$T_{j5}(x,y) = -52x^2+4.86x-40y^2-4.912y+45.86$	0.9917

TABLE IV
Junction Temperature Estimation Performance of Different Chips Under Different TCEs

Test case	Chips	Actual junction temperature	Estimated junction temperature	ε
Type–1 TCE	Q_1	53.84 °C	53.6 °C	0.45%
	Q_3	53.37 °C	53.15 °C	0.41%
Type–2 TCE	Q_3	53.51 °C	53.28 °C	0.42%
	Q_5	53.87 °C	53.6 °C	0.50%
Type–3 TCE	Q_1	54.56 °C	54.32 °C	0.44%
	Q_3	56.38 °C	56.16 °C	0.38%
	Q_5	54.56 °C	54.33 °C	0.42%

determination coefficient means an acceptable performance. According to Table III, it is clear that the fitted junction temperature distribution functions allow to reflect the junction temperature distributions of different chips with the TCEs.

With the proposed thermal model and the extracted junction temperature distribution functions, the junction temperature at the chip center for different chips with the TCEs is calculated, which can be seen in Table IV. Seen from Table IV, it is suggested that the proposed thermal model features a satisfactory thermal characterization performance under different types of TCEs. More specifically, a good matching between the estimated junction temperature and the actual junction temperature is provided, and a limited junction temperature estimation error is maintained.

V. Experimental Tests

A. Test Bench

To validate the effectiveness of the proposed thermal model, experiments are performed on a three-phase inverter test bench, as shown in Fig. 14, respectively. The test bench includes a main circuit, a junction temperature measurement circuit, and a controller. The main circuit consists of a DC power supply (Chroma 62180D-600), a three-phase inverter, the tested IGBT module (Infineon FP25R12RT4), the driver board, the sampling board, and an oscilloscope (Teledyne LeCroy HDO

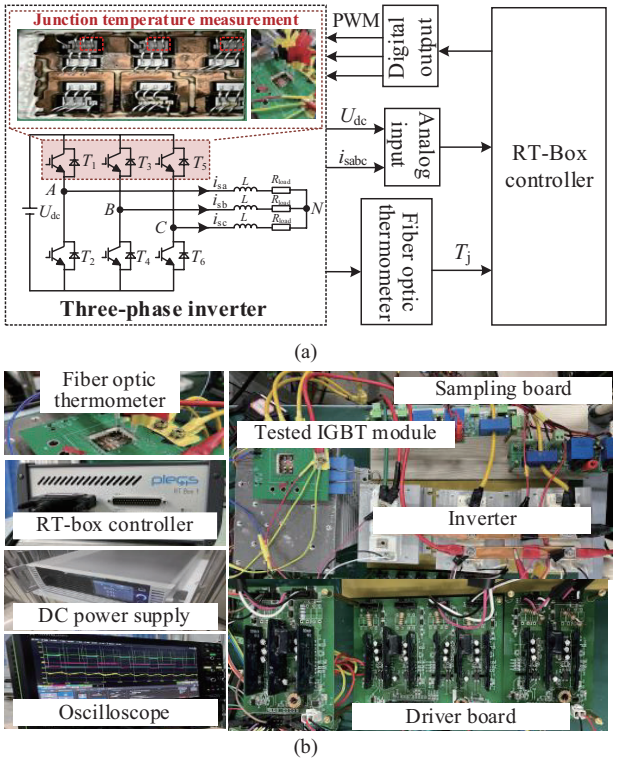

Fig. 14. A three-phase inverter test bench. (a) The block diagram of the test bench. (b) The photo of the test bench.

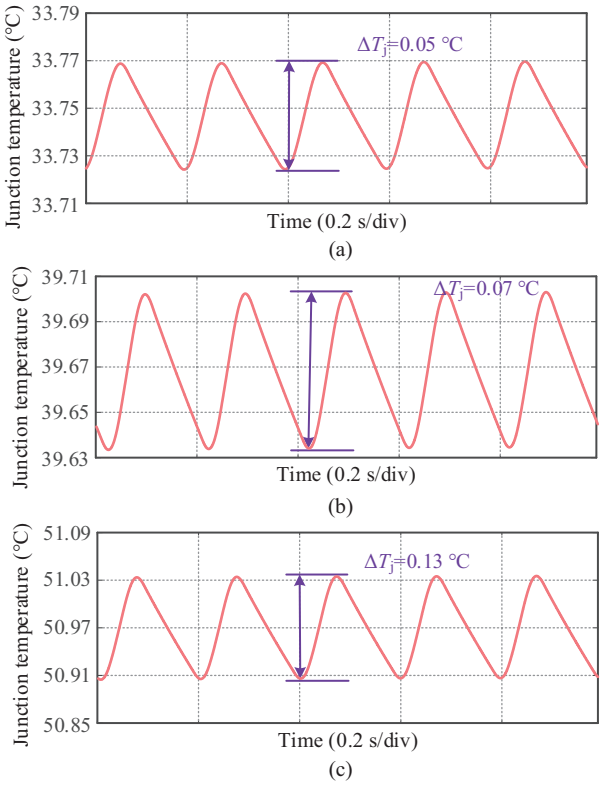

Fig. 15. Junction temperature of the chip Q_3 with the fundamental frequency of 5 Hz under different load currents. (a) 7.5 A. (b) 10 A. (c) 15 A.

6104B). And, three resistances and three inductances are used to emulate the load of the three-phase inverter. It is noting that in the junction temperature measurement circuit, the fiber optic thermometer (Opsens CSC-4U-S13) is adopted to obtain the junction temperature information of different chips of the tested multi-chip IGBT module. Moreover, the whole control strategy of the three-phase inverter is implemented by the RT-Box controller (RT-Box 1).

Notably, in the experimental tests, the upper arm of the multi-chip IGBT module is used as the case study (see Fig. 14(a)). And, the three chips share the same drive signal, and different types of TCEs are simulated by controlling the on-off actions of different chips. For example, to simulate the type-1 TCE, the chips Q_1 and Q_3 are in the on-state while the chip Q_5 is in the off-state by controlling the drive signal. Additionally, the three chips Q_1, Q_3, and Q_5 are in the on-state to simulate the type-3 TCE.

B. Thermal Behaviors of the Multi-Chip IGBT Module With TCEs

Experimental tests are first carried out to explore the thermal behaviors of the multi-chip IGBT module with the TCEs, and the corresponding results are provided in Fig. 15, where the chip Q_3 is taken as an example. In this case, the power losses are injected into the chips Q_1 and Q_5, and the power losses are absent in the chip Q_3. Moreover, the fundamental frequency is set to 5 Hz. Observations in Fig. 15(a) indicate that even without the injected power losses, the junction temperature increase of the chip Q_3 still can be observed, and the chip Q_3 suffers from the issue of junction temperature swings. This becomes serious when the load current is increased. That is, the increase of the load current will expand the TCEs, and then, apparently affects the thermal behaviors of the multichip IGBT module (see Figs. 15(b) and (c)).

Additionally, the TCEs with a small fundamental frequency of 1 Hz are experimentally investigated, which is shown in Fig. 16. Seen from Fig. 16, as expected, the increases of the junction temperature and obvious junction temperature swings are observed in the chip Q_3 under the TCEs. Notably, compared to Fig. 15, it is clear that a small fundamental frequency leads to larger junction temperature swings with the TCEs, which is attributed that with a small fundamental frequency, the time of the fundamental period becomes longer. As a consequence, the time of on-off actions of the multi-chip IGBT module also becomes longer. Due to this, more power losses generated from the chips Q_1 and Q_5 diffuse to the chip Q_3, causing larger junction temperature swings.

C. Performance of the Proposed Thermal Model Under Different Cases

Then, the performance of the proposed thermal model under different cases is extensively explored through experimental tests. In Fig. 17, different TCEs are applied, and the fundamental frequency and the load current are set to 5 Hz and 5 A, respectively. According to Fig. 17, the estimated junction temperature makes a satisfactory agreement with the actual junction temperature under different types of TCEs, and

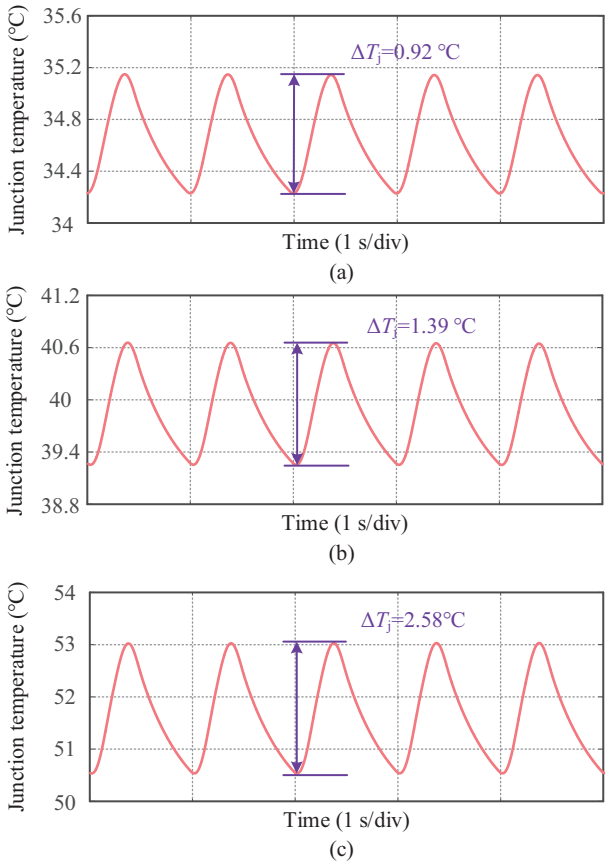

Fig. 16. Junction temperature of the chip Q_3 with the fundamental frequency of 1 Hz under different load currents. (a) 7.5 A. (b) 10 A. (c) 15 A.

a narrow range of junction temperature estimation errors is observed. Moreover, it is also seen from Fig. 17 that with the TCEs, both the average junction temperature and the junction temperature swings of the chip Q_3 are increased, which further justifies the effectiveness of the thermal characterization analysis of the multi-chip IGBT module with the TCEs.

To further investigate the performance of the proposed thermal model with the TCEs, the corresponding experimental tests are implemented. In Fig. 18, the type-2 TCE is used as a case study, and the fundamental frequency is set to 10 Hz. Moreover, different load currents (e.g., 5 A, 7.5 A, and 10 A) are applied. Seen from Fig. 18, the estimated junction temperature approaches the actual junction temperature well with different load currents, and the estimation errors are limited in the range of ±1 °C, which means that the load current variations show an insignificant effect on the performance of the proposed thermal model. The performance of the proposed thermal model with the type-3 TCE is verified, and the experimental results are illustrated in Fig. 19. The load current of 10 A and three fundamental frequencies of 1 Hz, 5 Hz, and 10 Hz are adopted in this case. Observations in Fig. 19 suggest that the proposed thermal model is the enabler of providing a satisfactory thermal characterization with different fundamental frequencies, which makes the junction temperature estimation errors lie in a small range. That is, the proposed thermal model is free from the effects of fundamental frequency variations.

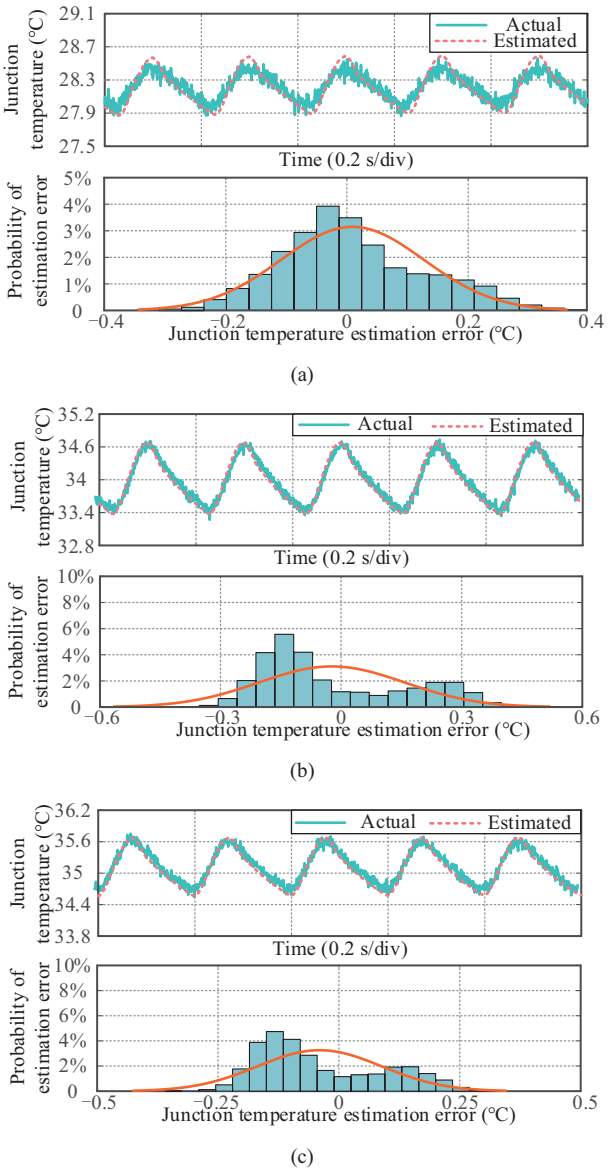

Fig. 17. Junction temperature estimation performance of the chip Q_3 under different cases. (a) Without the TCEs. (b) with the type-2 TCE. (c) With the type-3 TCE.

VI. Conclusion

The thermal model was devoted to characterize the thermal properties of power modules. However, many thermal models experienced an undesirable thermal analysis accuracy due to the presence of the TCEs, especially in the multi-chip power modules. To address this, a thermal model with the capability of characterizing various TCEs was proposed in this paper for multi-chip IGBT modules. Starting from a brief introduction of the classical thermal models, the TCEs on the performance of the classical thermal network models were detailed. Afterward, the thermal behaviors of the multi-chip IGBT module with the TCEs were thoroughly analyzed. According to the thermal analysis, the self-thermal parameters and the coupling thermal parameters were calculated, and then, the proposed thermal

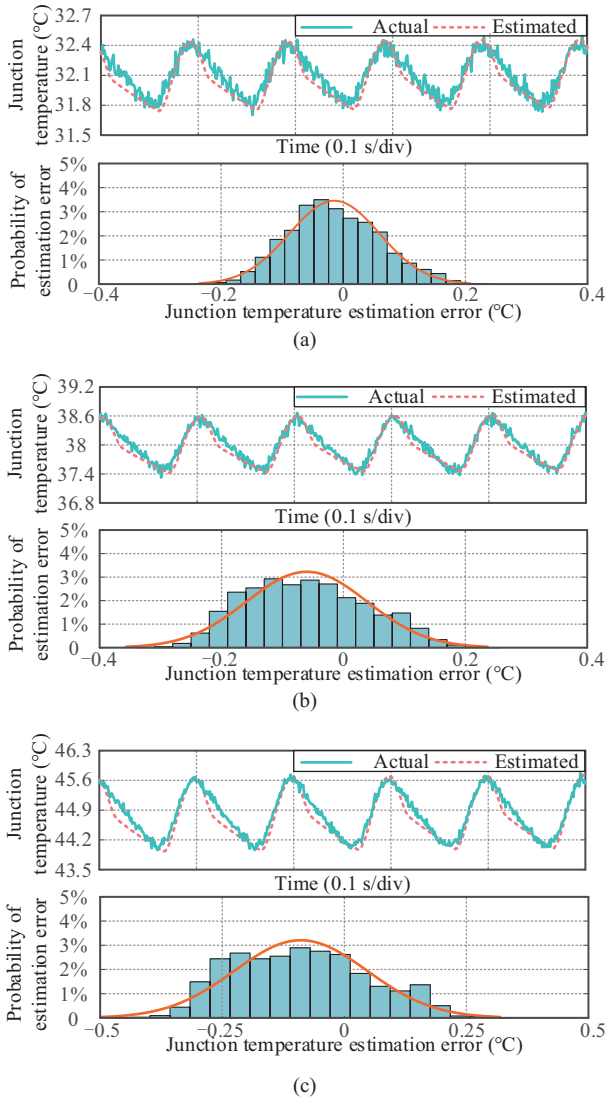

Fig. 18. Junction temperature estimation performance of the chip Q_3 with the type-2 TCE under different load currents. (a) 5 A. (b) 7.5 A. (c) 10 A.

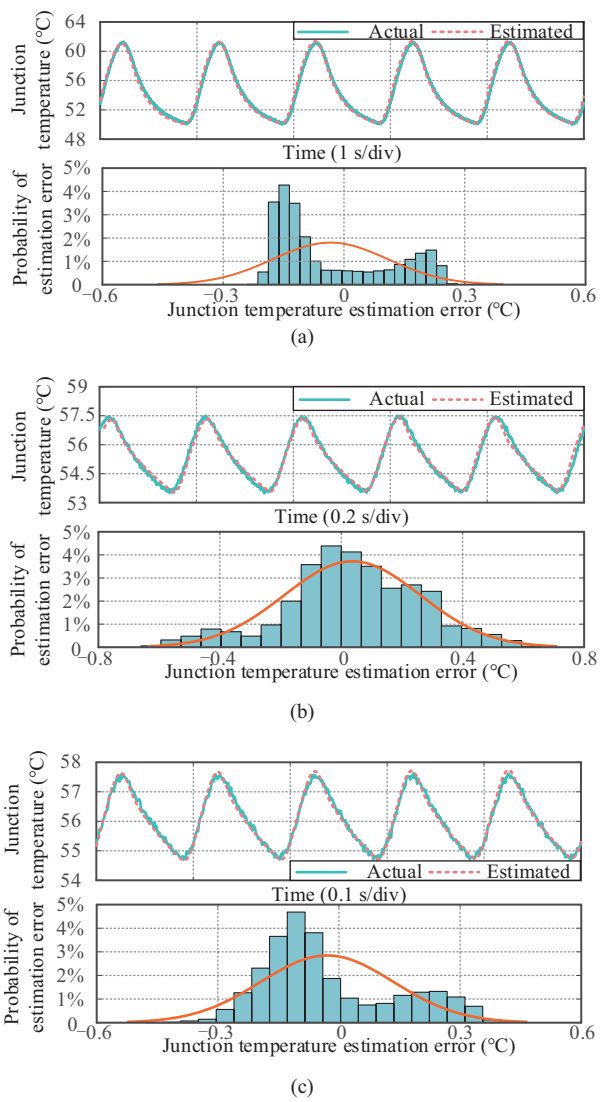

Fig. 19. Junction temperature estimation performance of the chip Q_3 with the type-3 TCE under different fundamental frequencies. (a) 1 Hz. (b) 5 Hz. (c) 10 Hz.

model was established.

Since the estimated junction temperature from the proposed thermal model cannot accurately reflect the junction temperature information of different chips, a solution using the junction temperature distribution function was developed, enabling precise estimation of the junction temperatures of various chips. Experimental tests were conducted to validate the effectiveness of the proposed thermal model under various conditions. Experimental results show that the proposed thermal model is effective in illustrating the thermal behaviors of the multi-chip IGBT module with the TCEs. Consequently, the benefit of accurately estimating the junction temperature of different chips was achieved.

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