Optimization Strategy for Continuous Control Set Model Predictive Control in Three-Phase Four-Wire Three-Level Inverter

Aiwen QU, Yixin ZHANG, and Jianhua XUE

***Abstract*—To enhance the output voltage quality and system efficiency of a three-phase four-wire (3P4W) three-level inverter under unbalanced load conditions, this paper proposes an optimization strategy for continuous control set model predictive control (CCS-MPC) based on hybrid modulation. First, an active damping method employing a notch filter is integrated into the CCS-MPC to suppress resonance caused by load-filter interactions, improving the output voltage quality. Phase correction is also applied to the output voltage reference generated via two-step prediction. Second, based on neutral-point (NP) voltage balancing control, a fuzzy logic algorithm (FLA)-based hybrid pulse width modulation (HPWM) method is proposed to further increase system efficiency. The FLA evaluates NP voltage fluctuation amplitude and balancing capability to adaptively determine whether to disassemble the O switching state, enabling optimal combination of dual-carrier sinusoidal pulse width modulation (SPWM) and double modulation wave carrier-based pulse width modulation (DMW-CBPWM). Compared with traditional zero-level disassembly (ZD) method, the proposed FLA-based HPWM method maintains NP voltage balance while achieving higher system efficiency. Finally, the feasibility and effectiveness of the proposed optimization strategy are verified by simulation and experiment results.**

***Index Terms*—Active damping, fuzzy logic algorithm, hybrid modulation, model predictive control, three-level inverter.**

I. Introduction

With the development of power electronics technology, the T-type three-level inverter demonstrates advantages over two-level inverter including lower output voltage harmonics, reduced voltage stress on switching devices, reduced electromagnetic interference (EMI), and smaller filter inductor volumes. These characteristics make it particularly suitable for applications in distributed power generation systems and uninterruptible power supply (UPS) [1]–[4]. The three-phase four-wire (3P4W) T-type three-level inverter utilizes a neutral wire to decouple the three phases. This enables independent control of phase voltages and provides better power quality under unbalanced loads conditions.

A critical challenge for three-level inverters is neutral-point (NP) voltage fluctuation. This fluctuation increase the low-order harmonics in output voltage and the voltage stress on switching devices, while also reducing the service life of DC-link capacitors [5], [6]. Compared to traditional linear control methods, model predictive control (MPC) has advantages including fast dynamic response, simple structure, and fewer adjustable parameters, and has been extensively applied [7]–[13]. MPC is primarily categorized into finite control set model predictive control (FCS-MPC) and continuous control set model predictive control (CCS-MPC). FCS-MPC generally achieves NP voltage balancing by optimizing the selection of switching action vectors, which increases the computational burden and system complexity [14]. In contrast, CCS-MPC integrates deadbeat control with improved modulation strategies to maintain NP voltage balance. This approach reduces the number of calculations to a single iteration per control cycle, significantly decreasing the computational burden and complexity of the control system [4].

A significant research directions for three-level inverters involves enhancing system performance through hybrid modulation strategies that combine different switching techniques. [15] proposes a hybrid modulation strategy combining space vector pulse width modulation (SVPWM) and virtual SVPWM (VSVPWM). This approach achieves NP voltage balance across full output voltage ranges and for all-load power factors with a minimum output voltage switching-frequency distortion. [16] presents a hybrid modulation strategy based on dual modulation wave single carrier modulation. This method achieves NP voltage balance under full modulation index and full power factor with low switching losses, by decomposing the zero-sequence injected phase voltage modulation waves under the constraints of switching times and unconditional balanced neutral point voltage. [17] introduces a hybrid active modulation strategy that employs different modulation methods during system startup and generation mode: the nearest three vector is used in the startup process and an enhanced carrier-based virtual-space-vector modulation technique is involved in generation mode. This strategy aims to eliminate NP voltage fluctuation, suppress common-mode voltage, and reduce

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switching losses. [18] proposes a hybrid carrier-based pulse width modulation (PWM) method to obtain the suitable values of three degrees of freedom, thereby achieving the maximum controllability of the NP voltage across the full range of the power factor and the modulation index with a lower switching frequency. The three degrees of freedom include zero-sequence voltage, zero-level disassembly phase, and the extent of zero-level disassembled. [15]–[18] all focus on optimizing system performance under balanced load conditions by hybridizing the corresponding modulation strategies and leveraging the advantages of each modulation strategy in different time intervals. However, they did not investigate unbalanced load conditions with aggravated NP voltage fluctuations.

To enhance the performance of the 3P4W three-level inverter under unbalanced load conditions, some modulation strategies have been proposed [4], [19], [20]. The zero-level disassembly (ZD) method [19] selects a phase for disassembly based on the NP control margin (NPCM) value. The selected phase employs double modulation wave carrier-based PWM (DMW-CBPWM), while the other phases utilize dual-carrier sinusoidal PWM (SPWM). However, this method can increase switching losses, particularly when the NP voltage fluctuation is minimal and the maximum NPCM is positive small. [4] proposes a zero-sequence voltage injection method using CBPWM to mitigate NP voltage fluctuations. A drawback of this approach is the generation of a zero-sequence current within the inherent zero-sequence loop, which may distort output voltage and current waveforms. [20] proposes a compensation-based 3D space vector PWM (3D-SVPWM) strategy. This method constructs the 3D space vector diagram using the real-time sampling values of positive and negative DC-link voltages. It optimizes subsector subdivision based on basic vector positions and recalculates vector dwell times, maintaining high-quality output voltage waveforms even during significant NP oscillations caused by asymmetrical loads. Nevertheless, SVPWM-based methods like this are generally more complex to implement than CBPWM approaches. Furthermore, resonance can occur in the 3P4W T-type three-level inverter with LC filters under resistive-inductive load or no-load conditions, adversely affecting the output power quality and the system's stable operation. However, the resonance caused by load-filter interactions was not considered in [4], [19], [20].

To suppress system resonance, a passive damping method using a filter capacitor in series with a resistor can be employed [21]. However, this method attenuates high-frequency harmonics less effectively, increasing output voltage total harmonic distortion (THD) and reducing system efficiency. [22] proposes an active damping method utilizing a virtual resistor in parallel with the filter capacitor. However, this method is suitable for MPC with output current as the control objective, but not applicable to MPC with output voltage as the control objective.

Based on the above analysis, a hybrid CBPWM-based optimization strategy for CCS-MPC is proposed to enhance the output voltage quality and system efficiency of a 3P4W three-level inverter under unbalanced load conditions. The effectiveness of this proposed strategy is validated through both simulations and experiments.

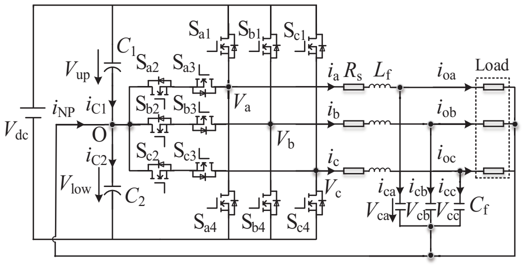


Fig. 1. 3P4W T-type three-level inverter topology.

TABLE I
3P4W T-Type Three-Level Inverter Switching Status

S_{x1}	S_{x2}	S_{x3}	S_{x4}	Switching State
1	1	0	0	P
0	1	1	0	O
0	0	1	1	N

The two main innovations of this paper are as follows:

1) To enhance the output voltage quality of 3P4W three-level inverter under unbalanced load conditions, an active damping method with a notch filter is proposed for CCS-MPC to suppress resonance arising from load-filter interaction. Additionally, the phase of the output reference voltage is corrected to compensate for the phase lag introduced by the notch filter.

2) To achieve coordinated control of NP voltage balance and system efficiency, a hybrid PWM method based on fuzzy logic algorithm (FLA) (termed FLA-based HPWM) is proposed, which optimally combines dual-carrier SPWM and DMW-CBPWM.

II. Mathematical Model

The 3P4W three-level inverter studied in this paper employs a T-type three-level topology, as shown in Fig. 1. Each phase leg comprises four switching devices. The switching devices S_{x1} and S_{x3}, as well as S_{x2} and S_{x4} (x=a, b, c), are driven with complementary gating signals. Table I details the relationship between the switching states in phase-x and the corresponding on/off status of these devices. Fig. 2 depicts the energy flow paths associated with the P, O, and N switching states under the condition i_x>0. Notably, operation in either the P or N switching state results in fluctuations of the DC-link NP voltage.

Based on Fig. 1, the mathematical model of the system can be derived as:

$$\begin{cases} V_{xo} = L_f \dfrac{\mathrm{d}i_x}{\mathrm{d}t} + R_s i_x + V_{cx} \\ i_x - i_{ox} = C_f \dfrac{\mathrm{d}V_{cx}}{\mathrm{d}t} \end{cases} \tag{1}$$

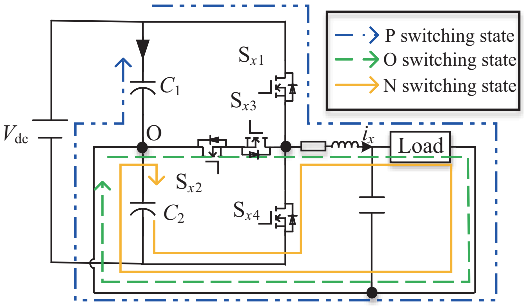


Fig. 2. Schematic diagram of energy flow under three switching states (i_x>0).

where x=a, b, c represents phase-a, phase-b, and phase-c; V_{xo} denotes the inverter-side bridge leg voltage; V_{cx} represents the three-phase output voltages; i_x indicates the inverter-side currents; i_{ox} represents the three-phase load currents; R_s, L_f, and C_f are the parasitic resistance of the filter inductor, filter inductor, and filter capacitance, respectively.

By discretizing (1) using the forward Euler method, the predictive model at the (k+1)th instant can be derived as

$$\begin{cases} i_x(k+1)=i_x(k)+\dfrac{T_s}{L_f}\left(V_{xo}(k)-R_si_x(k)-V_{cx}(k)\right) \\ V_{cx}(k+1)=V_{cx}(k)+\dfrac{T_s}{C_f}\left(i_x(k)-i_{ox}(k)\right) \end{cases} \tag{2}$$

where T_s represents the sampling period; $i_x(k)$, $V_{xo}(k)$, $V_{cx}(k)$, and $i_{ox}(k)$ represent the inverter-side current, inverter-side leg voltage, output voltage, and load current of phase-x (x=a, b, c) at the kth instant, respectively; $i_x(k+1)$ and $V_{cx}(k+1)$ represent the inverter-side current and output voltage of phase-x at the (k+1)th instant, respectively.

III. OPTIMIZATION STRATEGY FOR CCS-MPC

A. Two-Step Prediction Compensation

MPC aims to rapidly and accurately track the inverter's three-phase output voltage reference. Addressing practical control delay effects within the system, a two-step prediction compensation method [4] is utilized. The cost function is constructed as:

$$g_{cx}=\left[V_{cx}^*(k+2)-V_{cx}(k+2)\right]^2 \tag{3}$$

where $V_{cx}(k+2)$ and $V_{cx}^*(k+2)$ (x=a, b, c) represent the predictive value and the reference value for phase-x output voltage at the (k+2)th sampling period, respectively.

$V_{cx}^*(k+2)$ can be expressed as

$$\begin{cases} V_{ca}^*(k+2)=V_m\cos\left[\omega_n(k+2)T_s\right] \\ V_{cb}^*(k+2)=V_m\cos\left[\omega_n(k+2)T_s-2\pi/3\right] \\ V_{cc}^*(k+2)=V_m\cos\left[\omega_n(k+2)T_s+2\pi/3\right] \end{cases} \tag{4}$$

where V_m denotes the magnitude of output voltage references, and ω_n is the reference angular frequency.

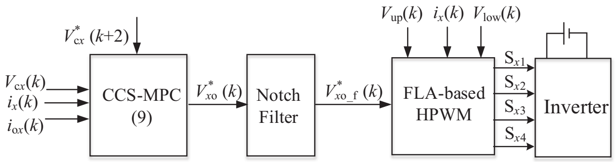


Fig. 3. System control block diagram.

From (2), $V_{cx}(k+2)$ is obtained as

$$V_{cx}(k+2)=V_{cx}(k+1)+\frac{T_s}{C_f}\left(i_x(k+1)-i_{ox}(k+1)\right) \tag{5}$$

Substituting (2) into (5), $V_{cx}(k+2)$ is expressed as

$$\begin{aligned} V_{cx}(k+2)=(1-\frac{T_s^2}{L_fC_f})V_{cx}(k)+(\frac{2T_s}{C_f}-\frac{T_s^2R_s}{L_fC_f})i_x(k)+ \\ \frac{T_s^2}{L_fC_f}V_{xo}(k)-\frac{T_s}{C_f}i_{ox}(k)-\frac{T_s}{C_f}i_{ox}(k+1) \end{aligned} \tag{6}$$

From (3), the first-order derivative of the cost function can be obtained as

$$\frac{\partial g_{cx}[V_{xo}(k)]}{\partial V_{xo}(k)}=-2\left[V_{cx}^*(k+2)-V_{cx}(k+2)\right]\frac{\partial V_{cx}(k+2)}{\partial V_{xo}(k)} \tag{7}$$

From (6) and (7), the second-order derivative of the cost function is derived as

$$\frac{\partial^2 g_{cx}[V_{xo}(k)]}{\partial V_{xo}(k)^2}=\frac{2T_s^4}{L_f^2C_f^2}>0 \tag{8}$$

Since the second-order derivative of the cost function is positive, its first-order derivative is monotonically increasing. Minimizing the cost function therefore requires its first-order derivative to be zero, leading to $V_{cx}(k+2)=V_{cx}^*(k+2)$. Given that the sampling frequency is significantly higher than the fundamental frequency of output voltages, the load current can be assumed constant within a single sampling period, expressed as $i_{ox}(k+1)\approx i_{ox}(k)$ [4]. Consequently, the inverter-side leg reference voltage $V_{xo}^*(k)$ (x=a, b, c) at kth instant is derived from (6) as

$$\begin{aligned} V_{xo}^*(k)=2L_f/T_si_{ox}(k)+(R_s-2L_f/T_s)i_x(k)+ \\ (1-L_fC_f/T_s^2)V_{cx}(k)+L_fC_f/T_s^2V_{cx}^*(k+2) \end{aligned} \tag{9}$$

B. CCS-MPC With Active Damping

Taking the output voltage as the control objective, the resonance can occur in the inverter system under no-load or resistive-inductive load conditions, leading to system instability. To suppress resonance, an active damping method integrating a notch filter within MPC framework is proposed in this paper. The system control block diagram is illustrated in Fig. 3.

The continuous-domain transfer function of the notch filter in Fig. 3 is expressed as

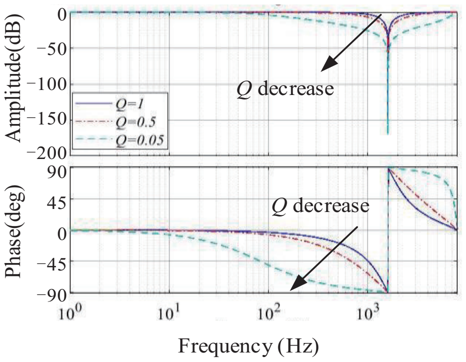


Fig. 4. Bode diagram of the discretized notch filter.

$$H(s)=\frac{s^2+\omega_f^{\,2}}{s^2+\omega_f s/Q+\omega_f^{\,2}} \tag{10}$$

where Q denotes the quality factor of the notch filter; ω_f is the notch angular frequency.

The amplitude-frequency characteristic $A(\omega)$ and phase-frequency characteristic $\varphi(\omega)$ of the notch filter are given by

$$\begin{cases} A(\omega)=20\ \lg\dfrac{|1-(\omega/\omega_f)^2|}{\sqrt{[1-(\omega/\omega_f)^2]^2+[\omega/(\omega_f Q)]^2}} \\ \varphi(\omega)=-\arctan[\omega_f\omega/(Q(\omega_f^{\,2}-\omega^2))] \end{cases} \tag{11}$$

To ensure effective resonance suppression, ω_f is set equal to the system's resonance angular frequency ω_r, with the notch bandwidth $\Delta\omega=0.1\omega_r$. Furthermore, the notch depth $A(\omega_r\pm\Delta\omega)$ at frequencies $\omega_r\pm\Delta\omega$ is no greater than the negative amplitude of the system's output voltage at the resonant angular frequency. Applying the bilinear transform method, the notch filter transfer function is discretized as follows

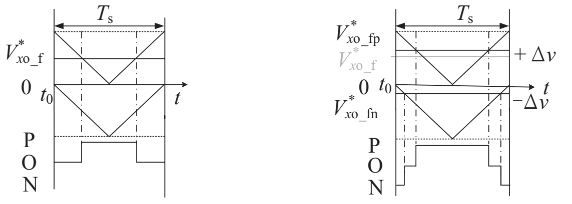
$$\begin{aligned} H(z)&=\left.\frac{s^2+\omega_f^{\,2}}{s^2+\omega_f s/Q+\omega_f^{\,2}}\right|_{s=\frac{2}{T_s}\cdot\frac{1-z^{-1}}{1+z^{-1}}} \\ &=\frac{a_1+b_1z^{-1}+a_1z^{-2}}{(a_1+c_1)+b_1z^{-1}+(a_1-c_1)z^{-2}} \end{aligned} \tag{12}$$

where

$$\begin{cases} a_1=4+(\omega_f T_s)^2 \\ b_1=-8+2(\omega_f T_s)^2 \\ c_1=2\omega_f T_s/Q \end{cases} \tag{13}$$

Fig. 4 presents the Bode diagram of the discretized notch filter. The plot demonstrates that a lower quality factor Q results in a wider notch bandwidth and greater attenuation capability for resonance peaks. Consequently, Q is set to 0.05 in this study.

After processing by the notch filter, the amplitude of the fundamental frequency signal remains unchanged while incurring a phase lag. Therefore, $V^*_{cx}(k+2)$ (x=a, b, c) requires phase compensation.



(a) (b)

Fig. 5. PWM sequence generated using different modulation methods ($V^*_{xo\_f}>0$). (a) Dual-carrier SPWM. (b) DMW-CBPWM.

$$\begin{cases} V^*_{ca}(k+2)=V_m\cos\left(\omega_n T_s(k+2)+\dfrac{2\pi\psi_x}{360°}\right) \\ V^*_{cb}(k+2)=V_m\cos\left(\omega_n T_s(k+2)+\dfrac{2\pi\psi_x}{360°}-\dfrac{2\pi}{3}\right) \\ V^*_{cc}(k+2)=V_m\cos\left(\omega_n T_s(k+2)+\dfrac{2\pi\psi_x}{360°}+\dfrac{2\pi}{3}\right) \end{cases} \tag{14}$$

where ψ_x denotes the angular deviation of the fundamental frequency signal after passing through the notch filter.

C. Hybrid Modulation Method

Under unbalanced load conditions, the 3P4W T-type three-level inverter experiences aggravated NP voltage fluctuation. To mitigate this NP voltage imbalance while simultaneously optimizing system efficiency, a hybrid modulation method combining DMW-CBPWM and dual-carrier SPWM based on FLA is proposed in this study.

1) Dual-Carrier SPWM

Fig. 5(a) presents the PWM sequence generated using dual-carrier SPWM during the positive half-cycle of the output modulation signal. With this modulation strategy, the neutral-point current i_{NP} that affects NP voltage fluctuation can be derived from Fig. 1.

$$i_{NP}=2(|V^*_{ao\_f}|\,i_a+|V^*_{bo\_f}|\,i_b+|V^*_{co\_f}|\,i_c)/V_{dc} \tag{15}$$

where V_{dc} denotes the DC-link voltage, $V^*_{ao\_f}$, $V^*_{bo\_f}$, and $V^*_{co\_f}$ denote the inverter-side output reference voltages of phase-a, phase-b, and phase-c, respectively, after passing through the notch filter.

Futhermore, as shown in Fig. 1, i_{NP} is also equal to the difference between the capacitor current i_{C2} and capacitor current i_{C1}. Combining this relationship with the capacitor current formula, it is derived that:

$$i_{NP}=C_{dc}\frac{dV_{low}}{dt}-C_{dc}\frac{dV_{up}}{dt}=-C_{dc}\frac{d\Delta V_{NP}}{dt} \tag{16}$$

where ΔV_{NP} denotes the DC-link NP voltage fluctuation value, defined as $\Delta V_{NP}=V_{up}-V_{low}$. Here, V_{up} and V_{low} represent the upper and lower capacitor voltages of the DC-link, respectively; C_{dc} is the capacitance value of DC-link capacitors C_1 and C_2.

As shown in (15) and (16), the NP voltage of the three-level inverter fluctuates when the dual-carrier SPWM is employed.

2) DMW-CBPWM

Fig. 5(b) presents the PWM sequence generated by DMW-CBPWM during the positive half-cycle of the output modulation signal. In one sampling cycle of DMW-CBPWM, the duration of the O switching state (T_O) is disassembled into equal durations of P and N switching states for regulation, thereby achieving NP voltage balance control. The balancing principle is as follows: As shown in Fig. 2, under the conditions i_x>0 and ΔV_{NP}>0, the P switching state discharges capacitor C_1, causing V_{up} to decrease. while the N switching state charges capacitor C_2, causing V_{low} to rise. Thus, the deviation between V_{up} and V_{low} is reduced by partially disassembling the O switching state duration into equal action times of the P and N switching state, mitigating fluctuation in NP voltage.

To prevent the duration of the O switching state from being entirely disassembled, which would cause the system to become a two-level system, the remaining O switching state duration after disassembly must be greater than the sum of the switching device's turn-on time t_{on} and turn-off time t_{off}. Only when the disassembly time Δt_{dis_x} of phase-x O switching state is greater than zero can the phase-x be disassembled. Then Δt_{dis_x} is defined as:

$$\Delta t_{dis\_x} = \max\{0, \min[C_{dc}\frac{\Delta V_{NP}}{i_x},\ T_O - 2(t_{on} + t_{off})]\} \tag{17}$$

The DMW-CBPWM method involves disassembling the reference voltage $V^*_{xo\_f}$ (x=a, b, c) into two modulation signals: the positive modulation signal $V^*_{xo\_fp}$ and the negative modulation signal $V^*_{xo\_fn}$. These two modulation signals are combined with upper and lower stacked carrier waves through PMW to determine the activation duration of the P, O, and N switching states. The signals $V^*_{xo\_fp}$ and $V^*_{xo\_fn}$ are defined as:

$$\begin{cases} V^*_{xo\_fp} = V^*_{xo\_f} + \Delta v \\ V^*_{xo\_fn} = -\Delta v \end{cases} \tag{18}$$

where Δv represents the variation of the DMW-CBPWM modulation voltage signal, and is defined as

$$\Delta v = \Delta t_{dis\_x} V_{dc} / (8T_s) \tag{19}$$

The NP voltage balancing capability depends on the magnitudes of $V^*_{xo\_f}$ and i_x. A larger i_x allows more charge to be extracted from or injected into the DC-link capacitor, improving NP voltage balancing effect; A smaller $|V^*_{xo\_f}|$ enables more disassembly time allocation to participate O switching state, thus enhancing the balancing performance. To characterize the strength of the NP voltage balancing capability, the NP control margin NPCM$_x$ (x=a, b, c) is therefore defined.

$$\mathrm{NPCM}_x = \mathrm{sign}(\Delta V_{NP})[1 - |V^*_{xo\_f}|/(0.5V_{dc})]\cdot i_x \tag{20}$$

where

$$\mathrm{sign}(\Delta V_{NP}) = \begin{cases} 1 & \Delta V_{NP} > 0 \\ 0 & \Delta V_{NP} = 0 \\ -1 & \Delta V_{NP} < 0 \end{cases} \tag{21}$$

Equation (20) reveals that the NP voltage fluctuation can only be suppressed by disassembling the O switching state duration of phase-x when NPCM$_x$ is positive. Moreover, the larger the positive NPCM$_x$ value is, the stronger the NP voltage balancing capability of phase-x will be.

Next, the power transistor losses of the inverter under the two modulation methods are analyzed. Taking the positive half-cycle of the output modulation signal ($V^*_{xo\_f}$>0) in Fig. 5(a) as an example, during one switching cycle under dual-carrier SPWM, the total energies dissipation E_{all_S} of the power switches in a single-phase leg circuit is equal to the sum of the conduction energies dissipation E_{cn_S} and the switching energies dissipation E_{sw_S}.

$$\begin{aligned} E_{cn\_S} = {} & \int_{t_0}^{t_0+\frac{T_O}{2}} (i^2 R_{DS} + V_D i)\mathrm{d}t + \int_{t_0+\frac{T_O}{2}}^{t_0+\frac{T_O}{2}+T_P} i^2 R_{DS}\mathrm{d}t + \\ & \int_{t_0+\frac{T_O}{2}+T_P}^{t_0+T_s} (i^2 R_{DS} + V_D i)\mathrm{d}t \end{aligned} \tag{22}$$

$$E_{sw\_S} = 2E_{on}(V_{up}) + E_{off}(V_{up}) + V_{up}Q_{rr} \tag{23}$$

where i denotes the current flowing through the power switch; R_{DS} represents the on-state resistance of the power switch; T_p indicates the duration of the P switching state; V_D signifies the forward voltage of the anti-parallel diode; Q_{rr} corresponds to the reverse recovery charge of the anti-parallel diode; $E_{on}(V)$ and $E_{off}(V)$ are the energies dissipation during the turn-on and turn-off process of the power transistor, respectively.

$$\begin{cases} E_{on}(V) = Vi(t_{ri} + t_{fu})/2 \\ E_{off}(V) = Vi(t_{fi} + t_{ru})/2 \end{cases} \tag{24}$$

where t_{ri}, t_{fi}, t_{fu}, and t_{ru} represent the current rise time, current fall time, voltage fall time, and voltage rise time of the power transistor during switching transitions, respectively.

During one switching cycle of DMW-CBPWM, the total energies dissipation E_{all_D} of the power switches in a single-phase leg circuit equals the sum of the conduction energies dissipation E_{cn_D} and the switching energies dissipation E_{sw_D}.

$$\begin{aligned} E_{cn\_D} = {} & \int_{t_0}^{t_0+\frac{\Delta t_{dis\_x}}{4}} V_D i\mathrm{d}t + \int_{t_0+\frac{\Delta t_{dis\_x}}{4}/4}^{t_0+\frac{T_O}{2}-\frac{\Delta t_{dis\_x}}{4}} (i^2 R_{DS} + V_D i)\mathrm{d}t + \\ & \int_{t_0+\frac{T_O}{2}-\frac{\Delta t_{dis\_x}}{4}}^{t_0+\frac{T_O}{2}+T_P+\frac{\Delta t_{dis\_x}}{4}} i^2 R_{DS}\mathrm{d}t + \int_{t_0+\frac{T_O}{2}+T_P+\frac{\Delta t_{dis\_x}}{4}}^{T_s-\frac{\Delta t_{dis\_x}}{4}} (i^2 R_{DS} + V_D i)\mathrm{d}t + \\ & \int_{T_s-\frac{\Delta t_{dis\_x}}{4}}^{T_s} V_D i\mathrm{d}t \end{aligned} \tag{25}$$

$$\begin{aligned} E_{sw\_D} = {} & 2\left(E_{on}(V_{low}) + E_{on}(V_{up})\right) + (V_{up} + V_{low})Q_{rr} + \\ & \left(E_{off}(V_{low}) + E_{off}(V_{up})\right) \end{aligned} \tag{26}$$

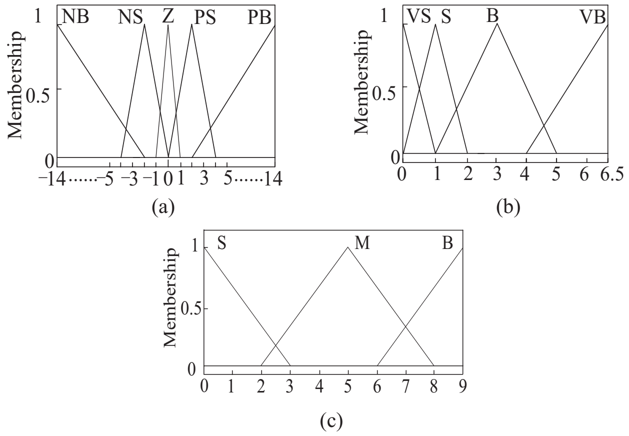


Fig. 6. Fuzzy membership functions. (a) The input ΔV_{NP}. (b) The input $NPCM_{max}$. (c) The output *h*.

As can be seen from (22)–(26), the total energy dissipation of the power switches using dual-carrier SPWM is lower than that of DMW-CBPWM within one switching period.

3) FLA-Based HPWM

To achieve coordinated control of NP voltage balance and system efficiency, a FLA-based HPWM method that integrates DMW-CBPWM with dual-carrier SPWM through FLA is proposed in this paper. The modulation principle of FLA-based HPWM involves selecting the phase with the strongest NP voltage balancing capability to participate in FLA operations, thereby determining whether this phase adopts DMW-CBPWM or dual-carrier SPWM, while the other two phases use dual-carrier SPWM. When ΔV_{NP} is small and the maximum NP control margin ($NPCM_{max}$) is positive small, this phase employs dual-carrier SPWM to reduce power transistor losses; in other case, it uses DWM-CBPWM. Furthermore, if the $NPCM_x$ values of all three phases are negative, meaning $NPCM_{max}$ is negative, the three phases employ dual-carrier SPWM.

The method for determining whether to apply dual-carrier SPWM or DMW-CBPWM in the phase with the strongest NP balancing capability using FLA is as follows: In the FLA, the NP voltage fluctuation ΔV_{NP} and the non-negative $NPCM_{max}$ are the two inputs, and the comparison coefficient h is the output. When $h > NPCM_{max}$, the dual-carrier SPWM strategy is applied to that phase; when $h < NPCM_{max}$, the DMW-CBPWM strategy is selected for that phase.

Fuzzification: ΔV_{NP} and the non-negative $NPCM_{max}$ are the inputs of FLA. Based on experimental parameters and considering extreme operating conditions involving single-phase with no load condition during operation, ΔV_{NP} is defined on the range [−14, 14] with five fuzzy labels: negative big (NB), negative small (NS), zero (Z), positive small (PS), positive big (PB). $NPCM_{max}$ is defined on the range [0, 6.5] with four fuzzy labels: very small (VS), small (S), big (B), very big (VB). Output h is defined on the range [0, 9] with three fuzzy labels: small (S), medium (M), big (B). The membership functions for the input and output variables are defined with the triangular, as illustrated in Fig. 6.

Rule evaluation: The fuzzy rule of membership functions employed for FLA-based HPWM to determine the comparison coefficient *h* is depicted in Table II.

TABLE II
FUZZY RULE

h		$NPCM_{max}$			
		VS	S	B	VB
ΔV_{NP}	NB	S	0	0	0
	NS	M	M	S	0
	Z	B	M	M	S
	PS	M	M	S	0
	PB	S	0	0	0

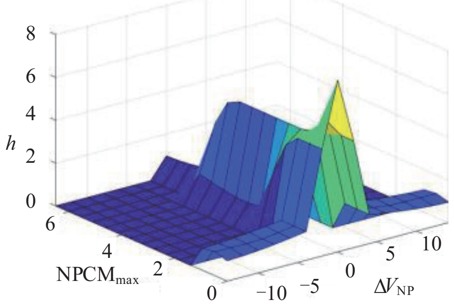


Fig. 7. Surface view of the FLA.

Defuzzification: By employing the center of gravity defuzzification method, the comparative coefficient *h* is converted back into the crisp value. The surface view of the FLA is depicted in Fig. 7.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Time-domain simulations are performed in PSIM to evaluate the proposed optimized strategy for CCS-MPC based on hybrid modulation. Table III presents the main circuit parameters used in simulation and experiment. The test conditions are detailed as follows:

Condition 1: Balanced resistive (R) loads ($R_a = R_b = R_c = R_R$).

Condition 2: Unbalanced loads, phase-a with no load ($R_a = \infty$), phase-b and phase-c with R loads ($R_b = R_c = R_R$).

Condition 3: Balanced resistive-inductive (RL) loads ($R_a = R_b = R_c = R_L$, $L_a = L_b = L_c = L_L$).

Condition 4: Unbalanced loads, phase-a with R load ($R_a = R_R$), phase-b and phase-c with RL loads ($R_b = R_c = R_L$, $L_b = L_c = L_L$).

Condition 5: Unbalanced loads, phase-a with no load($R_a = \infty$); phase-b and phase-c with RL loads ($R_b = R_c = R_L$, $L_b = L_c = L_L$).

Condition 6: Unbalanced loads, phase-a with nonlinear load (Fig. 8), phase-b and phase-c with RL loads ($R_b = R_c = R_L$, $L_b = L_c = L_L$).

Due to space constraints, only simulation waveforms under typical load transients are provided, as shown in Fig. 9. The figure illustrates the three-phase output voltages (V_{ca}, V_{cb}, V_{cc}), three-phase load currents (i_{oa}, i_{ob}, i_{oc}), and DC-link capacitor voltages (V_{up}, V_{low}) during transitions from Condition 3 to Condition 5, and from Condition 6 to Condition 5.

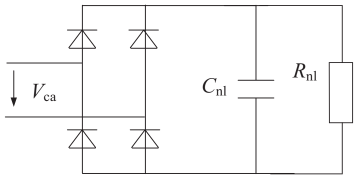


Fig. 8. Single-phase nonlinear load.

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

symbol	Parameter	Simulation values	Experimental values
V_{dc}	DC-link voltage	700 V	160 V
V_{m}/f	Output voltage/frequency	311 V/50 Hz	65 V/50 Hz
f_s	Sampling frequency	16 kHz	16 kHz
C_1/C_2	DC-link capacitors	3 mF/3 mF	3 mF/3 mF
L_f	Filter inductance	4.6 mH	4.6 mH
R_s	Parasitic resistance	0.3 Ω	0.3 Ω
C_f	Filter capacitor	2.2 μF	2.2 μF
ω_f	Notch angular frequency	1600*2π	1750*2π
Q	Notch quality factor	0.05	0.05
R_R	R load	48.4 Ω	11 Ω
R_L/L_L	RL load	42 Ω/77.5 mH	11 Ω/9.5 mH
R_{nl}/C_{nl}	Nonlinear load	39 Ω/20 μF	8 Ω/94 μF

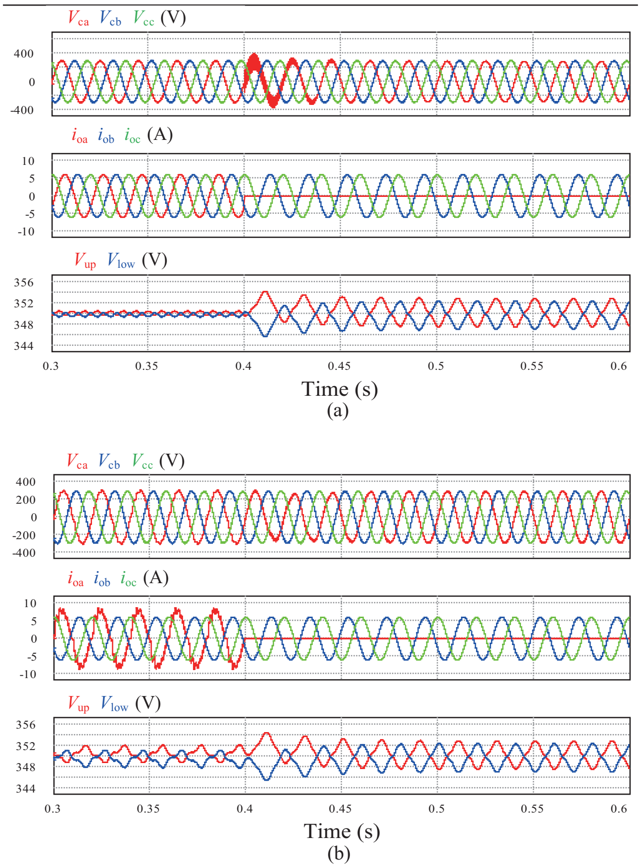


Fig. 9. Load transient simulation waveform. (a) Transition from Condition 3 to Condition 5. (b) Transition from Condition 6 to Condition 5.

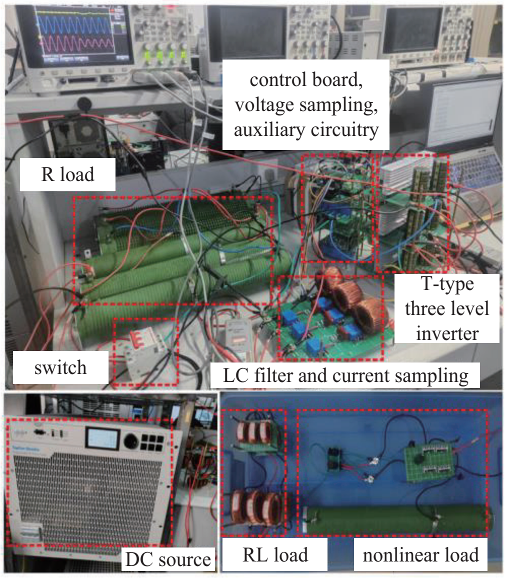


Fig. 10. Experimental platform.

From Fig. 9, it is observed that during the transition from three-phase resistive-inductive load condition to phase-a no load condition, resonance occurs in the output voltage at the initial stage of the transient. Subsequently, the resonance is effectively suppressed within 2.5 power frequency cycles. The simulation results verify that the proposed optimization strategy stabilizes the system output voltages, effectively mitigates NP voltage fluctuations, and suppresses resonance.

B. Experimental Results

To verify the effectiveness of the proposed CCS-MPC optimization strategy based on hybrid modulation, a 3P4W T-type three-level inverter experimental platform was constructed, as shown in Fig. 10. MOSFET IXFK40N90P was chosen as the power switch. The control algorithms were implemented using a DSP (TMS320F28377). The programmable DC power supply TC.P.32.200.400.S.HMI, serving as the input source, has a maximum output voltage of 200 V. Owing to constraints of experimental conditions and for safety reasons, the voltage level was reduced in the experiments. Detailed experimental parameters are listed in Table III.

1) Resonance Rejection

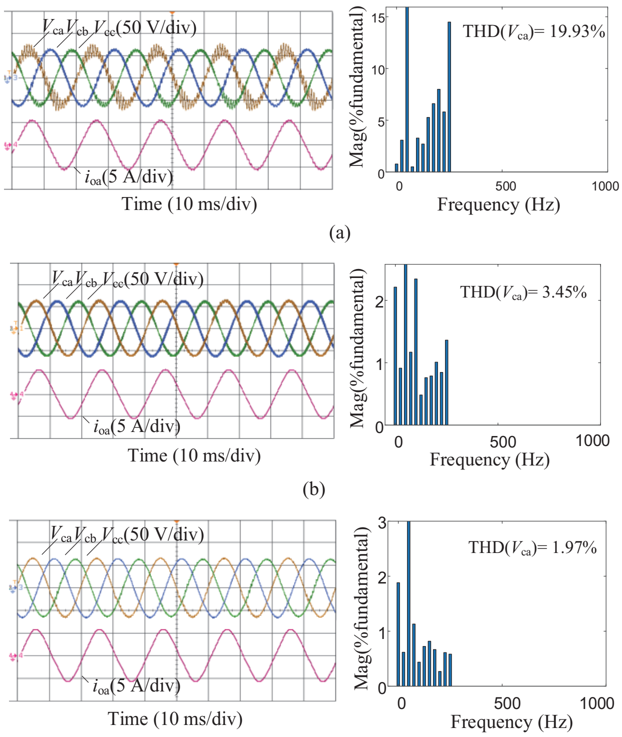
To verify the effectiveness of the proposed strategy in resonance suppression, the output waveform quality of the passive damping method and that of the notch filter-based active damping method are compared under Condition 3. The passive damping method is implemented by connecting a damping resistor R_d in series with the filter capacitor, and its value is determined by the following formula [23]:

$$R_d \geqslant 2\xi k\omega_n\left(L_f+L_L\right)/(k+1)^2 \tag{27}$$

where ζ denotes the damping coefficient, $k = L_f/L_L$, and the expression for ω_n is given by:

$$\omega_n = \sqrt{(L_f+L_L)/(L_fL_LC_f)} \tag{28}$$

According to [23], ζ=0.3 is selected. Given the system para-



(a)

(b)

(c)

Fig. 11. Experimental waveforms under Condition 3. (a) Passive damping method (R_d=30 Ω). (b) Passive damping method (R_d =39 Ω). (c) The proposed active damping method with a notch filter.

meters L_f = 4.6 mH, L_L = 9.5 mH, and C_f = 2.2 μF, the required damping resistance R_d is determined to be no less than 23 Ω to meet resonance suppression requirements while keeping R_d as small as possible.

Fig. 11 shows the experimental waveforms of the three-phase output voltages V_{ca}, V_{cb}, V_{cc} and phase-a current i_{oa}, together with the FFT spectrum of the phase-a output voltage V_{ca} under Condition 3. The results presented in this figure compare the passive damping method and the proposed active damping method employing a notch filter.

As shown in Fig. 11, when the damping resistance R_d is set to 30 Ω, the output voltage exhibits resonant phenomena. When R_d is increased to 39 Ω, the resonance phenomenon disappears. However, the passive damping approach degrades the high-frequency harmonic attenuation capability of the LC filter, resulting in an output voltage THD of 3.45%. In contrast, the proposed active damping method not only suppresses resonance effectively but also achieves a lower output voltage THD of 1.97%, outperforming the passive damping approach.

2) Performance Comparison of Modulation Methods

The system efficiency of the ZD method proposed in [19] and the FLA-based HPWM method proposed in this paper was tested under different operating conditions with experimental results presented in Table IV and Table V. As observed from the results, both modulation methods achieve higher efficiencies under load-balanced conditions (Condition 1 and Condition 3) compared to those under the other four unbalanced conditions. When the load is unbalanced, the NP voltage exhibits more significant fluctuations. To suppress these fluctuations, the disassembly times of the zero level state increase, resulting in an increase in switching loss. Under all tested conditions, the system efficiency of the FLA-based HPWM is higher than that of the ZD method. Futhermore, even under unbalanced load conditions, both the ZD and FLA-based HPWM methods can still restrict the NP voltage fluctuation to within 8 V and achieve the output voltage THD below 5%.

TABLE IV
EXPERIMENTAL SYSTEM EFFICIENCY

	η(ZD)	η(FLA-based HPWM)
Condition 1	91.926%	92.611%
Condition 2	91.166%	91.691%
Condition 3	91.270%	92.203%
Condition 4	91.228%	92.091%
Condition 5	91.184%	91.603%
Condition 6	90.688%	90.786%

TABLE V
EXPERIMENTAL OUTPUT VOLTAGE THD AND NP VOLTAGE FLUCTUATION

	THD of V_{ca}		NP voltage fluctuation	
	ZD	FLA-based HPWM	ZD	FLA-based HPWM
Condition 1	2.06%	1.89%	2.1V	2.5 V
Condition 2	2.05%	2.16%	7.3 V	7.5 V
Condition 3	1.99%	1.97%	2.1 V	2.5 V
Condition 4	1.99%	2.25%	2.7 V	3.0 V
Condition 5	1.98%	2.01%	6.4 V	7.2 V
Condition 6	4.43%	4.58%	6.5 V	7.0 V

The system efficiency below 93% shown in Table IV is attributed to two primary factors. First, the operating voltage was reduced during experiments. Since the output current in the experiment did not change much compared to the rated value, the reduced voltage level had little effect on conduction losses, but led to lower switching losses. However, the total output power declined more significantly, resulting in lower overall efficiency under reduced voltage conditions compared to rated operation. Furthermore, the power switches and drive circuits were not optimized for this application, and the existing components available in the laboratory were utilized, which adversely affected the overall system efficiency. However, testing the two modulation methods under identical conditions does not affect the comparison of their efficiencies.

Fig. 12, Fig. 14, Fig. 16, and Fig. 18 present experimental waveforms of the three-phase output voltages (V_{ca}, V_{cb}, V_{cc}), phase-a load current i_{oa} and DC-link capacitor voltages (V_{up}, V_{low}) under Condition 1, Condition 3, Condition 5, and Condition 6 respectively, for both the ZD method and the proposed FLA-based HPWM method. Additionally, Fig. 13, Fig. 15, Fig. 17, and Fig. 19 further present the FFT results of the phase-a output voltage V_{ca}. In conclusion, the proposed FLA-based HPWM method not only enhances system

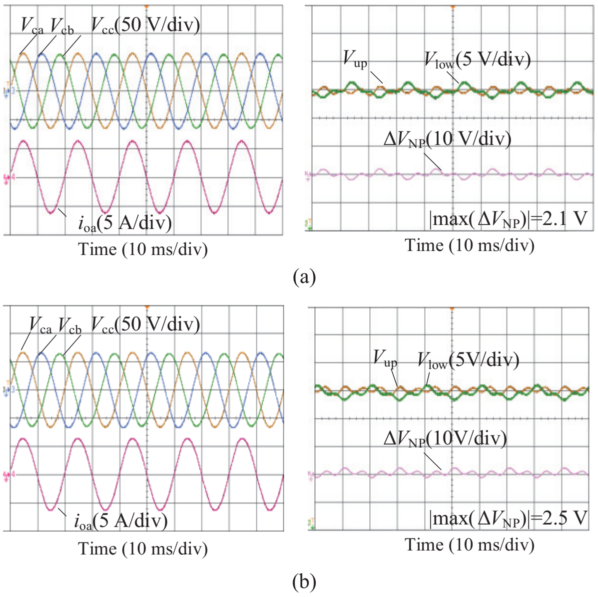


Fig. 12. Experimental waveforms under Condition 1. (a) ZD. (b) FLA-based HPWM.

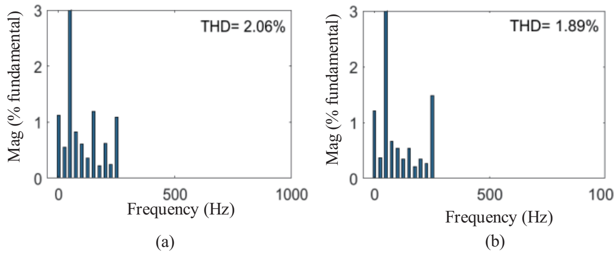


Fig. 13. FFT results of V_{ca} under Condition 1. (a) ZD. (b) FLA-based HPWM.

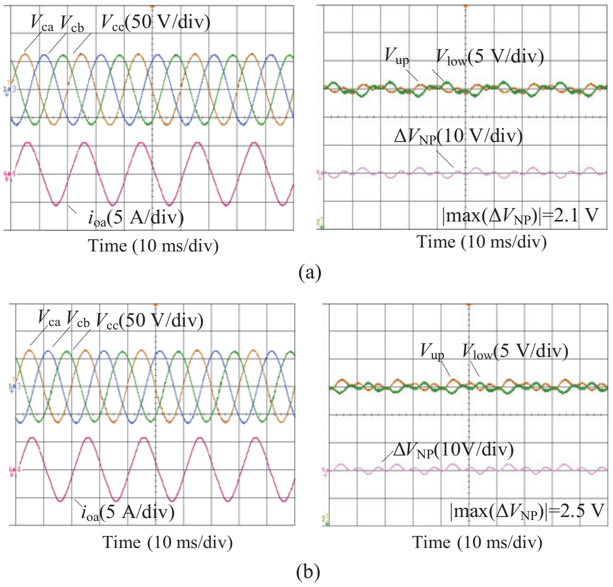


Fig. 14. Experimental waveforms under Condition 3. (a) ZD. (b) FLA-based HPWM.

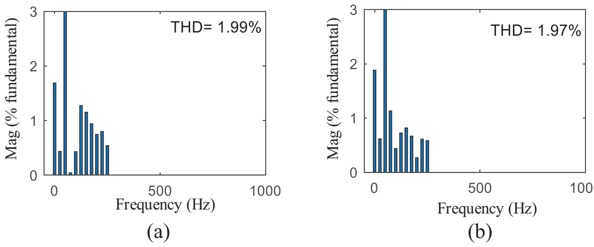


Fig. 15. FFT results of V_{ca} under Condition 3. (a) ZD. (b) FLA-based HPWM.

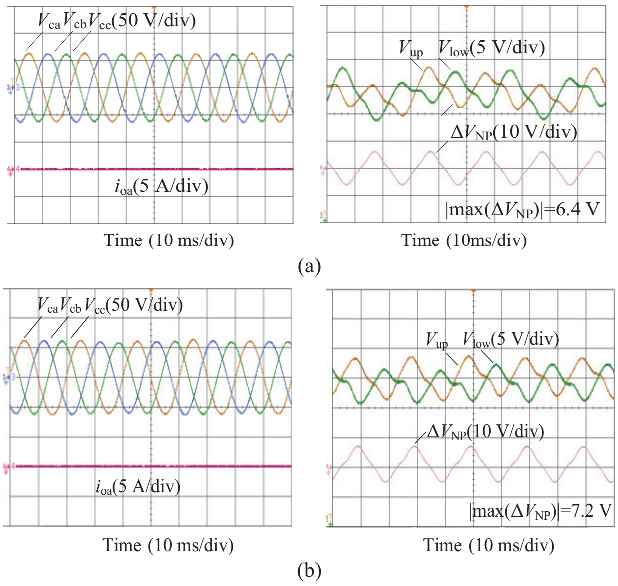


Fig. 16. Experimental waveforms under Condition 5. (a) ZD. (b) FLA-based HPWM.

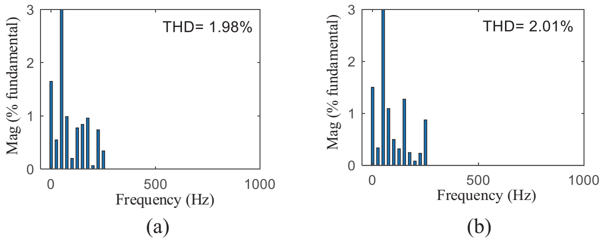
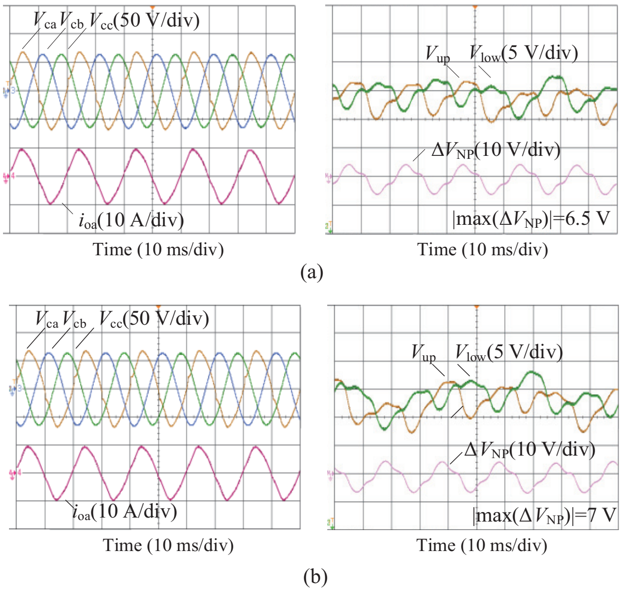


Fig. 17. FFT results of V_{ca} under Condition 5. (a) ZD. (b) FLA-based HPWM.

efficiency but also exhibits similar performance to the ZD method with regard to NP voltage balancing capability and the output voltage quality.

3) Dynamic Performance

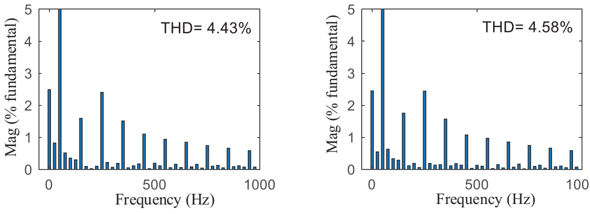
Fig. 20 presents experimental waveforms of the DC-link capacitor voltages (V_{up}, V_{low}), phase-a output voltage V_{ca} and phase-a load current i_{oa} under five distinct load switching conditions, obtained using the proposed strategy. Specifically, Fig. 20(a) and Fig. 20(b) show the experimental waveforms when the three-phase balanced resistive loads is switched from R_R to $2R_R$ and from $2R_R$ to R_R. Fig. 20(c) and Fig. 20(d) illustrate the experimental waveforms when the phase-a load is switched from a resistive-inductive load (Condition 3) and a non-linear load (Condition 6) to a no load condition (Condition 5), respectively. Conversely, Fig. 20(e) and Fig. 20(f) present the experimental waveforms when the phase-a



(a)

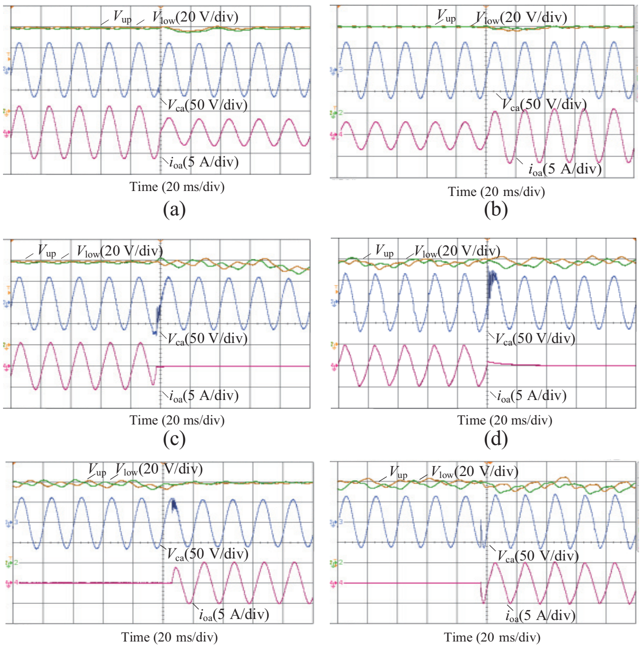
(b)

Fig. 18. Experimental waveforms under Condition 6. (a) ZD. (b) FLA-based HPWM.



(a) (b)

Fig. 19. FFT results of V_{ca} under Condition 6. (a) ZD. (b) FLA-based HPWM.



(a) (b) (c) (d) (e) (f)

Fig. 20. Experimental waveforms under load switching conditions. (a) R_R to $2R_R$. (b) $2R_R$ to R_R. (c) Condition 3 to Condition 5. (d) Condition 6 to Condition 5. (e) Condition 5 to Condition3. (f) Condition 5 to Condition 6.

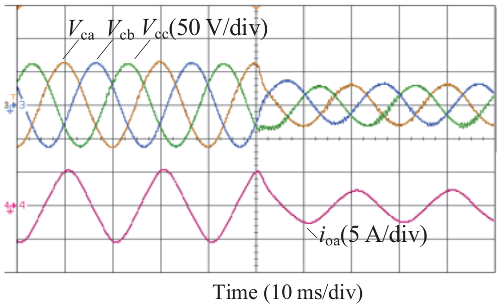


Fig. 21. Experimental waveforms under reference voltage transient condition.

load is switched from the no load condition (Condition 5) to a resistive-inductive load (Condition 3) and a non-linear load (Condition 6), respectively. As observed in Fig. 20(a) and Fig. 20(b), the system output voltage reaches its sinusoidal steady state within the first quarter of an output voltage cycle following the load step change. This verifies that the output voltage can be effectively controlled at the desired sinusoidal steady-state during load transients. As seen in Fig. 20(c) to Fig. 20(e), when the system load is switched to no-load or a resistive-inductive load, resonance initially appears in the output voltage. However, this resonance is rapidly damped within half an output voltage cycle. Furthermore, the fluctuation amplitude of the NP voltage is constrained within 9 V across all cases.

Fig. 21 shows experimental waveforms under Condition 3 during a step change in the amplitude of the three-phase reference voltage from 65 V to 32.5 V. From the figure, the output voltage reaches sinusoidal steady state within half an output voltage cycle after the reference voltage step change.

In summary, the proposed strategy endows strong robustness under both load switching and reference voltage transient condition due to its fast dynamic response.

V. Conclusion

This paper proposes an optimization strategy for CCS-MPC with hybrid modulation for 3P4W three-level inverters under unbalanced loads. By integrating a notch filter-based active damping method into the CCS-MPC loop, filter-load resonance is effectively suppressed, yielding high-quality output voltages. By evaluating the fluctuation amplitude of NP voltage and the NP voltage balancing capability of each phase combined with FLA, the strategy dynamically selects between DMW-CBPWM and dual-carrier SPWM. This achieves the balanced control of NP voltage while optimizing system efficiency. Experimental results demonstrate that the proposed optimization strategy can ensure system steady-state performance and rapid dynamic response while effectively achieving the balanced control of output voltage quality and system efficiency.

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