Reliability Improvement of a Three-Port Converter for Standalone PV-Battery Applications

Mohammad Raja AL-SOEIDAT, Habes Ali KHAWALDEH, Khaled Al KHALYFEH, Dylan Dah-Chuan LU, and Muheeb Ahmad ALKHALAYFEH

***Abstract*—Three-port converters are increasingly preferred for standalone PV-battery systems due to their versatility and multi-functional operation, which allow the system to effectively mitigate the effects of intermittency in renewable power generation. However, their reliability is often lower than that of two-port converters, as they involve more components, experience higher thermal stress, require complex control algorithms, and operate in multiple modes. This paper investigates and evaluates the reliability of a three-port power converter under different operating modes using the MIL-HDBK-217F standard. Component-level failure rates were analyzed, and design improvements were proposed to reduce stress and enhance performance. Based on the reliability analysis, a novel reliability-oriented control strategy is proposed to enhance the resilience of the standalone system. By implementing a state-of-charge (SoC) based management algorithm, the converter avoids high-stress operating modes, such as the SISO PV-load mode, thereby extending the expected operational lifetime. The effectiveness of these improvements was verified through LTspice simulations and Scilab calculations, providing a robust validation method given that physical lifecycle testing requires extended operational durations. Results indicate a significant reduction in failure rates, improved system efficiency, and extended operational lifetime.**

***Index Terms*—Capacitor, failure rates, MIL-HDBK-217F, mean-time-to-failure, nonisolated converter, photovoltaic, reliability, renewable energy, three-port converter.**

I. Introduction

TRADITIONAL DC-DC converters, including boost, buck, and buck-boost configurations are well established and widely employed; however, their long-term performance is often constrained by component stress, which directly impacts system reliability. Recent studies have proposed restructuring techniques that alter the placement of the output capacitor, reducing voltage stress without additional components. This approach lowers the risk of capacitor failure and extends converter lifetime. Compared to conventional topologies, restructured designs preserve output performance while achieving lower energy losses and enhanced robustness, making them well suited for high-gain applications where capacitor reliability is critical [1].

Renewable energy sources are inherently intermittent and produce fluctuating power outputs, while power demand is also variable. As a result, energy storage systems are essential for balancing generation and consumption, thereby enhancing both sustainability and efficiency [2]–[4]. To efficiently manage power flow among multiple sources, storage elements, and loads, multi-port converters (MPCs) are employed [5], [6]. These topologies integrate a power management controller that dynamically regulates energy distribution to meet the specific demands of each connected port. These converters operate in various modes depending on photovoltaic (PV) availability and power conditioning requirements, enabling key functions such as maximum power point tracking (MPPT), battery energy management, output voltage regulation, and high voltage gain—all while maintaining a low component count through shared use of circuit elements [7], [8].

While MPCs offer high integration and energy management flexibility, their reliability is challenged by increased current and voltage stress due to component sharing, complex control strategies, climate conditions and elevated thermal loads [9]. To ensure long-term operational stability in renewable energy systems, design optimisation, accurate thermal modelling, proper maintenance, and comprehensive failure mode analysis are essential [10].

Electronic switches, gate drivers, diodes, capacitors, controllers, inductors and thermal management systems are used to build the electronic circuit. Electronic switches, diodes and capacitors are among the most vulnerable components, often susceptible to thermal and electrical stress-induced wear-out failures [11]. Analysing component stress and failure rates in electronic circuits, including integrated MPCs, is essential for ensuring system availability, reliability, and effective lifecycle planning. By developing a proper lifecycle plan, informed and optimal decisions can be made regarding maintenance,

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M. R. Al-Soeidat is with the Department of Electrical Engineering, Al-Hussein Bin Talal University, Ma'an 71111, Jordan (e-mail: mo.soeidat@gmail.com, mo. soeidat@ahu.edu.jo).

H. A. Khawaldeh is with the Renewable Energy Engineering Department, Faculty of Engineering, Al Al-Bayt University, Mafraq 25113, Jordan (e-mail: habes.a.khawaldeh@aabu.edu.jo).

K. A. Khalyfeh is with the Department of Chemistry, Faculty ofNatural Sciences, Al-Hussein Bin Talal University, Ma'an 71111, Jordan (e-mail: k.khalyfeh@ahu.edu.jo).

D. D.-C. Lu is with the School of Electrical and Data Engineering, University of Technology Sydney, Ultimo, NSW 2007, Australia (e-mail: dylandclu@ieee.org).

M. A. Alkhalayfeh is with the School of Physics, Universiti Sains Malaysia,11800 USM, Penang, Malaysia (e-mail: muheebphy@usm.my).

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repair, and replacement schedules. This approach also supports cost-effective design and enables the manufacturing of converters that are both optimised and reliable [12].

Recent research studies have focused on evaluating the reliability of power converters [1], [11], [13]–[16]. One of the most commonly used methods is outlined in Military Handbook 217F (MIL-HDBK-217F) due to its well-established and extensive database of components [17]. However, this handbook may be outdated for assessing the reliability of newer technologies and devices. Another general guideline for mission profile-based failure rate prediction has been introduced by the International Electrotechnical Commission (IEC) through standards such as IEC TR 62380 and IEC 61709 [18]–[20]. These standards provide methodologies for estimating failure rates by considering real-world operating conditions, such as temperature variations, on/off cycling, and environmental stress factors, rather than relying solely on fixed reference conditions.

The reliability of power converters can be enhanced through several strategies [21]. The most straightforward method is to overrate the components, ensuring they operate well below their maximum stress limits to reduce the likelihood of failure. Another effective approach is the implementation of redundancy, which allows the system to continue functioning even in the event of a component failure. A more advanced technique involves analysing the operational environment and identifying potential failure modes, then using this information to redesign the converter for improved robustness and performance [16]. Integrating these techniques plays a critical role in extending both the reliability and lifetime of power electronic systems.

Therefore, this paper presents a reliability analysis of a non-isolated three-port converter (TPC) designed for standalone PV-battery-powered applications. The failure rate of each component within the converter circuit is evaluated using the MIL-HDBK-217F military standard, as the examined converter does not incorporate any advanced or newer technologies. Consequently, the failure rates of all the components can be accurately estimated using this standard, and significantly reduced through specific reliability enhancement techniques. These strategies, which represent the core novelty of this work as detailed in Section IV, include the selection of robust components with optimised voltage ratings and quality factors, the implementation of active thermal management systems to lower environmental stress, the reduction of power losses through efficient circuit design, and the application of novel control algorithms. Recent research has demonstrated the effectiveness of reliability-aware management strategies in other hybrid domains, such as fuel cell-battery systems for electric vehicles [22]. However, while existing literature focuses heavily on hardware topology restructuring, there is a notable gap in research regarding comprehensive, multi-faceted reliability enhancement frameworks for multi-port PV-battery converters. This study fills that gap by presenting a reliability analysis based on the MIL-HDBK-217F standard and introducing a holistic approach that integrates these four elements to minimise component stress. It is important to note that although most failure rate formulas presented in this standard have an identical structure, the specific parameter values (e.g., π_T, π_E, π_Q) depend entirely on the specific component selected. These differences, while seemingly small, can significantly affect the calculated failure rate, making it essential to use the correct value for each part.

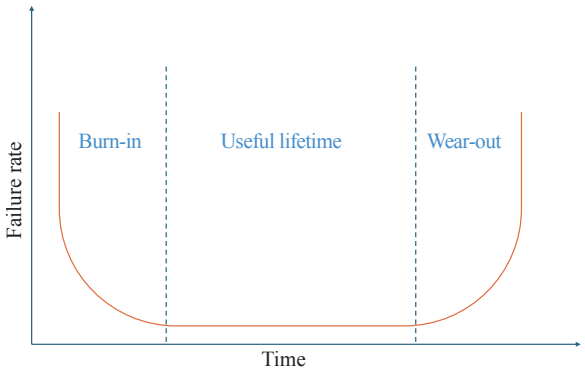

Fig. 1. The bathtub curve represents failure rates across three distinct phases.

The paper is organised as follows: Section II discusses reliability assessment and failure mechanisms in power electronic systems. Section III presents the reliability assessment results and related discussions. In Section IV, the failure rates and improvements in mean time to failure (MTTF) are explored. Finally, Section V provides the conclusions.

II. Reliability Assessment and Failures in Power Electronic Systems

Due to its status as an international standard for reliability prediction, MIL-HDBK-217F, along with MIL-HDBK-217F Notice 2 [23], is employed in this study to assess the reliability and estimate the individual failure rates of power components in the converter proposed in [24].

The operational life cycle of electronic components is typically segmented into three primary phases: the burn-in (infant mortality) period, the useful life phase, and the wear-out phase [25]. This behaviour is commonly illustrated by the bathtub curve, as depicted in Fig. 1. The initial burn-in phase is characterised by a high and decreasing failure rate, often attributed to latent manufacturing defects, substandard material properties, or assembly-related inconsistencies that escape standard quality assurance processes. To mitigate these early-life failures and improve long-term reliability, manufacturers employ stress screening techniques such as highly accelerated life testing (HALT), burn-in procedures, and environmental stress testing. These processes are designed to precipitate latent defects, ensuring only robust components enter the subsequent useful life phase, where the failure rate stabilises at a relatively low constant level.

During the useful life period, the failure rate stabilises and remains approximately constant, representing a phase dominated by random failures. These failures typically occur due to unpredictable external factors, such as sudden electrical stress, environmental disturbances, or operational anomalies, rather

than inherent design or manufacturing defects. This phase is critical for assessing system reliability, as it encompasses the majority of the component's operational lifetime. Eventually, the system enters the wear-out phase, during which components begin to degrade due to ageing mechanisms such as material fatigue, electromigration, or thermal cycling. Consequently, accurately identifying and quantifying the failure rate during the useful life period is essential for conducting meaningful reliability analysis and predicting system performance over time [26].

By assuming a constant failure rate during the useful life period, MTTF can be estimated as the inverse of the total failure rate, which is calculated by summing the individual failure rates of all components within the system i.e., λ_{Di}, λ_{Mi}, and λ_{Ci}.

$$\mathrm{MTTF} = \lambda^{-1} = \left(\sum_{i=1}^{n_D} \lambda_{Di} + \sum_{i=1}^{n_M} \lambda_{Mi} + \sum_{i=1}^{n_C} \lambda_{Ci} \right)^{-1} \tag{1}$$

where n_D, n_M and n_C are the number of diodes, MOSFETs and capacitors, respectively, in the power stage of the converter under study. The individual failure rates of all components in the system are calculated as follows:

A. Diode

One Schottky power diode, D_1(MBR2035CT), is used to build the circuit. By referring to MIL-HDBK-217F [17] Sec. 6.1, the failure rate is estimated as

$$\lambda_D = \lambda_b \, \pi_T \, \pi_S \, \pi_C \, \pi_Q \, \pi_E, \text{ failures}/10^6 \text{ hours} \tag{2}$$

where λ_b is the base failure rate, listed for all electronic device categories in the handbook. For the power rectifier (the Schottky power diode), the value of $\lambda_b = 0.003$.

The temperature factor π_T is obtained by the following expression:

$$\pi_T = \exp\left[-3091 \left(\frac{1}{T_J + 273} - \frac{1}{T_{Ref}} \right) \right] \tag{3}$$

where T_J is the junction temperature (°C) and T_{Ref} is the reference ambient temperature in Kelvin (298 K, corresponding to 25 °C). As the junction temperature is not directly measurable, it can be estimated using a linear RC ladder network, following the approach described in [14].

$$T_J = T_a + P_D \times \theta_{ja} \tag{4}$$

$$\theta_{ja} = \theta_{jc} + \theta_{cs} + \theta_{sa} \tag{5}$$

where θ_{ja}, θ_{jc}, θ_{cs} and θ_{sa} are junction-ambient thermal resistance, junction-case thermal resistance, case-heatsink thermal resistance, and heatsink-ambient thermal resistance, respectively. T_a is the case temperature (°C). According to MIL-HDBK-217F Sec. 6.14, the case temperature at the ground benign (GB) includes laboratory instruments and test equipment equals 30 °C. P_D is the device worst-case power dissipation (W), and its value is extracted from the circuit simulation for each operation mode.

The electrical stress factor π_S is calculated by

$$\pi_S = \left(\frac{\text{Voltage applied}}{\text{Voltage rated}} \right)^{2.43} \tag{6}$$

The rated voltage of the selected diode equals 35 V, where the voltage applied to each diode is obtained from the circuit simulation.

π_C is the contact construction factor of metallurgically bonded, and $\pi_C = 1$.

Based on the parts specifications, the quality level can be identified. Each part has a different quality factor π_Q, which has a direct effect on the failure rate. These values range from a high level, such as the JANTX category to a low level, such as the plastic category. In this study, π_Q is selected to be 5.5 to meet industrial application standards.

The environment factor π_E reflects the impact of the operational environment on the performance and durability of electronic components. This factor reflects how varying environmental conditions, such as temperature fluctuations, humidity, vibration and mechanical stress, affect the performance and longevity of components. The value of π_E is determined by the specific environment in which the system operates, with standard classifications provided in MIL-HDBK-217F, including ground benign (GB), ground fixed (GF), airborne (A), and naval (N) environments, among others. For this analysis, the system is assumed to operate under GB conditions, which represent a controlled, low-stress environment such as a laboratory or clean indoor facility. Accordingly, the environmental factor is set to $\pi_E = 1$, indicating minimal environmental impact on component reliability.

B. MOSFET

In [24], three MOSFETs, IRF540NPBF, are used two implement two main switches. According to MIL-HDBK-217F and its Notice 2, the failure rate of low frequency Si FET (MOSFET) is estimated as

$$\lambda_M = \lambda_b \, \pi_T \, \pi_A \, \pi_Q \, \pi_E, \text{ failure}/10^6 \text{ hours} \tag{7}$$

where the constant λ_b is the base failure rate for the MOSFET, and its value equals 0.012. The temperature stress factor π_T is obtained by the expression

$$\pi_T = \exp\left[-1925 \left(\frac{1}{T_J + 273} - \frac{1}{T_{Ref}} \right) \right] \tag{8}$$

where the junction temperature T_J is calculated using (4).

The power application factor π_A based on the rated power for the analyzed converter equals 8. The quality factor π_Q and environment factor π_E values are the same as those for the diode.

C. Capacitor

The failure rate of capacitors, according to MIL-HDBK-217F, Sec.10 [17], is modelled as

$$\lambda_C = \lambda_b \, \pi_T \, \pi_C \, \pi_V \, \pi_{SR} \, \pi_Q \, \pi_E, \text{ failure}/10^6 \text{ hours} \tag{9}$$

where λ_b is the base failure rate for the capacitor, and its value

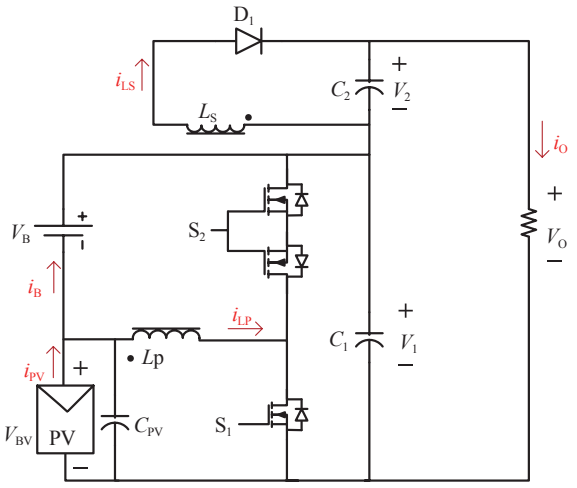

Fig. 2. The TPC topology proposed in [24] and analyzed for reliability evaluation in this study.

depends on the type of capacitor used. The temperature factor π_T is obtained by the expression

$$\pi_T = \exp\left[\frac{-0.15}{8.617\times10^{-5}}\left(\frac{1}{T_J+273}-\frac{1}{T_{Ref}}\right)\right] \quad (10)$$

The capacitance factor π_C is calculated as

$$\pi_C = C^{0.23} \quad (11)$$

The voltage stress factor π_V is expressed by

$$\pi_V = \left(\frac{S}{0.6}\right)^{17} + 1 \quad (12)$$

where S is the operation voltage of the capacitor over its rated voltage. In this study, the input and output capacitor rated voltages are 25 V and 63 V, respectively.

Other remaining failure factors of the capacitor are λ_b = 0.0004, π_{SR} = 1, π_Q = 10, π_E = 1, according to their appropriate categories.

The inductor's failure rate is negligible compared to that of semiconductors, and thus is typically disregarded in reliability analysis [14], [26].

Although most failure rate formulas have an almost identical structure, the parameter values (e.g., π_T, π_E) depend on the specific component selected. These differences, while seemingly small, can significantly affect the calculated failure rate, making it essential to use the correct value for each part.

III. Reliability Assessments and Discussions

The TPC shown in Fig. 2, has six different operation modes, namely: single-input single-output (SISO) PV-battery mode, SISO PV-load mode, SISO battery-load mode, dual-input single-output (DISO) mode, single-input dual-output (SIDO), dual-input dual-output (DIDO) [24]. The physical implementation of the converter utilises a coupled inductor based on the RM14/1-3C95 core with a primary-to-secondary turns ratio of N_P/N_S = 1/2, designed to achieve high voltage gain. The switching frequency is regulated at 50 kHz to balance efficiency and thermal stress. To verify the circuit operation and measure the voltage stress and the power losses, a circuit simulator (LTSpice©) is used in this study across various operation modes. To ensure accurate results, realistic models provided by semiconductor manufacturers are used and verified against the component datasheets used in the circuit design. The complete circuit specification and component details are summarized in Table I, where the stress factor obtained for the simulation is listed in Table II.

TABLE I
Circuit Specification and Components Details

Component	Model / Value
Switching frequency	50 kHz
MOSFET	IRF540NPBF
D_1	MBR2045CT
Coupled inductor core	RM14/I-3C95
N_P/N_S	1 / 2
C_1 & C_2	470 µF
C_{PV}	100 µF
V_{PV}	18.5 V
V_B	12 V
V_O	50 V
Heat sink	SW50-5G

TABLE II
Components Power Losses

Operation modes	Power losses (mW)						
	D_1	S_1	S_{2L}	S_{2U}	C_{PV}	C_1	C_2
SISO PV-battery	28.3	2400	1597	2502	2007	130	479
SISO PV-load	435	396.3	3588	3069	7802	124	065
SISO battery-load	467	965.8	1494	563.6	044	242	080
DISO	479	1254.2	901	1832	151	588	086
SIDO	95	2244.2	1246	2132	214	1159	3
DIDO	425	1527	365	3110	240	253	74

The reliability assessment of the individual components was performed in accordance with the MIL-HDBK-217F standard, utilizing Scilab for the failure rate calculations. The analysis incorporates the maximum electrical stress parameters, namely voltage, current and power dissipation, experienced by each component, as derived from simulation results under nominal operating conditions. The calculated failure rates for all critical components are summarized in Table III, forming the foundation for evaluating overall system reliability and identifying the components with the most significant impact on the MTTF.

The following analysis presents a comprehensive evaluation of the converter's performance and reliability across its distinct operating modes. This assessment is conducted in accordance with the MIL-HDBK-217F standard and its Notice 2 update,

TABLE III
INDIVIDUAL FAILURE RATES OF THE COMPONENTS

Operation modes	λ_{D1}	λ_{MS1}	λ_{MS2L}	λ_{MSU}	λ_{CPV}	λ_{C1}	λ_{C2}
SISO PV-battery	0.007	1.794	1.294	1.866	0.164	0.037	0.024
SISO PV-load	0.003	1.184	0.715	0.695	2.838	0.020	0.019
SISO battery-load	0.003	0.971	1.237	1.275	0.418	0.021	0.019
DISO	0.003	1.111	0.941	1.430	0.189	0.026	0.019
SIDO	0.005	1.689	1.107	1.616	0.125	0.034	0.018
DIDO	0.004	1.255	0.717	0.697	0.063	0.021	0.019

which provides a structured methodology for estimating failure rates under defined environmental and electrical stress conditions. Each operating mode imposes unique electrical and thermal stresses on the converter's components, which directly influence their reliability characteristics. This approach allows for the identification of the most critical stress scenarios and the components most susceptible to failure, thereby supporting design decisions aimed at enhancing system robustness and extending operational lifetime.

As shown in Fig. 3, in power electronic systems, the failure of a single component can affect the operation of other components or compromise the functionality of the entire system. For example, a high failure rate of the input capacitor leads to a reduced MTTF of the circuit operating in the SISO PV-load mode. This increased failure rate is primarily due to the absence of the battery, which typically acts as a low-impedance voltage clamp. In SISO PV-load mode, the input capacitor loses this buffering effect and is forced to absorb the full instantaneous power mismatch between the intermittent PV source and the load. This results in significantly higher voltage ripple and root mean square (RMS) current stress compared to modes where the battery is active.

Compared to passive components like capacitors or inductors, MOSFETs have significantly higher failure rates due to their active nature and complex internal structure, which functions as the main control element in power electronics. Additionally, MOSFETs may experience voltage and current spikes that can lead to avalanche breakdown or oxide degradation, both of which reduce the MTTF. Furthermore, the high voltage stress caused by rapid switching induces electric stress and power losses, resulting in thermal fatigue. This thermal cycling can lead to solder joint fatigue, bond wire lift-off, and cracking in the packaging, all of which are leading causes of failure.

In the SISO PV-battery mode, the MOSFET S_1 exhibits a higher failure rate compared to other MOSFETs for several reasons. In this mode, only two ports are active, and the converter operates as a buck-boost converter with no power transferred to the output. Consequently, the coupled inductor is inactive, and all power is routed through the buck-boost circuit, which includes S_1, S_{2L}, S_{2U}, L_1, C_{pv}, and C_1. This results in high voltage stress and power losses across these components, particularly S_1, which bears the brunt of the switching stress. Meanwhile, diode D_1 and capacitor C_2 remain in standby mode, subjected to high reverse voltage without active conduction, which also

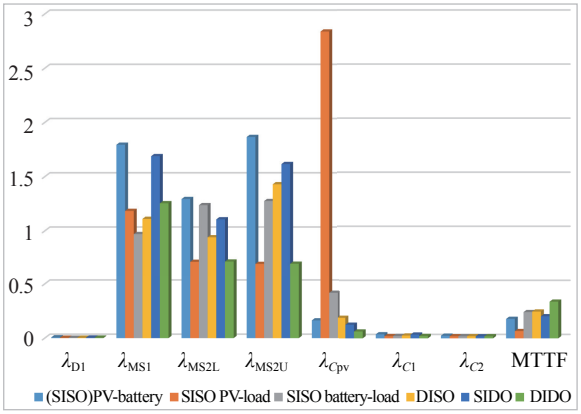

Fig. 3. Calculated failure rates and MTTF. The failure rate is expressed in units of 10^{-6} failures per hour, where the MTTF is expressed in units 10^{6} hours.

contributes to their relatively high failure rates. It is clear that, according to the MIL-HDBK-217F standard, the failure rate calculation includes all components, regardless of whether they are active or idle during operation.

IV. FAILURE RATE AND MTTF IMPROVEMENT

Based on military standards and the analysis of critical stress modes, this paper proposes a comprehensive framework to enhance system reliability. The high stress observed is addressed through a multi-layered approach, starting with over-rating the input capacitors (e.g., 50 V rating) to ensure capacitors can withstand the residual stress during any unavoidable battery-less operation. Complementing this hardware robustness, a novel control strategy is implemented to retain the battery connection (DIDO mode) by limiting state-of-charge (SoC) to 90%, thereby preserving the voltage clamping effect, while thermal management and power loss reduction are employed as secondary mitigation layers.

A. Component Selection

Component selection plays a crucial role in improving reliability. Choosing higher-rated components, such as MOSFETs, capacitors, and diodes with voltage and current ratings well above the expected operating conditions, can significantly reduce stress and failure rates.

Table IV proves a significant improvement in both failure rate and MTTF, in SISO PV-load mode, by selecting capacitors with different voltage ratings while keeping the capacitance constant at 100 µF across all cases. In the first scenario, the input capacitor is rated at 25 V, with an actual operating voltage regulated at 18 V. This setup results in a relatively high failure rate compared to other circuit components, mainly due to the high voltage stress exerted on the capacitor. Subsequent cases involve capacitors of the same type and package, Aluminum electrolytic capacitors with radial leads, but with higher voltage ratings: the UPJ1V101MPD rated at 35 V and the UPJ1H101MPD and UPJ1H101MPD6 rated at 50 V. These capacitors exhibit marked improvements in both failure rate

TABLE IV
IMPACT OF CAPACITOR SELECTION ON FAILURE RATE AND MTTF IN A SISO PV-LOAD MODE WITH INITIALLY HIGH FAILURE RATE

Part number	Voltage rating/V	Size $D \times L$/mm	Impedance/Ω	Voltage stress	λ_{CPV}(μ failures/h)	MTTF/h
UPJ1E101MED	25	6.3 × 15	0.39	0.753	2.8380783	182665
UPJ1V101MED	35	8 × 11.5	0.26	0.538	0.0665428	368763
UPJ1H101MED	50	8 × 20	0.18	0.377	0.0386167	372491
UPJ1E101MED6	50	10 × 16	0.21	0.377	0.0262272	374218

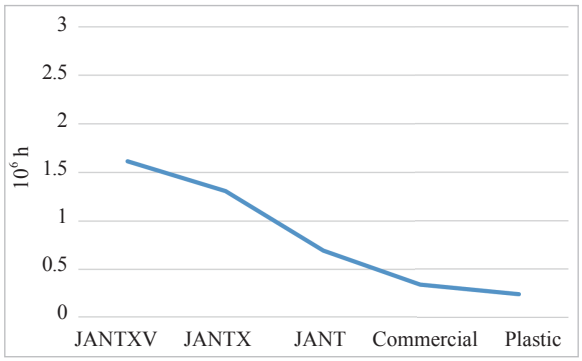

Fig. 4. MTTF calculation for DIDO mode under different quality factors π_Q. π_Q equals 0.7 for JANTXV, 1 for JANTX, 2.4 for JANT, 5.5 for commercial and 8 for plastic.

and MTTF. To ensure that these reliability gains were primarily due to increased voltage ratings rather than differences in physical size (which could affect thermal or electrical performance), failure rate calculations were performed twice: first assuming similar dimensions, and then using the actual component sizes. In both instances, the results confirmed that voltage rating is the dominant factor driving reliability improvements. Overall, simulation and analytical results indicate that operating a capacitor at 50% or less of its rated voltage generally ensures reliable long-term performance.

Additionally, selecting components with a high reliability and quality factor π_Q, such as those qualified under JANTX and JANTXV standards, further enhances system reliability by improving the overall MTTF. As shown in Fig. 4, the MTTF in DIDO mode improves considerably when the quality factor π_Q increases, for instance, from (0.33 to 1.38) × 10^6 h due to replacing a commercial MOSFET IRF540NPBF with a high-reliability IRF150 JANTX MOSFET device.

In addition to the previous discussion on the MOSFET and capacitor design selection, a cost comparison among these components is presented in Table V. Mouser electronics is used as the primary source for the pricing of most components, while other sources such as AliExpress and UTSOURCE are used to find some rare components. It is clear that the capacitor price depends on the voltage rating, ranging from $0.32 to $0.54 for the selected capacitors. However, the cost is also influenced by the physical size or packaging. For example, both capacitors UPJ1H101MPD and UPJ1H101MPD6 have the same voltage rating but differ in package size, which results in a price difference. For the MOSFET selection, both IRF540NPBF and IRF150 were considered. The IRF540NPBF is commercially

TABLE V
COST COMPARISON OF SELECTED CAPACITORS AND MOSFETS

Parts	Part number	Cost ($)	Cost source
Capacitor	UPJ1E101MED	0.32	Mouser
	UPJ1V101MED	0.36	Mouser
	UPJ1H101MED	0.54	Mouser
	UPJ1H101MED6	0.60	Mouser
MOSFET	IRF540NPBF	1.06	Mouser
	IRF150	2.30	AliExpress
	IRF150	5.46	UTSOURCE
	TK34A10N1	2.61	Mouser

available and priced at approximately $1.06, while the IRF150 was sourced from two different suppliers, with its price varying significantly across vendors. In general, high-reliability components such as IRF150 JANTX are produced under military specification standards and often reserved for defence contractors or government-approved projects. These components are typically more expensive, have longer lead times, and are limited in availability, as they are produced in smaller batches due to lower demand compared to commercial-grade parts. Manufacturers may not keep them in stock and often produce them only on a specialorder basis. Nevertheless, another MOSFET, TK34A10N1, with similar voltage stress characteristics but a lower R_{DSON} was selected. The simulation results are presented in Table VI. It is evident from the table that reducing R_{DSON} from 44 mΩ (IRF540NPBF) to 7.9 mΩ (TK34A10N1) can contribute to a lower failure rate and improved efficiency. However, this improvement comes at the cost of a higher unit price, as the TK34A10N1 is approximately twice as expensive as the IRF540NPBF.

Based on the above discussion, it is highly recommended to select capacitors with a higher voltage rating, as this significantly improves reliability. For example, the MTTF increases from 182665 h to 372491 h, effectively doubling the lifetime, while the cost increases by only $0.21. Additionally, if the physical size of the converter is not a limiting factor, it is also beneficial to choose larger capacitors with the same voltage rating, as they typically offer better thermal performance and durability. Although the price increase for MOSFET is more substantial, it is still worthwhile to use a higher-grade JANTX device, as the MTTF increases significantly, from 0.35 × 10^6 h to 1.3 × 10^6 h, reflecting a major improvement in reliability under harsh operating conditions.

TABLE VI
COMPARISON OF FAILURE RATE AND MTTF FOR TWO DIFFERENT MOSFETS

Operation modes	IRF540NPBF				TK34A10N1			
	λ_{MS1} (μ failures/h)	λ_{MS2L} (μ failures/h)	λ_{MS2U} (μ failures/h)	MTTF (h)	λ_{MS1} (μ failures/h)	λ_{MS2L} (μ failures/h)	λ_{MS2U} (μ failures/h)	MTTF (h)
SISO PV-battery	1.794	1.294	1.866	192860	1.387	0.983	0.736	303525
SISO PV-load	1.184	0.715	0.695	182670	1.098	0.824	0.647	232762
SISO battery-load	0.971	1.237	1.275	253570	0.960	0.737	0.783	336532
DISO	1.111	0.941	1.430	268920	0.614	0.676	0.693	457357
SIDO	1.689	1.107	1.616	217650	1.270	0.919	0.709	327030
DIDO	1.255	0.717	0.697	360250	1.087	0.842	0.646	372129

B. Thermal Management

Thermal management plays a critical role in enhancing system reliability. In general, effective cooling techniques, such as the use of heat sinks, thermal vias, and fans, help to maintain safe operating temperatures and reduce thermal stress on components. Additionally, controlling the operating environment to lower the ambient temperature can significantly reduce failure rates.

To improve the reliability of the selected converter, the ambient temperature needs to be effectively controlled, as excessive heat is a leading contributor to premature component failure. One practical solution is to install the converter in a thermally conductive enclosure, designed to facilitate efficient heat dissipation. This enclosure should be equipped with a thermal sensor and an actively controlled fan, which together help maintain a stable internal temperature and protect the converter from environmental stressors such as dust, direct sunlight, and high humidity. The thermal sensor continuously monitors the internal temperature, allowing the fan to respond dynamically to changing thermal conditions. The fan's operation can be easily managed by the microcontroller already embedded in the system, which also handles the converter's control logic and operating modes. This integration reduces the need for additional hardware and ensures responsive thermal regulation based on real-time system demands.

Once the converter is installed in a thermally conductive enclosure and the fan is actively controlled to maintain the temperature around a specified value, the environmental classification can effectively be changed from GF to GB, as defined in MIL-HDBK-217F, which corresponds to a decrease in ambient temperature from 40 °C to 30 °C. As shown in Fig. 5, the sensitivity analysis confirms that a 10 °C reduction in ambient temperature leads to an MTTF improvement of approximately 11%–14%. This improvement is critical because high RMS currents in the converter generate significant heat ($P_{loss} = I_{rms}^2 \times ESR$). Managing this heat prevents it from accelerating component wear-out, serving as a secondary mitigation layer alongside electrical stress reduction.

C. Power Loss Reduction

Minimising power loss in power systems and power electronics is crucial not only for improving efficiency but also for enhancing long-term reliability [27]. Therefore, optimising

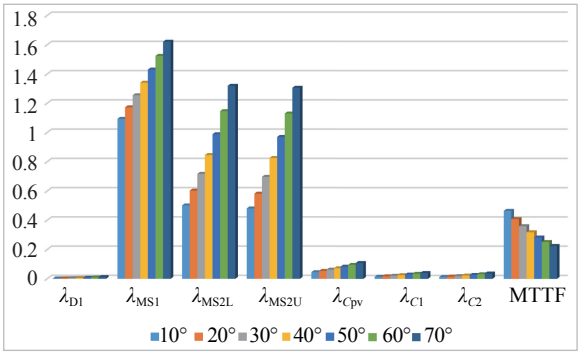

Fig. 5. Failure rates and MTTF calculated at various ambient temperatures corresponding to standard environmental conditions, including GB at 30 °C, GF at 40 °C, Ground Mobile (GM) at 45–55 °C and Airborne Inhabited Controlled (AIC) at 70 °C. The failure rate is expressed in units of 10^{-6} failures/h, where the MTTF is expressed in units 10^6 h.

circuit design to reduce power losses is an effective strategy to increase system reliability. By applying various techniques to minimise both switching and conduction losses, the MTTF of the studied inverter can be significantly extended.

These techniques include implementing soft-switching methods such as zero voltage switching (ZVS) and zero current switching (ZCS), which reduce voltage and current stresses on semiconductor devices during switching transitions [28]. This significantly lowers switching losses and mitigates thermal cycling effects. Additionally, the incorporation of snubber circuits and clamping diodes helps suppress voltage spikes and transient overvoltages, protecting components like MOSFETs and diodes from premature failure. Selecting components with low equivalent series resistance (ESR) and low on-resistance (R_{on}) is another critical strategy. For instance, polyester film capacitors, known for their low ESR, excellent thermal stability, and high reliability under pulsed conditions, minimise heating and energy dissipation in filtering and energy storage stages [29]. Likewise, choosing power semiconductors with optimised packaging and reduced R_{on} values decreases conduction losses [30]. All these techniques can be incorporated into future designs to significantly enhance the reliability of power converters.

D. Control-Based Reliability Enhancement

The SISO PV–load operating mode exhibits the highest

component failure rate and the lowest MTTF, which highlights the need for special attention during both circuit design and control strategy development. In this mode, the PV module alone supplies power to the load while the battery remains disconnected, typically because it is fully charged. Under these conditions, the PV converter operates at a higher voltage and current stress, especially on the switching devices and input capacitors, resulting in higher junction temperature fluctuations and accelerated aging.

To mitigate this, a reliability-oriented control strategy is implemented that limits the battery SoC to a maximum of 90%. This ensures the converter operates predominantly in DIDO mode, where the battery remains connected to buffer transient power mismatches, effectively eliminating the high-stress SISO PV-load operating condition. This requires a minor modification to the control algorithm to ensure that the battery remains slightly involved in the energy flow, even when it is nearly fully charged, thereby reducing stress on the PV path. The proposed enhancement involves SoC based mode management. Instead of allowing the battery to reach a 100% charge state, an upper threshold is defined (e.g., $SoC_{\max} = 90\%$). By maintaining the SoC below this threshold, the converter avoids entering the high-stress SISO PV-load mode entirely. This ensures that the PV module never supplies the full load current alone, leading to more balanced current distribution among components.

Maintaining the SoC below 90% can be achieved by slightly derating the PV output power through control of the operating point on the PV curve. Specifically, the converter can be regulated to operate a few volts below the maximum power point (MPP), reducing the charging current to the battery and allowing small discharging intervals to keep the SoC within the desired range. This controlled deviation from the MPP trades a marginal reduction in energy-harvesting efficiency for a significant improvement in converter reliability and component lifetime.

To verify the effectiveness of the proposed technique, a comprehensive case study was conducted where the converter circuit was re-simulated for all operating modes. In this analysis, the power losses of active components were first determined, followed by a recalculation of component failure rates and MTTF using the updated thermal stress data. The results demonstrate a significant reliability improvement achieved by eliminating the high-stress SISO PV-load mode: the average system MTTF increased from 213036.35 h under the conventional control strategy to 242313.24 h with the reliability-based control. This substantial enhancement confirms that integrating reliability considerations into the control algorithm effectively reduces thermal and electrical stress on critical components, thereby significantly extending the expected operational lifespan of the system.

V. Conclusion

This paper presented a comprehensive reliability assessment and enhancement strategy for a non-isolated TPC utilised in standalone PV-battery systems. The analysis, conducted in accordance with the MIL-HDBK-217F standard, quantified component failure rates across six distinct operating modes. The investigation identified MOSFETs and input capacitors as the critical failure points, with the SISO PV-load mode exhibiting the highest stress levels due to elevated voltage and thermal burdens.

The study established four primary pathways for reliability improvement, supported by simulation and analytical verification:

• Component derating and selection: Analysis confirms that operating capacitors at or below 50% of their rated voltage is a dominant factor in extending lifespan. Specifically, increasing the capacitor voltage rating from 25 to 50 V resulted in a twofold increase in component MTTF (from 182665 to 372491 h) with a negligible cost increment. Furthermore, replacing commercial-grade MOSFETs with high-reliability JANTX devices significantly improved MTTF from 0.35×10^6 to 1.3×10^6 h.

• Minimisation of conduction losses: The selection of MOSFETs with lower on-resistance (R_{DSON}) was shown to mitigate thermal stress effectively. Comparing a standard device (44 mΩ) with a low-resistance alternative (7.9 mΩ) revealed a notable reduction in failure rates, validating the trade-off between higher component cost and extended system durability.

• Thermal sensitivity: Sensitivity analysis quantified the impact of environmental conditions, demonstrating that a 10 °C reduction in ambient temperature—achievable through active thermal management and enclosure de- sign—yields an approximate 11%–14% improvement in system MTTF.

• Reliability-aware control strategy: A novel control algorithm based on SoC management was proposed to mitigate the effects of the high-stress SISO PV-load mode. By dynamically regulating the battery SoC to avoid this operating region, the average system MTTF increased from 213036 h under conventional control to 242313 h.

These findings demonstrate that integrating reliability constraints into both the hardware design phase and the control algorithm significantly enhances the resilience of MPCs. Future work will focus on experimental aging tests to further validate these theoretical models under dynamic mission profiles.

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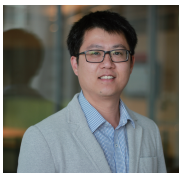
Mohammad Raja Al-Soeidat received the B.Eng. degree in Electrical Engineering (Communication Engineering) from Al-Hussein Bin Talal University (AHU), Ma'an, Jordan, in 2013, the M.Eng. degree in electrical engineering from the University of Sydney, Sydney, Australia, in 2016, and the Ph.D. degree in power electronics from the University of Technology Sydney (UTS), Sydney, Australia, in 2020, at the School of Electrical and Data Engineering. In 2013, he joined Zain Jordan as a Radio Access Network Engineer. From 2017 to 2021, he was a Senior Research Assistant with the School of Electrical and Data Engineering, UTS. In 2022, he joined Al-Hussein Bin Talal University as a Lecturer in the Department of Electrical Engineering and was promoted to Assistant Professor in 2023. His research interests include renewable energy applications and reliability, power electronics, energy conversion systems, smart grids, electric vehicles, and energy storage systems. He received a grant from AHU to support his Master's and Ph.D. studies.

Habes Ali Khawaldeh received the B.E. degree in electrical and computer engineering from the Hashemite University, Jordan, in 2009, and the M.S. degree in electrical power engineering from Yarmouk University, Jordan, in 2013. In 2022, Habes Ali Khawaldeh received his Ph.D. degree in power electronics engineering from Faculty of Engineering and Information Technology, University of Technology Sydney (UTS), Australia. Currently, Habes is an assistant professor at the University of AL AL-bayt in Jordan.

Khaled Al Khalyfeh is an Associate Professor of Inorganic Chemistry at Al-Hussein Bin Talal University (AHU), Ma'an, Jordan. Earned the Ph.D. in inorganic chemistry/electrochemistry from Chemnitz University of Technology, Germany in 2017. He focuses on inorganic/electrochemical materials research topics, and has a long stand collaboration on several projects funded by the German Research Foundation (DFG), Chemnitz University of Technology (Visiting Scholar) and AHU. His recent work centers on developing advanced sensing materials.



Dylan Dah-Chuan Lu received his Ph.D. degree in Electronic and Information Engineering from the Hong Kong Polytechnic University in 2004. From 2006 to 2016, he was a full-time faculty member at the University of Sydney, Australia. In July 2016, he joined the University of Technology Sydney, where he currently serves as a Professor and Head of Discipline of Electrical Power and Energy Systems in the School of Electrical and Data Engineering. His research interests and publications are centered on developing efficient, cost-effective, and reliable power conversion solutions for renewable energy sources, energy storage systems, and microgrids.

Muheeb Ahmad Alkhalayfeh is a research fellow at the Institute of Nano Optoelectronics Research and Technology (INOR), Universiti Sains Malaysia. He obtained his B.Sc. degree in physics from Al- Hussein Bin Talal University in 2011, followed by an M.Sc. degree in physics from Mu'tah University, Jordan. In 2022, he obtained his Ph.D. from Universiti Sains Malaysia (USM), Malaysia. His research interests mainly focus on enhanced polymer and perovskite solar cells for indoor applications.