A Cascaded High-Step-Up Boost DC-DC Converter Circuit With Switched-Capacitor

Qiao ZHANG, Xuemei LI, Yang ZHOU, and Xuefeng HU

***Abstract*—This paper presents a switched-capacitor cascaded boost converter designed to overcome the limitations of the traditional topology. The proposed converter integrates a switched-capacitor unit, which enables the superposition of inductor energy onto the output side during the switch-off period, thereby achieving double the voltage gain of a conventional cascaded boost converter (CCBC), as defined by $M = 2/(1-D)^2$. This structure also results in significantly reduced voltage stress on the semiconductor devices. Furthermore, a collaborative filtering mechanism between the primary stage (C_2/C_3) and the secondary stage (C_0) reduces dependency on individual capacitor values while simultaneously enhancing output ripple suppression. Additional advantages include inherent input-output common ground for effective electromagnetic interference (EMI) suppression and a simplified gate driver design due to the synchronized operation of the two switches. The operational principle and steady-state performance are analyzed thoroughly. A mathematical model is derived using the state-space averaging technique and validated by simulation. Experimental results from a 250 W hardware prototype (32 V input to 400 V output) confirm the feasibility of the proposed topology.**

***Index Terms*—Boost converter, cascaded, high-step-up, low stress, switched-capacitor.**

I. Introduction

CURRENTLY, photovoltaic and fuel cell technologies are regarded as highly promising power generation solutions owing to their clean and renewable nature [1]. However, both inherently deliver low output voltages (generally below 50 V), which necessitates the use of high-gain DC-DC converters to elevate the voltage to levels compatible with grid integration (e.g., 400 V AC or ±380 V DC)[2], as illustrated in Fig. 1. In response to this challenge, extensive studies have been conducted on high-gain DC-DC converters, which can be broadly categorized into isolated and non-isolated types [3]–[11]. Isolated converter topologies typically rely on high-turn-ratio transformers for voltage amplification. This approach, however, introduces notable drawbacks, particularly energy loss due to transformer leakage inductance and voltage spikes across switching devices, which degrade efficiency and increase component stress. Therefore, non-isolated high-gain topologies based on the conventional boost structure have gained broader acceptance in practical applications, especially in renewable energy grid integration [12], [13]. These structures are valued for their design simplicity and high cost-effectiveness, along with the elimination of electrical isolation requirements. Nevertheless, they are constrained by inherent limitations such as restricted voltage gain and diode reverse recovery issues, which thereby hinders their application in high-power scenarios. To overcome these limitations, a range of high-gain solutions has been developed in the literature, such as coupled-inductor [14], [15], interleaved parallel [16]–[18], and switched-capacitor/switched-inductor cell topologies [19], [20]. While effectively improving voltage gain, these methods pose significant challenges, including greater control complexity, more difficult magnetic design, and limited efficiency optimization potential. Coupled-inductor converters can achieve higher gain by adjusting the turns ratio. However, this benefit comes at the cost of elevated voltage stress on the switches due to leakage inductance. Additional clamping circuits are therefore required, thereby introducing higher system complexity and cost, lower efficiency, and aggravated electromagnetic interference (EMI), especially during light-load operation. The benefits of interleaved parallel converters, such as reduced current ripple and increased power capacity, can be offset when the duty cycle deviates significantly from 0.5. Under such conditions, current sharing is complicated, control becomes more complex, and multiple drivers and sensors are needed. This leads to higher costs and restricts their application in wide-input-voltage scenarios. Although switched-capacitor and switched-inductor converters utilize combinations of passive components to enhance voltage gain, a larger number of switching devices is often required. Furthermore, issues such as capacitor voltage imbalance and low utilization of inductor cores remain prominent. Specifically, whereas simple structures offer only limited gain, multi-stage cascading tends to result in reduced efficiency

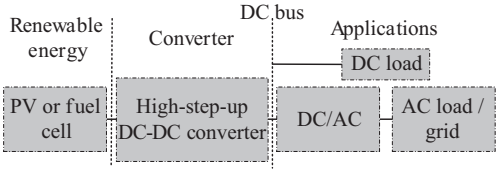

Fig. 1. Typical renewable energy generation system.

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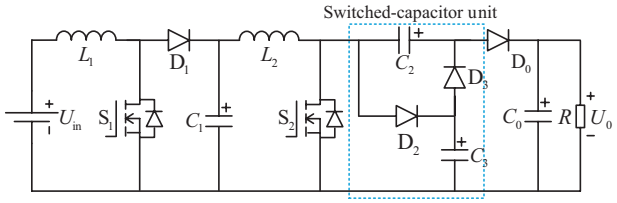

Fig. 2. Topology of the proposed boost converter.

and increased control complexity. Other derived topologies, including multilevel and *Z*-source/*qZ*-source converters [21]–[23], are also confronted with several limitations. These include challenges in capacitor voltage balancing, the occurrence of high inrush currents, and the fact that devices are subjected to significant electrical stress.

To overcome the above shortcomings, a novel dual-switch controlled cascaded switched-capacitor high-gain DC-DC topology is introduced. Its control strategy ensures both an extremely high voltage gain and markedly reduced switch voltage stress. The rational cascaded design further allows for high conversion efficiency to be maintained, along with a significant reduction in passive components and effective handling of capacitor voltage balancing. Experimental results confirm that the proposed circuit structure maintains a common ground between its input and output ports while achieving a high voltage gain. This feature significantly reduces EMI, making the converter well-suited for high-gain applications, particularly in grid-connected photovoltaic systems. This paper is structured as follows: Section II details the topological configuration and working principles of the proposed converter. Section III presents a steady-state performance analysis. Sections IV and V cover component design and comparative evaluation, respectively, while experimental verification and conclusions are provided in Sections VI and VII.

II. Principle of the Proposed Converter

A. Circuit Composition

The converter is composed of a front-end cascaded structure and a rear-end switched-capacitor unit as depicted in Fig. 2. The front-end section includes two power switches (S_1 and S_2), two inductors (L_1 and L_2), diode D_1 and capacitor C_1. The switched-capacitor cell comprises D_2, D_3, and C_2, C_3. V_{in} and V_0 denote the input and output voltages. V_{C1}, V_{C2}, V_{C3}, V_{C0} represent the voltages across C_1, C_2, C_3 and C_0. Similarly, U_{D1}, U_{D2}, U_{D3} and U_{D0} denote the voltages across D_1, D_2, D_3 and D_0, respectively. The main waveforms and equivalent circuits of the converter in different operating states are depicted in Figs. 3 and 4.

B. Operating Principles

For simplicity, the analytical framework relies on the following assumptions:

1) All components are treated as ideal, neglecting parasitic effects such as equivalent series resistance (ESR) and stray capacitance.

2) Capacitors are selected to be large enough that their terminal voltages remain nearly constant over an operating cycle.

3) S_1 and S_2 are driven with synchronized gate signals and operate at the same duty ratio ($d_1 = d_2 = d$).

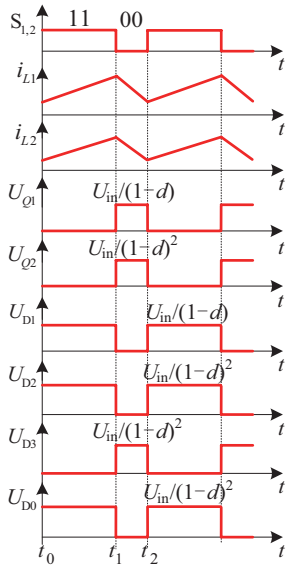

Fig. 3. Key waveforms of the proposed converter.

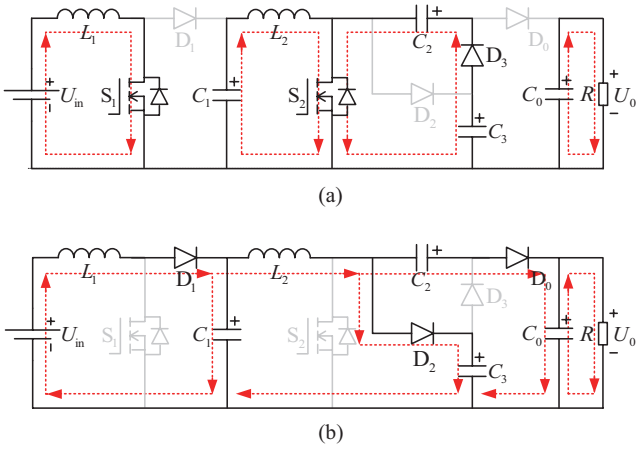

Fig. 4. Switching states of the proposed converter. (a) S_1S_2 are turned on. (b) S_1S_2 are turned off.

The operational analysis in this section is carried out according to the two distinct states within a switching cycle, which are segmented in time as illustrated in Fig. 3.

State 1 (t_0–t_1): During this period, S_1 and S_2 are conducted on by synchronized pulse width modulation (PWM) gate signals. D_0–D_2 are reverse biased owing to C_0, C_1, C_3, depicted in Fig. 4(a). The input source V_{in} and C_1 energize L_1 and L_2 through S_1 and S_2, respectively (path: V_{in}–L_1–S_1, C_1–L_2–S_2). Resulting in a linear increase of inductor current. Capacitor C_3 discharges to C_2 through D_3 and S_2 (path: C_3–D_3–C_2–S_2). During this period, the C_0 deliveries power to R.

State 2 (t_1–t_2): During this stage, both S_1 and S_2 are off. The input source V_{in} and L_1 are connected in series, conducting through D_1, thereby forming the primary charging path for C_1 (path: V_{in}–L_1–D_1–C_1). Concurrently, the same current continues through D_2 and L_2 to charge C_3 (path: V_{in}–L_1–D_1–L_2–D_2–C_3). Finally, energy is transferred to the output via D_0 and C_2,

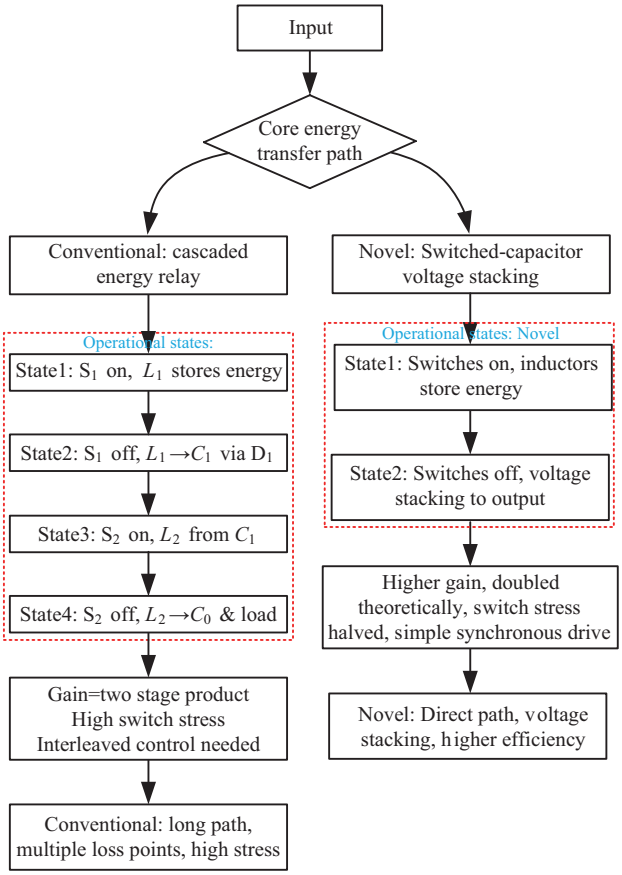

Fig. 5. Comparison of energy transfer mechanisms between CCBC and the proposed converter.

feeding the load (path: V_{in}–L_1–D_1–L_2–C_2–D_0–C_0/R).

C. Comparative Analysis of Circuit Operation Principle

The fundamental operational difference between the conventional two-switch cascaded boost converter and the proposed topology can be conceptualized through their distinct energy transfer philosophies, as summarized in Fig. 5. The conventional converter operates on a "cascaded energy relay" principle, where energy is processed and transferred sequentially through two completely decoupled stages, as shown in Fig. 5 (left). In stark contrast, the proposed converter employs a "switched-capacitor voltage stacking" principle. Here, during the switch-off period, the inductor current is directed to charge the switched-capacitor network, whose voltage is then algebraically added to the input source voltage before being delivered to the output, as shown in Fig. 5 (right). This intrinsic difference in the energy transfer path is the root cause for the superior performance metrics, such as the higher voltage gain and reduced voltage stress, as listed in Table I.

III. Steady-State Performance Analysis

A. Calculations of Voltages

When S_1 and S_2 are driven ON, the closed-loop paths in the power stage, as shown in Fig. 4(a) are analyzed using Kirchhoff's voltage law (KVL), leading to (1):

$$\begin{cases} -V_{in} + V_{L1+} = 0 \\ -V_{C1} + V_{L2+} = 0 \\ -V_{C2} + V_{C3} = 0 \end{cases} \tag{1}$$

Following the same procedure, the voltage equations for the loops in Fig. 4(b) are derived using KVL:

$$\begin{cases} -V_{in} + V_{L1-} + V_{C1} = 0 \\ -V_{in} + V_{L1-} + V_{L2-} + V_{C3} = 0 \\ -V_{in} + V_{L1-} + V_{L2-} - V_{C2} + V_{C0} = 0 \end{cases} \tag{2}$$

where the subscript "+" denotes the inductor's charging state; "–" denotes its discharging state.

By considering the volt-second balance principle in (1) and (2), a governing expression for inductors L_1 and L_2 is derived:

$$\begin{cases} d \times V_{in} + (1-d) \times (V_{in} - V_{C1}) = 0 \\ d \times V_{C1} + (1-d) \times (V_{C1} - V_{C3}) = 0 \end{cases} \tag{3}$$

The voltage values of all capacitors can then be obtained.

$$\begin{cases} V_{C1} = \dfrac{1}{1-d} \times U_{in} \\ V_{C2} = V_{C3} = \dfrac{1}{(1-d)^2} \times V_{in} \\ V_{C0} = \dfrac{2}{(1-d)^2} \times V_{in} \end{cases} \tag{4}$$

The voltage gain can be obtained as:

$$M = \frac{V_0}{V_{in}} = \frac{2}{(1-d)^2} \tag{5}$$

From the analysis of the circuit states described above, combined with (1)–(4), the voltage stress across all components can be determined:

$$\begin{cases} V_{S1} = V_{D1} = V_{C1} = \dfrac{1}{1-d} \times V_{in} \\ V_{S2} = V_{D2} = V_{D3} = V_{D0} = V_{C3} = \dfrac{1}{(1-d)^2} \times V_{in} \end{cases} \tag{6}$$

B. Calculations of Currents

Based on the two switching-state equivalent circuits shown in Fig. 4, the instantaneous expressions for all capacitor currents are formulated through the application of Kirchhoff's current law (KCL):

$$\begin{cases} I_{C1(on)} = -I_{L2} \\ I_{C2(on)} = -I_{C3(on)} \\ I_{C3(on)} = -I_{C2(on)} \\ I_{C0(on)} = -I_0 \end{cases} \quad \begin{cases} I_{C1(off)} = I_{L1} - I_{L2} \\ I_{C2(off)} = -I_{L2} + I_{C3(off)} \\ I_{C3(off)} = I_{L2} + I_{C2(off)} \\ I_{C0(off)} = -I_0 - I_{C2(off)} \end{cases} \tag{7}$$

Assuming 100% efficiency and based on the principle of power conservation ($P_{in} = P_{out}$), the charging and discharging

TABLE I
THE COMPARISONS BETWEEN THE PROPOSED TYPOLOGY AND THE OTHER TYPOLOGIES

Topology	Switches	Diodes	Capacitors	Inductors	Total elements	V_{S_max}/V_0	V_{D_max}/V_0	Common ground	Voltage gain
Boost	1	1	1	1	4	1	1	Yes	$\frac{1}{1-d}$
[12]	1	3	3	1	8	1/2	1/2	No	$\frac{2}{1-d}$
[8]	2	3	3	2	10	1/(3−d)	2/(3−d)	No	$\frac{3-d}{1-d}$
CCBC	2	2	2	2	8	1	1	Yes	$\frac{1}{(1-d)^2}$
[19]	1	4	3	2	10	1/(2−d)	1/(2−d)	Yes	$\frac{2-d}{(1-d)^2}$
[21]	1	4	4	3	12	1/(1+d)	1/(1+d)	No	$\frac{1-d}{(1-d)^2}$
[13]	1	5	3	3	12	1	1	Yes	$\frac{2}{(1-d)^2}$
Proposed	2	4	2	4	12	1/2	1/2	Yes	$\frac{2}{(1-d)^2}$

of inductors in the circuit, I_{L1} and I_{L2} can be derived.

$$\begin{cases} I_{L1} = I_{\text{in}} = \dfrac{2}{(1-d)^2} \times I_0 \\ I_{L2} = \dfrac{2}{1-d} \times I_0 \end{cases} \tag{8}$$

By combining the circuit equations from (7) and (8) and applying the charge-balance principle, the capacitor current expressions for both switching states are derived, thus obtaining the following results:

$$\begin{cases} I_{C1(\text{on})} = \dfrac{-2I_0}{1-d} \\ I_{C2(\text{on})} = \dfrac{I_0}{d} \\ I_{C3(\text{on})} = \dfrac{-I_0}{d} \\ I_{C0(\text{on})} = -I_0 \end{cases} \text{ and } \begin{cases} I_{C1(\text{off})} = \dfrac{2dI_0}{(1-d)^2} \\ I_{C2(\text{off})} = \dfrac{-I_0}{1-d} \\ I_{C3(\text{off})} = \dfrac{I_0}{1-d} \\ I_{C0(\text{off})} = \dfrac{dI_0}{1-d} \end{cases} \tag{9}$$

On the basis of the preceding analysis, the current stress experienced by the switches and diodes is summarized as follows:

$$\begin{cases} I_{S1} = \dfrac{2I_0}{(1-d)^2} \\ I_{S2} = \dfrac{(1+d)I_0}{d(1-d)} \end{cases} \quad \begin{cases} I_{D1} = \dfrac{2I_0}{(1-d)^2} \\ I_{D0} = I_{D2} = \dfrac{I_0}{1-d} \\ I_{D3} = \dfrac{I_0}{d} \end{cases} \tag{10}$$

Based on the circuit analysis, the root mean square (RMS) current levels for the semiconductor elements are determined as:

$$\begin{cases} I_{S1(\text{rms})} = \dfrac{2\sqrt{d}}{d(1-d)^2} I_0 \\ I_{S2(\text{rms})} = \dfrac{\sqrt{d}(1+d)}{d^2(1-d)} I_0 \\ I_{D1(\text{rms})} = \dfrac{2\sqrt{1-d}}{(1-d)^3} I_0 \\ I_{D0(\text{rms})} = I_{D2(\text{rms})} = \dfrac{\sqrt{1-d}}{(1-d)^2} I_0 \\ I_{D3(\text{rms})} = \dfrac{\sqrt{d}}{d^2} I_0 \end{cases} \tag{11}$$

As can be seen from (11), the switches S_1 and S_2 and D_1 located in the main power transfer path are subject to current stresses that are multiples of the output current I_0. This is an inherent trade-off for achieving high voltage gain. In contrast, D_0, D_2, and D_3 only conduct currents comparable to or less than the load current, as they are not directly involved in the primary voltage-boosting process.

Consistent with (8), the RMS current of L_1 and L_2 equal its average value. The RMS current calculations for the capacitive components proceed as follows:

$$\begin{cases} I_{C1(\text{rms})} = \dfrac{2\sqrt{d}}{\sqrt{1-d}(1-d)} I_0 \\ I_{C2(\text{rms})} = I_{C3(\text{rms})} = \sqrt{\dfrac{1}{d(1-d)}} I_0 \\ I_{C0(\text{rms})} = \sqrt{\dfrac{d}{1-d}} I_0 \end{cases} \tag{12}$$

As indicated in (12), the current stress on C_1 is the most pronounced. This is attributed to its critical role in both charge transfer and energy buffering during the two switching states. In

contrast, the output C_0 exhibits the minimum current stress, which aligns with its primary function as an output voltage filter.

C. Inductor and Capacitor Ripple

Combining the established voltage-current equations with previous analytical results allows for the determination of the inductor current ripple (Δi_{L1}, Δi_{L2}) and capacitor voltage variations (Δv_{C1}, Δv_{C2}, Δv_{C3}, and Δv_{C0}) as follows:

$$\begin{cases} \Delta i_{L1} = \dfrac{d(1-d)^2 U_0 T_S}{2L_1} \\ \Delta i_{L2} = \dfrac{d(1-d) U_0 T_S}{2L_2} \end{cases} \quad \begin{cases} \Delta u_{C1} = \dfrac{2dU_0 T_S}{(1-d)RC_1} \\ \Delta u_{C2} = \dfrac{U_0 T_S}{RC_2} \\ \Delta u_{C3} = \dfrac{U_0 T_S}{RC_3} \\ \Delta u_{C0} = \dfrac{dU_0 T_S}{RC_0} \end{cases} \tag{13}$$

(13) reveals the dependencies of both the inductor current ripple and the capacitor voltage ripples on circuit parameters, including D, V_0, T_s, R, and the respective component values. This relationship thus serves as a direct basis for determining the required values of L_1, L_2, C_1, C_2, C_3, and C_0.

D. Losses and Efficiency

The total power loss of the switches is primarily composed of conduction losses and switching losses.

$$P_S = \sum_{i=1}^{2} I_{Si(\mathrm{rms})}{}^2 r_{dsi} + \sum_{i=1}^{2} \frac{1}{2} V_{Si} \left[V_{Si} C_{ossi} + I_{Si}(t_{ri} + t_{fi}) \right] f_S \tag{14}$$

where the parameters are defined as: r_{ds} = on-state resis-tance, C_{oss} = output capacitance, t_r = rise time, and t_f = fall time.

The total power loss in the diode arises from two components: the loss due to the forward voltage drop (V_F) and the ohmic loss associated with its on-state resistance (r_D).

$$P_D = \sum_{i=1}^{3} V_{Fi} I_{Di} + V_{F0} I_{D0} + \sum_{i=1}^{3} I_{Di(\mathrm{rms})}{}^2 r_{Di} + I_{D0(\mathrm{rms})}{}^2 r_{D0} \tag{15}$$

The total power dissipation in L_1 and L_2 can be determined using the following expression, which accounts for the RMS currents and ESR (r_L):

$$P_L = \sum_{i=1}^{2} I_{Li(\mathrm{rms})}{}^2 r_{Li} \tag{16}$$

The capacitor losses are calculated as below:

$$P_C = \sum_{i=1}^{3} I_{Ci(\mathrm{rms})}{}^2 r_{Ci} + I_{C0(\mathrm{rms})}{}^2 r_{C0} \tag{17}$$

where r_C denotes the ESR of capacitor.

By incorporating the loss parameters obtained from (14) to (17) into the efficiency model, the overall conversion efficiency of the converter is derived as:

$$\eta = \frac{P_0}{P_{sum}} = \frac{P_0}{P_0 + P_S + P_D + P_L + P_C} \tag{18}$$

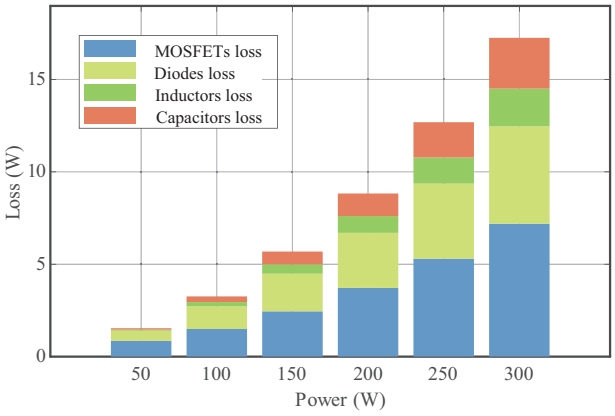

Fig. 6. Histogram of loss distribution.

$$\begin{aligned} P_{sum} &= P_0 + P_S + P_D + P_L + P_C \\ &= \frac{P_0}{Rd}(4\alpha^2 r_{ds1} + \beta^2 r_{ds2}) + \frac{4\alpha P_0(\alpha r_{L1} + r_{L2})}{R} + \\ &\quad \frac{P_0 f_S}{4}[2\alpha\delta(t_{r1} + t_{f1}) + \beta(t_{r2} + t_{f2})] + 2\alpha V_{F1} I_0 + \\ &\quad \frac{(V_{F2} + V_{F0}) I_0}{\delta} + \frac{V_{F3} I_0}{d} + \frac{4\alpha^2 P_0 r_{D1}}{\delta R} + \\ &\quad \frac{\alpha^2 \delta P_0 (r_{D0} + r_{D2})}{R} + \frac{P_0 r_{D3}}{d^3 R} + \frac{4d\alpha^2 P_0 r_{C1}}{\delta R} + \frac{P_0(r_{C2} + r_{C3})}{d\delta R} + \\ &\quad \frac{dP_0 r_{C0}}{\delta R} + \frac{V_o^2 f_S}{8}(\delta^2 C_{oss1} + C_{oss2}) \end{aligned} \tag{19}$$

where $\alpha = 1/(1-d)^2$, $\beta = (1+d)/d(1-d)$ and $\delta = (1-d)$.

The loss distribution and theoretical efficiency are analyzed using parameters obtained from the component datasheets. Fig. 6 presents the loss distribution in histogram form derived from the analytical model. The corresponding efficiency curve is plotted in Fig. 7, which shows that the converter achieves a peak efficiency of 97.01% at a light load of 50 W, with efficiency monotonically decreasing as the output power increases to the full-load condition of 300 W.

E. Small Singal Analysis

The operational states define specific capacitor connections. When S_1, S_2 are turned ON simultaneously, C_3 is connected in parallel with C_2 through D_3 and S_2. Conversely, when both switches are OFF, C_3 forms a series connection with C_2, and this combination is then placed in parallel with the output capacitor C_0 via D_0, as illustrated in Fig. 4. These interconnection constraints lead to the following relationship among the capacitors, indicating a dependency that reduces the number of independent variables in the system.

$$\begin{cases} \dfrac{C_2 \mathrm{d}v_{C2}}{\mathrm{d}t} = -\dfrac{C_3 \mathrm{d}v_{C3}}{\mathrm{d}t} \\ V_{C2} + V_{C3} = V_{C0} \end{cases} \tag{20}$$

To eliminate the ineffective variables, an ESR is introduced into the loop, and thus (20) can be rewritten as:

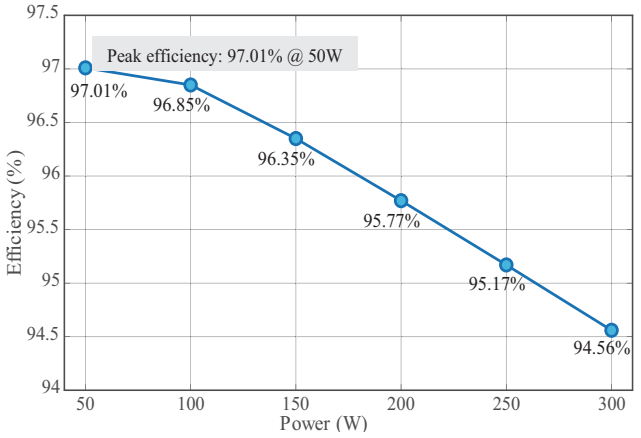

Fig. 7. Curve of the theoretical efficiency.

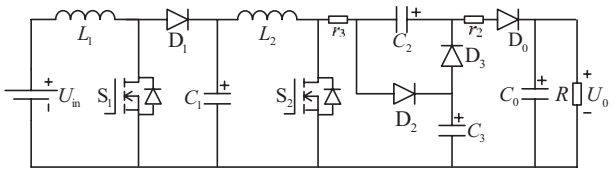

Fig. 8. Equivalent circuit with a series equivalent resistance.

$$\begin{cases} -\dfrac{C_3 \mathrm{d}v_3}{\mathrm{d}t} = \dfrac{V_{C3} - V_{C2}}{r_3} \\ -\dfrac{C_2 \mathrm{d}v_{C2}}{\mathrm{d}t} = \dfrac{V_{C3} + V_{C2} - V_{C0}}{r_2} \end{cases} \tag{21}$$

In the model, r_3 (ESR of the C_2–C_3 loop) and r_2 (ESR of the C_2–C_3–C_0 loop) are both set to 30 mΩ. The associated equivalent circuit is presented in Fig. 8.

Analysis of State 1 operation (duration dT_S) under the above conditions, using KVL and KCL on the circuit in Fig. 4(a), leads to (22).

$$\begin{cases} V_{L1} = V_{\mathrm{in}} = \dfrac{L_1 \mathrm{d}i_{L1}}{\mathrm{d}t} \\ V_{L2} = V_{C1} = \dfrac{L_2 \mathrm{d}i_{L2}}{\mathrm{d}t} \\ i_{C1} = -i_{L2} = \dfrac{C_1 \mathrm{d}v_{C1}}{\mathrm{d}t} \\ i_{C2} = \dfrac{V_{C3} - V_{C2}}{r_3} = \dfrac{C_2 \mathrm{d}v_{C2}}{\mathrm{d}t} \\ i_{C3} = -i_{C2} = \dfrac{V_{C2} - V_{C3}}{r_3} = \dfrac{C_3 \mathrm{d}v_{C3}}{\mathrm{d}t} \\ i_{C0} = -\dfrac{V_{C0}}{R} = \dfrac{C_0 \mathrm{d}v_{C0}}{\mathrm{d}t} \end{cases} \tag{22}$$

The state-space model for State 1, given in matrix form by (23), characterizes the system dynamics when both switches are ON. This model explicitly defines the coupling relationships between the inductor currents and capacitor voltages. Of particular note is the structure of the system matrix, which reveals that the output voltage v_{C0} is primarily governed by the dynamics of capacitor C_0 and the load R, as evidenced by the term $-1/RC_0$ in the lower-right corner. This structure provides critical insight for the subsequent controller design.

$$\begin{bmatrix} \dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C1}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C3}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1}{L_2} & 0 & 0 & 0 \\ 0 & \dfrac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \dfrac{-1}{r_3 C_2} & \dfrac{1}{r_3 C_2} & 0 \\ 0 & 0 & 0 & \dfrac{1}{r_3 C_3} & \dfrac{-1}{r_3 C_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & \dfrac{-1}{RC_0} \end{bmatrix} \times \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ v_{C3}(t) \\ v_{C0}(t) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \times v_{\mathrm{in}}(t) \tag{23}$$

Similarly, when the converter operates in state 2, applying KVL and KCL law, (24) can be obtained.

$$\begin{cases} V_{L1} = V_{\mathrm{in}} - V_{C1} = \dfrac{L_1 \mathrm{d}i_{L1}}{\mathrm{d}t} \\ V_{L2} = V_{C1} - i_{L2} \cdot r_3 - V_{C3} = \dfrac{L_2 \mathrm{d}i_{L2}}{\mathrm{d}t} \\ i_{C1} = i_{L1} - i_{L2} = \dfrac{C_1 \mathrm{d}v_{C1}}{\mathrm{d}t} \\ i_{C2} = \dfrac{V_{C0} - V_{C2} - V_{C3}}{r_2} = \dfrac{C_2 \mathrm{d}v_{C2}}{\mathrm{d}t} \\ i_{C3} = i_{L2} + i_{C2} = i_{L2} + \dfrac{V_{C0} - V_{C2} - V_{C3}}{r_2} = \dfrac{C_3 \mathrm{d}v_{C3}}{\mathrm{d}t} \\ i_{C0} = -i_{C2} - \dfrac{V_{C0}}{R} = \dfrac{V_{C2} + V_{C3} - V_{C0}}{r_2} - \dfrac{V_{C0}}{R} = \dfrac{C_0 \mathrm{d}v_{C0}}{\mathrm{d}t} \end{cases} \tag{24}$$

The model for state 2, described by (25), exhibits a more complex system matrix compared to state 1. This complexity arises from the series-parallel reconfiguration of capacitors C_2 and C_3 with the output, introducing additional coupling terms, particularly those involving the ESR r_2. The resulting averaged model (25), incorporates the interactions between the two switching states, forming the foundation for frequency-domain analysis and control design.

$$\begin{bmatrix} \dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C1}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C3}(t)}{\mathrm{d}t} \\ \dfrac{\mathrm{d}v_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \dfrac{-1}{L_1} & 0 & 0 & 0 \\ 0 & \dfrac{-r_3}{L_2} & \dfrac{1}{L_2} & 0 & \dfrac{-1}{L_2} & 0 \\ \dfrac{1}{C_1} & \dfrac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \dfrac{-1}{r_2 C_2} & \dfrac{-1}{r_2 C_2} & \dfrac{1}{r_2 C_2} \\ 0 & \dfrac{1}{C_3} & 0 & \dfrac{-1}{r_2 C_3} & \dfrac{-1}{r_2 C_3} & \dfrac{1}{r_2 C_3} \\ 0 & 0 & 0 & \dfrac{1}{r_2 C_0} & \dfrac{1}{r_2 C_0} & \dfrac{R + r_2}{-r_2 R C_0} \end{bmatrix} \times \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ v_{C3}(t) \\ v_{C0}(t) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \times v_{\mathrm{in}}(t) \tag{25}$$

From (23) and (25), the state-space averaged equation for one switching cycle is derived, as given in (26).

$$\begin{bmatrix} \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}v_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1-d}{-L_1} & 0 & 0 & 0 \\ 0 & \frac{r(1-d)}{-L_2} & \frac{1}{L_2} & 0 & \frac{1-d}{-L_2} & 0 \\ \frac{1-d}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{rC_2} & \frac{2d-1}{rC_2} & \frac{1-d}{rC_2} \\ 0 & \frac{1-d}{C_3} & 0 & \frac{2d-1}{rC_3} & \frac{-1}{rC_3} & \frac{1-d}{rC_3} \\ 0 & 0 & 0 & \frac{1-d}{rC_0} & \frac{1-d}{rC_0} & \frac{dR-R-r}{rRC_0} \end{bmatrix} \times \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ v_{C3}(t) \\ v_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \times v_{\mathrm{in}}(t) \tag{26}$$

Express all variables as the sum of their DC and small-signal components, i.e., introducing perturbations, as shown in (27).

I_{L1}, I_{L2}, V_{C1}, V_{C2}, V_{C3}, V_{in}, V_{C0}, and D denote the steady-state components, and $i_{L1}(t)$, $i_{L2}(t)$, $v_{C1}(t)$, $v_{C2}(t)$, $v_{C3}(t)$, $v_{\mathrm{in}}(t)$, $v_{C0}(t)$, and d represent the dynamic small-signal perturbations corresponding to the system's steady-state operating point.

$$\begin{cases} i_{L1}(t) = I_{L1} + \hat{i}_{L1}(t) \\ i_{L2}(t) = I_{L2} + \hat{i}_{L2}(t) \\ v_{C1}(t) = V_{C1} + \hat{v}_{C1}(t) \\ v_{C2}(t) = V_{C2} + \hat{v}_{C2}(t) \\ v_{C3}(t) = V_{C3} + \hat{v}_{C3}(t) \\ v_{C0}(t) = V_{C0} + \hat{v}_{C0}(t) \\ d = D + \hat{d} \end{cases} \tag{27}$$

By substituting (27) into the resulting expression, separating the disturbance terms, and neglecting higher-order small-signal components, the small-signal model of the proposed converter is derived. The complete algebraic formulation of this model is presented in (28) below.

$$\begin{bmatrix} \frac{\mathrm{d}\hat{i}_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{i}_{L2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C0}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1-d}{-L_1} & 0 & 0 & 0 \\ 0 & \frac{r(1-d)}{-L_2} & \frac{1}{L_2} & 0 & \frac{1-d}{-L_2} & 0 \\ \frac{1-d}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{rC_2} & \frac{2d-1}{rC_2} & \frac{1-d}{rC_2} \\ 0 & \frac{1-d}{C_3} & 0 & \frac{2d-1}{rC_3} & \frac{-1}{rC_3} & \frac{1-d}{rC_3} \\ 0 & 0 & 0 & \frac{1-d}{rC_0} & \frac{1-d}{rC_0} & \frac{dR-R-r}{rRC_0} \end{bmatrix} \times \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{C0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \times \hat{u}_{\mathrm{in}}(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{r}{L_2} & 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{-1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{rC_2} & \frac{-1}{rC_2} \\ 0 & \frac{-1}{C_3} & 0 & \frac{2}{rC_3} & 0 & \frac{-1}{rC_3} \\ 0 & 0 & 0 & \frac{-1}{rC_0} & \frac{-1}{rC_0} & \frac{1}{rC_0} \end{bmatrix} \times \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C3} \\ U_{C0} \end{bmatrix} \times \hat{d}(t) \tag{28}$$

$$G_{v_0 d}(s) = \frac{\hat{v}_0(s)}{\hat{d}(s)}\Big|_{\hat{v}_{\mathrm{in}}(s)=0} = \frac{1.6\times10^{39}s^5 - 6.1\times10^{56}s^4 - 1.0\times10^{62}s^3 + 1.4\times10^{66}s^2 - 6.6\times10^{68}s + 5.0\times10^{72}}{4.0\times10^{47}s^6 + 1.3\times10^{53}s^5 + 1.1\times10^{58}s^4 + 9.4\times10^{59}s^3 + 4.5\times10^{64}s^2 + 9.8\times10^{65}s + 2.5\times10^{69}} \tag{29}$$

IV. Parameters Design

The design of the power and controller circuit parameters of the target converter is carried out as subsequent analysis.

A. Power Circuit

The operating conditions for the proposed converter are defined as:

1) DC supply voltage (input): $V_{\mathrm{dc,in}} = 32$ V;
2) High-voltage DC output: $V_{\mathrm{dc,out}} = 400$ V;
3) Target output power: $P_{\mathrm{load}} = 250$ W;
4) Converter operating frequency $f_{\mathrm{SW}} = 20$ kHz.

Guided by the preceding electrical stress characterization of semiconductor devices—including voltage/current stress, and switching dynamics, the following device models are designed to align with the observed operational constraints, ensuring

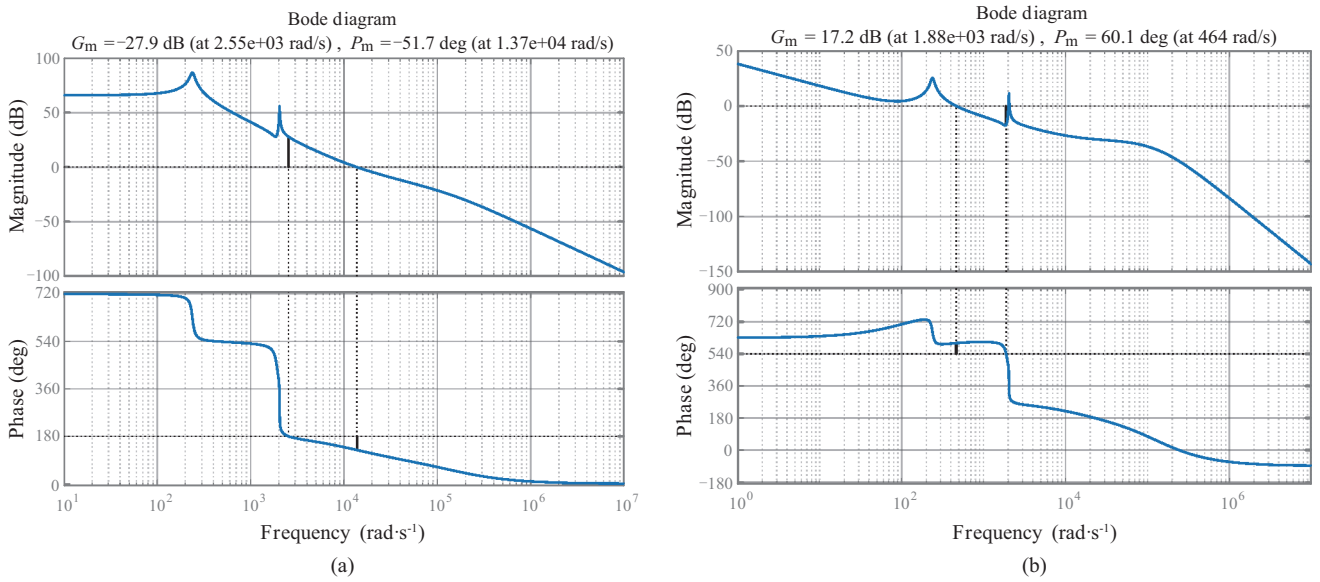

Fig. 9. Bode plot of (a) open-loop system and (b) closed-loop system.

accurate representation of real-world performance under specified loading conditions.

5) S_1 and S_2: IXTK102N30P (V_{DSS} = 300 V, I_D= 102 A);

6) D_0–D_3: DSEC60-03A (V_{RRM} = 300 V, I_{FAV}= 60 A).

The minimum required design parameters for the inductors and capacitors are obtained from (30).

$$\begin{cases} C_1 \geqslant \dfrac{2dV_0T_S}{(1-d)R\Delta v_{C1}} \\ C_2 \geqslant \dfrac{V_0T_S}{R\Delta v_{C2}} \\ C_3 \geqslant \dfrac{V_0T_S}{R\Delta v_{C3}} \\ C_0 \geqslant \dfrac{dV_0T_S}{R\Delta v_{C0}} \end{cases} \quad \begin{cases} L_1 \geqslant \dfrac{d(1-d)^2V_0T_S}{2\Delta i_{L1}} \\ L_2 \geqslant \dfrac{d(1-d)V_0T_S}{2\Delta i_{L2}} \end{cases} \tag{30}$$

For inductors L_1/L_2, design ripple current is set to 30% of the rated current; for capacitors C_1–C_3, permissible voltage ripple is 1%; and for output capacitor C_0, it is 0.5%.

The analysis above yields the following design values for the energy storage components. Specifically, L_1= 330 μH, L_2= 2 mH, C_1= 220 μF, C_2 = C_3= 68 μF, and C_0= 120 μF.

B. Controller Circuit Design

Substituting the defined parameters and component specifications into (28) and applying the Laplace transform yields the converter's control-to-output transfer function, given by (29) at the bottom of the previous page.

The bode plot derived from the uncompensated system function, as shown in Fig. 9(a), reveals a gain margin of −27.9 dB and a phase margin of −57.1°. These negative margins indicate instability under the current configuration, necessitating compensation to achieve the required dynamic response and steady-state performance.

To this end, a lead-lag compensation network is employed. The compensation function is presented in (31).

$$G_C = \frac{44787(s+120)^2}{s(s+1.256\times10^5)^2} \tag{31}$$

The closed-loop frequency response, depicted in Fig. 9(b), demonstrates significant improvement: The phase margin reaches 60.1° and the gain margin 17.2 dB, which effectively ensures system stability and enhances dynamic performance.

C. Control Design Implications

The small-signal modeling conducted in this section yields several critical conclusions that directly guide the compensator design:

1) System order and complexity: The sixth-order averaged model confirms the complex, multi-state nature of the proposed converter. The compensator must be designed to ensure stability across these interacting states.

2) Key control-to-output paths: The model identifies the primary paths from the control duty cycle (d) to the output voltage, which are essential for shaping the loop gain.

3) Stability objective: The initial analysis of the uncompensated system depicted in Fig. 9(a), conclusively demonstrates negative gain and phase margins, unequivocally necessitating compensation to achieve stable operation.

4) Compensator role: The derived transfer function, (29) provides the precise plant model required to design the type-III compensator, as show in Fig. 10. The compensator's zero/pole placement is strategically chosen to provide sufficient phase boost at the target crossover frequency, counteracting the inherent phase lag of the power stage.

In summary, the core conclusion is that while the converter's multi-element structure introduces complexity, a carefully designed lead-lag compensator is both necessary and sufficient to achieve robust stability and satisfactory dynamic performance, as

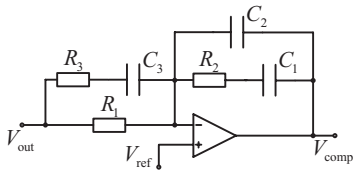

Fig. 10. Diagram of the type-III controller.

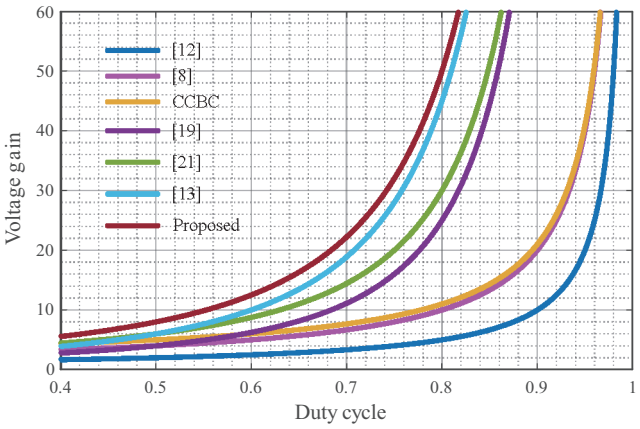

Fig. 11. Voltage gain compared with other converters.

conclusively verified by the improved margins in Fig. 9(b).

V. Comparison With Other Converters

Table I provides a comparative summary of key performance metrics for the proposed converter and several recent topologies, all designed for low-voltage renewable sources. The proposed converter achieves a superior voltage gain with lower semiconductor voltage stress, as evidenced in Fig. 11. For instance, it significantly reduces the voltage stress compared to the component-similar design in [13], attains a higher gain and lower switch stress than the simplified converter in [19], and achieves a more favorable gain-to-stress balance than the topology in [21]. These collective advantages-higher gain, reduced stress, and high efficiency-collectively demonstrate a fundamental advancement for high-step-up applications.

VI. Experimental Verification and Analysis

A prototype was built and tested in the lab for experimental validation, as illustrated in Fig. 12. Following the parameters in Section VI, the measured results confirm the analytical findings, as summarized in Table II.

Fig. 13 presents the experimental waveforms capturing the key electrical quantities at both the input and output ports (V_{in}, I_{in}, V_{out}, I_{out}) for the proposed switched-capacitor-based cascaded high-gain boost converter. As demonstrated, with an input voltage of 32 V, the converter successfully achieves a stable output voltage of 400 V, corresponding to a voltage gain of approximately 12.5. The waveforms clearly validate the excellent step-up capability of the proposed topology.

The inductor currents exhibit the expected linear ramping during the switch on and off periods, confirming the theoretical operating principle, as depicted in Fig. 14.

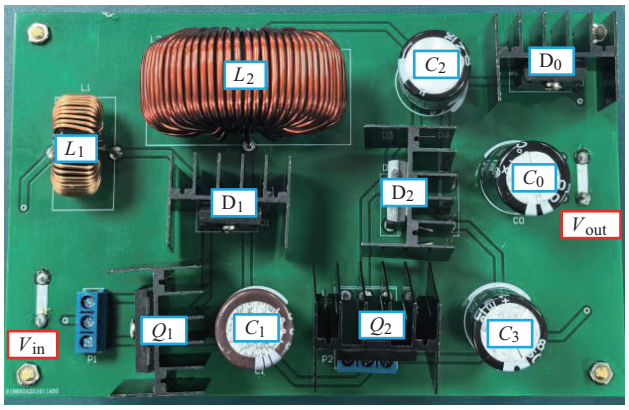

Fig. 12. Prototype of the proposed converter.

TABLE II
Components and Parameters of Prototype

Components	Parameters
Input voltage V_{in}	32 V
Output voltage V_0	400 V
Output power P	250 W
Switching frequency f_s	20 kHz
Inductors L_1 / L_2	330 μH/2 mH
MOSFETs Q_1 and Q_2	IXTK102N30P
Diodes D_0–D_2	DSEC60-03A
Capacitors C_1 / C_0	220 μF/120 μF
Capacitors C_2 and C_3	68 μF

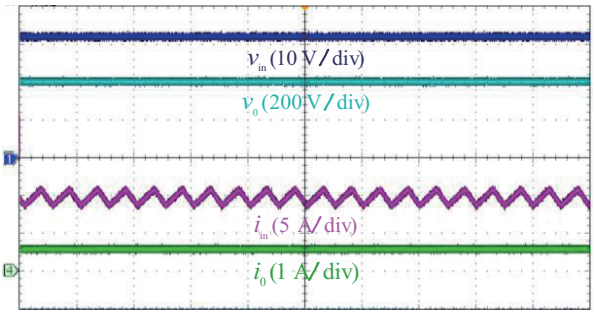

Fig. 13. Input/output voltage and current waveforms.

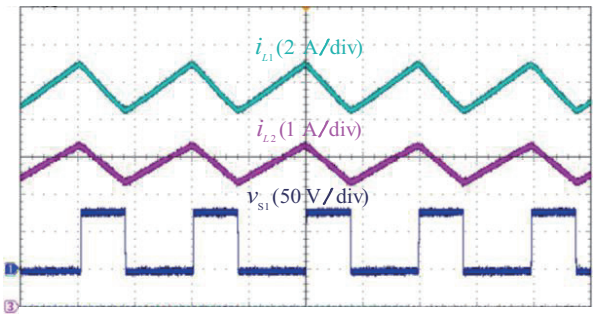

Fig. 14. Inductor L_1 and L_2 current waveforms.

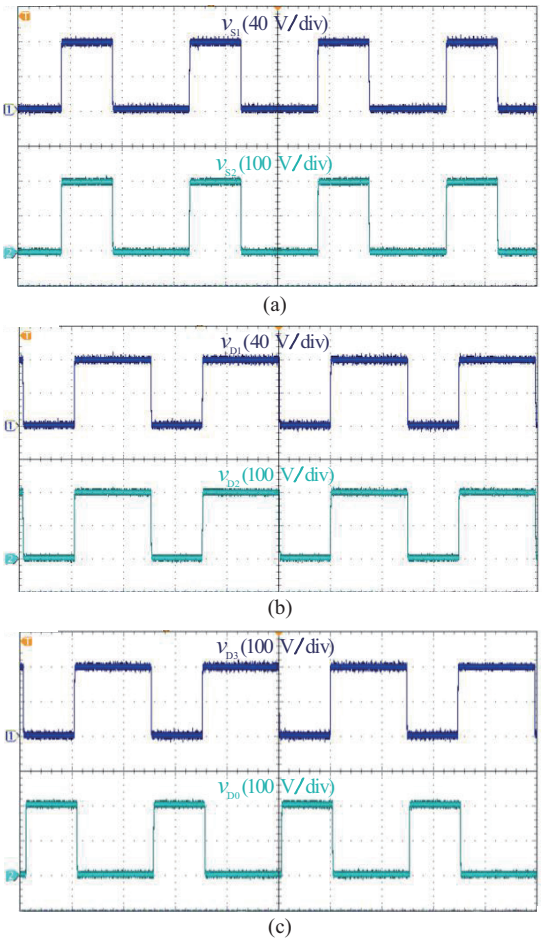

Fig. 15. Experimental verification of the voltage stresses across main semiconductors. (a) Voltage stress of switches S_1 and S_2. (b) Voltage stress of diodes D_1 and D_2. (c) Voltage stress of diodes D_3 and D_0.

Fig. 15(a)–(c) shows the voltage stress distribution across power switches S_1–S_2 and diodes D_0–D_3. Analysis reveals that the maximum voltage stress across these semiconductor devices reaches approximately 200 V—precisely half the output voltage. This feature permits the selection of low-on-resistance switches—aimed at minimizing conduction losses and high-performance diodes featuring suitably low voltage ratings to boost conversion efficiency.

To demonstrate the dynamic performance of the proposed converter, a load step-change experiment was performed by varying the load between 800 Ω and 400 Ω. As shown in Fig. 16(a), the output current rapidly increases from 0.5 A to 1 A, while the output voltage (U_0) remains regulated at approximately 400 V due to the action of the voltage control loop. Furthermore, Fig. 16(b) confirms that the output voltage remains stable at 400 V despite input voltage changes. These results collectively attest to the converter's excellent dynamic regulation.

The experimental results are summarized in Fig. 17, which illustrates the efficiency performance of the proposed converter with respect to both input voltage variation and output power variation.

Fig. 17(a) depicts the measured efficiency as a function of

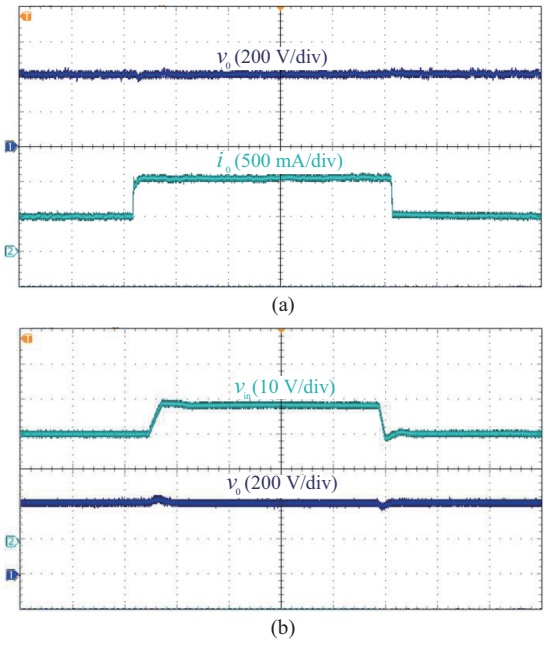

Fig. 16. Dynamic experimental waveforms of the converter. (a) Output response to a step load. (b) Input voltage disturbance.

input voltage under full-load conditions (250 W). It can be observed that the converter maintains high efficiency across a wide input voltage range, demonstrating its robustness against input variations. Fig. 17(b) compares the theoretical efficiency (red curve), derived from the analytical loss model in Section III, with the experimentally measured efficiency (blue curve) as the output power increases from 50 W to 300 W. The close theoretical-experimental alignment confirms the accuracy of the loss model in (14)–(18). The experimental results confirm a peak efficiency of 95.6% at approximately 50 W and a full-load efficiency of 94.3% at 250 W, which matches the theoretical predictions shown in Fig. 7. The slight discrepancy at medium load levels can be attributed to parasitic effects and non-ideal switching behaviors that were not fully accounted for in the theoretical model.

To further elucidate the sources of power loss at the rated operating point, a detailed loss breakdown analysis was conducted. This analysis corresponds to the experimental efficiency point at the full-load condition of P_0 = 250 W (with V_{in} = 32 V and V_{out} = 400 V), as indicated on the blue curve in Fig. 17(b).

The resulting loss distribution is presented in Fig. 17(c). It provides a quantitative dissection of the total losses, revealing that switching losses in the power MOSFETs constitute the most significant portion, accounting for approximately 40% of the total loss. This breakdown offers critical insights that align with the observations from the efficiency curves. Specifically, it corroborates why the experimental efficiency at 250 W is slightly lower than the theoretical prediction, as the model may have underestimated the switching losses. These experimental findings effectively corroborate the converter's practical efficiency performance and reinforce the conclusions drawn from the theoretical loss analysis.

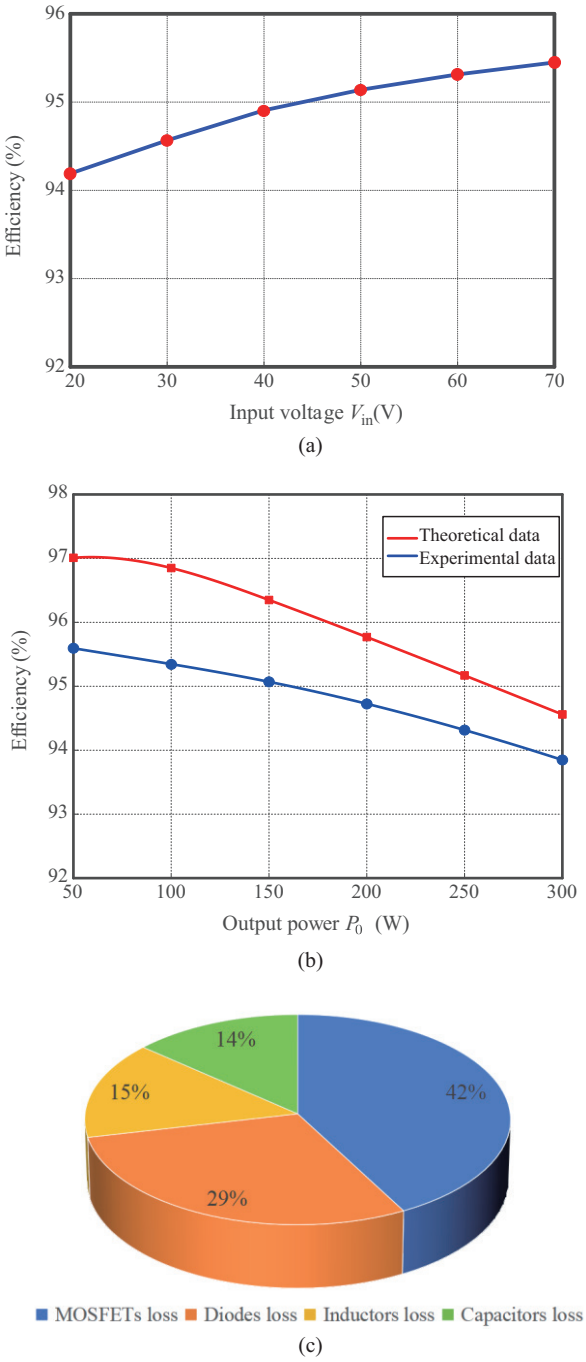

Fig. 17. Experimental efficiency of the proposed converter under various input voltage and load power. (a) Input voltage variation. (b) Load power variation. (c) Loss breakdown analysis.

VII. Conclusion

To overcome the issue of high voltage stress on semiconductor devices in conventional cascaded boost converters, this paper proposes a novel topology that incorporates a switched-capacitor unit. This design achieves a high voltage gain while significantly reducing the voltage stress across all semiconductors, effectively limiting it to 50% of the output voltage. Furthermore, the implemented common-ground configuration between the input and output ports not only reduces maintenance requirements but also mitigates electromagnetic interference, enhancing overall system reliability. Owing to these advantages, the proposed converter is particularly suitable for high-step-up conversion applications, such as solar photovoltaic and fuel cell power generation systems.

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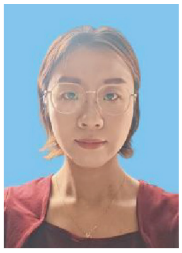

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