Hybrid Vector Control of Open-Winding Induction Motor Driven by a New L-Type Dual-Output Three-Level Inverter

Qigang DU, Guifeng WANG, Yunhui JIANG, Weipeng SHI, Chao LUO, and Ke LI

***Abstract*—To simplify the dual-inverter architecture for driving open-end winding induction motors (OEWIMs), this study proposes a dual-port 120° phase-shifted drive scheme based on an L-type dual-output three-level converter (L-DO-TLC). The proposed L-DO-TLC topology is constructed by cascading a T-type three-level inverter with a nine-switch converter in an L-shaped configuration. By reusing devices, it generates two independent three-level outputs, reducing the number of power switches from 24 to 15. Based on this topology, a hybrid-vector (HV) finite control set model predictive control (FCS-MPC) strategy is introduced. The prediction model of the OEWIM is formulated using forward Euler discretization. A voltage vector selection mechanism is then developed based on the zero-sequence current (ZSC) suppression principle, significantly reducing the computational complexity of the predictive control algorithm. To further improve control performance, an HV-MPC decision-making strategy is proposed that jointly optimizes current tracking and vector application. This method effectively mitigates the large torque ripple observed in single-vector (SV)-MPC and the high switching frequency encountered in dual-vector (DV)-MPC. Simulation and hardware-in-the-loop experimental results validate the effectiveness and advantages of the proposed strategy.**

***Index Terms*—Hybrid-vector model predictive control, L-type dual-output three-level inverter, model predictive control, open-end winding induction motor.**

I. Introduction

OPEN-END winding induction motor (OEWIM) drive system, powered by dual inverters supplying both ends of the stator windings, offers several advantages, including multi-level output capability, a relatively simple structure, and high DC voltage utilization. Consequently, it has been widely investigated in various applications [1]–[3].

Based on the DC bus power supply configuration, OEWIM drive systems can be categorized into two types: common DC bus systems [4] and isolated DC bus systems [5]. In isolated DC bus systems, the dual inverters are powered by two independent sources, which increases both system cost and complexity. In contrast, common DC bus systems utilize a single DC source, but inherently introduce a zero-sequence current (ZSC) loop, which reduces overall motor efficiency and therefore necessitates additional control strategies for ZSC suppression.

In [6], a space vector pulse width modulation (SVPWM) algorithm is proposed, in which voltage vectors corresponding to the hexagon vertices are selected to synthesize a zero-sequence voltage (ZSV) of zero, thereby effectively suppressing ZSC generation. This method fundamentally depends on the 120° decomposition of voltage vectors to synthesize the desired output voltage. Subsequently, [7] introduces a direct decoupling of voltage vectors in the dual inverter system, simplifying implementation. Compared to SVPWM, carrier-based PWM strategies reduce algorithmic complexity by incorporating controllable zero-sequence components to modulate the waveform [8]. Although various ZSC suppression algorithms have been developed, their single-objective optimization frameworks often fall short of satisfying the system's multidimensional control requirements. In contrast, finite control set model predictive control (FCS-MPC) demonstrates clear advantages under complex operating conditions due to its ability to achieve multi-objective coor-dinated optimization [9].

Building on model predictive current control, [10] formulates a cost function based on *dq*-axis current error and ZSC as optimization objectives, and introduces a voltage vector allocation mechanism within a semi-controlled common DC bus dual-inverter configuration to reduce algorithmic complexity. However, this approach does not fully consider the influence of zero-sequence components on candidate voltage vectors. To better optimize voltage vector selection, [11] proposes a hybrid dual-vector (DV) model predictive strategy. In each control cycle, Inverter 1 applies one non-zero and one zero vector, while Inverter 2 applies two non-zero vectors. This technique effectively suppresses ZSC, minimizes

Manuscript received October 31, 2025; revised January 20, 2025 and March 5, 2026; accepted March 13, 2026. Date of publication June 30, 2026; date of current version April 27, 2026. This work was supported in part by the Project of Universities in Xuzhou Serving the Development of the "343" Industries under the grant gx2024009. (*Corresponding author: Weipeng Shi*.)

Q. Du, G. Wang, W. Shi, and C. Luo are with the School of Electrical Engineering and Automation, Jiangsu Normal University, Xuzhou 221116, China (e-mail: 2020231815@jsnu.edu.cn; 6020160105@jsnu.edu.cn; shiweipeng@jsnu.edu.cn; 2020231837@jsnu.edu.cn).

Y. Jiang is with the School of Electrical Engineering, China University of Mining and Technology, Xuzhou 221116, China (e-mail: tb25230003a41@cumt.edu.cn).

K. Li is with the Xuzhou Nanpu Electromechanical Technology Co., Ltd., Xuzhou 221116, China (e-mail: 17557930062@163.com).

Digital Object Identifier 10.24295/CPSSTPEA.2026.000011

current ripple, and enhances system reliability. To address the computational burden of vector selection in predictive control, [12] presents a ZSC hysteresis-based DV predictive current control strategy. By predicting the sector and sub-sector of the reference voltage vector, two candidate voltage vectors are selected, and a ZSV with opposite polarity to the ZSC is applied. This approach improves computational efficiency, enhances control performance, and reduces torque ripple in the motor. As algorithmic refinements to DV-MPC continue [13], this control method has shown significant improvements in control accuracy, dynamic response, and overall performance [14]–[16]. However, due to the control mechanism, the average switching frequency is typically much higher than that of conventional single-vector MPC (SV-MPC) schemes.

Optimization of dual-inverter control systems involves not only algorithmic improvements but also enhancements to system architecture. Traditional dual-inverter configurations often require an excessive number of power devices, reducing system efficiency and increasing cost. To mitigate this, [17] proposes a dual-output neutral-point-clamped (NPC) three-level topology, which eliminates four power switches compared to conventional dual-NPC configurations. By employing time-sharing modulation and virtual space vector PWM, independent dual three-level outputs are achieved. Building upon this, [18] introduces a novel 15-switch dual-output three-level topology that eliminates five power switches and six diodes, enabling the construction of dual-port voltage vectors and supporting both synchronous and asynchronous frequency control modes. To differentiate between upper and lower output ports, [19] proposes a dual-output T-type three-level topology, using sinusoidal PWM with DC bias, and analyzes key parameters such as voltage level selection, displacement angle constraints, and modulation range across various operating conditions. Although several dual-output topologies have been presented, their applicability to OEWIM systems remains limited due to the constraints of switch-sharing topologies, where the voltage at the upper output port is always greater than or equal to that at the lower port [20]–[22]. As a result, conventional per-phase wiring schemes cannot generate negative voltage outputs. Furthermore, the output states of the two ports are coupled, preventing the introduction of a phase shift via control signals, thereby restricting proper OEWIM operation.

To address these issues, this paper proposes a 120° phase-shifted dual-port drive scheme for OEWIMs based on a novel L-type dual-output three-level converter (L-DO-TLC). By employing device-sharing techniques, the proposed topology achieves independent dual three-level outputs and reduces the number of power switches from 24 to 15 compared to conventional dual-inverter structures, thereby significantly decreasing hardware costs. Based on the output characteristics of the L-DO-TLC topology, a 120° phase-shifted dual-port configuration is adopted to deliver the necessary voltage and phase differences required for OEWIM operation. The relationship between switching states and output voltage vectors in the proposed topology is derived,

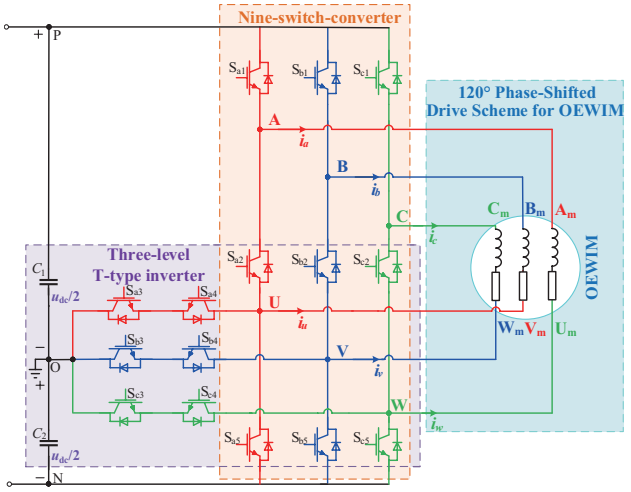

Fig. 1. Topology of L-DO-TLC driving OEWIM.

and a corresponding voltage space vector diagram is provided to establish the theoretical basis for the subsequent vector selection mechanism. To mitigate the large torque ripple associated with SV-FCS-MPC and the high switching frequency inherent in DV-MPC, a hybrid-vector MPC (HV-MPC) strategy is proposed. A voltage vector screening mechanism is designed based on the ZSC suppression principle, which substantially reduces algorithmic complexity. By combining the respective strengths of SV-MPC and DV-MPC, an alternating control mechanism is introduced to maintain current tracking accuracy while effectively suppressing torque ripple and optimizing the switching frequency.

II. Operational Principle of OEWIM Driven by L-DO-TLC

The topology of the L-DO-TLC driving the OEWIM is illustrated in Fig. 1. It comprises 15 power switches and two capacitors, C_1 and C_2. Each phase leg consists of five insulated gate bipolar transistors (IGBTs), labeled S_{x1} to S_{x5} ($x \in \{a, b, c\}$), each equipped with an anti-parallel diode. The capacitors maintain a DC bus voltage of $u_{dc}/2$. The proposed topology integrates a nine-switch converter and a T-type three-level inverter in an "L"-shaped configuration, enabling dual-port three-level output.

The voltages u_{ao}, u_{bo}, and u_{co} represent the phase voltages of nodes A, B, and C, respectively, with respect to the neutral point O, and are defined as the upper output phase voltages. Correspondingly, the currents i_a, i_b, and i_c, are the upper output currents. Similarly, the voltages u_{uo}, u_{vo}, and u_{wo} denote the phase voltages at nodes U, V, and W, respectively, with respect to point O, and are defined as the lower output phase voltages. The corresponding lower output currents are i_u, i_v, and i_w. To distinguish from the traditional OEWIM wiring configuration, the phase windings of the OEWIM are defined as AU, BV, and CW, respectively.

Compared to other dual-output three-level topologies, the L-DO-TLC utilizes a switch-sharing structure, which reduces the number of power switches, as summarized in Table I. This

TABLE I
L-DO-TLC COMPARE WITH OTHER DUAL-OUTPUT THREE-LEVEL-CONVERTER

Parameters	Dual-parallel mono-NPC-TLC	Dual-parallel mono-T-TLC	Dual-Output-NPC-TLC [17]	New-15-switches-TLC [18]	New-Dual-Output-TLC	Dual-Output-T-TLC [19]	Proposed Dual-Output-L-TLC
Switch No.	24	24	20	15	21	18	15
Clamping diode No.	12	0	12	6	0	0	0
Switch or bidirectional switch blocking U_{dc} No.	0	12	2	0	0	6	6
Switch or bidirectional switch blocking $U_{dc}/2$ No.	24	24	18	15	21	12	9

TABLE II
L-DO-TLC AU PHASE OUTPUT STATUS

State	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	u_{ao}	u_{uo}
1	OFF	ON	OFF	ON	ON	$-u_{dc}/2$	$-u_{dc}/2$
2	OFF	ON	ON	ON	OFF	0	0
3	ON	ON	ON	OFF	OFF	$u_{dc}/2$	$u_{dc}/2$
4	ON	OFF	ON	ON	OFF	$u_{dc}/2$	0
5	ON	OFF	OFF	ON	ON	$u_{dc}/2$	$-u_{dc}/2$

design offers distinct advantages in terms of both cost and physical volume.

A. Topological Analysis of the L-DO-TLC

While the L-DO-TLC employs switch-sharing to reduce the number of power devices, this structure also imposes constraints on permissible output states. Taking the AU phase leg as an example, five valid switching states are derived to ensure that the output terminals are not left floating and that the DC bus is not short-circuited. These states, listed in Table II, define the corresponding upper and lower output phase voltages, u_{ao} and u_{uo}, respectively. Notably, the output voltage always satisfies the condition that the upper phase voltage is greater than or equal to the lower phase voltage. The BV and CW bridge arms are subject to the same constraints.

The conduction state of switch S_{a3} is complementary to that of S_{a5}, i.e., $S_{a3} = \overline{S_{a5}}$, while the conduction state of S_{a4} is complementary to the series conduction of S_{a1} and S_{a2}, i.e., $S_{a4} = \overline{S_{a1} \cap S_{a2}}$. This strategy effectively reduces the switching frequency of power devices. For example, during the transition from switching state 1 to state 2, only two power switches are activated, preventing double-step voltage transitions and significantly reducing switching losses.

By analyzing the relationship between phase voltages and the switching states shown in Table II, it is observed that when phase A outputs $u_{dc}/2$, switch S_{a1} remains ON, while S_{a2} and S_{a5} are turned ON in series. Conversely, when phase U outputs $-u_{dc}/2$, S_{a5} remains ON, and S_{a1} and S_{a2} conduct in series. The conduction states of S_{a3} and S_{a4} are determined by the logic of the remaining power switches. Therefore, the relationship between the phase voltage u_{ao} and the power switches can be expressed as:

$$\begin{bmatrix} u_{ao} \\ u_{uo} \end{bmatrix} = \begin{bmatrix} S_a \\ S_u \end{bmatrix} U_{dc}/2 = \begin{bmatrix} S_{a1} - S_{a2} \cap S_{a5} \\ S_{al} \cap S_{a2} - S_{a5} \end{bmatrix} u_{dc}/2 \quad (1)$$

Since the conduction strategies for the BV and CW bridge arms are identical to those for the AU bridge arm, the relationships between the phase voltages and corresponding switches for these arms can similarly be expressed as:

$$\begin{bmatrix} u_{bo} \\ u_{vo} \\ u_{co} \\ u_{wo} \end{bmatrix} = \begin{bmatrix} S_b \\ S_v \\ S_c \\ S_w \end{bmatrix} U_{dc}/2 = \begin{bmatrix} S_{b1} - S_{b2} \cap S_{b5} \\ S_{bl} \cap S_{b2} - S_{b5} \\ S_{c1} - S_{c2} \cap S_{c5} \\ S_{cl} \cap S_{c2} - S_{c5} \end{bmatrix} u_{dc}/2 \quad (2)$$

Furthermore, the voltage and current stresses on the power devices serve as critical indicators for evaluating the proposed topology. Regarding the voltage stress, the blocking voltages are determined by the clamping mechanism of the DC bus capacitors and the complementary conduction logic. Specifically, the switches S_{a3} and S_{a4} sustain a maximum blocking voltage of $U_{dc}/2$, whereas the switches S_{a1}, S_{a2}, and S_{a5} are subjected to a maximum voltage stress of U_{dc}. In terms of current stress, owing to the dual-port series connection configuration, the current flowing through each active switch corresponds directly to the stator phase current of the OEWIM. Crucially, despite the switch-sharing structure, the specific switching logic ensures that no single device carries superimposed currents from multiple phases, thereby maintaining the current stress within the rated limits.

B. Reference Current Generation Mechanism

When the L-DO-TLC drives an OEWIM using a conventional dual-inverter configuration, in which each phase output port is directly connected, the switch-sharing structure imposes a constraint whereby the upper port voltage is always greater than or equal to the lower port voltage. Furthermore, the output states of the two ports are inherently coupled, preventing the introduction of a phase shift via control signals. To overcome this limitation under same-frequency operation, a dual-port

TABLE III
AW PHASE OUTPUT STATUS OF L-DO-TLC OEWIM

Output state	u_{ao}	u_{wo}	u_{aw}
I	$u_{dc}/2$	$-u_{dc}/2$	u_{dc}
II	0	$-u_{dc}/2$	$u_{dc}/2$
III	$u_{dc}/2$	0	$u_{dc}/2$
IV	$-u_{dc}/2$	$-u_{dc}/2$	0
V	0	0	0
VI	$u_{dc}/2$	$u_{dc}/2$	0
VII	0	$u_{dc}/2$	$-u_{dc}/2$
VIII	$-u_{dc}/2$	0	$-u_{dc}/2$
IX	$-u_{dc}/2$	$u_{dc}/2$	$-u_{dc}$

120° phase-shifted connection scheme is proposed for OEWIM operation, as illustrated in Fig. 1.

In this scheme, the upper output current i_a flows from node A through the single-phase winding AU and exits at node W, while the lower output current is i_w=−i_a. Similarly, the upper output current i_b flows from node B through winding BV to node U, yielding i_u=−i_b. For phase C, the upper output current i_c flows from node C through winding CW to node V, resulting in a lower output current of i_v=−i_c. Consequently, nodes AW, BU, and CV are directly connected via the OEWIM, and the windings form a 120° phase-shifted connection at both ends. The voltages across the phase-shifted windings are determined by the differences between the upper and lower phase voltages:

$$\begin{cases} u_{aw} = u_{ao} - u_{wo} \\ u_{bu} = u_{bo} - u_{uo} \\ u_{cv} = u_{co} - u_{vo} \end{cases} \tag{3}$$

Taking the single-phase winding voltage u_{aw} as an example, both the upper and lower phase voltages, u_{ao} and u_{wo}, exhibit three-level outputs corresponding to five distinct switching states for each phase. As a result, the single-phase winding voltage u_{aw} can attain nine possible output levels and 25 distinct switching combinations, as summarized in Table III.

In the OEWIM drive system, each phase winding is energized by an upper and a lower output terminal, yielding nine output voltage combinations and 25 distinct switching states. Due to the 120° phase-shifted connection method, the phase voltage is unaffected by the voltages from the upper and lower terminals of the same phase. This configuration enables the phase voltage output to achieve five discrete levels. Consequently, the output waveform quality is improved, allowing each phase winding to realize five switching states: $\pm u_{dc}$, $\pm u_{dc}/2$, and 0.

III. PREDICTIVE MODELING AND VECTOR SELECTION MECHANISM FOR OEWIM DRIVEN BY L-DO-TLC

A. Mathematical Model of OEWIM

Based on the analysis of the output voltage states across the single-phase windings of the OEWIM, a dynamic mathematical model is established in the *dq* reference frame aligned with the rotor flux:

$$\begin{cases} \dfrac{\mathrm{d}\psi_{rd}}{\mathrm{d}t} = -\dfrac{1}{T_r}\psi_{rd} + \dfrac{L_m}{T_r} i_{sd} \\ \dfrac{\mathrm{d}i_{sd}}{\mathrm{d}t} = \dfrac{k_r}{\delta L_r T_r}\psi_{rd} - \dfrac{r_o}{\delta L_s} i_{sd} + \omega_e i_{sq} + \dfrac{1}{\delta L_s} u_{sd} \\ \dfrac{\mathrm{d}i_{sq}}{\mathrm{d}t} = -\dfrac{n_p k_r \omega}{\delta L_r}\psi_{rd} - \dfrac{r_o}{\delta L_s} i_{sq} - \omega_e i_{sd} + \dfrac{1}{\delta L_s} u_{sd} \end{cases} \tag{4}$$

In the above equations, i_{sd} and i_{sq} denote the stator currents along the *d*- and *q*-axis, respectively, while u_{sd} and u_{sq} represent the corresponding stator voltages. ψ_{rd} is the *d*-axis rotor flux linkage. R_s and R_r are the stator and rotor resistances, while L_s and L_r are the stator and rotor inductances, respectively. L_m denotes the mutual inductance. ω_e and ω represent the synchronous and rotor angular velocities, respectively, and n_p is the number of pole pairs. Additional parameter definitions include: $T_r = L_r / R_r$ as the rotor electromagnetic time constant. $k_r = L_m / L_r$, $r_o = R_s + R_r \times k_r^2$, and $\delta = 1 - L_m^2 / (L_s \times L_r)$.

To discretize the flux and current expressions in (4), the forward Euler method is applied. This yields the flux and current prediction models in the *dq* reference frame as:

$$\begin{cases} \psi_{rd}^{k+1} = (1 - \dfrac{T_s}{T_r})\psi_{rd}^{k} + \dfrac{L_m T_s}{T_r} i_{sd}^{k} \\ i_{sd}^{k+1} = (1 - \dfrac{T_s r_o}{\delta L_s}) i_{sd}^{k} + \dfrac{T_s k_r}{\delta L_r T_r}\psi_{rd}^{k} + T_s \omega_e i_{sq}^{k} + \dfrac{T_s}{\delta L_s} u_{sd}^{k} \\ i_{sq}^{k+1} = (1 - \dfrac{T_s r_o}{\delta L_s}) i_{sq}^{k} - \dfrac{T_s n_p k_r \omega}{\delta L_r}\psi_{rd}^{k} - T_s \omega_e i_{sd}^{k} + \dfrac{T_s}{\delta L_s} u_{sd}^{k} \end{cases} \tag{5}$$

To improve current tracking performance, delay compensation is introduced using a second-order Lagrange extrapolation method:

$$\begin{cases} i^{*k+1} = 3i^{*k} - 3i^{*k-1} + i^{*k-2} \\ i^{*k+2} = 3i^{*k+1} - 3i^{*k} + i^{*k-1} \end{cases} \tag{6}$$

Here, i^{*t} where $t \in \{k+2, k+1, k, k-1, k-2\}$ denotes the current values at different time steps. To maintain prediction accuracy, delay compensation for the rotor flux linkage is also implemented:

$$\psi_{rd}^{k+2} = (1 - \frac{T_s}{T_r})\psi_{rd}^{k+1} + \frac{L_m T_s}{T_r} i_{sd}^{k+1} \tag{7}$$

B. Establishment of Voltage Space Vectors in the OEWIM Drive System

In the *dq* reference frame, the stator voltage of the OEWIM is derived based on the relationship between the L-DO-TLC output phase voltages and the corresponding power switch

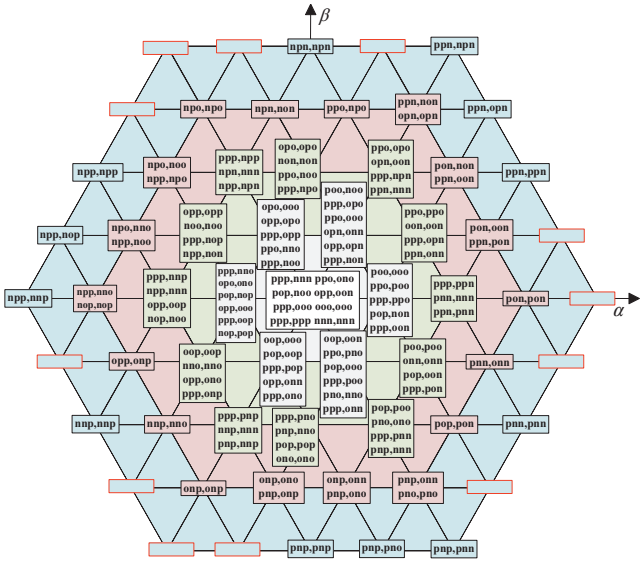

Fig. 2. Voltage space vector of L-DO-TLC OEWIM.

states, as well as the inter-phase voltages of the OEWIM windings. The functional relationship between the OEWIM's three-phase winding voltages at time k and the switching states of the L-DO-TLC is expressed as:

$$\begin{bmatrix} u_{\mathrm{aw}}^{k} \\ u_{\mathrm{bu}}^{k} \\ u_{\mathrm{cv}}^{k} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{ao}}^{k} - u_{\mathrm{wo}}^{k} \\ u_{\mathrm{bo}}^{k} - u_{\mathrm{uo}}^{k} \\ u_{\mathrm{co}}^{k} - u_{\mathrm{vo}}^{k} \end{bmatrix} = \begin{bmatrix} S_{\mathrm{a}}^{k} - S_{\mathrm{w}}^{k} \\ S_{\mathrm{b}}^{k} - S_{\mathrm{u}}^{k} \\ S_{\mathrm{c}}^{k} - S_{\mathrm{v}}^{k} \end{bmatrix} u_{\mathrm{dc}} / 2 \tag{8}$$

By applying the standard transformation matrix from the three-phase stationary reference frame to the dq reference frame, the OEWIM stator voltage is expressed as:

$$\begin{bmatrix} u_{sd}^{k} \\ u_{sq}^{k} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2}{3}\pi\right) & \cos\left(\theta + \frac{2}{3}\pi\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2}{3}\pi\right) & -\sin\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} \begin{bmatrix} u_{\mathrm{aw}}^{k} \\ u_{\mathrm{bu}}^{k} \\ u_{\mathrm{cv}}^{k} \end{bmatrix} \tag{9}$$

where θ denotes the electrical angle of the rotor. To enable a more intuitive representation of the relationship between the three-phase output voltages and the switching states of the L-DO-TLC, the voltage space vector of the OEWIM drive system is established as:

$$\begin{aligned} V &= \frac{2}{3}\left(u_{\mathrm{aw}} + u_{\mathrm{bu}} e^{j\frac{2\pi}{3}} + u_{\mathrm{cv}} e^{j\frac{4\pi}{3}}\right) \\ &= \frac{2}{3}\left[\frac{1}{2}(2u_{\mathrm{aw}} - u_{\mathrm{bu}} - u_{\mathrm{cv}}) + \frac{\sqrt{3}}{2} j(u_{\mathrm{bu}} - u_{\mathrm{cv}})\right] \end{aligned} \tag{10}$$

By substituting (3) into the space vector formulation, the voltage space vector diagram shown in Fig. 2 is obtained. Each phase-leg of the L-DO-TLC can generate five distinct switching states, resulting in 125 possible switching combinations for the three-phase windings of the OEWIM. However, due to switching redundancy, only 49 unique voltage space vectors are ultimately produced.

The voltage space vector diagram of the OEWIM driven by the L-DO-TLC resembles that of a five-level inverter. However, owing to the switch-reuse topology employed in the L-DO-TLC, the upper output phase voltage is always greater than or equal to the lower output phase voltage. As a result, certain outer voltage vectors are absent from the diagram. In the two-phase stationary reference frame, the numerals within the circles represent the upper output phase voltages u_{ao}, u_{bo}, u_{co} and the lower output phase voltages u_{uo}, u_{vo}, u_{wo}, respectively. The notations p, o, and n correspond to output voltage levels of $-u_{\mathrm{dc}}/2$, 0, $u_{\mathrm{dc}}/2$, respectively.

C. Vector Selection Strategy Based on Zero-Sequence Voltage Suppression

During the steady-state operation of the OEWIM, the presence of ZSV results in an uneven distribution of phase-to-ground or inter-phase voltages, which may compromise motor insulation. Therefore, suppression of ZSV is considered a key control objective.

For the L-DO-TLC, the common-mode voltages generated at the upper and lower outputs, denoted as U_{com1} and U_{com2}, are defined as follows:

$$\begin{cases} U_{\mathrm{com1}} = \dfrac{u_{\mathrm{ao}} + u_{\mathrm{bo}} + u_{\mathrm{co}}}{3} \\ U_{\mathrm{com2}} = \dfrac{u_{\mathrm{uo}} + u_{\mathrm{vo}} + u_{\mathrm{wo}}}{3} \end{cases} \tag{11}$$

Accordingly, the ZSV between the OEWIM windings is expressed as:

$$U_{\mathrm{ZSV}} = \frac{u_{\mathrm{ao}} + u_{\mathrm{bo}} + u_{\mathrm{co}}}{6} - \frac{u_{\mathrm{uo}} + u_{\mathrm{vo}} + u_{\mathrm{wo}}}{6} \tag{12}$$

By substituting the 125 switching vectors from the modulation region shown in Fig. 2 into (11) and (12), the common-mode voltages at the upper and lower outputs, as well as the resulting ZSV across the OEWIM windings, are obtained and summarized in Table IV.

The common-mode voltages at both the upper and lower outputs lie within the range $[-u_{\mathrm{dc}}/2, u_{\mathrm{dc}}/2]$. However, due to the switch-sharing topology of the L-DO-TLC, the ZSV across the OEWIM windings remains strictly positive. To simplify the control algorithm and mitigate the negative impact of ZSV, all of the voltage vectors associated with non-zero ZSV are excluded. From the remaining set, 27 candidate vectors are selected for further evaluation. Their corresponding voltage space vectors are shown in Fig. 3. By restricting the optimization space to these specific 27 vectors, ZSV excitation

TABLE IV
COMMON VOLTAGE

Space voltage	Common voltage		ZSV
	U_{com1}	U_{com2}	U_{ZSV}
ppp,nnn	$u_{dc}/2$	$-u_{dc}/2$	u_{dc}
ppp,non ppp,onn ppp,nno	$u_{dc}/2$	$-u_{dc}/3$	$5u_{dc}/6$
pop,non ppo,nno opp,onn	$u_{dc}/3$	$-u_{dc}/3$	$2u_{dc}/3$
ppn,nnn pnp,nnn npp,nnn	$u_{dc}/6$	$-u_{dc}/2$	$2u_{dc}/3$
ppp,nop ppp,opn ppp,pno ppp,pon ppp,npo ppp,onp ppp,ooo	$u_{dc}/2$	0	$u_{dc}/2$
ppo,noo opp,ono opp,ono pop,oon pop,noo opp,oon	$u_{dc}/3$	$-u_{dc}/6$	$u_{dc}/2$
npp,non ppn,onn ppn,non pnp,onn npp,nno pnp,nno	$u_{dc}/6$	$-u_{dc}/3$	$u_{dc}/2$
ppp,npp ppp,pnp ppp,ppn ppp,opo ppp,poo ppp,oop	$u_{dc}/2$	$u_{dc}/6$	$u_{dc}/3$
poo,noo oop,oon opo,ono ppn,pnn ppn,npn npp,npn pnp,nnp npp,noo ppn,oon pnp,ono pnp,pnn	$u_{dc}/6$	$-u_{dc}/6$	$u_{dc}/3$
opn,onn pno,nno pon,non onp,onn npo,nno nop,non	0	$-u_{dc}/3$	$u_{dc}/3$
pnn,nnn npn,nnn nnp,nnn	$-u_{dc}/6$	$-u_{dc}/2$	$u_{dc}/3$
ppp,ppo ppp,opp ppp,pop	$u_{dc}/2$	$u_{dc}/3$	$u_{dc}/6$
opp,oop ppo,opo pop,poo ppo,poo opp,opo pop,oop	$u_{dc}/3$	$u_{dc}/6$	$u_{dc}/6$
pop,pon ppo,npo opp,onp pop,nop ppo,ooo pop,ooo opp,ooo opp,opn ppo,pno	$u_{dc}/3$	0	$u_{dc}/6$
ppp,nnp ppp,npn ppp,pnn ppp,oon ppp,noo ppp,ono	$u_{dc}/2$	$-u_{dc}/6$	$u_{dc}/6$
poo,ooo opo,ooo oop,ooo npp,nop ppn,pon pnp,onp npp,npo ppn,opn pnp,pno	$u_{dc}/6$	0	$u_{dc}/6$
opn,oon pno,ono nop,noo pon,oon onp,ono npo,noo	0	$-u_{dc}/6$	$u_{dc}/6$
pnn,onn npn,non nnp,nno	$-u_{dc}/6$	$-u_{dc}/3$	$u_{dc}/6$
ppp,ppp	$u_{dc}/2$	$u_{dc}/2$	0
pop,pop opp,opp ppo,ppo	$u_{dc}/3$	$u_{dc}/3$	0
opo,opo oop,oop poo,poo npp,npp ppn,ppn pnp,pnp	$u_{dc}/6$	$u_{dc}/6$	0
ooo,ooo pon,pon opn,opn pno,pno npo,npo onp,onp nop,nop	0	0	0
oon,oon ono,ono noo,noo npn,npn nnp,nnp pnn,pnn	$-u_{dc}/6$	$-u_{dc}/6$	0
onn,onn non,non nno,nno	$-u_{dc}/3$	$-u_{dc}/3$	0
nnn,nnn	$-u_{dc}/2$	$-u_{dc}/2$	0

is eliminated at the topological source. This inherent constraint ensures effective ZSC suppression.

Current tracking performance is a critical indicator for assessing the effectiveness of the OEWIM control strategy. SV-MPC based on the principle of minimizing the current tracking error, the optimal current tracking evaluation function g^k is defined as:

$$g^k = \left|i_{sd}^{*k+1} - i_{sd}^{k+2}\right| + \left|i_{sq}^{*k+1} - i_{sq}^{k+2}\right| \tag{13}$$

It is worth noting that in practical applications, inverter non-linearities, such as dead-time effects and on-state voltage drops, inevitably introduce disturbance voltages, acting as a source of ZSC. However, the proposed HV-MPC strategy relies on the closed-loop feedback of measured stator currents, where the effects of these nonlinearities are naturally reflected.

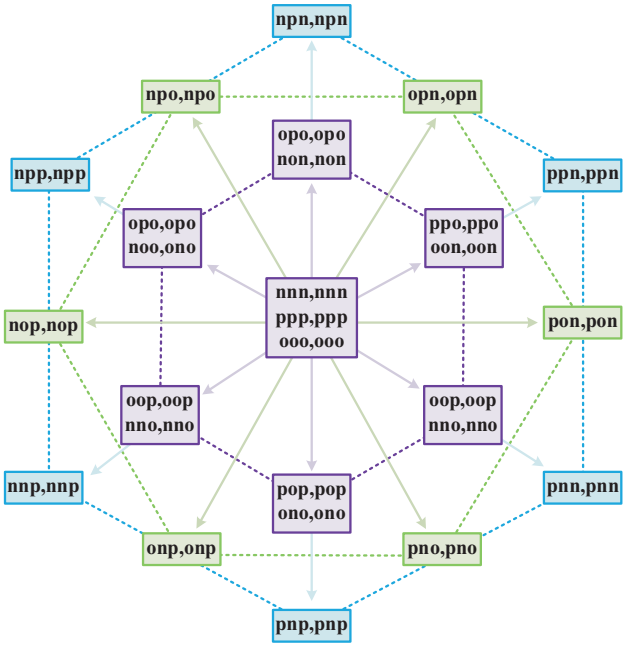

Fig. 3. Voltage vector for satisfactory common-mode voltage.

Through the optimization mechanism of the cost function, the algorithm automatically selects voltage vectors to counteract these disturbances, thereby demonstrating inherent robustness against inverter nonlinearities.

IV. HV-MPC-BASED CONTROL

Conventional DV-MPC generates both an optimal and a suboptimal voltage vector within each control cycle. While this improves control performance relative to SV-MPC, it leads to higher switching frequencies and increased computational load. Conversely, SV-MPC using only one vector per cycle tends to result in significant torque ripple. To address these limitations, an HV-MPC strategy is proposed. By comparing current tracking performance under globally optimized single- and double-vector conditions, the optimal voltage vector combination is selected based on a minimum cost function criterion. This approach reduces switching frequency and computational complexity while maintaining dynamic performance.

In the proposed HV-MPC operating under DV mode, the first voltage vector is fixed as the vector applied at the end of the previous control cycle, while the second is selected to suppress the ZSV.

As shown in Fig. 4, the dynamic operation is divided into discrete sampling intervals, where the period from t_{k-1} to t_k represents the previous control cycle and t_k to t_{k+1} the current cycle. Candidate vectors for the current cycle t_k are derived based on the optimal vector S_{old} from the preceding cycle, ensuring a consistent starting point for the optimization process.

Three possible voltage vector transition strategies are evaluated within the current cycle. In conventional DV-MPC, when the optimal vector for t_k differs from S_{old}, two additional switching actions are incurred at the cycle boundary, leading to increased switching frequency and power losses. In contrast,

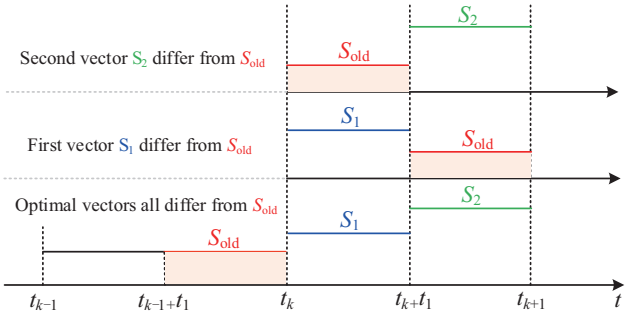

Fig. 4. Switching Vector Selection.

the proposed strategy retains S_{old} as the first vector of the current sequence. This logical constraint ensures continuity of the switching state at the cycle transition, ensuring that only a single vector transition occurs at the sub-cycle boundaries. This approach effectively eliminates redundant switching actions and reduces the average switching frequency from the perspective of topological constraints.

Under SV-MPC mode in HV-MPC, voltage vector optimization is limited to vectors satisfying the ZSV suppression criterion. At the beginning of each control cycle, the *d-q* axis current sampling values are first updated and the cost function values are initialized, followed by a parallel evaluation loop for the 27 candidate vectors.

Step 1: In SV-MPC mode, the algorithm calculates the current prediction error for each candidate vector when applied over the entire cycle, thereby selecting the optimal current-tracking vector V_{opt} and storing its corresponding optimal cost g_{opt}.

Step 2: In the improved DV-MPC mode, the algorithm fixes the first sequence vector as S_{old} and dynamically allocates the duty cycles t_1 and t_2 based on the ratio of the prediction errors produced by the respective candidate vectors.

Step 3: The comprehensive cost values g_{opt} and f_{opt} are compared in real time to determine the optimal execution scheme.If the tracking accuracy of the single-vector mode meets or exceeds the current control requirements, the system gives priority to the single-vector output to further suppress unnecessary switching actions. This dynamic adjustment mechanism achieves an effective balance between control accuracy and operational efficiency.

The application times t_1 and t_2 for hybrid vectors V_{opt1} and V_{opt2} are computed based on f_1^k and f_2^k . The greater the value of f_1^k (or f_2^k), the shorter the corresponding application time t_1 (or t_2) within the control cycle:

$$\begin{cases} t_1 = \dfrac{f_2^k}{f_1^k + f_2^k} T_s \\ t_2 = \dfrac{f_1^k}{f_1^k + f_2^k} T_s \end{cases} \tag{14}$$

The overall HV-MPC decision-making process is illustrated in Fig. 5. The evaluation function f_k for current tracking under DV mode is given as:

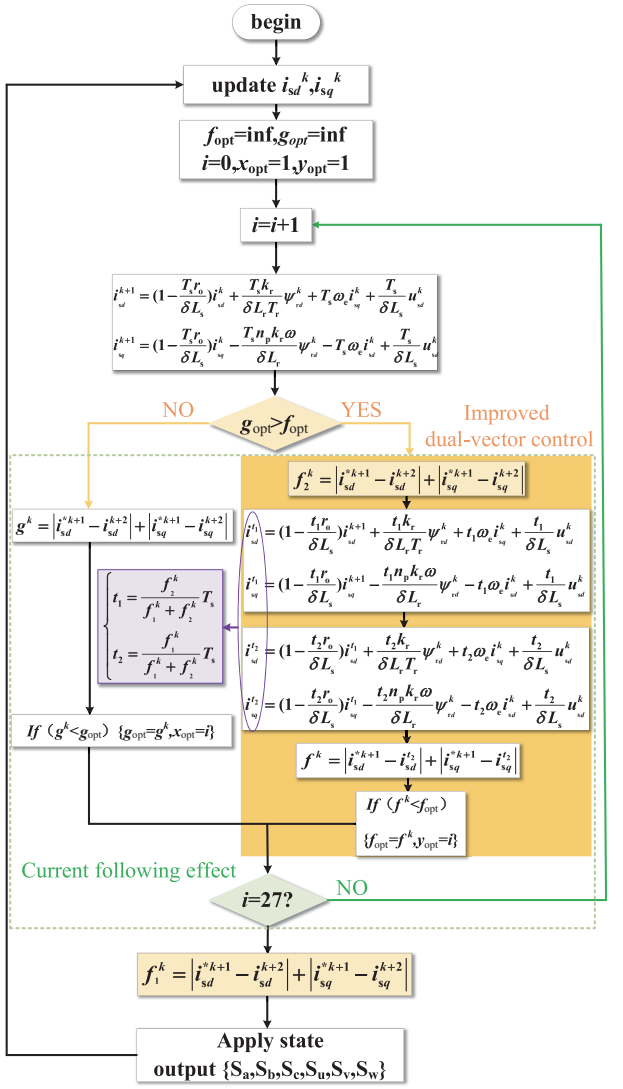

Fig. 5. Layered optimization flowchart.

$$f^k = \left|i_{sd}^{*k+1} - i_{sd}^{t_2}\right| + \left|i_{sq}^{*k+2} - i_{sq}^{t_2}\right| \tag{15}$$

The predicted current values i_{sd}^{t2} and i_{sq}^{t2} depend on the selected voltage vectors at instants t_1 and t_2. The complete control block diagram of the L-DO-TLC driven OEWIM system is presented in Fig. 6.

V. Simulation and Experimentation

A. Simulation Analysis

To verify the feasibility of the proposed L-DO-TLC dual-port 120°-shifted drive scheme for OEWIM and to assess the effectiveness of the HV-MPC strategy in reducing torque ripple and switching frequency, both simulation and experimental evaluations were conducted. The simulations were performed in MATLAB/Simulink and hardware-in-the-loop (HIL) validation was carried out using a platform comprising DSP, FPGA, and the Typhoon HIL402. The simulation parameters for

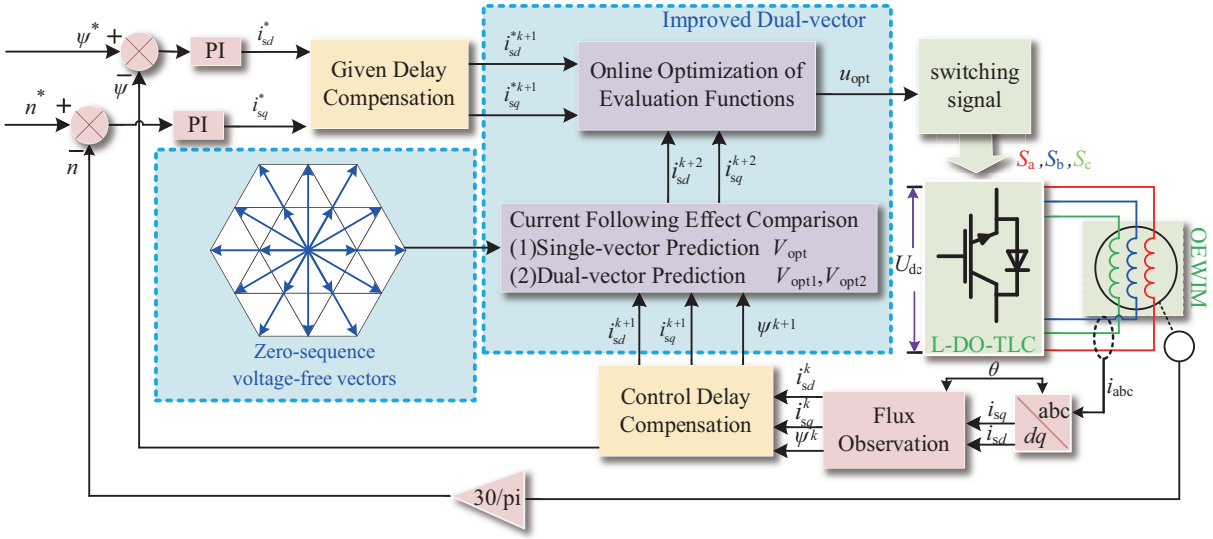

Fig. 6. L-DO-TLC drive OEWIM system control block diagram.

TABLE V
SIMULATION PARAMETERS OF OEWIM

Parameters	Numerical Value
Rated voltage	380 V
Rated current	12.1 A
Rated power	5.5 kW
Rated speed	1450 r/min
Rated torque	36.2 N·m
Number of pole pairs	2
Stator resistance	1.91 Ω
Rotor resistance	1.45 Ω
Stator inductance	0.249 H
Rotor inductance	0.249 H
Mutual inductance	0.225 H
Rated rotor flux	0.98 Wb

the OEWIM are listed in Table V, with a DC-side voltage of $u_{dc}/2$=400 V and a sampling frequency of 10 kHz.

Under normal operating conditions (n=1450 r/min), the feasibility of the topology and the effectiveness of ZSV suppression were verified using the proposed L-DO-TLC dual-port 120°-shifted drive. As shown in Fig. 7, the three-phase output current i_{abc} is distorted when optimization includes all 125 voltage vectors, without eliminating non-zero ZSV vectors. In particular, phase current i_c is shifted downward due to the presence of ZSC, resulting in current imbalance.

When the optimization range is limited to 27 voltage vectors with zero ZSV, the output three-phase currents i_{abc} maintain a stable amplitude of 5 A, as shown in Fig. 8. However, because SV-MPC selects only one optimal voltage vector per control cycle, discretization errors remain in the output waveform, leading to observable current ripple.

After ZSC suppression, the current tracking performance for phase A under SV-MPC is shown in Fig. 9. A maximum

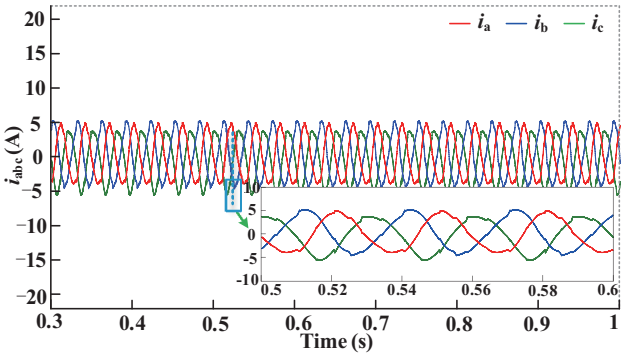

Fig. 7. The output three-phase currents i_{abc} without ZSC suppression.

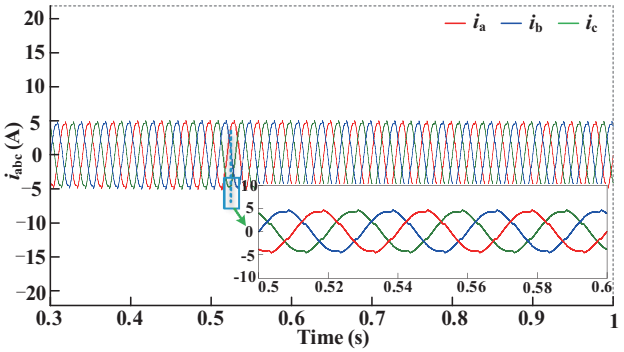

Fig. 8. The output three-phase currents i_{abc} with ZSC suppression.

current deviation of ΔI_{max}=1A is observed between the reference current i_{a_ref} and the actual current i_a. The actual electromagnetic torque T_e and the reference load torque T_L during steady-state operation are depicted in Fig. 10, showing a maximum torque fluctuation of ΔT_e=3.9 N·m.

The speed tracking performance under SV-MPC at a reference speed of n=1450 r/min is presented in Fig. 11. The response time to reach steady-state speed is T_r=0.21 s, with a speed ripple of Δn=0.5 r/min. In summary, the proposed L-DO-TLC dual-port 120°-shifted drive, with ZSV suppression,

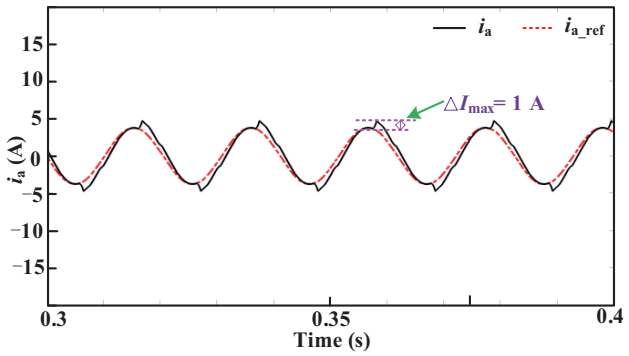

Fig. 9. The current tracking effect of phase A under SV-MPC.

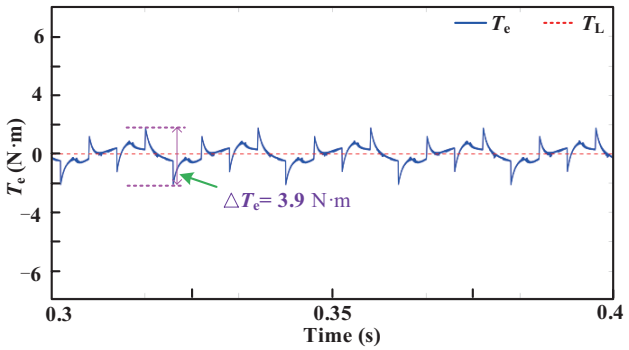

Fig. 10. Comparison between output load torque and actual torque.

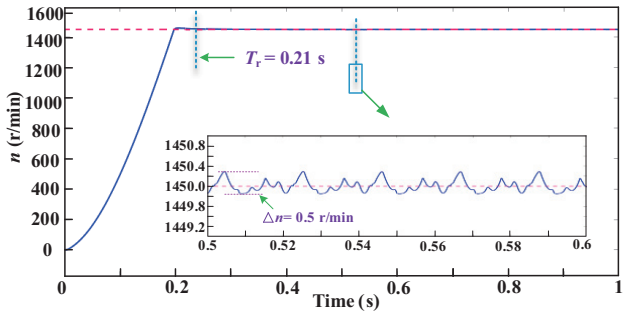

Fig. 11. SV-MPC output speed tracking effect.

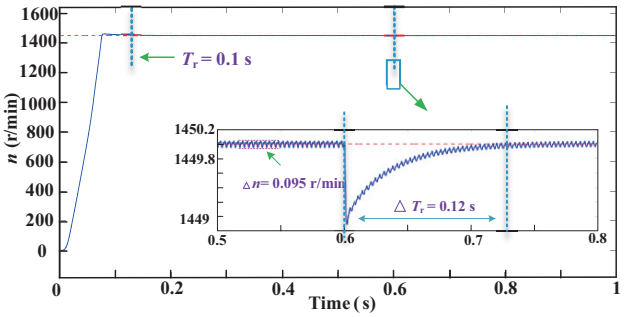

Fig. 12. HV-MPC output speed tracking effect.

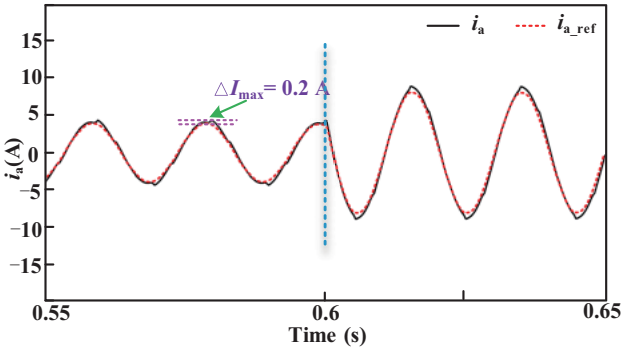

Fig. 13. The current tracking effect of phase A under HV-MPC.

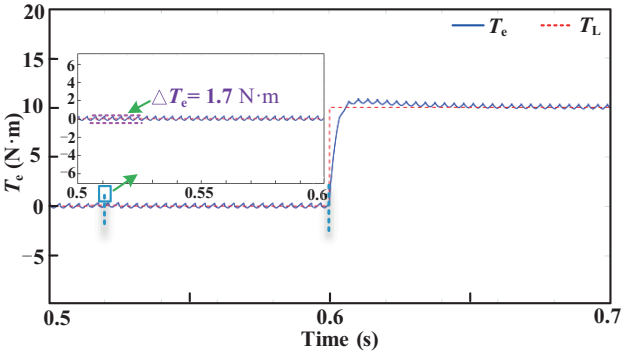

Fig. 14. Comparison between output load torque and actual torque.

effectively mitigates the influence of ZSC while ensuring stable and efficient motor operation. This demonstrates its viability as a simplified alternative to traditional dual-inverter OEWIM systems.

To evaluate the HV-MPC strategy, a load torque of 20 N·m was applied at t=0.6 s. As shown in Fig. 12, under HV-MPC, the system reaches the steady-state speed is T_r=0.1 s, with a speed ripple of Δn=0.095 r/min, which is nearly negligible. Compared to SV-MPC, HV-MPC reduces both response time and torque ripple. After applying the load torque, the response time to regain stability is ΔT_r=0.12 s, and torque fluctuations remain minimal.

The current tracking performance of phase A under HV-MPC is shown in Fig. 13. The maximum current deviation is ΔI_{max}=0.2 A. As illustrated in Fig. 14, the actual and reference torques exhibit a reduced maximum fluctuation of ΔT_e=1.7 N·m. Following load application, the output current and torque remain stable.

To assess the dynamic performance of the system under different control strategies, the response characteristics of SV-MPC under abrupt speed variation conditions were analyzed. As illustrated in Fig. 15, particular emphasis was placed on the acceleration and deceleration response times under this control strategy. The initial rotational speed was set to 1200 r/min. At t = 0.4 s, an acceleration command was applied, with the target speed stepping up to 1450 r/min. The measured rise time was T_{r_u} = 0.1 s. Subsequently, at t = 0.8 s, a deceleration command was issued, reducing the target speed to 800 r/min. The recorded settling time during this braking phase was T_{r_d} = 0.12 s, which is slightly longer than the rise time, indicating a marginally slower dynamic response in the deceleration process.

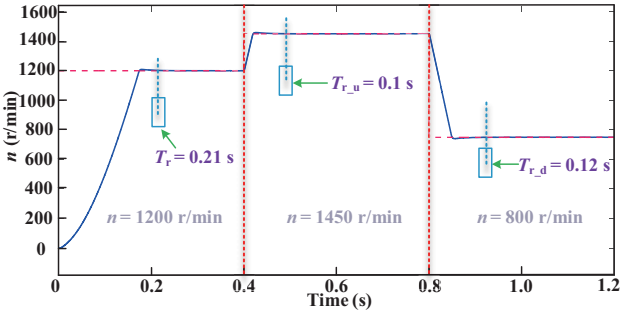

Fig. 15. SV-MPC acceleration/deceleration response time.

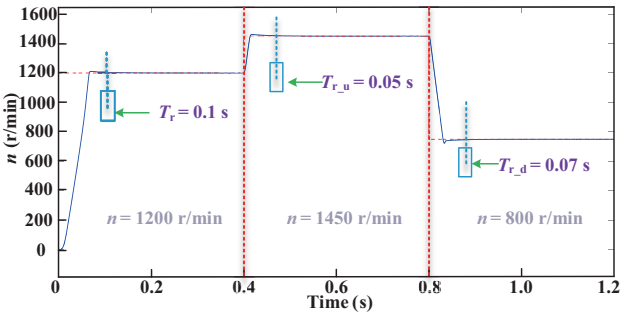

Fig. 16. HV-MPC acceleration/deceleration response time.

In comparison to the SV-MPC strategy, the HV-MPC strategy exhibits markedly superior transient performance, as quantitatively demonstrated by its dynamic response metrics. As illustrated in Fig. 16, under an acceleration command applied at t = 0.4 s, with the target speed stepping up to 1450 r/min, the measured rise time T_{r_u} = 0.05 s. Similarly, when a deceleration command is initiated at t = 0.8 s, reducing the target speed to 800 r/min, the resulting settling time T_{r_d} = 0.07 s. These values represent a substantial reduction in response time relative to the SV-MPC strategy, confirming enhanced dynamic performance during both operational phases. The improved transient characteristics underscore the efficacy of the HV-MPC approach in achieving rapid and precise speed regulation under demanding conditions.

In summary, when comparing the current tracking effectiveness of DV-MPC and SV-MPC, the HV-MPC strategy offers reduced current and torque ripple, which are characteristics comparable to DV-MPC, thereby enhancing overall system stability.

B. Experimental Result Analysis

To validate the effectiveness of the proposed control strategy, a hardware-in-the-loop (HIL) experimental platform was constructed, as shown in Fig. 17. This setup was used to verify the HV-MPC method applied to the L-DO-TLC-driven OEWIM. The main circuit model was implemented on the Typhoon HIL402 platform, and output pulses were generated by the HDSP-DF28335P controller. Experimental parameters were consistent with those used in the simulation section.

The output current waveforms and current tracking performance in the *dq* coordinate system under different control strategies are presented in Figs. 18–20. As shown in Fig. 18, the SV-MPC-controlled output exhibits low waveform quality, with significant fluctuations between the actual currents i_{sd}, i_{sq} and their reference values i_{sd_ref} and i_{sq_ref}. Additionally, the corresponding FFT analysis reveals a high THD of 7.34% with significant high-frequency switching noise and pronounced low-frequency harmonic amplitudes, which lead to severe waveform distortion and degraded power quality. This quantitatively confirms the poor sinusoidal quality and substantial current ripple.

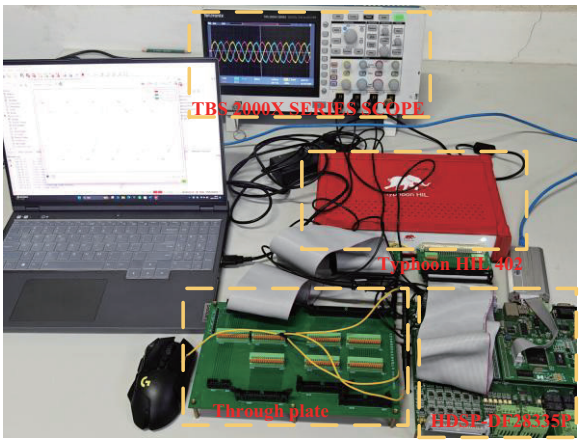

Fig. 17. Hardware-in-the-loop experimental platform.

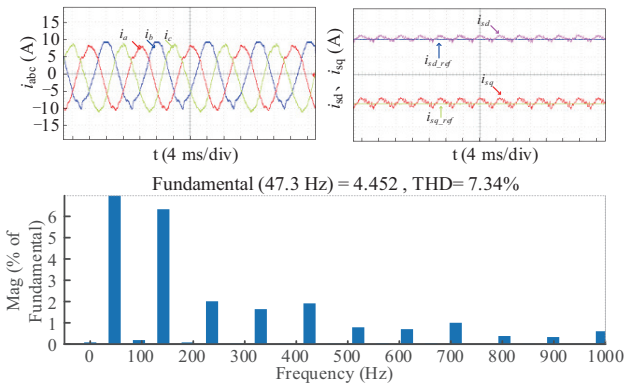

Fig. 18. Experimental current waveforms and FFT analysis of SV-MPC.

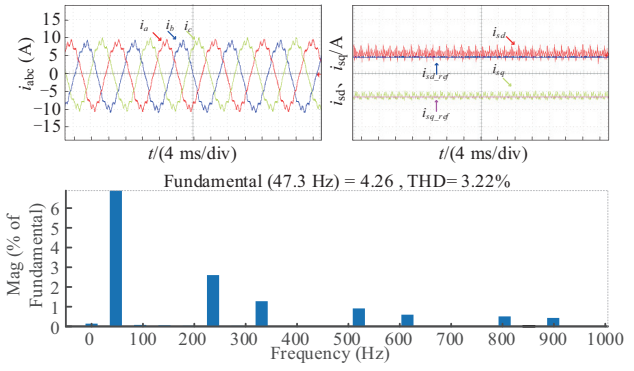

Fig. 19. Experimental current waveforms and FFT analysis of DV-MPC.

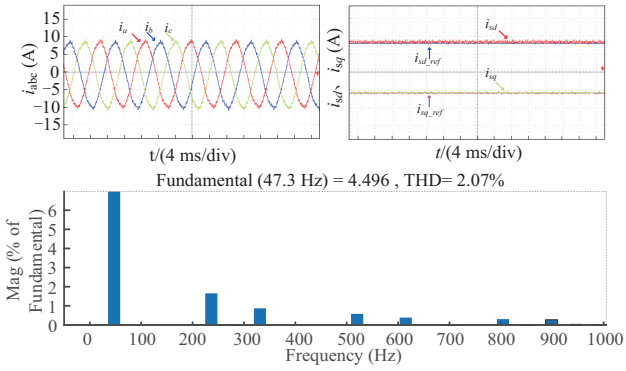

Fig. 20. Experimental current waveforms and FFT analysis of HV-MPC.

In contrast, the waveform under DV-MPC, shown in Fig. 19, demonstrates improved three-phase current quality compared to SV-MPC. However, the increase in switching frequency results in a higher current ripple frequency in the *dq* frame, with some residual fluctuations. Nonetheless, the amplitude of these fluctuations is lower than that observed in SV-MPC. In contrast, the current waveforms under DV-MPC demonstrate improved quality with a reduced THD of 3.22%. Due to the dual-vector synthesis, the high-frequency switching noise is effectively suppressed while attenuating the major harmonic components, which contributes to an enhanced current waveform quality. However, the limited voltage vector space under the L-DO-TLC topology constraints leads to residual low-frequency harmonics, which become more prominent in the time-domain waveforms. Nonetheless, the amplitude of these fluctuations is lower than that in SV-MPC.

Under HV-MPC control, the waveform shown in Fig. 20 exhibits superior sinusoidal quality compared to both DV-MPC and SV-MPC, achieving a THD of 2.07%. The amplitude of current ripple in the *dq* frame is substantially reduced, and the corresponding FFT analysis reveals that both high-frequency switching noise and low-frequency harmonics are effectively suppressed, which confirms the effectiveness of the proposed HV-MPC in enhancing the steady-state performance of L-DO-TLC-driven OEWIM systems.

To assess the dynamic performance of the three vector control strategies, experimental results under a sudden load torque change are presented in Fig. 21. The torque waveforms under SV-MPC, DV-MPC, and HV-MPC are shown respectively. Fig. 21(a) depicts the torque response of SV-MPC under a step torque load of 10 N·m. A relatively large torque ripple ΔT_e is observed before and after the disturbance. By comparison, torque ripples under DV-MPC and HV-MPC are significantly reduced. Notably, HV-MPC demonstrates the smallest ripple amplitude, validating its superiority in mitigating excessive torque ripple common in SV-MPC schemes.

To evaluate the switching losses under different control strategies, the switching frequencies under various given speeds and load torques are compared. The switching frequency calculation involves extracting the drive signals of the switching devices from the simulation results. By detecting

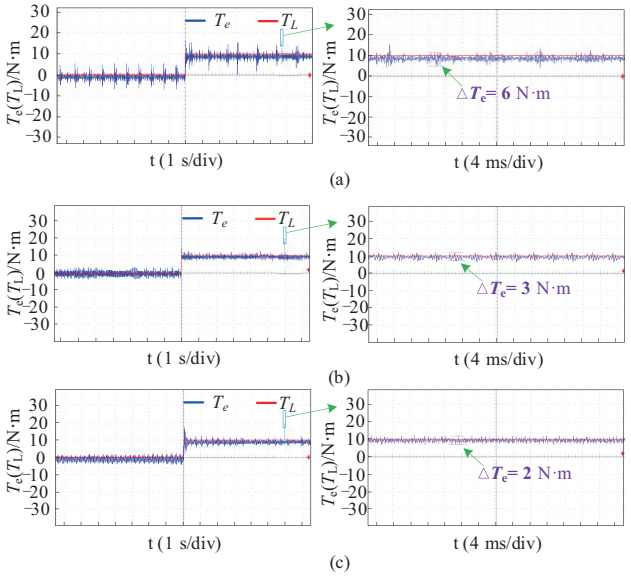

Fig. 21. Dynamic response effect of different control strategies. (a) Single-vector. (b) Dual-vector. (c) Mixed-vector.

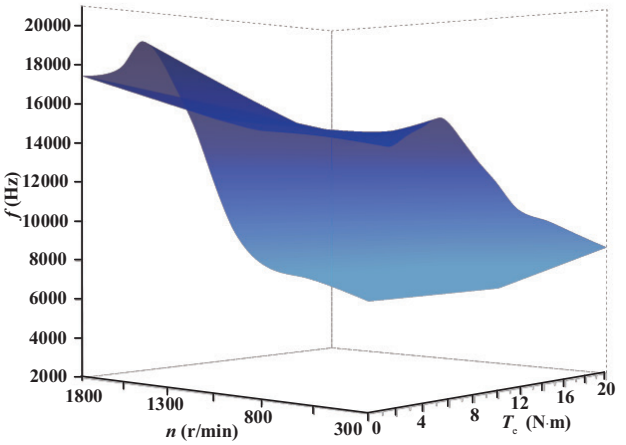

Fig. 22. DV-MPC output switching frequency.

the rising and falling edges of the drive signals, each switching cycle is computed, and the corresponding switching frequency for each cycle is recorded chronologically to generate a time-series sequence of switching frequency variations. Based on different rotational speeds and torques, the variation patterns of switching frequencies under specified operating conditions are illustrated in the figures.

As illustrated in Fig. 22, the switching frequency under DV-MPC increases with rising motor speed and load torque, as more voltage vector transitions are triggered in the L-DO-TLC.

When comparing Figs. 22 and 23, it is evident that SV-MPC consistently produces lower switching frequencies than DV-MPC across all of the operating conditions.

The switching frequency under HV-MPC is illustrated in Fig. 24. By combining single vector and DV strategies, the hybrid vector approach enhances torque control, ensures smoother speed transitions, and reduces unnecessary speed adjustments. As a result, the switching frequency under HV-

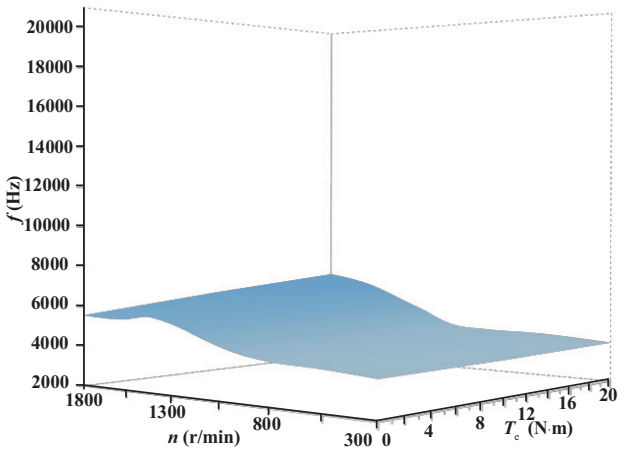

Fig. 23. SV-MPC output switching frequency.

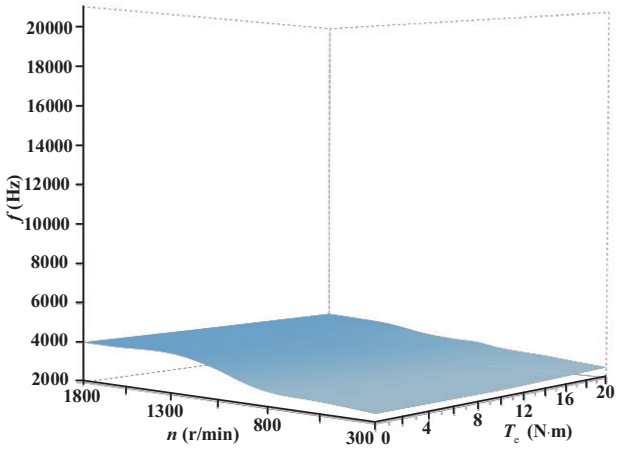

Fig. 24. HV-MPC output switching frequency.

MPC is slightly lower than that under SV-MPC, with minimal variation across different OEWIM operating conditions. Thus, HV-MPC effectively mitigates the excessively high switching frequency observed in DV-MPC.

Fig. 25 shows the average computation time comparison of the DV-MPC, SV-MPC, and HV-MPC control strategies, respectively. From the statistical results, it can be observed that the average computation time of DV-MPC is 56.27 μs, while that of SV-MPC is 27.88 μs. In contrast, HV-MPC further reduces the average computation time to 26.23 μs. While maintaining control performance comparable to DV-MPC, HV-MPC significantly decreases the computational burden, demonstrating superior computational efficiency and real-time capability. This makes it more suitable for motor control systems with demanding real-time requirements.

VI. Conclusion

This paper proposes a novel OEWIM drive scheme based on an L-DO-TLC, which significantly enhances system performance by optimizing both the inverter topology and the control strategy. The proposed L-DO-TLC adopts an

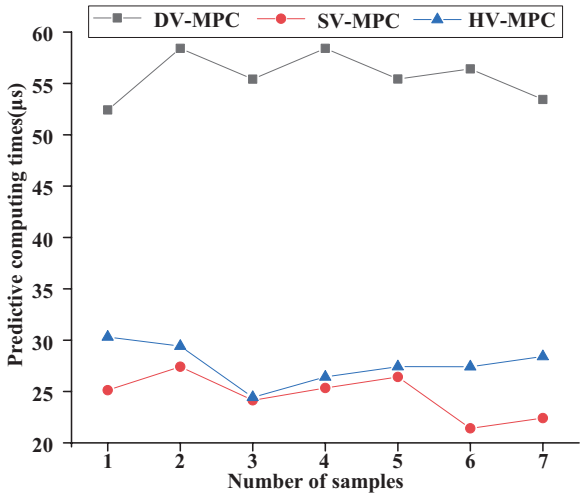

Fig. 25. Comparison of computation time for different control strategies.

innovative "L"-shaped cascaded structure and a device reuse approach, reducing the number of power switches by 37.5% while preserving three-level output functionality. This effectively improves system cost-efficiency and power density. Based on this topology, a dual-port 120°-phase-shifted wiring configuration is introduced to ensure the necessary voltage and phase differences for OEWIM operation under the switch-sharing constraint. In terms of control, the proposed HV-MPC method simplifies the vector selection process and reduces computational complexity through a ZSC suppression mechanism. The proposed control strategy is validated through comprehensive simulation studies and HIL experiments. Furthermore, HV-MPC dynamically combines SV and DV control to reduce torque ripple and optimize switching frequency, thereby achieving stable and efficient operation of the OEWIM drive system.

References

[1] X. Zhang and Y. He, "Robust model predictive direct speed control for SPMSM drives based on full parameters and load observer," in *2019 IEEE International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE)*, Quanzhou, China, 2019, pp. 1–5.

[2] L. Xu and Z. Q. Zhu, "Novel SVPWM for open winding PMSM drives with simultaneous common mode voltage control and full frequency zero sequence current suppression," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 2, pp. 2151–2163, Apr. 2023.

[3] U. R. Muduli, A. R. Beig, K. Al Jaafari, K. Al Hosani, A. S. Al-Sumaiti, and R. K. Behera, "Dual motor power sharing control for electric vehicles with battery power management," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 12, pp. 12024–12035, Dec. 2023.

[4] X. Lin, W. Huang, and L. Wang, "SVPWM strategy based on the hysteresis controller of zero-sequence current for three-phase open-end winding PMSM," in *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3474–3486, Apr. 2019.

[5] S. G. Petkar and V. K. Thippiripati, "A simplified predictive current control of open-end winding permanent magnet synchronous motor," in *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 816–826, Jan. 2023.

[6] Y. Geng, L. Wang, J. Xu, and C. Wei, "A modulation strategy of dual inverter using sigma-delta converter," in *Transactions of China Electrotechnical Society*, vol. 32, no. 8, pp. 239–247, Sept. 2017.

[7] Q. An and L. Sun, "Research on novel open-end winding permanent magnet synchronous motor vector control systems," in *Proceedings of the CSEE*, vol. 35, no. 22, pp. 5891–5898, Nov. 2015.

[8] J. Yin, X. Jin, J. Yang, and J. Li, "The differential common mode voltage elimination of dual three-level converter for open-end winding motor drives," in *Transactions of China Electrotechnical Society*, vol. 31, no. 15, pp. 178–186, Aug. 2016.

[9] K. Dong, T. Shi, S. Xiao, X. Li, and C. Xia, "Finite set model predictive control method for quasi-z source inverter-permanent magnet synchronous motor drive system," in *IET Electric Power Applications*, vol. 13, no. 3, pp. 302–309, Mar. 2019.

[10] X. Zhang and K. Wang, "Current prediction based zero sequence current suppression strategy for the semicontrolled open-winding PMSM generation system with a common DC bus," in IEEE Transactions on Industrial Electronics, vol. 65, no. 8, pp. 6066–6076, Aug. 2018.

[11] X. Zhang, K. Yan, and W. Zhang, "Hybrid double vector model predictive control for open-winding permanent magnet synchronous motor with common DC bus," in *Transactions of China Electrotechnical Society*, vol. 36, no. 1, pp. 96–106, Jan. 2021.

[12] L. Cheng, H. Jianhui, and S. Jing, "Dual-vector predictive current control of open-end winding PMSM with zero-sequence current hysteresis control," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 184–195, Feb. 2022.

[13] Q. An, J. Liu, Z. Peng, L. Sun, and L. Sun, "Dual-space vector control of open-end winding permanent magnet synchronous motor drive fed by dual inverter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8329–8342, Dec. 2016.

[14] H. Yang, M. Li, Y. Zhang, and A. Xu, "FCS-MPC for three-level NPC inverter-fed SPMSM drives without information of motor parameters and DC capacitor," in *IEEE Transactions on Industrial Electronics*, vol. 71, no. 4, pp. 3504–3513, Apr. 2024.

[15] H. Kawai, J. Cordier, R. Kennel, and S. Doki, "Model predictive current control with a finite set of novel voltages and modulator in permanent magnet synchronous motor drives," in *IET Electric Power Applications*, vol. 17, no. 9, pp. 1197–1211, Sept. 2023.

[16] C. Zhang, B. Xu, J. Jasni, M. A. M. Radzi, "Three voltage vector duty cycle optimization strategy of the permanent magnet synchronous motor driving system for new energy electric vehicles based on finite set model predictive control," in *Energies*, vol. 16, no. 6, p. 2684, Mar. 2023.

[17] S. Xia, X. Wu, J. Zheng, X. Li, and K. Wang, "A virtual space vector PWM with active neutral point voltage control and common mode voltage suppression for three-level NPC converters," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 11761–11771, Dec. 2021.

[18] J. Haruna and N. Hoshi, "A novel three-level inverter which can drive two PMSMs," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, Manchester, UK, 2014, pp. 1–6.

[19] R. Wang, S. Yuan, C. Liu, D. Guo, and X. Shao, "A three-phase dual-output T-type three-level converter," in *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 1844–1859, Feb. 2023.

[20] C. I. Odeh, A. Lewicki, M. Morawiec, and D. Kondratenko, "Three-level F-type inverter," in *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11265–11275, Oct. 2021.

[21] K. Arunachalam, S. K. Vairakannu, and G. Nallathambi, "Comparison and optimisation of three-level neutral point clamped dual output inverter," in *IET Circuits, Devices & Systems*, vol. 14, no. 1, pp. 48–59. Oct. 2019.

[22] R. Wang, X. Wu, and X. Wang, "Three-phase hybrid converter with simultaneous DC and AC outputs," in *IEEE Access*, vol. 11, pp. 24382–24393, 2023.

Qigang Du was born in Xuzhou, China, in 2002. He received the B.S. degree in Electrical Engineering and Automation from Changchun Institute of Technology, Changchun, China, in 2022. He is currently working toward the M.S. degree in Electronic Information with Jiangsu Normal University, Xuzhou, China. His current research interests include model predictive control, power conversion, and power quality.

Guifeng Wang was born in Linyi, Shandong, China, in 1982. He obtained his B.S. degree in Electrical Engineering and Automation and M.S. degree in Electrical Engineering from the School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou, China, in 2004 and 2007, respectively. In 2016, he was awarded a Ph.D. in Power Electronics and Electrical Drive from Shanghai Jiao Tong University, Shanghai, China. Currently, He holds the position of Senior Engineer at the College of Electrical Engineering and Automation, Jiangsu Normal University, Xuzhou. His research primarily focuses on power electronic converters for electrical drives and power quality enhancement.

Junhui Jiang was born in Nantong, China, in 1998. He received the B.S. degree from Jiangsu Ocean University, Lianyungang, China, in 2021, and the M.S. degree from Jiangsu Normal University, Xuzhou, China, in 2025. He is currently pursuing the Ph.D. degree in School of Electrical Engineering and Automation, China University of Mining and Technology, Xuzhou, China. His current research interests include power electronics and electric machines drives.

Weipeng Shi received the Ph.D. degree from Southeast University, Nanjing, China, in 2024. He is currently a Lecturer with the School of Electrical Engineering and Automation, Jiangsu Normal University, Xuzhou, China. His research interests include computer vision, remote sensing detection, and fundamental theory and applications of artificial intelligence.

Chao Luo was born in Taizhou, China, in 2001. He received the B.S. degree in Electrical Engineering and Automation from Nanjing Tech University, China, in 2023. He is currently working toward the M.S. degree in Electronic Information with Jiangsu Normal University, Xuzhou, China. His current research interests lie in the fields of power electronics and electric machine drives.

Ke Li received the B.S. degree in Electrical Engineering and Automation from Xi'an University of Architecture and Technology, Xi'an, China, in 2025. He is currently working as an Electrical Motor R&D Engineer at Xuzhou South-Power Electromechanical Technology Co., Ltd., Xuzhou, China. His current research interests include electrical machine design, motor drives, and power electronics.