An Enhanced Non-Isolated DC-DC Converter With High Voltage Gain Capability for Efficient Power Conversion

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***Abstract*—This paper introduces an enhanced non-isolated DC-DC converter with high voltage gain capability for efficient power conversion. The proposed configuration achieves significant voltage gain with minimal components, ensuring optimal performance under various operating conditions. In particular, it maintains a common ground between the input and output, enhancing safety and reliability. Furthermore, the design offers high efficiency, balanced voltage and current distribution, reduced stress on switching devices, and effectively minimizes voltage fluctuations. These attributes make it a highly suitable solution for various power conversion applications. The paper provides a comprehensive analysis of converter key waveforms, operating principles, steady-state behavior, and design equations. The voltage conversion ratio, as well as voltage and current stress, is derived and compared with other converters in the literature. To validate the proposed converter design, a 400 W prototype was developed and successfully tested, demonstrating efficient voltage conversion from 32 V to 400 V.**

***Index Terms*—Common ground, high voltage gain, reduced current stress, reduced voltage stress, switched capacitor and inductor.**

I. Introduction

HIGH gain DC-DC converters are crucial in various advanced applications, including DC microgrids, electric vehicles, uninterruptible power supplies, fuel cells, and photovoltaic (PV) systems [1]. These converters are broadly classified into two categories: non-isolated and isolated types. Non-isolated DC-DC converters that utilize active switched inductor (ASL) technology [2] achieve higher step-up voltage gains compared to those based on switched capacitor (SC) techniques. However, conventional ASL converters exhibit limited voltage amplification capability [3]. To enhance voltage gain, several topologies have been developed that integrate ASL with passive switched capacitors (PSC) [4]–[9]. In addition, auxiliary switches have been introduced to further improve increased voltage gain [10]. Although these configurations effectively increase the voltage gain, they also require additional gate-drive circuits, thereby increasing the system size, cost, and control complexity. Moreover, these designs expose the auxiliary switches and output diodes to significant voltage stress [11], [12]. A major limitation of ASL converters [4]–[12] is their high sensitivity to parameter variations, leading to increased voltage and current stress across circuit elements, uneven current distribution among identical components, and, in some cases, the absence of common grounding. The resonance circuit formed by the switch drain-source capacitor and inductors induces voltage oscillations across the switches, contributing to elevated voltage stress and reduced efficiency. To address voltage distribution challenges, some designs incorporate SC networks [13], [14]; however, this modification can compromise the converter step-up voltage gain. Furthermore, the lack of common ground between the input and output stages intensifies electromagnetic interference (EMI) issues, which negatively impact the reliability and longevity of renewable energy sources such as fuel cells and PV systems.

DC-DC converters with high voltage gain and common ground are highly recommended for fuel cell and solar applications, as they effectively address key operational challenges [15]. However, these converters typically function within a limited duty cycle range, making them particularly susceptible to duty cycle variations, which can compromise operational stability. In search of better designs, [16] introduces an innovative SEPIC-based converter for fuel cell applications. This design incorporates a single switch and a greater number of circuit elements but lacks common ground. Alternatively, [17] and [18] propose a common ground ASL/PSC hybrid voltage quadruple converter, which employs two switches and fewer circuit components. Despite these advancements, the converters presented in [16], [17], and [18] still face several notable challenges. These include lower voltage gain, elevated inductor currents requiring components with higher ratings, increased voltage and current stress on switches and diodes, uneven current distribution among identical components, and an overall reduction in efficiency.

To address these limitations, this study presents an advanced non-isolated DC-DC converter featuring high voltage gain capability, achieved through an active switched inductor/capacitor network. This innovative design effectively overcomes the challenges associated with existing topologies while enhancing voltage gain, efficiency, and operational stability.

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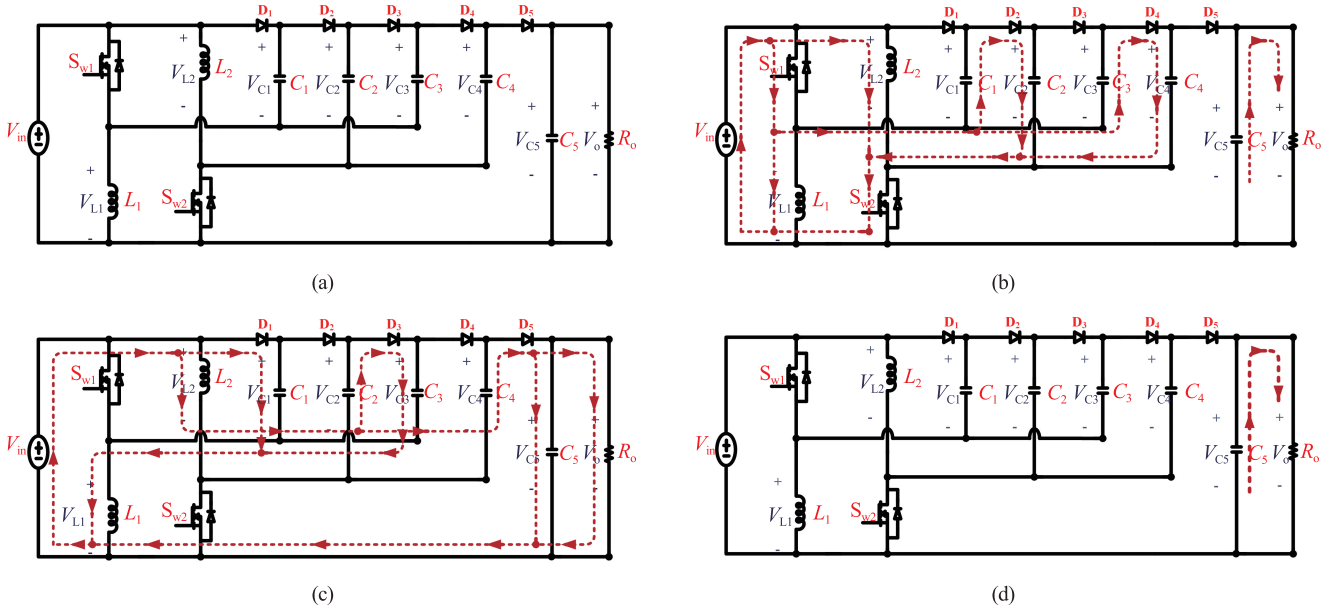

Fig. 1. Converter configuration showing. (a) Proposed converter. (b) Current path in state-1. (c) Current path in state-2. (d) Current path in state-3.

II. Operation of Proposed Converter

Fig. 1(a) illustrates the circuit diagram of the proposed converter configuration. The design incorporates two inductors (L_1 and L_2), five diodes (D_1–D_5), two switching devices (S_{w1} and S_{w2}), and five capacitors (C_1–C_5). In this configuration, the duty cycle of the switches is represented by the variable d, while F_s denotes the switching frequency.

A. CCM Operation

In continuous conduction mode (CCM), the converter undergoes two distinct operational states within one cycle.

1) State-1 ($0 - dT_s$): During State-1, the switches (S_{w1} and S_{w2}) and the diodes (D_2 and D_4) conduct, while the diodes (D_1, D_3, and D_5) remain in an OFF state. Fig. 1(b) illustrates the current flow within the converter during this phase. In this state, the voltage across the inductors is equal to the input voltage. During same time, the capacitors (C_1 and C_3) discharge, facilitating the charging of the capacitors (C_2 and C_4). Meanwhile, the capacitor (C_5) delivers its stored energy to the load. By applying Kirchhoff's Voltage Law, the following equations can be derived.

$$\begin{cases} V_{L1} = V_{in} = V_{C2} - V_{C1} = V_{C4} - V_{C3} \\ V_{L2} = V_{in} \\ V_o = V_{C5} \end{cases} \tag{1}$$

2) State-2 ($dT_s - T_s$): During State-2, the switches (S_{w1} and S_{w2}) and diodes (D_2 and D_4) remain OFF, while diodes (D_1, D_3, and D_5) conduct. Fig. 1(c) illustrates the current flow in this operational phase. In this state, the input is connected in series with the inductor (L_1) and capacitor (C_1). In addition, the inductor (L_1), inductor (L_2), capacitor (C_2), and capacitor (C_3) form another series network. Finally, the inductor (L_2) and the capacitor (C_4) establish a series connection, discharging through the load and the capacitor (C_5). Fig. 2(a) illustrates the waveform of key components during the CCM states. Applying Kirchhoff's Voltage Law, the following equations can be derived.

$$\begin{cases} V_{L1} = V_{in} - V_{C1} = V_{C2} - V_{C3} - V_{C4} + V_{C5} \\ V_{L2} = V_{in} + V_{C4} - V_{C5} \\ V_o = V_{C5} \end{cases} \tag{2}$$

B. DCM Operation

In discontinuous conduction mode (DCM), the voltage across the inductors (L_1 and L_2) drops to zero before the end of the switching cycle, resulting in the operation being divided into three distinct phases. Since the first two DCM operating states closely resemble those in CCM, this section exclusively examines the third state of DCM.

1) State-3: When the current in inductors (L_1 and L_2) reaches zero, the voltage across them also drops to zero, marking the onset of this operational state. As a result, all semiconductor devices transition to an OFF state. During this state, the capacitor (C_5) releases its stored energy to the load. Fig. 2(b) illustrates the waveform of key components during the DCM states.

III. Analysis of Proposed Converter

A. CCM Operation

The waveform of the critical components in CCM states is illustrated in Fig. 1(b), Fig. 1(c), and Fig. 2(a).

1) Voltage gain (M): Using flux balance across inductors, the converter capacitor voltages and voltage gain (M) are obtained:

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{(1-d)}, V_{C2} = \dfrac{(2-d)V_{in}}{(1-d)} \\ V_{C3} = \dfrac{3V_{in}}{(1-d)}, V_{C4} = \dfrac{(4-d)V_{in}}{(1-d)} \end{cases} \tag{3}$$

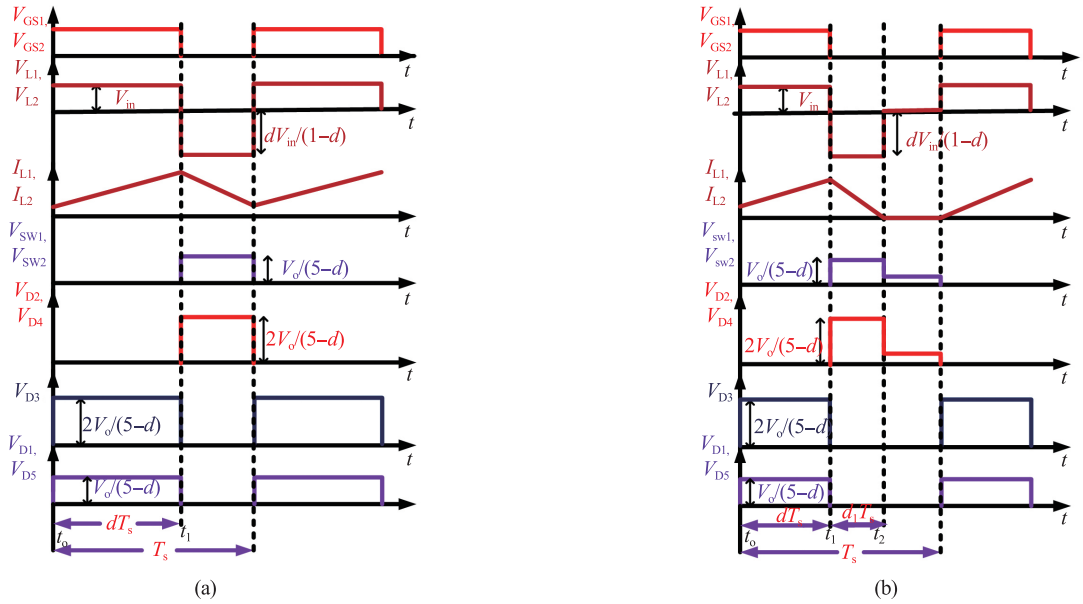

Fig. 2. Operating waveforms. (a) CCM. (b) DCM.

The voltage gain of proposed converter is given as

$$M = \frac{(5-d)}{(1-d)} \tag{4}$$

2) Voltage stress: The following are the voltage stress results of semiconductor devices from Fig. 1(b) and Fig. 1(c).

$$\begin{cases} V_{sw1} = V_{sw2} = \dfrac{V_{in}}{(1-d)} \\ V_{D1} = V_{D5} = \dfrac{V_{in}}{(1-d)} \\ V_{D2} = V_{D3} = V_{D2} = \dfrac{2V_{in}}{(1-d)} \end{cases} \tag{5}$$

3) Inductor current: The inductors current is determined by applying the charge balance principle across the capacitors.

$$I_{L1} = I_{L2} = \frac{2I_o}{(1-d)} \tag{6}$$

4) Current stress: The following section presents the RMS current stress imposed on capacitors and semiconductor devices.

$$\begin{cases} I_{C1} = I_{C2} = I_{C3} = I_{C4} = \dfrac{I_o}{\sqrt{d(1-d)}} \\ I_{C5} = \dfrac{I_o\sqrt{d}}{\sqrt{(1-d)}} \\ I_{sw1} = I_{sw2} = \dfrac{2I_o}{(1-d)\sqrt{d}} \\ I_{D2} = I_{D4} = \dfrac{I_o}{\sqrt{d}} \\ I_{D1} = I_{D3} = I_{D5} = \dfrac{I_o}{\sqrt{(1-d)}} \end{cases} \tag{7}$$

B. DCM Operation

The converter works in all three states in DCM. Fig. 2(b) illustrated the circuit conditions and important waveforms for DCM operation.

1) Voltage gain (M_{DCM}): The derivation of the voltage gain in DCM begins with evaluating the peak inductor currents attained during Stage-1 and Stage-2 of the switching cycle

$$\begin{cases} i_{Lpeak} = \dfrac{V_{in}}{L} dT_s & \text{Stage-1} \\ i_{Lpeak} = \dfrac{V_o - 8V_{in}}{L} d_1 T_s & \text{Stage-2} \end{cases} \tag{8}$$

Since the peak inductor currents attained during Stage-1 and Stage-2 are equal, the relationship between d_1 and d can be established accordingly

$$d_1 = \frac{4V_{in}d}{V_o - 8V_{in}} \tag{9}$$

Furthermore, the relationship between the peak inductor current and the load current can be expressed as follows

$$\frac{i_{Lpeak}}{2} = \frac{2V_o}{d_1 R_o} \tag{10}$$

From (9) and (10), the voltage gain expression in DCM an be derived as

$$M_{DCM} = 4 + \sqrt{16 + \frac{d^2 R_o}{LF_s}} \tag{11}$$

It can be observed that the voltage gain in DCM depends not only on the duty cycle d, but also on the inductance L, the switching frequency F_s, and the load resistance R_o.

2) Boundary condition: In boundary conduction mode (BCM),

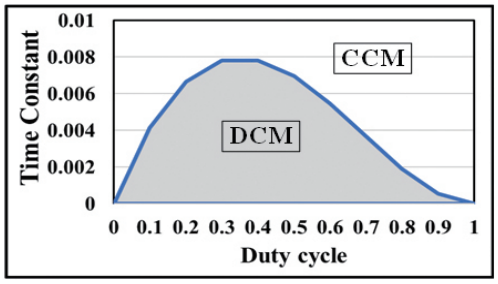

Fig. 3. Boundary conduction.

the currents through the semiconductor devices de- crease to zero at end of each switching period. The inductor current should be greater than half of ripple inductor to operate in CCM operation.

$$I_L > \frac{\Delta I_L}{2} \tag{12}$$

By substituting above equation

$$\text{Time constant}\left(\frac{L}{R_o T_s}\right) > \frac{d(1-d)^2}{4(5-d)} \tag{13}$$

Based on (13), the boundary condition versus duty cycle for the converter is illustrated in Fig. 3.

C. Voltage Oscillation Mitigation Across Switches

For optimal converter performance, the drain-source capacitance of the MOSFETs (C_{s1} and C_{s2}) and the inductance values (L_1 and L_2) should be equivalent. However, any parameter imbalance between C_{s1}, C_{s2}, L_1, and L_2 can lead to resonance, increasing voltage stress. Since precise parameter matching is practically unattainable, resonance-induced voltage stress inevitably occurs, as discussed in [3]–[8]. To mitigate this effect, the proposed converter incorporates capacitor C_1 in parallel with C_{s1} and capacitors C_4 and C_5 in parallel with C_{s2} as illustrated in Fig. 1. This configuration maintains a stable and uniform voltage across the switches and inductors, effectively minimizing resonance-induced voltage stress despite inevitable parameter variations.

D. Inductor Design

Current ripple (Δi_L), duty cycle (d), switching frequency (F_s), and average current through the inductor are some of the crucial variables that affect the inductance design. To guarantee CCM operation, the proper inductance values must be selected.

$$\begin{cases} L_1 \geqslant \dfrac{R_o d(1-d)^2}{2(5-d)\delta_L F_s} \\ L_2 \geqslant \dfrac{R_o d(1-d)^2}{2(5-d)\delta_L F_s} \end{cases} \tag{14}$$

where ripple current $\delta_L = \dfrac{\Delta I_L}{I_L}$.

E. Capacitor Design

Voltage ripple (ΔV_C), duty cycle (d), switching frequency (F_s), and voltage across capacitor are some of the crucial variables that affect capacitance design.

$$\begin{cases} C_1 \geqslant \dfrac{(5-d)}{\delta_{cx} R_o F_s}, C_2 \geqslant \dfrac{(5-d)}{(2-d)\,\delta_{cx} R_o F_s} \\ C_3 \geqslant \dfrac{(5-d)}{3\delta_{cx} R_o F_s}, C_4 \geqslant \dfrac{(5-d)}{(4-d)\,\delta_{cx} R_o F_s} \\ C_o \geqslant \dfrac{d}{\delta_{cx} R_o F_s} \end{cases} \tag{15}$$

where ripple voltage $\delta_{cx} = \dfrac{\Delta V_C}{V_C}$.

IV. Modelling of Proposed Converter

The dynamical characteristic of the proposed power converter are scrutinized utilizing a state-space model (SSM), wherein the currents flow through the inductors and the voltages across the capacitors are considered as state variables. The state variable matrix is delineated in (12) and (13). The SSM is constructed for both the ON and OFF states of the switching devices. The following equations formulation presents the state-space equation that governs the converter's operation over a complete switching interval.

$$\begin{pmatrix} \hat{I}_{L1} \\ \hat{I}_{L2} \\ \hat{V}_{C1} \\ \hat{V}_{C2} \\ \hat{V}_{C3} \\ \hat{V}_{C4} \\ \hat{V}_{C5} \end{pmatrix} = \begin{pmatrix} 0 & 0 & -\frac{(1-d)}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{(1-d)}{L_2} & \frac{-(1-d)}{L_2} \\ \frac{d}{C_1} & -\frac{(1-d)}{C_1} & 0 & 0 & 0 & 0 & 0 \\ \frac{-1}{C_2} & -\frac{(1-d)}{C_2} & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-d)}{C_3} & \frac{-1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-d)}{C_4} & \frac{-d}{C_4} & 0 & 0 & 0 & 0 & 0 \\ \frac{-(1-d)}{C_5} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_o C_5} \end{pmatrix} \times \begin{pmatrix} \hat{I}_{L1} \\ \hat{I}_{L2} \\ \hat{V}_{C1} \\ \hat{V}_{C2} \\ \hat{V}_{C3} \\ \hat{V}_{C4} \\ \hat{V}_{C5} \end{pmatrix} + \begin{pmatrix} I_{L1}\left(\frac{1}{C_1} - \frac{1}{C_3} - \frac{1}{C_4} + \frac{1}{C_5}\right) \\ I_{L2}\left(\frac{1}{C_1} + \frac{1}{C_2} - \frac{1}{C_4}\right) \\ V_{C1}\left(\frac{1}{L_1}\right) \\ 0 \\ 0 \\ V_{C4}\left(\frac{-1}{L_2}\right) \\ V_{C5}\left(\frac{1}{L_2}\right) \end{pmatrix} \hat{d} \tag{16}$$

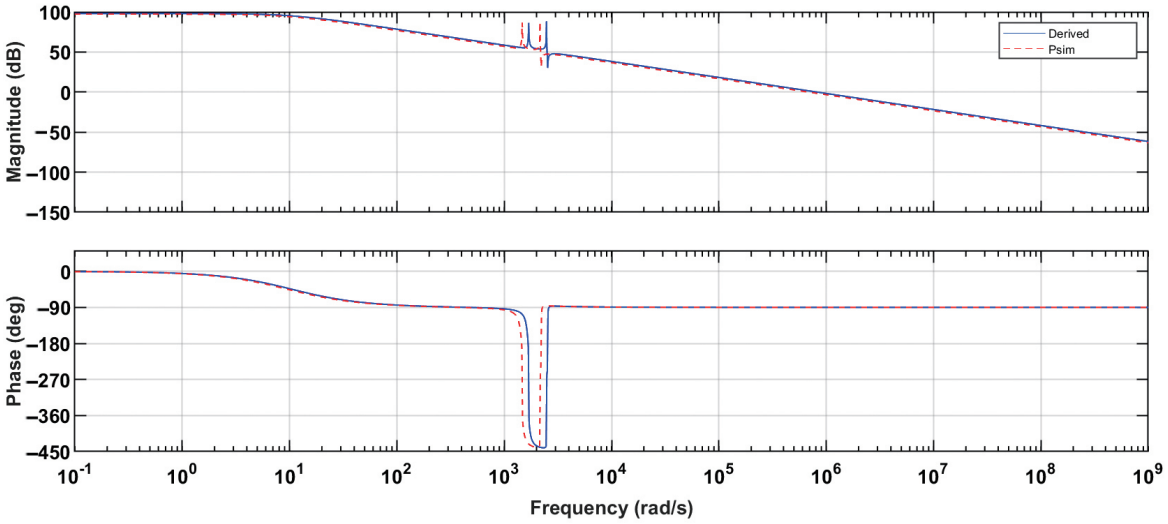

Fig. 4. Open loop frequency response.

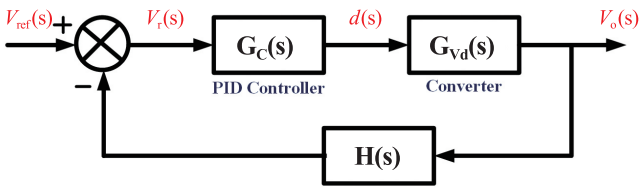

Fig. 5. Block diagram of closed loop controller.

$$(\hat{V}_0) = (0\ 0\ 0\ 0\ 0\ 0\ 1)\begin{pmatrix}\hat{I}_{L1}\\ \hat{I}_{L2}\\ \hat{V}_{C1}\\ \hat{V}_{C2}\\ \hat{V}_{C3}\\ \hat{V}_{C4}\\ \hat{V}_{C5}\end{pmatrix} \tag{17}$$

where $^{\wedge}$ represents small ac variation.

The proposed converter open-loop transfer function $G_{vd}(s)$ is given below.

$$\frac{V_o}{d(s)} = \frac{8.1694e^5(s^2 - 137.1s + 2.802e^6)(s^2 + 12.26s + 6.442e^6)}{(s+10.59)(s^2 + 3.581s + 2.853e^6)(s^2 - 1.669s + 6.123e^6)} \tag{18}$$

To appraise the dynamical performance of the system, an analysis based on small-signal frequency response is executed. Fig. 4 illustrates the open-loop frequency response transfer function. To ascertain the converter optimal operation, a proportional-integral-derivative (PID) controller is meticulously designed and integrated, with the intent to secure the requisite phase and gain margins is illustrated in Fig. 5. The PID controller was designed using the Ziegler-Nichols tuning method, which involved determining (K_u) and (P_u) by analyzing the system stable oscillatory response. Based on these values, the proportional, integral, and derivative gains were calculated following Ziegler-Nichols formulas.

V. Performance Comparison

The proposed converter performance parameters are rigorously compared with other converters recorded in the literature, as presented in Table I. The comparison is based on current stress, component count, common grounding (G_{com}), voltage gain, voltage stress, and resonance across switches (V_{sres}). Fig. 6 illustrates the voltage gains versus duty cycle, voltage and current stress of converters [3], [4], [6], [7], [8], [13], [14], [16], [17], and proposed converters using the gain formula described in Table I. When compared to the converters in the literature, the proposed converter performance is better.

VI. Experimental Analysis

The converter is meticulously designed, fabricated, and rigorously tested to assess its performance and effectiveness. Gating pulses were generated using the DSP LAUNCHXL-F28379D processor. Fig. 7 illustrates the converter experimental setup, while Table II provides a detailed specification of the components used.

At an operating point of M = 12.5, with an input voltage (V_{in}) of 32 V, the output voltage (V_o) and current (I_o) are measured to be 400 V and 1 A, respectively. Fig. 8 illustrates the experimental waveforms of V_o, V_{C4}, V_{C3}, and I_o. Under these operating conditions, V_o = 400 V, V_{C4} = 308 V, V_{C3} = 277 V, and I_o = 1 A, respectively. Fig. 9 illustrates the experimental waveforms of V_{C2}, V_{C1}, I_{L1}, and I_{L2}. Average currents via inductors L_1 and L_2 are 5.88 A each under these operating conditions, but the voltages across capacitors V_{C2} and V_{C1} are 124 V and 92 V, respectively. Fig. 10 illustrates the experimental waveforms of V_{sw1}, and V_{sw2}. The experimentally measured voltages across

TABLE I
COMPARISON OF DC-DC CONVERTERS

Converter	[6]	[8]	[4]	[3]	[7]	[13]	[14]	[16]	[17]	[18]	Proposed
S/D/L/C	2/4/3/5	2/5/2/5	2/2/3/3	2/4/3/1	2/3/2/3	2/2/2/4	2/4/2/4	1/5/3/7	2/5/2/5	2/4/2/4	2/5/2/5
M	$\frac{(5-d)}{(1-d)}$	$\frac{(5+d)}{(1-d)}$	$\frac{(1+3d)}{(1-d)}$	$\frac{(1+2d)}{(1-d)}$	$\frac{(3+d)}{(1-d)}$	$\frac{(1+d)}{(1-d)}$	$\frac{(3+d)}{(1-d)}$	$\frac{(2+2d)}{(1-d)}$	$\frac{4}{(1-d)}$	$\frac{(4-d)}{(1-d)}$	$\frac{(5-d)}{(1-d)}$
V_O at $d = 0.7$ and $V_{in} = 32$ V	458.6	608	330.6	256	394.6	181.3	394.6	362.6	426.6	352	458.6
$\frac{V_{sw}}{V_o}$	$\frac{1}{(5-d)}$	$\frac{1}{(5+d)}$	$\frac{1}{(3+d)}$	$\frac{1}{(1+2d)}$	$\frac{1}{(3+d)}$	$\frac{1}{(1+d)}$	$\frac{1}{(3+d)}$	$\frac{1}{(2+2d)}$	$\frac{1}{4}$	$\frac{1}{(4-d)}$	$\frac{1}{(5-d)}$
$\frac{V_D}{V_o}$	$\frac{2}{(5-d)}$	$\frac{2}{(5+d)}$	$\frac{2}{(3+d)}$	$\frac{(2+d)}{(1+2d)}$	$\frac{2}{(3+d)}$	$\frac{1}{(1+d)}$	$\frac{2}{(3+d)}$	$\frac{1}{(2+2d)}$	$\frac{1}{2}$	$\frac{2}{(4-d)}$	$\frac{2}{(5-d)}$
$\frac{V_C}{V_o}$	$\frac{(3+d)}{(5-d)}$	$\frac{(3+d)}{(5-d)}$	$\frac{(1+d)}{(3+d)}$	–	$\frac{2}{(3+d)}$	$\frac{1}{2}$	$\frac{(2+d)}{(3+d)}$	$\frac{1}{(2+2d)}$	$\frac{(2+d)}{4}$	$\frac{(3-d)}{(4-d)}$	$\frac{(4-d)}{(5-d)}$
$\frac{I_L}{I_o}$	$\frac{3}{(1-d)}$	$\frac{3}{(1-d)}$	$\frac{(1+d)}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{2}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{2}{(1-d)}$	$\frac{(2+2d)}{(1-d)}$	$\frac{3}{(1-d)}$	$\frac{2}{(1-d)}$	$\frac{2}{(1-d)}$
$\frac{I_{sw}}{I_o}$	$\frac{(2+d)}{d(1-d)}$	$\frac{(1+d)}{d(1-d)}$	$\frac{2}{d(1-d)}$	$\frac{2}{d(1-d)}$	$\frac{(1+d)}{d(1-d)}$	$\frac{(1+d)}{d(1-d)}$	$\frac{(1+d)}{d(1-d)}$	$\frac{(1+3d)}{d(1-d)}$	$\frac{(1+d)}{d(1-d)}$	$\frac{2}{d(1-d)}$	$\frac{2}{d(1-d}$
$\frac{I_D}{V_o}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$	$\frac{1}{(1-d)}$
G_{com}	No	No	No	No	No	No	No	No	No	Yes	Yes
V_{sres}	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No

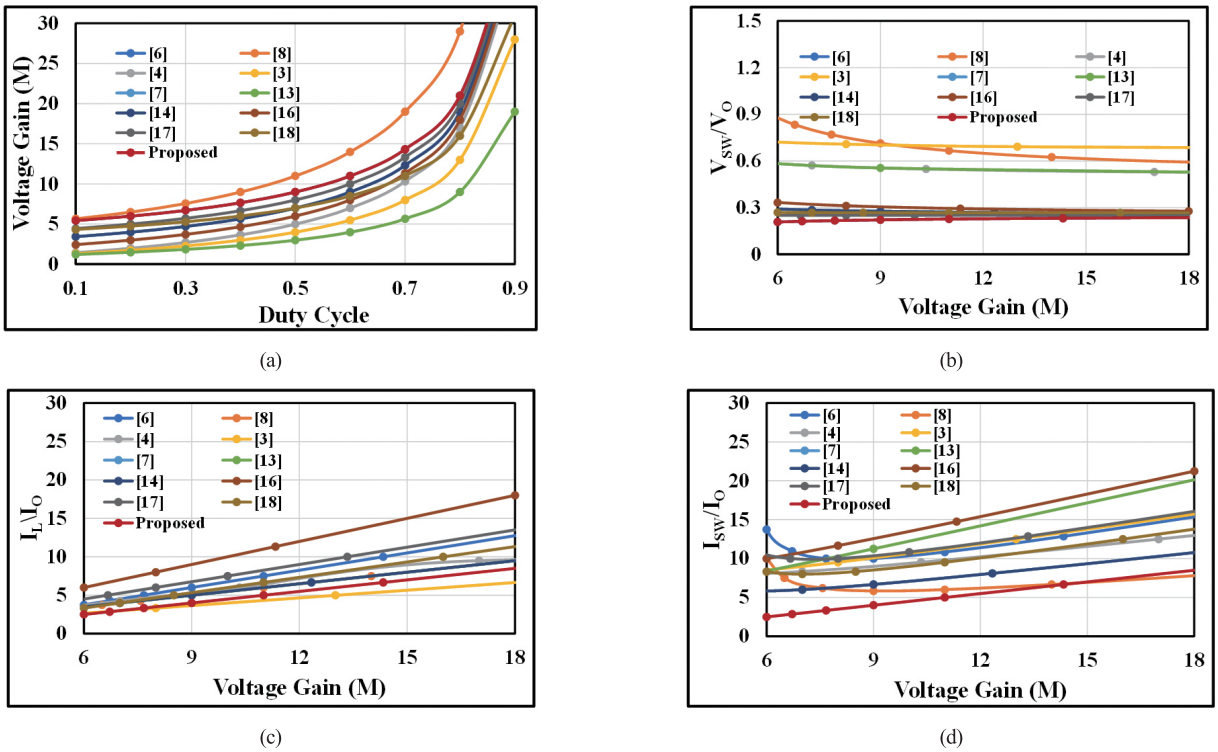

Fig. 6. Comparison of proposed converter. (a) Voltage gain vs duty cycle. (b) Max. V_{sw}/V_o vs voltage gain. (c) Max. I_L/I_o vs voltage gain. (d) Max. I_{sw}/I_o vs voltage gain.

switches are $V_{sw1} = V_{sw2} = 92$ V.

Fig. 11 illustrates the experimental waveforms of V_{D1} and V_{D2}. The experimentally measured voltages across diodes are $V_{D1} = 92$ V, and $V_{D2} = 184$ V. Fig. 12 illustrates the experimental waveforms of V_{D3}, V_{D4}, and V_{D5}. The experimentally measured voltages across diodes are $V_{D3} = 184$ V, $V_{D4} = 184$ V, and $V_{D5} = 92$ V. The voltages across all semiconductor devices remain significantly lower than the output voltage under all operating conditions.

Fig. 13 illustrates the initial transient responses of the output voltage and current in closed-loop operation. Furthermore, to evaluate the converter anti-interference capability during load variations, a load step change experiment was conducted. In this test, the converter output power alternates between 400 W

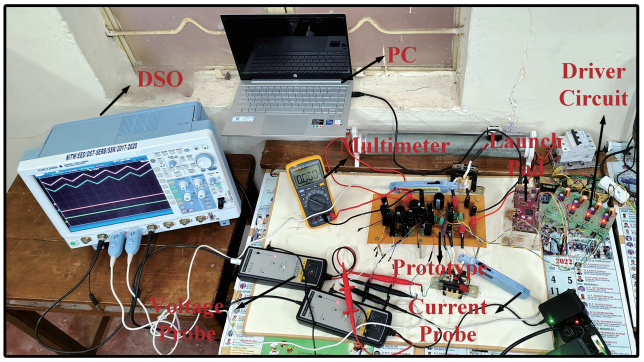

Fig. 7. Experimental setup.

TABLE II
CONVERTER SPECIFICATIONS

Component	Rating/Value
Input voltage	32 V
Inductors	0.5 mH
Capacitors	100 µF, 200 µF
Load	400 Ω
Switching frequency	25 kHz
Switches	IRF300P226
Diodes	STTH61W04S
PID Values	$K_P = 0.002$, $K_I = 2$ $K_D = 2e^{-6}$, $N_D = 20000$

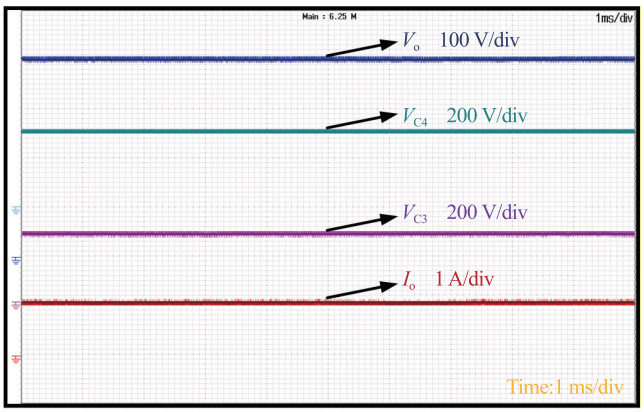

Fig. 8. Experimental results: V_o, V_{C4}, V_{C3}, and I_o.

and 200 W while consistently maintaining an output voltage (V_o) of 400 V. The output current at 200 W is observed to be half that at 400 W. The experimental results of this assessment are illustrated in Fig. 14.

Efficiency is a vital metric for assessing the converter's performance, necessitating individual component evaluation. The power loss distribution is computed using thermal analysis on the PSIM software platform, adhering to the converter specifications.

Inductor Loss: The majority of power loss in the inductors arises from their parasitic series resistance, which can be evaluated using the RMS current flowing through them.

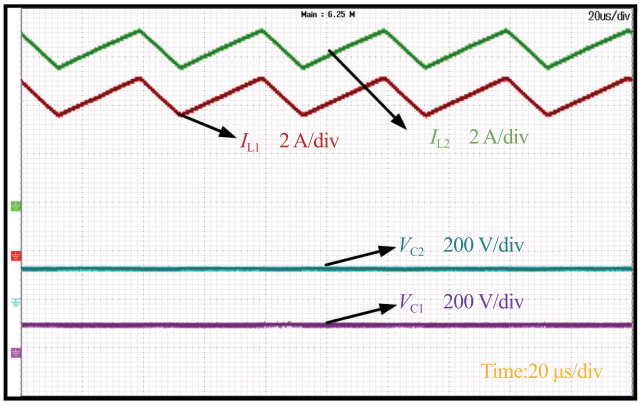

Fig. 9. Experimental results: V_{C2}, V_{C1}, I_{L1}, and I_{L2}.

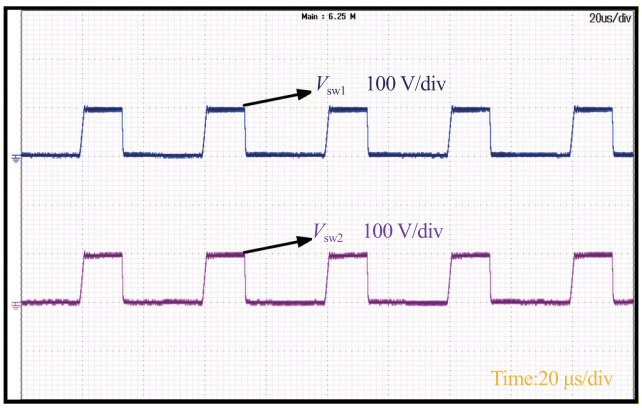

Fig. 10. Experimental results: V_{sw1} and V_{sw2}.

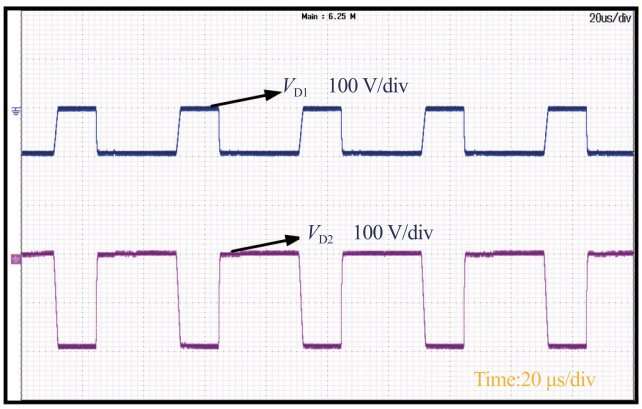

Fig. 11. Experimental results: V_{D1} and V_{D2}.

$$P_{\text{Loss, L}} = r_L I^2_{\text{Rms, L}} \tag{19}$$

$$P_{\text{(Total loss in inductor)}} = 0.5 \text{ W} \tag{20}$$

Capacitor Loss: The majority of power loss in the capacitors arises from their parasitic series resistance, which can be evaluated using the RMS current flowing through them.

$$P_{\text{Loss,C}} = r_C I^2_{\text{Rms, C}} \tag{21}$$

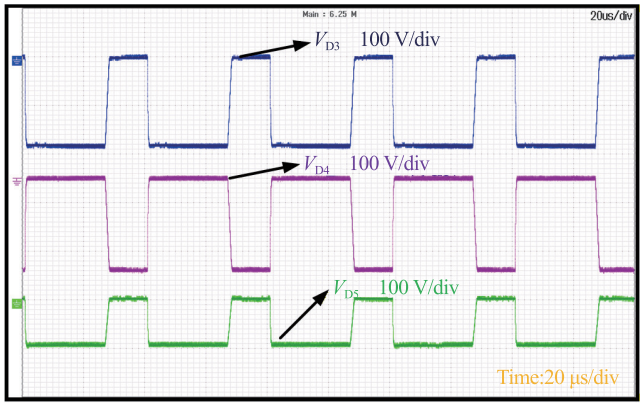

Fig. 12. Experimental results: V_{D3}, V_{D4}, and V_{D5}.

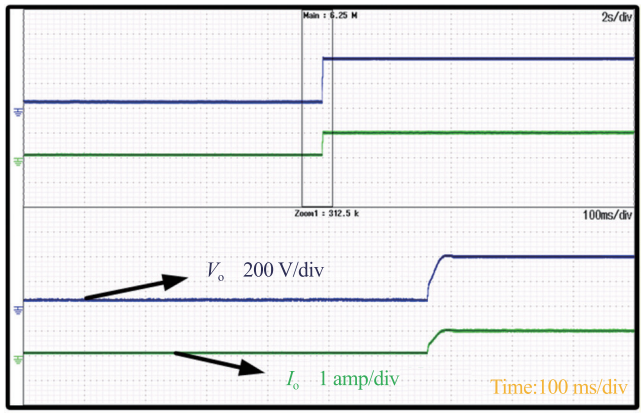

Fig. 13. Experimental results during closed loop operation: Initial operation.

$$P_{(\text{Total loss in capacitor})} = 7\ \text{W} \tag{22}$$

Switch Loss: The total power dissipation in the switch consists of both switching and conduction losses, which are evaluated using the RMS and average current flowing through the device.

$$P_{\text{Loss,sw}} = P_{\text{Switching,sw}} + P_{\text{conduction,sw}} \tag{23}$$

$$P_{\text{Loss, sw}} = 0.5F_s\,(t_r + t_f)\,I_{\text{Avg, sw}}\,V_{\text{sw, ON}} + r_{\text{sw}}I^2_{\text{Rms, sw}} \tag{24}$$

$$P_{(\text{Total losses in switches})} = 0.475\ \text{W} \tag{25}$$

Diode Loss: The overall power loss in diodes arises from the forward voltage drop and conduction loss, which depend on the internal resistance of the device. These losses can be quantified using the following equations.

$$P_{\text{Loss,D}} = P_{\text{Forward drop, D}} + P_{\text{conduction, D}} \tag{26}$$

$$P_{\text{Loss, D}} = V_{\text{FD}}\,I^2_{\text{Avg, D}} + r_{\text{D}}I^2_{\text{Rms, D}} \tag{27}$$

$$P_{(\text{Total losses in diodes})} = 5.68\ \text{W} \tag{28}$$

The overall losses of the converter are obtained as follows.

$$P_{\text{Losses}} = 13.66\ \text{W} \tag{29}$$

The above losses doesn't take miscellanies losses into account which is an important factor when it comes to practical matters. Therefore, the total loss in converter is

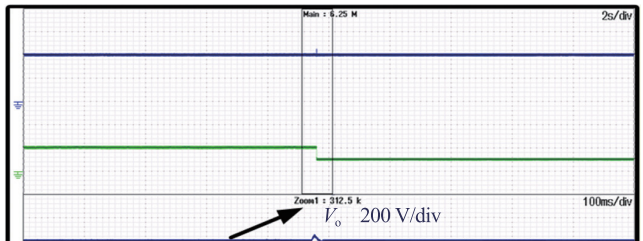

Fig. 14. Experimental results during closed loop operation: Step change in load operation.

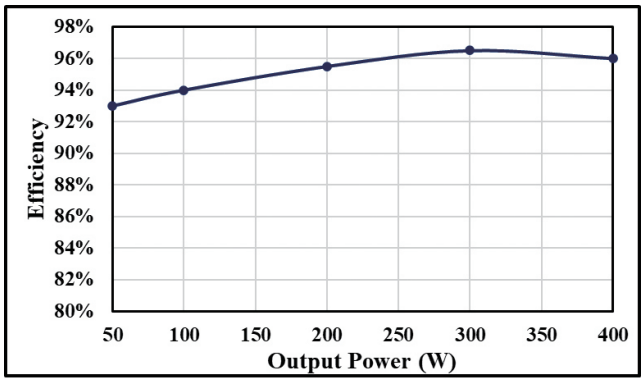

Fig. 15. Experimental efficiency vs output power.

$$P_{\text{Total losses}} = P_{\text{Losses}} + P_{\text{miscellanies loss}} = 13.66\ \text{W} + 3\ \text{W} \tag{30}$$

The converter efficiency is obtained as follows:

$$\eta_{\text{converter}} = \frac{400}{400 + 16.66} \times 100 = 96\% \tag{31}$$

Fig. 15 illustrates the experimental efficiency of the converter with a voltage gain of M =12.5. The highest experimental efficiency, 96.5 %, was achieved with a output power of 300 W with a voltage ratio of 12.5. Fig. 16 illustrates the power loss distribution at output power of 400 W, indicating that the capacitors experience the highest losses, followed by the diodes.

VII. Conclusion

This paper presents a comprehensive analysis of an enhanced non-isolated DC-DC converter with high voltage gain capability, designed for efficient power conversion. The proposed design offers several key advantages, including improved voltage gain, increased efficiency, and reduced inductor currents, enabling the use of components with lower ratings. In addition, it minimizes voltage and current stress on both diodes and switches, contributing to overall system reliability.

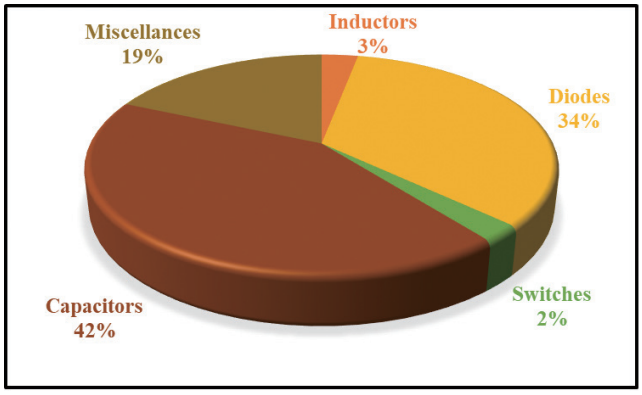

Fig. 16. Losses distribution at 400 W output power.

The converter features common grounding, ensures uniform current distribution among identical components, and effectively suppresses voltage oscillations across power switches. Experimental results validate the superior performance of the proposed converter compared to other designs documented in the literature. The duty cycle was carefully optimized to maintain a stable output power of 400 V, achieving an exceptional efficiency of 96.5% at 300 W with a voltage gain of 12.5.

References

[1] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[2] L. -S. Yang, T. -J. Liang, and J. -F. Chen, "Transformerless DC-DC converters with high step-up voltage dain," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.

[3] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Hybrid switched-inductor converters for high step-up conversion," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 3, pp. 1480–1490, Mar. 2015.

[4] M. A. Salvador, T. B. Lazzarin, and R. F. Coelho, "High step-up DC-DC converter with active switched-inductor and passive switched-capacitor networks," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5644–5654, Jul. 2018.

[5] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," in *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2959–2968, Jun. 2014.

[6] A. M. S. S. Andrade, T. M. K. Faistel, A. Toebe, and R. A. Guisso, "Family of transformerless active switched inductor and switched capacitor Ćuk DC-DC converter for high voltage gain applications," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 4, pp. 390–398, Oct. 2021.

[7] M. A. Salvador, J. M. de Andrade, T. B. Lazzarin, and R. F. Coelho, "Nonisolated high-step-up DC-DC converter derived from switched-inductors and switched-capacitors," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8506–8516, Oct. 2020.

[8] A. M. S. S. Andrade, T. M. K. Faistel, R. A. Guisso, and A. Toebe, "Hybrid high voltage gain transformerless DC-DC converter," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2470–2479, Mar. 2022.

[9] S. Gopinathan, V. S. Rao, and K. Sundaramoorthy, "Family of non-isolated quadratic high gain DC-DC converters based on extended capacitor-diode network for renewable energy source integration," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 5, pp. 6218–6230, Oct. 2022.

[10] M. Lakshmi and S. Hemamalini, "Nonisolated high gain DC-DC converter for DC microgrids," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1205–1212, Feb. 2018.

[11] V. Marzang, S. H. Hosseini, N. Rostami, P. Alavi, P. Mohseni, and S. M. Hashemzadeh, "A high step-up nonisolated DC-DC converter with flexible voltage gain," in *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10489–10500, Oct. 2020.

[12] B. Faridpak, M. Bayat, M. Nasiri, R. Samanbakhsh, and M. Farrokhifar, "Improved hybrid switched inductor/switched capacitor DC-DC converters," in *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3053–3062, Mar. 2021.

[13] Y. Tang, H. Tong, J. Kan, Y. Zhang, and K. Xu, "Symmetric dual-switch converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11955–11964, Nov. 2020.

[14] C. Cui, Y. Tang, Y. Guo, H. Sun, and L. Jiang, "High step-up switched-capacitor active switched-inductor converter with self-voltage balancing and low stress," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 10, pp. 10112–10128, Oct. 2022.

[15] Y. Zhang, C. Fu, M. Sumner, and P. Wang, "A wide input-voltage range quasi-Z-source Boost DC-DC converter with high-voltage gain for fuel cell vehicles," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 5201–5212, Jun. 2018.

[16] N. Elsayad, H. Moradisizkoohi, and O. Mohammed, "A new SEPIC-based step-up DC-DC converter with wide conversion ratio for fuel cell vehicles: Analysis and design," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 6390–6400, Aug. 2021.

[17] M. R. Mohammed, A. S. Al-Sumaiti, A. R. Beig, K. Al Hosani, and C. Wang, "A common grounded voltage quadrupler ASL/PSC hybrid converter with reduced voltage stress," in *IEEE Transactions on Industrial Electronics*, vol. 71, no. 5, pp. 4773–4784, May 2024.

[18] M. R. Mohammed, A. S. Al-Sumaiti, and A. R. Beig, "Hybrid active switched inductor DC-DC converter with common ground and suppressed voltage oscillation for fuel cell vehicles," in *IEEE Transactions on Transportation Electrification*, vol. 11, no. 1, pp. 3204–3214, Feb. 2025.

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