

Research on Wide-Range Core Loss Measurement Model and Method Based on DC Power Method

Qingbin CHEN, Wei QIU, Jinjiang LI, Qing HE, Xixian GUO, and Wei CHEN

Abstract—To address the engineering bottleneck of frequent recalibration in core loss measurement using the DC power method that caused by the narrow prediction range and low accuracy of existing inverter loss models, this paper proposes a novel wide-range calibration model. The model comprehensively incorporates multi-modal loss mechanisms, including hard- and soft-switching, as well as the dependence on duty cycle. By imposing physical constraints on the fitting parameters, a general model applicable to both asymmetric and symmetric pulse width modulation (PWM) excitations is established. Experimental results demonstrate that over a wide measurement range of 20–100 kHz switching frequency, 0.2–0.5 duty cycle, and 1.01–43.01 V input voltage, the proposed model requires only a single calibration to achieve an average relative error of 1.80%. Compared with existing methods, the maximum relative error is reduced by at least 16.27% and up to 59.07%.

Index Terms—Core loss, DC power method, inverter loss calibration model, wide-range measurement.

I. INTRODUCTION

At present, the mainstream methods for measuring core losses, both domestically and internationally, can be broadly classified into three categories: the AC power method [1]–[3], the calorimetric method [4]–[5], and the DC power method [6]–[9].

The AC power method is widely used due to its simplicity and ease of implementation. However, significant measurement errors arise under high impedance angle conditions. Although the impedance angle can be reduced by connecting parallel capacitors or series inductors to improve measurement accuracy [10], [11], this approach inevitably introduces additional losses associated with the added capacitive or inductive components, which are difficult to quantify accurately. Moreover, the AC power method is limited to sinusoidal excitation and is therefore incapable of evaluating core losses under pulse width modulation (PWM) excitation, which is commonly encountered

in magnetic components of practical power converter applications.

In theory, the calorimetric method is applicable to loss measurements under arbitrary excitation waveforms [12]–[14]. However, in practical implementations, not only the thermal medium but also auxiliary components such as stirrers and insulated containers absorb heat. Consequently, calculating losses solely based on the specific heat capacity of the thermal medium inevitably introduces measurement errors. In addition, achieving perfect thermal insulation is extremely challenging, and as the heating duration increases, a portion of the generated heat is gradually dissipated into the surrounding environment. Although the use of precision insulated containers can mitigate these errors to some extent, the calorimetric method remains unsuitable for the rapid and convenient measurement of core losses under PWM excitation commonly encountered in engineering applications, due to its multiple error sources, complex procedures, and time-consuming measurement process.

By contrast, the DC power method has been developed to overcome the limitations associated with the aforementioned measurement techniques effectively. This method employs a full-bridge inverter to convert a DC voltage source into symmetric or asymmetric PWM excitation with an adjustable duty cycle, which is applied to the magnetic core under test. By measuring the input power on the DC side and subtracting the power losses of the inverter itself, the core loss can be accurately determined.

The DC power method not only eliminates the measurement inaccuracies encountered by the AC power method under high impedance angle conditions, but also avoids the complexity and time-consuming nature of the calorimetric method. Moreover, it is well-suited for evaluating core losses under PWM excitation waveforms commonly encountered in practical engineering applications, thereby demonstrating significant practical applicability and engineering value.

In the DC power method, the accuracy of core loss measurement is highly dependent on the precision of inverter loss calibration. Specifically, the inverter losses must be subtracted from the total input power measured on the DC side to obtain the actual core loss. However, existing inverter loss calibration models under PWM excitation exhibit significant limitations. On the one hand, the hard-switching behavior of power semiconductor devices and the associated duty cycle dependent loss characteristics are typically neglected. On the other hand, during nonlinear fitting of the loss models, no physical constraints are imposed on the signs of the model parameters

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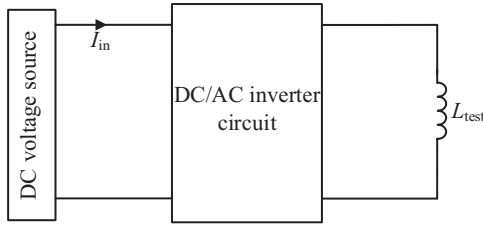


Fig. 1. Schematic diagram of the DC power method.

[15]–[19], which restricts both the prediction range and the achievable calibration accuracy.

As a result, when conducting wide-range core loss measurements, cumbersome and repetitive calibration procedures are required under different operating conditions, significantly reducing measurement efficiency and severely hindering the practical adoption of the DC power method. Therefore, although the International Electrotechnical Commission (IEC) has standardized the DC power method in IEC 63300–2023 released in 2023, this technique has not yet been widely applied in engineering practice due to the aforementioned technical bottlenecks.

To address the limitations of existing inverter loss models, this paper systematically investigates the loss characteristics of a full-bridge inverter operating under different switching modes, including complete soft switching, zero-voltage turn-on, and hard switching of the power semiconductor devices. During the nonlinear fitting process, physical constraints are imposed on the magnitudes of key model parameters to ensure physical consistency. Based on this analysis, a wide-range inverter loss calibration model that explicitly incorporates duty cycle variations is proposed and experimentally validated. Finally, the proposed model is compared with existing loss models, demonstrating its superior accuracy and advanced performance in wide-range core loss measurements.

II. WIDE-RANGE LOSS ANALYSIS AND MODELING OF AN INVERTER FOR DC POWER-BASED CORE LOSS MEASUREMENT

The DC power method employs a DC/AC inverter as the main circuit topology, enabling the generation of PWM excitation waveforms that are representative of those commonly encountered in practical power converter operating conditions. The principle of the DC power method is illustrated in Fig. 1 [20], [21].

A DC voltage source is converted by a DC/AC full-bridge inverter to generate PWM excitation waveforms with adjustable frequency, duty cycle, and amplitude, which are applied to the magnetic component under test, denoted as L_{test} . The loss of the magnetic component is obtained by measuring the input power on the DC side and subtracting the power losses of the DC/AC inverter. To reduce the measurement error of the DC input power, high-precision DC voltage and current meters are employed. Consequently, the measurement accuracy of the magnetic component loss is mainly determined by the calibration accuracy of the inverter losses.

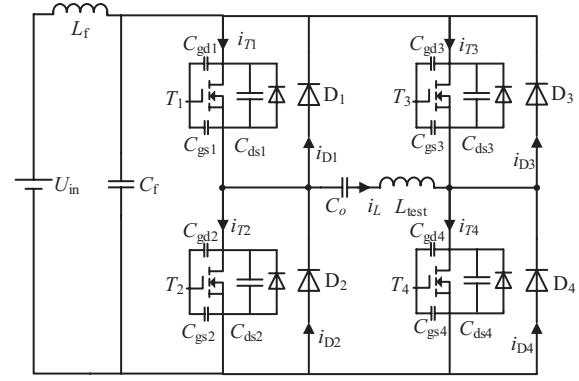


Fig. 2. Schematic diagram of the full-bridge inverter circuit.

The schematic diagram of the DC/AC full-bridge inverter considering parasitic parameters is shown in Fig. 2 [22], [23]. In this figure, U_{in} represents the DC voltage source, C_f is the filter capacitor, and C_o is the DC-blocking capacitor. T_1 – T_4 denote the power MOSFETs, while D_1 – D_4 are the corresponding antiparallel diodes. C_{gd1} – C_{gd4} , C_{gs1} – C_{gs4} , and C_{ds1} – C_{ds4} represent the parasitic gate-to-drain, gate-to-source, and drain-to-source capacitances of the MOSFET, respectively.

A. Inverter Loss Analysis and Modeling Under Asymmetric PWM Excitation

1) Inverter Loss Analysis With MOSFET Operating in Complete Soft-Switching Mode

When the MOSFETs operate under complete soft-switching conditions, i.e., zero-voltage switching (ZVS) or zero-current switching (ZCS) is achieved during both turn-on and turn-off transitions, the switching losses of the MOSFETs in the full-bridge inverter can be neglected. Under this operating condition, the dominant loss components of the inverter are the ohmic losses in the circuit and the equivalent series resistance (ESR) losses of the capacitive elements. The total inverter loss in this case can be expressed by (1).

$$P_{\text{ex}} = k \cdot I_{\text{pk}}^2 \quad (1)$$

In (1), P_{ex} denotes the inverter loss, I_{pk} is the peak current flowing through the MOSFET, and k is a positive parameter to be determined.

2) Inverter Loss Analysis With MOSFET Operating Under Zero-Voltage Turn-on

To develop an accurate inverter loss calibration model, the losses occurring during each switching transition of the MOSFET must be analyzed in detail. Fig. 3 illustrates the voltage and current waveforms of the relevant devices when the MOSFET operates under ZVS. The waveform duration in the figure has been adjusted for clarity in explaining the losses generated during the dynamic switching process and does not represent the actual operating time.

For the sake of analyzing dynamic losses, it is assumed that all MOSFETs are of the same model, manufacturing variations in device parameters are neglected, and the parasitic capacitances

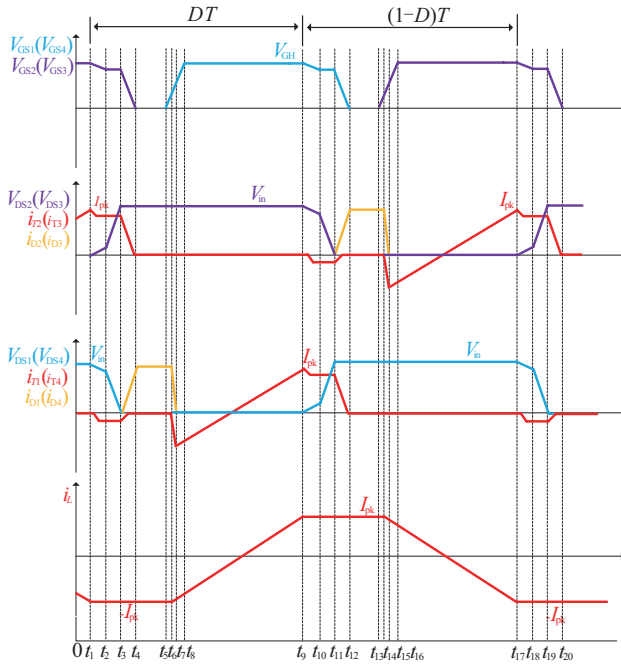


Fig. 3. Voltage and current waveforms of main devices in the inverter under asymmetric PWM excitation with zero-voltage turn-on.

of all MOSFETs are considered equal. Furthermore, the inductor current is assumed to remain constant during the charging and discharging of the capacitors.

In Fig. 3, $V_{GS1}(V_{GS4})$ and $V_{GS2}(V_{GS3})$ denote the gate-to-source voltage waveforms of $T_1(T_4)$ and $T_2(T_3)$, respectively. $i_{T1}(i_{T4})$ and $i_{T2}(i_{T3})$ represent the currents flowing through $T_1(T_4)$ and $T_2(T_3)$. $i_{D1}(i_{D4})$ and $i_{D2}(i_{D3})$ correspond to the currents through the antiparallel diodes $D_1(D_4)$ and $D_2(D_3)$ and i_L denotes the current of the inductor under test.

During the interval t_1-t_2 , the drain-to-source voltage of the MOSFETs rises gradually, but at t_2 , V_{DS2} and V_{DS3} have increased only slightly. Hence, the losses in this period can be neglected.

From t_2-t_3 , a portion of the current charges C_{ds2} and C_{ds3} , causing an increase in the drain-to-source voltages V_{DS2} and V_{DS3} . This portion of current is defined as $c \cdot I_{pk}$. The turn-off losses of T_2 and T_3 , together with the discharge losses of the drain-to-source capacitances of T_1 and T_4 , can be expressed by (2), where k_1 is a positive parameter to be determined. The duration of this interval, $\Delta t_2(t_3-t_2)$, can be calculated using (3).

$$W_1 = 2 \int_{t_2}^{t_3} i_{T2} \cdot V_{ds2} dt + 2 \int_{t_2}^{t_3} i_{T1} \cdot V_{ds1} dt = k_1 \cdot V_{in}^2 \quad (2)$$

$$\Delta t_2 = \frac{C_{ds} \cdot V_{in}}{c \cdot I_{pk}} \quad (3)$$

The losses during the interval t_3-t_4 are expressed by (4), where W_2 includes the partial turn-off losses of T_2 and T_3 as well as the conduction losses of the antiparallel diodes.

$$\begin{aligned} W_2 &= 2 \int_{t_3}^{t_4} V_{in} \cdot \frac{c_1 \cdot I_{pk}}{\Delta t_3} \cdot (t_4 - t) dt + 2 \int_{t_3}^{t_4} i_{D1} \cdot v_{D1} dt \\ &= k_2 \cdot V_{in} \cdot I_{pk} - k_3 \cdot I_{pk}^2 + \frac{k_4 \cdot I_{pk}^2 \cdot \ln(I_{pk})}{V_{in}} - k_5 \frac{I_{pk}^2}{V_{in}} \end{aligned} \quad (4)$$

For the sake of simplifying the calculation, it is assumed that the current i_{T3} flows through the parasitic inductance L_{p3} of T_3 and decreases linearly. Under this assumption, the duration of this interval, $\Delta t_3(t_4-t_3)$ can be calculated as

$$\Delta t_3 = \frac{L_{p3} \cdot c_1 \cdot I_{pk}}{V_{in}} \quad (5)$$

In (4) and (5), k_2-k_5 are positive parameters to be determined.

During the interval t_4-t_5 , the inductor current flows entirely through the diodes for freewheeling. The losses in this period consist solely of the diode conduction losses, which can be calculated as

$$W_3 = 2 \int_{t_4}^{t_5} i_{D1} \cdot v_{D1} dt = I_{pk} \cdot V_{D1} \cdot \Delta t_4 \quad (6)$$

The dead time t_d during the interval t_1-t_5 is set via the host computer and can therefore be considered a known parameter.

$$\Delta t_4 = t_d - \Delta t_1 - \Delta t_2 - \Delta t_3 \quad (7)$$

By substituting Δt_4 into (6), (8) can be obtained, where k_6-k_{11} are positive parameters to be determined.

$$\begin{aligned} W_3 &= k_6 I_{pk} \ln(I_{pk}) - k_7 V_{in} \ln(I_{pk}) \\ &\quad - k_8 \frac{I_{pk}^2}{V_{in}} \ln(I_{pk}) - k_9 I_{pk} + k_{10} V_{in} + k_{11} \frac{I_{pk}^2}{V_{in}} \end{aligned} \quad (8)$$

During the interval t_5-t_6 , the losses consist solely of the diode conduction losses, which can be expressed by (9).

$$W_4 = 2 \int_{t_5}^{t_6} i_{D1} \cdot v_{D1} dt = I_{pk} \cdot V_{D1} \cdot \Delta t_5 \quad (9)$$

The duration of this interval, $\Delta t_5(t_6-t_5)$ can be calculated as

$$\Delta t_5 = \frac{C_{gs} + C_{ds}}{I_g} V_{th} \quad (10)$$

Finally, the diode conduction loss during this interval can be expressed by (11), where k_{12} and k_{13} are positive parameters to be determined.

$$W_4 = k_{12} \cdot I_{pk} \ln(I_{pk}) + k_{13} \cdot I_{pk} \quad (11)$$

During the interval t_6-t_7 , T_1 and T_4 operate under zero-voltage turn-on, and their conduction losses can be considered negligible.

During the interval t_7-t_9 , the currents i_{T1} and i_{T4} increase from $-I_{pk}$ to I_{pk} . During this period, MOSFET losses are primarily dominated by conduction losses, which can be expressed as.

$$W_5 = 2 \int_{t_7}^{t_9} \left[-I_{pk} + \frac{2I_{pk}}{\Delta t_6} \cdot (t - t_7) \right]^2 R_{ds} dt \quad (12)$$

Here, R_{ds} denotes the MOSFET on-resistance, and $\Delta t_6(t_9-t_7)$ can be calculated as

$$\Delta t_6 = DT - t_d - \Delta t_5 \quad (13)$$

The simplified MOSFET conduction loss during this interval can be expressed by (14), where k_{14} and k_{15} are positive parameters to be determined.

$$W_5 = k_{14} \cdot D \cdot T I_{pk}^2 + k_{15} \cdot I_{pk}^2 \quad (14)$$

The loss analysis during the interval t_9 – t_{10} is similar to that of the interval t_1 – t_2 . The losses during t_{10} – t_{11} are expressed similarly to W_1 , and those during t_{11} – t_{12} are expressed similarly to W_2 . subsequent intervals follow the same pattern.

During the interval t_{15} – t_{17} , the loss analysis is consistent with that of W_5 ; however, the duration $\Delta t_7(t_{17}$ – $t_{15})$ is calculated differently from the interval $\Delta t_6(t_9$ – $t_7)$, as shown in (15).

$$\Delta t_7 = (1-D)T - t_d - \Delta t_5 \quad (15)$$

During this interval, the conduction losses of T_2 and T_3 can be expressed by (16), where k_{16} and k_{17} are positive parameters to be determined.

$$\begin{aligned} W_6 &= 2 \int_{t_{15}}^{t_{17}} \left[-I_{pk} + \frac{2 \cdot I_{pk}}{\Delta t_6} \cdot (t - t_7) \right]^2 R_{ds} dt \\ &= k_{16} \cdot (1-D)T \cdot I_{pk}^2 + k_{17} \cdot I_{pk}^2 \end{aligned} \quad (16)$$

Therefore, under zero-voltage turn-on of the MOSFETs, the average power loss over one period under asymmetric PWM excitation can be expressed by (17).

$$\begin{aligned} P_{ex} &= [(W_1 + W_2 + W_3 + W_4) \cdot 2 + (W_5 + W_6)] \cdot f \\ &= \lambda_1 I_{pk}^2 f + \lambda_2 V_{in}^2 f + \lambda_3 V_{in} I_{pk} f \\ &\quad + \lambda_4 \frac{I_{pk}^2 \ln(I_{pk})}{V_{in}} f + \lambda_5 \frac{I_{pk}^2}{V_{in}} f \\ &\quad + \lambda_6 I_{pk} \ln(I_{pk}) f + \lambda_7 V_{in} \ln(I_{pk}) f \\ &\quad + \lambda_8 I_{pk} f + \lambda_9 V_{in} f + \lambda_{10} D I_{pk}^2 + \lambda_{11} I_{pk}^2 \end{aligned} \quad (17)$$

In (17), coefficients λ_1 – λ_{11} are parameters to be determined, where the signs of λ_1 , λ_4 , λ_5 , λ_8 and λ_{10} are to be determined, λ_7 is negative, and the remaining coefficients are positive. V_{in} denotes the DC input voltage, I_{pk} is the peak current, f is the operating frequency, and D is the duty cycle.

3) Inverter Loss Analysis With MOSFET Operating Under Hard-Switching Conduction

As the operating frequency increases, the MOSFET cannot maintain soft-switching throughout the entire cycle and therefore operates in hard-switching mode. The measured turn-on and turn-off voltage waveforms of T_1 under this condition are shown in Figs. 4 and 5.

Based on the measured waveforms of the MOSFET under hard-switching conditions with asymmetric PWM excitation, the voltage and current waveforms of the relevant components

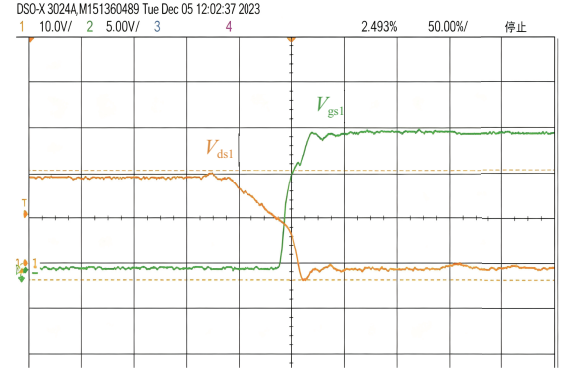


Fig. 4. Voltage waveform of T_1 turn-on.

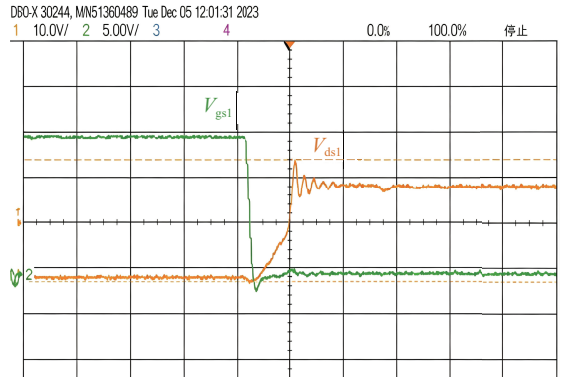


Fig. 5. Voltage waveform of T_1 turn-off.

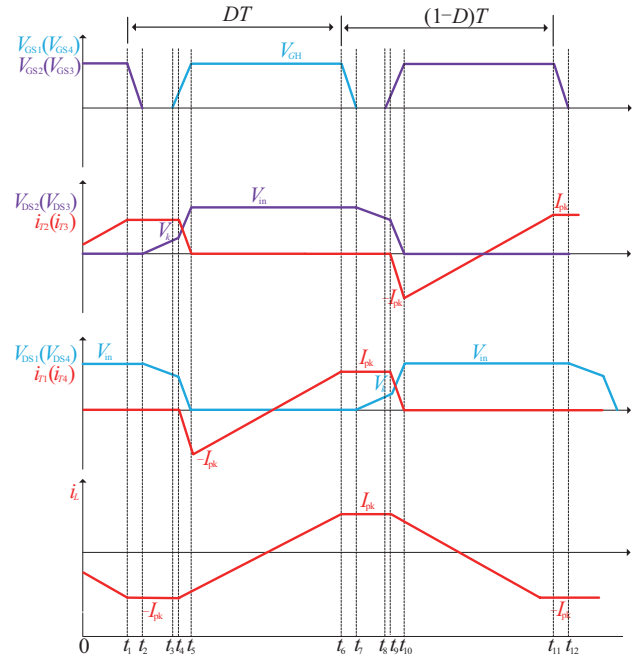


Fig. 6. Voltage and current waveforms of main devices in the inverter during hard switching under asymmetric PWM excitation.

in the inverter circuit are illustrated in Fig. 6.

In Fig. 6, $V_{gs1}(V_{gs4})$ and $V_{gs2}(V_{gs3})$ represent the gate-to-source voltage waveforms of $T_1(T_4)$ and $T_2(T_3)$, respectively.

$i_{T1}(i_{T4})$ and $i_{T2}(i_{T3})$ denote the currents flowing through $T_1(T_4)$ and $T_2(T_3)$, and i_L is the current of the inductor under test.

When the MOSFETs operate under hard-switching conditions, the analysis method is similar to that of soft switching, with a focus on the turn-on and turn-off losses of the MOSFETs.

At t_2 , the drain-to-source parasitic capacitances C_{ds2} and C_{ds3} of T_2 and T_3 begin to charge slowly, resulting in an increase of V_{DS2} and V_{DS3} . According to Kirchhoff's law, the drain-to-source voltages V_{DS1} and V_{DS4} of T_1 and T_4 decrease correspondingly, and a portion of the inductor current flows through T_1 and T_4 to discharge C_{ds1} and C_{ds4} .

At t_4 , V_{DS2} and V_{DS3} rise to V_k , at which point T_1 and T_4 just begin to turn on, and the MOSFET drain-to-source capacitances start charging and discharging at a faster rate. Therefore, the turn-off losses of T_2 and T_3 during the interval t_2 – t_5 can be expressed by (18).

$$\left\{ \begin{aligned} W_1 &= 2 \int_{t_2}^{t_4} i_{T2} \cdot V_{DS2} dt + 2 \int_{t_4}^{t_5} i_{T3} \cdot V_{DS3} dt \\ &= 2 \int_{t_2}^{t_4} I_{pk} \cdot \frac{V_k}{\Delta t_2} \cdot (t - t_2) dt \\ &\quad + \int_{t_2}^{t_4} I_{pk} \cdot 2 \int_{t_4}^{t_5} \frac{I_{pk}}{\Delta t_4} \cdot (t - t_4) \cdot \frac{V_{in} - V_k}{\Delta t_4} \cdot (t - t_4) dt \\ V_k &= \frac{I_{pk} \cdot \Delta t_2}{C_{ds}} \end{aligned} \right. \quad (18)$$

In (18), V_k denotes the drain-to-source voltage of T_2 and T_3 .

Given the known dead time, the duration of the interval $\Delta t_2(t_2$ – $t_4)$ can be calculated using (19), where Δt_1 , Δt_3 , and Δt_4 represent the durations from the current moment to the next switching instant, and k_1 , k_2 , and k_3 are the proportionality coefficients of the gate drive currents.

$$\left\{ \begin{aligned} \Delta t_1 &= \frac{C_{gs} \cdot V_{GH}}{k_1 I_g} \\ \Delta t_2 &= t_d - \Delta t_1 + \Delta t_3 \\ \Delta t_3 &= \frac{C_{gs} \cdot V_{th}}{k_2 I_g} \\ \Delta t_4 &= \frac{C_{gs} \cdot (V_{GH} - V_{th})}{k_3 I_g} \end{aligned} \right. \quad (19)$$

After simplification, the loss expression for this interval can be expressed by (20), where a_1 – a_2 are positive parameters to be determined.

$$W_1 = a_1 \cdot I_{pk}^2 + a_2 \cdot I_{pk} \cdot V_{in} \quad (20)$$

At t_4 , the gate drive voltages of T_1 and T_4 rise to the threshold voltage V_{th} , causing T_1 and T_4 to turn on and transition from the cutoff region to the linear region. At this moment, the drain-to-source capacitances of T_1 and T_4 , as well as T_2 and T_3 , undergo faster charging and discharging. Therefore, during the interval t_4 to t_5 , the turn-on loss of T_1 and T_4 can be approximated as the

energy discharged from their drain-to-source capacitances C_{ds1} and C_{ds4} . The corresponding expression for the turn-on loss is given by (21).

$$\left\{ \begin{aligned} W_2 &= \frac{1}{2} C_{DS} (V_{in} - V_k)^2 = \frac{1}{2} C_{DS} \left(V_{in} - \frac{I_{pk} \cdot \Delta t}{C_{DS}} \right)^2 \\ V_k &= \frac{I_{pk} \cdot \Delta t_2}{C_{ds}} \end{aligned} \right. \quad (21)$$

The duration of this interval can be calculated as

$$\Delta t_4 = \frac{C_{gs} \cdot (V_{GH} - V_{th})}{k_3 I_g} \quad (22)$$

After simplification, the turn-on loss for this interval can be expressed by (23), where a_3 – a_5 are positive parameters to be determined.

$$W_2 = a_3 V_{in}^2 - a_4 V_{in} I_{pk} + a_5 I_{pk}^2 \quad (23)$$

In summary, under hard-switching conditions, the MOSFET switching losses over one operating period can be expressed by

$$\begin{aligned} P_{switch} &= [2(W_1 + W_2)]f \\ &= \gamma_1 \cdot V_{in}^2 \cdot f + \gamma_2 \cdot I_{pk}^2 \cdot f + \gamma_3 \cdot V_{in} \cdot I_{pk} \cdot f \end{aligned} \quad (24)$$

In (24), coefficients γ_1 – γ_3 are parameters to be determined, where the sign of γ_2 is undetermined and the remaining coefficients are positive. V_{in} denotes the DC input voltage, I_{pk} is the peak current flowing through the MOSFET, and f is the switching frequency.

4) Lumped Inverter Loss Model Under Asymmetric PWM Excitation

Based on the above analysis of device losses in each stage, a lumped inverter loss model under asymmetric PWM excitation is proposed. This model accounts for the DC/AC inverter losses of MOSFETs operating in different states. The calibrated full-bridge inverter loss model under asymmetric PWM excitation is presented in (25).

$$\begin{aligned} P_{ex} &= a_1 I_{pk}^2 f + a_2 V_{in}^2 f + a_3 V_{in} I_{pk} f \\ &\quad + a_4 \frac{I_{pk}^2 \ln(I_{pk})}{V_{in}} f + a_5 \frac{I_{pk}^2}{V_{in}} f \\ &\quad + a_6 I_{pk} \ln(I_{pk}) f + a_7 V_{in} \ln(I_{pk}) f \\ &\quad + a_8 I_{pk} f + a_9 V_{in} f + a_{10} D I_{pk}^2 + a_{11} I_{pk}^2 \end{aligned} \quad (25)$$

In (25), coefficients a_1 – a_{11} are the parameters to be determined for the full-bridge inverter loss calibration model under asymmetric PWM excitation. Among them, the signs of coefficients a_3 , a_4 , a_5 , a_8 , and a_{10} are undetermined, a_7 is negative, and the remaining coefficients are positive.

During the nonlinear fitting of the inverter loss calibration model, it is essential to ensure that the signs of all coefficients

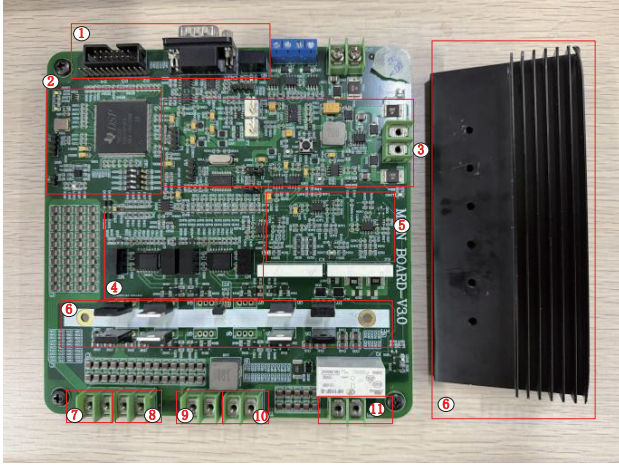


Fig. 8. Photograph of the inverter circuit board.

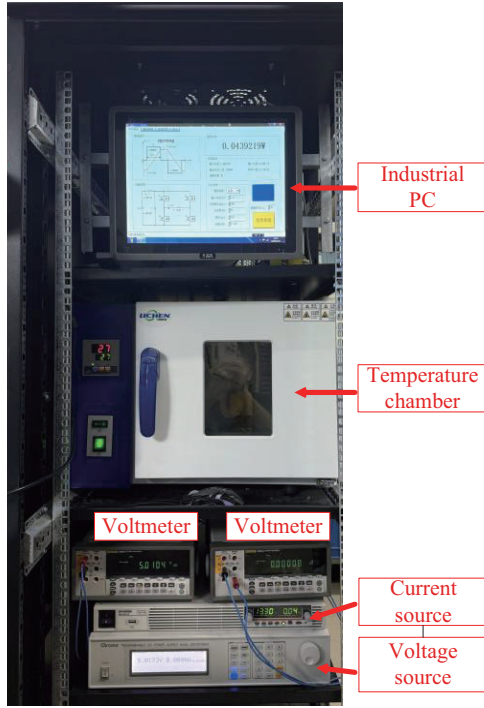


Fig. 9. Integrated wide-range core loss measurement platform.

design, an integrated wide-range core loss measurement platform is constructed, as shown in Fig. 9, where the inverter circuit board is placed behind the industrial computer.

The DC/AC inverter of the measurement platform is capable of generating PWM excitation waveforms with arbitrary voltage, duty cycle, and frequency. Experimental results indicate that the inverter meets the requirements for wide-range core loss measurements, as shown in Fig. 10.

B. Accurate Measurement and Calibration of Inverter Losses Under Asymmetric and Symmetric PWM Excitations

To accurately calibrate the losses of the full-bridge inverter, a uniformly wound air-core inductor with an inductance of

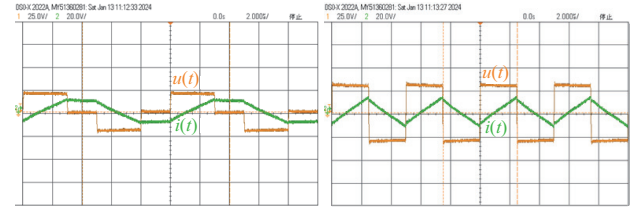
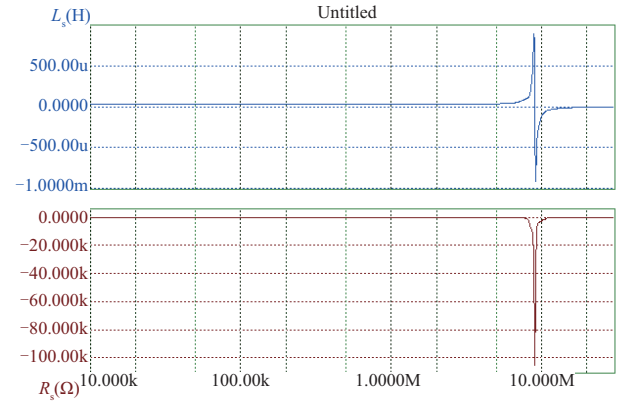


Fig. 10. Oscilloscope measurements of voltage and current waveforms under symmetric and asymmetric PWM.

Fig. 11. Optimized air-core inductor (24.6 μ H) for improved calibration accuracy.Fig. 12. Impedance characteristics of the 24.62 μ H air-core inductor.

24.62 μ H was employed, as shown in Fig. 11. To improve calibration accuracy, the inductor was optimized by adopting a toroidal circular cross-section, which maximizes the winding cross-sectional area for a given wire length. Since the impedance angle of an air-core inductor is proportional to the winding cross-sectional area and inversely proportional to the winding length, this design effectively increases the impedance angle and reduces the AC resistance. Consequently, the proportion of inverter losses in the total measured losses is significantly increased, thereby minimizing potential errors when deducting the inductor winding losses.

In Fig. 12, experimental results indicate that after optimization, the inverter losses account for approximately 67% of the total losses during calibration, significantly improving the accuracy and reliability of the calibration data. Furthermore, impedance analyzer measurements indicate that the resonant frequency of the inductor is approximately 9 MHz, which is far above the maximum operating frequency of the measurement system, 100 kHz. This demonstrates that the inductor is fully suitable for calibrating full-bridge inverter losses.

The losses of the full-bridge inverter are obtained by subtracting the winding losses of the air-core inductor from the

TABLE II
NONLINEAR FITTING PARAMETERS OF THE INVERTER LOSS MODEL

Undetermined coefficient	Loss model of the device	
	Asymmetric PWM waves	Symmetric PWM waves
a1	2.66E-07	3.42E-07
a2	2.99E-21	3.10E-10
a3	1.11E-08	2.29E-26
a4	-2.57E-07	-7.27E-07
a5	1.15E-06	1.25E-06
a6	1.51E-07	1.95E-07
a7	-9.49E-09	-9.01E-09
a8	-9.19E-08	-2.21E-07
a9	1.06E-20	1.21E-08
a10	-9.91E-03	-3.23E-01
a11	7.37E-02	2.31E-01

measured input power. Since the air-core inductor has no core losses, its winding losses are determined using a high-precision impedance analyzer combined with current Fourier decomposition.

The measured losses of the inverter setup under asymmetric and symmetric PWM excitations are used as nonlinear fitting points. The parameter ranges are frequency 20–100 kHz with a step of 20 kHz, duty cycle 0.2–0.5 with a step of 0.1, and input voltage 1.01–43.01 V. Based on these data, the unknown coefficients of the proposed model are identified, as summarized in Table II. The coefficients of determination (R^2) for the nonlinear fitting under asymmetric and symmetric PWM excitations are 0.9990 and 0.9995, respectively, indicating that the proposed model exhibits excellent agreement with the measured inverter losses.

Furthermore, the measured losses under asymmetric and symmetric PWM excitations with parameter ranges of frequency 30–90 kHz with a step of 20 kHz, duty cycle 0.25–0.45 with a step of 0.1, and input voltage 1.02–33.02 V are selected as prediction points to validate the accuracy of the proposed model further.

IV. ACCURACY VERIFICATION OF INVERTER LOSS MODELS UNDER ASYMMETRIC AND SYMMETRIC PWM EXCITATIONS AND COMPARISON WITH EXISTING MODELS

Figs. 13–15 present the accuracy evaluation results of the wide-range full-bridge inverter loss model based on the least-squares method, where the prediction performance of the model is analyzed under variations in duty cycle, switching frequency, and input voltage. For duty cycle and frequency, multiple measurement points with identical parameters are used, and the mean relative error (MRE) is adopted as the evaluation metric. For the input voltage, the MRE curve is plotted with a step of 1 V. The results indicate that the model predictions agree well with the measured values under both asymmetric and symmetric PWM excitations. Specifically, within the duty cycle range of 0.2–0.5, the maximum MREs under asymmetric and symmetric PWM excitations are 2.3381% and 2.7534%,

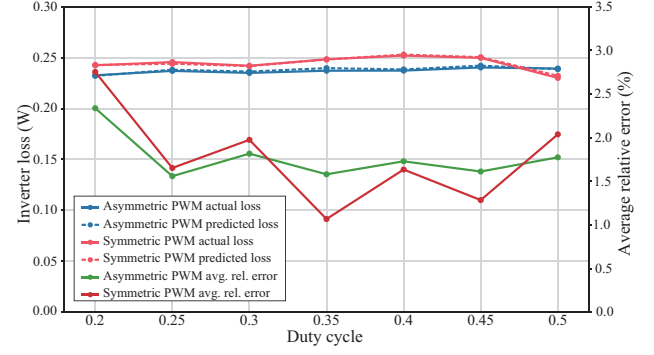


Fig. 13. Model accuracy variation with duty cycle under PWM excitation.

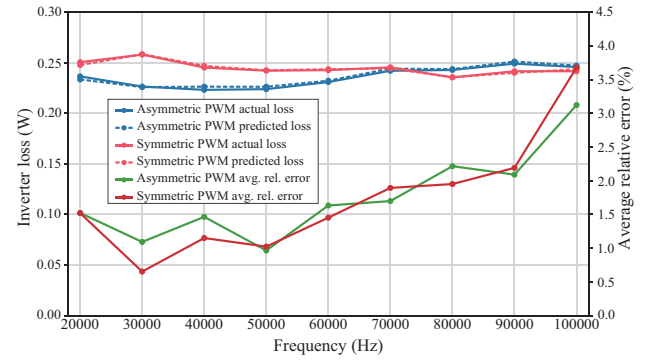


Fig. 14. Model accuracy variation with frequency under PWM excitation.

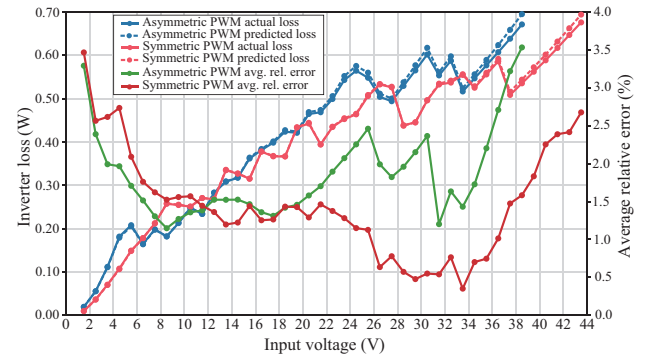


Fig. 15. Accuracy of the proposed model under PWM excitation as a function of input voltage.

respectively. Within the frequency range of 20–100 kHz, the corresponding maximum MREs are 3.1211% and 3.6772%. Within the input voltage range of 1.01–43.01 V, the maximum MREs are 3.5312% and 3.4653%. These results verify the accuracy and robustness of the proposed model over a wide measurement range.

Figs. 16 and 17 compare the maximum relative error of the proposed model with those of the models reported in [16] and [17] under both asymmetric and symmetric PWM excitations, as functions of duty cycle and switching frequency. The results indicate that the model in [16] exhibits severe error fluctuations, with maximum MREs reaching 73.56% and 74.07% under symmetric and asymmetric PWM, respectively. The model in [17] shows maximum MREs of 58.40% and 31.27%,

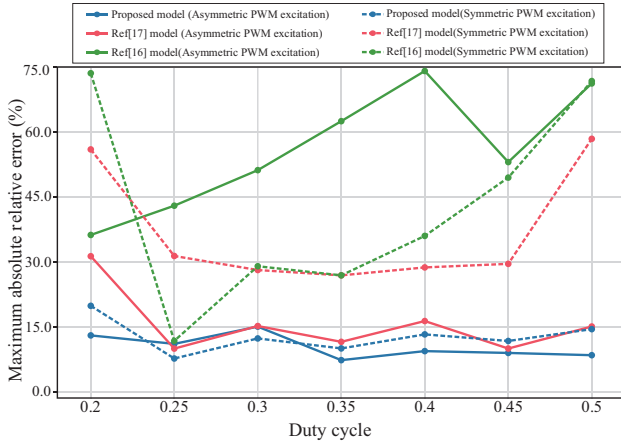


Fig. 16. Model accuracy comparison with duty cycle under PWM excitations.

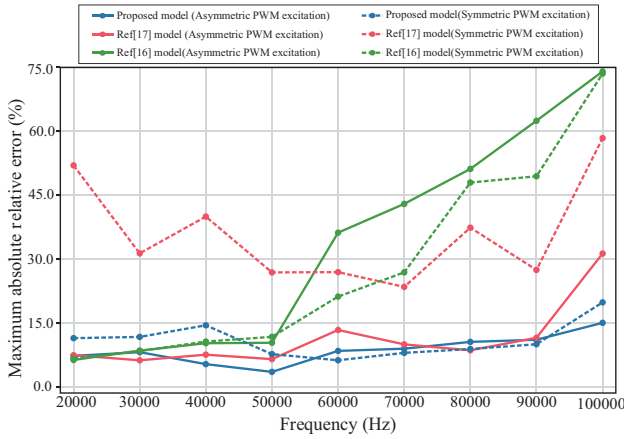


Fig. 17. Model accuracy comparison with frequency under PWM excitations.

demonstrating relatively poor stability. In contrast, the proposed model achieves maximum MREs of only 19.81% and 15.00% under the two PWM excitations, maintaining low errors across a wide operating range and demonstrating a clear advantage in accuracy.

Figs. 18 and 19 further illustrate the scatter distribution of relative errors for the three models as the input voltage varies. The models reported in [16] and [17] show significant error increases near the low-and high-voltage boundaries, with maximum relative errors reaching 74.07% and 58.40%, respectively, and overall higher errors under symmetric PWM. In contrast, the proposed model exhibits only a slight increase at the low-voltage end, with overall errors maintained below 20% and most measurement points below 5%, demonstrating excellent robustness.

V. CONCLUSION

Accurate measurement of core losses using the DC power method requires precise deduction of the losses of the full-bridge inverter. However, existing inverter loss models suffer from insufficient accuracy and limited ability to predict over a wide operating range. To address these issues, this paper proposes an improved model for inverter losses.

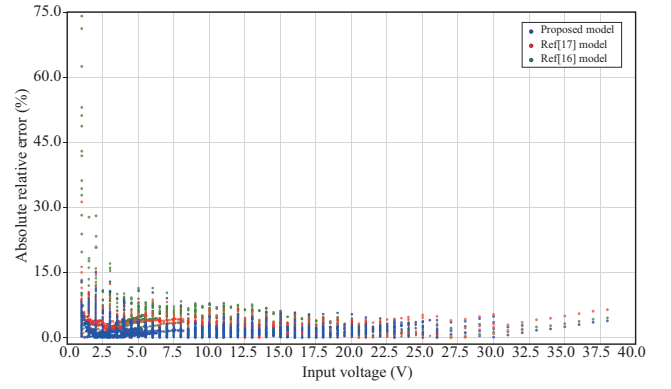


Fig. 18. Scatter plot of relative errors versus input voltage under asymmetric PWM excitation.

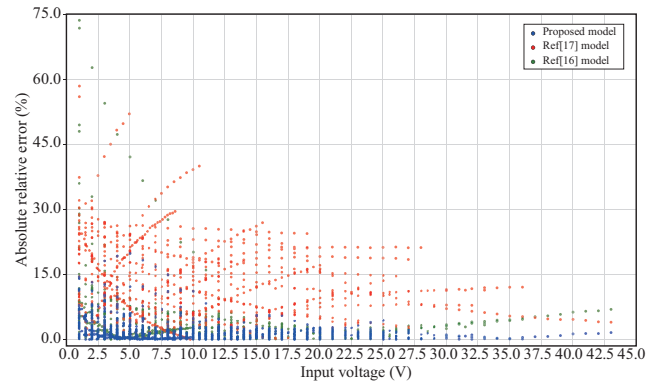


Fig. 19. Scatter plot of relative errors versus input voltage under symmetric PWM excitation.

The proposed model innovatively accounts for three operating modes of the MOSFETs in the full-bridge inverter under varying duty cycles: fully soft switching, zero-voltage turn-on, and hard switching. During the nonlinear fitting process, physical constraints are applied to the undetermined parameters, which effectively enhances the predictive accuracy and applicability of the model. Consequently, the proposed model significantly improves the accuracy and convenience of core loss measurements using the DC power method over a wide measurement range, providing a reliable solution for engineering applications.

Experimental results indicate that the proposed model can achieve high-accuracy prediction of full-bridge inverter losses over a wide range of duty cycles (0.2–0.5), input voltages (1.01–43.01 V), and operating frequencies (20–100 kHz). Under asymmetric and symmetric PWM excitations, the MREs are 3.5312% and 3.4653%, respectively. Compared with existing models, the proposed model demonstrates a clear accuracy advantage: under asymmetric PWM excitation, the maximum relative error is 15.00%, representing reductions of 59.07% and 16.27% relative to the models in [16] and [17], respectively. Under symmetric PWM excitation, the maximum relative error is 19.81%, corresponding to reductions of 53.75% and 38.59% relative to [16] and [17].

In summary, the proposed high-accuracy, wide-range full-bridge inverter loss model provides crucial support for wide-

range core loss measurements using the DC power method, thereby enhancing the convenience, precision, and effectiveness of the measurement approach.

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