

Near-Field Coupling Analysis and Modeling of the Input Plug on EMI Performance in Power Delivery Adapter

Qingbin CHEN, Zirui QIAN, Yujie LAN, Qing HE, and Wei CHEN

Abstract—With the continuous enhancement of power density in power delivery (PD) adapters, devices are positioned in close proximity to each other. Consequently, the proximity raises the concern for electromagnetic interference (EMI) due to magnetic near-field coupling effects, making EMI mitigation a priority in PD adapters. This paper addresses potential near-field couplings within a PD adapter and introduces a differential-mode (DM) EMI circuit model that accounts for near-field coupling effects. The magnetic field coupling between high-frequency (HF) power printed circuit board (PCB) loops and the input plug loop is identified as the pivotal factor affecting the differential-mode EMI noise. By electromagnetic field theory, a mathematical model is established for near-field coupling between the power PCB loops and the input plug loop. The model calculations and simulation examine the impact of power PCB loop dimension parameters. Ultimately, this study proposes three primary PCB layout design approaches for both single-sided and double-sided PCBs to mitigate near-field coupling effects. Empirical results validate the accuracy and applicability of the theoretical analysis.

Index Terms—Differential-mode EMI, input plug loop, near-field coupling, PCB loop.

I. INTRODUCTION

WITH the increase in switching frequency of power electronic devices and advancements in packaging technology, the power density of power delivery (PD) adapters has been significantly improved, which has also led to increasingly smaller distances between components. This, in turn, has caused more severe electromagnetic interference (EMI) issues.

EMI filters are widely used to suppress conducted EMI noise in power electronic systems. The attenuation characteristics of their passive components may be affected by near-field coupling. Specifically, the near-field coupling effects of EMI filters can be categorized into the near-field coupling between magnetic power components and EMI filters, as well as the

near-field coupling inside the filters [1]–[6]. The internal coupling of the filter can be further divided into magnetic field coupling and electric field coupling.

Near-field coupling directly couples noise signals to the linear impedance stabilization network (LISN) through magnetic or electric fields, bypassing the EMI filter and thereby degrading the filter's performance. Therefore, the accurate characterization and reasonable control of near-field coupling between components are of great significance for studying the electromagnetic compatibility (EMC) characteristics of power electronic systems [7]–[9].

Previous studies have focused on reducing the near-field couplings between magnetic power components and EMI filters. Through the analysis of the sensitivity of common mode choke (CMC) to the stray magnetic distribution generated by the power factor correction (PFC) choke, a differential-mode (DM) circuit model that incorporates the magnetic field coupling effect is built up, and few methods are proposed for mitigating magnetic coupling in [10]. Further, the magnetic field coupling between two critical components in switching-mode power converters, planar transformer, and common mode (CM) choke coil, is discussed in [11]. Additionally, to counteract the effects of magnetic near-field coupling and mitigate EMI noise, three near-field coupling reduction techniques are proposed, including layout design, magnetic shielding, and the stacked CMC structure.

Near-field coupling inside the EMI filter also has a significant impact on EMI issues. It is worth noting that [12] points out that the magnetic coupling inside the EMI filter has no effect on the CM performance of the EMI filter, but only affects its DM performance. The influence of parasitic parameters on the high-frequency (HF) attenuation characteristic of the EMI filter have been investigated in [13]. [14] proposes a method for extracting all coupling parameters in a single-phase EMI filter and points out that in a one-stage EMI filter, the coupling between X-capacitors and the coupling between capacitors and inductors have a significant impact on the filter performance. In a two-stage EMI filter, the coupling between CMC has a great influence on low-frequency performance because it may change the corner frequency of the filter. Meanwhile, the coupling between capacitors has a significant impact on the performance of the filter. And EMI filter performance has been improved by canceling critical couplings, as documented in [15]. In addition, [16] analyzes the capacitive coupling of T-type EMI filters and further explores the impact of the relative positions of inductors on the coupling capacitance,

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All authors are with College of Electrical Engineering and Automation, Fuzhou University, Fuzhou 350108, China (e-mail: cqbf@fzu.edu.cn; 18270090424@163.com; 230110006@fzu.edu.cn; hq12138@126.com; chw@fzu.edu.cn).

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thereby optimizing the attenuation performance of the filter. [17] introduces a series inductor in-tegration approach, derived from analyzing magnetic field coupling in a two-stage EMI filter, which aims to enhance the low-frequency performance of the DM EMI filter. [18] conducted an in-depth investigation into the self-parasitics and coupling issues of three-phase filtering components. Firstly, the DM near-field coupling was optimized by adjusting the layout configuration of the filter components. Secondly, the influence of ground parasitic parameters of the CM filter was mitigated through optimized printed circuit board (PCB) layout. Finally, the capacitive coupling between the boost inductor and the EMI filter was reduced by means of electric field shielding. In addition to the above literature, [19] proposed optimizing the structural design of the PFC inductor in the bridgeless to-tem-pole PFC circuit to reduce the influence of its leakage magnetic field on other sensitive components. However, for circuit topologies without a PFC inductor, such as the flyback converter, the coupling problems caused by HF PCB loops are usually ignored, and the inductor design methods mentioned in the above literature are no longer applicable.

All the aforementioned schemes are designed to suppress the interference imposed on the parasitic parameters of the EMI filter. Nevertheless, the coupling problem induced by HF PCB loops has not been addressed or reported in existing literature.

However, in addition to degrading filter performance, the near-field coupling serves as the EMI noise propagation. For example, under the influence of near-field coupling, the noise current will be generated on the input plug situated near the HF power PCB loops or magnetic power components and flow to the power grid, especially in high power density applications, as cited in [20]–[22]. It is noteworthy that the PD adapter typically adopts a double-wire parallel wound CMC to mitigate near-field coupling effects between magnetic power components and CMC. Consequently, near-field coupling paths in the compact PD adapter deviate from conventional ones.

To address the aforementioned issues, this paper proposes a mathematical model to represent the coupling between various components in a PD adapter. Secondly, by leveraging the proposed model and combining it with finite element simulation, the key coupling factors are identified. To mitigate the impact of coupling, three types of HF power PCB layouts are put forward in this paper. Compared with placing capacitive suppressors near switching circuits to damp loop inductance, the method proposed in this paper requires no additional components or cost. Finally, the effectiveness of the optimization measures proposed in this paper is verified through tests on a 40 W PD power adapter.

The remaining parts of this article are arranged as follows: The second part explores the influence of near-field coupling on the DM conducted EMI noise in compact PD adapters and identifies the key influencing factors. The third part further investigates the magnetic field coupling issue between the HF power PCB loop and the input plug loop, constructs a mathematical coupling model, and analyzes the impact of HF

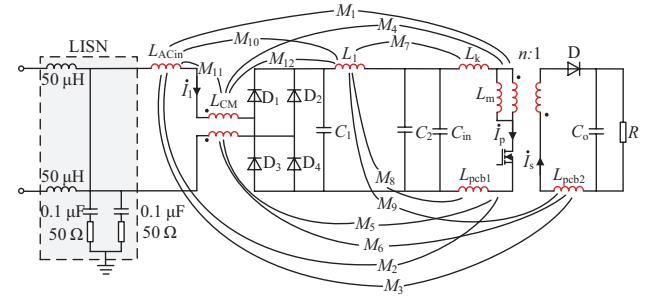


Fig. 1. Complete near-field coupling model of the PD adapter.

power PCB loop parameters on magnetic field coupling. The fourth part proposes three optimization methods for near-field coupling based on the above analysis results. The fifth part tests the prototypes before and after optimization to verify the accuracy and applicability of the proposed methods. The sixth part summarizes the key conclusions and significance of the research presented in this paper.

II. NEAR-FIELD COUPLING ANALYSIS OF PD ADAPTER

A. Analysis of Coupling in PD Adapter

1) DM Noise Model Analysis

Fig. 1 depicts the primary circuit of a PD adapter and its associated conducted EMI emission test layout. The configuration of the PD adapter includes a CMC, a rectifier bridge, a π filter, and a flyback converter. In analyzing the near-field coupling within the PD adapter, it is crucial to initially consider the magnetic power components of the circuit. This is due to their propensity to generate intense electrical and magnetic stray fields. Additionally, attention must be given to both the input plug and the HF power PCB loops. The comprehensive near-field coupling circuit model for the PD adapter is presented in Fig. 1. Here, L_{ACin} represents the parasitic inductance linked with the input plug; L_{CM} denotes the inductance of the CMC; L_1 signifies the inductance of the DM choke; L_{pcb1} and L_{pcb2} correspond to the parasitic inductances of the primary and secondary HF power PCB loops, respectively; L_k is the leakage inductance of the transformer; and C_{in} designates the busbar capacitance.

In this study, L_{ACin} , L_{CM} , and L_1 are identified as the sensitive components susceptible to near-field coupling. Concurrently, M_1 to M_{12} denote the mutual inductances between individual pairs of components or loop. The details are shown in Table I.

The near-field coupling effect between the DM choke L_1 and the magnetic components within the PD adapter, as well as the primary and secondary HF power PCB loops, can be represented by an associated current-controlled voltage source. The DM noise equivalent circuit for this relationship is illustrated in Fig. 2.

(1) gives the expression for the DM noise current flowing into the LISN under the coupled interference on DM choke L_1 , as illustrated in the equation, the noise current coupled into L_1

TABLE I
EXPLANATION TABLE OF NEAR-FIELD COUPLING IN PD POWER ADAPTERS

M	Explanation of M_1 – M_{12}
M_1	Coupling between the transformer and the input plug
M_2	Coupling between the primary-side HF PCB loop the input plug
M_3	Coupling between the secondary-side HF PCB loop and the input plug
M_4	Coupling between the transformer and the CMC
M_5	Coupling between the primary-side HF PCB loop and the CMC
M_6	Coupling between the secondary-side HF PCB loop and the CMC
M_7	Coupling between the transformer and the DM choke
M_8	Coupling between the primary-side HF PCB loop and the DM choke
M_9	Coupling between the secondary-side HF PCB loop and the DM choke
M_{10}	Coupling between the DM choke and the input plug
M_{11}	Coupling between the CMC and the input plug
M_{12}	Coupling between the CMC and the DM choke

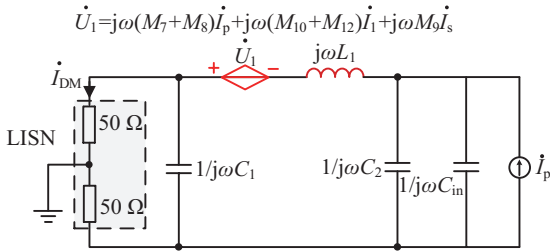


Fig. 2. DM noise equivalent circuit considering the effects of near-field coupling on DM choke.

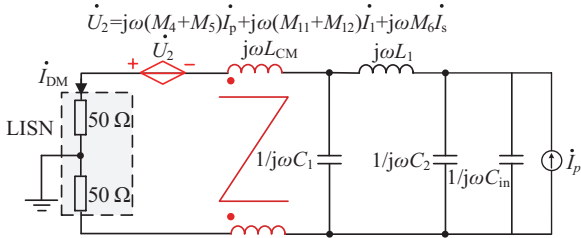


Fig. 3. DM noise equivalent circuit considering the effects of near-field coupling on CMC.

can be diverted through X-capacitor C_1 .

$$\dot{I}_{DM} = \dot{I}_{DM1} + \frac{\dot{V}_1 \cdot \frac{1}{100 \cdot j\omega C_1 + 1}}{1 + 100 \cdot j\omega C_1 + \frac{1}{j\omega(C_2 + C_{in})} + j\omega L_1} \quad (1)$$

Fig. 3 and (2) presents the equivalent circuit taking into account the near-field coupling effects of the DM component L_{DM} of the CMC, as well as the formula for the DM noise current flowing into the LISN with this coupling incorporated. Given that the two-wire parallel wound CMC L_{DM} is prevalently applied in PD adapters, its internal near-field coupling effects tend to neutralize each other. Consequently, the CMC possesses robust immunity against the disturbances arising from near-field coupling. The interference resulting from near-

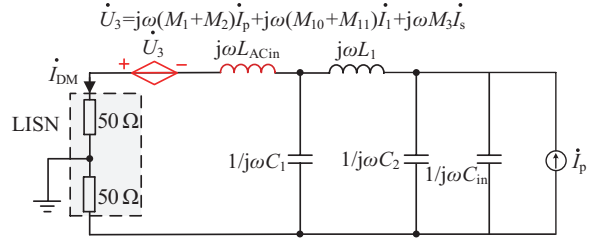


Fig. 4. DM noise equivalent circuit considering near-field coupling.

field coupling between the CMC and other components or loops is negligible.

$$\dot{I}_{DM} = \dot{I}_{DM1} + \frac{\dot{V}_2}{100 + j\omega L_{DM} + \frac{(1 - \omega^2 L_1 C_2 - \omega^2 L_1 C_{in}) \cdot j\omega C_1}{1 - \omega^2 (C_2 + C_{in})(L_1 - C_1)}} \quad (2)$$

When coupling occurs in the input plug loop, the X-capacitor C_1 and the input plug parasitic inductance L_{ACin} are sensitive components. Nevertheless, the loop area of C_1 is much smaller than that of L_{ACin} , resulting in weaker coupling interference. Moreover, the coupling between the X-capacitor and the HF PCB loop can be reduced or eliminated through layout optimization. Thus, the impact of this coupling has been minimized by shielding and layout adjustment of the X-capacitor in this work.

Fig. 4 and (3) respectively present the equivalent circuit considering the near-field coupling effects of the input plug, as well as the DM noise current flowing into the LISN with such coupling taken into account. As can be seen from Fig. 4, the noise current originating from the inductive coupling of the parasitic inductance L_{ACin} of the input plug can flow directly into the LISN, thereby generating DM noise. Affected by the coupling inductance, the placement positions of the controlled sources in Fig. 2 and Fig. 4 differ: one is placed inside the π -type filter, while the other is placed at its front end. The controlled source located at the equivalent position before the π -type filter causes part of the noise to be directly transmitted to the LISN, thus degrading the EMI characteristics of the circuit.

$$\dot{I}_{DM} = \dot{I}_{DM1} + \frac{\dot{V}_3}{100 + j\omega L_{ACin} + \frac{(1 - \omega^2 L_1 C_2 - \omega^2 L_1 C_{in}) \cdot j\omega C_1}{1 - \omega^2 (C_2 + C_{in})(L_1 - C_1)}} \quad (3)$$

To further verify the influence of the key coupling factors in the above analysis, this paper simulates each coupling parameter based on the DM equivalent circuit established earlier. The simulation results are shown in Fig. 5. The green curve represents the noise current flowing into the LISN when only the coupling between the HF PCB loop and the input plug loop (M_1 – M_3) is considered. The blue curve represents the noise current flowing into the LISN when only the coupling between the EMI filter and the remaining parts (M_4 – M_{12}) is

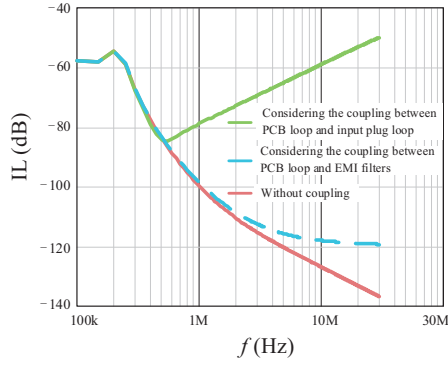


Fig. 5. DM noise simulation results considering near-field coupling.

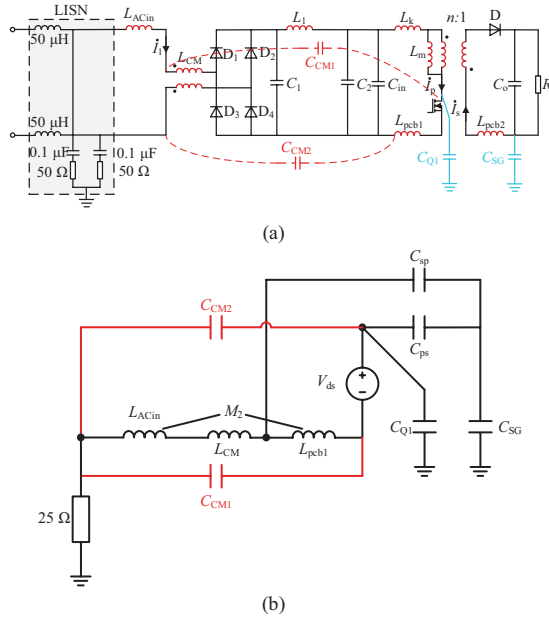


Fig. 6. CM noise equivalent circuit of PD Adapter. (a) Flyback adapter with filter. (b) CM equivalent circuit considering both capacitive coupling and magnetic coupling.

considered. The red curve represents the noise current flowing into the LISN without any coupling.

The above simulation results show that the coupling effect between the HF PCB loop and the EMI filter is very small, much smaller than that between the HF PCB loop and the input plug loop. Therefore, in the subsequent work, this paper focuses on the investigation of the coupling between the HF PCB loop and the input plug loop. In addition, since the prototype used in this study has a small size and does not adopt complex structures such as a metal chassis, the coupling with the chassis is not considered in this paper.

2) CM Noise Model Analysis

For CM equivalent circuit, the X-capacitor and electrolytic capacitors exhibit very low impedance within the conducted emission frequency band and can thus be treated as a short circuit. Owing to the constraint of leakage current, no Y-capacitor is used in this prototype. Accordingly, the CM equivalent circuit is represented by Fig. 6, where the drain-source voltage of the MOSFET serves as the CM noise source, C_{Q1} denotes the

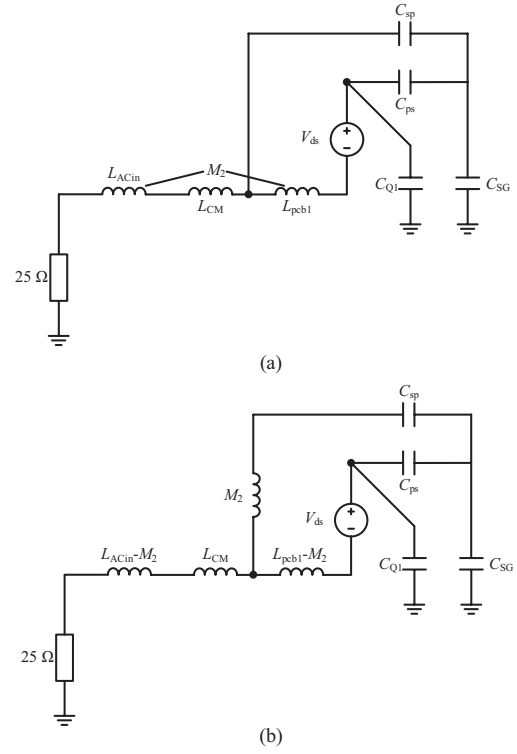


Fig. 7. CM equivalent circuit with only magnetic coupling considered. (a) CM equivalent circuit diagram considering only magnetic coupling. (b) Decoupled CM equivalent circuit diagram.

switching device-to-ground capacitance, C_{ps} and C_{sp} represent the CM capacitances of the transformer [23]. C_{CM1} represents the capacitive coupling between the potential switching node and the input terminal of the EMI filter, while C_{CM2} denotes the capacitive coupling between the primary-side ground and the input terminal of the EMI filter [24]. Both degrade the filter performance and aggravate CM noise.

Fig. 5(b) presents a simplified CM noise model involving magnetic coupling and two types of capacitive coupling. The CM noise generated by the coupling of capacitor C_{CM1} directly bypasses the attenuation of the filter, whereas the coupling via C_{CM2} is equivalent to shifting the resonant frequency of the CMC, thus deteriorating its HF performance.

As this paper mainly investigates the influence induced by magnetic coupling in such converters, a comb-shaped shielding structure is adopted to suppress capacitive coupling, so as to minimize the aforementioned capacitive coupling effect. This shielding can shield the electric field without altering the magnetic field distribution [25]. When capacitive coupling is neglected, the CM equivalent circuit and the decoupled circuit are shown in Fig. 7.

Based on the Thevenin equivalent circuit, the final CM noise equivalent circuit can be represented by Fig. 8, where V_{CM} denotes the CM voltage drop across the LISN. V_{eq} and C_{eq} represent the equivalent voltage source and equivalent capacitance, respectively, which can be obtained by the following:

$$V_{eq} = \frac{\omega^2 M_2 C_1 (C_{ps} + C_1 + C_2) + C_{ps} + C_2}{-\omega^2 L_{pcb1} C_1 (C_{ps} + C_1 + C_2) + C_1} \cdot V_{ds} \quad (4)$$

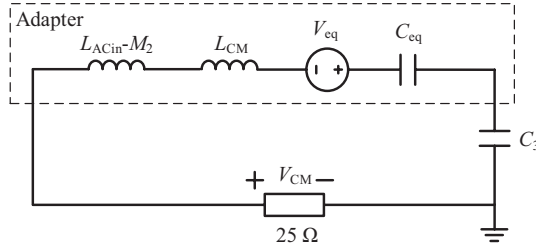


Fig. 8. Final CM noise model of the PD adapter.

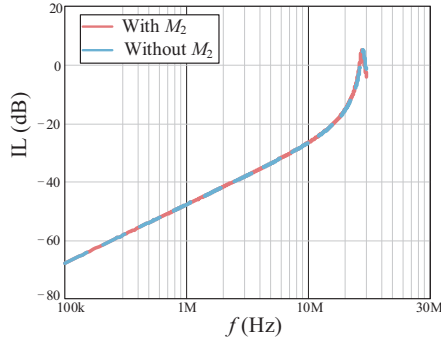


Fig. 9. CM noise simulation results considering near-field coupling.

$$C_{eq} = \frac{(C_{ps} + C_1 + C_2) - \omega^2 L_{pcb1} C_1 (C_{ps} + C_2)}{[1 - \omega^2 C_1 (L_{pcb1} - M_2)] \cdot [1 - \omega^2 M_2 (C_{ps} + C_2)]} \quad (5)$$

$$\begin{cases} C_1 = \frac{C_{ps} C_{Q1}}{C_{SG}} + C_{ps} + C_{Q1} \\ C_2 = \frac{C_{ps} C_{SG}}{C_{Q1}} + C_{ps} + C_{SG} \\ C_3 = \frac{C_{Q1} C_{SG}}{C_{ps}} + C_{Q1} + C_{SG} \end{cases} \quad (6)$$

Based on the CM equivalent circuit shown in Fig. 7, this paper compares the noise current flowing into the LISN with and without the coupling M_2 between the HF PCB loop and the input plug loop in the simulation. The results are presented in Fig. 9. Since mutual inductance M_2 is much smaller than the parasitic inductances of the primary HF power PCB loops L_{pcb1} and the inductance of the input plug L_{ACin} , M_2 has almost no effect on CM noise within the conducted emission frequency band.

In summary, the near-field interactions between the input plug and other components within the PD adapter stand out as pivotal determinants that could influence the EMI performance of the PD adapter. Although increasing the filter parameters can suppress DM noise, in practical power supply design, enlarging the DM choke L_1 will increase power loss, and the filter volume is also subject to certain constraints. Therefore, the DM noise suppression of flyback power supplies generally cannot rely solely on increasing the filter size.

In addition, in the prototype used in this study, an X-capacitor C_2 with a capacitance of 18 μF has been placed on the primary

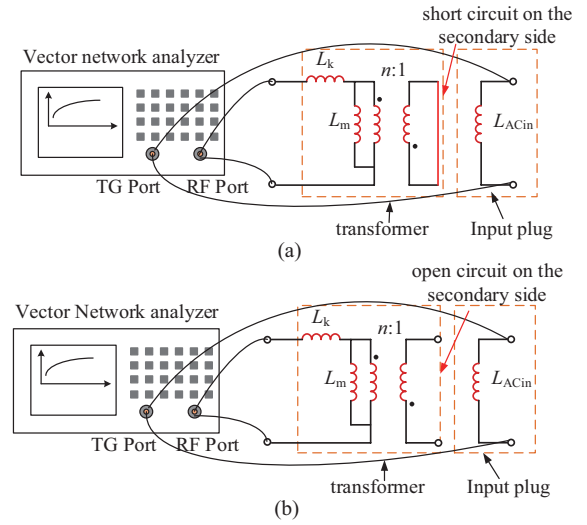


Fig. 10. Measurement methods. (a) Mutual inductance between transformer part and input plug. (b) Mutual inductance between inductor part and input plug.

HF PCB loop side to suppress the coupling interference introduced by the loop. Nevertheless, limited by the poor layout of the prototype, the filtering effect of C_2 is insufficient, which still results in excessive conducted emission.

If a capacitor is connected in parallel across the switch, it will increase the turn-on loss of the switch, the layout space, and the cost. Furthermore, the capacitor itself has parasitic inductance. At high frequencies, the capacitor, the PCB parasitic inductance, and the device parasitic inductance may form resonance, which will further amplify the circuit noise in some frequency bands, which is unacceptable.

Based on the above analysis, this paper proposes a method to reduce the leakage magnetic field of the HF power PCB loop by optimizing the PCB layout. Compared with conventional methods, the proposed method does not require any additional components and only needs to be considered in the early design stage.

B. Coupling Between Transformer and Input Plug

A flyback transformer is the integration of a transformer and an inductor. When evaluating the near-field coupling between the flyback transformer and the input plug loop, the transformer and the inductor parts need to be considered.

The testing of Fig. 10 is based on small-signal measurements using a vector network analyzer, with a voltage of 1 V applied to the ports and the impedance of the voltage source set to the standard 50 Ω . The measurement frequency ranges from 100 kHz to 1 MHz.

The near-field coupling can be quantified using two-port equipment and gauged by the insertion loss (IL) parameter. Fig. 10 illustrates the schematic diagram of the insertion loss measurement circuit. When assessing the near-field coupling between the transformer segment of the flyback transformer and the input plug, the transformer's secondary side is short-circuited. Under this condition, we evaluate the mutual inductance arising between the transformer's leakage inductance and the input

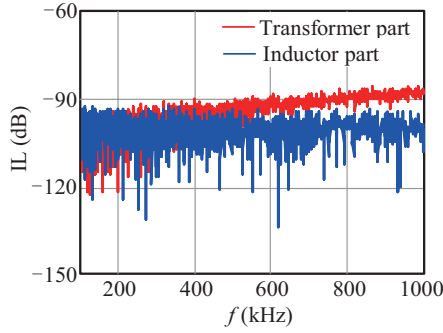


Fig. 11. The insertion loss of mutual inductance between the input plug and the flyback transformer.

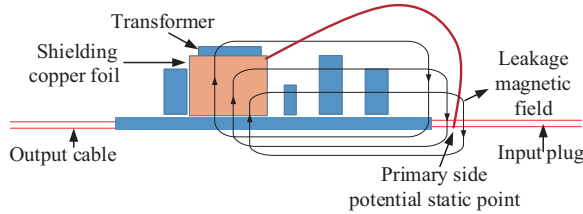


Fig. 12. The method to shield the transformer with a copper foil connected to the primary side potential static point.

plug loop. Conversely, when probing the near-field coupling between the inductor segment of the flyback transformer and the input plug, the transformer's secondary side remains open. Subsequently, the mutual inductance between the transformer's excitation inductance and the input loop is gauged.

Fig. 11 displays the resultant insertion loss measurements. The insertion loss pertaining to the mutual inductance between the inductor segment of the flyback transformer and the input plug loop closely mirrors the background noise. This suggests that the magnitude of this near-field coupling is minimal and is typically negligible. However, attention must be directed to the transformer segment of the flyback transformer.

To mitigate the near-field coupling induced by the transformer segment, a shielding copper foil can be affixed externally to the transformer and connected to the primary side's potential static point, as delineated in Fig. 12. Relying on Faraday's Law, this shielding copper foil acts as a barrier to the HF magnetic field. Consequently, it curtails the outward leakage of the transformer's magnetic field. This shielding technique enjoys widespread adoption in practical scenarios.

Post the application of the shielding copper foil, the insertion loss measurements are presented in Fig. 13.

As evident in Fig. 13, the use of copper foil as a shield significantly diminishes the near-field coupling between the flyback transformer and the input plug.

C. Coupling Between HF Power PCB Loops and Input Plug

To understand the near-field coupling between the HF power PCB loop and the input plug loop, a simulation of the magnetic field distribution produced by the HF power PCB loop was conducted.

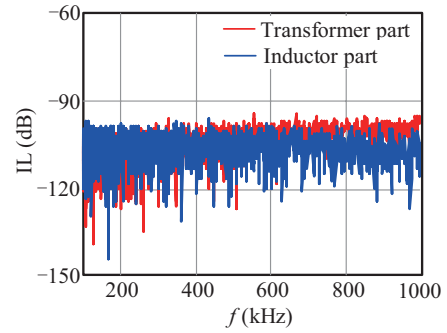


Fig. 13. The insertion loss of mutual inductance between the input plug and the flyback transformer with the shielding.

As shown in Fig. 14, the simulation is also grounded in S -parameter theory. Hence, the port excitation conditions mirror those of Fig. 8. Magnetic fields in the X and Z directions, originating from the HF power PCB loop, intersect with the input plug loop, leading to magnetic field coupling. Simulation results indicate that the magnetic field component in the X direction traversing the input plug loop measures at 3.05×10^{-10} A/m, while the component in the Z direction registers at 4.11×10^{-10} A/m.

Diminishing the magnetic flux penetrating the input plug can attenuate the near-field coupling. This necessitates optimization of both the input plug structure and the HF power PCB loops. Often, the design of the input plug is non-negotiable, making the HF power PCB loops the primary focus for near-field coupling mitigation. Conventional shielding using copper foil typically isn't suitable for guarding power PCB loops. Building on this insight, this study aims to formulate a near-field coupling model delineating the relationship between the power PCB loop and the input plug. It will further probe into the variables impacting this coupling and explore potential suppression strategies. It is worth mentioning that in the simulation of the mutual inductance between the HF PCB loop and the input plug loop, this paper adopts a current with an amplitude of 1 A as the excitation. Since the magnitude of mutual inductance is determined by the geometry, materials and other properties of the current loops, while the magnitude and type of the applied excitation exert no influence on mutual inductance, this study does not use an excitation matching the current level of the actual power adapter in the simulation.

III. THE MUTUAL INDUCTANCE CALCULATION MODEL BETWEEN THE POWER PCB LOOP AND THE INPUT PLUG LOOP

A. The Mutual Inductance Calculation Model Between the PCB Loop and the Input Plug Loop

Mutual inductance is commonly used to describe near-field coupling. Consider a quadrilateral PCB loop situated in the xOy plane with a current I , as illustrated in Fig. 15. The magnetic flux density B at the point (x_2, y_2, z_2) can be represented by (7).

$$\begin{aligned}
\mathbf{B} &= \frac{\mu_0}{4\pi} \oint \mathbf{I} d\mathbf{l} \times \mathbf{\bar{e}}_R / R^2 \\
&= \frac{\mu_0 \mathbf{I}}{4\pi} \left\{ \oint_{l_1} \frac{dy_1 \mathbf{\bar{e}}_y \times \left[\frac{(x_2 - x_1)\mathbf{\bar{e}}_x + (y_2 - y_1)\mathbf{\bar{e}}_y + z_2\mathbf{\bar{e}}_z}{R} \right]}{R^2} + \right. \\
&\quad \oint_{l_2} \frac{dx_1 \mathbf{\bar{e}}_x \times \left[\frac{(x_2 - x_1)\mathbf{\bar{e}}_x + (y_2 - y_1)\mathbf{\bar{e}}_y + z_2\mathbf{\bar{e}}_z}{R} \right]}{R^2} + \\
&\quad \oint_{l_3} \frac{dy_1 \mathbf{\bar{e}}_y \times \left[\frac{(x_2 - x_1)\mathbf{\bar{e}}_x + (y_2 - y_1)\mathbf{\bar{e}}_y + z_2\mathbf{\bar{e}}_z}{R} \right]}{R^2} + \\
&\quad \left. \oint_{l_4} \frac{[dx_1 \mathbf{\bar{e}}_x + dy_1 \mathbf{\bar{e}}_y] \times \left[\frac{(x_2 - x_1)\mathbf{\bar{e}}_x + (y_2 - y_1)\mathbf{\bar{e}}_y + z_2\mathbf{\bar{e}}_z}{R} \right]}{R^2} \right\} \quad (7) \\
&= \frac{\mu_0 \mathbf{I}}{4\pi} \left[\int_c^{-b} \frac{(a - x_2)dy_1 \mathbf{\bar{e}}_z + z_2 dy_1 \mathbf{\bar{e}}_x}{(\sqrt{(x_2 - a)^2 + (y_2 - y_1)^2 + z_2^2})^3} + \right. \\
&\quad \int_a^{-a} \frac{(y_2 + b)dx_1 \mathbf{\bar{e}}_z - z_2 dx_1 \mathbf{\bar{e}}_y}{(\sqrt{(x_2 - x_1)^2 + (y_2 + b)^2 + z_2^2})^3} + \\
&\quad \int_{-b}^b \frac{-(x_2 + a)dy_1 \mathbf{\bar{e}}_z + z_2 dy_1 \mathbf{\bar{e}}_x}{(\sqrt{(x_2 + a)^2 + (y_2 - y_1)^2 + z_2^2})^3} + \\
&\quad \int_{-a}^a \frac{(y_2 - \frac{c-b}{2a}x_1 - \frac{b+c}{2})dx_1 \mathbf{\bar{e}}_z - z_2 dx_1 \mathbf{\bar{e}}_y}{(\sqrt{(x_2 - x_1)^2 + (y_2 - \frac{c-b}{2a}x_1 - \frac{b+c}{2})^2 + z_2^2})^3} + \\
&\quad \left. \int_{-a}^a \frac{-\frac{c-b}{2a}(x_2 - x_1)dx_1 \mathbf{\bar{e}}_z + \frac{c-b}{2a}z_2 dx_1 \mathbf{\bar{e}}_x}{(\sqrt{(x_2 - x_1)^2 + (y_2 - \frac{c-b}{2a}x_1 - \frac{b+c}{2})^2 + z_2^2})^3} \right]
\end{aligned}$$

where $(x_1, y_1, 0)$ represents the coordinates of a current element on the quadrilateral loop, and R denotes the distance between a specific point in space and the current element. The dimensions of this quadrilateral loop are defined by the parameters a , b , and c .

In a similar vein, the magnetic flux density produced by a PCB loop of any given shape can be determined using the aforementioned method. Consequently, the mutual inductance between such loops is described as:

$$M = \frac{\Phi_m}{I} = \frac{\oint_S \mathbf{\bar{B}} \cdot d\mathbf{\bar{S}}}{I} \quad (8)$$

Consider a real-world power PCB loop, exemplified in Fig. 16. For calculation simplicity, this primary HF power PCB loop is approximated using three trapezoidal loops and one rectangular loop. These four quadrilateral loops maintain the same current direction as the original primary HF power PCB loop. The input plug loop can be represented equivalently by four rectangular loops, labeled as Loop 1, Loop 2, Loop 3, and Loop 4. Therefore, the mutual inductance, denoted as M_{pri} between the primary HF power PCB loop and the input plug loop can be computed as follows:

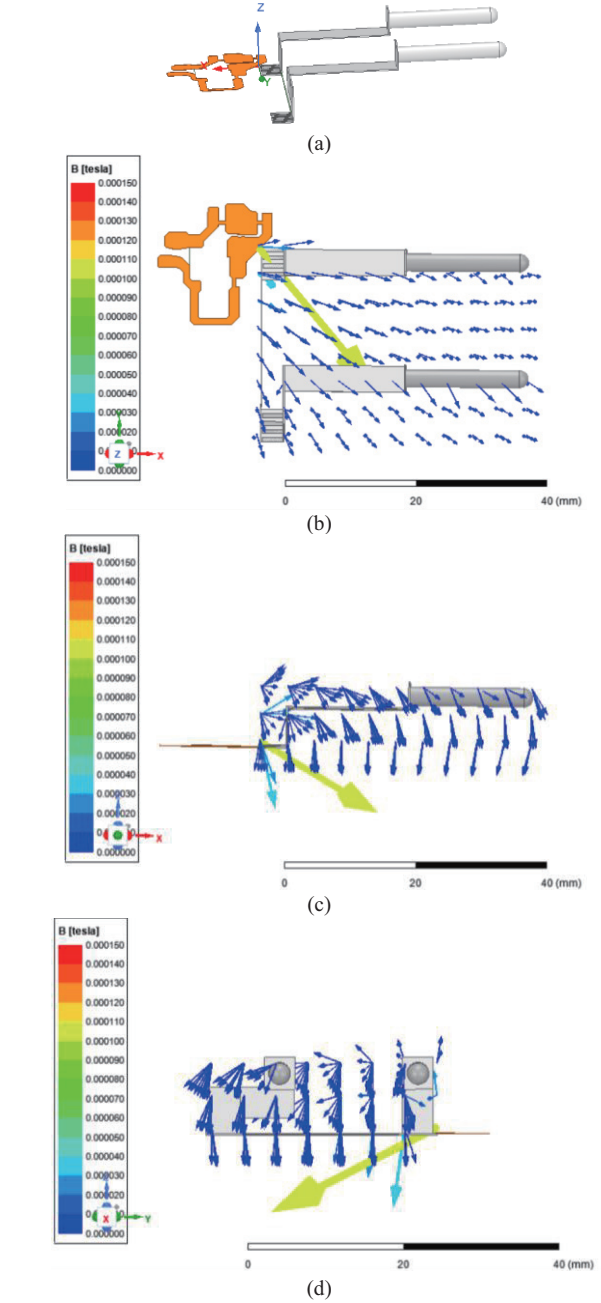
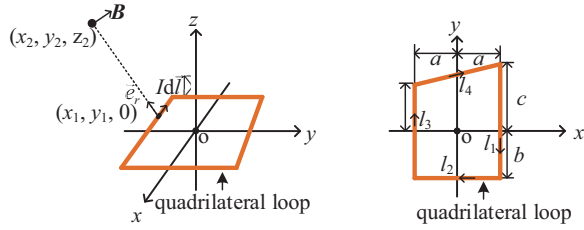
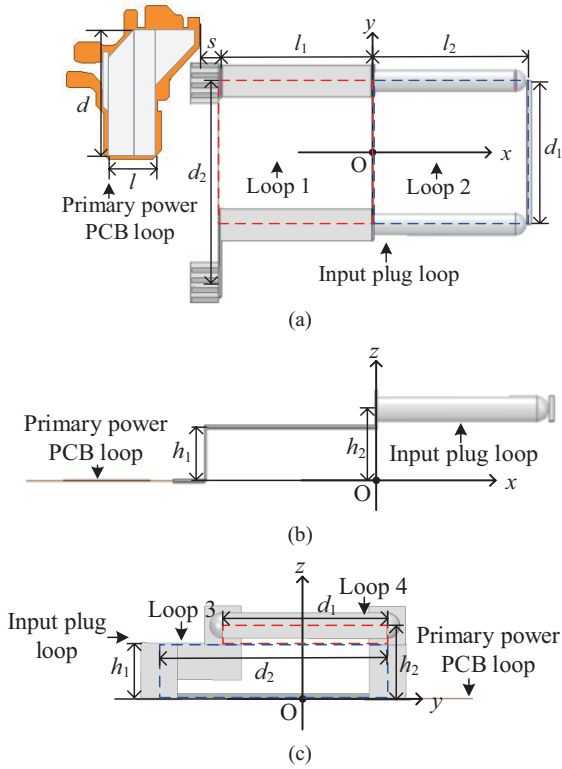


Fig. 14. The magnetic field distribution generated by the primary HF power PCB loop. (a) Magnetic field coupling simulation. (b) Magnetic field distribution in xOy plane. (c) Magnetic field distribution in xOz plane. (d) Magnetic field distribution in yOz plane.

$$\begin{aligned}
M_{\text{pri}} &= \left[\iint_{\text{Loop1}} \mathbf{B}_z(x_2, y_2, h_1) d\sigma + \iint_{\text{Loop2}} \mathbf{B}_z(x_2, y_2, h_2) d\sigma + \right. \\
&\quad \left. \iint_{\text{Loop3}} \mathbf{B}_x(-l_1, y_2, z_2) d\sigma + \iint_{\text{Loop4}} \mathbf{B}_x(0, y_2, z_2) d\sigma \right] / I \\
&= \left[\int_{-\frac{d_1}{2}}^{\frac{d_1}{2}} \int_{-l_1}^0 \mathbf{B}_z(x_2, y_2, h_1) dx_2 dy_2 + \int_{-\frac{d_1}{2}}^{\frac{d_1}{2}} \int_0^{l_2} \mathbf{B}_z(x_2, y_2, h_2) dx_2 dy_2 + \right. \\
&\quad \left. \int_{-\frac{d_2}{2}}^{\frac{d_2}{2}} \int_0^{h_1} \mathbf{B}_x(-l_1, y_2, z_2) dz_2 dy_2 + \int_{-\frac{d_1}{2}}^{\frac{d_1}{2}} \int_{h_1}^{h_2} \mathbf{B}_x(0, y_2, z_2) dz_2 dy_2 \right] / I \quad (9)
\end{aligned}$$

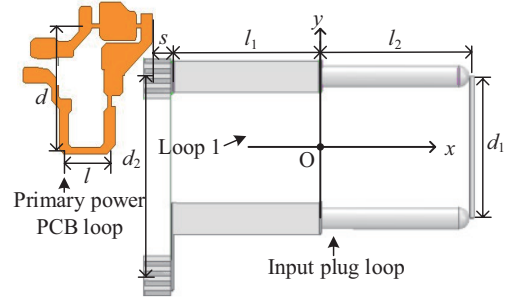
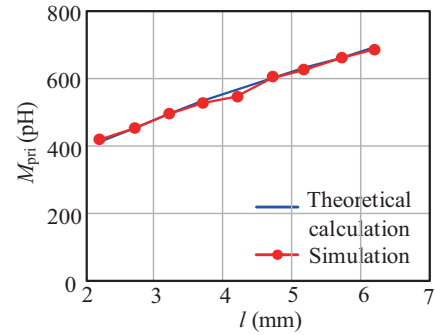
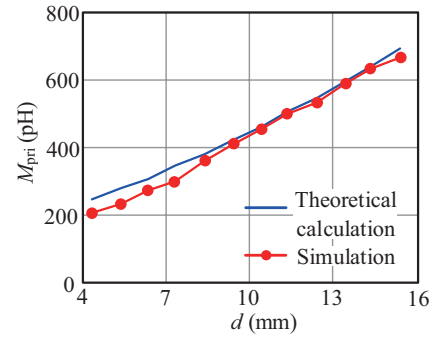
Fig. 15. Magnetic flux density B generated by the quadrilateral loop.Fig. 16. The magnetic field distribution generated by the primary HF power PCB loop. (a) xOy plane view. (b) xOz plane view. (c) yOz plane view.

B. Calculation and Simulation Results

In practical applications, PCB traces possess a distinct width, and the current doesn't flow strictly along the trace's centerline. This diverges from the previously mentioned theoretical assumptions.

Simulations were executed to investigate the factors that influence the mutual inductance between the primary HF power PCB loop and the input plug loop within the PD adapter. Specifically, the impacts of PCB loop parameters, namely l and d , along with the loop spacing s , were scrutinized. The finite element analysis (FEA) simulation model is illustrated in Fig. 17.

By maintaining two out of the three parameters—length l , width d , and loop spacing s —constant, the mutual inductance between the primary HF power PCB loop and the input plug loop under varying conditions was gleaned from simulations. Here, the values are $l=6.19$ mm, $d=15.34$ mm, $s=1.94$ mm, $l_1=18.8$ mm, $l_2=19.2$ mm, $d_1=18$ mm, $h_1=6$ mm, and $h_2=8$ mm.

Fig. 17. 3D Finite Element Analysis simulation model of primary HF power PCB loop and input plug loop (xOy plane view).Fig. 18. Mutual inductance M_{pri} between two loops varies with l .Fig. 19. Mutual inductance M_{pri} between two loops varies with d .

Figs. 16–18 depict the trends of mutual inductance, M_{pri} , between the two loops concerning l , d , and s , juxtaposed against results deduced from the theoretical model. Figs. 16 and 17 reveal that the mutual inductance, M_{pri} , between the primary HF power PCB loop and the input plug loop amplifies in tandem with the PCB loop parameters l and d . Notably, the simulation outcomes align with the theoretical computations. Among these, the distance d between input plug loops can be controlled by adopting shielded cables. However, according to the IEC 60884 standard, the plug position of PD power adapters is fixed, so approaches such as using shielded cables cannot be applied to reduce the coupling magnitude.

Analogously, the magnetic field coupling between the secondary HF power PCB loop and the input plug loop can be both theoretically assessed and simulated using a congruent methodology.

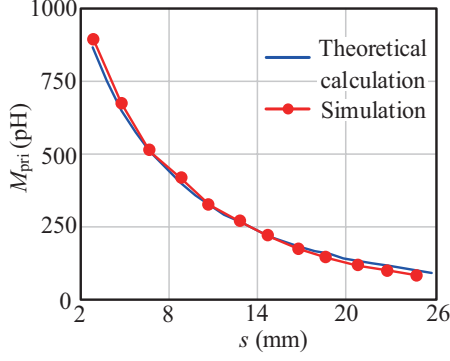


Fig. 20. Mutual inductance M_{pri} between two loops varies with s .

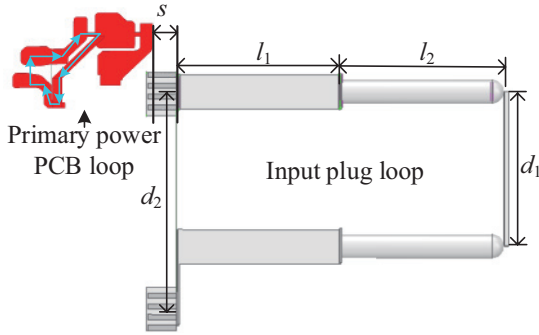


Fig. 21. The primary HF power PCB layout with minimal wiring distance in single-sided PCB (Layout 1).

IV. THE NEAR-FIELD COUPLING OPTIMIZATION METHOD BETWEEN THE PCB LOOP AND THE INPUT PLUG LOOP

From the preceding analysis, it's evident that the impacts of near-field coupling on the input plug loop can be mitigated by expanding the loop spacing, s , between the input plug loop and the HF power PCB loops. However, given the constraints regarding the PD adapter's size, the feasibility of this method remains limited.

Alternatively, the ramifications of near-field coupling on the input plug loop can be tempered by reconfiguring the layout of both primary and secondary HF power PCB loops. As illustrated in Fig. 21, when employing a single-sided PCB, a reimagined primary HF power PCB loop layout, characterized by minimized wiring distances, is suggested to curtail the mutual inductance, M_{pri} , between the primary HF power PCB loop and the input plug loop. Nonetheless, due to inherent constraints of real-world PCB design, the footprint of the single-sided PCB loop cannot be exceedingly compact. With regard to a double-sided PCB, parallel overlapping traces can be architecture on each face of the PCB, effectively rendering the loop's area null. This conceptual design is portrayed in Fig. 22.

For a double-sided PCB, an intertwined trace layout can be conceived, facilitating a scenario where positive and negative couplings between the HF power PCB loop and the input plug loop offset one another, as exemplified in Fig. 23.

By adopting an astute PCB design, the mutual inductance between the HF power loop and the input plug loop can be

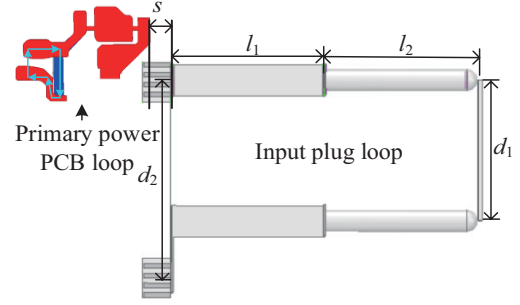


Fig. 22. The primary HF power PCB layout with parallel overlapping wiring on both sides in a double-sided PCB (Layout 2).

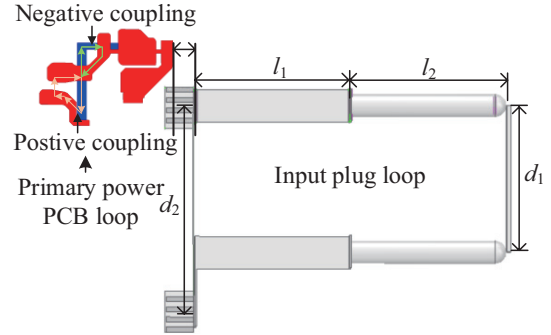


Fig. 23. The primary HF power PCB layout with twisted wiring in double-layer PCB (Layout 3).

TABLE II
SIMULATION RESULTS OF MUTUAL INDUCTANCE UNDER DIFFERENT LAYOUTS

Layout scheme	Mutual inductance before optimization M/pH	Mutual inductance after optimization M/pH
Fig. 21 (Layout 1)	825.3	521.8
Fig. 22 (Layout 2)	825.3	120.1
Fig. 23 (Layout 3)	825.3	73.95

approximated to zero. This, in turn, minimizes the perturbations due to near-field coupling on the input plug and effectively suppresses DM conducted disturbances. As presented in Table II, all three PCB layouts proposed in this paper achieve varying degrees of reduction in the mutual inductance between the HF PCB loop and the input plug loop.

In this section, three PCB layouts are proposed to reduce the coupling between the HF PCB power loop and the input connector. Layout 1 uses a single-layer PCB and reduces the coupling by controlling the loop area. Owing to the single-layer structure, it features low cost but provides only marginal improvement. In contrast, Layout 2 adopts a double-layer PCB, where parallel routing between the top and bottom layers can further reduce the area of the HF power PCB loop. Although the cost increases slightly, the suppression effect is significantly better. Based on Layout 2, Layout 3 uses an interleaved routing scheme such that the positive and negative couplings between the HF power PCB loop and the input plug loop cancel each other. Since it is impractical to use single-layer

TABLE III
SUMMARY OF THE THREE PROPOSED PCB LAYOUTS

Layout scheme	Mutual inductance M/pH	PCB layer count	Implement effort
Fig. 21	521.8	1	Easy
Fig. 22	120.1	2	Relatively Simple
Fig. 23	73.95	2	Relatively Simple

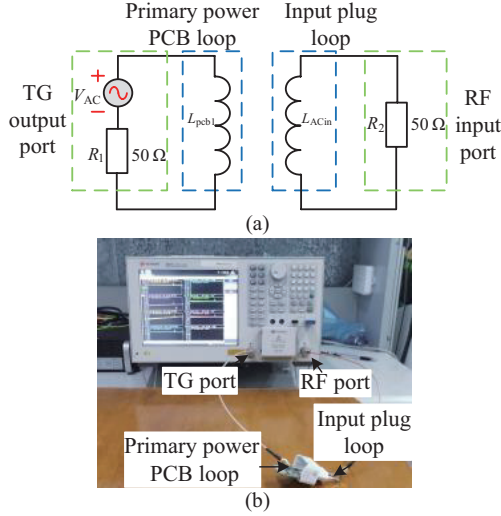


Fig. 24. Mutual inductance measurement. (a) Measurement approach of mutual inductance. (b) Object diagram.

boards for most circuits in practical PCB design, Layout 3 is strongly recommended in this paper as the preferred layout for HF power PCB loops. A comparison of these layouts is summarized in Table III. Furthermore, it is verified that Layout 3 remains effective even for different circuit topologies. The analysis presented in this paper focuses on various PCB layout structures and is independent of the specific filter parameters.

V. EXPERIMENTAL VALIDATION

A. The Measurement Results of Mutual Inductance

The insertion loss method is adopted to gauge the mutual inductance between the primary HF power PCB loop and the input plug loop, with its formulation presented in (10) as referenced in [26].

Upon short-circuiting the MOSFET and the bus capacitor, C_{in} , within the primary HF power PCB loop, connections are made: the primary HF power PCB loop to the timing generator (TG) output port of the vector network analyzer (VNA) and the input plug loop to the radio frequency (RF) input port, as depicted in Fig. 24. Through comprehensive circuit theoretical deliberations and computations, the relationship between the insertion loss and mutual inductance can be articulated as (10).

$$|M| = \left| \frac{(50 + j\omega L_{pcb1}) \cdot (50 + j\omega L_{ACin})}{100 \cdot j\omega} \right| \cdot 10^{20} \quad (10)$$

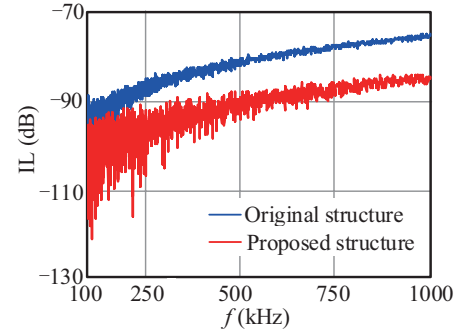


Fig. 25. Insertion loss curve of the mutual inductance.

TABLE IV
MEASUREMENT RESULTS OF MUTUAL INDUCTANCE

Item	Insertion loss K/dB	Mutual inductance M/pH
Original primary HF power PCB loop	-79.483	767.8
Proposed primary HF power PCB loop (Fig. 23)	-90.5	216

In this context, L_{pcb1} represents the self-inductance of the primary HF power PCB loop, while L_{ACin} denotes the self-inductance of the input plug loop. The insertion loss of mutual inductance between the original and proposed primary HF power PCB loop and plug loop is shown in Fig. 25. The same method is used to test the mutual inductance between the secondary HF power PCB loop and the input plug loop.

The measurement results under original and proposed primary power PCB layouts at $f = 550$ kHz are shown in Table IV.

As illustrated in Fig. 25 and Table IV, the near-field coupling effects can be significantly reduced by adopting the transformer optimization proposed in Chapter 2 and the PCB loop layout optimization presented in Chapter 4.

B. Conducted EMI Tests Results of Prototype

A PD adapter is taken as the prototype for the experiment. The physical diagram of the PD adapter is as shown in Fig. 26, with an input voltage V_{in} of 220 V, an output voltage V_{out} of 24 V, an output power P_{out} of 40 W, and a switching frequency f of 60 kHz.

According to standard EMI measurement principles CIS-PR22, the prototype's noise spectrums under two primary PCB loop layouts are tested in an electromagnetic shielding chamber. It mainly comprises the device under test (DUT), ESH2-Z5 LISN, EZ-17 current probe (for differential and common mode noise separation) and R&S ESCI EMI receiver.

Fig. 27 compares the original noise with the noise results after integrating the transformer optimization from Chapter 2 and the PCB loop optimization from Chapter 4. Compared to the original noise, the DM noise is reduced by 0–12 dB from 150 kHz to 8 MHz, while the CM noise remains essentially unchanged. By reducing the area of the primary HF power PCB loop, the mutual inductance between the input plug

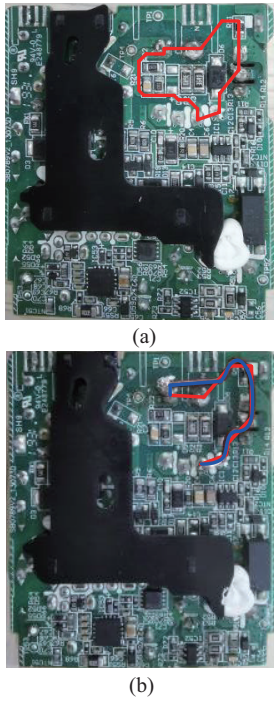


Fig. 26. The layout of the prototype. (a) Original primary PCB loop layout. (b) Proposed primary PCB loop layout.

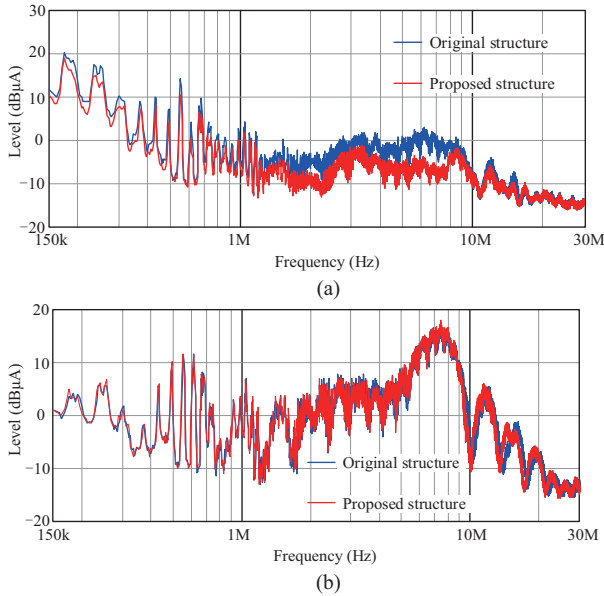


Fig. 27. Noise comparison of the prototype. (a) DM noise current. (b) CM noise current.

loop and the primary HF power PCB loop is suppressed. Due to the reduction in near-field coupling, the DM conducted noise performance of the PD adapter is improved in the low-frequency band. Furthermore, consistent with the foregoing analysis, the CM noise is unaffected due to the weak coupling between the HF PCB power loop and the input plug loop.

VI. CONCLUSION

In this study, we focused on the magnetic power components, HF power PCB loops, and the input plug to inves-

tigate potential magnetic near-field couplings within the PD adapter. Our findings highlight that the dominant nearfield coupling occurs between the HF power PCB loops and the input plug loop in the PD adapter. Based on this, we developed a mathematical model characterizing the near-field coupling between these elements. Leveraging the proposed mathematical model and finite element simulation results, we identified key influencing factors of near-field coupling. Notably, both the dimensions of the HF power PCB loops and the spacing between them play significant roles in determining the coupling effects. Engineers should avoid overly large HF power PCB loops during design, which would lead to excessive leakage magnetic fields. To suppress such coupling effects, three novel PCB wiring schemes are proposed in this paper for different application scenarios: a minimal wiring distance approach for single-sided PCBs, a parallel overlapping wiring strategy for double-sided PCBs, and a twisted wiring design for double-layer PCBs. Their core objective is to reduce the leakage magnetic field of the HF power PCB loops. For experimental validation, a 40 W PD adapter prototype was developed to verify the effectiveness and feasibility of the proposed optimization methods.

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Committee of China Power Supply Society (CPSS).

Qingbin Chen was born in Quanzhou, China. He received the B.E. and Ph.D. degrees in electrical engineering from Fuzhou University, Fuzhou, China in 2007 and 2012, respectively. He worked as a visiting scholar in University of Florida, Florida, the USA from 2017 to 2018. His research includes high frequency magnetic technology, EMC diagnosis and suppression technology, and wireless power transfer. Dr. Chen served as the Vice chairperson and Deputy Secretary General of Magnetic Component Specialty



Zirui Qian was born in Zhejiang, China, in 2000. He received the B.S. degree in electrical engineering and automation from the Changchun University of Technology, China, in 2023. He is currently pursuing the master's degree with the Fuzhou University, Fuzhou. His research interest includes high frequency magnetic technology.



Yujie Lan was born in Fujian, China, in 1998. He received the B.S. degree in electrical engineering and automation from the Harbin University of Science and Technology, Harbin, China, in 2021. He is currently pursuing the Ph.D. degree with the Fuzhou University, Fuzhou. His research interest includes high frequency magnetic technology.



Qing He was born in Jiangxi, China, in 1999. He received the B.S. degree in electrical engineering and automation from the Tiangong University, Tianjin, China, in 2022. Currently, he is pursuing a doctoral degree at Fuzhou University. His research interests include the suppression and diagnosis of electromagnetic compatibility and wireless power transfer technology.



Wei Chen received the M.S. and Ph.D. degrees in electrical engineering from Fuzhou University, Fuzhou, China, in 1987 and 1990, respectively. He was a Senior Visiting Professor with the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, from 1996 to 1998. He was a Research and Development Manager with Delta Electronics Company Ltd., and the Delta Power Electronics Center, Shanghai, China, from 1999 to 2008. He has authored or coauthored more than 80 technical articles. He held more than 40 approved patents from China and USA. His research interests include power conversion, high-frequency magnetic technology, EMI debug and solution, wireless power transfer, electromagnetic field analysis, and applications. Prof. Chen is a fellow of the Council of China Power Supply Society (CPSS).