

High Power Density High Current Density LLC-DCX Converter for Datacenter Application

Yang CAO, Bin WANG, Zhanshan ZHU, Min XU, and David Wei ZHANG

Abstract—This paper presents a high-efficiency LLC resonant bus converter with a 10:1 step-down ratio, tailored for 48 V data center applications. To address the challenges of power density and current density, a compact design was achieved by employing a single-PCB planar transformer and a high-density integration scheme, significantly reducing the converter's footprint compared to conventional approaches. Furthermore, a primary winding connection method for current sharing and a copper-plated secondary termination design were proposed. The implemented prototype demonstrates excellent performance: with a 48 V input, it delivers a maximum output current of 85 A and a peak efficiency of 98.8%; under 60 V input conditions, the converter achieves a current density of 0.29 A/mm² and a power density of 3548 W/inch³.

Index Terms—Datacenter, DCX, high current density, high power density.

I. INTRODUCTION

WITH the rapid development of artificial intelligence (AI) applications, greater computing capability is required to meet the demands of large-scale machine learning tasks [1]–[4]. Consequently, more advanced xPUs and system architectures are implemented in high-performance computing systems. This trend has led to a sharp increase in energy consumption in datacenters. Currently, the thermal design power (TDP) of a single CPU/GPU chip can reach 700 W or even higher, with operating voltage decreased to 1 V or lower, and the current has increased to 500 A or higher [5]–[7].

To improve the overall system efficiency and reduce distribution loss, 48 V power systems are inevitably used to replace the traditional 12 V systems [8]–[10], as shown in Fig. 1(a). Two-stage 48 V power delivery system is adopted widely by industry for its balance between efficiency and scalability. Generally, it utilized a non-regulated intermediates bus converters (IBCs) with a fixed conversion ratio for the first-stage, followed with a buck converter which can provide a regulated voltage for the xPUs, as shown in Fig. 1(b). The first-stage IBCs can be designed in a very high efficiency and power den-

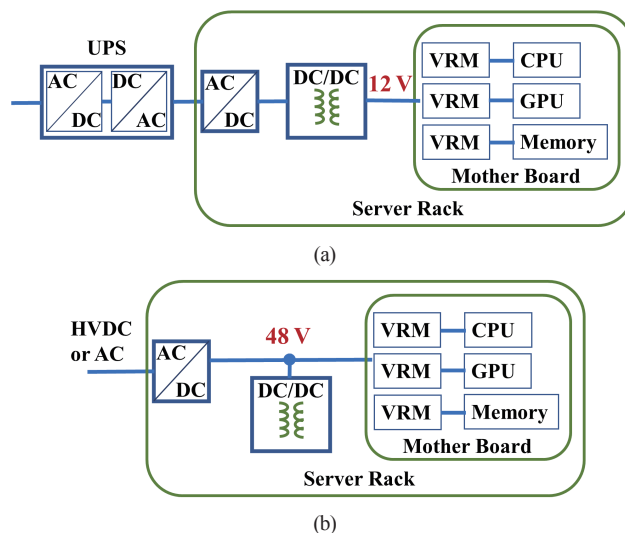


Fig. 1. Datacenter distribution system. (a) Traditional 12 V distribution. (b) DC distribution with 48 V.

sity module.

To be compatible with original 12 V systems, IBCs are often designed to output 12 V. It is an emerging trend to place high-frequency voltage regulators (VRs) in close vicinity to xPUs for distribution loss reduction. Hence, it is desirable to employ a lower intermediate bus voltage. In another hands, to enhance the efficiency of the overall system and that of the two-stage buck converter, a lower intermediate bus voltage is preferred. For example, as reported in [11], reducing the intermediate bus voltage from 12 V to 6 V can boost the overall system efficiency by more than 2%. As a result, there is an increasing research interest in solutions for converting 48 V to 3–6 V [12]–[16]. However, this approach requires power modules with higher current area density (A/mm²) and power density (W/mm³).

LLC resonant converters and switched-capacitors converters (SCCs) are two types of topologies commonly used in IBCs. For SCCs, it can meet the demands of high efficiency and high power density at 12 V output [17], [18]. However, increasing the conversion ratio requires more components, including capacitors and switches, which reduces the power density and efficiency [19]. However LLC-DCX converters have demonstrated high power density and high efficiency even with the high conversion ratios [20], [21].

Increasing the switching frequency helps reduce the size of passive components such as transformers or inductors, which

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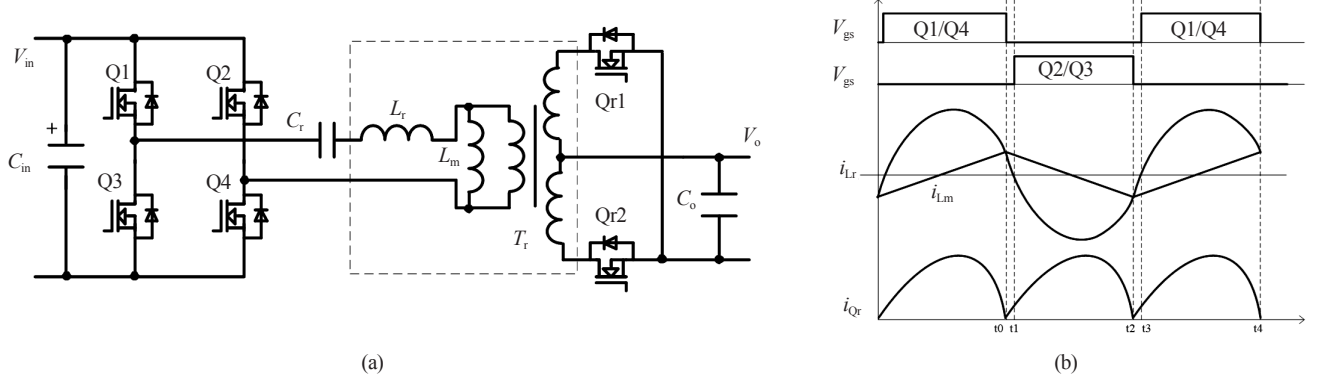


Fig. 2. Circuit and waveforms. (a) LLC resonant converter circuit. (b) Waveforms with operation at resonant frequency.

TABLE I
SELECTION OF PRIMARY DEVICES

PN	BV _{DSS} (V)	R _{DS(on)} @25°C (mΩ)	C _{ISS} (pF)	Q _G (nC)	Dimension (mm)
EPC2053	100	3.1 @ 5V	1453	11.4	3.5 × 2
ISC027N10NM6	100	2.3 @ 10V	4300	58	5 × 6
ISC030N10NM6	100	2.6 @ 10V	4000	55	5 × 6
BSC025N08LS5	80	2.6 @ 5V	5800	44	5 × 6

TABLE II
SELECTION OF SECONDARY DEVICES

PN	BV _{DSS} (V)	R _{DS(on)} @25°C (mΩ)	C _{ISS} (pF)	Q _G (nC)	Dimension (mm)
EPC2024	40	1.2	2050	18	6.05 × 2.3
EPC2023	30	1.15	1850	19	6.05 × 2.3
IQE006NE2LM5	25	0.65	1700	28.5	3.3 × 3.3

in turn contributes to improving power density. Meanwhile, to reduce the control complexity of the LLC at MHz, a fixed-frequency operating mode is adopted [22], [23]. The zero-voltage switching (ZVS) for primary switches and zero-current switching (ZCS) for secondary switches can be achieved with the resonant frequency slightly higher than the switching frequency. In this mode, the switching loss mainly depends on the turn-off loss of the primary-side devices. Gallium Nitride (GaN) power devices [24], [25] can be used to replace silicon (Si) devices, mainly because GaN power devices almost no turn-off loss [26]. Meanwhile, GaN power devices have a lower gate charger, so the driving loss is also lower than Si MOSFET.

Designing a transformer suitable for high-current applications at high frequencies is a challenging task, mainly limited by conduction loss from the eddy current effect, proximity effect [9], [20]. PCB planar transformers are commonly used in these transformer-based converters at high frequency, because of high efficiency and low leakage inductance. However, the traditional single PCB planar transformer configuration tends to suffer from undesirable AC winding losses and termination losses [27]. The reasons for this are unbalanced current sharing among windings and current crowding at the terminations, respectively. Hence, matrix transformers are often employed in IBCs to minimize the aforementioned losses which uniform which enables the more uniform current distribution in each phase and less root mean square (RMS) owing to the in-series primary windings [9], [21], [28]. To further reduce termination loss, numerous studies [9], [29], [30], [31] have explored magnetic circuit design, the placement of secondary-side components and vias, and the impact of paralleled output filter capaci-

tors for LLC converters equipped with planar transformers. For example, the termination structure consisting of synchronous rectifier (SR) devices and output capacitors replaces part of the secondary windings. However, the IBCs with matrix planar transformer, which results in long windings structure, usually occupy a larger footprint. It is not conducive to achieving high power density and high current density.

In this article, a turn ratio 10:1 LLC-DCX converter with a single planar transformer is proposed to achieve lower output voltage with higher power density and smaller planar area. By optimizing terminal design and implementing a 3D stacking system integration scheme, the prototype was built with an input voltage range of 40 V–60 V. It achieved a peak efficiency of 98.8% (excluding driver loss) at 48 V input. Under the 60 V condition, the maximum output power is 510 W, with the peak efficiency of 98.3% (excluding driver loss), and a power density of 3548 W/in³. The corresponding current area density could reach 0.29 A/mm².

II. LLC-DCX CONFIGURATION

The resonant LLC circuit and its operating waveforms are shown in Fig. 2. The resonant inductor L_r , magnetizing inductor L_m , and transformer are integrated into a PCB planar transformer, providing higher power density and improved efficiency. A full-bridge configuration is used on the primary side, while a center-tapped full-wave rectifier is employed on the secondary side. The LLC circuit operates at a fixed frequency F_{sw} of 1 MHz.

The input voltage range for bus converters varies between 40 V and 60 V, necessitating primary switches rated at either

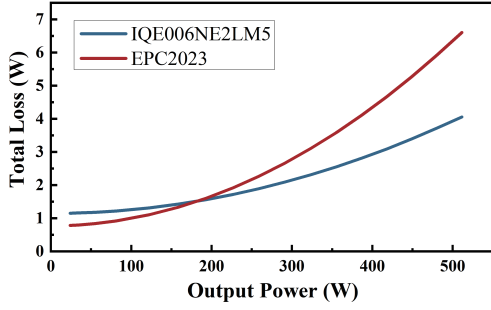


Fig. 3. Power loss comparison of secondary devices at 1 MHz.

80 V or 100 V. Table I outlines the key specifications of both Si and GaN devices considered for this application. Among the options, the GaN EPC2053 is particularly advantageous due to its compact size and low gate charge, which contribute to improved power density and efficiency. Consequently, the EPC2053 is selected for the primary side.

Given a maximum output voltage of 6 V at a 60 V input, the breakdown voltage of the secondary-side devices must be greater than 15 V. Table II presents the key parameters of the candidate devices, with the IQE006NE2LM5 standing out for its reduced size and lower on-resistance compared to the GaN alternatives.

The secondary-side SR switching devices feature ZVS and ZCS. Therefore, the estimation of total loss considering only conduction loss and drive loss is expressed as follows:

$$P_{\text{cond}} = I_{\text{RMS}}^2 \frac{R_{\text{DS(on)}}}{N_{\text{Para}}} \quad (1)$$

$$P_{\text{driver}} = V_{\text{GS}} Q_{\text{G}} F_{\text{SW}} N_{\text{Para}} \quad (2)$$

where N_{Para} is the number of parallel devices.

Fig. 3 illustrates the calculated power loss curve for the secondary-side devices, including the driving loss as a function of output power. At light load, the loss of the IQE006NE2LM5 is slightly higher than that of the GaN EPC2023, primarily due to its larger driver loss. However, at higher loads, the IQE006NE2LM5 exhibits significantly lower loss compared to the GaN device, owing to its much lower on-resistance. As a result, the IQE006NE2LM5 was chosen for the secondary side.

III. HIGH POWER DENSITY HIGH CURRENT DENSITY PCB PLANAR TRANSFORMER DESIGN

Designing the PCB planar transformer is one of the main challenges in an LLC-based IBCs, particularly when targeting low-voltage, high-current outputs with a large step-down ratio. Critical aspects of the design include the choice of core structure, the layout of the windings, and the configuration of the termination loop. These factors collectively have a significant impact on both the achievable power density and the overall efficiency. Furthermore, to achieve the goal of high current density, a single-transformer structure is adopted to reduce its footprint.

First, it is essential to choose a magnetic material that offers

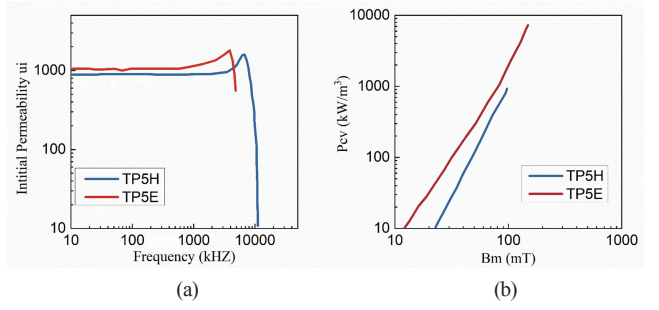


Fig. 4. Comparison of (a) initial permeability and (b) core loss density.

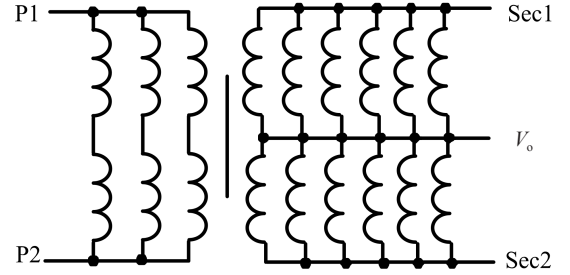


Fig. 5. Transformer equivalent circuit.

low core-loss density and maintains stable initial permeability. Fig. 4 compares the characteristics of TDG's TP5H and TP5E materials across different frequencies. The results show that TP5H provides both lower core losses and more consistent permeability above 1 MHz. Therefore, TP5H is selected for the design.

A. Dimension Design of Transformer

The PCB planar transformer is designed with a 10:1 turns ratio. On the primary side, a 6-layer PCB is used, configured as five turns per layer in a 2-series, 3-parallel arrangement. The secondary side consists of 12 PCB layers, where each half of the center-tap structure employs a parallel winding formed by six layers. The transformer's equivalent circuit diagram is shown in Fig. 5.

To further optimize the footprint and power density of the single-central-leg transformer, it is necessary to analyze how the transformer's loss varies with its physical dimensions. In particular, the core's central-leg radius r and the winding c width play dominant roles in determining both the loss and the occupied area. The total transformer loss is obtained by combining the core loss and the winding loss, is expressed as follows:

$$P_{\text{Tr}} = P_{\text{core}} + P_{\text{winding}} \quad (3)$$

(4) expresses the core loss of the transformer, which is determined by the core volume V_{core} , the peak flux density B_m and the material-dependent parameters k , α , and β .

$$P_{\text{core}} = k \cdot B_m^\alpha \cdot f^\beta \cdot V_{\text{core}} \quad (4)$$

The winding loss is evaluated using the Dowell AC resis-

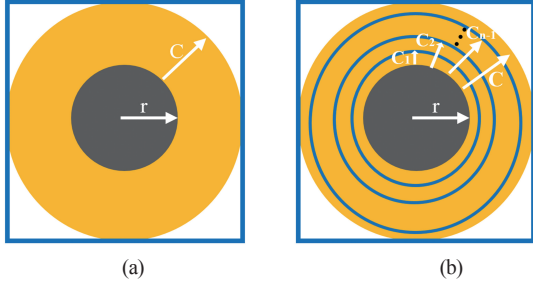


Fig. 6. Schematic of dimensions. (a) Primary winding. (b) Secondary winding.

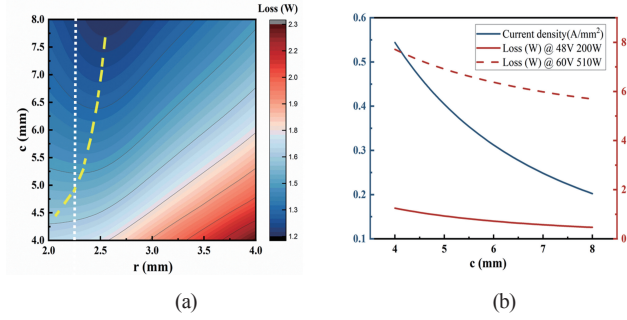


Fig. 7. Transformer dimension design. (a) Relationship between transformer loss and size. (b) Relationship between loss, current density, and winding width.

tance model [19]. Based on this approach, the AC resistance of the primary and secondary windings is roughly obtained from (5) and (6), respectively. Fig. 6 shows the dimensions of single transformer primary and secondary windings.

$$R_{ac_pri} = \frac{2F_r}{3} \frac{2\pi\rho}{h} \frac{25}{\ln(r+c) - \ln r} \quad (5)$$

$$R_{ac_sec} = \frac{F_r}{6} \frac{2\pi\rho}{h} \frac{1}{\ln(r+c) - \ln r} \quad (6)$$

where F_r represents the AC resistance coefficient, h is the copper thickness, and ρ denotes the copper resistivity. r and c correspond to the core radius and winding width. Taking into account winding loss, termination loss, and core loss, the relationship between total transformer loss and size is shown in the Fig. 7(a).

Moreover, to ensure that the magnetic flux density remains below 100 mT at a maximum input voltage of 60 V, the core center post radius must satisfy $r \geq 2.25$ mm. Fig. 7(b) illustrates the variation of planar transformer loss and current density with winding width for a core center post radius of 2.25 mm. To achieve a relatively high current density, this work sets the target current density of the planar transformer at 0.4 A/mm. The corresponding winding width is approximately 5 mm. At an output power of 510 W and an output voltage of 6 V, a winding width of 5 mm increases the loss by about 1 W compared to an 8 mm width, but the current density is reduced by 50%. At an output power of 200 W and an output voltage of 4.8 V, the 5 mm width increases the loss by about 0.2 W relative to the 8 mm width.

In summary, a core center post radius of 2.25 mm and a

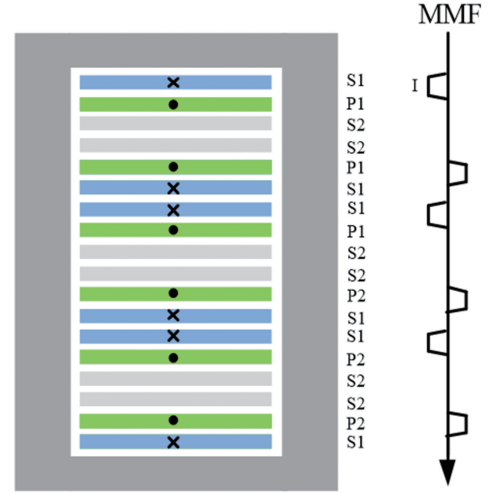


Fig. 8. Winding arrangement.

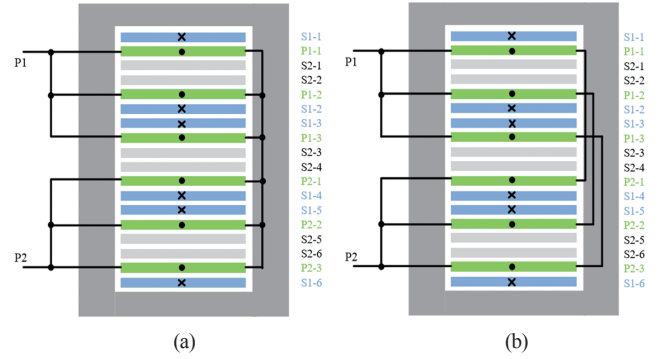


Fig. 9. Winding arrangement of (a) traditional connection and (b) proposed connection.

winding width of 5 mm are ultimately selected as the planar transformer dimensions.

B. Windings Arrangement and Connection

In this work, the layer configuration illustrated in Fig. 8 is adopted. By implementing the S1–P–S2–S2–P–S1 sequence, an alternating MMF pattern is established within the core, enabling uniform current sharing across all parallel winding layers [28], [32], [33].

A matrix transformer topology is typically composed of n identical transformers—each with a 1:1:1 turns ratio—and employed to attain the remaining n :1 voltage reduction. This structure naturally enables effective current sharing and reduces termination losses. Matrix transformers typically use only a few layers, whereas a single-transformer structure often requires many parallel windings to deliver higher power. This can lead to current imbalance among the windings, a problem that becomes more pronounced as the number of layers increases, ultimately reducing system efficiency and causing additional temperature rise that limits the overall output power. Addressing this issue is essential to fully realize the advantages of the single-transformer architecture.

The arrangement and interconnection of parallel PCB wind-

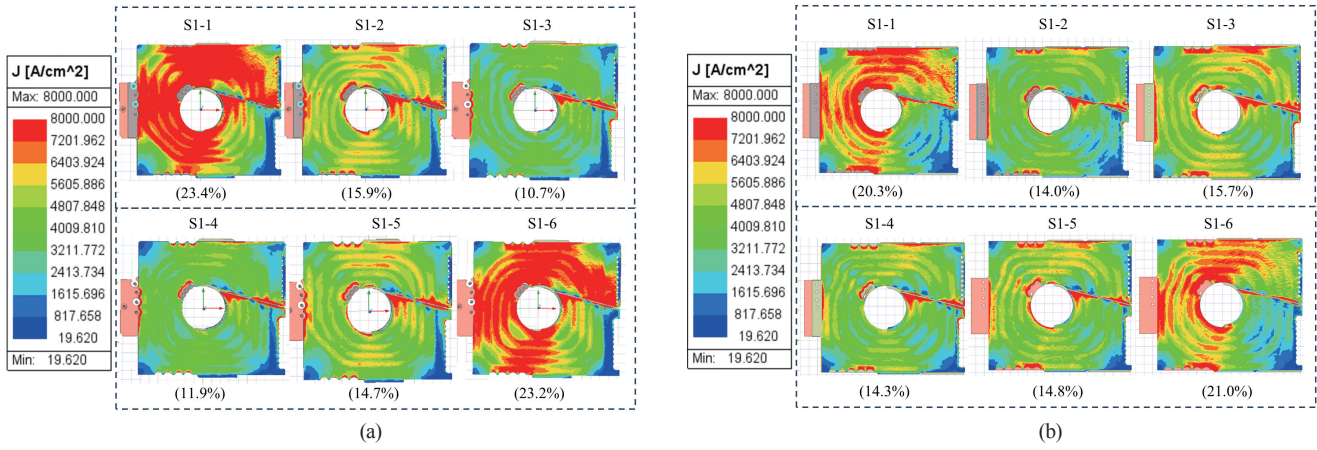


Fig. 10. Current distribution of secondary windings with (a) traditional connection and (b) proposed connection.

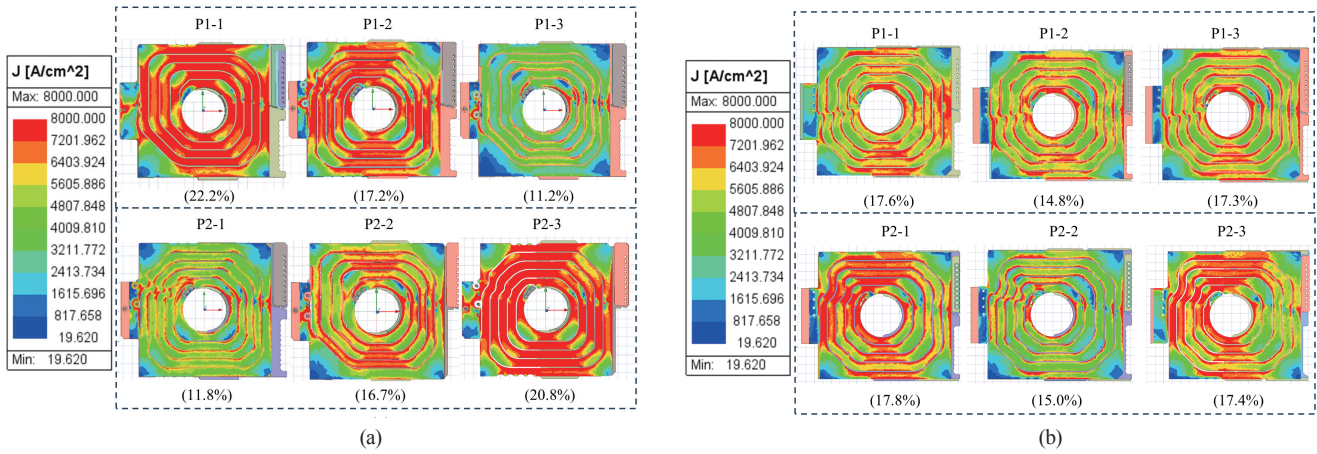


Fig. 11. Current distribution of primary windings with (a) traditional connection and (b) proposed connection.

ings have a significant impact on current sharing. The primary windings' connection significantly influences current sharing mentioned above. Because the rectification loops are placed on the PCB surface and all secondary windings operate in parallel, the layers closest to the surface have shorter conduction paths and therefore tend to carry more current. This uneven distribution mainly results in poor current sharing and increased winding loss.

Fig. 9(a) illustrates the proposed winding layout using the conventional connection scheme. In this connection leads to a pronounced imbalance in current distribution. The resulting secondary-side current profile, obtained from a Maxwell 3D finite-element model, is shown in Fig. 10(a). The current in the outer layer is 13% higher than that in the inner layer, and even exceeds twice that amount. And the primary has the similar phenomenon, as shown in Fig. 11(a).

Fig. 9(b) illustrates the revised connection strategy. In this scheme, the first primary layer is placed in series with the fourth, the second with the fifth, and the third with the final layer. By arranging the windings in this manner, the parallel primary paths obtain nearly identical conduction lengths, which in turn promotes a more uniform current distribution on the secondary side. Although connecting all primary layers entirely in

series could also equalize current, such a configuration limits the achievable turns ratio and enlarges the footprint due to the additional intermediate tapping points required. The resulting secondary current distribution for the proposed connection is shown in Fig. 10(b), derived from Maxwell 3D simulations. The difference in current density between outer and inner layers is reduced to about 6%, representing a substantial improvement over the traditional layout. Fig. 11(b) reveals that the primary winding currents P1 and P2, P3 and P4, along with P5 and P6, are identical. Furthermore, the inner layers of the winding effectively carry the current as well.

Furthermore, many existing studies and commercial products adopt an interconnection and current sharing approach in which the primary winding is configured in a fully series-connected mode, thereby enabling forced current sharing on the secondary side. The secondary side is arranged as described in the manuscript. For example, a schematic diagram of the 3 primary winding layer connection is shown in Fig. 12.

For a 10:1 turns ratio example, to maintain the same number of turns per layer in the primary winding, this winding connection scheme can only be implemented by connecting ten primary layers in series, with one turn per layer. In addition, each of the two secondary windings occupies ten layers, total-

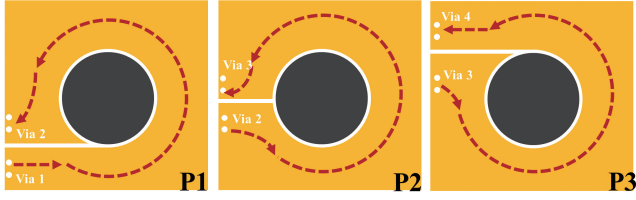


Fig. 12. Schematic diagram of primary winding layers of series connection.

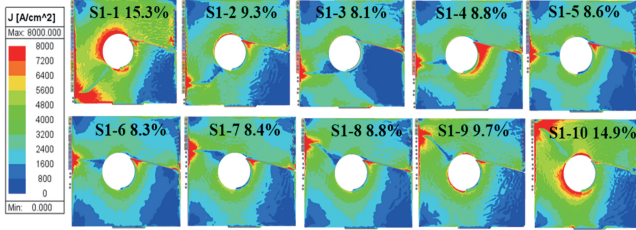


Fig. 13. Simulation results of current distribution in the secondary winding of series scheme.

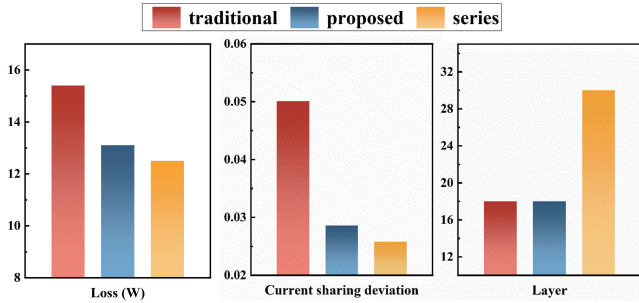


Fig. 14. Simulation results of current distribution in the primary winding with copper plating and via arrangement.

ing twenty layers. As a result, the entire transformer winding structure requires thirty layers in total.

A thirty-layer transformer was modeled and simulated, yielding a total loss of 12.5 W which got a reduction of 0.6 W comparing to the proposed current sharing scheme. The corresponding current distribution of winding are illustrated in the Fig. 13. The overall standard deviation of the current distribution is 0.0258.

It can be seen that the proposed scheme in this paper has better current sharing performance, and its loss is relatively close to that of the series scheme, but the number of layers is reduced by 40%. Compared with the traditional scheme, under the condition of the same number of layers, the current sharing performance is significantly better, and the effect of loss reduction of 2.3 W is also very obvious as shown in Fig. 14.

C. Terminal Loop Design

The high-frequency alternating current at the transformer output often leads to considerable terminal losses because the current tends to crowd at the kind of termination off the windings [28], [34] as shown in Fig. 15.

To mitigate this issue, many studies have adopted the ma-

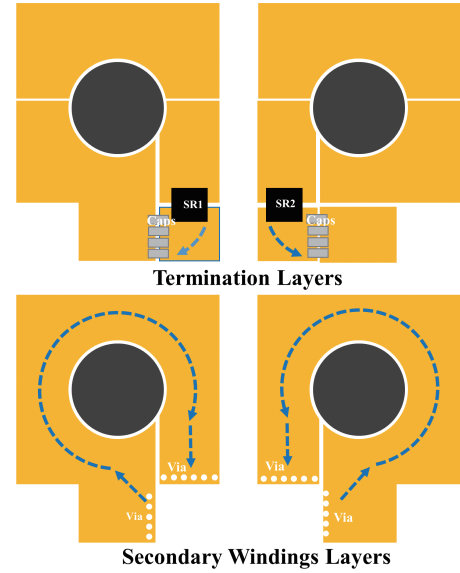


Fig. 15. Design of termination and secondary windings.

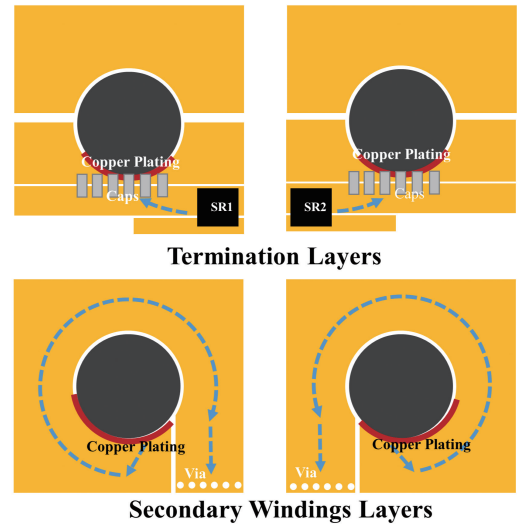


Fig. 16. Design of proposed termination and secondary windings.

trix-transformer concept. By dividing the secondary synchronous-rectification path into multiple isolated loops, this topology effectively lowers the secondary-side leakage inductance and AC resistance, resulting in reduced power dissipation [9], [21], [28], [29], [35], [36]. In particular, the work [37] introduced a configuration in which each secondary winding layer is routed to its own rectifier stage instead of directly paralleling all secondary layers. Furthermore, careful optimization of the commutation path on each PCB layer—together with the use of overlapping copper traces near the terminals—can further suppress AC resistance and substantially reduce associated losses.

For applications requiring a 10:1 turns ratio to achieve a low output voltage and high output current, the skin and proximity effects become more pronounced, leading to noticeable efficiency degradation and increased secondary-side voltage

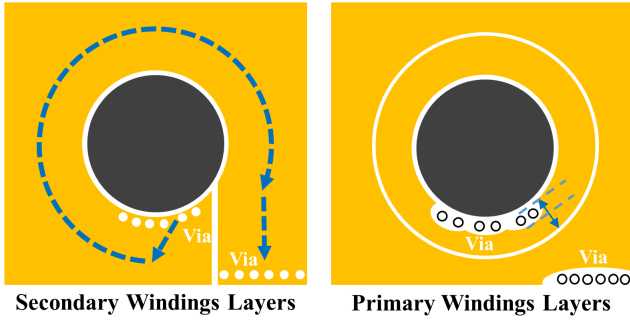


Fig. 17. Schematic of inner layer of secondary winding and primary winding with via connected.

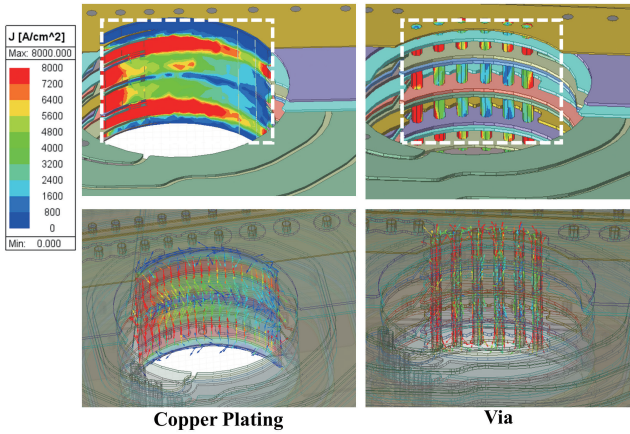


Fig. 18. Simulation results of current distribution of copper plating and Via.

drop. In this work, the structure of secondary side termination and winding are proposed as shown in Fig. 16. The current in the SR flows through the vias to the secondary winding layers and then returns through the copper-plated center hole, forming a complete conduction loop, which shortens the connection resulting in lower loss. In addition, PCB edge-copper plating is employed to expand the effective conduction cross-section, further mitigating high-frequency losses.

To clarify the advantages of the side-plating scheme, we performed numerical simulations for the non-plated approach, which relies on vias for implementation. A schematic of the winding layer structure for this design is shown in Fig. 18. A schematic of the winding layer structure for this design is shown in Fig. 17.

PCB fabrication is generally subject to process constraints. For heavy copper boards, the distance from the hole edge to other nets or to the board edge must be at least 15 mil or 8 mil, respectively, while the spacing between hole edges within the same net should exceed about 7.5 mil. Based on this layout, the simulated current density distribution is illustrated in the following Fig. 18. It can be observed that the current distribution of the copper-plating scheme is more uniform.

Because vias occupy a portion of the primary winding area, the primary winding exhibits a more pronounced current crowding effect. Moreover, numerical simulation results show that at 500 W, the copper-plating scheme has a noticeably lower loss—by

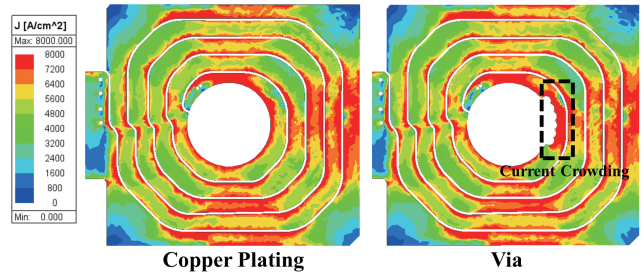


Fig. 19. Simulation results of current distribution in the primary winding with copper plating and via arrangement.

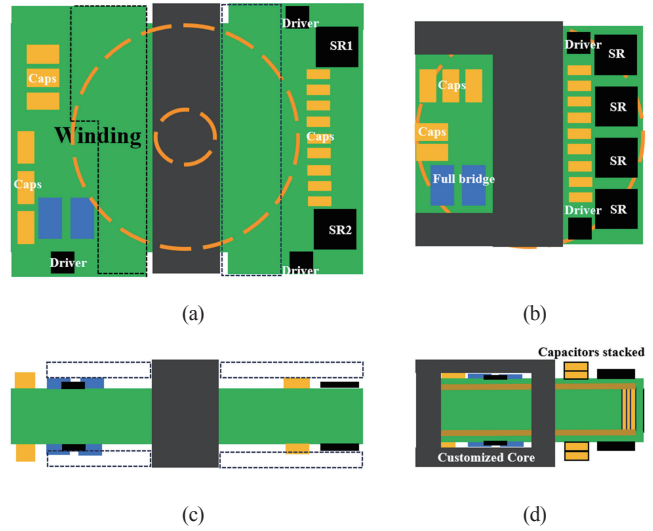


Fig. 20. (a) Top and (c) side view of traditional design. (b) Top and (d) side view of proposed high density integration design.

1.3 W—compared to the via-based scheme. This demonstrates that the copper-plating approach is conducive to achieving high efficiency and high power density. If the via-based scheme is to avoid the impact of via occupation while maintaining the same winding width, the planar dimensions would need to be extended by 0.7 mm, resulting in a current density of approximately 93% of the copper plating design.

D. High Density Layout Design

To alleviate these issues, this work adopts a dual-side rectification scheme, placing SR MOSFET on both top and bottom winding layers. The top and side views of a conventional power module are shown in Fig. 20(a) and (c). Due to the varying component heights, the internal space cannot be fully utilized, which ultimately limits the achievable power density. For a standard rectangular PCB, the magnetic core typically extends beyond the board's lateral dimension to allow proper mounting. This added overhang increases the converter's total width and, in turn, limits the attainable power density. In most designs, components are placed around the transformer and its windings, resulting in a larger module footprint. Consequently, the regions marked by the dashed boxes remain unused.

To improve area utilization and minimize the planar foot-

TABLE III
DIMENSIONS OF MAJOR COMPONENTS

Location	Part number	Area (mm)	Height (mm)	Quantity
GaN	EPC2053	3.5×2	0.88	4
GaN driver	LMG1205	2.0×1.8	0.6	2
Input capacitor	2.2 μ F/100 V	2.0×1.25	1.25	6
Resonant capacitor	220 nF/50 V	2.0×1.25	0.85	2
SR	IQE006NE2LM5	2×2	0.8	8
SR driver	ucc27614	1×0.5	0.5	4
Output capacitor	22 μ F/10 V	1×0.5	0.8	44

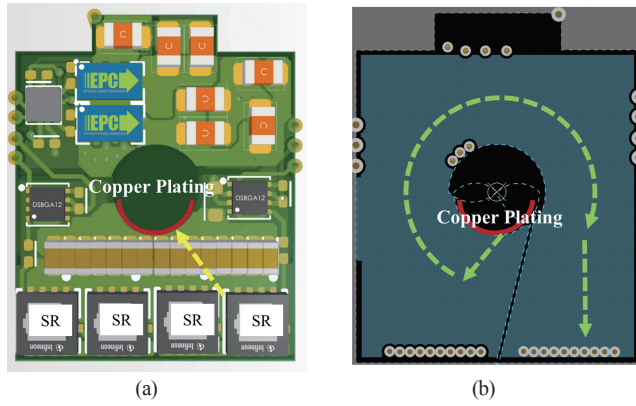


Fig. 21. PCB layout of (a) top layer of termination and (b) inner secondary layer.

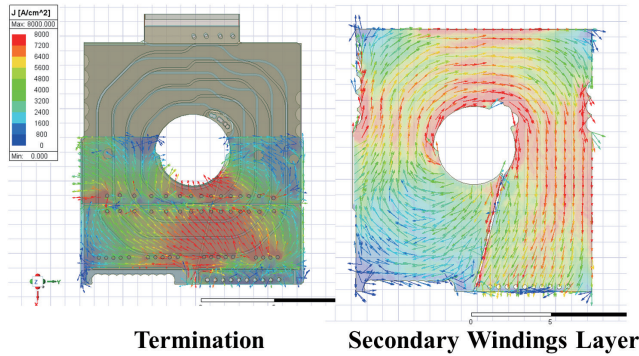


Fig. 22. Simulation results of current distribution and flow.

print, a high density integration approach is introduced. The overall concept is illustrated in Fig. 20(b) and (d). In this architecture, key components—including primary GaN switches, secondary rectifiers, capacitors, and gate drivers—are mounted directly above transformer windings with the same size. Based on the component dimensions listed in Table III, the driver ICs—only 0.5 mm in height and generating relatively little heat—allow a 1.5 mm magnetic core to be positioned directly above them. The output capacitors, each 0.8 mm tall and required in large numbers, are arranged in two stacked layers to reduce the overall footprint. The secondary MOSFETs, also 0.8 mm high but with considerably higher power dissipation, are

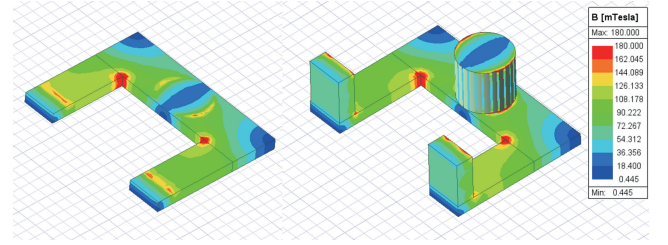


Fig. 23. Simulation results of magnetic core flux distribution.

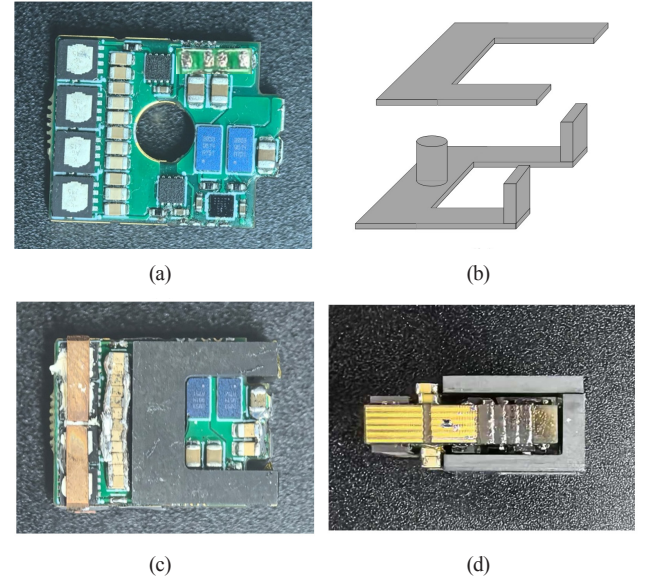


Fig. 24. Prototype with 3D stacking integration proposed. (a) Top view. (b) Core shape. (c) Top view under assembly. (d) Side view under assembly.

equipped with an additional heat sink to enhance thermal management.

Fig. 21(a) presents the PCB's top-layer layout based on the aforementioned design approach, while Fig. 21(b) shows the inner-layer structure of the secondary winding. The arrows denote the AC conduction path. The alternating current flows from the winding terminals through vias to the top layer, then passes through the SR MOSFET and capacitors before returning via the lower edge of the PCB opening. This edge is interconnected with the remaining layers through copper plating along the PCB rim. By creating a large overlapping region between the forward and return paths, this layout effectively reduces both AC resistance and secondary-side leakage inductance.

A Maxwell 3D finite-element model was developed to evaluate the proposed structure, and the resulting current distribution is illustrated in Fig. 22. The simulation shows that the rectification loop exhibits a uniform current profile, with no noticeable regions of current crowding. Fig. 23 shows the magnetic flux of core under a 6 V output condition, and core loss is 0.3 W.

Fig. 24 presents the prototype assembly. Fig. 24(a) shows the PCB top view, where the components are densely arranged, Fig. 24(b) illustrates the customized magnetic core geometry, Fig. 24(c) provides the top view of the assembled power mod-

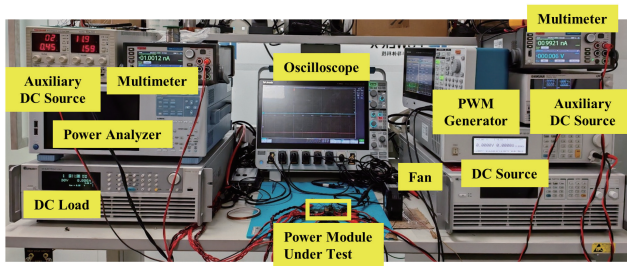
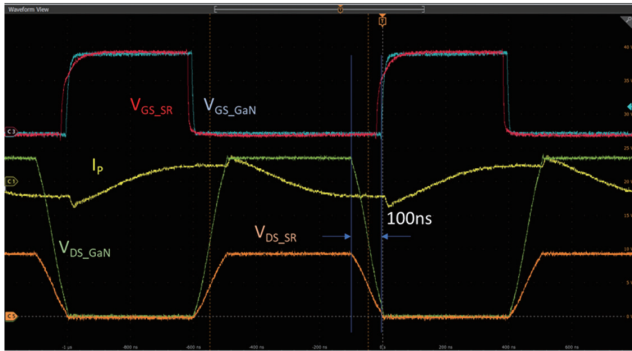
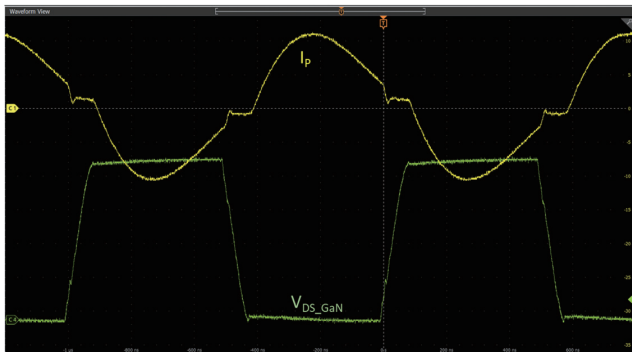


Fig. 25. Experimental platform.



(a)



(b)

Fig. 26. Waveforms of (a) open load and (b) full load at 48 V input.

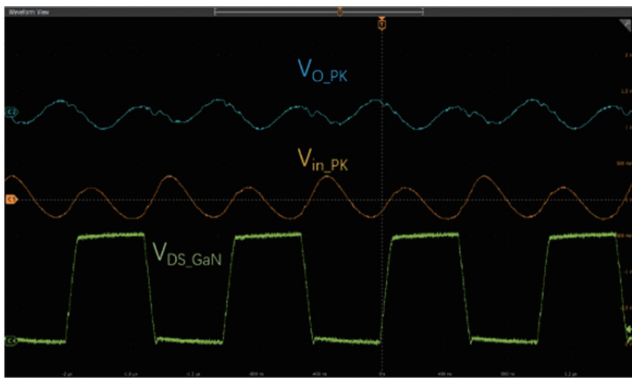


Fig. 27. Voltage ripple measured at 60 V input.

ule, and Fig. 24(d) shows the side view. The magnetic core adopts a special custom shape that extends over the driver IC and unused PCB regions, while its side legs are positioned at

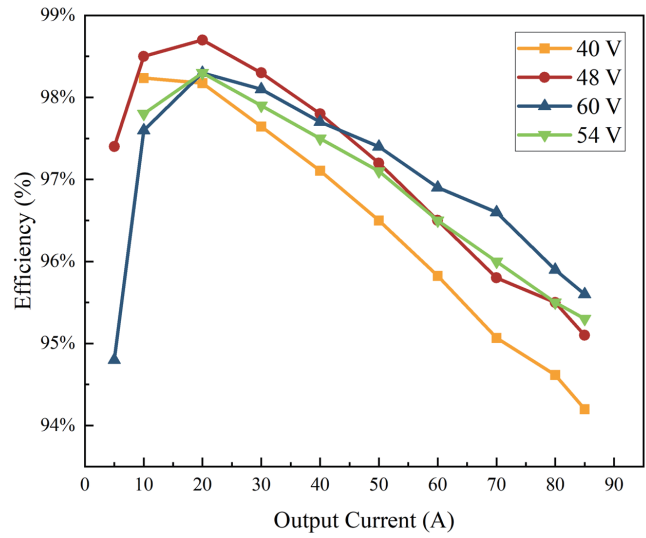


Fig. 28. Efficiency of prototype under different input voltages and output currents.

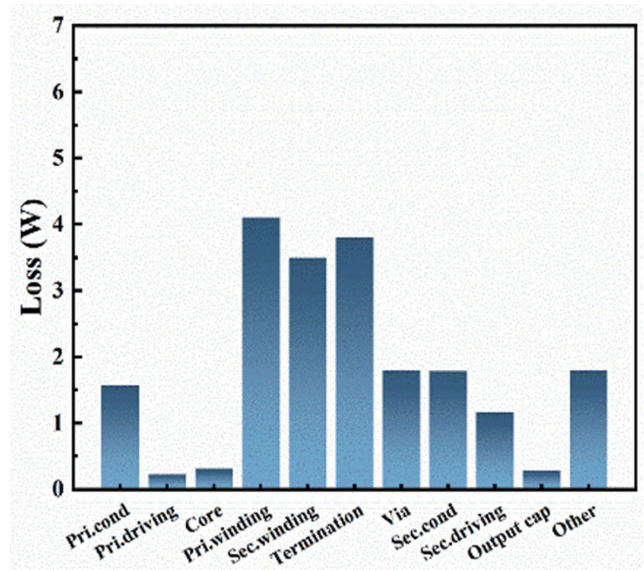


Fig. 29. Loss breakdown of DCX converter under 60 V input and 85 A output.

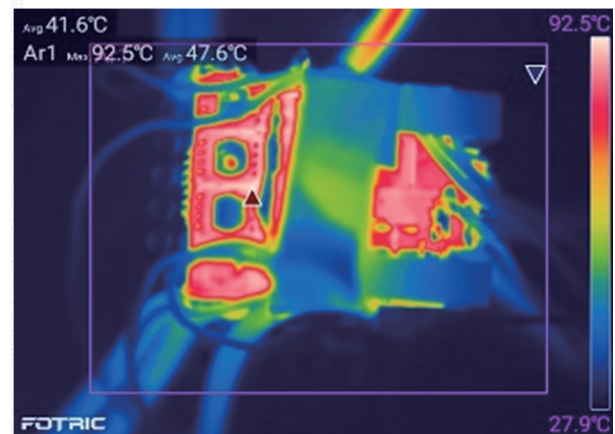


Fig. 30. Thermal image at 60 V input full load.

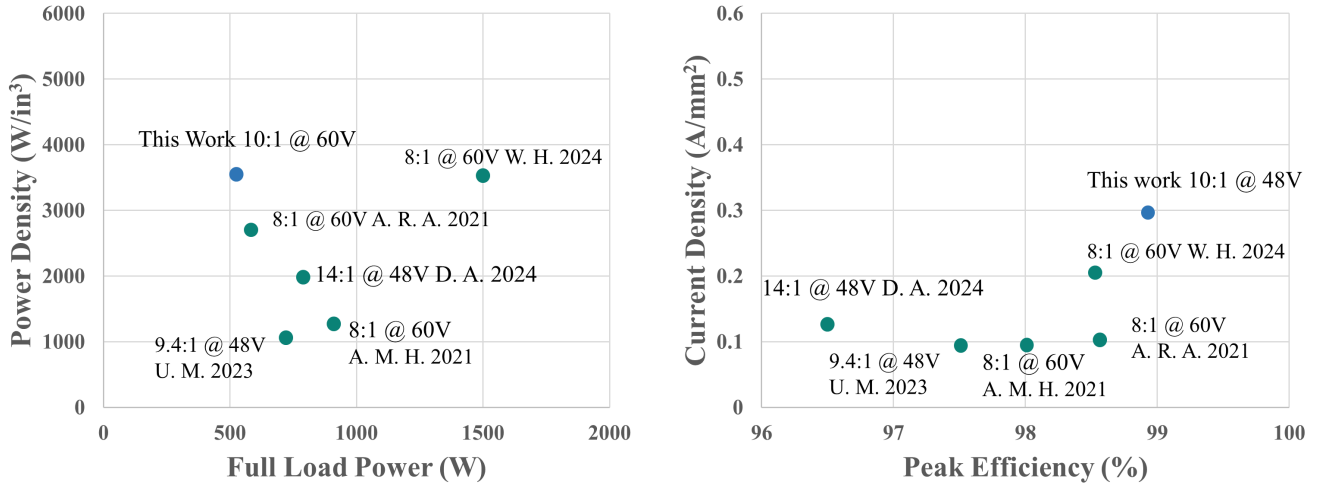


Fig. 31. IBCs with state-of-the-art [12], [14], [15], [28], [38].

the PCB corners so that no extra planar area is consumed. With this approach, the complete system occupies only $19 \text{ mm} \times 15.5 \text{ mm} \times 8 \text{ mm}$, corresponding to a planar area of 294.5 mm^2 and a total volume of 2356 mm^3 .

IV. EXPERIMENTAL VERIFICATION

The experimental setup is shown in Fig. 25. A Chroma 62150 supplies the 40–60 V DC input, while a Chroma 63203E operates as the constant-current load. The primary GaN devices and secondary SR MOSFET are driven by a 1 MHz PWM signal generated by a RIGOL DG5102. A Sorensen XPF 35-10 provides the 5 V gate-drive supply and 12 V for the cooling fan. The oscilloscope used in testing is a Tektronix AFG31000, and a KEITHLEY 2450 is employed to capture input and output voltage measurements. Temperature data are recorded using a FOTRIC 285 thermal imager.

Fig. 26 presents the measured waveforms under open-load and full-load conditions at a 48 V input. As shown, both the primary GaN switches and the secondary SR MOSFETs operate with zero-voltage switching. Fig. 27 illustrates the input and output ripple voltages at full load. The input ripple exhibits a peak-to-peak value of 620 mV, while the output ripple is 42 mV, confirming that the stacked capacitor design provides adequate filtering.

Fig. 28 shows the measured efficiency of the prototype. The converter achieves a peak efficiency of 98.7% at a 48 V input. Under full-load operation, the efficiencies at 60 V, 54 V, 48 V, and 40 V inputs are 95.9%, 95.5%, 95.3%, and 94.6%, respectively. The loss distribution of full load of 85A is illustrated in the Fig. 29. The current density and power density is 0.29 A/mm^2 and 3548 W/in^3 , respectively. The current density is defined as the electric current per unit bottom area of the power module. The prototype measures $19 \text{ mm} \times 15.5 \text{ mm}$ with a full-load current of 85 A. Fig. 30 shows the thermal image under full-load conditions at 60 V. Here, the highest temperature of 92.5°C is observed at the secondary devices in the absence of a heatsink. Fig. 31 presents a comparison of the demonstrated IBCs with state-of-the-art from literature [12], [14], [15], [28], [38].

V. CONCLUSION

This paper presents an LLC-based intermediate bus converter with a 10:1 turns ratio designed to deliver high power density, high current density and compact power processing. To address excessive winding and termination losses, a loss-suppression design has been implemented by optimizing the winding and termination structures as well as the inter-layer interconnection. Combined with a compact PCB layout design for the power module, the prototype's compliance with high-performance specifications has been ensured through a combination of numerical simulation verification and experimental testing.

A prototype capable of supplying 85 A was constructed to validate the approach. It achieves a current density of 0.29 A/mm^2 , a volumetric power density of 3548 W/in^3 at a 60 V input, and a peak efficiency of 98.8% under 48 V operation.

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