

Investigation of GaN HEMT Degradation in High Temperature Power Electronics Using Application Level Reliability Test

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Abstract—Extreme environmental and high-power density applications, such as those in oil and gas industry, rely on power electronic circuits to drive sensors and control systems. These circuits are often subjected to harsh thermal conditions and must demonstrate high reliability to ensure uninterrupted operation. Gallium nitride (GaN) based semiconductor switches offer several advantages over conventional silicon (Si) devices, including a higher breakdown electric field and superior electron mobility, enabling more efficient and compact power electronics. However, as a relatively new technology with immature epitaxial processes, GaN reliability remains a critical concern, particularly in applications where unexpected downtime can lead to substantial economic losses. In high temperature environments, this challenge is further amplified by the frequent need for devices to operate beyond their datasheet-specified limits. In this work we explore the reliability of different GaN power semiconductor technologies in these conditions using realistic test procedure that is very closer to an actual converter operation. Devices were stressed for extended durations of up to 1000 h with their static parameters continuously monitored. The collected data were analyzed to identify failure modes and their underlying root causes, providing insights into the robustness of GaN devices under extreme condition.

Index Terms—Down-hole power electronics, gallium nitride high electron mobility transistors (GaN HEMTs), high temperature, reliability.

I. INTRODUCTION

GALLIUM nitride (GaN) power semiconductor devices have gained adoption in a wide range of medium- to high-voltage applications recently, including consumer electronics, data centers, and robotics [1]–[4]. With advancements in their development, there is growing interest in extending their use to higher-power applications such as traction inverters and industrial drives. However, one area where the potential of GaN-based power switches remains rarely explored is high temperature power electronics.

High temperature power electronics are generally defined

as systems operating in ambient conditions exceeding 150 °C [5]–[7]. In such environments, the primary heat source is the surrounding medium rather than self-heating from device losses. A prominent example is downhole oil and gas exploration, where the Earth's geothermal gradient averages approximately 25 °C per kilometer of depth [8]. Recent trends toward deeper drilling, driven by declining resources, have elevated ambient temperatures in some wells to nearly 200 °C. Nevertheless, in most cases, downhole power electronics operate within an ambient range of 150–175 °C.

In such applications, a reliable power supply is critical for sustaining the signal chain responsible for acquiring essential data such as radioactivity, magnetic resonance, permeability, water/hydrocarbon saturation, lithology, porosity, pressure, temperature, vibration, and valve control. Any failure in this electronics infrastructure can halt operations for an entire day, resulting in potential losses on the order of millions of dollars [5]. Ensuring the reliability of such systems is therefore of utmost importance. This challenge is compounded by the already elevated ambient temperatures, where passive cooling methods such as heatsinks are ineffective and active cooling is neither economical nor practical in deep-Earth environments due to strict constraints on size and weight [9]. Components must therefore operate reliably at elevated junction temperatures. Unfortunately, most devices, including semiconductors, capacitors, and integrated circuits, are rated for maximum operating temperatures of only 125–150 °C, making it difficult to source components that guarantee long term reliability under these conditions. A common mitigation strategy is derating, particularly for power semiconductors and ICs, by operating them well below their rated electrical limits [10], [11]. Furthermore, it is standard practice to define a finite operating lifetime for each power converter, typically 200 to 1000 h, depending on the application's criticality and environmental severity, after which the units are replaced. However, it remains imperative that no unit fails within its specified operational period, as such failures can result in substantial economic losses from unplanned downtime. The degradation of standard semiconductor material performance and reliability at high temperatures is a well-documented issue [12]. One major concern is the increase in intrinsic carrier density with temperature [13]. At sufficiently high temperatures, the number of thermally generated electrons in the undoped regions of a device can approach that of the

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TABLE I
ELECTRICAL PROPERTIES OF SEMICONDUCTORS AT 200 °C AS PER

Semi- conductors	E_g /eV	$v_{sat}/(\times 10^7 \text{ cm} \cdot \text{s}^{-1})$	$E_{BR}/(\text{kV} \cdot \text{cm}^{-1})$	$K/(\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-1})$
Si	1.07	< 0.85	> 300	90
SiC	2.79	1.55	> 2400	230
GaN	3.11	2.02	> 5000	100

doped regions, effectively eliminating controllability. Another critical issue is the exponentially rising leakage current, which increases power losses, elevates junction temperature, and can ultimately lead to thermal runaway [14]. In addition, key material parameters, such as the strength of dielectric breakdown and the velocity of electron saturation, decrease at elevated temperatures, further degrading the device performance [15]. Mechanical reliability is also challenged by thermal stress resulting from the coefficient of thermal expansion (CTE) mismatch between materials in the device package, as well as electromigration [16] in conductive regions, both of which contribute to long-term degradation and potential failure. GaN offers significant advantages over silicon (Si) in addressing some of these challenges. For example, GaN exhibits a much lower intrinsic carrier density compared to Si, meaning that its junction temperature must reach a substantially higher level before intrinsic carriers surpass the dopant concentration. Moreover, GaN maintains comparatively high breakdown electric field and electron saturation velocity even at junction temperatures around 200 °C (Table I) [15]. Despite these advantages, commercially available GaN power devices are not purely GaN-based; but are lateral high electron mobility transistors (HEMTs) grown on foreign substrates, typically Si [17]. The presence of Si in the die offsets some of GaN's inherent benefits, and the final device characteristics are strongly influenced by the epitaxial process. Additionally, GaN HEMT architectures are not standardized; commercial GaN devices are available in various configurations, including schottky p-GaN HEMTs (SP-HEMT), hybrid drain gate injection transistors (HD-GIT), cascode structures, and integrated GaN solutions with embedded gate drivers. Therefore, post-process validation of these devices under realistic conditions is essential before their deployment in high temperature applications.

Literature indicates that several studies have investigated the performance of GaN HEMTs under elevated temperatures. Lundh et al. [18] employed electrical characterization techniques, including DC and pulsed I - V measurements, up to 600 °C, while Jiang et al. [19] utilized double-pulse testing to assess dynamic on-state resistance at high junction temperatures. Dong et al. [20] measured transient data across a range of temperatures up to 175 °C to develop electro-thermal models for predicting high temperature behavior. From a robustness perspective, Fleury et al. conducted step-stress testing up to the breakdown limit and observed a sharp reduction in break down voltage as temperature increased from 25 °C to 420 °C [21]. [22] subjected GaN devices to prolonged exposure at 500 °C, noting stable threshold voltage but degradation in on-state resistance

and saturation current. Furthermore, [23] performed in situ transmission electron microscopy (TEM) heating up to 800 °C, revealing critical degradation mechanisms such as gate metal lization recession and field plate deterioration. However, there remains a significant gap in understanding the long-term reliability of GaN power devices under continuous high temperature switching conditions, which is essential for mission-critical applications. The reliability of GaN HEMTs is an active area of research [24]–[26], as these devices are relatively new to the market and field data remain limited. In addition to conventional reliability tests developed primarily for Si devices, such as high temperature gate bias (HTGB), high temperature reverse bias (HTRB), and power cycling, manufacturers also conduct extended reliability evaluations under more realistic switching conditions [27]–[32]. These are commonly referred to as dynamic high temperature operating lifetime (DHTOL) tests or simply application reliability tests, designed specifically to address the reliability concerns associated with the heterostructure of GaN HEMTs. In such tests, stress profiles are chosen to mimic operating conditions representative of the target applications. Typically, stress is applied at voltage and/or temperature levels above the intended application case but still within the datasheet-specified limits. However, for extreme environments such as downhole applications, devices are required to operate at ambient conditions that exceed these limits. Consequently, thermal stress levels in testing must be set above nominal operating temperatures for these applications, but also remain below the threshold that could induce immediate thermal runaway.

The primary objective of this study is to investigate the potential failure mechanisms of different commercially available GaN HEMT technologies when subjected to prolonged switching operation at high temperature conditions. Such conditions are typical in the oil and gas industry, where ambient temperatures often exceed 150 °C and surpass the datasheet limits of most commercial devices. This work is aimed at bridging the gap in literature regarding the long-term reliability of GaN under such conditions, specifically the ones associated with cumulative degradations occurring during extended operation. To facilitate this study, a test bench is developed, which can apply realistic system-level stress on GaN devices at extreme temperatures, while also preventing any temperature-related non-GaN failures. The applied electrical stress profile of the test setup is based on a flyback converter topology. Using the developed test setup, multiple samples form three different commercial enhancement-mode GaN device architectures are stressed for prolonged duration to facilitate a comparative assessment of their robustness. Based on the observed results, the most vulnerable device structures are further examined using cross-sectional electron microscopy to identify the underlying failure mechanisms and points of weakness. In addition, key electrical parameters of the tested samples are characterized throughout the test at regular intervals. This is helpful in keeping track of the device parameter degradations throughout aging. The results of this study could be useful for developing real-time reliability enhancement techniques, such as state of health monitoring solutions. These approaches can help prevent cata-

strophic device failures that may lead to unplanned downtime and are particularly beneficial for mission-critical industrial applications.

II. EXPERIMENTAL TEST SETUP

The reliability and robustness of traditional Si devices are typically evaluated using standardized tests specified by governing bodies such as JEDEC and AEC-Q. According to these standards, separate accelerated lifetime tests are conducted to assess weaknesses in different regions of the device. For example, HTGB and HTRB for gate oxide reliability, power cycling for package integrity, and unclamped inductive switching for avalanche ruggedness of PN junctions. Although most GaN vendors adopt these conventional qualification practices, they may not always provide an accurate representation of GaN HEMT reliability due to structural differences, such as the absence of a body diode and gate oxide. To address these limitations, JEDEC has recommended the use of DHTOL testing, performed with system-level product test vehicles, to comprehensively evaluate HEMT reliability. Consequently, in this study, DHTOL testing has been chosen to comparatively assess the robustness of different GaN device architectures under high temperature conditions. To achieve this, a highly scalable and modular test bench featuring five independent test vehicles has been developed. In most oil wells, power is generated using a turbo generator and typically distributed via a DC bus operating at voltage levels between 150 V and 350 V [33], [11]. This voltage must be stepped down to 5–12 V to meet, the requirements of sensors and control valves, using power converters that must also function reliably under extreme temperatures. For this range of voltage conversion, the flyback converter is the most commonly used topology due to its low component count and high gain step-down capability. Consequently, the test vehicles selected for the developed DHTOL test bench are implemented in the form of flyback converters, as initially introduced in [34]. Fig. 1 shows the schematic of the test vehicle circuit along with simulated current and voltage waveforms. Further details regarding parameter selection and circuit operation can be found in [34].

Fig. 2(a) illustrates the developed test bench consisting of five test vehicles. Each test vehicle (Fig. 2(b)) is dedicated to stressing a single device under test (DUT), which is mounted on a plug-in adapter card (Fig. 2(c)). This modular setup allows DUTs to be easily inserted and removed from the test bench for characterization using an external analyzer, enabling periodic monitoring of parameter variations during the stress process. Each adaptor card is designed with footprints that correspond to the specific GaN HEMT part numbers selected for testing. Thermal stress is applied through heat generated by a wire-wound resistor mounted on top of the DUT in the adapter card. A k-type thermocouple, placed between the heating resistor and the DUT, senses the applied thermal stress, as illustrated in Fig. 2(d). The heat level is controlled by adjusting the power dissipated in the resistor, achieved by regulating the current through it via the duty cycle of a solid-state relay connected in

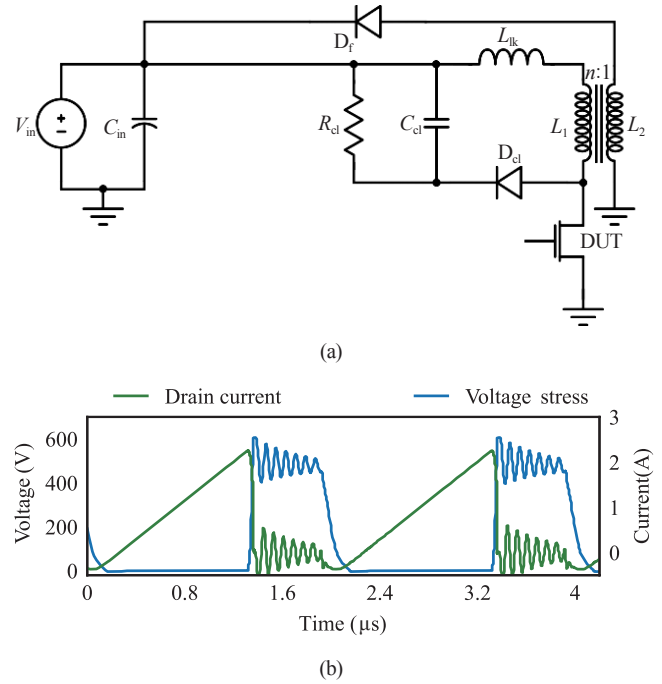


Fig. 1. Test vehicle overview. (a) Schematic of the power circuit of the test vehicle. (b) Simulated result of the voltage and current stress applied to the DUT.

series. Each test vehicle is equipped with an F280029 microcontroller, which provides the gate-drive signals for the DUT. The thermocouple output is conditioned and fed to the microcontroller's ADC, where a PI controller adjusts the relay duty cycle to regulate the thermal stress according to a predefined reference temperature. The turns ratio of the flyback transformer is selected to be 2:1, resulting in a steady state voltage stress of three times the input DC link voltage as per the relation, $V_{DS} = (1 + n)V_{in}$ [34]. The peak transient voltage is controlled by adjusting the clamp resistor. In the event of a short circuit failure of a DUT in any of the test vehicles, the failed device can short out the entire DC link, rendering all test vehicles inoperable. To mitigate this risk, fuses are incorporated into the input connections of each test vehicle in the test setup. The fuse ratings are carefully selected on the basis of the set output current limit of the DC supply. If a short circuit occurs in a test vehicle, the corresponding fuse will react and disconnect the faulty unit from the test bench, allowing the remaining test vehicles to continue operating normally. The primary motivation for selecting this specific test vehicle circuit topology lies in its convenience: avoiding the need for a load dissipation element and minimizing power loss while effectively replicating high-frequency converter level switching stress on the DUTs. However, any potential insights gained from this study are not limited to flyback converter applications, but are broadly applicable to general switch-mode power supply systems operating under extreme temperature conditions.

III. DEVICE TESTING AND OBSERVED PARAMETERS VARIATIONS

The main objective of this study is to compare the robustness of various GaN HEMT architectures under application level

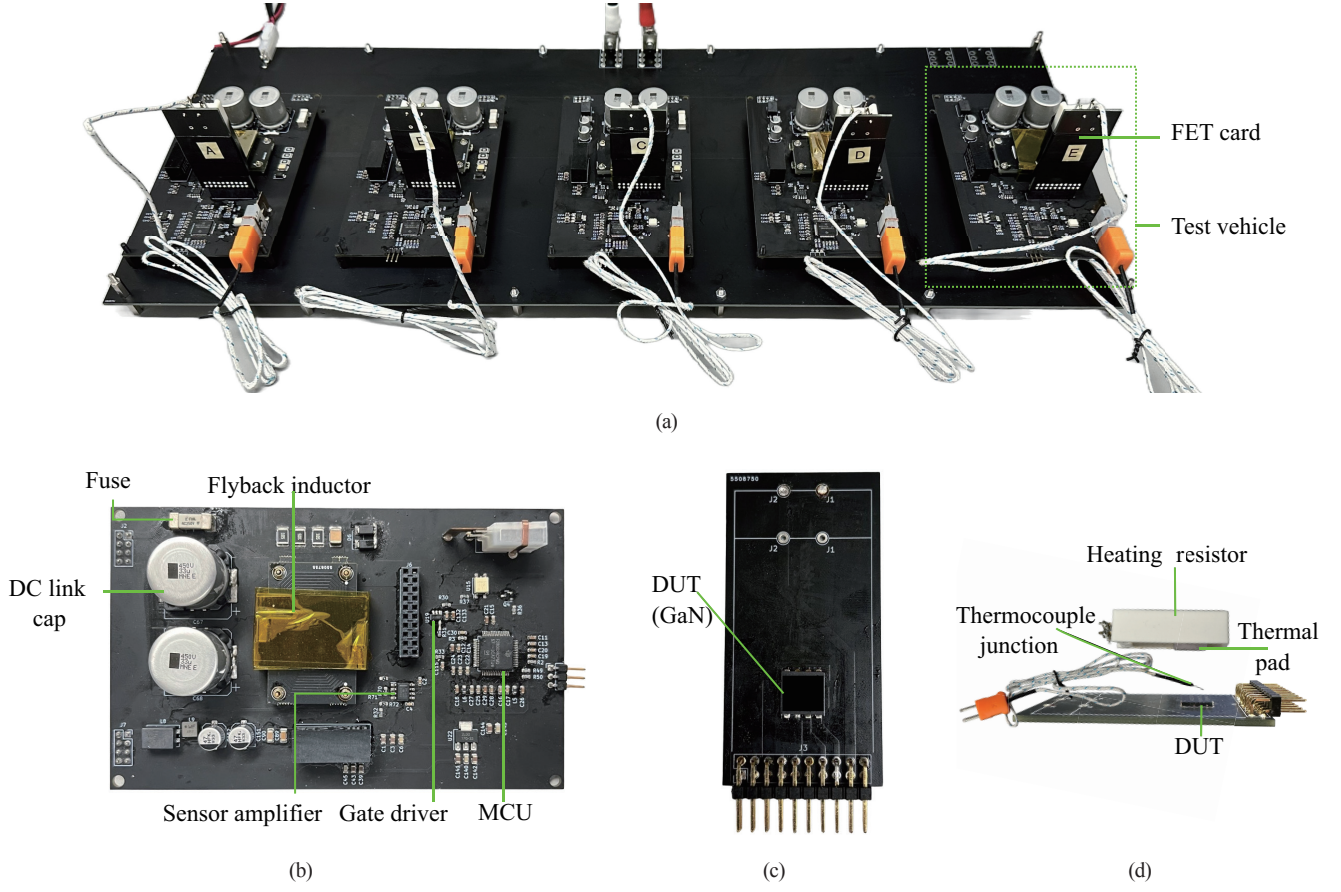


Fig. 2. Developed experimental setup. (a) Complete test bench rack featuring five test vehicles. (b) Individual test vehicle designed based on flyback converter. (c) FET card for housing DUT; plug-in nature allows for easy place in and out of test vehicle for periodic characterization. (d) Application of thermal stress on DUTs using a heating resistor, device case temperature is sensed via a thermocouple with junction positioned between the heater and DUT.

ambient temperatures of 150–175 °C and identify potential architecture specific failure mechanisms. For testing, four different GaN part numbers are selected with specifications as illustrated in Table II. Since the majority of GaN devices currently available in the market are of the Schottky p-GaN type, two-part numbers from separate vendors are chosen, hereafter referred to as SP-HEMT1 and SP-HEMT2. The remaining two devices consist of one part number each from the gate-injection transistor (HD-GIT) and cascode families. Integrated GaN devices are excluded from this study because most commercially available options specify a maximum junction temperature of only 125 °C and incorporate Si-based driver and protection circuitry, which complicates the isolation of intrinsic power device failure mechanisms. All selected devices are of SMD packaging. Among them, SP-HEMT2 features a copper clip interconnect, while the remaining devices utilize conventional wire-bonded interconnections.

Five samples of each (labeled A-B-C-D-E) of the four selected GaN HEMT parts are chosen for testing and subjected to DHTOL-level stress for an intended duration of 1000 h per device. While performing application reliability test, JEDEC recommends keeping one or two operating conditions near the application extreme [35]. The application power level being considered in this study is low to medium power supplies, such as those used

TABLE II
DUT DATA SHEET PARAMETERS

Device types	$V_{DS,max} / V$	$R_{DS(on)}^* / m\Omega$	$R_{th,jc} / (^\circ C \cdot W^{-1})$
SP-HEMT1	650	175	0.65
SP-HEMT2	650	170	0.7
HD-GIT	600	100	1.1
Cascode	650	62	0.5

*: $I_d = 1 A$, $T_j = 185 ^\circ C$.

for powering signal acquisition chain. In this power level, most significant GaN reliability concern arises from movement of charges within the heterostructure or buffer region failures [36], both of which are strongly influenced by the electric field distribution across the device. Consequently, along with temperature, drain voltage stress is chosen as an extreme operation. The devices selected for testing in this study all have a datasheet limit of 600–650 V for V_{DS} and a T_j limit of 150 °C. The applied thermal stress is selected to be 185 °C, corresponding to a typical application extreme, which is 35 °C above the device ratings. Accordingly, a rule of thumb is employed to derate the voltage stress extreme in context to its maximum limit to avoid any immediate dielectric breakdown. The voltage stress limit is

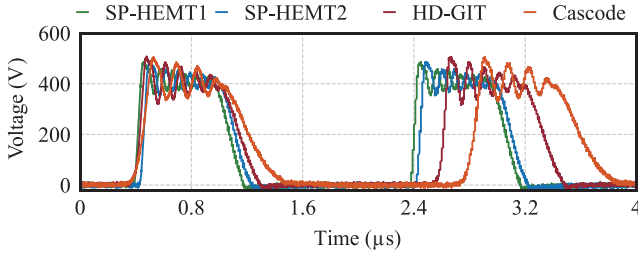


Fig. 3. Experimental waveform of voltage stress across the DUT for different device types.

derated by 1% for every degree increase in temperature above its datasheet limit. Consequently, $(1-0.35) \times 600 \approx 400$ V is selected as the applied plateau voltage stress. Although high temperature applications typically warrant even larger derating margins, the 400 V limit is retained to preserve a modest acceleration factor. To facilitate a fair comparison, it is essential to ensure that the junction temperatures of all tested devices are in a respectable range at the start of the test. For this test, vehicles are operated in soft switching mode, emulating a quasi-resonant (QR) flyback operation to eliminate switching losses. To achieve this, the frequencies are adjusted for each device from 420 kHz to 500 KHz as illustrated in Fig. 3. In addition, peak current stress is set around 1.2 A, resulting in an RMS current of less than 1 A, which is well below the rated current of the devices and thereby minimizing the conduction losses. Consequently, the total losses would be minimal and as per the details in Table II, the calculated junction temperature of all devices at the start of the test would be very close to the controlled case temperature value. Similar practices of minimizing self-heating through derating are common in field applications involving high ambient temperature to prevent the T_j from raising beyond a safety limit. Gate drive voltages are set according to the datasheet recommendations: 5 V for the two SP-HEMT devices, and 12 V for the cascode device. For gate injection transistors, it is often recommended to use a specialized driver circuit that enables high current injection at turn-on to achieve fast slew rate but also minimizes the leakage during the steady on-state. However, in this experiment, the system is operating in DCM mode, and hence the slew rate is not important. Consequently, a gate drive voltage of 3.5 V and gate resistance of 20 Ω is employed to limit the average gate input current.

Each sample is subjected to DHTOL testing until failure or up to 1000 h of stress, whichever occurred first. In this study, a device is classified as "failed" when it experienced catastrophic failure, resulting in short or open circuit conditions, or when it underwent soft failure, where the device remained functional but exhibited abnormal parameter shifts that rendered it practically unusable. The DHTOL stress is applied in sets of 20-h intervals, after which the DUTs are characterized using a Keysight B1506A power device analyzer. A relaxation period of one hour is allowed prior to characterization to ensure that the device temperatures returned to the ambient temperature. Table III summarizes the test outcomes for each device type. All five HD-GIT samples experienced catastrophic breakdown, whereas all

TABLE III
DHTOL TEST SUMMARY, PINK-CATASTROPHIC FAILURE, YELLOW-SOFT FAILURE, BLUE-NO FAILURE h

Device types	A	B	C	D	E
SP-HEMT1	440	600	1000	1000	1000
SP-HEMT2	1000	440	1000	40	1000
HD-GIT	40	260	280	300	220
Cascode	1000	1000	1000	1000	1000

cascode devices successfully withstood the full 1000 h of testing without failure. Among the SP-HEMT1 samples, one device exhibited soft failure, another suffered catastrophic breakdown near the end of the test duration, and the remaining three completed testing without failure. For the SP-HEMT2 devices, two samples experienced non-catastrophic soft breakdown, one being an early failure, while the remaining three survived the entire test duration. The remainder of this section provides a detailed discussion on how each of the measured parameters evolved across the test duration, highlighting the nature and extent of degradation or the absence thereof observed in the different device types.

A. Drain Leakage Current (I_{DSS})

For all 20 tested samples across the four categories, the drain leakage current is measured at a drain blocking voltage of 600 V with the gate-to-source voltage set to zero, and the results are illustrated in Fig. 4. The initial drain leakage current for the SP-HEMT devices ranged from tens to hundreds of nA, while for the HD-GITs and cascode devices it is in the order of μ A. Within the SP-HEMT group, one device exhibited an abrupt increase in leakage current to hundreds of μ A range after approximately 440 h of stress. Although the device remained functional with no observable degradation in other parameters, it is classified as a soft-breakdown failure and is removed from further testing. Another sample in this group suffered a short-circuit failure at around 660 h, accompanied by the expected sharp rise in leakage current. Similar behavior is observed in two of the SP-HEMT2 samples: one experienced an early soft breakdown after just 40 h of testing, while another failed close to the 440-h mark. The remaining samples from both SP-HEMT1 and SP-HEMT2 exhibited no significant change in drain leakage current throughout the test duration.

For the tested samples from HD-GIT family, one device experienced an early short-circuit failure after just 40 h of stress, resulting in the expected sharp increase in leakage current. Among the remaining samples, three devices (B, C, and E) exhibited a sudden rise in leakage current to 5–10 times their initial values within the first 40 h of stressing. Beyond this point, the rate of increase remained minimal until all three eventually succumbed to catastrophic breakdown before reaching 300 h. The fifth sample (D) showed a relatively gradual degradation with leakage current increasing to nearly three times its initial value before ultimately failing through short-circuit break down.

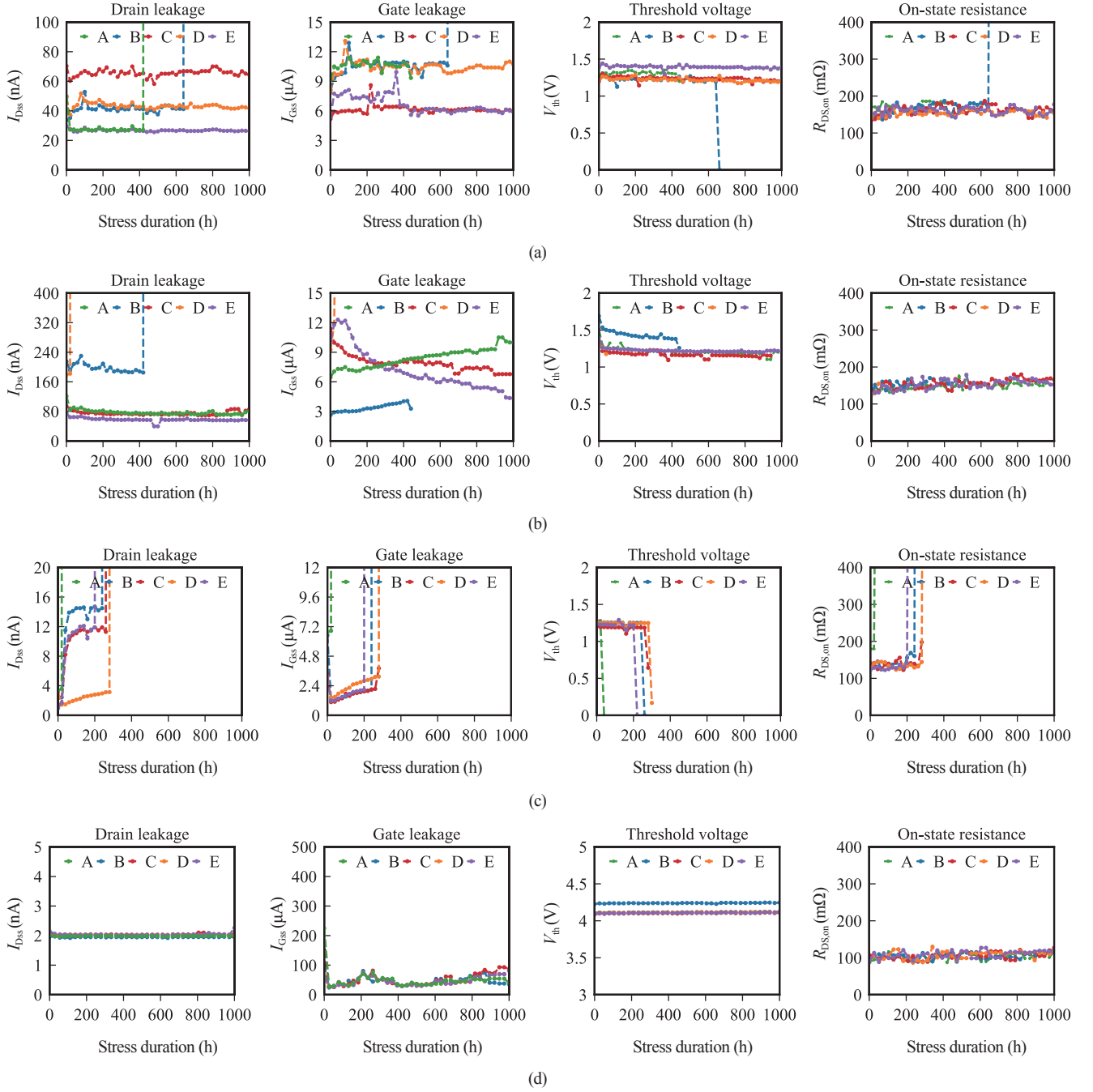


Fig. 4. Measured electrical parameter values of the tested devices across the 1000-h application reliability test duration. (a) SP-HEMT1. (b) SP-HEMT2. (c) HD-GIT. (d) Cascode.

The cascode device samples maintained a nearly constant drain leakage current of approximately 2 μA throughout the entire 1000-h test duration, showing no signs of degradation or abnormal shifts.

B. Gate Leakage Current (I_{GS})

For the SP-HEMT devices, the gate leakage current is measured at the datasheet specified best biasing condition of 5 V with drain and source terminals shorted to each other. For all survived samples from SP-HEMT1, the gate leakage current

value remained close to the original value throughout the test duration. For the device experienced the soft breakdown, the parameter remained almost similar to the initial value after the failure. The device experienced catastrophic failure, shown a step increment in the parameter after its breakdown. For the survived samples from SP-HEMT2, two samples (B and E) showed a slight decrease in the parameter, while the sample A exhibited a slight decrease. However, in both cases the variations remained within a very narrow range, and can be neglected in the scale used to convey any parameter degradation.

The term gate leakage is somewhat non-trivial for gate injection devices, since at the nominal driving voltage, the gate is designed to conduct a defined injection current, as implied by their name. In these devices, the gate–source junction behaves like a diode, exhibiting a forward voltage drop in the range of 3–3.5 V. Therefore, when the applied gate voltage is below this threshold, ideally no current should flow into the gate, and any current measured under such conditions can thus be classified as leakage current. Consequently, in this study, the gate leakage current for HD-GITs is measured by applying a 2 V bias between gate and source, with the drain shorted to the source. As illustrated in Fig. 4(c), the gate leakage current gradually increased with stress duration until each device ultimately failed through short-circuit breakdown, at which point the leakage exhibited a sudden sharp rise.

For the cascode devices, which employ a Si-oxide gate, gate leakage is measured at the datasheet-specified maximum bias of 20 V. Owing to their insulated oxide structure, these devices inherently exhibit much lower leakage currents, typically in the pA range, compared to conductive-gate devices. During stressing, an initial dip in leakage current is observed after the first measurement at the 20-h mark, decreasing from the hundreds of pA to just tens of pA. This behavior is likely attributable to hole trapping within the oxide region, a phenomenon also reported in Si and SiC devices [37]. Beyond this initial dip, the gate leakage current of all tested cascode samples remained nearly constant throughout the entire test duration.

C. Threshold Voltage (V_{th})

In this study, the threshold voltage is defined as the gate voltage required to achieve a drain current of 5 mA. For the SP-HEMTs and HD-GITs, the original threshold voltage is measured in the range of 1–1.5 V, whereas for the cascode device it is usually higher, at 4–4.5 V, due to the presence of the Si device acting as the driver stage. Among the SPHEMT samples, the surviving devices showed no significant change in threshold voltage, while those that experienced soft breakdown exhibited a slight reduction of 0.1–0.2 V. This reduction is likely attributable to the increased leakage current rather than to any degradation to the gate turn-on properties of the devices. For HD-GITs, no consistent trend in the threshold voltage variation is observed prior to their catastrophic breakdown. Likewise, none of the tested cascode devices showed no measurable deviation in threshold voltage values throughout the aging process, indicating the absence of gate-related degradation.

D. On-State Resistance ($R_{DS,on}$)

Accurate measurement of the on state resistance $R_{DS,on}$ of SMD devices using a power device analyzer is challenging, since the measured value inherently includes contributions from the device itself, the resistance of the adapter card, and the resistance of the solder joints. In this study, the difficulty is further compounded by the elevated temperature maintained over a prolonged period, which subjected the solder layer to deformation during testing. Such issues are uncommon in practical

TABLE IV
SIGNIFICANT ELECTRICAL PARAMETER DEGRADATIONS OBSERVED FOR EACH TEST CASE (CATASTROPHIC FAILURES EXCLUDED)

Device types	I_{DSS}	I_{GSS}	V_{th}	$R_{DS,on}$
SP-HEMT1	✓	×	×	×
SP-HEMT2	✓	×	×	×
HD-GIT	✓	✓	×	×
Cascode	×	×	×	×

high temperature power electronics, where superior soldering practices are employed. Consequently, only significant changes in $R_{DS,on}$, typically arising from bond wire failures or other forms of package degradation, are considered meaningful. The resistance of all devices is measured using a pulsed current of 1 A with a 100 μ s duration. Throughout testing, none of the devices exhibited a notable shift in this parameter that would indicate bond wire failure. However, samples that experienced catastrophic breakdown showed a sharp increase in $R_{DS,on}$. Post-testing analysis revealed that this is due to degradation of the solder joint caused by the surging short-circuit current occurring in the brief interval before the fuse disconnected the respective test vehicle from the DC input.

Table IV summarizes the electrical parameter degradation observed across each device category evaluated in this study, indicating whether at least one tested sample exhibited a significant shift in the measured parameters.

IV. FAILURE ANALYSIS AND DISCUSSION

Among the tested device types, the HD-GIT devices are found to be the most vulnerable under high temperature operating conditions, with all samples experiencing catastrophic failure within 500 h of testing. To gain further insight into the nature of these failures, the affected devices underwent detailed physical examination. Exterior of the device package showed no visible cracks or burn marks, ruling out the possibility of extrinsic thermo-mechanical failure. Additionally, one of the failed samples is decapsulated for closer inspection, as illustrated in the optical micrograph of Fig. 5(a). From the micrograph, burn-out marks were observed on the die, indicative of thermal runaway, with the damage localized near the source region, completely breaking down that area. However, all bond wires connecting the drain, source, and gate terminals remained intact, ruling out any package-related failures. To investigate the origin of the breakdown, the sample is subjected to scanning electron microscope (SEM) characterization, as shown in Fig. 5(b). The analysis revealed that the breakdown occurred almost exclusively within the device drain. The drain structure is partially or completely destroyed with some material debris remaining, whereas the source structure appeared to remain intact. For further insight, a scanning electron microscopy-focused ion beam (SEM-FIB) dual-beam technique is performed to obtain a crosssectional view of the device and reveal its internal structural changes. The FIB is used to milling and cutting the device to

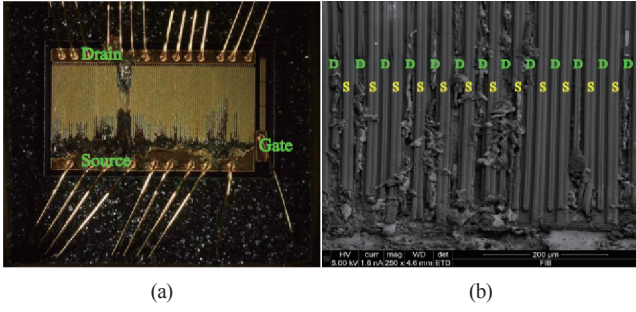


Fig. 5. Imaging results of a failed HD-GIT sample. (a) Optical micrograph of the decapsulated device sample. (b) SEM image showing the top view of the failed device sample.

make cross-section of the device, while the SEM is used to image the device cross-sections. The cross-sectional cuts were made at both the unaffected and breakdown regions of the device as illustrated in Fig. 6(a)–(c). The cross-sectional image of the device in Fig. 6(a) is taken from the unaffected region and clearly represent the intact device structure, which is consistent with a healthy HD-GIT structure. However the results in Fig. 6(b) show that the drain metal contact had melted, collapsed, and even diffused into the channel region, resulting in a localized short circuit. In addition, complete drain breakdown in certain regions appears to have induced localized source and p-GaN gate contact metal breakdown, resulting in the formation of a short circuit path between the source and gate. As shown in Fig. 6(c), defects are observed in the source contact metal, and obvious cracks are found in the gate metal contact region. From the failure analysis, the authors infer that the breakdown in these devices is mainly attributed to the hybrid drain structure of the device. The p-GaN layer structure near the drain, which is galvanically connected to the drain contact metal, injects holes into the drain access during high voltage off-state and switching events. These injected holes neutralize the electrons trapped in the vicinity of the 2DEG channel and mitigate the current collapse phenomenon usually prevalent in GaN HEMTs. The potential mechanism behind the observed drain instability could be attributed to the temperature dependence of hole injection as discussed below.

Hole injection occurs during both turn-on and turn-off transitions and can be modeled as an additional leakage component comprising short transient current pulses (I_{DP}) [38]. These pulses introduce extra power dissipation, which is primarily localized near the drain region of the lateral structure, where the electric potential is at highest. Additionally, the magnitude of I_{DP} decreases from drain towards source, as most trap-assisted recombination occurs in the drain access region. Accordingly, the additional drain-localized power dissipation concurring exclusively in HDGITs can be expressed as:

$$P_{\text{drain,holes}} = F_{\text{sw}} \times \int V_{\text{DS}} \times I_{\text{DP}} \times dt \quad (1)$$

Under normal operating conditions, this dissipation is mitigated by incorporating intentionally carbon-doped buffer traps that suppress I_{DP} . However, when operated beyond the rated temperature, as in the conducted experiments, thermally activated

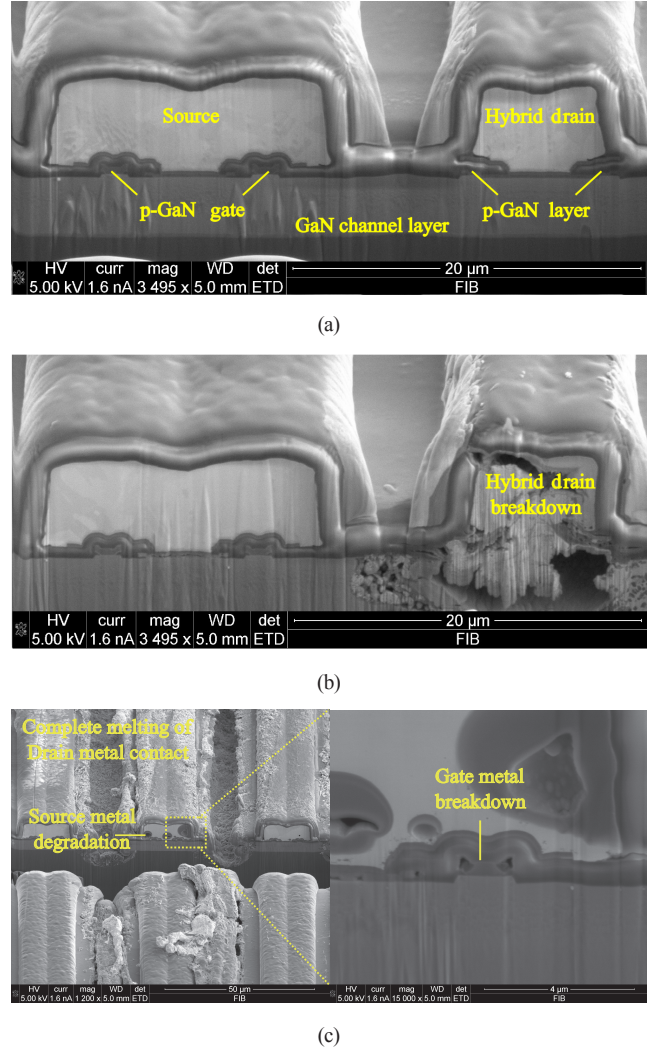


Fig. 6. SEM images of the device cross section. (a) Intact device structure from an unaffected area. (b) Hybrid drain breakdown. (c) Induced source and gate metal breakdown.

emission from the p-GaN region becomes dominant, rendering hole injection strongly temperature dependent. This behavior can be approximately described using a Richardson–Dushman type thermionic model as:

$$I_{\text{DP}} = A_p T_e^{2-q\phi_B/kT} \quad (2)$$

where A_p is the Richardson constant for holes, T is the temperature, k is the Boltzmann constant, and ϕ_B is the Barrier height between p-GaN region and the 2DEG.

Therefore, the drain-localized power dissipation associated with hole injection exhibits a strong temperature dependence and can be expressed by combining (1) and (2).

$$P_{\text{drain,holes}} \propto V_{\text{DS}} \times F_{\text{sw}} \times T_e^{2-q\phi_B/kT} \quad (3)$$

The increased power dissipation at the drain, particularly under high frequency and high temperature environment as in the study, leads to localized self-heating in this region. The resulting hot spots promote defect generation, which modifies

local electric field crowding and further intensifies the hot spots. This establishes a positive electro-thermal feedback loop, and over time the cumulative damage at the drain reaches a critical level, culminating in thermal runaway and structural failure of the drain metal as observed.

In addition to the catastrophic failure caused by the breakdown of the hybrid drain, the HD-GITs exhibited an exponential increase in leakage current, as discussed in the previous section. This behavior is consistent with the findings reported in [39], where HD-GITs were subjected to power cycling tests. According to the referenced study, this phenomenon arises from gate metal degradation induced by electromigration between the drain and source. Under high temperature and high-electric-field conditions, the increased electron flow transfers momentum to metal atoms within the gate interconnects and contacts, leading to their displacement and gradual structural damage. The resulting metallurgical degradation ultimately facilitates the formation of leakage paths near the gate region through trap-assisted tunneling, contributing to the observed rise in leakage current. It is also observed that the gradual rise in leakage current is less pronounced in Schottky p-gate devices. This can be attributed to the inherently higher gate leakage in GIT gate structures compared to their Schottky counterparts, which reduces the susceptibility to electromigration-induced degradation. In addition, the type of gate metal employed in each device category might also have influenced the extent of electromigration and its associated impact on leakage characteristics.

Out of the ten SP-HEMT samples tested from two vendors, only one experienced catastrophic breakdown, indicating that SP-HEMTs are generally more resilient to high temperature applications compared to HD-GITs. However, three samples exhibited a soft breakdown mechanism, characterized by an abnormal increase in drain leakage current at high blocking voltages. Similar types of failures have also been reported in [40] and [41], where the devices were subjected to power-cycling tests. The underlying root causes could arise from several mechanisms, including hot-electron-induced trap generation, drain side gate-edge degradation, or the formation of leakage paths between the buffer and substrate. The employed microscopy in this work may not be sufficient to identify some of these failure modes, and therefore, a detailed root cause investigation lies beyond the scope of this article and will require further study. Although this increased leakage could eventually shorten device lifetime, its impact on system performance is not as immediate or severe as catastrophic failure. This is demonstrated by successfully operating one of the affected samples for an additional 40 h under the same conditions.

All tested cascade devices demonstrated stable parameter retention throughout the 1000-h evaluation period. This result is not particularly surprising, given the absence of a p-GaN structure in the GaN chip, which helps minimize hetero structure-related instabilities. Additionally, the gate drive utilizes a Si FET, a mature technology with decades of development and refinement, further contributing to the device's reliability.

V. CONCLUSION

In this work, the authors comprehensively evaluate the parameter degradation and robustness of different commercial GaN HEMT architectures when deployed in high temperature applications. An application relevant to the test profile has been chosen for this investigation, which subjects DUTs to dynamic stress conditions. To facilitate this, a highly scalable test bench was developed, which subjects the DUTs to stress similar to that experienced by a practical flyback converter at a very high frequency for the applied voltage level at an elevated case temperature of 185 °C. Using the developed stress profile, multiple device samples from three different GaN architectures were subjected to an exhaustive test duration of up to 1000 h.

The results of the experiment performed showed that HD-GITs are more vulnerable in these environments, with all of the tested samples failing before the end of the test duration. The post failure studies performed on a failed sample indicates that the hybrid drain structure of the HDGITs are a region of weakness under these conditions. The increased hole injection forms the p-GaN region at an elevated temperature, which forms a positive electrothermal feedback effect resulting in the eventual failure of the structure to thermal runaway. In addition, another type of degradation involving the gate of the devices was also observed in HDGITs, increasing leakage current. However, this might not be as severe as the former, as it could be mitigated by using specialized gate drivers for GITs that reduces the leakage current at steady state at the expense of increased cost and component count. The tested Schottky gate devices exhibited better robustness and parameter stability relative to HDGITs. However, a few of the tested samples showed a soft breakdown type of failure with increased leakage current. Unfortunately, we don't have enough data to claim that this type of failures is exclusive to the Schottky p-GaN gate structures alone. The cascode devices gave the best result of all tested types with zero failures or significant parameter shifts throughout the test duration. The reason could be mainly because of the absence of p-GaN layer growth, and the use of Si FET based driver techniques employed. Though the cascode device offers better reliability, it is not a pure GaN power transistor. The addition of a separate Si die takes away some of the benefits in terms of switching speed and FOM. It possesses a slightly higher input and output capacitance as well as an increased threshold voltage as compared to E-mode GaN devices. These factors can limit system power density and efficiency, so device selection should align with application criticality.

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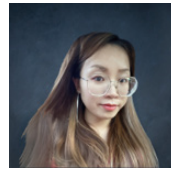
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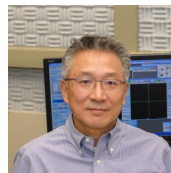
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